Lab 7

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1. Topic: Divider

- Task: 4-bit divisor and dividend

2. Code:

a) Code:

```
module divider_4bit(btn, dividend, divisor, quotient, remainder, error_LED);
    input btn;
    input [3:0] dividend, divisor;
    output reg [3:0] quotient, remainder;
    output reg error_LED;
    integer idx;

    always@(posedge btn) begin
        if (divisor == 0) begin
            quotient <= 4'b0;
            remainder <= 4'b0;
            error_LED <= 1;
        end else begin
            error_LED <= 0;
            for (idx=0; idx<16; idx=idx+1) begin
                if (dividend >= idx * divisor) begin
                    quotient <= idx;
                    remainder <= dividend - idx * divisor;
                end
            end
        end
    end
endmodule
```

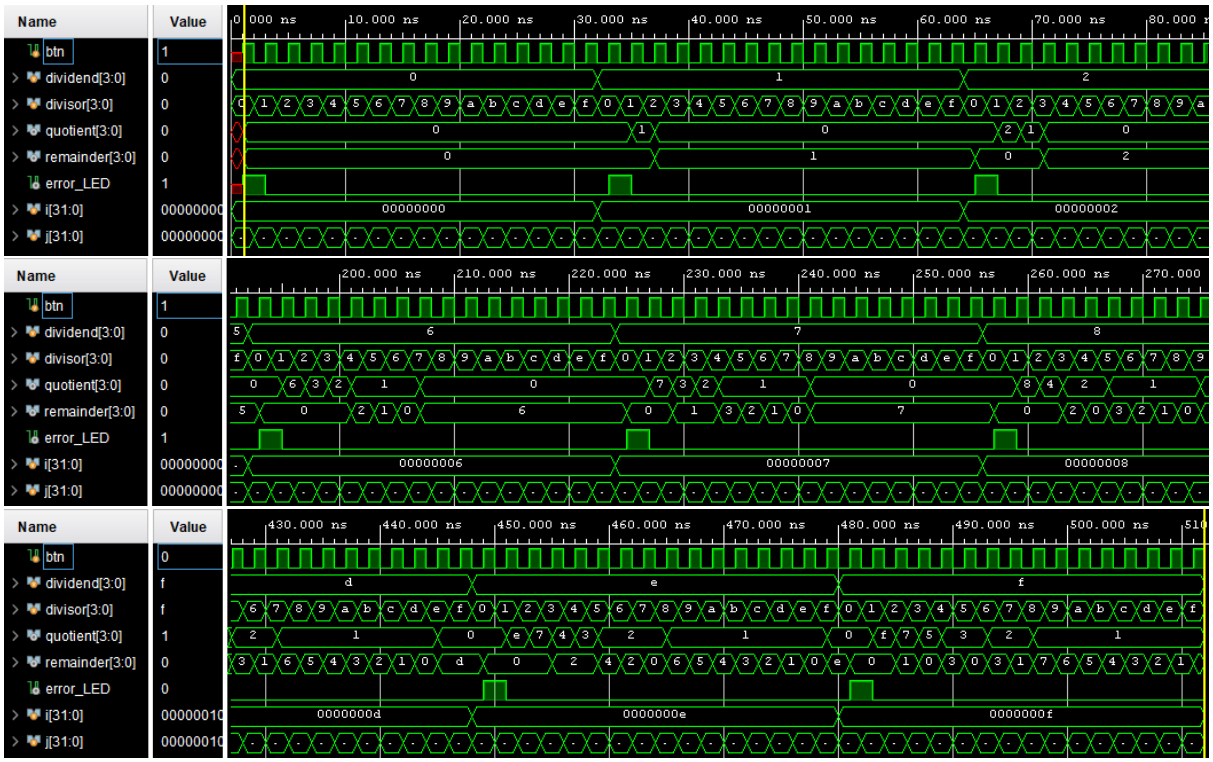
b) Test Bench:

```
module tb_divider_4bit;
// Inputs
    reg btn;
    reg [3:0] dividend, divisor;
    wire [3:0] quotient, remainder;
    wire error_LED;

    integer i, j;

    // Initial the Unit Under Test
    divider_4bit uut(btn, dividend, divisor, quotient, remainder, error_LED);
    initial begin
        for (i=0; i<16; i=i+1) begin
            for (j=0; j<16; j=j+1) begin
                dividend = i;
                divisor = j;
                #1 btn = 1;
                #1 btn = 0;
            end
        end
        $finish;
    end
endmodule
```

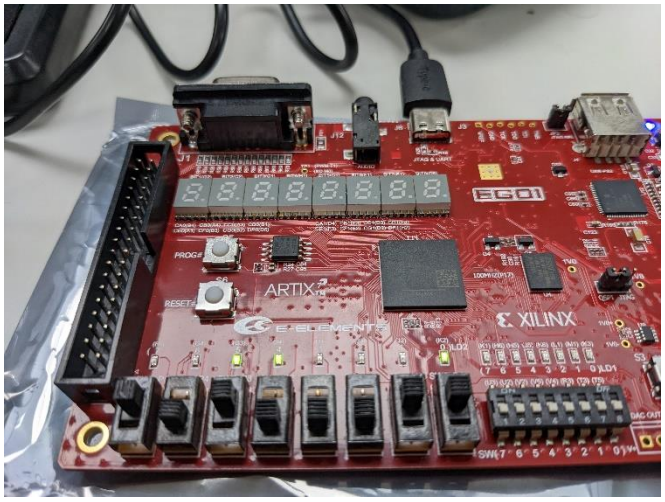
3. Simulation Waveforms:



4. FPGA Results:

Trying to divide by 0,
ERROR.

12 // 5 = 2
12 % 5 = 2



10 // 3 = 3
10 % 3 = 1

12 // 3 = 4
12 % 3 = 0

5. Reflection:

This was the last lab of the semester. It was pretty easy compared to the previous two labs. And from the results we can see that the lab went as expected.