Laboratory Report # 1

Name: German E Felisarta III **Group Number:** Group 3

Laboratory Exercise Title: Design Flow of Digital Systems **Date Completed:**

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.
CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 1A:

The goal of this is exercise is to set up a project in Quartus. To create a new project, the “new project wizard” should be clicked. When a prompt window appears, click Next. In the next prompt, you can set your project destination folder and the project name, it will be called “LightControl.” After clicking next, “Empty Project” is selected and then the next button is clicked again two times because additional files are not needed. In the Family, Device, and Board Settings, the Family selected should be MAX10, and the board should be the model, 10M50DAF484C7G. The next button will then be clicked two times again because EDA tools settings do not need to be changed. When the summary pops up, the information was reviewed and then the Finish Button was clicked.

Exercise 1B:

The goal of this exercise is to form a basic circuit using a Verilog HDL file. To create a Verilog HDL file (.v), in the menu bar, FILE>NEW is pressed and the Verilog HDL file should be selected. The given code should be copied in the .v file and then saved. After copying, the Analysis & Synthesis button, under the Tasks panel, should be clicked. After a while, if successful, there should be a checkmark on the left side of the button and a summary will be displayed. To view the logic diagram version of the file, open the drop-down of Analysis & Synthesis, under Netlist Viewers, select the RTL Viewer and the logic diagram should be displayed.

Exercise 1C:

In this exercise, the steps in Ex 1A and 1B are repeated but in this case, only the Verilog Design Entry is changed so that it would display a Half Adder Circuit in the RTL viewer.

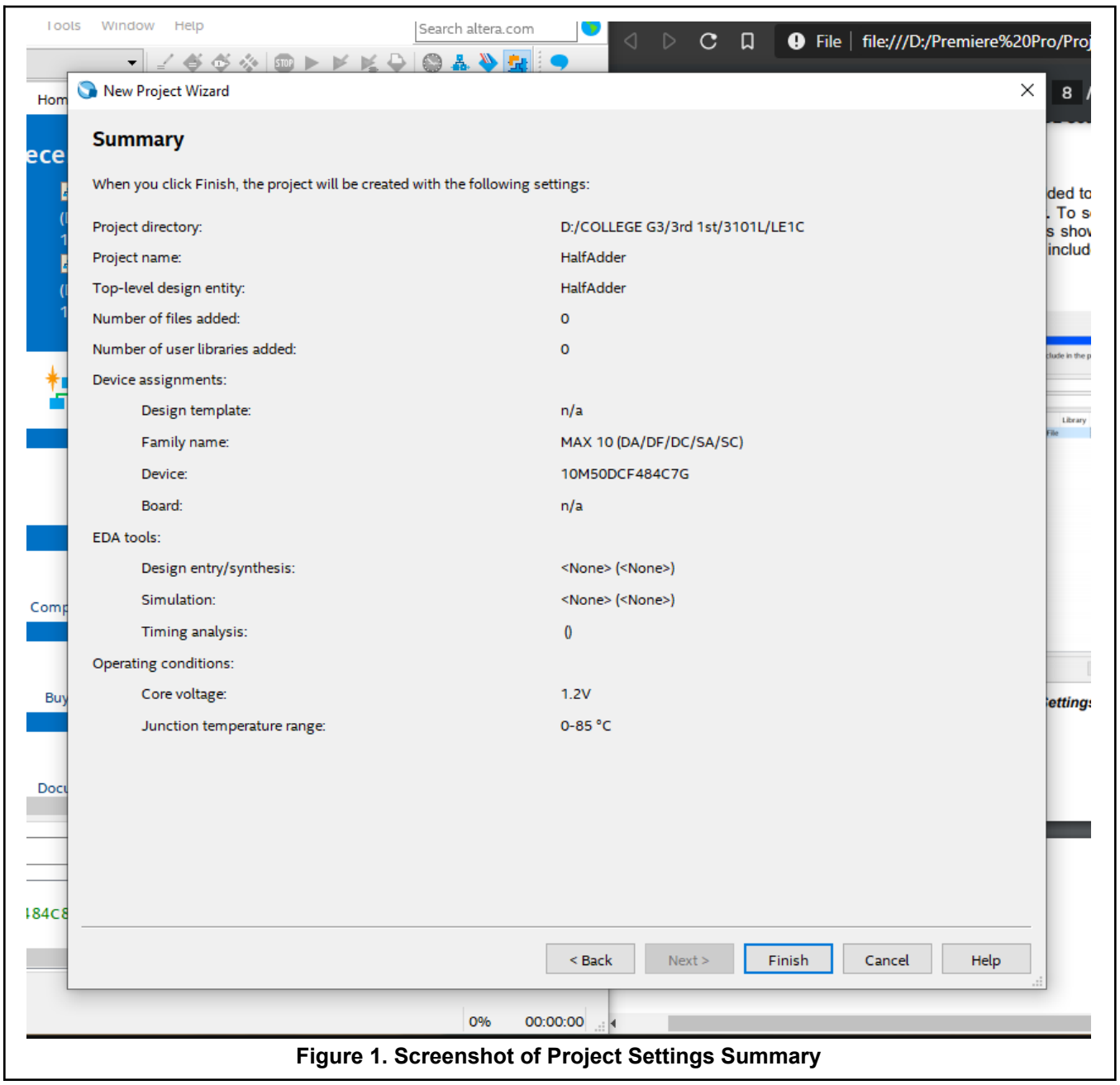
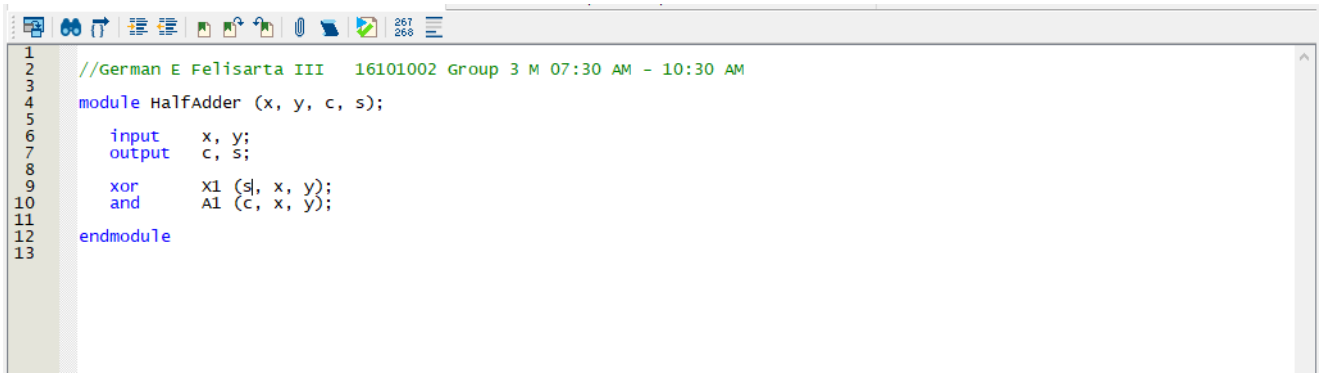


Figure 1. Screenshot of Project Settings Summary



```
1
2   //German E Felisarta III   16101002 Group 3 M 07:30 AM - 10:30 AM
3
4   module HalfAdder (x, y, c, s);
5
6       input    x, y;
7       output   c, s;
8
9       xor      X1 (s, x, y);
10      and      A1 (c, x, y);
11
12  endmodule
13
```

Figure 2. Screenshot of Verilog HDL Design Entry

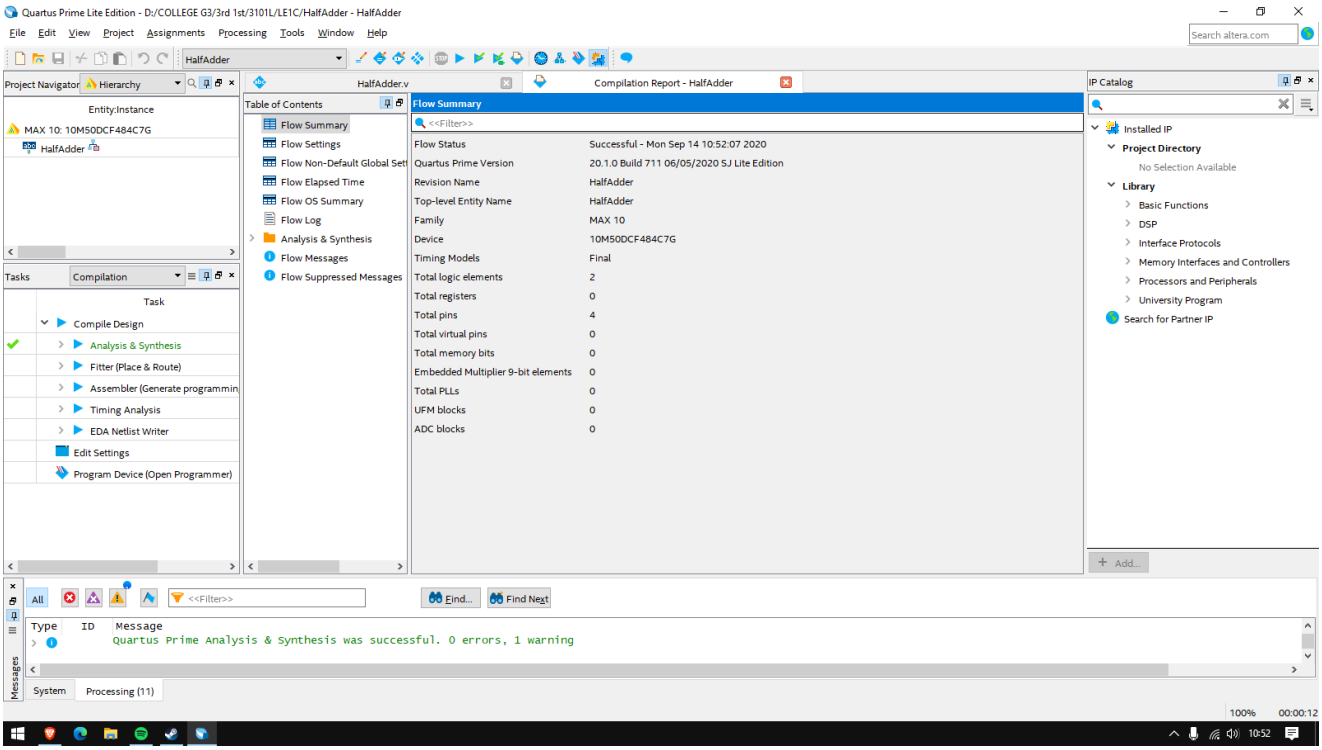


Figure 3. Screenshot of Compilation Report for the Flow Summary

There are 2 logic elements and a total of 4 pins used.

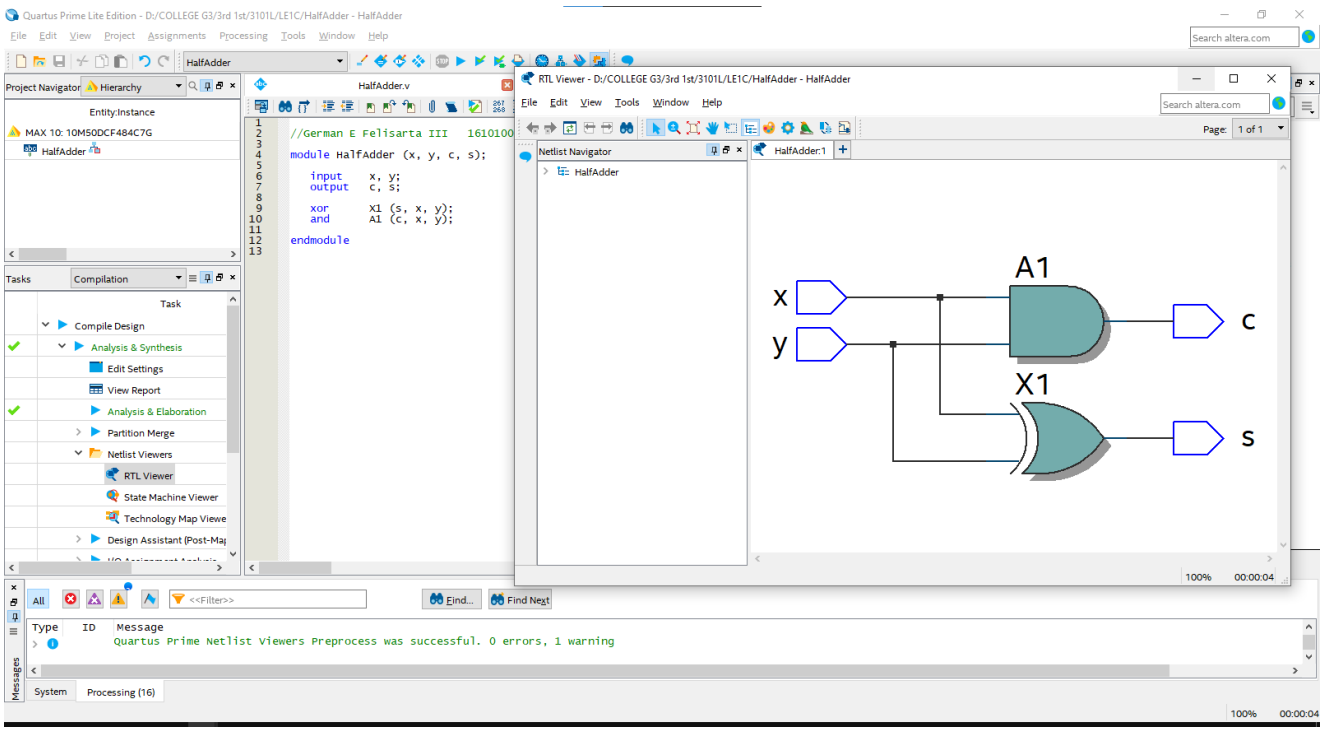


Figure 4. Screenshot of Schematic Diagram of Synthesized Circuit