

**HDL Example 4.7 FULL ADDER****Verilog**

In Verilog, *wires* are used to represent internal variables whose values are defined by `assign` statements such as `assign p = a ^ b;` Wires technically have to be declared only for multibit busses, but it is good practice to include them for all internal variables; their declaration could have been omitted in this example.

```
module fulladder(input a, b, cin,
                  output s, cout);

  wire p, g;

  assign p = a ^ b;
  assign g = a & b;

  assign s = p ^ cin;
  assign cout = g | (p & cin);
endmodule
```

**VHDL**

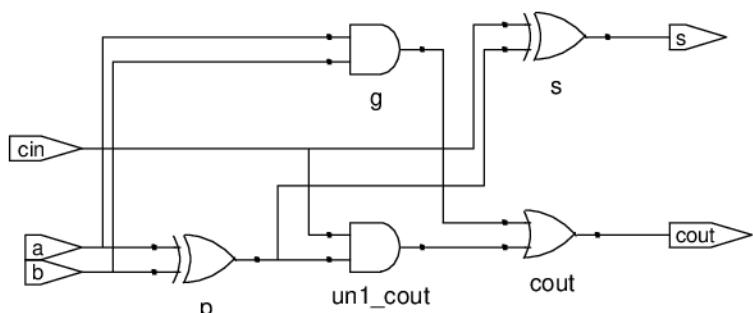
In VHDL, *signals* are used to represent internal variables whose values are defined by *concurrent signal assignment statements* such as `p <= a xor b;`

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity fulladder is
  port(a, b, cin: in STD_LOGIC;
       s, cout: out STD_LOGIC);
end;

architecture synth of fulladder is
  signal p, g: STD_LOGIC;
begin
  begin
    p <= a xor b;
    g <= a and b;

    s <= p xor cin;
    cout <= g or (p and cin);
  end;
end;
```



**Figure 4.8** fulladder **synthesized circuit**

important that  $S = P \oplus C_{in}$  comes after  $P = A \oplus B$ , because statements are executed sequentially. In an HDL, the order does not matter. Like hardware, HDL assignment statements are evaluated any time the inputs, signals on the right hand side, change their value, regardless of the order in which the assignment statements appear in a module.

#### 4.2.6 Precedence

Notice that we parenthesized the `cout` computation in HDL Example 4.7 to define the order of operations as  $C_{out} = G + (P \cdot C_{in})$ , rather than  $C_{out} = (G + P) \cdot C_{in}$ . If we had not used parentheses, the default operation order is defined by the language. HDL Example 4.8 specifies operator precedence from highest to lowest for each language. The tables include arithmetic, shift, and comparison operators that will be defined in Chapter 5.

**HDL Example 4.8 OPERATOR PRECEDENCE****Verilog****Table 4.1 Verilog operator precedence**

Op	Meaning
H	~ NOT
i	*
g	/, % MUL, DIV, MOD
h	+, - PLUS, MINUS
e	<<, >> Logical Left/Right Shift
s	<<<, >>> Arithmetic Left/Right Shift
t	<, <=, >, >= Relative Comparison
	==, != Equality Comparison
L	&, ~& AND, NAND
o	
w	^, ~^ XOR, XNOR
e	
s	, ~  OR, NOR
t	? Conditional

The operator precedence for Verilog is much like you would expect in other programming languages. In particular, AND has precedence over OR. We could take advantage of this precedence to eliminate the parentheses.

```
assign cout = g | p & cin;
```

**VHDL****Table 4.2 VHDL operator precedence**

Op	Meaning
H	not NOT
i	*
g	/, mod, rem MUL, DIV, MOD, REM
h	+, -, & PLUS, MINUS, CONCATENATE
e	
s	rol, ror, srl, sll, sra, sla Rotate, Shift logical, Shift arithmetic
t	=, /=, <, <=, >, >= Comparison
L	
o	
w	
e	and, or, nand, nor, xor Logical Operations
s	
t	

Multiplication has precedence over addition in VHDL, as you would expect. However, unlike Verilog, all of the logical operations (and, or, etc.) have equal precedence, unlike what one might expect in Boolean algebra. Thus, parentheses are necessary; otherwise cout <= g or p and cin would be interpreted from left to right as cout <= (g or p) and cin.

**4.2.7 Numbers**

Numbers can be specified in a variety of bases. Underscores in numbers are ignored and can be helpful in breaking long numbers into more readable chunks. HDL Example 4.9 explains how numbers are written in each language.

**4.2.8 Z's and X's**

HDLs use *z* to indicate a floating value. *z* is particularly useful for describing a tristate buffer, whose output floats when the enable is 0. Recall from Section 2.6 that a bus can be driven by several tristate buffers, exactly one of which should be enabled. HDL Example 4.10 shows the idiom for a tristate buffer. If the buffer is enabled, the output is the same as the input. If the buffer is disabled, the output is assigned a floating value (*z*).

**HDL Example 4.9 NUMBERS****Verilog**

Verilog numbers can specify their base and size (the number of bits used to represent them). The format for declaring constants is  $N'B\text{value}$ , where  $N$  is the size in bits,  $B$  is the base, and  $\text{value}$  gives the value. For example  $9'h25$  indicates a 9-bit number with a value of  $25_{16} = 37_{10} = 000100101_2$ . Verilog supports ' $b$ ' for binary (base 2), ' $o$ ' for octal (base 8), ' $d$ ' for decimal (base 10), and ' $h$ ' for hexadecimal (base 16). If the base is omitted, the base defaults to decimal.

If the size is not given, the number is assumed to have as many bits as the expression in which it is being used. Zeros are automatically padded on the front of the number to bring it up to full size. For example, if  $w$  is a 6-bit bus, assign  $w = 'b11$  gives  $w$  the value 000011. It is better practice to explicitly give the size.

**Table 4.3 Verilog numbers**

Numbers	Bits	Base	Val	Stored
3'b101	3	2	5	101
'b11	?	2	3	000 ... 0011
8'b11	8	2	3	00000011
8'b1010_1011	8	2	171	10101011
3'd6	3	10	6	110
6'o42	6	8	34	100010
8'hAB	8	16	171	10101011
42	?	10	42	00 ... 0101010

**VHDL**

In VHDL, STD\_LOGIC numbers are written in binary and enclosed in single quotes: '0' and '1' indicate logic 0 and 1.

STD\_LOGIC\_VECTOR numbers are written in binary or hexadecimal and enclosed in double quotation marks. The base is binary by default and can be explicitly defined with the prefix  $X$  for hexadecimal or  $B$  for binary.

**Table 4.4 VHDL numbers**

Numbers	Bits	Base	Val	Stored
"101"	3	2	5	101
B"101"	3	2	5	101
X"AB"	8	16	161	10101011

**HDL Example 4.10 TRISTATE BUFFER****Verilog**

```
module tristate(input [3:0] a,
                  input en,
                  output [3:0] y);

    assign y = en ? a : 4'bz;
endmodule
```

**VHDL**

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity tristate is
    port(a: in STD_LOGIC_VECTOR(3 downto 0);
         en: in STD_LOGIC;
         y: out STD_LOGIC_VECTOR(3 downto 0));
end;

architecture synth of tristate is
begin
    y <= "ZZZZ" when en = '0' else a;
end;
```

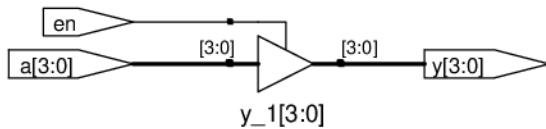


Figure 4.9 tristate synthesized circuit

Similarly, HDLs use  $x$  to indicate an invalid logic level. If a bus is simultaneously driven to 0 and 1 by two enabled tristate buffers (or other gates), the result is  $x$ , indicating contention. If all the tristate buffers driving a bus are simultaneously OFF, the bus will float, indicated by  $z$ .

At the start of simulation, state nodes such as flip-flop outputs are initialized to an unknown state ( $x$  in Verilog and  $u$  in VHDL). This is helpful to track errors caused by forgetting to reset a flip-flop before its output is used.

If a gate receives a floating input, it may produce an  $x$  output when it can't determine the correct output value. Similarly, if it receives an illegal or uninitialized input, it may produce an  $x$  output. HDL Example 4.11 shows how Verilog and VHDL combine these different signal values in logic gates.

#### HDL Example 4.11 TRUTH TABLES WITH UNDEFINED AND FLOATING INPUTS

##### Verilog

Verilog signal values are 0, 1,  $z$ , and  $x$ . Verilog constants starting with  $z$  or  $x$  are padded with leading  $z$ 's or  $x$ 's (instead of 0's) to reach their full length when necessary.

Table 4.5 shows a truth table for an AND gate using all four possible signal values. Note that the gate can sometimes determine the output despite some inputs being unknown. For example 0 &  $z$  returns 0 because the output of an AND gate is always 0 if either input is 0. Otherwise, floating or invalid inputs cause invalid outputs, displayed as  $x$  in Verilog or invalid inputs cause invalid outputs, displayed as  $x$  in Verilog.

Table 4.5 Verilog AND gate truth table with  $z$  and  $x$ 

&		0	1	A	$z$	$x$
		0	0	0	0	0
		1	0	1	$x$	$x$
		$z$	0	$x$	$x$	$x$
		$x$	0	$x$	$x$	$x$

##### VHDL

VHDL STD\_LOGIC signals are '0', '1', 'z', 'x', and 'u'.

Table 4.6 shows a truth table for an AND gate using all five possible signal values. Notice that the gate can sometimes determine the output despite some inputs being unknown. For example, '0' and 'z' returns '0' because the output of an AND gate is always '0' if either input is '0.' Otherwise, floating or invalid inputs cause invalid outputs, displayed as ' $x$ ' in VHDL. Uninitialized inputs cause uninitialized outputs, displayed as ' $u$ ' in VHDL.

Table 4.6 VHDL AND gate truth table with  $z$ ,  $x$ , and  $u$ 

AND		0	1	A	$z$	$x$	$u$
		0	0	0	0	0	0
		1	0	1	$x$	$x$	$u$
		$z$	0	$x$	$x$	$x$	$u$
		$x$	0	$x$	$x$	$x$	$u$
		$u$	0	$u$	$u$	$u$	$u$

**HDL Example 4.12 BIT SWIZZLING****Verilog**

```
assign y = {c[2:1], {3{d[0]}}, c[0], 3'b101};
```

The {} operator is used to concatenate busses. {3{d[0]}} indicates three copies of d[0].

Don't confuse the 3-bit binary constant 3'b101 with a bus named b. Note that it was critical to specify the length of 3 bits in the constant; otherwise, it would have had an unknown number of leading zeros that might appear in the middle of y.

If y were wider than 9 bits, zeros would be placed in the most significant bits.

**VHDL**

```
y <= c(2 downto 1) & d(0) & d(0) & d(0) & c(0) & "101";
```

The & operator is used to concatenate busses. y must be a 9-bit STD\_LOGIC\_VECTOR. Do not confuse & with the and operator in VHDL.

Seeing x or u values in simulation is almost always an indication of a bug or bad coding practice. In the synthesized circuit, this corresponds to a floating gate input, uninitialized state, or contention. The x or u may be interpreted randomly by the circuit as 0 or 1, leading to unpredictable behavior.

**4.2.9 Bit Swizzling**

Often it is necessary to operate on a subset of a bus or to concatenate (join together) signals to form busses. These operations are collectively known as *bit swizzling*. In HDL Example 4.12, y is given the 9-bit value c<sub>2</sub>c<sub>1</sub>d<sub>0</sub>d<sub>0</sub>c<sub>0</sub>101 using bit swizzling operations.

**4.2.10 Delays**

HDL statements may be associated with delays specified in arbitrary units. They are helpful during simulation to predict how fast a circuit will work (if you specify meaningful delays) and also for debugging purposes to understand cause and effect (deducing the source of a bad output is tricky if all signals change simultaneously in the simulation results). These delays are ignored during synthesis; the delay of a gate produced by the synthesizer depends on its  $t_{pd}$  and  $t_{cd}$  specifications, not on numbers in HDL code.

HDL Example 4.13 adds delays to the original function from HDL Example 4.1,  $y = \bar{a}\bar{b}\bar{c} + a\bar{b}\bar{c} + a\bar{b}c$ . It assumes that inverters have a delay of 1 ns, three-input AND gates have a delay of 2 ns, and three-input OR gates have a delay of 4 ns. Figure 4.10 shows the simulation waveforms, with y lagging 7 ns after the inputs. Note that y is initially unknown at the beginning of the simulation.

**HDL Example 4.13 LOGIC GATES WITH DELAYS****Verilog**

```
'timescale 1ns/1ps

module example(input a, b, c,
                output y);
    wire ab, bb, cb, n1, n2, n3;

    assign #1 {ab, bb, cb} = ~{a, b, c};
    assign #2 n1 = ab & bb & cb;
    assign #2 n2 = a & bb & cb;
    assign #2 n3 = a & bb & c;
    assign #4 y = n1 | n2 | n3;
endmodule
```

Verilog files can include a timescale directive that indicates the value of each time unit. The statement is of the form ‘timescale unit/precision. In this file, each unit is 1 ns, and the simulation has 1 ps precision. If no timescale directive is given in the file, a default unit and precision (usually 1 ns for both) is used. In Verilog, a # symbol is used to indicate the number of units of delay. It can be placed in assign statements, as well as non-blocking ( $<=$ ) and blocking ( $=$ ) assignments, which will be discussed in Section 4.5.4.

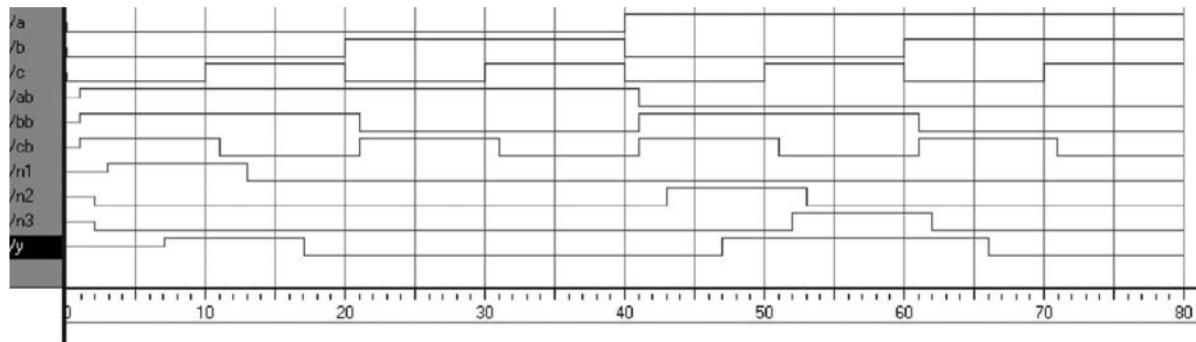
**VHDL**

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity example is
    port(a, b, c: in STD_LOGIC;
         y:        out STD_LOGIC);
end;

architecture synth of example is
begin
    ab <= not a after 1 ns;
    bb <= not b after 1 ns;
    cb <= not c after 1 ns;
    n1 <= ab and bb and cb after 2 ns;
    n2 <= a and bb and cb after 2 ns;
    n3 <= a and bb and c after 2 ns;
    y <= n1 or n2 or n3 after 4 ns;
end;
```

In VHDL, the after clause is used to indicate delay. The units, in this case, are specified as nanoseconds.



**Figure 4.10** Example simulation waveforms with delays (from the ModelSim simulator)

**4.2.11 VHDL Libraries and Types\***

(This section may be skipped by Verilog users.) Unlike Verilog, VHDL enforces a strict data typing system that can protect the user from some errors but that is also clumsy at times.

Despite its fundamental importance, the STD\_LOGIC type is not built into VHDL. Instead, it is part of the IEEE.STD\_LOGIC\_1164 library. Thus, every file must contain the library statements shown in the previous examples.

Moreover, IEEE.STD\_LOGIC\_1164 lacks basic operations such as addition, comparison, shifts, and conversion to integers for the STD\_LOGIC\_VECTOR data. Most CAD vendors have adopted yet more libraries containing these functions: IEEE.STD\_LOGIC\_UNSIGNED and IEEE.STD\_LOGIC\_SIGNED. See Section 1.4 for a discussion of unsigned and signed numbers and examples of these operations.

VHDL also has a BOOLEAN type with two values: true and false. BOOLEAN values are returned by comparisons (such as the equality comparison,  $s = '0'$ ) and are used in conditional statements such as when. Despite the temptation to believe a BOOLEAN true value should be equivalent to a STD\_LOGIC '1' and BOOLEAN false should mean STD\_LOGIC '0', these types are not interchangeable. Thus, the following code is illegal:

```
y <= d1 when s else d0;
q <= (state = S2);
```

Instead, we must write

```
y <= d1 when (s = '1') else d0;
q <= '1' when (state = S2) else '0';
```

Although we do not declare any signals to be BOOLEAN, they are automatically implied by comparisons and used by conditional statements.

Similarly, VHDL has an INTEGER type that represents both positive and negative integers. Signals of type INTEGER span at least the values  $-2^{31}$  to  $2^{31} - 1$ . Integer values are used as indices of busses. For example, in the statement

```
y <= a(3) and a(2) and a(1) and a(0);
```

0, 1, 2, and 3 are integers serving as an index to choose bits of the a signal. We cannot directly index a bus with a STD\_LOGIC or STD\_LOGIC\_VECTOR signal. Instead, we must convert the signal to an INTEGER. This is demonstrated in HDL Example 4.14 for an 8:1 multiplexer that selects one bit from a vector using a 3-bit index. The CONV\_INTEGER function is defined in the IEEE.STD\_LOGIC\_UNSIGNED library and performs the conversion from STD\_LOGIC\_VECTOR to INTEGER for positive (unsigned) values.

VHDL is also strict about out ports being exclusively for output. For example, the following code for two and three-input AND gates is illegal VHDL because v is an output and is also used to compute w.

```
library IEEE; use IEEE.STD_LOGIC_1164.all;
entity and23 is
    port(a, b, c: in STD_LOGIC;
         v, w:     out STD_LOGIC);
end;
```

**HDL Example 4.14** 8:1 MULTIPLEXER WITH TYPE CONVERSION

```

library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_UNSIGNED.all;

entity mux8 is
    port(d: in STD_LOGIC_VECTOR(7 downto 0);
         s: in STD_LOGIC_VECTOR(2 downto 0);
         y: out STD_LOGIC);
end;

architecture synth of mux8 is
begin
    y <= d(CONV_INTEGER(s));
end;

```

Figure follows on next page.

```

architecture synth of and23 is
begin
    v <= a and b;
    w <= v and c;
end;

```

VHDL defines a special port type, buffer, to solve this problem. A signal connected to a buffer port behaves as an output but may also be used within the module. The corrected entity definition follows. Verilog does not have this limitation and does not require buffer ports.

```

entity and23 is
    port(a, b, c: in STD_LOGIC;
         v: buffer STD_LOGIC;
         w: out STD_LOGIC);
end;

```

VHDL supports *enumeration* types as an abstract way of representing information without assigning specific binary encodings. For example, the divide-by-3 FSM described in Section 3.4.2 uses three states. We can give the states names using the enumeration type rather than referring to them by binary values. This is powerful because it allows VHDL to search for the best state encoding during synthesis, rather than depending on an arbitrary encoding specified by the user.

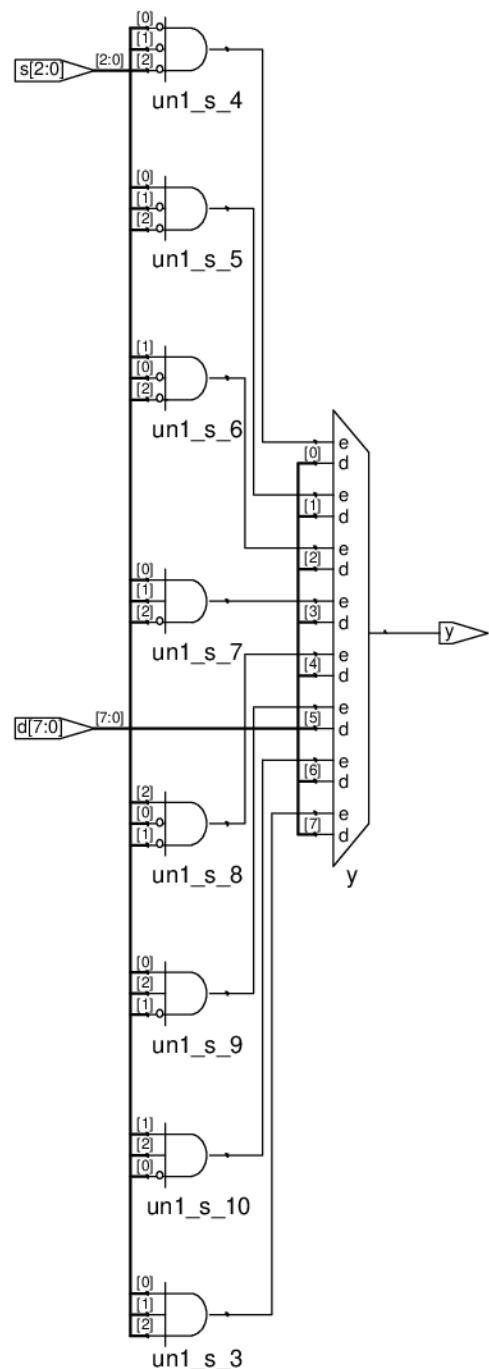
```

type statetype is (S0, S1, S2);
signal state, nextstate: statetype;

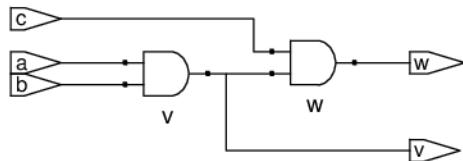
```

### 4.3 STRUCTURAL MODELING

The previous section discussed *behavioral* modeling, describing a module in terms of the relationships between inputs and outputs. This section



**Figure 4.11** mux8 synthesized circuit



**Figure 4.12** and23 synthesized circuit

examines *structural* modeling, describing a module in terms of how it is composed of simpler modules.

For example, HDL Example 4.15 shows how to assemble a 4:1 multiplexer from three 2:1 multiplexers. Each copy of the 2:1 multiplexer

#### HDL Example 4.15 STRUCTURAL MODEL OF 4:1 MULTIPLEXER

##### Verilog

```
module mux4 (input [3:0] d0, d1, d2, d3,
              input [1:0] s,
              output [3:0] y);

    wire [3:0] low, high;

    mux2 lowmux (d0, d1, s[0], low);
    mux2 highmux (d2, d3, s[0], high);
    mux2 finalmux (low, high, s[1], y);
endmodule
```

The three `mux2` instances are called `lowmux`, `highmux`, and `finalmux`. The `mux2` module must be defined elsewhere in the Verilog code.

##### VHDL

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity mux4 is
    port(d0, d1,
          d2, d3: in STD_LOGIC_VECTOR(3 downto 0);
          s: in STD_LOGIC_VECTOR(1 downto 0);
          y: out STD_LOGIC_VECTOR(3 downto 0));
end;

architecture struct of mux4 is
    component mux2
        port(d0,
              d1: in STD_LOGIC_VECTOR(3 downto 0);
              s: in STD_LOGIC;
              y: out STD_LOGIC_VECTOR(3 downto 0));
    end component;
    signal low, high: STD_LOGIC_VECTOR(3 downto 0);
begin
    lowmux: mux2 port map(d0, d1, s(0), low);
    highmux: mux2 port map(d2, d3, s(0), high);
    finalmux: mux2 port map(low, high, s(1), y);
end;
```

The architecture must first declare the `mux2` ports using the component declaration statement. This allows VHDL tools to check that the component you wish to use has the same ports as the entity that was declared somewhere else in another entity statement, preventing errors caused by changing the entity but not the instance. However, component declaration makes VHDL code rather cumbersome.

Note that this architecture of `mux4` was named `struct`, whereas architectures of modules with behavioral descriptions from Section 4.2 were named `synth`. VHDL allows multiple architectures (implementations) for the same entity; the architectures are distinguished by name. The names themselves have no significance to the CAD tools, but `struct` and `synth` are common. Synthesizable VHDL code generally contains only one architecture for each entity, so we will not discuss the VHDL syntax to configure which architecture is used when multiple architectures are defined.

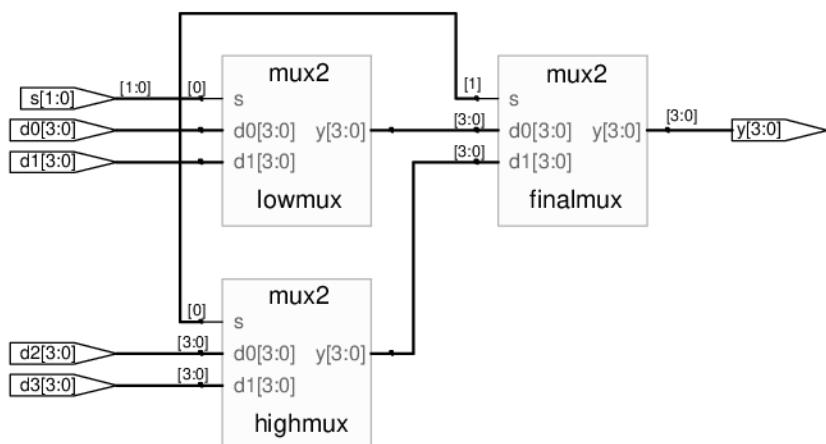


Figure 4.13 mux4 synthesized circuit

is called an *instance*. Multiple instances of the same module are distinguished by distinct names, in this case `lowmux`, `highmux`, and `finalmux`. This is an example of regularity, in which the 2:1 multiplexer is reused many times.

HDL Example 4.16 uses structural modeling to construct a 2:1 multiplexer from a pair of tristate buffers.

#### HDL Example 4.16 STRUCTURAL MODEL OF 2:1 MULTIPLEXER

##### Verilog

```
module mux2(input [3:0] d0, d1,
             input s,
             output [3:0] y);
  tristate t0(d0, ~s, y);
  tristate t1(d1, s, y);
endmodule
```

In Verilog, expressions such as `~s` are permitted in the port list for an instance. Arbitrarily complicated expressions are legal but discouraged because they make the code difficult to read.

##### VHDL

```
library IEEE; use IEEE.STD_LOGIC_1164.all;
entity mux2 is
  port (d0, d1: in STD_LOGIC_VECTOR(3 downto 0);
        s: in STD_LOGIC;
        y: out STD_LOGIC_VECTOR(3 downto 0));
end;

architecture struct of mux2 is
  component tristate
    port (a: in STD_LOGIC_VECTOR(3 downto 0);
          en: in STD_LOGIC;
          y: out STD_LOGIC_VECTOR(3 downto 0));
  end component;
  signal sbar: STD_LOGIC;
begin
  sbar <= not s;
  t0: tristate port map(d0, sbar, y);
  t1: tristate port map(d1, s, y);
end;
```

In VHDL, expressions such as `not s` are not permitted in the port map for an instance. Thus, `sbar` must be defined as a separate signal.

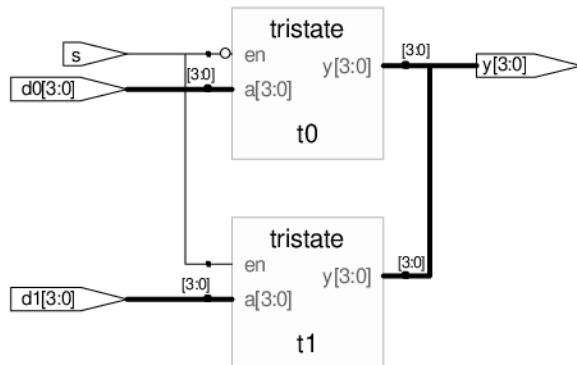


Figure 4.14 mux2 synthesized circuit

HDL Example 4.17 shows how modules can access part of a bus. An 8-bit wide 2:1 multiplexer is built using two of the 4-bit 2:1 multiplexers already defined, operating on the low and high nibbles of the byte.

In general, complex systems are designed *hierarchically*. The overall system is described structurally by instantiating its major components. Each of these components is described structurally from its building blocks, and so forth recursively until the pieces are simple enough to describe behaviorally. It is good style to avoid (or at least to minimize) mixing structural and behavioral descriptions within a single module.

#### HDL Example 4.17 ACCESSING PARTS OF BUSSES

##### Verilog

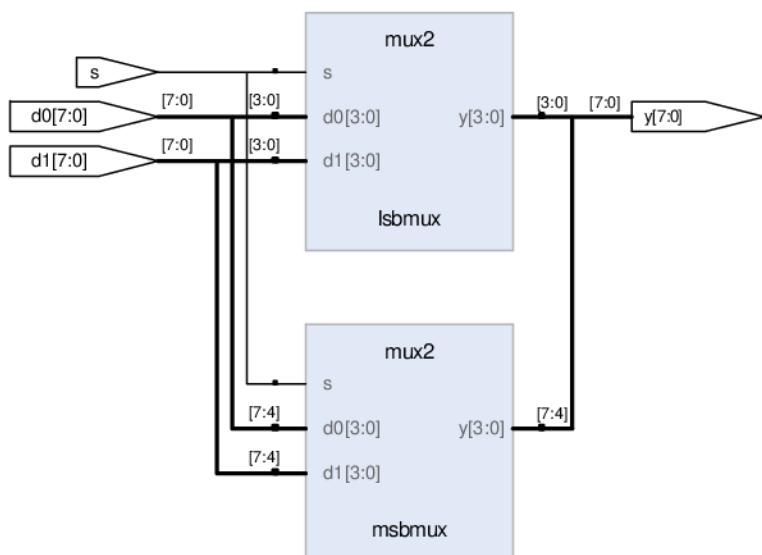
```
module mux2_8 (input [7:0] d0, d1,
               input s,
               output [7:0] y);

  mux2 lsbmux (d0[3:0], d1[3:0], s, y[3:0]);
  mux2 msbmux (d0[7:4], d1[7:4], s, y[7:4]);
endmodule
```

##### VHDL

```
library IEEE; use IEEE.STD_LOGIC_1164.all;
entity mux2_8 is
  port(d0, d1: in STD_LOGIC_VECTOR(7 downto 0);
       s:      in STD_LOGIC;
       y:      out STD_LOGIC_VECTOR(7 downto 0));
end;

architecture struct of mux2_8 is
  component mux2
    port(d0, d1: in STD_LOGIC_VECTOR(3
                                         downto 0);
         s:      in STD_LOGIC;
         y:      out STD_LOGIC_VECTOR(3 downto 0));
  end component;
begin
  lsbmux: mux2
    port map(d0(3 downto 0), d1(3 downto 0),
              s, y(3 downto 0));
  msbmux: mux2
    port map(d0(7 downto 4), d1(7 downto 4),
              s, y(7 downto 4));
end;
```



**Figure 4.15** mux2\_8 synthesized circuit

## 4.4 SEQUENTIAL LOGIC

HDL synthesizers recognize certain idioms and turn them into specific sequential circuits. Other coding styles may simulate correctly but synthesize into circuits with blatant or subtle errors. This section presents the proper idioms to describe registers and latches.

### 4.4.1 Registers

The vast majority of modern commercial systems are built with registers using positive edge-triggered D flip-flops. HDL Example 4.18 shows the idiom for such flip-flops.

In Verilog `always` statements and VHDL process statements, signals keep their old value until an event in the sensitivity list takes place that explicitly causes them to change. Hence, such code, with appropriate sensitivity lists, can be used to describe sequential circuits with memory. For example, the flip-flop includes only `clk` in the sensitive list. It remembers its old value of `q` until the next rising edge of the `clk`, even if `d` changes in the interim.

In contrast, Verilog continuous assignment statements (`assign`) and VHDL concurrent assignment statements (`<=`) are reevaluated anytime any of the inputs on the right hand side changes. Therefore, such code necessarily describes combinational logic.

**HDL Example 4.18 REGISTER****Verilog**

```
module flop(input      clk,
             input [3:0] d,
             output reg [3:0] q);

    always @ (posedge clk)
        q <= d;
endmodule
```

**A Verilog always statement is written in the form**

```
always @ (sensitivity list)
    statement;
```

The statement is executed only when the event specified in the sensitivity list occurs. In this example, the statement is `q <= d` (pronounced “`q gets d`”). Hence, the flip-flop copies `d` to `q` on the positive edge of the clock and otherwise remembers the old state of `q`.

`<=` is called a *nonblocking assignment*. Think of it as a regular `=` sign for now; we'll return to the more subtle points in Section 4.5.4. Note that `<=` is used instead of `assign` inside an `always` statement.

All signals on the left hand side of `<=` or `=` in an `always` statement must be declared as `reg`. In this example, `q` is both an output and a `reg`, so it is declared as `output reg [3:0] q`. Declaring a signal as `reg` does not mean the signal is actually the output of a register! All it means is that the signal appears on the left hand side of an assignment in an `always` statement. We will see later examples of `always` statements describing combinational logic in which the output is declared `reg` but does not come from a flip-flop.

**VHDL**

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity flop is
    port(clk: in STD_LOGIC;
          d: in STD_LOGIC_VECTOR(3 downto 0);
          q: out STD_LOGIC_VECTOR(3 downto 0));
end;

architecture synth of flop is
begin
    process(clk) begin
        if clk'event and clk = '1' then
            q <= d;
        end if;
    end process;
end;
```

**A VHDL process is written in the form**

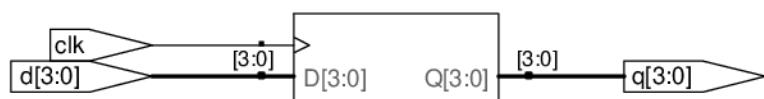
```
process(sensitivity list) begin
    statement;
end process;
```

The statement is executed when any of the variables in the sensitivity list change. In this example, the `if` statement is executed when `clk` changes, indicated by `clk'event`. If the change is a rising edge (`clk = '1'` after the event), then `q <= d` (pronounced “`q gets d`”). Hence, the flip-flop copies `d` to `q` on the positive edge of the clock and otherwise remembers the old state of `q`.

An alternative VHDL idiom for a flip-flop is

```
process(clk) begin
    if RISING_EDGE(clk) then
        q <= d;
    end if;
end process;
```

`RISING_EDGE(clk)` is synonymous with `clk'event` and `clk = 1`.



**Figure 4.16 flop synthesized circuit**

**4.4.2 Resettable Registers**

When simulation begins or power is first applied to a circuit, the output of a flop or register is unknown. This is indicated with `x` in Verilog and ‘`u`’ in VHDL. Generally, it is good practice to use resettable registers so that on powerup you can put your system in a known state. The reset may be

either asynchronous or synchronous. Recall that asynchronous reset occurs immediately, whereas synchronous reset clears the output only on the next rising edge of the clock. HDL Example 4.19 demonstrates the idioms for flip-flops with asynchronous and synchronous resets. Note that distinguishing synchronous and asynchronous reset in a schematic can be difficult. The schematic produced by Synplify Pro places asynchronous reset at the bottom of a flip-flop and synchronous reset on the left side.

#### HDL Example 4.19 RESETTABLE REGISTER

##### Verilog

```
module flopr (input      clk,
               input      reset,
               input [3:0] d,
               output reg [3:0] q);

  // asynchronous reset
  always @ (posedge clk, posedge reset)
    if (reset) q <= 4'b0;
    else       q <= d;
endmodule

module flopr (input      clk,
               input      reset,
               input [3:0] d,
               output reg [3:0] q);

  // synchronous reset
  always @ (posedge clk)
    if (reset) q <= 4'b0;
    else       q <= d;
endmodule
```

Multiple signals in an `always` statement sensitivity list are separated with a comma or the word `or`. Notice that `posedge reset` is in the sensitivity list on the asynchronously resettable flop, but not on the synchronously resettable flop. Thus, the asynchronously resettable flop immediately responds to a rising edge on `reset`, but the synchronously resettable flop responds to `reset` only on the rising edge of the clock.

Because the modules have the same name, `flopr`, you may include only one or the other in your design.

##### VHDL

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity flopr is
  port (clk,
        reset: in STD_LOGIC;
        d:    in STD_LOGIC_VECTOR(3 downto 0);
        q:    out STD_LOGIC_VECTOR(3 downto 0));
end;

architecture asynchronous of flopr is
begin
  process (clk, reset) begin
    if reset = '1' then
      q <= "0000";
    elsif clk' event and clk = '1' then
      q <= d;
    end if;
  end process;
end;

architecture synchronous of flopr is
begin
  process (clk) begin
    if clk'event and clk = '1' then
      if reset = '1' then
        q <= "0000";
      else q <= d;
      end if;
    end if;
  end process;
end;
```

Multiple signals in a process sensitivity list are separated with a comma. Notice that `reset` is in the sensitivity list on the asynchronously resettable flop, but not on the synchronously resettable flop. Thus, the asynchronously resettable flop immediately responds to a rising edge on `reset`, but the synchronously resettable flop responds to `reset` only on the rising edge of the clock.

Recall that the state of a flop is initialized to ‘u’ at startup during VHDL simulation.

As mentioned earlier, the name of the architecture (`asynchronous` or `synchronous`, in this example) is ignored by the VHDL tools but may be helpful to the human reading the code. Because both architectures describe the entity `flopr`, you may include only one or the other in your design.

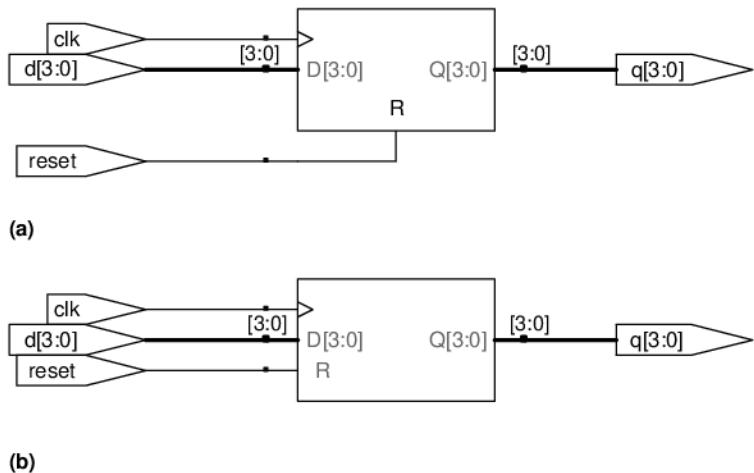


Figure 4.17 flopr synthesized circuit (a) asynchronous reset, (b) synchronous reset

#### 4.4.3 Enabled Registers

Enabled registers respond to the clock only when the enable is asserted. HDL Example 4.20 shows an asynchronously resettable enabled register that retains its old value if both reset and en are FALSE.

##### HDL Example 4.20 RESETTABLE ENABLED REGISTER

###### Verilog

```
module flopenr(input      clk,
                input      reset,
                input      en,
                input [3:0] d,
                output reg [3:0] q);

    // asynchronous reset
    always @ (posedge clk, posedge reset)
        if (reset) q <= 4'b0;
        else if(en) q <= d;
endmodule
```

###### VHDL

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity flopenr is
    port(clk,
          reset,
          en: in STD_LOGIC;
          d: in STD_LOGIC_VECTOR(3 downto 0);
          q: out STD_LOGIC_VECTOR(3 downto 0));
end;

architecture asynchronous of flopenr is
    -- asynchronous reset
begin
    process(clk, reset) begin
        if reset = '1' then
            q <= "0000";
        elsif clk'event and clk = '1' then
            if en = '1' then
                q <= d;
            end if;
        end if;
    end process;
end;
```

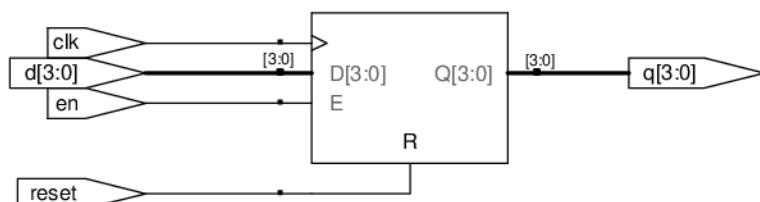


Figure 4.18 flopnr synthesized circuit

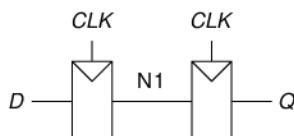


Figure 4.19 Synchronizer circuit

#### 4.4.4 Multiple Registers

A single always/process statement can be used to describe multiple pieces of hardware. For example, consider the synchronizer from Section 3.5.5 made of two back-to-back flip-flops, as shown in Figure 4.19. HDL Example 4.21 describes the synchronizer. On the rising edge of `clk`, `d` is copied to `n1`. At the same time, `n1` is copied to `q`.

#### HDL Example 4.21 SYNCHRONIZER

##### Verilog

```
module sync (input      clk,
              input      d,
              output reg q);

  reg n1;

  always @ (posedge clk)
  begin
    n1 <= d;
    q <= n1;
  end
endmodule
```

`n1` must be declared as a `reg` because it is an internal signal used on the left hand side of `<=` in an `always` statement. Also notice that the `begin/end` construct is necessary because multiple statements appear in the `always` statement. This is analogous to `{ }` in C or Java. The `begin/end` was not needed in the `flop` example because `if/else` counts as a single statement.

##### VHDL

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity sync is
  port(clk: in STD_LOGIC;
       d: in STD_LOGIC;
       q: out STD_LOGIC);
end;

architecture good of sync is
  signal n1: STD_LOGIC;
begin
  process(clk) begin
    if clk'event and clk = '1' then
      n1 <= d;
      q <= n1;
    end if;
  end process;
end;
```

`n1` must be declared as a `signal` because it is an internal signal used in the module.

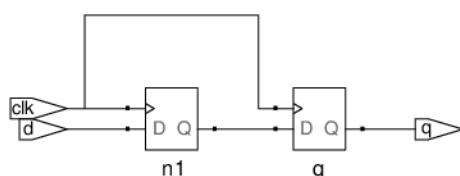


Figure 4.20 sync synthesized circuit

#### 4.4.5 Latches

Recall from Section 3.2.2 that a D latch is transparent when the clock is HIGH, allowing data to flow from input to output. The latch becomes opaque when the clock is LOW, retaining its old state. HDL Example 4.22 shows the idiom for a D latch.

Not all synthesis tools support latches well. Unless you know that your tool does support latches and you have a good reason to use them, avoid them and use edge-triggered flip-flops instead. Furthermore, take care that your HDL does not imply any unintended latches, something that is easy to do if you aren't attentive. Many synthesis tools warn you when a latch is created; if you didn't expect one, track down the bug in your HDL.

## 4.5 MORE COMBINATIONAL LOGIC

In Section 4.2, we used assignment statements to describe combinational logic behaviorally. Verilog `always` statements and VHDL process statements are used to describe sequential circuits, because they remember the old state when no new state is prescribed. However, `always/process`

#### HDL Example 4.22 D LATCH

##### Verilog

```
module latch (input      clk,
              input [3:0] d,
              output reg [3:0] q);
    always @ (clk, d)
        if (clk) q <= d;
endmodule
```

The sensitivity list contains both `clk` and `d`, so the `always` statement evaluates any time `clk` or `d` changes. If `clk` is HIGH, `d` flows through to `q`.

`q` must be declared to be a `reg` because it appears on the left hand side of `<=` in an `always` statement. This does not always mean that `q` is the output of a register.

##### VHDL

```
library IEEE; use IEEE.STD_LOGIC_1164.all;
entity latch is
    port(clk: in STD_LOGIC;
          d: in STD_LOGIC_VECTOR(3 downto 0);
          q: out STD_LOGIC_VECTOR(3 downto 0));
end;
architecture synth of latch is
begin
    process(clk, d) begin
        if clk = '1' then q <= d;
        end if;
    end process;
end;
```

The sensitivity list contains both `clk` and `d`, so the process evaluates anytime `clk` or `d` changes. If `clk` is HIGH, `d` flows through to `q`.

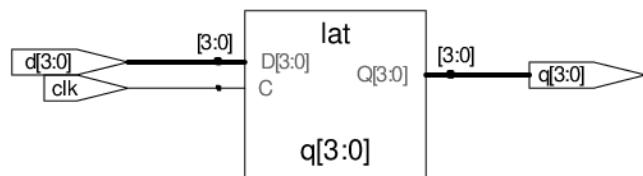


Figure 4.21 latch synthesized circuit

**HDL Example 4.23 INVERTER USING always/process****Verilog**

```
module inv(input [3:0] a,
            output reg [3:0] y);

    always @ (*)
        y = ~a;
endmodule
```

`always @ (*)` reevaluates the statements inside the `always` statement any time any of the signals on the right hand side of `<=` or `=` inside the `always` statement change. Thus, `@ (*)` is a safe way to model combinational logic. In this particular example, `@ (a)` would also have sufficed.

The `=` in the `always` statement is called a *blocking assignment*, in contrast to the `<=` nonblocking assignment. In Verilog, it is good practice to use blocking assignments for combinational logic and nonblocking assignments for sequential logic. This will be discussed further in Section 4.5.4.

Note that `y` must be declared as `reg` because it appears on the left hand side of a `<=` or `=` sign in an `always` statement. Nevertheless, `y` is the output of combinational logic, not a register.

**VHDL**

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity inv is
    port(a: in STD_LOGIC_VECTOR(3 downto 0);
         y: out STD_LOGIC_VECTOR(3 downto 0));
end;

architecture proc of inv is
begin
    process(a) begin
        y <= not a;
    end process;
end;
```

The `begin` and `end process` statements are required in VHDL even though the `process` contains only one assignment.

statements can also be used to describe combinational logic behaviorally if the sensitivity list is written to respond to changes in all of the inputs and the body prescribes the output value for every possible input combination. HDL Example 4.23 uses `always/process` statements to describe a bank of four inverters (see Figure 4.3 for the synthesized circuit).

HDLs support *blocking* and *nonblocking assignments* in an `always/process` statement. A group of blocking assignments are evaluated in the order in which they appear in the code, just as one would expect in a standard programming language. A group of nonblocking assignments are evaluated concurrently; all of the statements are evaluated before any of the signals on the left hand sides are updated.

HDL Example 4.24 defines a full adder using intermediate signals `p` and `g` to compute `s` and `cout`. It produces the same circuit from Figure 4.8, but uses `always/process` statements in place of assignment statements.

These two examples are poor applications of `always/process` statements for modeling combinational logic because they require more lines than the equivalent approach with assignment statements from Section 4.2.1. Moreover, they pose the risk of inadvertently implying sequential logic if the inputs are left out of the sensitivity list. However, `case` and `if` statements are convenient for modeling more complicated combinational logic. `case` and `if` statements must appear within `always/process` statements and are examined in the next sections.

**Verilog**

In a Verilog `always` statement, `=` indicates a blocking assignment and `<=` indicates a nonblocking assignment (also called a concurrent assignment).

Do not confuse either type with continuous assignment using the `assign` statement. `assign` statements must be used outside `always` statements and are also evaluated concurrently.

**VHDL**

In a VHDL `process` statement, `: =` indicates a blocking assignment and `<=` indicates a nonblocking assignment (also called a concurrent assignment). This is the first section where `: =` is introduced.

Nonblocking assignments are made to outputs and to signals. Blocking assignments are made to variables, which are declared in `process` statements (see HDL Example 4.24).

`<=` can also appear outside `process` statements, where it is also evaluated concurrently.

**HDL Example 4.24 FULL ADDER USING `always/process`****Verilog**

```
module fulladder(input      a, b, cin,
                  output reg s, cout);
  reg p, g;

  always @ (*)
    begin
      p = a ^ b;           // blocking
      g = a & b;           // blocking

      s = p ^ cin;        // blocking
      cout = g | (p & cin); // blocking
    end
endmodule
```

In this case, an `@ (a, b, cin)` would have been equivalent to `@ (*)`. However, `@ (*)` is better because it avoids common mistakes of missing signals in the stimulus list.

For reasons that will be discussed in Section 4.5.4, it is best to use blocking assignments for combinational logic. This example uses blocking assignments, first computing `p`, then `g`, then `s`, and finally `cout`.

Because `p` and `g` appear on the left hand side of an assignment in an `always` statement, they must be declared to be `reg`.

**VHDL**

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity fulladder is
  port(a, b, cin: in STD_LOGIC;
       s, cout: out STD_LOGIC);
end;

architecture synth of fulladder is
begin
  process(a, b, cin)
    variable p, g: STD_LOGIC;
  begin
    p := a xor b; -- blocking
    g := a and b; -- blocking

    s <= p xor cin;
    cout <= g or (p and cin);
  end process;
end;
```

The `process` sensitivity list must include `a`, `b`, and `cin` because combinational logic should respond to changes of any input.

For reasons that will be discussed in Section 4.5.4, it is best to use blocking assignments for intermediate variables in combinational logic. This example uses blocking assignments for `p` and `g` so that they get their new values before being used to compute `s` and `cout` that depend on them.

Because `p` and `g` appear on the left hand side of a blocking assignment (`: =`) in a `process` statement, they must be declared to be `variable` rather than `signal`. The `variable` declaration appears before the `begin` in the `process` where the variable is used.

### 4.5.1 Case Statements

A better application of using the `always/process` statement for combinational logic is a seven-segment display decoder that takes advantage of the `case` statement that must appear inside an `always/process` statement.

As you might have noticed in Example 2.10, the design process for large blocks of combinational logic is tedious and prone to error. HDLs offer a great improvement, allowing you to specify the function at a higher level of abstraction, and then automatically synthesize the function into gates. HDL Example 4.25 uses `case` statements to describe a seven-segment display decoder based on its truth table. (See Example 2.10 for a description of the seven-segment display decoder.) The `case`

#### HDL Example 4.25 SEVEN-SEGMENT DISPLAY DECODER

##### Verilog

```
module sevenseg (input      [3:0] data,
                  output reg [6:0] segments);
  always @(*) begin
    case (data)
      // abcdefg
      0: segments = 7'b111_1110;
      1: segments = 7'b011_0000;
      2: segments = 7'b110_1101;
      3: segments = 7'b111_1001;
      4: segments = 7'b011_0011;
      5: segments = 7'b101_1011;
      6: segments = 7'b101_1111;
      7: segments = 7'b111_0000;
      8: segments = 7'b111_1111;
      9: segments = 7'b111_1011;
      default: segments = 7'b000_0000;
    endcase
  endmodule
```

The `case` statement checks the value of `data`. When `data` is 0, the statement performs the action after the colon, setting `segments` to 1111110. The `case` statement similarly checks other `data` values up to 9 (note the use of the default base, base 10).

The `default` clause is a convenient way to define the output for all cases not explicitly listed, guaranteeing combinational logic.

In Verilog, `case` statements must appear inside `always` statements.

##### VHDL

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity seven_seg_decoder is
  port (data:  in STD_LOGIC_VECTOR (3 downto 0);
        segments: out STD_LOGIC_VECTOR (6 downto 0));
end;

architecture synth of seven_seg_decoder is
begin
  process (data) begin
    case data is
      -- abcdefg
      when X"0" => segments <= "1111110";
      when X"1" => segments <= "0110000";
      when X"2" => segments <= "1101101";
      when X"3" => segments <= "1111001";
      when X"4" => segments <= "0110011";
      when X"5" => segments <= "1011011";
      when X"6" => segments <= "1011111";
      when X"7" => segments <= "1110000";
      when X"8" => segments <= "1111111";
      when X"9" => segments <= "1111011";
      when others => segments <= "0000000";
    end case;
  end process;
end;
```

The `case` statement checks the value of `data`. When `data` is 0, the statement performs the action after the `=>`, setting `segments` to 1111110. The `case` statement similarly checks other `data` values up to 9 (note the use of `X` for hexadecimal numbers). The `others` clause is a convenient way to define the output for all cases not explicitly listed, guaranteeing combinational logic.

Unlike Verilog, VHDL supports selected signal assignment statements (see HDL Example 4.6), which are much like `case` statements but can appear outside processes. Thus, there is less reason to use processes to describe combinational logic.



Figure 4.22 sevenseg synthesized circuit

statement performs different actions depending on the value of its input. A `case` statement implies combinational logic if all possible input combinations are defined; otherwise it implies sequential logic, because the output will keep its old value in the undefined cases.

Synplify Pro synthesizes the seven-segment display decoder into a *read-only memory* (ROM) containing the 7 outputs for each of the 16 possible inputs. ROMs are discussed further in Section 5.5.6.

If the `default` or `others` clause were left out of the `case` statement, the decoder would have remembered its previous output anytime data were in the range of 10–15. This is strange behavior for hardware.

Ordinary decoders are also commonly written with `case` statements. HDL Example 4.26 describes a 3:8 decoder.

#### 4.5.2 If Statements

`always/process` statements may also contain `if` statements. The `if` statement may be followed by an `else` statement. If all possible input

##### HDL Example 4.26 3:8 DECODER

###### Verilog

```

module decoder3_8(input      [2:0] a,
                    output reg [7:0] y);
    always @ (*)
        case (a)
            3'b000: y = 8'b00000001;
            3'b001: y = 8'b00000010;
            3'b010: y = 8'b00000100;
            3'b011: y = 8'b00001000;
            3'b100: y = 8'b00010000;
            3'b101: y = 8'b00100000;
            3'b110: y = 8'b01000000;
            3'b111: y = 8'b10000000;
        endcase
    endmodule

```

No default statement is needed because all cases are covered.

###### VHDL

```

library IEEE; use IEEE.STD_LOGIC_1164.all;
entity decoder3_8 is
    port(a: in STD_LOGIC_VECTOR(2 downto 0);
         y: out STD_LOGIC_VECTOR(7 downto 0));
end;
architecture synth of decoder3_8 is
begin
    process (a) begin
        case a is
            when "000" => y <= "00000001";
            when "001" => y <= "00000010";
            when "010" => y <= "00000100";
            when "011" => y <= "00001000";
            when "100" => y <= "00010000";
            when "101" => y <= "00100000";
            when "110" => y <= "01000000";
            when "111" => y <= "10000000";
        end case;
    end process;
end;

```

No others clause is needed because all cases are covered.

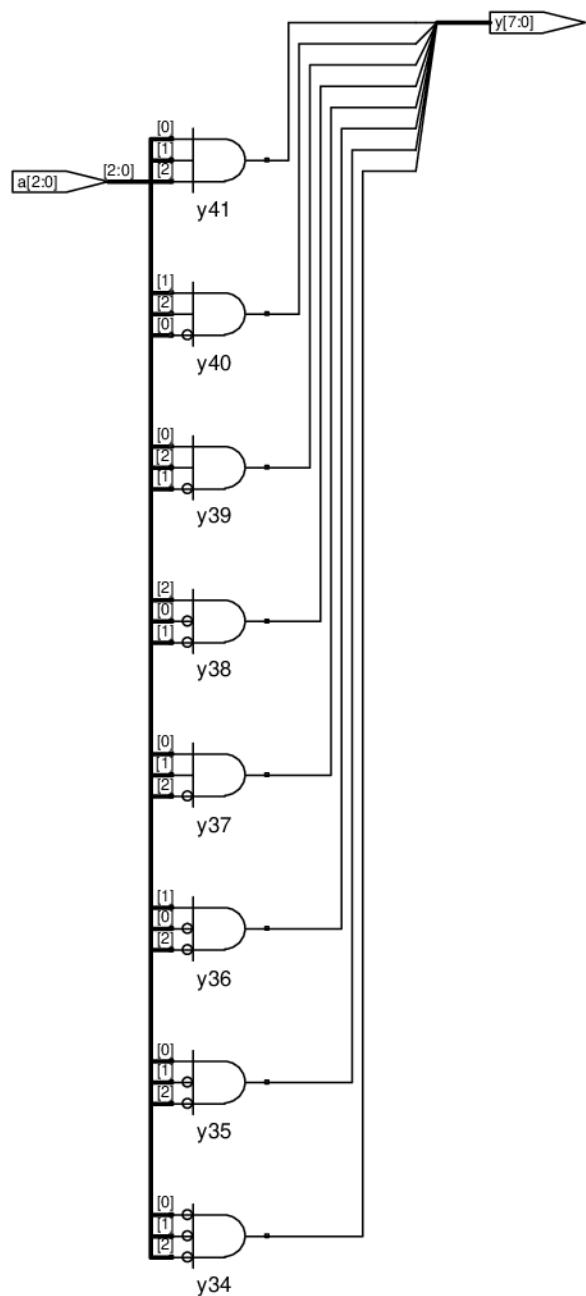


Figure 4.23 decoder3\_8 synthesized circuit

**HDL Example 4.27 PRIORITY CIRCUIT****Verilog**

```
module priority(input [3:0] a,
                output reg [3:0] y);

    always @ (*)
        if (a[3]) y = 4'b1000;
        else if (a[2]) y = 4'b0100;
        else if (a[1]) y = 4'b0010;
        else if (a[0]) y = 4'b0001;
        else           y = 4'b0000;
endmodule
```

In Verilog, if statements must appear inside of always statements.

**VHDL**

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity priority is
    port(a: in STD_LOGIC_VECTOR(3 downto 0);
         y: out STD_LOGIC_VECTOR(3 downto 0));
end;

architecture synth of priority is
begin
    process (a) begin
        if a(3) = '1' then y <= "1000";
        elsif a(2) = '1' then y <= "0100";
        elsif a(1) = '1' then y <= "0010";
        elsif a(0) = '1' then y <= "0001";
        else                  y <= "0000";
        end if;
    end process;
end;
```

Unlike Verilog, VHDL supports conditional signal assignment statements (see HDL Example 4.6), which are much like if statements but can appear outside processes. Thus, there is less reason to use processes to describe combinational logic. (Figure follows on next page.)

combinations are handled, the statement implies combinational logic; otherwise, it produces sequential logic (like the latch in Section 4.4.5).

HDL Example 4.27 uses if statements to describe a priority circuit, defined in Section 2.4. Recall that an  $N$ -input priority circuit sets the output TRUE that corresponds to the most significant input that is TRUE.

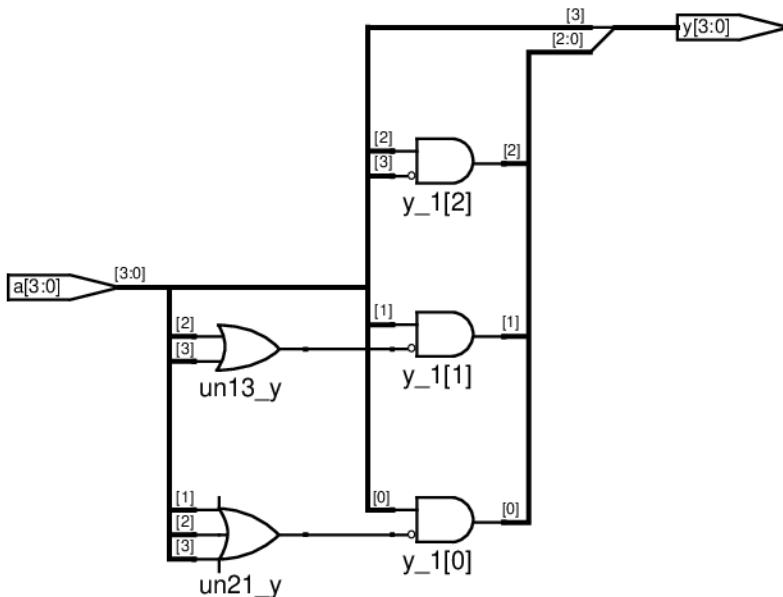
**4.5.3 Verilog casez\***

(This section may be skipped by VHDL users.) Verilog also provides the casez statement to describe truth tables with don't cares (indicated with ? in the casez statement). HDL Example 4.28 shows how to describe a priority circuit with casez.

Synplify Pro synthesizes a slightly different circuit for this module, shown in Figure 4.25, than it did for the priority circuit in Figure 4.24. However, the circuits are logically equivalent.

**4.5.4 Blocking and Nonblocking Assignments**

The guidelines on page 203 explain when and how to use each type of assignment. If these guidelines are not followed, it is possible to write



**Figure 4.24** priority synthesized circuit

#### HDL Example 4.28 PRIORITY CIRCUIT USING casez

```
module priority_casez(input      [3:0] a,
                      output reg [3:0] y);

  always @(*)
    casez (a)
      4'b1???: y = 4'b1000;
      4'b01???: y = 4'b0100;
      4'b001?: y = 4'b0010;
      4'b0001: y = 4'b0001;
      default: y = 4'b0000;
    endcase
endmodule
```

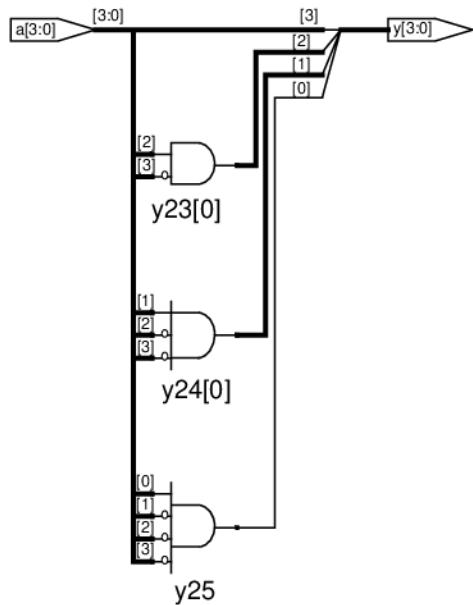
(See figure 4.25.)

code that appears to work in simulation but synthesizes to incorrect hardware. The optional remainder of this section explains the principles behind the guidelines.

#### Combinational Logic\*

The full adder from HDL Example 4.24 is correctly modeled using blocking assignments. This section explores how it operates and how it would differ if nonblocking assignments had been used.

Imagine that  $a$ ,  $b$ , and  $cin$  are all initially 0.  $p$ ,  $g$ ,  $s$ , and  $cout$  are thus 0 as well. At some time,  $a$  changes to 1, triggering the always/process statement. The four blocking assignments evaluate in



**Figure 4.25** priority\_casez  
synthesized circuit

#### BLOCKING AND NONBLOCKING ASSIGNMENT GUIDELINES

##### Verilog

1. Use `always @ (posedge clk)` and nonblocking assignments to model synchronous sequential logic.

```
always @ (posedge clk)
begin
    nl <= d; // nonblocking
    q <= nl; // nonblocking
end
```

2. Use continuous assignments to model simple combinational logic.

```
assign y = s ? d1 : d0;
```

3. Use `always @ (*)` and blocking assignments to model more complicated combinational logic where the `always` statement is helpful.

```
always @ (*)
begin
    p = a ^ b; // blocking
    g = a & b; // blocking
    s = p ^ cin;
    cout = g | (p & cin);
end
```

4. Do not make assignments to the same signal in more than one `always` statement or continuous assignment statement.

##### VHDL

1. Use `process (clk)` and nonblocking assignments to model synchronous sequential logic.

```
process (clk) begin
    if clk'event and clk = '1' then
        nl <= d; -- nonblocking
        q <= nl; -- nonblocking
    end if;
end process;
```

2. Use concurrent assignments outside `process` statements to model simple combinational logic.

```
y <= d0 when s = '0' else d1;
```

3. Use `process (in1, in2, ...)` to model more complicated combinational logic where the `process` is helpful. Use blocking assignments for internal variables.

```
process (a, b, cin)
    variable p, g: STD_LOGIC;
begin
    p := a xor b; -- blocking
    g := a and b; -- blocking
    s <= p xor cin;
    cout <= g or (p and cin);
end process;
```

4. Do not make assignments to the same variable in more than one `process` or concurrent assignment statement.

the order shown here. (In the VHDL code, `s` and `cout` are assigned concurrently.) Note that `p` and `g` get their new values before `s` and `cout` are computed because of the blocking assignments. This is important because we want to compute `s` and `cout` using the new values of `p` and `g`.

1.  $p \leftarrow 1 \oplus 0 = 1$
2.  $g \leftarrow 1 \bullet 0 = 0$
3.  $s \leftarrow 1 \oplus 0 = 1$
4.  $cout \leftarrow 0 + 1 \bullet 0 = 0$

In contrast, HDL Example 4.29 illustrates the use of nonblocking assignments.

Now consider the same case of a rising from 0 to 1 while `b` and `cin` are 0. The four nonblocking assignments evaluate concurrently:

$$p \leftarrow 1 \oplus 0 = 1 \quad g \leftarrow 1 \bullet 0 = 0 \quad s \leftarrow 0 \oplus 0 = 0 \quad cout \leftarrow 0 + 0 \bullet 0 = 0$$

Observe that `s` is computed concurrently with `p` and hence uses the old value of `p`, not the new value. Therefore, `s` remains 0 rather than

---

#### HDL Example 4.29 FULL ADDER USING NONBLOCKING ASSIGNMENTS

**Verilog**

```
// nonblocking assignments (not recommended)
module fulladder (input      a, b, cin,
                     output reg s, cout);
    reg p, g;

    always @ (*)
        begin
            p <= a ^ b; // nonblocking
            g <= a & b; // nonblocking

            s <= p ^ cin;
            cout <= g | (p & cin);
        end
    endmodule
```

Because `p` and `g` appear on the left hand side of an assignment in an `always` statement, they must be declared to be `reg`.

**VHDL**

```
-- nonblocking assignments (not recommended)
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity fulladder is
    port(a, b, cin: in STD_LOGIC;
         s, cout: out STD_LOGIC);
end;

architecture nonblocking of fulladder is
    signal p, g: STD_LOGIC;
begin
    process(a, b, cin, p, g)begin
        p <= a xor b; -- nonblocking
        g <= a and b; -- nonblocking

        s <= p xor cin;
        cout <= g or (p and cin);
    end process;
end;
```

Because `p` and `g` appear on the left hand side of a nonblocking assignment in a `process` statement, they must be declared to be `signal` rather than `variable`. The `signal` declaration appears before the `begin` in the `architecture`, not the `process`.

becoming 1. However,  $p$  does change from 0 to 1. This change triggers the `always/process` statement to evaluate a second time, as follows:

$$p \leftarrow 1 \oplus 0 = 1 \quad g \leftarrow 1 \bullet 0 = 0 \quad s \leftarrow 1 \oplus 0 = 1 \quad cout \leftarrow 0 + 1 \bullet 0 = 0$$

This time,  $p$  is already 1, so  $s$  correctly changes to 1. The nonblocking assignments eventually reach the right answer, but the `always/process` statement had to evaluate twice. This makes simulation slower, though it synthesizes to the same hardware.

Another drawback of nonblocking assignments in modeling combinational logic is that the HDL will produce the wrong result if you forget to include the intermediate variables in the sensitivity list.

Verilog	VHDL
If the sensitivity list of the <code>always</code> statement in HDL Example 4.29 were written as <code>always @ (a, b, cin)</code> rather than <code>always @ (*)</code> , then the statement would not reevaluate when $p$ or $g$ changes. In the previous example, $s$ would be incorrectly left at 0, not 1.	If the sensitivity list of the <code>process</code> statement in HDL Example 4.29 were written as <code>process (a, b, cin)</code> rather than <code>process (a, b, cin, p, g)</code> , then the statement would not reevaluate when $p$ or $g$ changes. In the previous example, $s$ would be incorrectly left at 0, not 1.

Worse yet, some synthesis tools will synthesize the correct hardware even when a faulty sensitivity list causes incorrect simulation. This leads to a mismatch between the simulation results and what the hardware actually does.

#### Sequential Logic\*

The synchronizer from HDL Example 4.21 is correctly modeled using non-blocking assignments. On the rising edge of the clock,  $d$  is copied to  $n1$  at the same time that  $n1$  is copied to  $q$ , so the code properly describes two registers. For example, suppose initially that  $d = 0$ ,  $n1 = 1$ , and  $q = 0$ . On the rising edge of the clock, the following two assignments occur concurrently, so that after the clock edge,  $n1 = 0$  and  $q = 1$ .

$$n1 \leftarrow d = 0 \quad q \leftarrow n1 = 1$$

HDL Example 4.30 tries to describe the same module using blocking assignments. On the rising edge of `clk`,  $d$  is copied to  $n1$ . Then this new value of  $n1$  is copied to  $q$ , resulting in  $d$  improperly appearing at both  $n1$  and  $q$ . The assignments occur one after the other so that after the clock edge,  $q = n1 = 0$ .

1.  $n1 \leftarrow d = 0$
2.  $q \leftarrow n1 = 0$

**HDL Example 4.30 BAD SYNCHRONIZER WITH BLOCKING ASSIGNMENTS****Verilog**

```
// Bad implementation using blocking assignments

module syncbad(input      clk,
                input      d,
                output reg q);

    reg n1;

    always @ (posedge clk)
    begin
        n1 = d; // blocking
        q = n1; // blocking
    end
endmodule
```

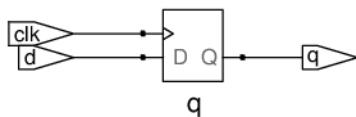
**VHDL**

```
-- Bad implementation using blocking assignment

library IEEE; use IEEE.STD_LOGIC_1164.all;

entity syncbad is
    port (clk: in STD_LOGIC;
          d:  in STD_LOGIC;
          q:  out STD_LOGIC);
end;

architecture bad of syncbad is
begin
    process (clk)
        variable n1: STD_LOGIC;
    begin
        if clk'event and clk = '1' then
            n1 := d; -- blocking
            q <= n1;
        end if;
    end process;
end;
```

**Figure 4.26** syncbad **synthesized circuit**

Because `n1` is invisible to the outside world and does not influence the behavior of `q`, the synthesizer optimizes it away entirely, as shown in Figure 4.26.

The moral of this illustration is to exclusively use nonblocking assignment in `always` statements when modeling sequential logic. With sufficient cleverness, such as reversing the orders of the assignments, you could make blocking assignments work correctly, but blocking assignments offer no advantages and only introduce the risk of unintended behavior. Certain sequential circuits will not work with blocking assignments no matter what the order.

## 4.6 FINITE STATE MACHINES

Recall that a finite state machine (FSM) consists of a state register and two blocks of combinational logic to compute the next state and the output given the current state and the input, as was shown in Figure 3.22. HDL descriptions of state machines are correspondingly divided into three parts to model the state register, the next state logic, and the output logic.

**HDL Example 4.31 DIVIDE-BY-3 FINITE STATE MACHINE****Verilog**

```
module divideby3FSM(input clk,
                      input reset,
                      output y);

    reg [1:0] state, nextstate;

    parameter S0 = 2'b00;
    parameter S1 = 2'b01;
    parameter S2 = 2'b10;

    // state register
    always @ (posedge clk, posedge reset)
        if (reset) state <= S0;
        else       state <= nextstate;

    // next state logic
    always @ (*)
        case (state)
            S0: nextstate = S1;
            S1: nextstate = S2;
            S2: nextstate = S0;
            default: nextstate = S0;
        endcase

    // output logic
    assign y = (state == S0);
endmodule
```

The parameter statement is used to define constants within a module. Naming the states with parameters is not required, but it makes changing state encodings much easier and makes the code more readable.

Notice how a case statement is used to define the state transition table. Because the next state logic should be combinational, a default is necessary even though the state  $2^{\text{bit}}$  should never arise.

The output,  $y$ , is 1 when the state is  $S_0$ . The *equality comparison*  $a == b$  evaluates to 1 if  $a$  equals  $b$  and 0 otherwise. The *inequality comparison*  $a != b$  does the inverse, evaluating to 1 if  $a$  does not equal  $b$ .

**VHDL**

```
library IEEE; use IEEE.STD_LOGIC_1164.all;
entity divideby3FSM is
    port(clk, reset: in STD_LOGIC;
          y:         out STD_LOGIC);
end;

architecture synth of divideby3FSM is
    type statetype is (S0, S1, S2);
    signal state, nextstate: statetype;
begin
    -- state register
    process (clk, reset) begin
        if reset = '1' then state <= S0;
        elsif clk'event and clk = '1' then
            state <= nextstate;
        end if;
    end process;

    -- next state logic
    nextstate <= S1 when state = S0 else
                  S2 when state = S1 else
                  S0;

    -- output logic
    y <= '1' when state = S0 else '0';
end;
```

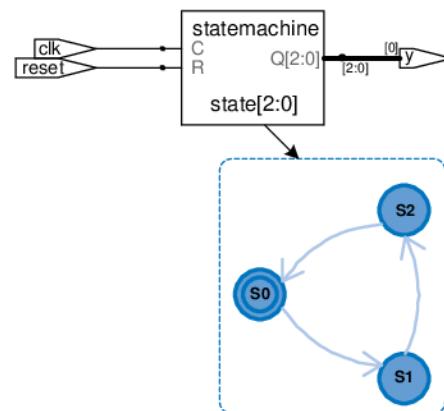
This example defines a new *enumeration* data type, *statetype*, with three possibilities:  $S_0$ ,  $S_1$ , and  $S_2$ . *state* and *nextstate* are *statetype* signals. By using an enumeration instead of choosing the state encoding, VHDL frees the synthesizer to explore various state encodings to choose the best one.

The output,  $y$ , is 1 when the state is  $S_0$ . The inequality-comparison uses  $/=$ . To produce an output of 1 when the state is anything but  $S_0$ , change the comparison to  $\text{state} /= S_0$ .

HDL Example 4.31 describes the divide-by-3 FSM from Section 3.4.2. It provides an asynchronous reset to initialize the FSM. The state register uses the ordinary idiom for flip-flops. The next state and output logic blocks are combinational.

The Synplify Pro Synthesis tool just produces a block diagram and state transition diagram for state machines; it does not show the logic gates or the inputs and outputs on the arcs and states. Therefore, be careful that you have specified the FSM correctly in your HDL code. The state transition diagram in Figure 4.27 for the divide-by-3 FSM is analogous to the diagram in Figure 3.28(b). The double circle indicates that

Notice that the synthesis tool uses a 3-bit encoding ( $Q[2:0]$ ) instead of the 2-bit encoding suggested in the Verilog code.



**Figure 4.27** divideby3fsm synthesized circuit

S0 is the reset state. Gate-level implementations of the divide-by-3 FSM were shown in Section 3.4.2.

If, for some reason, we had wanted the output to be HIGH in states S0 and S1, the output logic would be modified as follows.

Verilog	VHDL
// Output Logic assign y = (state == S0   state == S1);	-- output logic y <= '1' when (state = S0 or state = S1) else '0';

The next two examples describe the snail pattern recognizer FSM from Section 3.4.3. The code shows how to use `case` and `if` statements to handle next state and output logic that depend on the inputs as well as the current state. We show both Moore and Mealy modules. In the Moore machine (HDL Example 4.32), the output depends only on the current state, whereas in the Mealy machine (HDL Example 4.33), the output logic depends on both the current state and inputs.

### HDL Example 4.32 PATTERN RECOGNIZER MOORE FSM

#### Verilog

```

module patternMoore(input clk,
                     input reset,
                     input a,
                     output y);

reg [2:0] state, nextstate;

parameter S0 = 3'b000;
parameter S1 = 3'b001;
parameter S2 = 3'b010;
parameter S3 = 3'b011;
parameter S4 = 3'b100;

// state register
always @ (posedge clk, posedge reset)
  if (reset) state <= S0;
  else       state <= nextstate;

// next state logic
always @ (*)
  case (state)
    S0: if (a) nextstate = S1;
         else      nextstate = S0;
    S1: if (a) nextstate = S2;
         else      nextstate = S0;
    S2: if (a) nextstate = S3;
         else      nextstate = S3;
    S3: if (a) nextstate = S4;
         else      nextstate = S0;
    S4: if (a) nextstate = S2;
         else      nextstate = S0;
    default: nextstate = S0;
  endcase

// output logic
assign y = (state == S4);
endmodule

```

Note how nonblocking assignments ( $<=$ ) are used in the state register to describe sequential logic, whereas blocking assignments ( $=$ ) are used in the next state logic to describe combinational logic.

#### VHDL

```

library IEEE; use IEEE.STD_LOGIC_1164.all;
entity patternMoore is
  port(clk, reset: in STD_LOGIC;
        a:          in STD_LOGIC;
        y:          out STD_LOGIC);
end;

architecture synth of patternMoore is
  type statetype is (S0, S1, S2, S3, S4);
  signal state, nextstate: statetype;
begin
  -- state register
  process(clk, reset) begin
    if reset = '1' then state <= S0;
    elsif clk'event and clk = '1' then
      state <= nextstate;
    end if;
  end process;

  -- next state logic
  process(state, a) begin
    case state is
      when S0 => if a = '1' then
                    nextstate <= S1;
                  else nextstate <= S0;
                  end if;
      when S1 => if a = '1' then
                    nextstate <= S2;
                  else nextstate <= S0;
                  end if;
      when S2 => if a = '1' then
                    nextstate <= S3;
                  else nextstate <= S3;
                  end if;
      when S3 => if a = '1' then
                    nextstate <= S4;
                  else nextstate <= S0;
                  end if;
      when S4 => if a = '1' then
                    nextstate <= S2;
                  else nextstate <= S0;
                  end if;
      when others => nextstate <= S0;
    end case;
  end process;

  -- output logic
  y <= '1' when state = S4 else '0';
end;

```

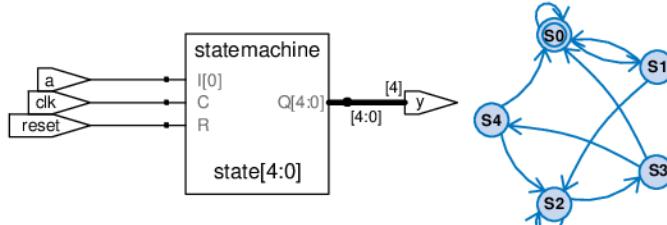


Figure 4.28 patternMoore synthesized circuit

**HDL Example 4.33 PATTERN RECOGNIZER MEALY FSM****Verilog**

```
module patternMealy (input clk,
                      input reset,
                      input a,
                      output y);

    reg [1:0] state, nextstate;

    parameter S0 = 2'b00;
    parameter S1 = 2'b01;
    parameter S2 = 2'b10;
    parameter S3 = 2'b11;

    // state register
    always @ (posedge clk, posedge reset)
        if(reset) state <= S0;
        else      state <= nextstate;

    // next state logic
    always @ (*)
        case (state)
            S0: if (a) nextstate = S1;
                  else      nextstate = S0;
            S1: if (a) nextstate = S2;
                  else      nextstate = S0;
            S2: if (a) nextstate = S3;
                  else      nextstate = S3;
            S3: if (a) nextstate = S1;
                  else      nextstate = S0;
            default: nextstate = S0;
        endcase

    // output logic
    assign y = (a & state == S3);
endmodule
```

**VHDL**

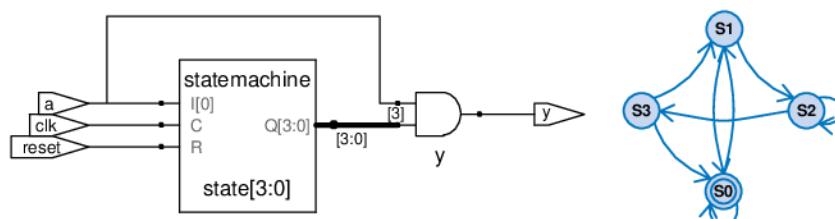
```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity patternMealy is
    port(clk, reset: in STD_LOGIC;
          a:         in STD_LOGIC;
          y:         out STD_LOGIC);
end;

architecture synth of patternMealy is
    type statetype is (S0, S1, S2, S3);
    signal state, nextstate: statetype;
begin
    -- state register
    process(clk, reset) begin
        if reset = '1' then state <= S0;
        elsif clk'event and clk = '1' then
            state <= nextstate;
        end if;
    end process;

    -- next state logic
    process(state, a) begin
        case state is
            when S0 => if a = '1' then
                nextstate <= S1;
                else nextstate <= S0;
            end if;
            when S1 => if a = '1' then
                nextstate <= S2;
                else nextstate <= S0;
            end if;
            when S2 => if a = '1' then
                nextstate <= S3;
                else nextstate <= S2;
            end if;
            when S3 => if a = '1' then
                nextstate <= S1;
                else nextstate <= S0;
            end if;
            when others => nextstate <= S0;
        end case;
    end process;

    -- output logic
    y <= '1' when (a = '1' and state = S3) else '0';
end;
```

**Figure 4.29** patternMealy synthesized circuit

## 4.7 PARAMETERIZED MODULES\*

So far all of our modules have had fixed-width inputs and outputs. For example, we had to define separate modules for 4- and 8-bit wide 2:1 multiplexers. HDLs permit variable bit widths using parameterized modules.

### HDL Example 4.34 PARAMETERIZED N-BIT MULTIPLEXERS

#### Verilog

```
module mux2
  #(parameter width = 8)
  (input [width-1:0] d0, d1,
   input           s,
   output [width-1:0] y);

  assign y = s ? d1 : d0;
endmodule
```

Verilog allows a `#(parameter ...)` statement before the inputs and outputs to define parameters. The parameter statement includes a default value (8) of the parameter, `width`. The number of bits in the inputs and outputs can depend on this parameter.

```
module mux4_8(input [7:0] d0, d1, d2, d3,
               input [1:0] s,
               output [7:0] y);

  wire [7:0] low, hi;

  mux2 lowmux(d0, d1, s[0], low);
  mux2 himux(d2, d3, s[1], hi);
  mux2 outmux(low, hi, s[1], y);
endmodule
```

The 8-bit 4:1 multiplexer instantiates three 2:1 multiplexers using their default widths.

In contrast, a 12-bit 4:1 multiplexer, `mux4_12`, would need to override the default width using `#()` before the instance name, as shown below.

```
module mux4_12(input [11:0] d0, d1, d2, d3,
               input [1:0] s,
               output [11:0] y);

  wire [11:0] low, hi;

  mux2 #(12) lowmux(d0, d1, s[0], low);
  mux2 #(12) himux(d2, d3, s[1], hi);
  mux2 #(12) outmux(low, hi, s[1], y);
endmodule
```

Do not confuse the use of the `#` sign indicating delays with the use of `#( ... )` in defining and overriding parameters.

#### VHDL

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity mux2 is
  generic(width: integer := 8);
  port(d0,
        d1: in STD_LOGIC_VECTOR(width-1 downto 0);
        s: in STD_LOGIC;
        y: out STD_LOGIC_VECTOR(width-1 downto 0));
end;
```

architecture synth of mux2 is  
begin  
 y <= d0 when s = '0' else d1;  
end;

The generic statement includes a default value (8) of width.  
The value is an integer.

```
entity mux4_8 is
  port(d0, d1, d2,
        d3: in STD_LOGIC_VECTOR(7 downto 0);
        s: in STD_LOGIC_VECTOR(1 downto 0);
        y: out STD_LOGIC_VECTOR(7 downto 0));
end;

architecture struct of mux4_8 is
  component mux2
    generic(width: integer);
    port(d0,
          d1: in STD_LOGIC_VECTOR(width-1 downto 0) ;
          s: in STD_LOGIC;
          y: out STD_LOGIC_VECTOR(width-1 downto 0));
  end component;
  signal low, hi: STD_LOGIC_VECTOR(7 downto 0);
begin
  lowmux: mux2 port map(d0, d1, s(0), low);
  himux: mux2 port map(d2, d3, s(1), hi);
  outmux: mux2 port map(low, hi, s(1), y);
end;
```

The 8-bit 4:1 multiplexer, `mux4_8`, instantiates three 2:1 multiplexers using their default widths.

In contrast, a 12-bit 4:1 multiplexer, `mux4_12`, would need to override the default width using generic map, as shown below.

```
lowmux: mux2 generic map (12)
          port map(d0, d1, s(0), low);
himux: mux2 generic map (12)
          port map(d2, d3, s(1), hi);
outmux: mux2 generic map (12)
          port map(low, hi, s(1), y);
```

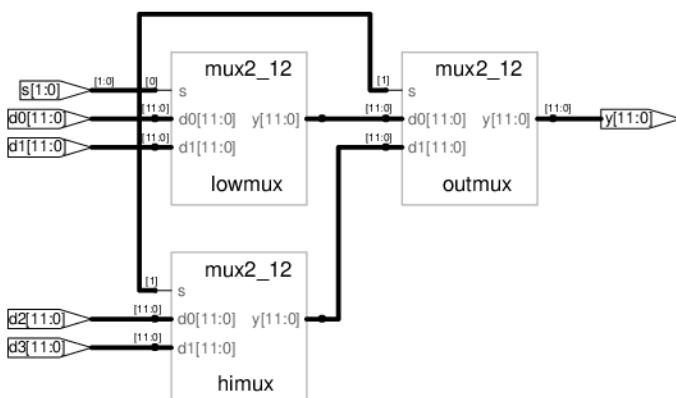


Figure 4.30 mux4\_12 synthesized circuit

**HDL Example 4.35 PARAMETERIZED N:2<sup>N</sup> DECODER****Verilog**

```
module decoder #(parameter N = 3)
    (input [N-1:0] a,
     output reg [2**N-1:0] y);

    always @ (*)
    begin
        y = 0;
        y[a] = 1;
    end
endmodule
```

2\*\*N indicates  $2^N$ .

**VHDL**

```
library IEEE; use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_UNSIGNED.all;
use IEEE.STD_LOGIC_ARITH.all;

entity decoder is
    generic(N: integer := 3);
    port(a: in STD_LOGIC_VECTOR(N-1 downto 0);
         y: out STD_LOGIC_VECTOR(2**N-1 downto 0));
end;

architecture synth of decoder is
begin
    process(a)
        variable tmp: STD_LOGIC_VECTOR(2**N-1 downto 0);
    begin
        tmp := CONV_STD_LOGIC_VECTOR(0, 2**N);
        tmp(CONV_INTEGER(a)) := '1';
        y <= tmp;
    end process;
end;
```

2\*\*N indicates  $2^N$ .

`CONV_STD_LOGIC_VECTOR(0, 2**N)` produces a `STD_LOGIC_VECTOR` of length  $2^N$  containing all 0's. It requires the `STD_LOGIC_ARITH` library. The function is useful in other parameterized functions, such as resettable flip-flops that need to be able to produce constants with a parameterized number of bits. The bit index in VHDL must be an integer, so the `CONV_INTEGER` function is used to convert a from a `STD_LOGIC_VECTOR` to an integer.

HDL Example 4.34 declares a parameterized 2:1 multiplexer with a default width of 8, then uses it to create 8- and 12-bit 4:1 multiplexers.

HDL Example 4.35 shows a decoder, which is an even better application of parameterized modules. A large  $N:2^N$  decoder is cumbersome to

specify with case statements, but easy using parameterized code that simply sets the appropriate output bit to 1. Specifically, the decoder uses blocking assignments to set all the bits to 0, then changes the appropriate bit to 1.

HDLs also provide generate statements to produce a variable amount of hardware depending on the value of a parameter. generate supports for loops and if statements to determine how many of what types of hardware to produce. HDL Example 4.36 demonstrates how to use generate statements to produce an  $N$ -input AND function from a cascade of two-input AND gates.

Use generate statements with caution; it is easy to produce a large amount of hardware unintentionally!

---

#### HDL Example 4.36 PARAMETERIZED N-INPUT AND GATE

**Verilog**

```
module andN
#(parameter width = 8)
  (input [width-1:0] a,
   output          y);

  genvar i;
  wire [width-1:1] x;

  generate
    for (i=1; i<width; i=i+1) begin:forloop
      if (i == 1)
        assign x[1] = a[0] & a[1];
      else
        assign x[i] = a[i] & x[i-1];
    end
  endgenerate
  assign y = x[width-1];
endmodule
```

The for statement loops through  $i = 1, 2, \dots, \text{width}-1$  to produce many consecutive AND gates. The begin in a generate for loop must be followed by a : and an arbitrary label (forloop, in this case).

Of course, writing `assign y = &a` would be much easier!

**VHDL**

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity andN is
  generic(width: integer := 8);
  port(a: in STD_LOGIC_VECTOR(width-1 downto 0);
       y: out STD_LOGIC);
end;

architecture synth of andN is
  signal i: integer;
  signal x: STD_LOGIC_VECTOR(width-1 downto 1);
begin
  AllBits: for i in 1 to width-1 generate
    LowBit: if i = 1 generate
      A1: x(1) <= a(0) and a(1);
    end generate;
    OtherBits: if i /= 1 generate
      Ai: x(i) <= a(i) and x(i-1);
    end generate;
  end generate;
  y <= x(width-1);
end;
```

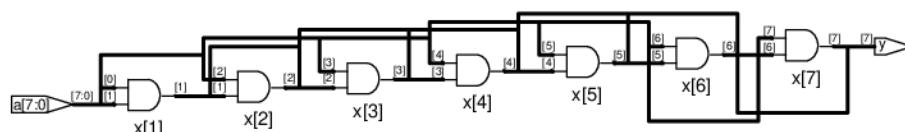


Figure 4.31 andN synthesized circuit

---

## 4.8 TESTBENCHES

Some tools also call the module to be tested the *unit under test (UUT)*.

A *testbench* is an HDL module that is used to test another module, called the *device under test (DUT)*. The testbench contains statements to apply inputs to the DUT and, ideally, to check that the correct outputs are produced. The input and desired output patterns are called *test vectors*.

Consider testing the *sillyfunction* module from Section 4.1.1 that computes  $y = \bar{a}\bar{b}\bar{c} + a\bar{b}\bar{c} + \bar{a}bc$ . This is a simple module, so we can perform exhaustive testing by applying all eight possible test vectors.

HDL Example 4.37 demonstrates a simple testbench. It instantiates the DUT, then applies the inputs. Blocking assignments and delays are used to apply the inputs in the appropriate order. The user must view the results of the simulation and verify by inspection that the correct outputs are produced. Testbenches are simulated the same as other HDL modules. However, they are not synthesizable.

### HDL Example 4.37 TESTBENCH

#### Verilog

```
module testbench1();
  reg a, b, c;
  wire y;

  // instantiate device under test
  sillyfunction dut(a, b, c, y);

  // apply inputs one at a time
  initial begin
    a = 0; b = 0; c = 0; #10;
    c = 1;           #10;
    b = 1; c = 0;     #10;
    c = 1;           #10;
    a = 1; b = 0; c = 0; #10;
    c = 1;           #10;
    b = 1; c = 0;     #10;
    c = 1;           #10;
  end
endmodule
```

The `initial` statement executes the statements in its body at the start of simulation. In this case, it first applies the input pattern 000 and waits for 10 time units. It then applies 001 and waits 10 more units, and so forth until all eight possible inputs have been applied. `initial` statements should be used only in testbenches for simulation, not in modules intended to be synthesized into actual hardware. Hardware has no way of magically executing a sequence of special steps when it is first turned on.

Like signals in `always` statements, signals in `initial` statements must be declared to be `reg`.

#### VHDL

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity testbench1 is -- no inputs or outputs
end;

architecture sim of testbench1 is
  component sillyfunction
    port(a, b, c: in STD_LOGIC;
         y:        out STD_LOGIC);
  end component;
  signal a, b, c, y: STD_LOGIC;
begin
  -- instantiate device under test
  dut: sillyfunction port map(a, b, c, y);

  -- apply inputs one at a time
  process begin
    a <= '0'; b <= '0'; c <= '0'; wait for 10 ns;
    c <= '1';           wait for 10 ns;
    b <= '1'; c <= '0';   wait for 10 ns;
    c <= '1';           wait for 10 ns;
    a <= '1'; b <= '0'; c <= '0'; wait for 10 ns;
    c <= '1';           wait for 10 ns;
    b <= '1'; c <= '0';   wait for 10 ns;
    c <= '1';           wait for 10 ns;
    wait; -- wait forever
  end process;
end;
```

The `process` statement first applies the input pattern 000 and waits for 10 ns. It then applies 001 and waits 10 more ns, and so forth until all eight possible inputs have been applied.

At the end, the process waits indefinitely; otherwise, the process would begin again, repeatedly applying the pattern of test vectors.

Checking for correct outputs is tedious and error-prone. Moreover, determining the correct outputs is much easier when the design is fresh in your mind; if you make minor changes and need to retest weeks later, determining the correct outputs becomes a hassle. A much better approach is to write a self-checking testbench, shown in HDL Example 4.38.

#### HDL Example 4.38 SELF-CHECKING TESTBENCH

##### Verilog

```
module testbench2 ();
    reg a, b, c;
    wire y;

    // instantiate device under test
    sillyfunction dut(a, b, c, y);

    // apply inputs one at a time
    // checking results
    initial begin
        a = 0; b = 0; c = 0; #10;
        if(y != 1) $display("000 failed.");
        c = 1;           #10;
        if(y != 0) $display("001 failed.");
        b = 1; c = 0;   #10;
        if(y != 0) $display("010 failed.");
        c = 1;           #10;
        if(y != 0) $display("011 failed.");
        a = 1; b = 0; c = 0; #10;
        if(y != 1) $display("100 failed.");
        c = 1;           #10;
        if(y != 1) $display("101 failed.");
        b = 1; c = 0;   #10;
        if(y != 0) $display("110 failed.");
        c = 1;           #10;
        if(y != 0) $display("111 failed.");
    end
endmodule
```

This module checks *y* against expectations after each input test vector is applied. In Verilog, comparison using == or != is effective between signals that do not take on the values of *x* and *z*. Testbenches use the === and !== operators for comparisons of equality and inequality, respectively, because these operators work correctly with operands that could be *x* or *z*. It uses the \$display system task to print a message on the simulator console if an error occurs. \$display is meaningful only in simulation, not synthesis.

##### VHDL

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity testbench2 is -- no inputs or outputs
end;

architecture sim of testbench2 is
    component sillyfunction
        port(a, b, c: in STD_LOGIC;
              y:      out STD_LOGIC);
    end component;
    signal a, b, c, y: STD_LOGIC;
begin
    -- instantiate device under test
    dut: sillyfunction port map (a, b, c, y);

    -- apply inputs one at a time
    -- checking results
    process begin
        a <= '0'; b <= '0'; c <= '0'; wait for 10 ns;
        assert y = '1' report "000 failed.";
        c <= '1';           wait for 10 ns;
        assert y = '0' report "001 failed.";
        b <= '1'; c <= '0';   wait for 10 ns;
        assert y = '0' report "010 failed.";
        c <= '1';           wait for 10 ns;
        assert y = '0' report "011 failed.";
        a <= '1'; b <= '0'; c <= '0'; wait for 10 ns;
        assert y = '1' report "100 failed.";
        c <= '1';           wait for 10 ns;
        assert y = '0' report "101 failed.";
        b <= '1'; c <= '0';   wait for 10 ns;
        assert y = '0' report "110 failed.";
        c <= '1';           wait for 10 ns;
        assert y = '0' report "111 failed.";
        wait; -- wait forever
    end process;
end;
```

The assert statement checks a condition and prints the message given in the report clause if the condition is not satisfied. assert is meaningful only in simulation, not in synthesis.

Writing code for each test vector also becomes tedious, especially for modules that require a large number of vectors. An even better approach is to place the test vectors in a separate file. The testbench simply reads the test vectors from the file, applies the input test vector to the DUT, waits, checks that the output values from the DUT match the output vector, and repeats until reaching the end of the test vectors file.

HDL Example 4.39 demonstrates such a testbench. The testbench generates a clock using an `always/process` statement with no stimulus list, so that it is continuously reevaluated. At the beginning of the simulation, it reads the test vectors from a text file and pulses reset for two cycles. `example.tv` is a text file containing the inputs and expected output written in binary:

```
000_1
001_0
010_0
011_0
100_1
101_1
110_0
111_0
```

#### **HDL Example 4.39 TESTBENCH WITH TEST VECTOR FILE**

##### **Verilog**

```
module testbench3 ();
    reg      clk, reset;
    reg      a, b, c, yexpected;
    wire     y;
    reg[31:0] vectornum, errors;
    reg[3:0]  testvectors [10000:0];

    // instantiate device under test
    sillyfunction dut(a, b, c, y);

    // generate clock
    always
    begin
        clk = 1; #5; clk = 0; #5;
    end

    // at start of test, load vectors
    // and pulse reset
    initial
    begin
        $readmemb ("example.tv", testvectors);
        vectornum = 0; errors = 0;
        reset = 1; #27; reset = 0;
    end

    // apply test vectors on rising edge of clk
    always @ (posedge clk)
    begin
        #1; {a, b, c, yexpected} =
            testvectors[vectornum];
    end

    // check results on falling edge of clk
    always @ (negedge clk)
    if (~reset) begin // skip during reset
        if (y != yexpected) begin
```

##### **VHDL**

```
library IEEE; use IEEE.STD_LOGIC_1164.all;
use STD.TEXTIO.all;

entity testbench3 is -- no inputs or outputs
end;

architecture sim of testbench3 is
    component sillyfunction
        port(a, b, c: in STD_LOGIC;
             y:       out STD_LOGIC);
    end component;
    signal a, b, c, y: STD_LOGIC;
    signal clk, reset: STD_LOGIC;
    signal yexpected: STD_LOGIC;
    constant MEMSIZE: integer := 10000;
    type tvarray is array (MEMSIZE downto 0) of
        STD_LOGIC_VECTOR(3 downto 0);
    signal testvectors: tvarray;
    shared variable vectornum, errors: integer;
begin
    -- instantiate device under test
    dut: sillyfunction port map(a, b, c, y);

    -- generate clock
    process begin
        clk <= '1'; wait for 5 ns;
        clk <= '0'; wait for 5 ns;
    end process;

    -- at start of test, load vectors
    -- and pulse reset
    process is
        file tv: TEXT;
        variable i, j: integer;
        variable L: line;
        variable ch: character;
```

```

$display ("Error: inputs = %b", {a, b, c});
$display (" outputs = %b (%b expected)",
          y, yexpected);
errors = errors + 1;
end
vectornum = vectornum + 1;
if (testvectors[vectornum] === 4'bx) begin
    $display ("%d tests completed with %d errors",
              vectornum, errors);
    $finish;
end
end
endmodule

```

\$readmemb reads a file of binary numbers into the testvectors array. \$readmemh is similar but reads a file of hexadecimal numbers.

The next block of code waits one time unit after the rising edge of the clock (to avoid any confusion if clock and data change simultaneously), then sets the three inputs and the expected output based on the four bits in the current test vector. The next block of code checks the output of the DUT at the negative edge of the clock, after the inputs have had time to propagate through the DUT to produce the output, y. The testbench compares the generated output, y, with the expected output, yexpected, and prints an error if they don't match. %b and %d indicate to print the values in binary and decimal, respectively. For example, \$display ("%b %b", y, yexpected); prints the two values, y and yexpected, in binary. %h prints a value in hexadecimal.

This process repeats until there are no more valid test vectors in the testvectors array. \$finish terminates the simulation.

Note that even though the Verilog module supports up to 10,001 test vectors, it will terminate the simulation after executing the eight vectors in the file.

```

begin
-- read file of test vectors
i := 0;
FILE_OPEN(tv, "example.tv", READ_MODE);
while not endfile(tv) loop
    readline(tv, L);
    for j in 0 to 3 loop
        read(L, ch);
        if (ch = '_') then read(L, ch);
        end if;
        if (ch = '0') then
            testvectors(i)(j) <= '0';
        else testvectors(i)(j) <= '1';
        end if;
    end loop;
    i := i + 1;
end loop;

vectornum := 0; errors := 0;
reset <= '1'; wait for 27 ns; reset <= '0';
wait;
end process;

-- apply test vectors on rising edge of clk
process (clk) begin
    if (clk'event and clk = '1') then
        a <= testvectors(vectornum)(0) after 1 ns;
        b <= testvectors(vectornum)(1) after 1 ns;
        c <= testvectors(vectornum)(2) after 1 ns;
        yexpected <= testvectors(vectornum)(3)
        after 1 ns;
    end if;
end process;

-- check results on falling edge of clk
process (clk) begin
    if (clk'event and clk = '0' and reset = '0') then
        assert y = yexpected
        report "Error: y = " & STD_LOGIC'image(y);
        if (y /= yexpected) then
            errors := errors + 1;
        end if;
        vectornum := vectornum + 1;
        if (is_x(testvectors(vectornum))) then
            if (errors = 0) then
                report "Just kidding --" &
                    integer'image(vectornum) &
                    "tests completed successfully."
                    severity failure;
            else
                report integer'image(vectornum) &
                    "tests completed, errors = " &
                    integer'image(errors)
                    severity failure;
            end if;
        end if;
    end if;
end process;
end;

```

The VHDL code is rather ungainly and uses file reading commands beyond the scope of this chapter, but it gives the sense of what a self-checking testbench looks like.

New inputs are applied on the rising edge of the clock, and the output is checked on the falling edge of the clock. This clock (and reset) would also be provided to the DUT if sequential logic were being tested. Errors are reported as they occur. At the end of the simulation, the testbench prints the total number of test vectors applied and the number of errors detected.

The testbench in HDL Example 4.39 is overkill for such a simple circuit. However, it can easily be modified to test more complex circuits by changing the `example.tv` file, instantiating the new DUT, and changing a few lines of code to set the inputs and check the outputs.

## 4.9 SUMMARY

Hardware description languages (HDLs) are extremely important tools for modern digital designers. Once you have learned Verilog or VHDL, you will be able to specify digital systems much faster than if you had to draw the complete schematics. The debug cycle is also often much faster, because modifications require code changes instead of tedious schematic rewiring. However, the debug cycle can be much *longer* using HDLs if you don't have a good idea of the hardware your code implies.

HDLs are used for both simulation and synthesis. Logic simulation is a powerful way to test a system on a computer before it is turned into hardware. Simulators let you check the values of signals inside your system that might be impossible to measure on a physical piece of hardware. Logic synthesis converts the HDL code into digital logic circuits.

The most important thing to remember when you are writing HDL code is that you are describing real hardware, not writing a computer program. The most common beginner's mistake is to write HDL code without thinking about the hardware you intend to produce. If you don't know what hardware you are implying, you are almost certain not to get what you want. Instead, begin by sketching a block diagram of your system, identifying which portions are combinational logic, which portions are sequential circuits or finite state machines, and so forth. Then write HDL code for each portion, using the correct idioms to imply the kind of hardware you need.

## Exercises

---

The following exercises may be done using your favorite HDL. If you have a simulator available, test your design. Print the waveforms and explain how they prove that it works. If you have a synthesizer available, synthesize your code. Print the generated circuit diagram, and explain why it matches your expectations.

**Exercise 4.1** Sketch a schematic of the circuit described by the following HDL code. Simplify the schematic so that it shows a minimum number of gates.

Verilog	VHDL
<pre>module exercisel(input a, b, c,                   output y, z);    assign y = a &amp; b &amp; c   a &amp; b &amp; ~c   a &amp; ~b &amp; c;   assign z = a &amp; b   ~a &amp; ~b; endmodule</pre>	<pre>library IEEE; use IEEE.STD_LOGIC_1164.all;  entity exercisel is   port(a, b, c: in STD_LOGIC;        y, z: out STD_LOGIC); end;  architecture synth of exercisel is begin   y &lt;= (a and b and c) or (a and b and (not c)) or         (a and (not b) and c);   z &lt;= (a and b) or ((not a) and (not b)); end;</pre>

**Exercise 4.2** Sketch a schematic of the circuit described by the following HDL code. Simplify the schematic so that it shows a minimum number of gates.

Verilog	VHDL
<pre>module exercise2(input      [3:0] a,                   output reg [1:0] y);    always @(*)     if      (a[0]) y = 2'b11;     else if(a[1]) y = 2'b10;     else if(a[2]) y = 2'b01;     else if(a[3]) y = 2'b00;     else          y = a[1:0]; endmodule</pre>	<pre>library IEEE; use IEEE.STD_LOGIC_1164.all;  entity exercise2 is   port(a: in STD_LOGIC_VECTOR(3 downto 0);        y: out STD_LOGIC_VECTOR(1 downto 0)); end;  architecture synth of exercise2 is begin   process (a)begin     if      a(0) = '1' then y &lt;= "11";     elsif a(1) = '1' then y &lt;= "10";     elsif a(2) = '1' then y &lt;= "01";     elsif a(3) = '1' then y &lt;= "00";     else                  y &lt;= a(1 downto 0);     end if;   end process; end;</pre>

**Exercise 4.3** Write an HDL module that computes a four-input XOR function. The input is  $a_{3:0}$ , and the output is  $y$ .

**Exercise 4.4** Write a self-checking testbench for Exercise 4.3. Create a test vector file containing all 16 test cases. Simulate the circuit and show that it works. Introduce an error in the test vector file and show that the testbench reports a mismatch.

**Exercise 4.5** Write an HDL module called `minority`. It receives three inputs, `a`, `b`, and `c`. It produces one output, `y`, that is TRUE if at least two of the inputs are FALSE.

**Exercise 4.6** Write an HDL module for a hexadecimal seven-segment display decoder. The decoder should handle the digits A, B, C, D, E, and F as well as 0–9.

**Exercise 4.7** Write a self-checking testbench for Exercise 4.6. Create a test vector file containing all 16 test cases. Simulate the circuit and show that it works. Introduce an error in the test vector file and show that the testbench reports a mismatch.

**Exercise 4.8** Write an 8:1 multiplexer module called `mux8` with inputs `s2:0`, `d0`, `d1`, `d2`, `d3`, `d4`, `d5`, `d6`, `d7`, and output `y`.

**Exercise 4.9** Write a structural module to compute the logic function,  $y = a\bar{b} + \bar{b}\bar{c} + \bar{a}bc$ , using multiplexer logic. Use the 8:1 multiplexer from Exercise 4.8.

**Exercise 4.10** Repeat Exercise 4.9 using a 4:1 multiplexer and as many NOT gates as you need.

**Exercise 4.11** Section 4.5.4 pointed out that a synchronizer could be correctly described with blocking assignments if the assignments were given in the proper order. Think of a simple sequential circuit that cannot be correctly described with blocking assignments, regardless of order.

**Exercise 4.12** Write an HDL module for an eight-input priority circuit.

**Exercise 4.13** Write an HDL module for a 2:4 decoder.

**Exercise 4.14** Write an HDL module for a 6:64 decoder using three instances of the 2:4 decoders from Exercise 4.13 and a bunch of three-input AND gates.

**Exercise 4.15** Write HDL modules that implement the Boolean equations from Exercise 2.7.

**Exercise 4.16** Write an HDL module that implements the circuit from Exercise 2.18.

**Exercise 4.17** Write an HDL module that implements the logic function from Exercise 2.19. Pay careful attention to how you handle don't cares.

**Exercise 4.18** Write an HDL module that implements the functions from Exercise 2.24.

**Exercise 4.19** Write an HDL module that implements the priority encoder from Exercise 2.25.

**Exercise 4.20** Write an HDL module that implements the binary-to-thermometer code converter from Exercise 2.27.

**Exercise 4.21** Write an HDL module implementing the days-in-month function from Question 2.2.

**Exercise 4.22** Sketch the state transition diagram for the FSM described by the following HDL code.

#### Verilog

```
module fsm2(input clk, reset,
            input a, b,
            output y);
    reg [1:0] state, nextstate;
    parameter S0 = 2'b00;
    parameter S1 = 2'b01;
    parameter S2 = 2'b10;
    parameter S3 = 2'b11;
    always @ (posedge clk, posedge reset)
        if (reset) state <= S0;
        else      state <= nextstate;
    always @ (*)
        case (state)
            S0: if(a ^ b) nextstate = S1;
                 else      nextstate = S0;
            S1: if(a & b) nextstate = S2;
                 else      nextstate = S0;
            S2: if(a | b) nextstate = S3;
                 else      nextstate = S0;
            S3: if(a | b) nextstate = S3;
                 else      nextstate = S0;
        endcase
        assign y = (state == S1) | (state == S2);
endmodule
```

#### VHDL

```
library IEEE; use IEEE.STD_LOGIC_1164.all;
entity fsm2 is
    port(clk, reset: in STD_LOGIC;
          a, b:      in STD_LOGIC;
          y:         out STD_LOGIC);
end;
architecture synth of fsm2 is
    type statetype is(S0, S1, S2, S3);
    signal state, nextstate: statetype;
begin
    process(clk, reset) begin
        if reset = '1' then state <= S0;
        elsif clk'event and clk = '1' then
            state <= nextstate;
        end if;
    end process;
    process(state, a, b)begin
        case state is
            when S0 => if(a xor b) = '1' then
                nextstate <= S1;
                else nextstate <= S0;
            end if;
            when S1 => if(a and b) = '1' then
                nextstate <= S2;
                else nextstate <= S0;
            end if;
            when S2 => if(a or b) = '1' then
                nextstate <= S3;
                else nextstate <= S0;
            end if;
            when S3 => if(a or b) = '1' then
                nextstate <= S3;
                else nextstate <= S0;
            end if;
        end case;
    end process;
    y <= '1' when ((state = S1) or (state = S2))
              else '0';
end;
```

**Exercise 4.23** Sketch the state transition diagram for the FSM described by the following HDL code. An FSM of this nature is used in a branch predictor on some microprocessors.

**Verilog**

```
module fsm1 (input  clk, reset,
              input  taken, back,
              output predicttaken);

  reg [4:0] state, nextstate;

  parameter S0 = 5'b00001;
  parameter S1 = 5'b00010;
  parameter S2 = 5'b00100;
  parameter S3 = 5'b01000;
  parameter S4 = 5'b10000;

  always @ (posedge clk, posedge reset)
    if(reset) state <= S2;
    else      state <= nextstate;

  always @ (*)
    case(state)
      S0: if(taken) nextstate = S1;
           else      nextstate = S0;
      S1: if(taken) nextstate = S2;
           else      nextstate = S0;
      S2: if(taken) nextstate = S3;
           else      nextstate = S1;
      S3: if(taken) nextstate = S4;
           else      nextstate = S2;
      S4: if(taken) nextstate = S4;
           else      nextstate = S3;
      default: nextstate = S2;
    endcase

    assign predicttaken = (state == S4) || |
                        (state == S3) || |
                        (state == S2 && back);
  endmodule
```

**VHDL**

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity fsm1 is
  port (clk, reset:  in STD_LOGIC;
        taken, back: in STD_LOGIC;
        predicttaken: out STD_LOGIC);
end;

architecture synth of fsm1 is
  type statetype is (S0, S1, S2, S3, S4);
  signal state, nextstate: statetype;
begin
  process (clk, reset) begin
    if reset = '1' then state <= S2;
    elsif clk'event and clk = '1' then
      state <= nextstate;
    end if;
  end process;

  process (state, taken) begin
    case state is
      when S0 => if taken = '1' then
                    nextstate <= S1;
                  else nextstate <= S0;
                  end if;
      when S1 => if taken = '1' then
                    nextstate <= S2;
                  else nextstate <= S0;
                  end if;
      when S2 => if taken = '1' then
                    nextstate <= S3;
                  else nextstate <= S1;
                  end if;
      when S3 => if taken = '1' then
                    nextstate <= S4;
                  else nextstate <= S2;
                  end if;
      when S4 => if taken = '1' then
                    nextstate <= S4;
                  else nextstate <= S3;
                  end if;
      when others => nextstate <= S2;
    end case;
  end process;

  -- output logic
  predicttaken <= '1' when
    ((state = S4) or (state = S3) or
     (state = S2 and back = '1'))
    else '0';
end;
```

**Exercise 4.24** Write an HDL module for an SR latch.

**Exercise 4.25** Write an HDL module for a *JK flip-flop*. The flip-flop has inputs, *clk*, *J*, and *K*, and output *Q*. On the rising edge of the clock, *Q* keeps its old value if *J* = *K* = 0. It sets *Q* to 1 if *J* = 1, resets *Q* to 0 if *K* = 1, and inverts *Q* if *J* = *K* = 1.

**Exercise 4.26** Write an HDL module for the latch from Figure 3.18. Use one assignment statement for each gate. Specify delays of 1 unit or 1 ns to each gate. Simulate the latch and show that it operates correctly. Then increase the inverter delay. How long does the delay have to be before a race condition causes the latch to malfunction?

**Exercise 4.27** Write an HDL module for the traffic light controller from Section 3.4.1.

**Exercise 4.28** Write three HDL modules for the factored parade mode traffic light controller from Example 3.8. The modules should be called *controller*, *mode*, and *lights*, and they should have the inputs and outputs shown in Figure 3.33(b).

**Exercise 4.29** Write an HDL module describing the circuit in Figure 3.40.

**Exercise 4.30** Write an HDL module for the FSM with the state transition diagram given in Figure 3.65 from Exercise 3.19.

**Exercise 4.31** Write an HDL module for the FSM with the state transition diagram given in Figure 3.66 from Exercise 3.20.

**Exercise 4.32** Write an HDL module for the improved traffic light controller from Exercise 3.21.

**Exercise 4.33** Write an HDL module for the daughter snail from Exercise 3.22.

**Exercise 4.34** Write an HDL module for the soda machine dispenser from Exercise 3.23.

**Exercise 4.35** Write an HDL module for the Gray code counter from Exercise 3.24.

**Exercise 4.36** Write an HDL module for the UP/DOWN Gray code counter from Exercise 3.25.

**Exercise 4.37** Write an HDL module for the FSM from Exercise 3.26.

**Exercise 4.38** Write an HDL module for the FSM from Exercise 3.27.

**Exercise 4.39** Write an HDL module for the serial two's completer from Question 3.2.

**Exercise 4.40** Write an HDL module for the circuit in Exercise 3.28.

**Exercise 4.41** Write an HDL module for the circuit in Exercise 3.29.

**Exercise 4.42** Write an HDL module for the circuit in Exercise 3.30.

**Exercise 4.43** Write an HDL module for the circuit in Exercise 3.31. You may use the full adder from Section 4.2.5.

### Verilog Exercises

The following exercises are specific to Verilog.

**Exercise 4.44** What does it mean for a signal to be declared `reg` in Verilog?

**Exercise 4.45** Rewrite the `syncbad` module from HDL Example 4.30. Use nonblocking assignments, but change the code to produce a correct synchronizer with two flip-flops.

**Exercise 4.46** Consider the following two Verilog modules. Do they have the same function? Sketch the hardware each one implies.

```
module code1 (input      clk, a, b, c,
               output reg y);
    reg x;

    always @ (posedge clk) begin
        x <= a & b;
        y <= x | c;
    end
endmodule

module code2 (input      a, b, c, clk,
               output reg y);
    reg x;

    always @ (posedge clk) begin
        y <= x | c;
        x <= a & b;
    end
endmodule
```

**Exercise 4.47** Repeat Exercise 4.46 if the `<=` is replaced by `=` in every assignment.

**Exercise 4.48** The following Verilog modules show errors that the authors have seen students make in the laboratory. Explain the error in each module and show how to fix it.

```
(a) module latch (input      clk,
                  input [3:0] d,
                  output reg [3:0] q);

  always @ (clk)
    if (clk) q <= d;
endmodule

(b) module gates (input [3:0] a, b,
                  output reg [3:0] y1, y2, y3, y4, y5);

  always @ (a)
  begin
    y1 = a & b;
    y2 = a | b;
    y3 = a ^ b;
    y4 = ~(a & b);
    y5 = ~(a | b);
  end
endmodule

(c) module mux2 (input [3:0] d0, d1,
                  input s,
                  output reg [3:0] y);

  always @ (posedge s)
    if (s) y <= d1;
    else y <= d0;
endmodule

(d) module twoflops (input      clk,
                     input      d0, d1,
                     output reg q0, q1);

  always @ (posedge clk)
    q1 = d1;
    q0 = d0;
endmodule
```

```
(e) module FSM(input      clk,
                input      a,
                output reg out1, out2);

    reg state;

    // next state logic and register (sequential)
    always @ (posedge clk)
        if(state == 0) begin
            if(a) state <= 1;
        end else begin
            if(~a) state <= 0;
        end

    always @ (*) // output logic (combinational)
        if(state == 0) out1 = 1;
        else           out2 = 1;
endmodule

(f) module priority(input      [3:0] a,
                     output reg [3:0] y);

    always @ (*)
        if      (a[3]) y = 4'b1000;
        else if(a[2]) y = 4'b0100;
        else if(a[1]) y = 4'b0010;
        else if(a[0]) y = 4'b0001;
endmodule

(g) module divideby3FSM(input  clk,
                        input  reset,
                        output out);

    reg [1:0] state, nextstate;

    parameter S0 = 2'b00;
    parameter S1 = 2'b01;
    parameter S2 = 2'b10;

    // State Register
    always @ (posedge clk, posedge reset)
        if(reset) state <= S0;
        else      state <= nextstate;

    // Next State Logic
    always @ (state)
        case(state)
            S0: nextstate = S1;
            S1: nextstate = S2;
            2: nextstate = S0;
        endcase

    // Output Logic
    assign out = (state == S2);
endmodule
```

```
(h) module mux2tri(input [3:0] d0, d1,
                     input      s,
                     output [3:0] y);

    tristate t0(d0, s, y);
    tristate t1(d1, s, y);
endmodule

(i) module floprsen(input          clk,
                     input          reset,
                     input          set,
                     input [3:0] d,
                     output reg [3:0] q);

    always @ (posedge clk, posedge reset)
        if(reset) q <= 0;
        else     q <= d;

    always @ (set)
        if(set)  q <= 1;
endmodule

(j) module and3(input      a, b, c,
                  output reg y);

    reg tmp;

    always @ (a, b, c)
    begin
        tmp <= a & b;
        y   <= tmp & c;
    end
endmodule
```

### VHDL Exercises

The following exercises are specific to VHDL.

**Exercise 4.49** In VHDL, why is it necessary to write

`q <= '1' when state = S0 else '0';`

rather than simply

`q <= (state = S0);`