Assignment 1, Operating Systems

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1.1

Address	Data
100	3*dev1*
101	5940
102	7*dev6*
940	0002
dev5	0003

Where *devX* is the I/O instruction for that device.

	Fetch		Execute	
Step 1	PC	100	PC	101
	AC		AC	0003
	IR	3*dev5*	IR	3*dev5*
Step 2	PC	101	PC	102
	AC	0003	AC	0005
	IR	5940	IR	5940
Step 3	PC	102	PC	103
	AC	0005	AC	0005
	IR	7*dev6*	IR	7*dev6*

1.2 I could not find or remember specific details on these, so this is my best guess:

Step 1 Fetch MAR = 940, MBR = 0003
Execute MAR = 000, MBR = 0000

Step 2 Fetch MAR = 941, MBR = 0002
Execute MAR = 000, MBR = 0000

Step 3 Fetch MAR = 941, MBR = 0005
Execute MAR = 000, MBR = 0000

1.3 (a) 2^{24}

(b) If our data bus transports only 16 bits and our data is 32 bits long, then we will need two fetch steps for every instruction cycle.
If our address bus transports only 16 bits, then we will still need two fetch steps.
I am unsure what the expected answer is on this one.

(c) 24 and 32

1.4 (a) 2^{16}

(b) 2^8

(c) Instructions for accessing IO modules.

(d) 2^8 and 2^{16}

1.6 (a) For input, give the CPU a load command along with the input register and enable the FGI input flag. For output, give the CPU a store command with the output register and the FGO flag enabled.

(b) By using IEN, the processor can be signalled to activate an IO process and continue to go through instructions while the IO process runs.

1.7 To ensure that user data that needs to be saved is saved?

1.10 (a) i and j will have neighboring memory locations and will be accessed together in every assignment.

(b) The assignment to $a[i]$ will occur on every iteration.