

10-1 SAP-1 architecture.

00111110,0011 NOP

TABLE 10-1. SAP-1 INSTRUCTION SET

Mnemonic	Operation		
LDA	Load RAM data into accumulator		
ADD	Add RAM data to accumulator		
SUB	Subtract RAM data from accumulator		
OUT	Load accumulator data into output register		
HLT	Stop processing		

TABLE 10-2. SAP-1 OP CODE

Mnemonic	Op code	
LDA	0000	
ADD	0001 0010	
SUB		
OUT	1110	
HLT	1111	

Instr Fatch

State	CON	Active Bits	3
<i>T</i> ₁	5E3H	E_{P}, \overline{L}_{M} C_{P}	Mare
T_2	BE3H	C_{P}	PLEP
T_3	263H	\overline{CE} , \overline{L}_{I}	IRE

TABLE 10-5. SAP-1 MICROPROGRAM†

Macro	State	CON	Active	
LDA	T4	1A3H	\overline{L}_M , \overline{E}_1	Mark IRy A + Mer
	T_5	2C3H	\overline{CE} , \overline{L}_{A}	A < Mer
	T_6	3E3H	None	
ADD	T_{4}	1A3H	\overline{L}_M , \overline{E}_I	Mare IR
	T_{5}	2E1H	\overline{CE} . \overline{L}_B	B & Mei
	T_6	3C7H	\overline{L}_{A} , E_{U}	
SUB	T_{ullet}	1A3H	$\overline{L}_{M}, \overline{E}_{I}$	Mar & IR B & Me E, A & Aluc-
	T ₅	2E1H	\overline{CE} , \overline{L}_{B}	B & Me
	T_6	3CFH	\overline{L}_{A} , S_{U} , I	•
OUT	T_{\bullet}	3F2H	E_A , \overline{L}_O	0 < A
	T_5	3E3H	None	
	T_6	3E3H	None	

 $\dagger \ \mathbf{CON} = \ \mathbf{C_PE_P\overline{L_M}\overline{CE}} \quad \overline{\mathbf{L_I}}\overline{\mathbf{E_I}}\overline{\mathbf{L}_A}\mathbf{E_A} \quad \mathbf{S_UE_U}\overline{\mathbf{L_B}}\overline{\mathbf{L}_O}.$