## Sample and hold circuit :-

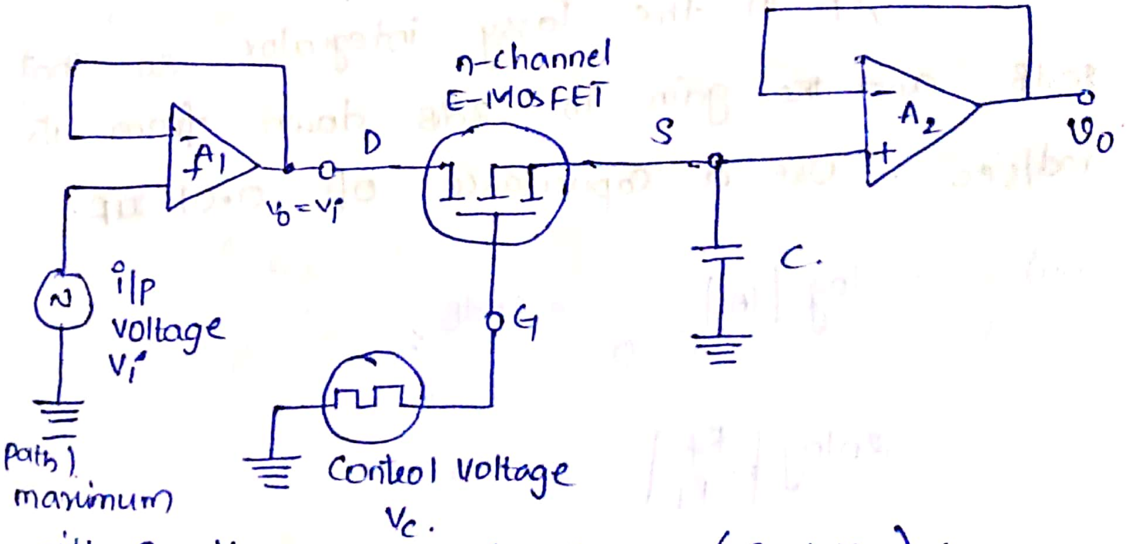
A sample and hold ckt samples an input signal and holds on to its last sampled value until the input sampled again. This type of ckt is very useful in digital interfacing and analog to digital and pulse code modulation. systems. An n-channel E-MOSFET is used as a switch and is controlled by a control voltage $V_c$. which is connected to gate of E-MOSFET. the i/p signal $V_i$ to be sampled. is applied at drain. The capacitor C stores the charge.

2 - Voltage follower op-Amp ckts are Present.

When $V_c$ - positive.

E MOSFET turns ON. (short circuited path)

Capacitor charge to a maximum value of input voltage with a time constant $RC = (R_o + r_{ds})C$




$R_o$ - O/P resistance of voltage follower $A_1$

$r_{DS}$ - Resistance of MOSFET when ON.

$\therefore V_0 = V_i$ ($\because A_2$ is voltage follower $V_0 = V_i$).

$V_i$ – Voltage across

When $V_c$ – OFF '0' volts

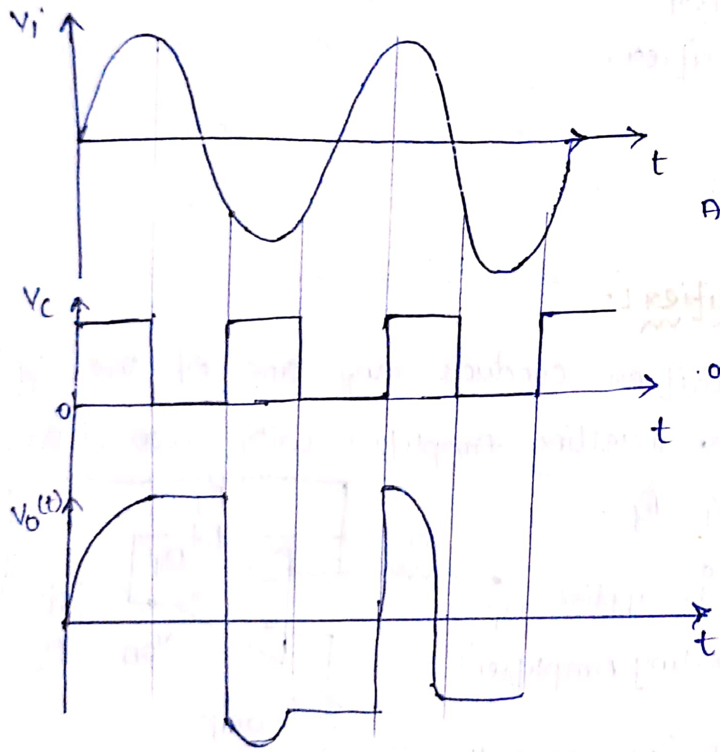
E-MOSFET turns to OFF.

Now Capacitor facing high input impedence from Voltage A and hence Cannot discharge. The Capacitor holds the volt. across it.

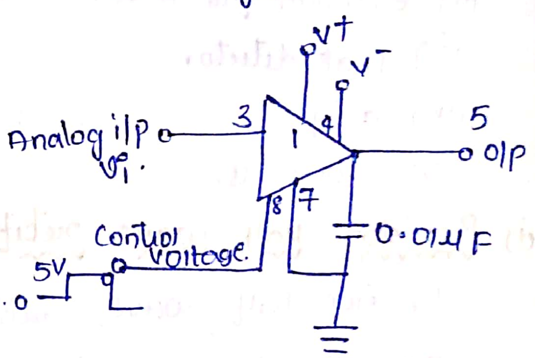
→ The time period during which voltage across Capacitor is equal to input voltage is called Sampling period ($T_S$).

→ The time period of $V_c$ during which the voltage across the capacitor is held Constant is called hold period ($T_H$).

→ The frequency of control voltage should be kept higher than (atleast twice) the input so as to retrive the input from output waveform.




Typical Connection Using LF398

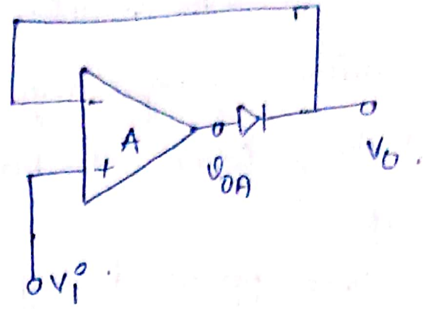


using diodes:-

The circuit which rectifies the input signal in order of mV or μV is called Precision diode.

(29)

A simple voltage divider circuit with a diode at output.




$$A = \frac{V_{OA}}{V_i} \Rightarrow V_{OA} = V_i A.$$

generally gain $A = 10^3$.

$$V_{OA} = 10^3 V_i$$

$$V_i = \frac{10 V_{OA}}{10^3} \Rightarrow V_i = V_{OA}\frac{0.7}{10^3}.$$ cut in voltage of a diode

$V_i = 0.7mV$, or $700\mu V$.

The Precision diode can also respond for a small voltages in order of m & μ volts.

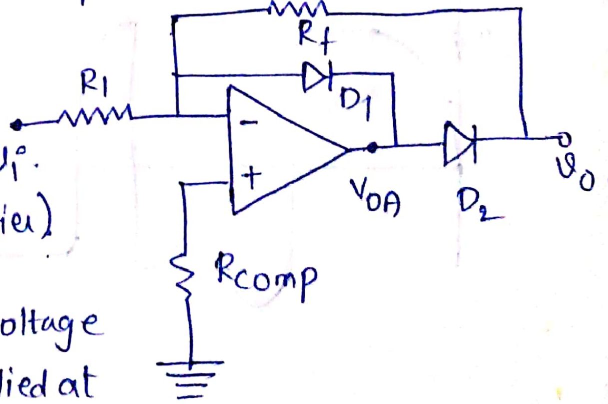
Applications:-

(i) Precision half wave rectifier
(ii) Precision full wave rectifier.
(iii) Peak detector.
(iv) clippers.
(V) clampers.

(i) Precision Half wave rectifier:-

Precision half wave rectifier conducts any one of the cycle.

The circuit represents an inverting Amplifier with two diodes $D_1$ and $D_2$ here Resistors $R_1 = R_f$.




(i) When positive half cycle is applied.

then $V_{OA} = -V_i$ (∵ inverting Amplifier)

$\Rightarrow D_1$ - ON $\quad D_2$ - OFF (∵ -ve voltage is applied at anode of $D_2$).

∴ $V_o = 0$.

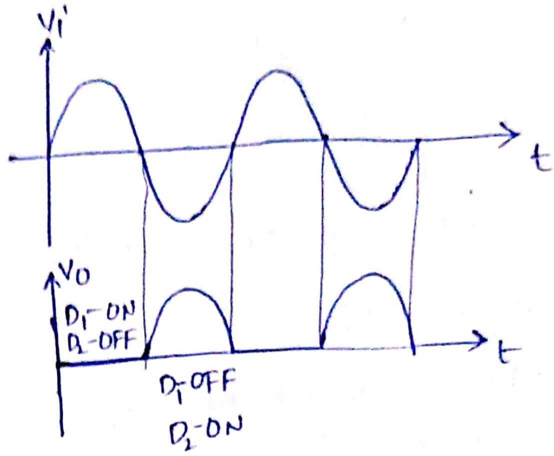
Negative half cycle is applied.

$V_{OA} = +V_i$.

$D_1$ - OFF (∵ -ve supply voltage is give to Positive terminal of Diode $D_2$. So, diode do not conducts).

$D_2$ - ON.

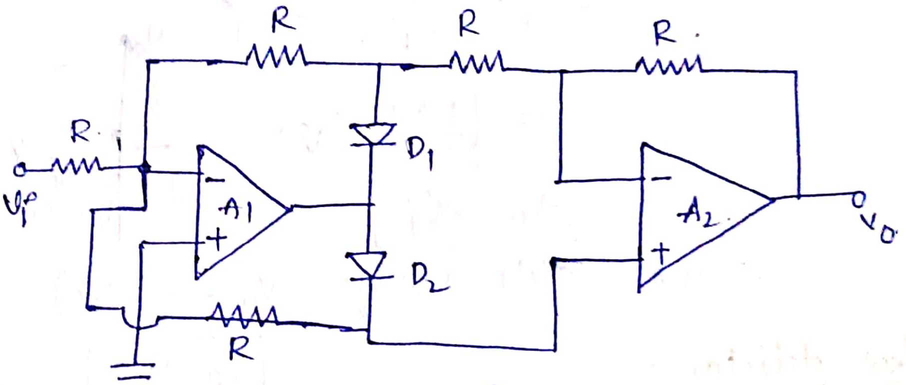
$V_{OA} = +V_i \Rightarrow \boxed{V_O = +V_i}$




(ii) Precision full wave rectifier :-

A full wave rectifier is also called as absolute value circuit. The input is applied across the inverting terminal of op-amp.

for easy Analysis consider all the Resistor values are equal.

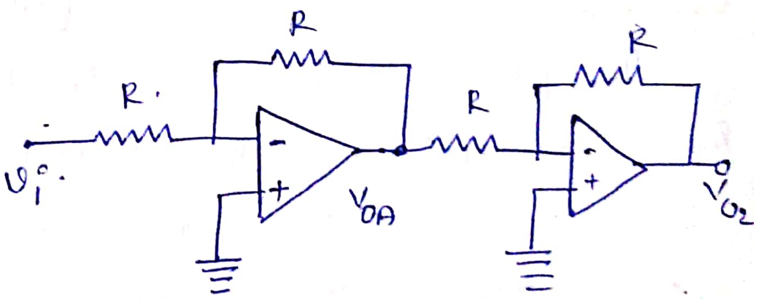



Case(i)

$V_i$ = +ve half cycle.

$D_1$ = ON ; $D_2$ = OFF

then ckt o/p becomes



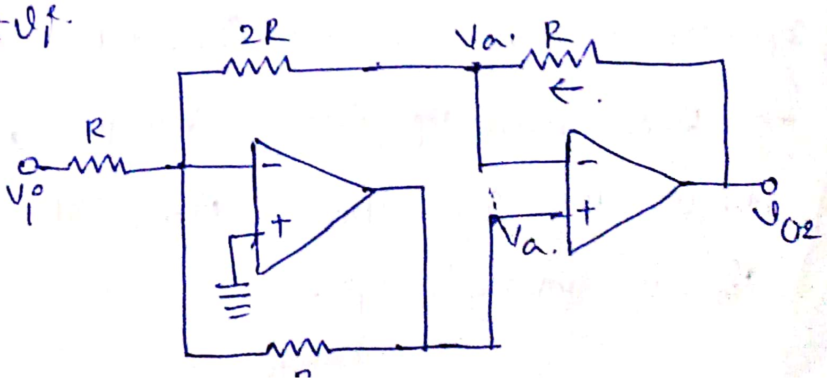

$\boxed{V_{O2} = V_i}$

Since voltage at $V_{OA}$ is $-V_i$ is applied to inverting Amplifier $A_2$ therefore o/p voltage $V_{O2} = +V_i$.

Case (ii) :-

$V_i$ = -ve half cycle.

$D_1$ - OFF ; $D_2$ - ON.



$$\frac{v_i - 0}{R} + \frac{V_a - 0}{2R} + \frac{V_a - 0}{R} = 0$$

$$\frac{2v_i + V_a + 2V_a = 0}{2R}$$

$$3V_a = 2v_i$$

$$\boxed{V_a = \frac{-2v_i}{3}}$$

The $A_2$ Op-amp amplifier acts as a non-inverting amplifier because the o/p voltage of $A_1$ op-amp is applied across non-inverting terminal of $A_2$.

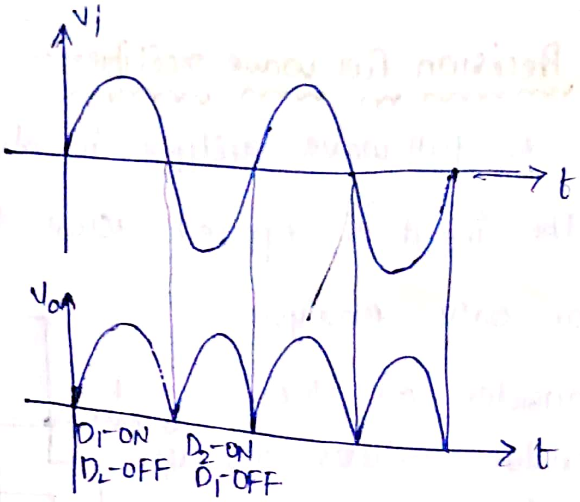
Find op-amp o/p

$$v_o = \left(1 + \frac{R_f}{R_1}\right) V_a$$

$$= \left(1 - \frac{R}{2R}\right) \frac{-2}{3} v_i$$

$$= \left(\frac{3}{2}\right)\left(\frac{-2}{3}\right) v_i$$

$$\boxed{v_o = -v_i}$$

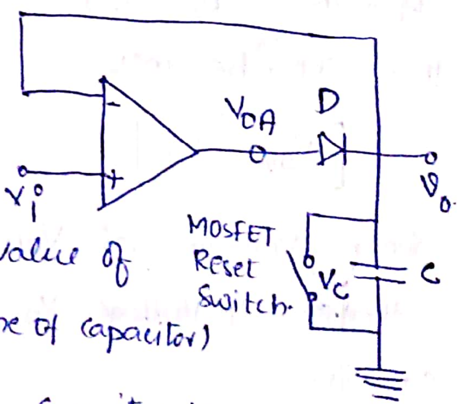



$\therefore$ Total o/p voltage $V_o = -(-v_i)$

$$\boxed{V_o = v_i}$$

Peak detector :-

The peak detector is used to detect the Highest Peak of The input signal ($v_i$). The highest peak voltage signal value is stored on a Capacitor. if Next highes peak comes along then the New value is stored Otherwise the value of capacitor remains Constant (i.e., discharging time of capacitor)



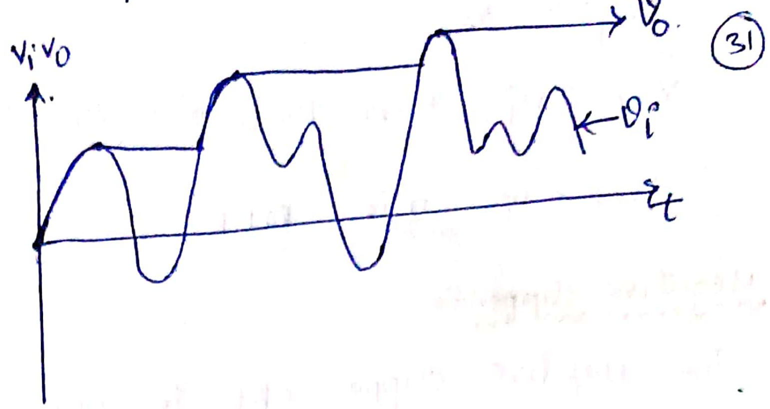

→ When input $v_i$ Exceeds Voltage across Capacitor $V_c$ the diode is forward bias. then ckt acts as an voltage follower $v_o$ is similar to $v_i$.

drops below $V_c$, the diode is reverse bias and capacitor

the Same ~~vol~~ charge till input voltage again attains a

voltage greater than $V_c$.






→ The Capacitor voltage is made zero by placing a leaking MOSFET Switch across it.

**Application:-**

→ Test and measurement Instrumentation.

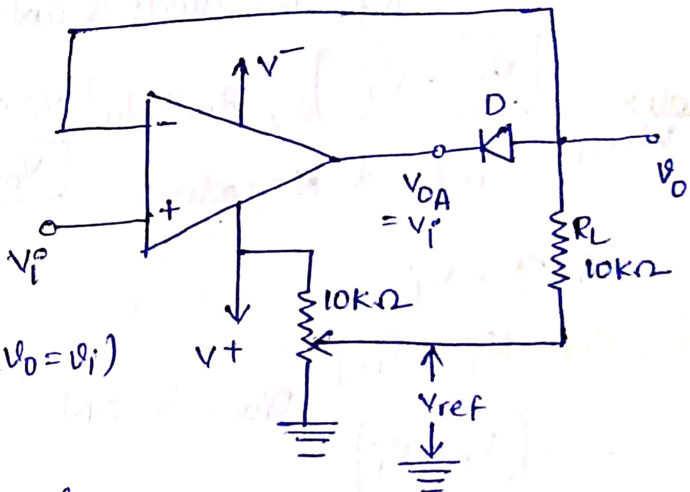
→ Amplitude modulation (AM) communications.

**clipper:-**

A Precision diode may also be used to clip-off a certain portion of the i/p signal to obtain a desired output waveform.

**Positive clipper:-**

The clipping level is determined by the reference Voltage $V_{ref}$ and could be obtained from the Positive supply voltage $V^+$. The ckt represents an voltage follower ckt. $(V_0 = V_i)$




Case(i)

When $V_{ref}$ is positive.

The o/p at $V_{OA} = V_i$.

i/p voltage $V_i < V_{ref}$, then Diode D is ON.

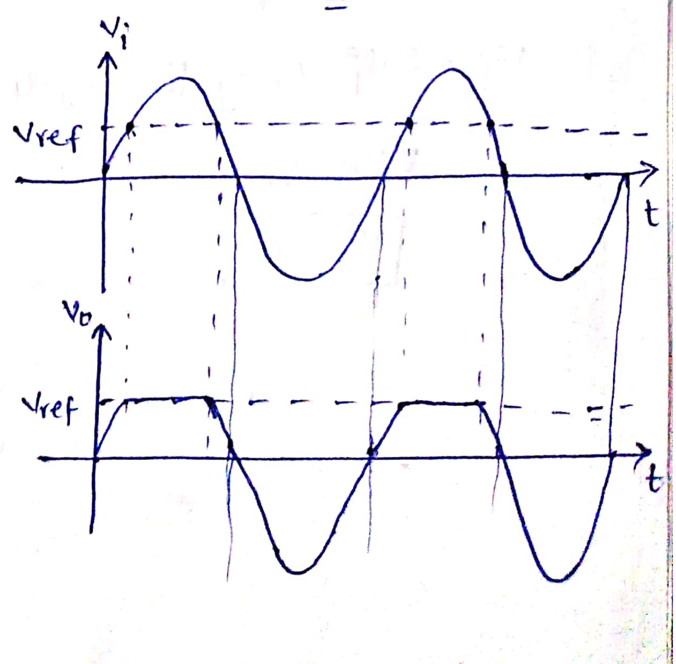
therefore output voltage

$$\boxed{V_0 = V_{ref}}$$

if $V_i > V_{ref}$ the Diode D is OFF

o/p Voltage

$$\boxed{V_0 = 0V}$$



Case(ii):-

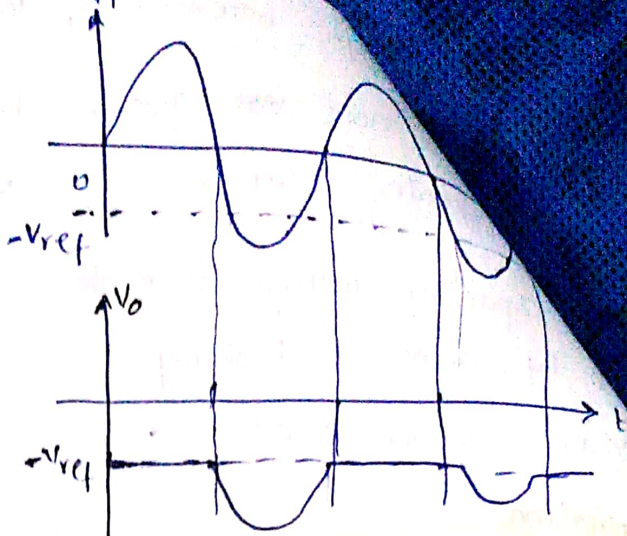
When $V_{ref}$ is Negative supply.

Similarly

$V_{ref} = -V_e.$

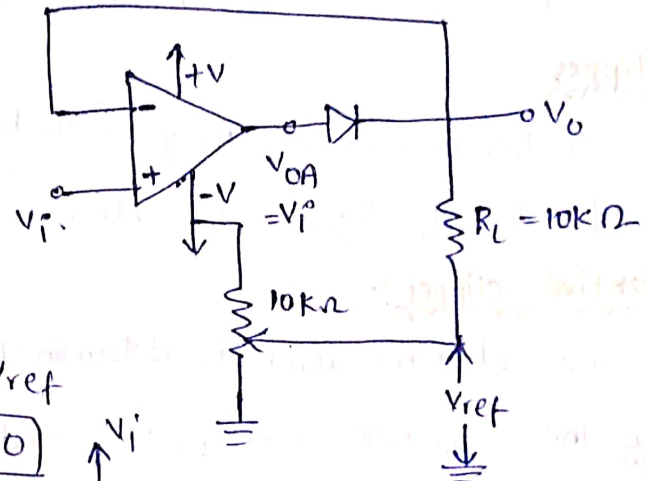
$V_{ref} > V_i$ then Diode D is ON.

$V_{ref} < V_i$ D is OFF




Negative clipper:-

The Negative clipper ckt is obtained simply by placing the Diode reverse and changing the polarities of the reference voltage. The input is applied across the Non-inverting terminal.




Case(i):-

When $V_{ref}$ is positive.

$V_i > V_{ref}$ then diode is ON.

$\boxed{V_o = V_i}$ ; Similarly $V_i < V_{ref}$ $\boxed{V_o = 0}$

Case(ii):- When $V_{ref}$ is Negative.

$V_i = +V_i$

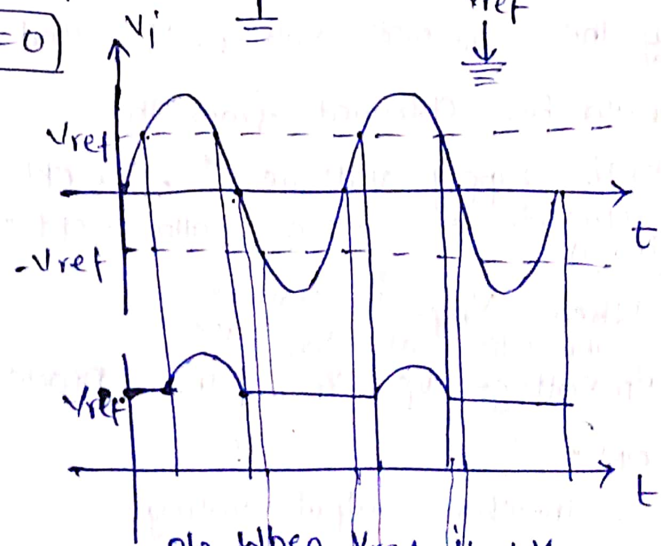
$V_i > V_{ref}$ Diode is ON

$\boxed{V_o = V_i}$

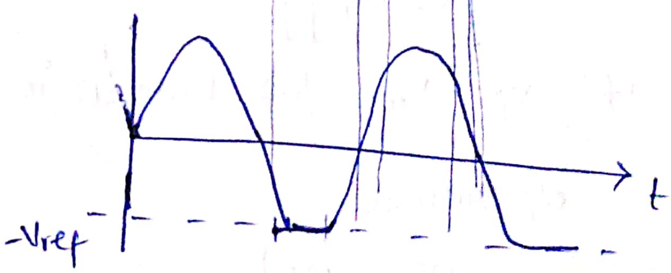
$V_i = -V_i$ (Negative cycle).

$V_i < V_{ref}$

$\boxed{V_o = 0}$




o/p when $V_{ref}$ is +Ve.




o/p W/F when $V_{ref}$ is -Ve.

...per is also known as dc inserter (or) restorer. The circuit is ... add a desired dc level to the output voltage.

(or)

The output is clamped to a desired dc level.

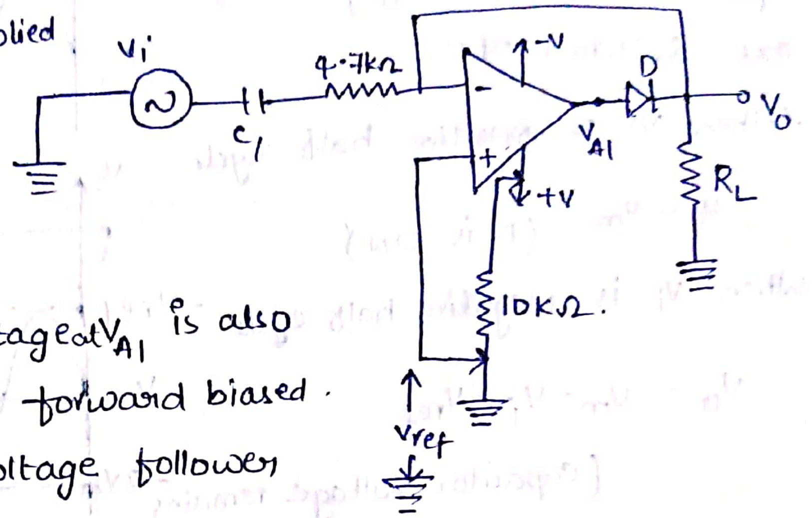
→ if clamped dc level is positive, it is called positive clamper.

→ if clamped dc level is Negative, then it is called Negative clamper.

Positive clamping circuit

→ The input signal $V_i$ is applied at inverting terminal.

→ The reference voltage ($V_{ref}$) is applied at +ve i/p terminal.



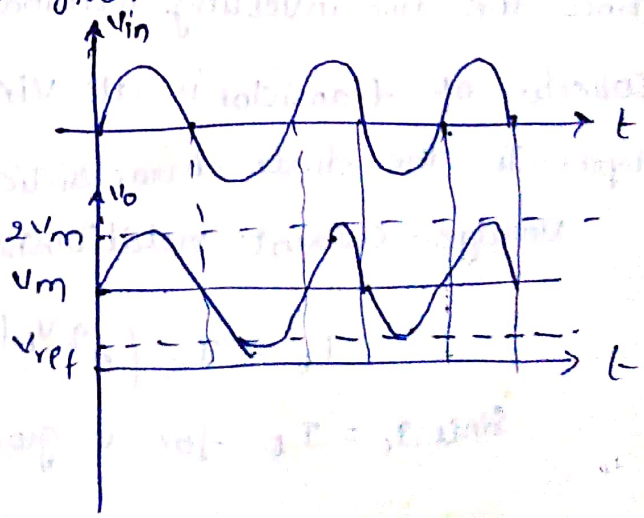

→ for positive $V_{ref}$ the voltage at $V_{A1}$ is also Positive, so that the diode is forward biased. The circuit operates as a voltage follower therefore output voltage

$$V_o = +V_{ref}$$

Now consider ac input signal $V_i = V_m \sin\omega t$. During negative half cycle of $V_i$, diode D conducts. The capacitor $C_1$ charges through diode D to a Negative peak voltage $V_m$.

During the positive half cycle of $V_i$ diode D is reverse biased the capacitor voltage remains constant ($V_m$). Since $V_m$ is in series with input voltage then output voltage is given as

$$V_o = V_m + V_{ref} + V_{in}$$



## Negative clamper ckt :-

Negative peak clamper is obtained by reversing the Diode D and a negative reference voltage $-V_{ref}$. The Resistor R is placed to protect the op-amp against excessive discharge currents from capacitor $C_1$ when supply voltages are switched off.

When $V_i$ is positive half cycle.

$V_o = V_m$. (D is ON)

When $V_i$ is Negative half cycle

$V_o = V_m - V_i - V_{ref}$

(Capacitor Voltage remains constant)

### Negative peak clamping