8/11

U-5 Synchronous Sequential Ckt Design
Asynchronous " " "

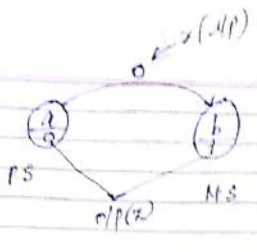
* Synchronous Sequential Ckt Design –

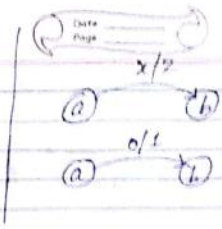
It is analysed by using two model /machine
(M/c – Moore m/c
– Mealy m/c)

Difference b/w Moore M/c & Mealy M/c

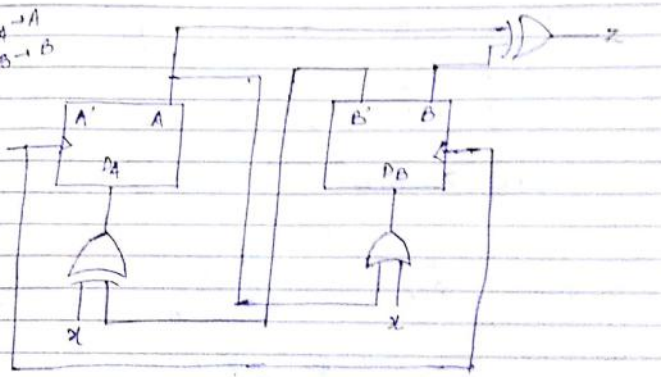
	Moore M/c	Mealy M/c
1	O/p Z depends upon only in present state (Q_n); [$Z = f(Q)$]	1. O/p depends upon present i/p as well as in i/p (x) ; [$Z = f(Q, x)$]
	2. If i/p changes, o/p doesn't change	2. If i/p changes, o/p Z also changes
	More number of states are required	3 Less number of states are required.
	Hardware requirement is more	4. Less
	A counter is Moore m/c	5 A counter is not Mealy M/c.

6.





Q. Analyse the following given sequential synchronous Ckt to determine whether this is an example of Mealy M/c or Moore M/c.
Draw state table.
Draw state diagram.



$D_A = x \oplus B = x \odot B$
$D_B = x + A$
$Z = A \oplus B$

O/p Z depends upon only in present states A & B so it is an example of Moore M/c

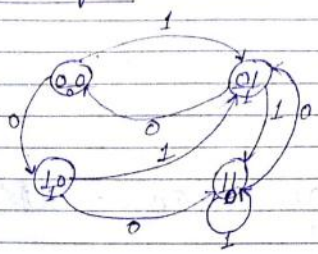
$\because Q_{n+1} = D$ (from excitation table of D ff) so $A^+ = D_A = x \odot B$ (NS)

$B^+ = D_B = x + A$

State table

PS: A	PS: B	i/p: x	NS: A^+	NS: B^+	o/p: Z
0	0	0	1	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	1
1	0	0	1	1	1
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	1	1	0

State diagram

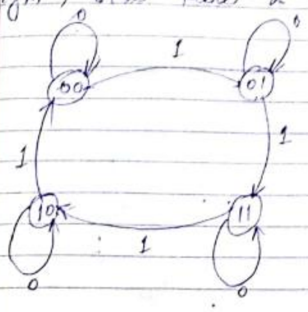


→ State dgm indicates transition from 1 state to next state

Q. In a clocked synchronous sequential ckt there are 2 D ffs A & B. When value x becomes zero, ff remains in present state & when value of x becomes 1, the following sequence comes:

↳ 00 → 01, 01 → 11, 11 → 10, 10 → 00

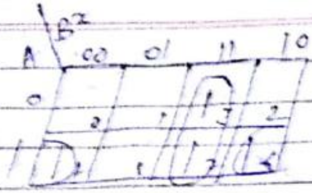
Design that synchronous seq ckt. (Draw state dgm, state table & value of ff i/ps)



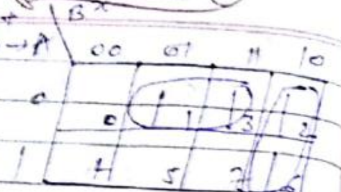
State table:

A	B	x	A^+	B^+
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	1	0

$A^+ \rightarrow$



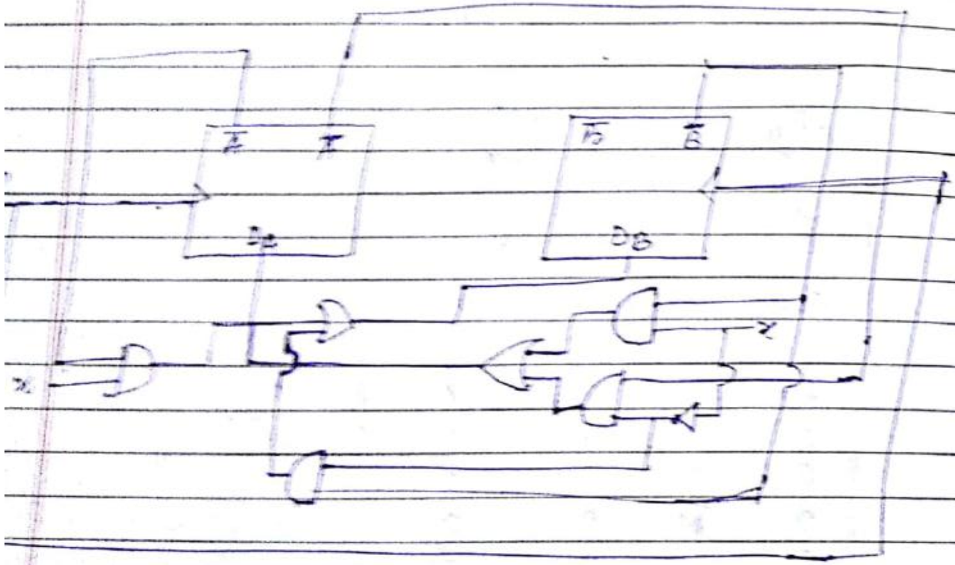
$B^+ \rightarrow$



$A^+ \rightarrow A\bar{x} + Bx$ $\quad$ $B^+ \rightarrow \bar{A}x + B\bar{x}$

$A^+ = D_A = Bx + A\bar{x}$

$B^+ = D_B = \bar{A}x + B\bar{x}$



Simulation - Compare expected result and actual result & then verify.

LAB Practicals

P.9. Design & simulate MOD 8 Asynchronous/Ripple Counter or 3-bit binary Asyn. Counter

P.10. Design & simulate MOD 6 Asynchronous Counter

P.11. Design & simulate 3-bit Johnson Counter

Software - ORCAD → project → SDI → New project

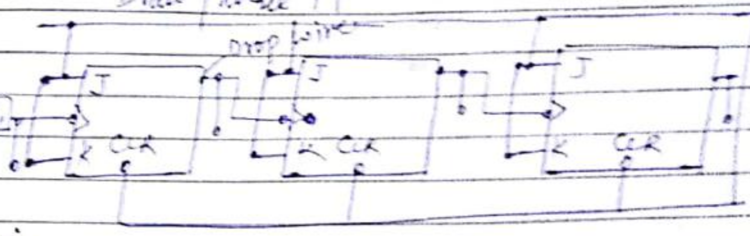
Voltage Marker ✓

Search 7473

+5V DC

Schematic - Page 1 ✓

Draw these FF -



JKFF → 7473

DFF → 7474

Select wire

Search for → +5V DC

Search for → Digclk

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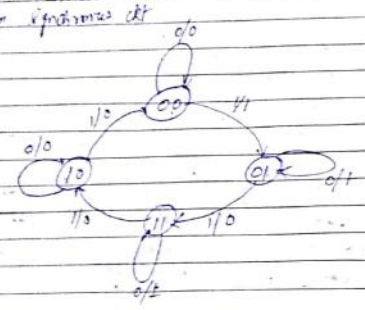
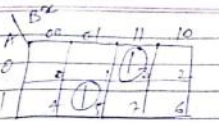
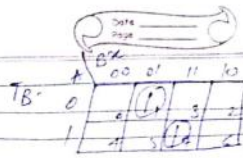
8. State dgm of sequential clocked ckt is given below:
Draw state table
design synchronous ckt



$T = Q \oplus Q^+$

PS		I/P	NS		O/P	FF	
A	B	x	A	B	Z	T_A	T_B
0	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1
0	1	0	0	1	1	0	0
0	1	1	1	1	0	1	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	1	0
1	1	0	1	1	1	0	0
1	1	1	1	0	0	0	1

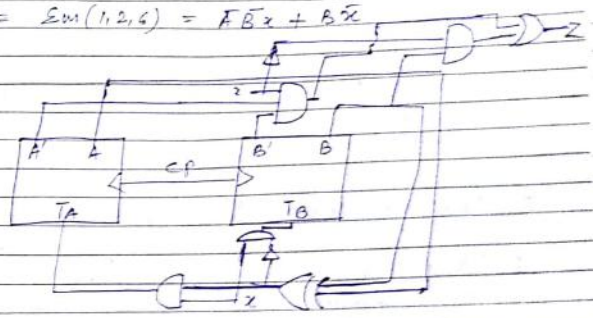




$T_A = A\bar{B}x + \bar{A}Bx$
$= x(A\bar{B} + \bar{A}B)$
$= x \cdot (A \oplus B)$

$T_B = AB'x + \bar{A}\bar{B}x$
$= x \cdot (A \odot B)$

$Z = \Sigma m(1,2,4) = \bar{A}\bar{B}x + B\bar{x}$

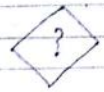


ASM Chart

ASM - Algorithmic State machine

 → start & stop

 → processing

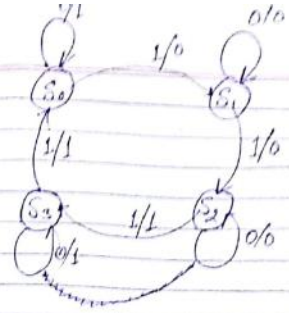
 → decision Making or conditional box

Q. Draw a ASM chart for following problems:

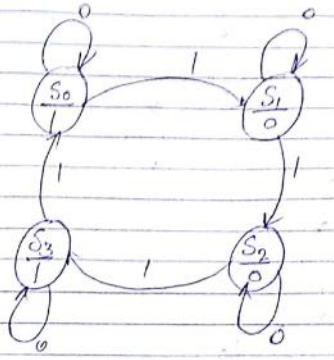
1. There is one control line X if X = 0 it remains in same state & when X = 1 it works as 2-bit up counter & when it reaches to minimum & or maximum value o/p becomes 1 o/w 0. Also draw state dgm.

or

$S_0 \rightarrow 00$
$S_1 \rightarrow 01$
$S_2 \rightarrow 10$
$S_3 \rightarrow 11$

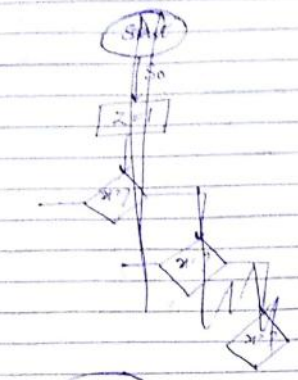


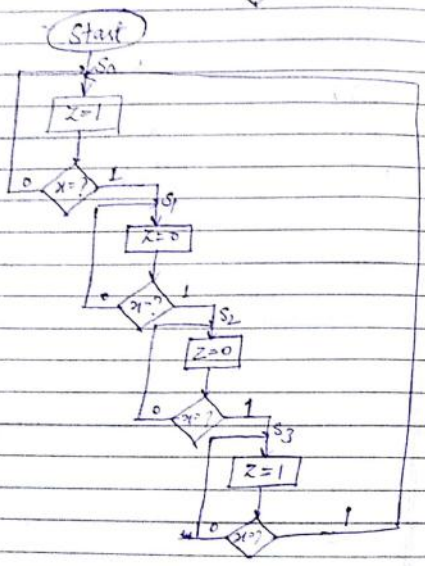
← Mealy



← Moore

ASM chart





Q. Draw the ASM chart if there is one control line c. if c=1, it works as 2 bit down counter if c=0 it works as up counter & when it reaches min/max value, o/p becomes 1 o/w 0.