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TEC–101

B. TECH. (FIRST SEMESTER)

END SEMESTER EXAMINATION, 2019

(All Branches)

BASIC ELECTRONICS ENGINEERING

Time : Three Hours

Maximum Marks : 100

Note : (i) All questions are compulsory.

(ii) Answer any *two* sub-questions among (a), (b) and (c) in each main question.

1. Attempt any *two* parts of choice from (a), (b) and (c). (2×10=20 Marks)

   (a) With the help of energy band diagram explain the mechanism of insulator, metal and semiconductor.

   (b) Explain the contact potential in a p-n junction. An abrupt silicon p-n junction has $N_a = 1 \times 10^{16}$ cm^{-3} on one side and $N_d = 1 \times 10^{17}$ cm^{-3} on other side, determine its contact potential. Given $n_i = 1.5 \times 10^{10}$ cm^{-3}.

   (c) With the help of suitable diagram explain the working principle of p-n junction diode. Draw its energy band diagram and also explain the mechanism drift and diffusion current component.

2. Attempt any *two* parts of choice from (a), (b) and (c). (2×10=20 Marks)

   (a) Draw and explain the circuit diagram of full wave rectifier. Also draw its peak load voltage waveform. What will happen when a capacitor is placed across the load resistance of a full wave rectifier circuit ? Explain with suitable waveform .

(b) Fig. 1 shows a simple Zener diode voltage regulator circuit. The voltage across the load is to be maintained constant 12 V while the load current varies from 0 to 200 mA. Find the value of V_Z and R_S. Also find the maximum power rating of Zener diode :

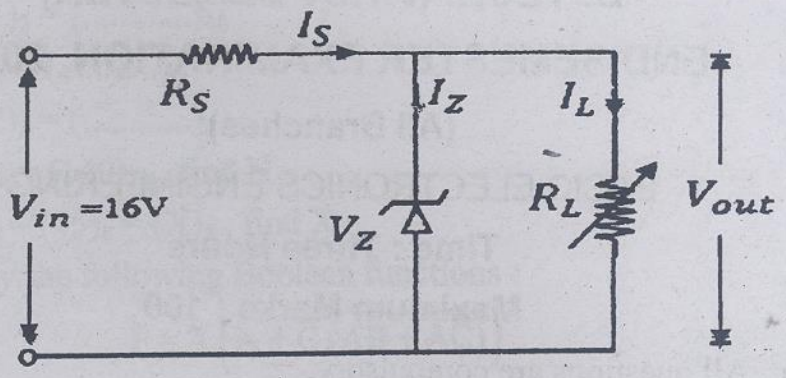

Fig. 1

(c) What do you mean by unregulated and regulated power supply ? Draw and explain the block diagram of a regulated power supply. Assume that the regulated supply produces little amount of ripple, then how it affect the performance of an audio amplifier and digital circuit.

3. Attempt any *two* parts of choice from (a), (b) and (c). (2×10=20 Marks)

(a) Explain common base configuration of BJT with suitable diagram. Also draw its input and output characteristics.

(b) A silicon BJT with $\beta = 100$, is shown in Fig. 2, compute the transistor parameters i_B, i_C, i_E and V_{CE}. In which mode the BJT is operating ?

(c) Explain all three configurations of a BJT in terms of :

(i) Input impedance

(ii) Output impedance

(iii) Voltage gain

(iv) Current gain

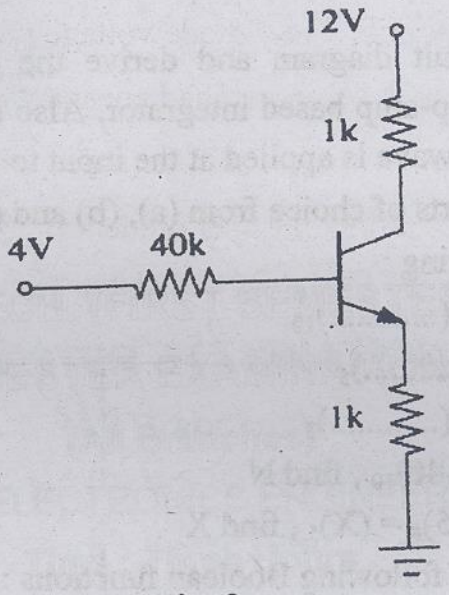

Fig. 2

4. Attempt any *two* parts of choice from (a), (b) and (c). (2×10=20 Marks)

(a) Explain the ideal characteristics of an op-amp in terms of input impedance, output impedance, differential and common mode voltage gain, common mode rejection ration, slew rate. Under what condition the open loop gain become infinite ?

(b) An op-amp based differential amplifier is shown in Fig. 3. Derive the expression for its output voltage (V_{out}) in terms of V1 and V2. Also find the value of the output voltage, assume $V_1 = 2$ V, $V_2 = 3$ V, when $R_1 = R_2 = 1\ k\Omega$, $R_3 = 5\ k\Omega$, and $R_4 = 8\ k\Omega$.

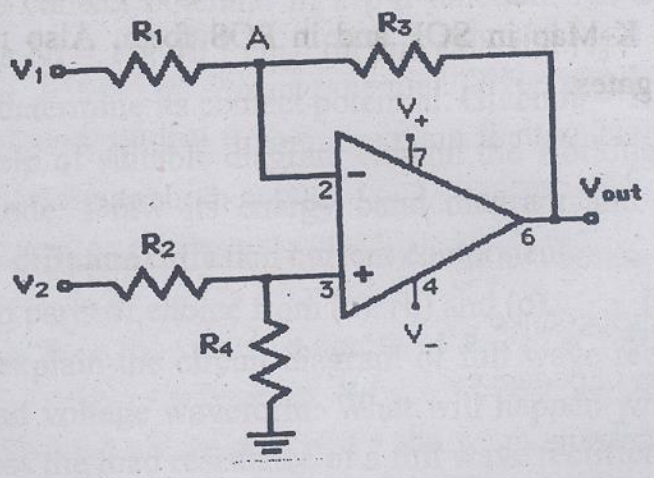

Fig. 3

(c) Draw the circuit diagram and derive the expression for the output voltage of an op-amp based integrator. Also draw the output wave form when a square wave is applied at the input to this integrator.

5. Attempt any *two* parts of choice from (a), (b) and (c). (2×10=20 Marks)

(a) Find the following :

(i) $(10.11)_2 = (\ldots\ldots\ldots)_{10}$

(ii) $(6.5)_{10} = (\ldots\ldots\ldots)_5$

(iii) $(57.32)_8 = (\ldots\ldots\ldots)_2$

(iv) $(257)_N = (140)_{10}$, find N

(v) $(103)_8 - (45)_8 = (X)_5$, find X

(b) (i) Simply the following Boolean functions :

$$F = A\left(A + \bar{C}\,\overline{(AB + A\bar{C})}\right)$$

(ii) What is the difference between canonical form and standard forms of representation of Boolean function ? Explain with suitable example.

(c) (i) Convert the following Boolean function in SOP, POS and Canonical SOP form :

$$F = (AB + C)(B + \bar{C}D)$$

(ii) Minimize the given function $F = \Sigma\,(0, 2, 3, 6, 7) + d\,(8, 10, 11, 15)$ using K-Map in SOP and in POS form. Also realize using basic logic gates.