50.002 COMPUTATIONAL STRUCTURES

INFORMATION SYSTEMS TECHNOLOGY AND DESIGN

Problem Set 6

1 Incomplete Finite State Machine

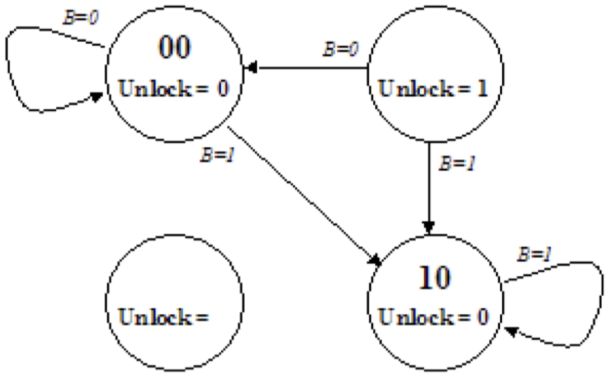
The ACME Company has recently received an order from a Mr. Wiley E. Coyote for their all-digital Perfectly Perplexing Padlock. The P3 has two buttons (”0” and ”1”) that when pressed cause the FSM controlling the lock to advance to a new state. In addition to advancing the FSM, each button press is encoded on the B signal (B=0 for button ”0”, B=1 for button ”1”). The padlock unlocks when the FSM sets the UNLOCK output signal to 1, which it does whenever the last N button presses correspond to the unique N-digit combination.

Unfortunately the design notes for the P3 are incomplete. Using the specification above and clues gleaned from the partially completed diagrams below fill in the information that is missing from the state transition diagram with its accompanying truth table. When done,

- each state in the transition diagram should be assigned a 2-bit state name S1S0 (note that in this design the state name is not derived from the combination that opens the lock),
- the arcs leaving each state should be mutually exclusive and collectively exhaustive,
- the value for UNLOCK should be specified for each state, and o the truth table should be completed.

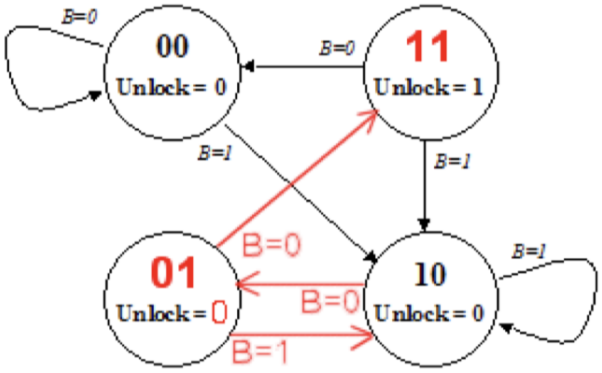
Also, What is the combination for the lock?

Solution:
The combination for the lock is 1 0 0.



S_1	S_0	B	S'_1	S'_0	UNLOCK
0	0	0	0	0	
0	0	1	1	0	
0	1	0	1	1	0
0	1	1			0
1	0	0	0	1	
1	0	1			
1	1	0			1
1	1	1			1

Figure 1



S_1	S_0	B	S'_1	S'_0	UNLOCK
0	0	0	0	0	**0**
0	0	1	1	0	**0**
0	1	0	1	1	0
0	1	1	**1**	**0**	0
1	0	0	0	1	**0**
1	0	1	**1**	**0**	**0**
1	1	0	**0**	**0**	1
1	1	1	**1**	**0**	1

Figure 2

2 Constructing FSM

Construct a ”divisible-by-3” FSM that accepts a binary number entered one bit at a time, most significant bit first, and indicates with a light if the number entered so far is divisible by 3. Answer the following questions:

1. Draw a state transition diagram for your FSM indicating the initial state and for which states the light should be turned on. Hint: the FSM has 3 states.
   Solution:
   If the value of the number entered so far is N, then after the digit b is entered, the value of the new number N’ is 2N + b. Using this fact:

   (a) if N is 0 mod 3 then for some p, N = 3p + 0. After the digit b is entered, N’ = 6p + b. So N’ is b mod 3.

(b) if N is 1 mod 3 then for some p, N = 3p + 1. After the digit b is entered, N' = 6p + 2 + b. So N' is b+2 mod 3.

(c) if N is 2 mod 3 then for some p, N = 3p + 2. After the digit b is entered, N' = 6p + 4 + b. So N' is b+1 mod 3.

This leads to the following transition diagram where the states are labeled with the value of N mod 3.

Figure 3

2. Construct a truth table for the FSM logic. Inputs include the state bits and the next bit of the number; outputs include the next state bits and the control for the light.

Solution:

S_1	S_0	b	S_1'	S_0'	light
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	1	0	0

Table 1

3. Draw a logic schematic (boolean equation) for the FSM.

Solution:

$$\text{light} = \overline{S_1} * \overline{S_0} \tag{1}$$

$$S_1' = \overline{S_1} * S_0 * b + S_1 * \overline{S_0} * b \tag{2}$$

$$S_0' = \overline{S_1} * \overline{S_0} * b + S_1 * \overline{S_0} * \overline{b} \tag{3}$$

3 Synchronizability

Which of the following cannot be made to function with perfect reliability, assuming reliable components and connections. Explain your reasoning. Some of the specifications refer to ”bounded time” which means there is a specified time interval, measured from the most recent input transition, after which the output is stable and valid.

1. A circuit that in unbounded time indicates which of two game show contestants pressed their button first.

   Solution:
   It is possible to build this unbounded-time arbiter. It may take an arbitrary period, after which it will produce (1) a decision and (2) a signal that indicates that its made a decision.

2. A circuit that in bounded time indicates which of two game show contestants pressed their button first.

   Solution:
   This is a restatement of the ”bounded time arbiter problem”, known to be unsolvable in theory. In practice we can build a circuit to solve this problem where the probability of failure is related to tPD. For ”large” tPD (eg, 10’s of nanoseconds in today’s technologies) the probability of failure can be made very small (eg, 1 failure in billions of years).

3. A circuit that determines if button A was pressed before a specified deadline. Assume the circuit has an accurate internal signal that transitions from 0 to 1 when the deadline is reached. The output should be 1 if the button was pressed on or before the deadline, 0 if pressed after the deadline. The output should be valid and stable within a specified tPD of the A input transition.

   Solution:
   This is another restatement of the ”bounded time arbiter problem”, known to be unsolvable in theory. Of course, given sufficiently long time bounds, we can engineer practical approximate solutions (see the answer to the previous question).

4. A circuit that in bounded time indicates which of two game show contestants pressed their button first if the presses were more than 0.1 second apart, otherwise the circuit lights up a ”TIE” light.

   Solution:
   This circuit will suffer metastability problems because the decision as to whether the presses were 0.1 seconds apart is subject to metastability problems.

5. A circuit that in bounded time indicates that at least one button has been pressed by some contestant.

   Solution:
   An OR gate will do the job.

6. A circuit that in bounded time indicates that exactly one of the contestants has pressed their button. You can assume there are only two contestants.

   Solution:
   An XOR gate will meet the spec.

7. A circuit that has two parts: (a) a subcircuit that indicates which of two game show contestants pressed their button first, and (b) a subcircuit that in bounded time lights a "TIE" light if the (a) subcircuit hasn't produced an answer after 1 second. The "TIE" light should stay lit even if (a) makes a decision at some later point.

   Solution:
   Both subcircuits will suffer metastability problems. (a) is asking for an arbiter (see part B above) and (b) has the same difficulties as outlined for part C above.

8. A circuit that converts button presses from two contestants into the following two-bit output encoding. The circuit has two inputs, A and B, one for each contestant. A contestant's input transitions from 0 to 1 when she presses her button.

   (a) 00 if neither contestant is pressing their button

   (b) 01 if contestant A is pressing her button

   (c) 10 if contestant B is pressing her button

   (d) 11 if both contestants are pressing their buttons

   The output should be valid and stable within a specified tPD of the most recent input transition.

   Solution:

   The low-order bit of the encoding is the signal from A, the high-order bit is the signal from B. Nothing to go metastable here.