



## **ISTD 50.002 Computation Structures**

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Original creator: Lozano-Perez, Tomas, using materials originally developed by Christopher J. Terman and Stephen A Ward. Course materials for ISTD 103, Computation Structures. MIT-SUTD Collaboration, 2012.

Modified by: Oka Kurniawan, 2013.

## Summary of $\beta$ Instruction Formats

### Operate Class:

31	26	25	21	20	16	15	11	10	0
10xxxx	Rc	Ra	Rb	unused					

OP(Ra,Rb,Rc):       $\text{Reg[Rc]} \leftarrow \text{Reg[Ra]} \text{ op } \text{Reg[Rb]}$

Opcodes: **ADD** (plus), **SUB** (minus), **MUL** (multiply), **DIV** (divided by)  
**AND** (bitwise and), **OR** (bitwise or), **XOR** (bitwise exclusive or)  
**CMPEQ** (equal), **CMPLT** (less than), **CMPLT** (less than or equal) [result = 1 if true, 0 if false]  
**SHL** (left shift), **SHR** (right shift w/o sign extension), **SRA** (right shift w/ sign extension)

Register	Symbol	Usage
R31	R31	Always zero
R30	XP	Exception pointer
R29	SP	Stack pointer
R28	LP	Linkage pointer
R27	BP	Base of frame pointer

31	26	25	21	20	16	15	0
11xxxx	Rc	Ra	literal (two's complement)				

OPC(Ra,literal,Rc):     $\text{Reg[Rc]} \leftarrow \text{Reg[Ra]} \text{ op } \text{SEXT(literal)}$

Opcodes: **ADDC** (plus), **SUBC** (minus), **MULC** (multiply), **DIVC** (divided by)  
**ANDC** (bitwise and), **ORC** (bitwise or), **XORC** (bitwise exclusive or)  
**CMPEQC** (equal), **CMPLTC** (less than), **CMPLTC** (less than or equal) [result = 1 if true, 0 if false]  
**SHLC** (left shift), **SHRC** (right shift w/o sign extension), **SRAC** (right shift w/ sign extension)

### Other:

31	26	25	21	20	16	15	0
01xxxx	Rc	Ra	literal (two's complement)				

**LD**(Ra,literal,Rc):       $\text{Reg[Rc]} \leftarrow \text{Mem}[\text{Reg[Ra]} + \text{SEXT(literal)}]$   
**ST**(Rc,literal,Ra):       $\text{Mem}[\text{Reg[Ra]} + \text{SEXT(literal)}] \leftarrow \text{Reg[Rc]}$   
**JMP**(Ra,Rc):             $\text{Reg[Rc]} \leftarrow \text{PC} + 4; \text{PC} \leftarrow \text{Reg[Ra]}$   
**BEQ/BF**(Ra,label,Rc):    $\text{Reg[Rc]} \leftarrow \text{PC} + 4; \text{if } \text{Reg[Ra]} = 0 \text{ then } \text{PC} \leftarrow \text{PC} + 4 + 4 * \text{SEXT(literal)}$   
**BNE/BT**(Ra,label,Rc):    $\text{Reg[Rc]} \leftarrow \text{PC} + 4; \text{if } \text{Reg[Ra]} \neq 0 \text{ then } \text{PC} \leftarrow \text{PC} + 4 + 4 * \text{SEXT(literal)}$   
**LDR**(label,Rc):           $\text{Reg[Rc]} \leftarrow \text{Mem}[\text{PC} + 4 + 4 * \text{SEXT(literal)}]$

### Opcode Table: (\*optional opcodes)

2:0								
5:3	000	001	010	011	100	101	110	111
000								
001								
010								
011	<b>LD</b>	<b>ST</b>		<b>JMP</b>		<b>BEQ</b>	<b>BNE</b>	<b>LDR</b>
100	<b>ADD</b>	<b>SUB</b>	<b>MUL*</b>	<b>DIV*</b>	<b>CMPEQ</b>	<b>CMPLT</b>	<b>CMPLT</b>	
101	<b>AND</b>	<b>OR</b>	<b>XOR</b>		<b>SHL</b>	<b>SHR</b>	<b>SRA</b>	
110	<b>ADDC</b>	<b>SUBC</b>	<b>MULC*</b>	<b>DIVC*</b>	<b>CMPEQC</b>	<b>CMPLTC</b>	<b>CMPLTC</b>	
111	<b>ANDC</b>	<b>ORC</b>	<b>XORC</b>		<b>SHLC</b>	<b>SHRC</b>	<b>SRAC</b>	