# 50.002 COMPUTATIONAL STRUCTURES

INFORMATION SYSTEMS TECHNOLOGY AND DESIGN

# Problem Set 3

## 1 Combinational Construction Rules

In lecture, we learned two basic principles regarding the class of combinational devices. The first allows us to build a combinational device from, e.g., electronic components. A combinational device is a circuit element that has:

1. one or more digital inputs
2. one or more digital outputs
3. a functional specification that details the value of each output for every possible combination of valid input values
4. a timing specification consisting (at minimum) of an upper bound $t_{pd}$ on the required time for the device to compute the specified output values from an arbitrary set of stable, valid input values.

while the second allows us to construct complex combinational devices from acyclic circuits containing simpler ones. A set of interconnected elements is a combinational device if:

1. each circuit element is combinational
2. every input is connected to exactly one output or to some vast supply of 0's and 1's
3. the circuit contains no directed cycles

In this problem, we ask you to think carefully about why these rules work - in particular, why an acyclic circuit of combinational devices, constructed according to the second principle, is itself a combinational device as defined by the first. You may assume for the following that every input and output is a logical 0 or 1. Consider the following 2-input acyclic circuit whose two components, A and B, are each combinational devices:

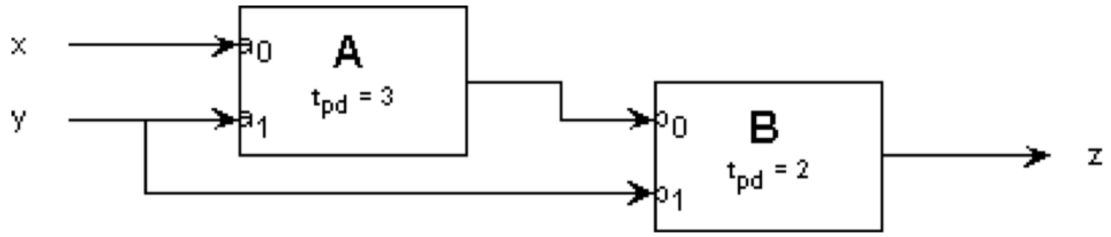


**Figure 1**

| $a_0$ | $a_1$ | $A_{a_0,a_1}$ | $b_0$ | . $b_1$ | $B_{b_0.b_1}$ |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 |

**Table 1**

The propagation delay - the upper bound on the output settling time - for each device is specified in nanoseconds. The functional specifications for each component are given as truth tables detailing output values for each combination of inputs:
Answer the following questions,

1. Give a truth table for the acyclic circuit, i.e. a table that specifies the value of z for each of the possible combinations of input values on x and y.

   **Solution:**

| x | y | z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Table 2**

2. Describe a general procedure by which a truth table can be computed for each output of an arbitrary acyclic circuit containing only combinational components. *Hint : construct a functional specification to each circuit node*.
   **Solution:**
   We can construct the truth table from left to right, i.e: solve the truth table for each component from the leftmost all the way to the rightmost one by one.

3. Specify a propagation delay (the upper bound required for each combinational device) for the circuit.

**Solution:**
The total propagation delay is $3 + 2 = 5$.

4. Describe a general procedure by which a propagation delay can be computed for an arbitrary acyclic circuit containing only combinational components. *Hint: add a timing specification to each circuit node*.

**Solution:**
One has to find the longest path from input to output to find the total propagation delay of the combinational circuit.

5. Do your general procedures for computing functional specifications and propagation delays work if the restriction to acyclic circuits is relaxed? Explain.

**Solution:**
No, the signal can propagate back in the circuit so using the longest path to calculate $t_{pd}$ is not accurate.

# 2 Combinational Circuit

Consider the following circuit that implements the 2-input function $H(A, B)$:

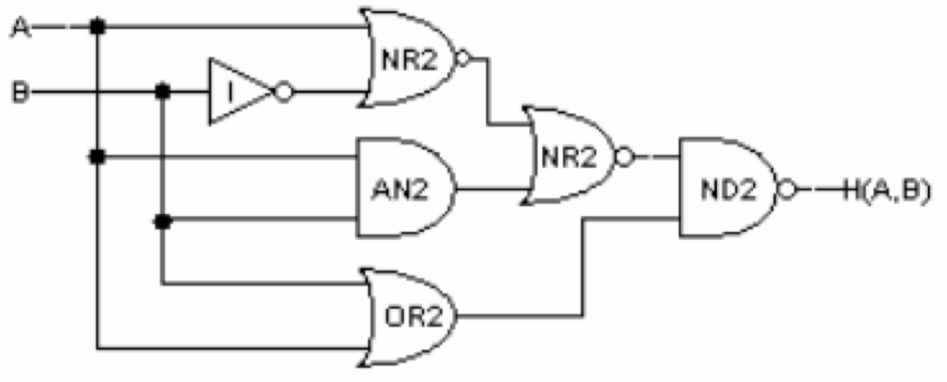


**Figure 2**

1. Give the truth table for $H$.Give a sum-of-products expression that corresponds to your truth table.

**Solution:**

| A | B | H |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**Table 3**

We begin by finding the expression of the topmost two circuits:, and applying de Morgan's law:

$$\overline{A + \overline{B}} = \overline{A}B \tag{1}$$

Then find the expression of the next pair, which is $AB$. We combine this with the above using a NOR gate and reduce the result,

$$\overline{\overline{A}B + AB} = \overline{B} \tag{2}$$

Finally, we find the expression for the bottom two pairs, which is simply $A + B$. Combine this with the above expression, we reduce and apply de Morgan's law:

$$\overline{(A + B)\overline{B}} = \overline{A\overline{B} + B\overline{B}} = \overline{A\overline{B}} = \overline{A} + B \tag{3}$$

2. Using the information below, what are the $t_{cd}$ and $t_{pd}$ of the circuit?

| gate | $t_{CD}$ | $t_{PD}$ | $t_R$ | $t_F$ |
|---|---|---|---|---|
| I | 3ps | 15ps | 8ps | 5ps |
| ND2 | 5ps | 30ps | 11ps | 7ps |
| AN2 | 12ps | 50ps | 13ps | 9ps |
| NR2 | 5ps | 30ps | 7ps | 11ps |
| OR2 | 12ps | 50ps | 9ps | 13ps |

**Figure 3**

**Solution:**
The contamination delay is the shortest path: NR2 + NR2 + ND2 = 5 + 5 + 5 = 16ps. The propagation delay is the longest path: AN2 + NR2 + ND2 = 50 + 30 + 11 = 110ps.

# 3 Gates and Boolean Equations

For the questions below, refer to the figure:

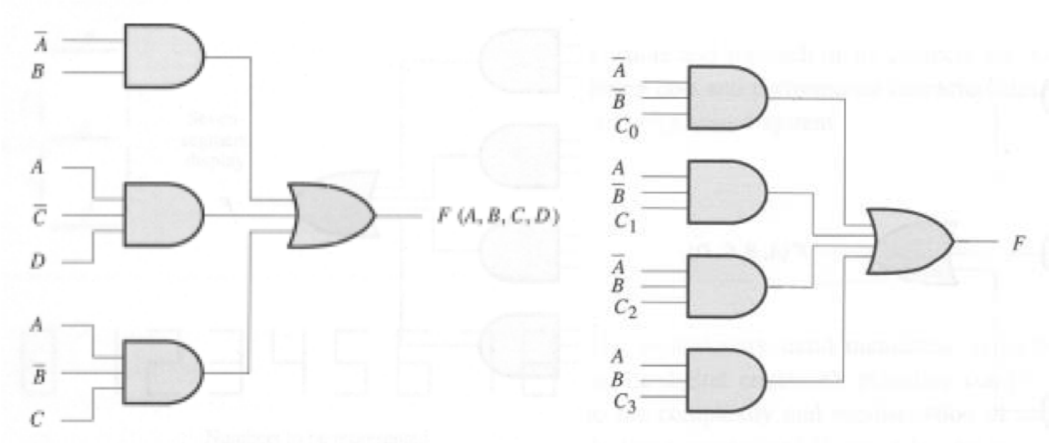


**Figure 4**

1. Show the Boolean equation for the function F described by the circuit on the left.
   **Solution:**
   $\overline{A}B + A\overline{C}D + A\overline{B}C$

2. Consider the circuit shown on the right. Each of the control inputs, $C_0$ through $C_3$, must be tied to a constant, either 0 or 1. What are the values of $C_0$ through $C_3$ that would cause F to be the *exclusive* OR (XOR) of A and B?

   **Solution:**
   The truth table for A XOR B is: $A = 0, B = 0, F = 0$, $A = 0, B = 1, F = 1$, $A = 1, B = 0, F = 1$, $A = 1, B = 1, F = 0$. In class, we know that XOR is equivalent to $A\overline{B} + \overline{A}B$. Since all the gates in the first column of the circuit on the right is an AND, setting any $C_i$ coefficient to 0 'disables' the gate, i.e: produces a zero. Hence, we can set $C_1$=1 and $C_2 = 1$ to follow the aforementioned boolean expression for XOR gate, and set $C_0$ and $C_3$ to zero to disable the rest if the AND gates.

3. Can any arbitrary Boolean function of A and B be realized through appropriate wiring of the control signals C0 through C3?
   **Solution:**
   Yes, the circuit on the right represents the sum of products, which can realise any boolean function, but it is not necessarily the smallest or the most efficient to build.

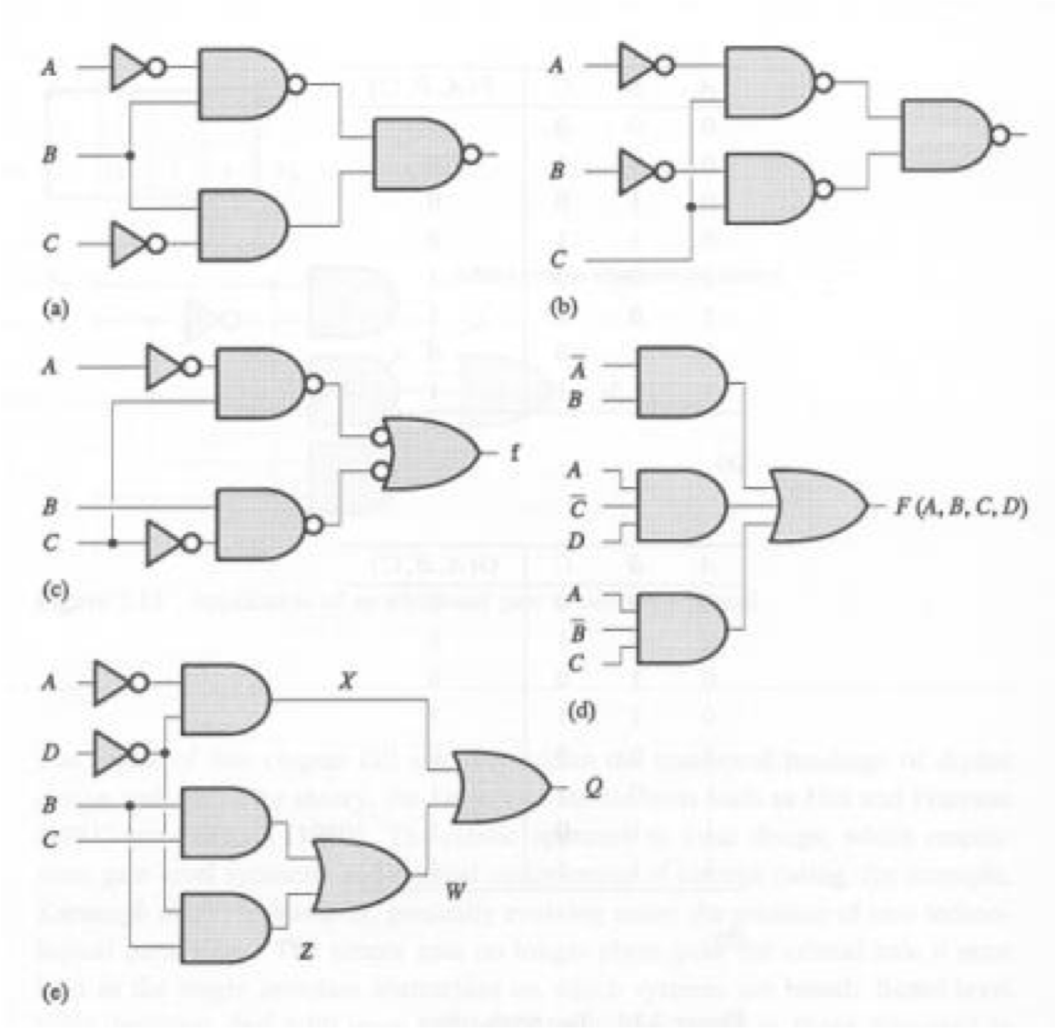


**Figure 5**

4. Give a sum-of-products expression for each of the following circuits:

   **Solution:**

   (a) $F = \overline{(A+\overline{B})\cdot\overline{C}B} = \overline{A\overline{C}B + \overline{C}B\overline{B}} = \overline{A} + \overline{B} + C$

   (b) $F = \overline{(A+\overline{C})(B+\overline{C})} = \overline{(A+\overline{C})} + \overline{(B+\overline{C})} = \overline{A}C + \overline{B}C$

   (c) $F = \overline{A+\overline{C}} + \overline{\overline{B}+C} = \overline{A}C + B\overline{C}$

   (d) $F = \overline{A}B + A\overline{C}D + A\overline{B}C$

   (e) $F = \overline{A}\ \overline{D} + BC + B\overline{D}$

5. Give a canonical sum-of-products expression for the Boolean function described by each truth table below:

| $A$ | $B$ | $C$ | $F(A,B,C)$ |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

| $A$ | $B$ | $C$ | $G(A,B,C)$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

**Figure 6**

**Solution:**
The canonical sum-of-products expression only take into account the rows where F is 1. So for the table on the left,

$$\overline{A}\ \overline{B}\ \overline{C} + A\overline{B}\ \overline{C} + A\overline{B}C + ABC \tag{4}$$

For the table on the right,

$$\overline{A}BC + A\overline{B}C + AB\overline{C} + ABC \tag{5}$$

6. We've seen that there are a total of sixteen 2-input Boolean functions: AND, OR, XOR, NOR, etc. How many 5-input Boolean functions are there?

**Solution:**
There will be $2^{2^5}$ 5-input boolean functions.