# 50.002 COMPUTATIONAL STRUCTURES

INFORMATION SYSTEMS TECHNOLOGY AND DESIGN

# TL;DR : The CMOS Technology

## 1 The Ideal Combinational Device

We would want our device to be:

1. Can tolerate some amount of errors, using Noise Margins : VTC gain > 1 and nonlinear gain
2. If we have **lots of gain**, that means we have **more noise margin**
3. Cheap, small
4. We want **zero power dissipation** when voltages aren't changing
5. Otherwise when voltage is changing fro, '0' to '1' or '1' to '0' then power has to dissipate
6. Our device has to be functional, meaning that it conforms to the **truth table** at all times

## 2 The MOSFET

Metal-oxide semiconductor field effect transistors (MOSFET, or shortened as FETs): to implement the functionality of our combinational device (see figure below).
Things to note about FETs:

1. Used to 'switch' 1s to 0s and vice versa, so that we can implement functionalities (truth table or logics)
2. The current flow between source and drain $I_{DS}$ is proportional to $W/L$ (the width and the length) of the FET.
3. Source and drain is physically symmetrical, we name them depending on which side has the **higher** potential.

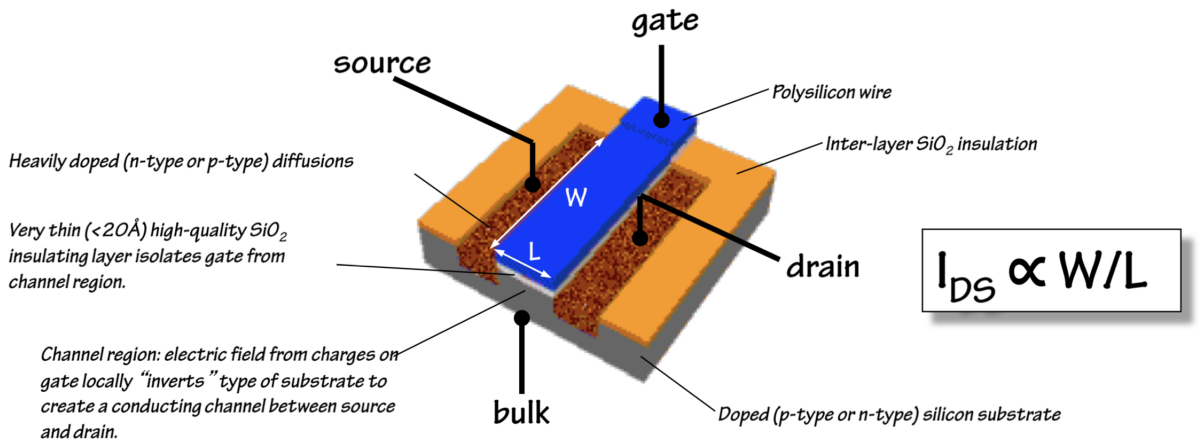


**Figure 1**

4. The side with the **higher potential is drain**, the one with the **lower potential is source**.
5. Current flows from higher potential (+) to lower potential (-)
6. Electron flows from lower potential (-) to higher potential (+)

# 3 Types of MOSFETs

There are two types of FETs: the **p-type** and the **n-type**:

1. The p-type : majority care holes (impurities), bulk is connected to VDD
2. The n-type : majority are electrons, bulk is connected to GND

Some terms you need to know:

1. VDD : voltage source
2. GND : ground
3. Reverse-biased: a state whereby D is insulated from S, where current cannot flow from D to S **in the presence of applied voltage**.

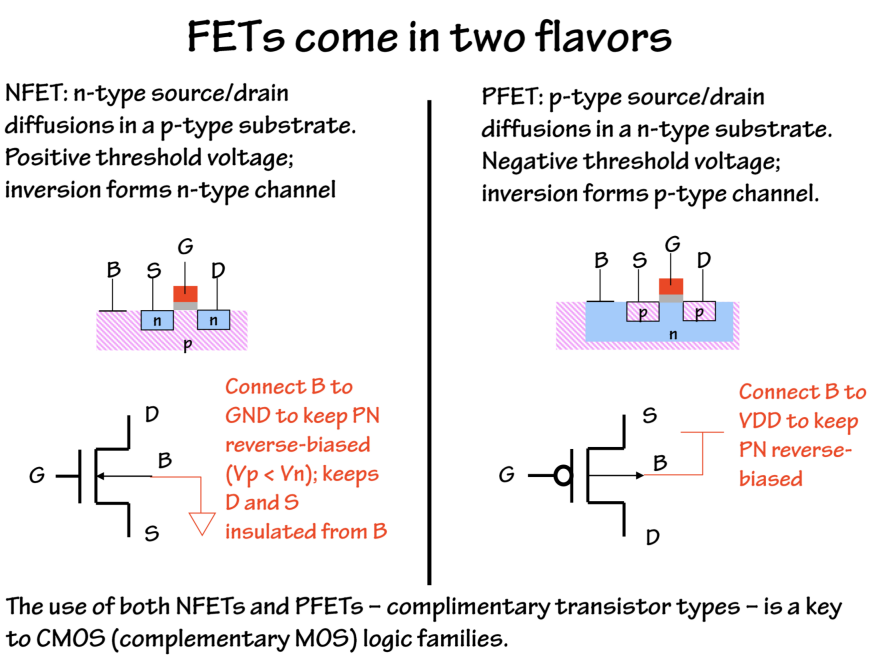


**Figure 2**

4. A FET that is ”ON” means that there’s connection between D and S, current can flow through them.
5. A FET that is ”OFF” means that there’s no connection between D and S, current cannot flow through them.

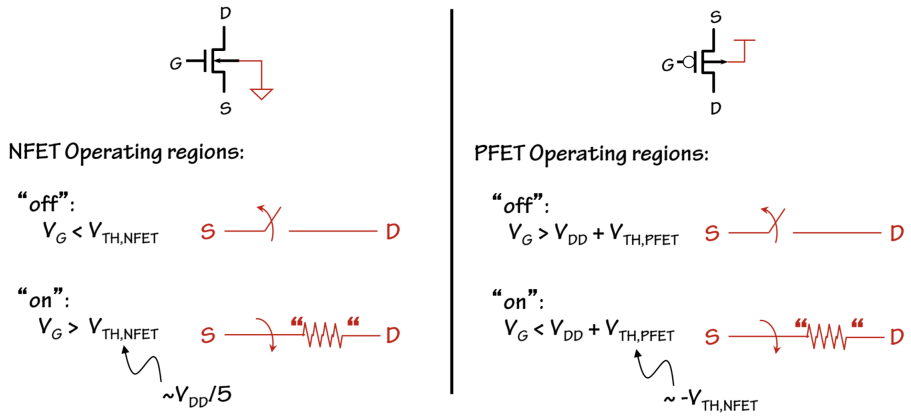


**Figure 3**

How n-type operates:

1. Indicated y the FET with **no** bubble ○
2. It is ”OFF” when $V_{gs}$ is **low**
3. It is ”ON” when $V_{gs}$ is **high**

4. Bulk is connected to GND
5. When it is ”ON” then current can pass from D to S through Bulk, but remember that there’s GND connected to the bulk
6. Hence, the output of an ”ON” n-type is ’0’

How p-type operates:

1. Indicated by the FET with the bubble ∘
2. It is ”OFF” when $V_{gs}$ is **high**
3. It is ”ON” when $V_{gs}$ is **low**
4. Bulk is connected to VDD
5. When it is ”ON” then current can pass from S to D through Bulk, but remember that there’s VDD connected to the bulk
6. Hence, the output of an ”ON” n-type is ’1’

# 4 Naming of Source and Drain

The naming of the Source terminal depends on the majority of the charge carrier. In p-FETS, current flows from Source to Drain, because the majority of the charge carrier is holes (positively charged). In n-FETS, current flows from Drain to Source, because the majority of the charge carrier is electrons (negatively charged).

**Note: Current (I) cannot flow out back to the Gate becaxwuse there’s a capacitor there (infinite resistance). The function of the gate capacitor is to create electric field enough to pull either electrons up to the gate in n-FETs or holes up to gate in p-FETs to create a conductive n-type (electrons) or p-type(holes) channel**.

# 5 The Pull-up and Pull-down Circuit in CMOS

These p-FETs and n-FETS can be connected together to form a CMOS : Complementary Metal-Oxide Semiconductor. There are two parts of CMOS: **the pull-up circuit** and **the pull-down circuit**, see figure below:
Contents of the pull-up circuit:

1. All FETs in the pull-up circuit is p-type
2. So all is connected to the VDD
3. It is called ’pull-up’ because when any of them is ”ON” then the output of the overall CMOS circuit is 1

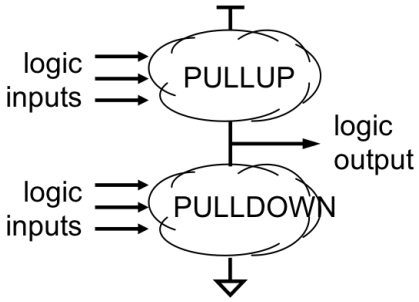


**Figure 4**

Contents of the pull-down circuit:

1. All FETs in the pull-down circuit is n-type
2. So all is connected to the GND
3. It is called 'pull-down' because when any of them is "ON" then the output of the overall CMOS circuit is 0

# 6 The CMOS Complements

Imagine if pull-up and pull-down is bot "ON". This means that VDD has a straight open connection to GND : resulting in short-circuit. Hence, **it is very important for a CMOS circuit to contain complementary pull-ups and pull-downs**.
The CMOS complements is summarized as below:
An example below explains the CMOS complement more clearly. Explanation: (make sure you know how these works)

1. From the diagram, A is connected to the p-FET on the **left** and the n-FET on the **top**
2. B is connected to the p-FET on the **right** and the n-FET on the **bottom**

Case 1:

1. Lets see what happens when A = 1 and B = 1.
2. When A = 1, the p-FET on the **left** is "OFF", the n-FET on the **top** is "ON"
3. When B = 1, the p-FET on the **right** is "OFF" and the n-FET on the **bottom** is "ON"
4. Current from VDD **cannot** flow to the output through any of the left and the right p-FET
5. Current at the output **is drained down to the GND** through either n-FET on the top or n-FET on the bottom.

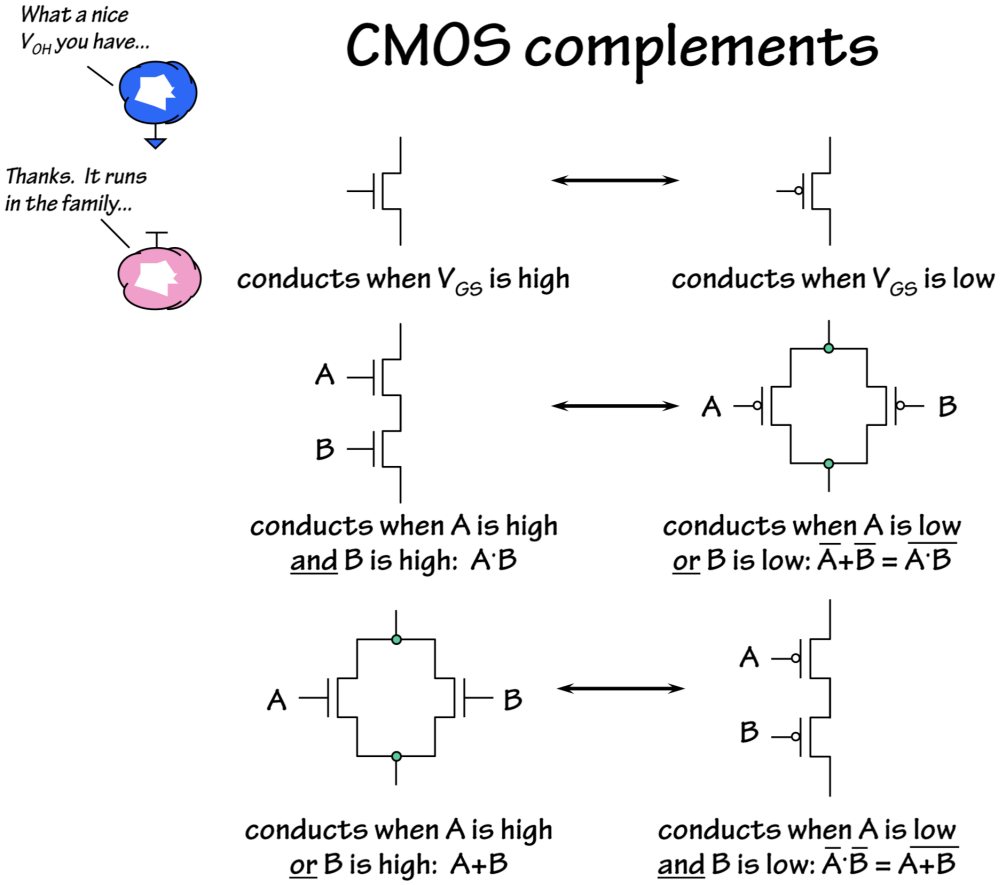


**Figure 5**

6. Hence the output is 0 when A = 1 and B = 1

Case 2:

1. Another case, when A = 0, and B = 1,
2. When A = 0, the p-FET on the **left** is ”ON”, the n-FET on the **top** is ”OFF”
3. When B = 1, the p-FET on the **right** is ”OFF” and the n-FET on the bottom is ”ON”. This draws current from B = 1 and pull it down to 0.
4. Current from VDD can still flow from the p-FET on the **left** to the output
5. Hence the output is 1 when A = 0 and B = 1

Notice how there’s parallel p-FET in the pull-up, and series n-FET in the pull-down: **they are the CMOS complement**.

# 7 The Propagation Delay $t_{pd}$

$t_{pd}$ is the time delay from **valid** input to **valid** output. The effective $t_{pd}$ of an entire circuit is the **maximum** cumulative propagation delay over all paths from inputs to

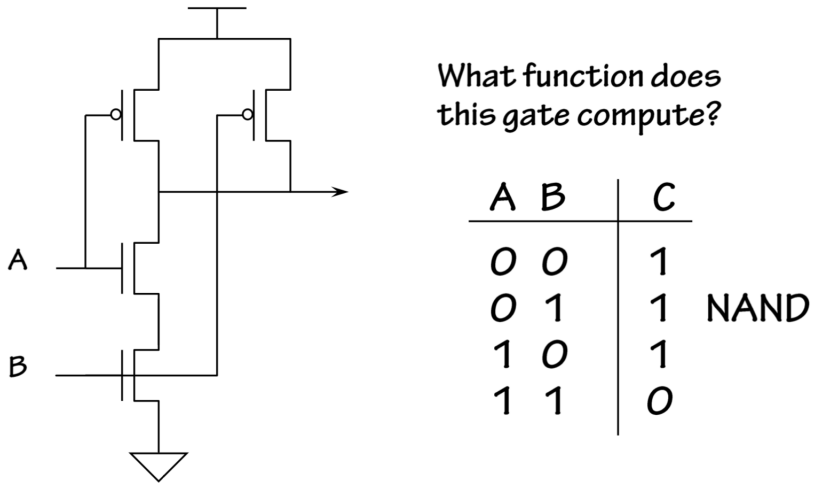


**Figure 6**

outputs. This works only in **acyclic circuits**.

# 8 The Contamination delay $t_{cd}$

$t_{cd}$ is the time delay from **invalid** input to **invalid** output. The effective $t_{cd}$ of an entire circuit is the **minimum** cumulative contamination delay over all paths from inputs to outputs. This works only in **acyclic circuits**.

# 9 Timing Example

Complementary pull-up (made up of p-FETs) and pull-down circuits (made up of n-FETs) form a CMOS gate. $t_{pd}$ and $t_{cd}$ are specified per gates. Consider the example below on how to calculate these timings,

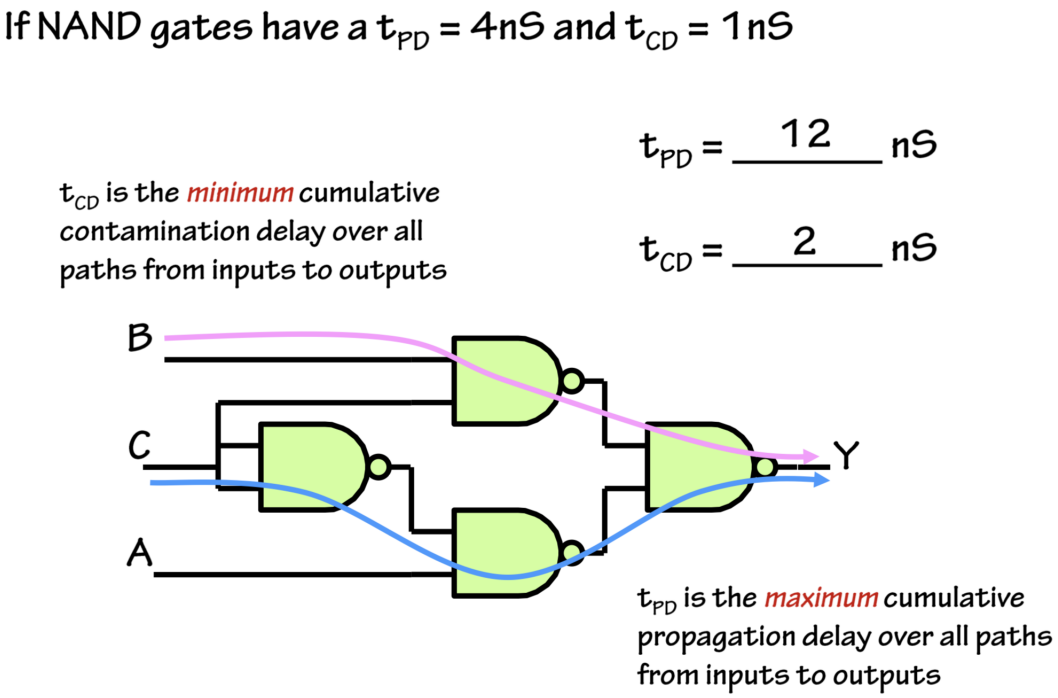
If NAND gates have a $t_{PD}$ = 4nS and $t_{CD}$ = 1nS
$t_{PD}$ = 12 nS
$t_{CD}$ = 2 nS
$t_{CD}$ is the minimum cumulative contamination delay over all paths from inputs to outputs
B
C
A
Y
$t_{PD}$ is the maximum cumulative propagation delay over all paths from inputs to outputs

**Figure 7**