Release Notes

Introduction

This document summarizes release 20 of the ALP-4.3 application programming interface (API). The following remarks are to indicate additional programming capabilities.

These release notes apply to ALP-4.3 components of the following versions:

- API (alp4395.dll): 1.0.y.x, y≥20, x≥36
- API header file (alp.h): 20
- ALP API description (ALP-4 API description.pdf): 2017-11-30 (see last page of that document)

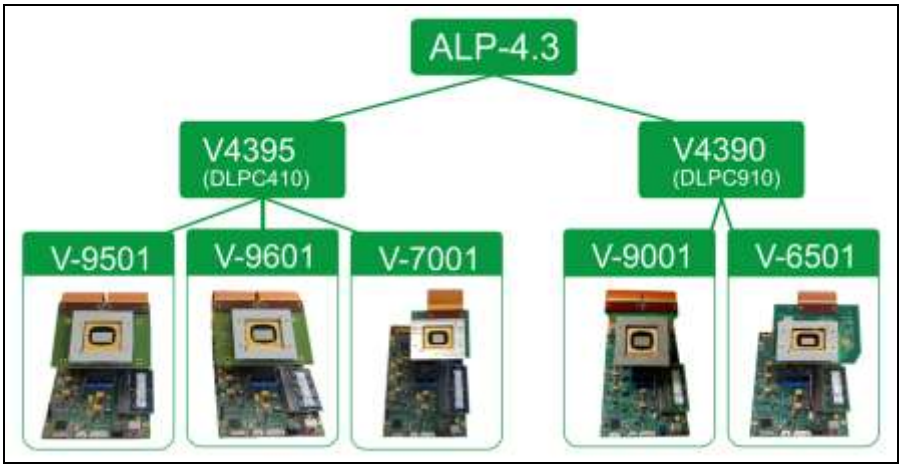
ALP APIs are compatible to each other regarding their software interface. However, they are specialized to support individual hardware versions. The ALP hardware/software table summarizes the combinations for the three versions of DLL:

- **ALP-4.1** (alpD41.dll)
- **ALP-4.2** (alpV42.dll)
- **ALP-4.3** (alp4395.dll)

ALP hardware/software table:

DLP DMD Chip	DLP Controller FPGA	DLP Controller Board	Supporting ALP-4 Software	ViALUX Product
DLP7000 DLP9500	DLPC410	ViALUX VX4100 or TI DCB4100	ALP-4.1 (as an option)	Discovery™4100 Development Kit
DLP7000		ViALUX V4100	ALP-4.2	V-7000
DLP7000		ViALUX V4395	ALP-4.3	V-7001
DLP9500				V-9501
DLP9600*				V-9601
DLP6500	DLPC910	ViALUX V4390		V-6501
DLP9000X				V-9001

* DLP9600 is an abbreviation for DLP 0.96” WUXGA 2x LVDS DMD, this DMD is available in the V-9601 SuperSpeed V-Module only, it is not sold as a chipset.



ALP-4 software supporting end-of-life products

DLP DMD Chip	DLP Controller FPGA	DLP Controller Board	Supporting ALP-4 Software	ViALUX Product
DLP9500	DLPC410	ViALUX VX4100	ALP-4.1	V-9500 (end-of-life)
DLP9600*				V-9600 (end-of-life)

Summary of Modifications

Support for V-6501

Beginning with version 1.0.20.x of alp4395.dll, ViALUX offers a new SuperSpeed V-Module. The V-6501 has a DLP6500 1080p DMD, controlled by a V4390 controller board.

See also ALP API-4.3 description: ALP_DMDTYPE_1080P_065A, ALP_DMDTYPE_1080P_065_S600, ALP_DMDTYPE_DLPC910REV, *AlpSeqTiming*.

DMD Mask

Image data processing now involves a mask. This is a filter that hides image data at static areas of the DMD.

See also ALP-4.3 API description: ALP_DMD_MASK_SELECT and ALP_DMD_MASK_WRITE

Bit Depth of Grayscale Display

Applications that require large bit depths had to assemble images as a sequence of 8-bit frames. V-Modules can now display increased bit depths up to 12 bit natively.

See also ALP-4.3 API description: *AlpSeqAlloc*, ALP_BITPLANES, ALP_BITNUM

Bit Depth in Flexible PWM Mode

Flexible PWM mode has been extended even further, now allowing up to 32 bit planes.

See also ALP-4.3 API description: Flexible PWM Mode

Input/Output Pins

General Purpose IO pins are switched to a specified state after AlpDevFree.

See also ALP-4.3 API description: section Pin assignment and default states

Support for Windows 10

Microsoft has implemented a policy that can cause drivers to fail loading on certain versions of Windows 10. At the time of writing, ALP drivers support Windows 10 (Microsoft Windows Version 1703 Build 15063.674) without any issues and without any operating system setting modifications required.

Other Improvements and Bug-fixes

Irregular terminating scenarios (e.g. “TerminateProcess” or kill application in Windows task manager) could cause inconsistent internal state. A bug has been fixed and the device restores clean state for subsequent initialization (*AlpDevAlloc*).

Concurrent image data transfer (*AlpSeqPut*) during sequence display (*AlpProjStart[Cont]*) is available without restrictions.