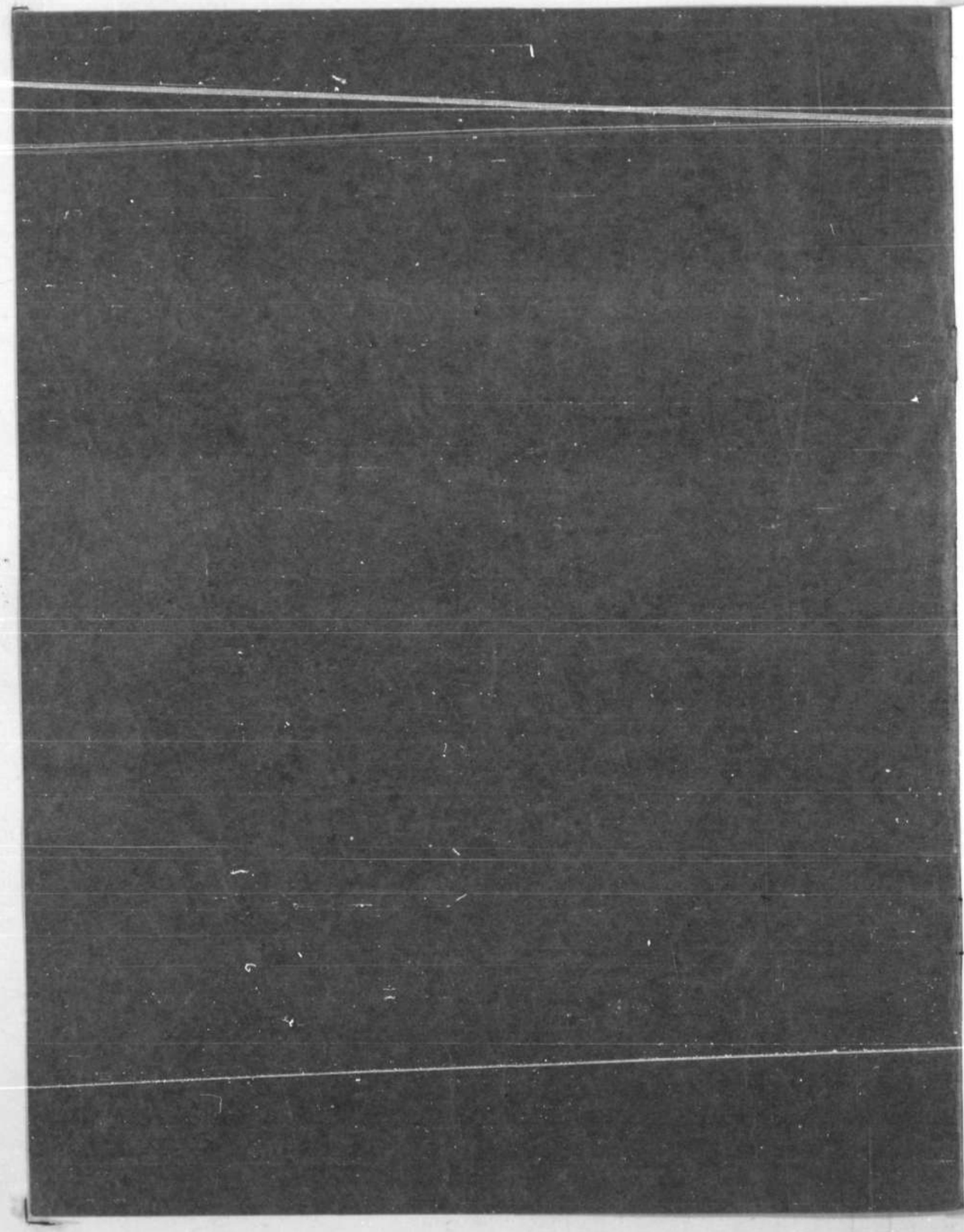

PROJECT WHIRLWIND
(Device 24-x-3)

SUMMARY REPORT NO. 20
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Cambridge 39, Massachusetts
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2. SYSTEM ENGINEERING

2.1 INSTALLATION AND TESTING OF WWI

2.11 Equipment & Wiring Installed

As described in Summary Report 19, power wiring was complete and equipment was installed by July 1 for all of the computer except electrostatic storage and input-output equipment. The past 3 months have witnessed substantial progress in the installation of electrostatic storage; and the special display equipment, an element of the computer output, has been installed and put into operation (see Section 2.22).

All electrostatic-storage control and deflection panels have been installed in their final locations, and power wiring for these panels is complete as far as the racks are concerned. Final connection to the power distribution system must await completion of additional distribution panels and racks, which will be finished during October. This control and deflection equipment, filling 6 racks, is now being tested with power supplied from a temporary circuit-breaker panel, and no marginal checking is available for it at present.

Electrostatic-storage proper and its special power supplies remain to be installed, a total of 19 racks of equipment. No input-output equipment except special display has been installed.

The transmission line used for distributing deflection voltages to the storage tubes was installed in the 16 electrostatic-storage digit racks, as were power distribution strips, filament transformers, and other miscelianeous rack hardware.

During this 3-month period approximately 50 new WWI panels were completed, and 10 existing spare panels were modified for use in electrostatic-storage control and input-output control. In addition, power cables for most of these panels and nearly all video cables for them were completed.

2.12 Revision of Test Control

The Whirlwind test control has evolved into very nearly its final form. Test control at the present time contains the necessary controls for starting and stopping the computer and introducing initial conditions, as well as trouble-location aids. Ultimately these controls will be located at the operator's console, which is not yet built. However, the main purpose of test control, both in its final form and at present, is to provide at one central point all the information and control needed for trouble location and testing.

The original arrangement of test control was described in Summary Reports 13 and 15 and Report R-161. Test control provided a substitute for the central control of the computer; it consisted of an array of Whirlwind test equipment. This permitted complete testing of the arithmetic element and other flip-flop registers independent of central control. Thus it was possible to have a reliable arithmetic element when the Whirlwind system with test storage was tied together for the first time in early August. At that point both the arithmetic element and central control were reasonably dependable units. As a result there was little lost motion when the two were tied together, and the system was soon operating on simple programs using test storage.

About August 15 it became evident that the substitute central control would no longer be needed even as stand-by equipment. It was then removed from test control. At the same time other parts of test control were rearranged to provide greater flexibility. Facilities for introducing a variable delay element in series with synchroscope sweep triggers were provided. This allows viewing of pulses on a fast sweep of a synchroscope at any portion of a long computer program.

Also test control was arranged to use 6 digits of the program counter (only 5 program-counter digits are needed with test storage, leaving 6 normally unused digits) for periodic (cyclic) operation. The advantages of periodic testing were pointed out in Section 2.233 of Summary Report 19. The extension of this type of testing for Whirlwind operating with central control requires that a wait period be applied just after any arbitrary time pulse or step of an arithmetic operation within any order of a long program. This is accomplished, as stated in E-252, by use of 6 program-counter digits. To apply a wait period after time pulse m of order n: Time pulse m (from a push-button selector) is applied to the first of the 6 program-counter digits and the counter reset to 64 - n. The overflow of the counter is then used to halt operation. The computer is then cleared and the initial values reintroduced, and the program is restarted after a wait period determined by a master frequency divider.

In summary, the main parts of test control are:

1. Neon indicator lights for all flip-flops.
2. Push-button controls for starting and stopping computation.
3. Controls for setting flip-flop storage and certain other registers.
4. Automatic and manual voltage-variation controls.
5. Power switches and remote fuse indicators.
6. Circuits for the synchronization and delay of synchroscope sweeps.
7. Controls and associated equipment for periodic operation.
8. Error alarm indicators for built-in checking facilities.

2.13 Test Results

2.131 Marginal Checking

In their present state, marginal checking facilities consist only of manual selection and manual variation, the automatic functions not having been connected. However, the present marginal checking installation has proved extremely valuable in two functions: the testing of flip-flop balance and the improvement of circuit design.

The balance of all flip-flops is being periodically checked by means of screen-voltage variation. This has resulted in the replacement of several flip-flop tubes and crystal rectifiers before they became bad enough to cause steady errors.

Another important use of marginal checking in system tests has been the variation of certain voltages affecting signal amplitude in a given channel for the purpose of picking up weak links in the channel. For example, the +90-volt gate-tube screen voltage in the pulse generator and frequency divider was found in early system tests to have an operating range of 70 to 98 volts. The indicated design change now permits a variation from 60 to 120 volts without operation failure.

The automatic selection and variation equipment, now nearing completion, is expected to be even more valuable.

2.132 D-C Coupling of Control Matrix Outputs

Operation of the control matrix is now satisfactory. In its initial tests the output of gate circuits was found to vary considerably depending upon which line was selected (i.e., which order was being decoded). This variation, caused by vacuum-tube differences, was accentuated by the coupling between the gate tubes and the last amplifier stage. A change in the coupling circuits from a-c coupling to d-c coupling has greatly stabilized the gate-tube outputs. In addition, degeneration in the form of unbypassed screen-grid dropping resistors in matrix drivers has further stabilized gate-tube outputs.

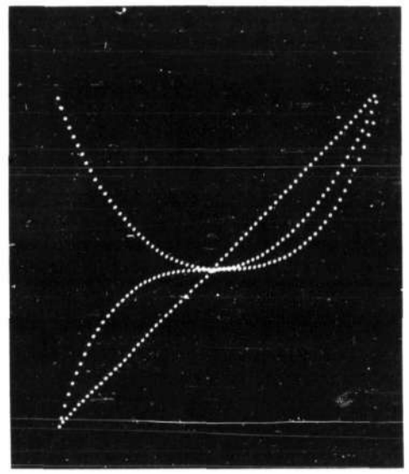
2.133 Test Storage Difficulties

The test storage output has given difficulties similar to those of the control matrix. The output of the storage registers has been found to vary according to the contents of the register. Also the output amplitude has been critically dependent upon the condition of the 2C51 driver stages.

The changes made in the control matrix were not directly applicable here. The test storage originally had not nearly so great a design margin as the control matrix, because its space allotment as a test item was not so great. Thus the power available does not permit the same stabilization as used in the control matrix. Several changes such as the addition of peaking inductors have been made. However, the problem has not yet been solved, and is still under study.

2.2 WHIRLWIND I OPERATION WITH CENTRAL CONTROL AND TEST STORAGE

After nearly two years of research, design, construction, and tests, the computing section of WWI has just passed a most significant milestone: solving an equation and displaying its solution. The accompanying photograph shows an oscilloscope display in which a family of curves, representing the powers of x, is plotted as a series of discrete points calculated by the machine.



Oscilloscope display of the solution of x, x^2, and x^3 for varying values of x.

Lest the simplicity of the problem belie its importance, the reader should be reminded that previous test problems given to the computer required merely single-point solutions, and that a progressive display, no matter how simple, can result only when all the basic parts of the computer act in harmony. Until recently, when all components of central control and test storage were

The sa 31 operation stores any overflow digit from the addition of the smaller halves, and the ca 20 operation automatically adds in the carry, if any. Double-length multiplication requires from 19 to 35 orders, depending on the accuracy of round-off desired; double-length division, about 80 orders. These figures compare with 3 orders for ordinary single-length multiplication or division.

6.13 Subprogramming

The programs for a problem using double- or higher-precision and/or floating-point numbers (henceforth called multiple-register programs) will unavoidably require 2 to 10 times as much computing time as the ordinary programs for the same problem simply because there is more computing to be done; but multiple-register programming need not require either much extra program storage capacity or more work on the part of the coder than ordinary programming. For by the use of subprograms to carry out the multiple-register arithmetic, and by the use of one of several special techniques for entering such subprograms, the program can be written in much the same fashion as usual. Briefly, the several subprogramming techniques can be described in order of increasing complexity of the subprogram or in order of decreasing complexity of the translation from a single-register to a multiple-register program.

1. Three-address subprograms in which the addresses of 2 operands and the address in which the result is to be stored are supplied to a chosen subprogram which performs the arithmetic. Fssentially this is the technique for which the automatic subprogram operations were intended, as described in M-328. Since the elimination of these as, ax, ay, az operations, the 3-address subprograms require the use of 4 orders in the main program, 3 to give the 3 addresses and one to choose the particular subprogram.
2. Single-address subprograms in which each order, with the possible exception of red-tape orders, is replaced by a pair of orders, one indicating the operation, the other the address. This is the 2-register method described in Summary Report 10, page 18, and in M-659.
3. Re-coding programs in which a regular single-register program written according to a few special rules is examined order by order by a master re-code program and each order is replaced by its multiple-register equivalent.

The first two procedures have been worked out in some detail as described in the references given. The third procedure has not yet been thoroughly investigated. The first technique demands that the program be written with multiple-register performance in mind. The second technique provides a fairly straightforward method for translating manually a single-register program into a multiple-register program. The third technique will enable an ordinary single-register program to be inserted without modification into the computer, with the computation being carried out in multiple-register form. Each of the three techniques costs more in terms of computing time than the preceding one; the use of subprograms at all costs more in computing time than not using subprograms; and the multiple-register programs cost more than the single-register programs regardless of the technique used. For almost any problem requiring great precision, however, the computing time will not be the critical factor.

All of these techniques will be described in detail in a forthcoming report, together with other techniques and with descriptions of subprograms for such operations as square-rooting, trigonometric function evaluation, interpolation, etc., as well as for floating-point and double-precision operations. It is expected that this report will appear at the end of the next quarter under the title, "Subprogramming for Whirlwind I".

6.2 CODING OF TEST PROBLEMS

The successful performance of several different test programs by the Whirlwind computer is reported in Section 2.2 of this report. The need for such programs has of course long been realized, and the programs were for the most part written before the installation of test storage and other essential components of the Whirlwind I system. The principles used in coding several different problems, all of which have been successfully performed by the computer, are described below. A number of other programs have been written and tried; the programs treated below have been selected as being especially interesting and representative.

6.21 The Switch Check Program

The "switch check" program is only in a loose sense a program at all. Basically, switch check is a procedure which may be used under Whirlwind I control or under test control to perform a continuous check on the storage switch, on digits 11 to 15 of the program counter, and on some of digits 11 to 15 of toggle-switch storage. In operation, switch check proceeds by taking the content of toggle-switch register No. 0 and sending it to the storage switch (using the program register in its normal role as intermediate storage). The content of register No. 0 is at the same time compared with the content of the program counter, and an alarm is given if the two numbers differ. The toggle switches are set so that register No. M contains the quantity M + 1; i.e., so that register No. 0 contains 1, No. 1 contains 2, etc., and No. 31 contains 0. Thus, initially, the content of register No. 0, namely 1, is sent to the program register, thence to the storage switch (selecting register No. 1 for the next cycle), and thence to the check register. Meanwhile, the program counter has been indexed by 1, so that it now contains a 1, and its content has also been sent to the check register. A transfer check pulse then performs an identity check on the two numbers. The storage switch now selects storage register No. 1, which contains 2, and when the program counter is again indexed it also contains 2, thus again yielding a correct identity check. The process continues until all 32 positions of the storage switch are used, and the cycle automatically repeats indefinitely with a repetition rate of about 3125 times per second. The procedure is described in more detail in M-863.

6.22 Test Program No. I

One of the early test procedures for checking the operation of the many flip-flops in the computer was a cyclic complementing of all flip-flops by means of single pulses injected on the restorer line at an audio-frequency rate. The visual result of the procedure was that all the indicator lights, both red (1 side) and white (0 side), lit with equal intensity. If any flip-flop was sticking, only one of its pair of indicator lights would be on, and this fault would be immediately apparent to even a casual observer. This procedure seemed to be so fruitful that a program was written to mimic, as nearly as possible, this computer complementing cycle.

Test Program No. I uses some arithmetic gyrations to put 1's into all digits of the arithmetic element registers (AR, AC, AC carry, and BR) and to make sure that the 1's actually stay in those registers. Then 1's are stored in all digits of all flip-flop storage registers, and after 0.70 second, during which the computer is occupied with counting to 32768 by 1's in the accumulator, the content of each of the flip-flop registers is checked against all 1's stored in a toggle-switch register. The read-in, wait, and check process is then repeated with all 0's substituted for all 1's. The complete cycle is repeated indefinitely, each cycle lasting about 1.4 seconds. The cycles can be shortened to about 500 microseconds by not requiring the computer to count to 32768 by 1's.

The technique of delaying the computer between parts of a program by causing it to count a large number of small increments has been used frequently since this first application. Such a delaying procedure can be used to slow the computer down so that different sets of results may be observed visually.

There is an obvious advantage to the computer complement program over the straight audio-frequency complement pulse scheme: no visual check is necessary, and any error, even a single transient error, will be detected. Test Program No. I is described in detail in E-295.

6.23 Test Program No. II

The completion of the central control element was heralded by the performance of Test Program No. II, which provides a strenuous test of the 24 operations so far adopted for Whirlwind I with the exception of the 6 input-output operations (see Summary Report 19, pp. 24-25). Since repeated use must be made of the check operation qc (a temporary operation which checks the content of AC against the content of the indicated storage register; see E-250), the program must make frequent use of the numerical properties of the orders. That is, since there is not sufficient test storage available to permit storing a 28-order program and numerous constants, many of the orders are made to serve a second function as numbers. The program is a good example of this special technique intended to make the most of cramped storage. The program is given, together with an explanation, in E-296.

6.24 Binary-to-Decimal Conversion and Reconversion

Since it is intended that by means of a special subroutine the Whirlwind I computer will itself convert orders, data, and results from binary-coded decimal to binary and from binary to binary-coded decimal form, one of the first programs of a practical nature to have been tested on the computer is the conversion program. The program actually contains two separate programs, one for converting from binary to binary-coded decimal and one for binary-coded decimal to binary, both stored together in test storage. These two programs are each of interest as display programs. The insertion of a binary number in one register (the flip-flop registers are used since they have lights and switches in the control room) and the selection of the proper program yields as a result the decimal equivalent, one decimal digit appearing in binary-coded form in each of the 4 remaining flip-flop registers. The insertion of decimal numbers with the proper program yields the binary equivalent. One of the two programs is selected by setting the program counter reset switches to the register containing the first order of the desired program.

The computer actually performs the conversions repeatedly at a rate of about 5000 conversions per second.

For test purposes the two programs are combined so that a binary number is converted to coded decimal form and then the coded decimal result is reconverted to binary form and checked against the original binary number. The binary number is then increased by adding a 1 in the right-hand end, and the process is repeated. In this way the computer is made to perform and check all possible conversions from 1 to 16383, a feat requiring about 7 seconds (n.b., the computing times are given for the present system using test storage with its 1-microsecond access time; when electrostatic storage is used, the times will be at least doubled, since ultimate access time of at best 5 or 6 microseconds is anticipated). The details of the conversion program (known as Test Program No. V) appear in E-299.

6.25 Demonstration Programs Using Special Display

The recent installation of special display equipment (see Sections 2.22 and 5.2 of this report) provided an opportunity to try some programs intended for use with test storage and the display scope, such as the programs discussed in E-220. An important convenience factor had to be considered, namely that it is desirable to be able to alter the program slightly or even to change the program completely by using the switches on the test-control racks. By use of the switches which determine the numbers to which the flip-flop storage registers and the program counter are reset, a change can be introduced without any interruption while the computer is in operation, since the registers in question are actually reset only by a pulse from special display during the flyback time of the display scope. The switches of toggle-switch storage (since they, unlike the reset switches, actually pass video pulses) are in the computer room and hence, although readily accessible, are not "front panel" controls.

With these factors in mind, two quite elementary programs were written, each being quite short so that both can be stored simultaneously in toggle-switch storage, and either one selected at will by changing the program counter reset switches (the same scheme was used in the conversion program, Section 6.24 above).

The first of these programs simply plots the values of x, x^2, and x^3 for x between -1 and 1. In this powers-of-x program, the values are plotted for $-1 + 2^{-15} + nh$, where n simply increases until a value of x greater than 1 is reached and where the value of the increment h can be chosen at will, using the reset switches of a flip-flop register. Photographs of the resultant curves are shown in connection with Section 2.22 of this report. The program used proceeds as follows (see Summary Report 19 for explanation of code):

Register No.	Order	Description
1	ca 10	Puts the content of register No. 10, originally $-1 + 2^{-15}$, into AC
2	ad 11	Adds the desired increment to the x in AC
3	qd 10	Stores the new value of x in register No. 10 and displays x on the display scope
4	mh 10	Multiplies x in AC by x from register No. 10, forming x^2 in AC
5	qd 9	Stores x^2 in a dummy register and displays x^2 on the display scope
6	mh 10	Multiplies x^2 in AC by x from register No. 10, forming x^3 in AC
7	qd 9	Stores x^3 in a dummy register and displays x^3 on the display scope
8	sp 1	Returns to the order in Register No. 1, thus repeating the cycle for a new value of x
(FF register) 9		Temporary storage
(FF register) 10		Contains x, reset to 1.000000000000000 initially
(FF register) 11		Contains h equals approximately 2^{-7}

No provision is made to prevent the value of x from overflowing (becoming greater than 1). The arithmetic check pulse is suppressed by means of a front panel switch for this program so that no alarm occurs. The effect of an overflow is, therefore, to start over again at -1. The plot of values of x from -1 to 1 is therefore simply repeated until the display scope ends its sweep and starts the whole program over again; thus by adjustment of the display sweep frequency the cycle can be stopped before x exceeds 1 and the overflow prevented if so desired.

The second display program is designed to plot the pairs of curves $\pm Ax^2$ for $-1 < x < 1$ and for several values of A in the range $1 > A \geq 0$. The program used is as follows; the registers used are in practice chosen so that they will not conflict with the powers-of-x program (the actual program is given in E-300).

Register No.	Order	Description
(FF register) 1	ca 16	Puts a value of A (initially from register No. 16) into AC
2	mh 21	Multiplies by x (initially $-1 + 2^{-15}$) from register No. 21
3	mh 21	Multiplies again by x
4	qd 24	Displays Ax^2 and stores it in register No. 24
5	cs 24	Puts $-Ax^2$ into AC
6	qd 24	Displays $-Ax^2$ and stores it in register No. 24
7	ao 1	Increases the content of register No. 1 by 2^{-15} (initially changing from ca 16 to ca 17), thereby selecting a new value of A
8	su 23	Subtracts ca 15 + n from the quantity ca 16 + n in AC (where n is the number of pairs of curves desired)
9	cp 1	If the result is negative or 0, meaning that fewer than n pairs have been plotted, control is returned to register No. 1 to plot another pair
10	ca 21	All the curves having been plotted for one value of x, x is put into AC
11	ad 22	h is added to x, thereby giving a new value of x
12	ts 21	The sum is stored in register No. 21
13	ca 20	The order ca 16 comes to AC from register No. 20
14	ts 1	The order ca 16 is stored in register No. 1, thus preparing to repeat the whole cycle for the new value of x
15	sp 1	Control is returned to register No. 1 to repeat the whole cycle
16	0.111111111111111 = $1 - 2^{-15}$	
17	0.100000000000000 = 1/2	
18	0.010000000000000 = 1/4	
19	0.000000000000000 = 0	
20	ca 16	
(FF register) 21		Contains x, reset to 1.000000000000000
(FF register) 22		Contains h, equal approximately to 2^{-7}
(FF register) 23		Reset to ca 15 + n, where n is the number of pairs of curves desired
(FF register) 24		Temporary or dummy storage

The comment made in the last paragraph concerning the overflow as x is increased past 1 is applicable here. The two programs appear to require 11 + 24 = 35 registers, but since registers 9, 10, and 11 in the first program serve the same purpose as registers 24, 21, and 22 in the second program, these registers can be common to both, and only 32 total registers are required. Note that by changing the reset switches of register 23 the number of pairs can be varied. The increment h and the initial value of x can be changed in both programs.

6.3 NUMBER OF ELECTROSTATIC STORAGE REGISTERS IN WWI

6.31 The 2048-Register Specification

WWI is limited to 2048 registers of storage by the register length of 16 binary digits: 5 digits are assigned to operation selection and 11 digits to the address or storage-location selection. More than 2048 storage registers would require an address with more than 11 digits, which would in turn require an increased register length. Increasing the register length of WWI may be desirable for other reasons and may actually be accomplished in the future, but this problem is not under discussion here.

The original choice of 11 address digits for 2048 storage registers in WWI was made on the following basis: For convenience in selection, the linear array should be a power of 2, thus making the total array a power of 4. It was felt that 16×16 or 256 would be inadequate, 32×32 or 1024 attainable and reasonable, and 64×64 or 4096 of substantial difficulty in both tube design and deflection-circuit design. Therefore 32×32 was specified as the density. The selection of one spot in such a tube requires 10 binary digits, 5 to select the vertical deflection and 5 to select the horizontal deflection. A total of 11 digits was specified, to provide for 2 banks of tubes. In view of the original conception of WWI as a prototype for larger machines, a study of the operation of multiple banks is more important than the provision of twice as much storage.

6.32 Usefulness of Initial 256 Registers

The first bank of storage tubes to be installed in WWI will have a storage capacity of 16×16 spots. The efforts of the development group have been applied almost entirely to the problems of stability, reliability, and reproducibility, with relatively little consideration given to increasing the storage density or reducing the access time. Consequently the production run of tubes for WWI, which will begin in the next quarter, will be of the 16×16 design.

During the several months which will elapse between the initial operation of WWI with 16×16 tubes and the completion of replacement tubes of greater capacity, the machine will necessarily be restricted to limited classes of useful problems. These classes are by no means insignificant.

A storage capacity of 256 registers (or more descriptively, 4096 binary digits), while small compared to the needs of the large-scale electronic calculator, is substantial compared to the capacities of existing machines. There are many problems fitting this storage capacity that are not trivial. An example of such a problem is the solution of a non-linear differential equation with two-point boundary conditions, of order up to fifth or more depending on the complexity of the problem.

A capacity of 256 storage registers will handle segments of most problems of ultimate interest and will be adequate for many months during which the use of a machine like WWI is being studied. All basic code sequences can be tested, and methods of machine operation and the use of library programs can be developed. Many scientific problems which tax the commonly available computing facilities can be handled with limited storage working in cooperation with input-output tape equipment.

It is expected that additional storage capacity will be available before the possibilities of 256 registers have been fully explored.

6.4 OPTIMUM SPOT NUMBERING SYSTEM FOR INTERIM WWI STORAGE TUBES

The numbering of the stored spots in the storage tubes in WWI is by no means fixed by the nature of the tubes. The particular spot chosen by a particular address is of no importance as long as it is the same one every time. The numbering system is determined by the nature of the deflection decoders and by their connections to the main bus. Since there are no logical restrictions except that the numbering system be consecutive, it can be chosen on the basis of convenience or flexibility or both.

As described in Section 6.3 of this report, the density specified for WWI storage tubes is 32×32. In order to select any spot in this array, two 32-position (5-binary-digit) deflection decoders have been designed and built (see Section 4.323). These are of the binary-weighted current-adding type.

Many different connections of the decoders are possible, some of which are shown in the accompanying diagrams. The curves and table show that the connections of Figure 4 have great advantages in certain cases. Particularly with tubes capable of storing an array intermediate between 16×16 and 32×32, this arrangement gains both in the total

number of available registers and in the number of consecutively numbered registers.

If the inputs to these decoders are connected to the main bus in the simple order shown in Figure 1, then spot numbering starts with 0 in one corner of the tubes of one bank (the upper left corner is shown for convenience, but the actual corner depends on how you look at the tube). The numbering proceeds along a row, then starts over on the next row, etc. Spot No. 1023 is in the lower right corner. When two banks of tubes are used bus digit 5 is connected to the bank-selection FF. Spot No. 1024 is in the upper left corner of the tubes in the second bank, with the numbering proceeding as in the first bank. This numbering system is simple and straightforward; it was originally selected as the numbering system for the 32×32 tubes.

But trouble arises when it becomes desirable to substitute tubes storing less than 32×32 digits. The first problem is the numbering for 16×16 tubes. The simplest approach physically is simply to disconnect the inputs to the 1's increments in both decoders. This will omit every other row and every other spot in the remaining rows. See Figure 1. A 16×16 array will remain, with centering and gain for the deflection generators unchanged. The difficulty is that the remaining registers are no longer consecutively numbered. Gaps in the sequence of numbers are at best a great nuisance to the programmer, and at worst render the machine completely useless.

This arrangement is one of the worst possible. WWI is a single-address machine and as such takes its orders consecutively unless interrupted by a subprogram order. There are no consecutively numbered registers in the above arrangement; consequently the only recourse for the machine is to make every order a subprogram order directing the machine to omit the succeeding nonexistent register. This is an extreme situation. Practically, non-consecutively numbered registers have a value provided they are accompanied by a sufficient group of consecutively numbered registers to hold the orders. The non-consecutively numbered registers can be used for constants and partial results or even for short subprograms if the registers come in groups. The ideal is for all usable registers to be consecutively numbered.

Many numbering systems will provide consecutive numbering for all 256 registers in 16×16 tubes, one of them being shown in Figure 2. The 1's digit in each decoder is left unconnected. The remaining sections are connected in order, with the right-hand 8 of the 11 bus lines assigned to the address. The numbering system is now the same as for the 32×32 tubes, but with half the number of rows and columns. This system was originally selected for the 16×16 tubes. It was planned to keep the 16×16 array until 32×32 tubes became available and then to change the cabling to that shown in Figure 1. If two banks

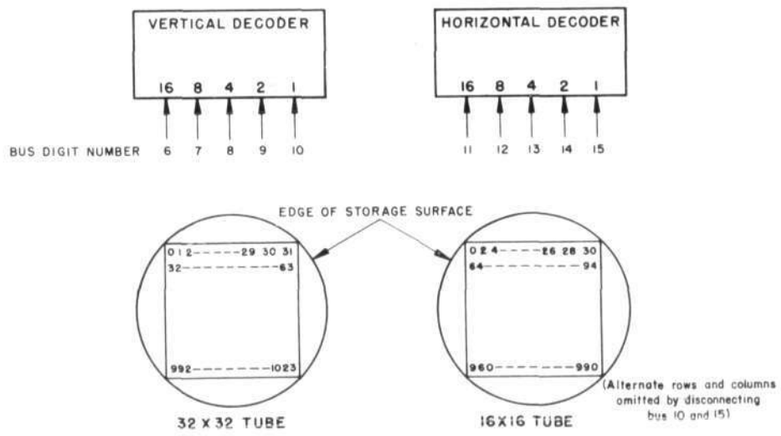


FIG. 1. OLD CONNECTIONS.