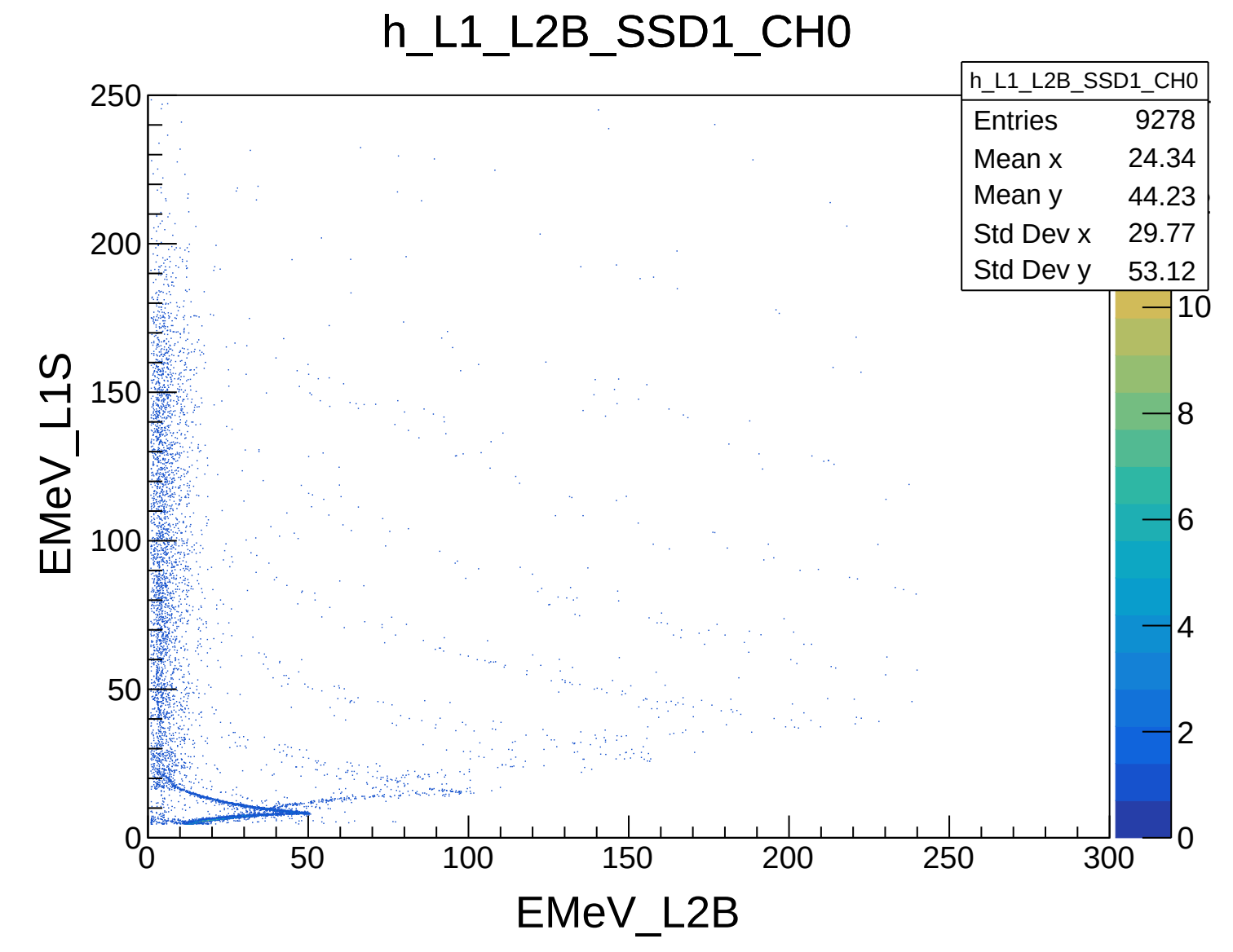
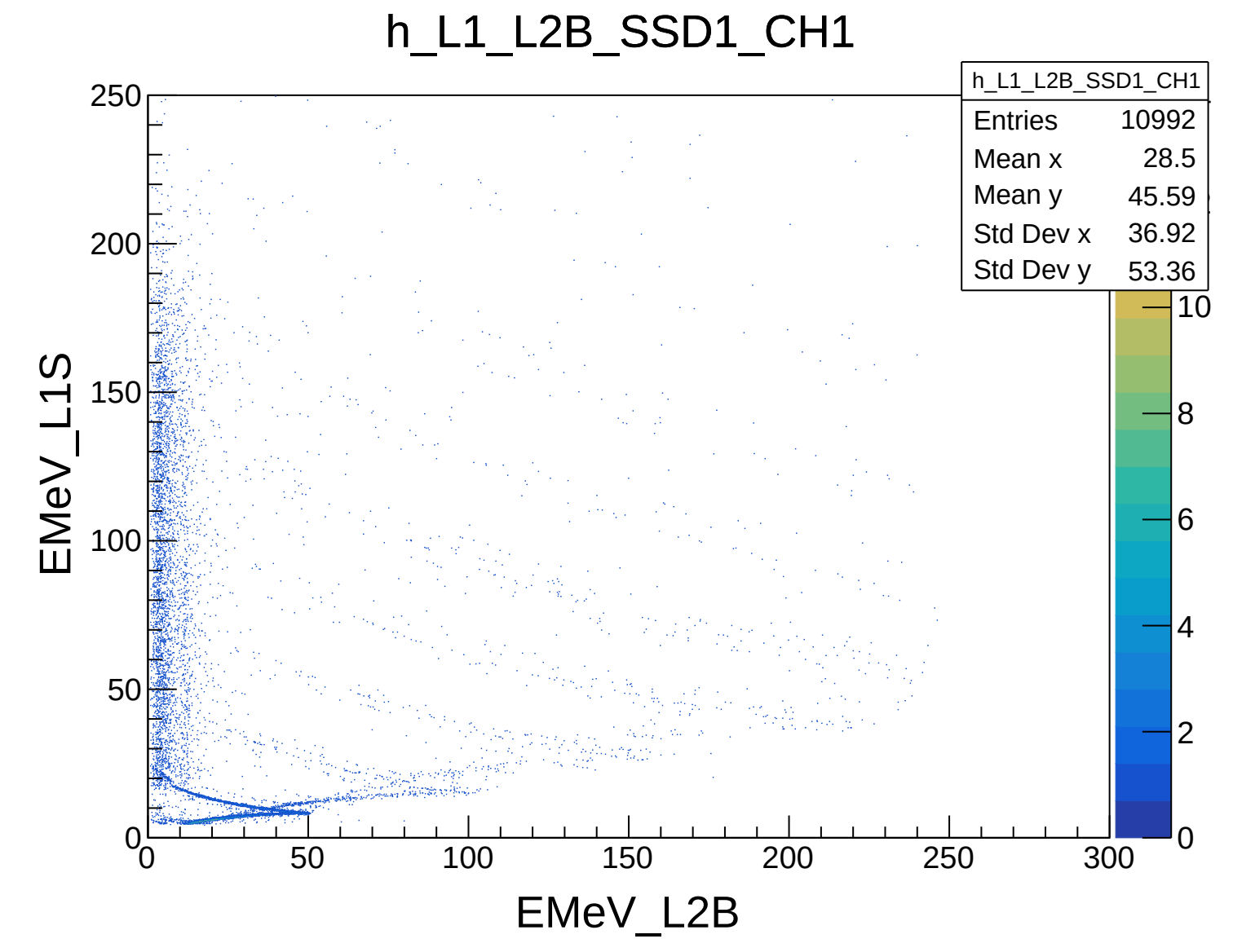
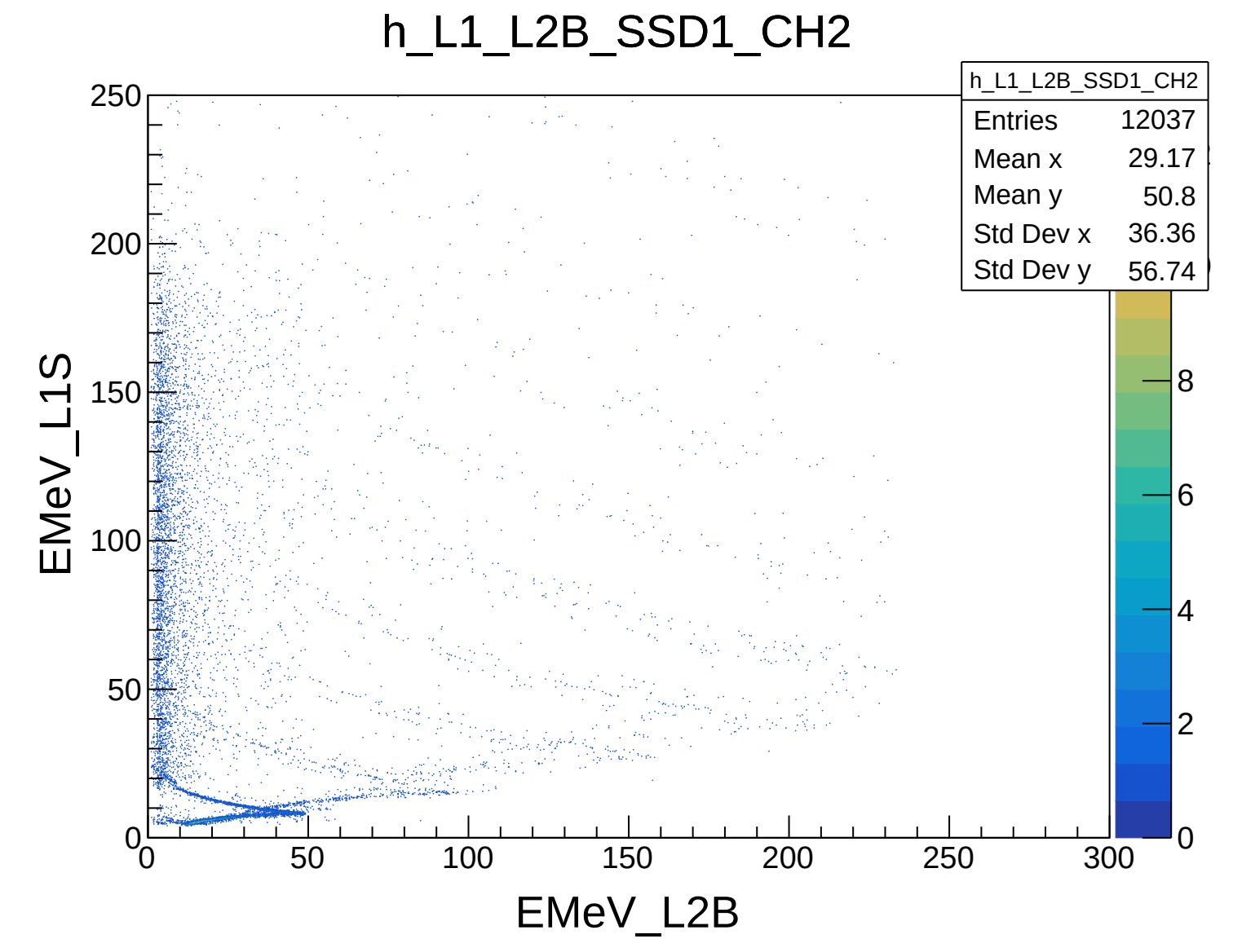
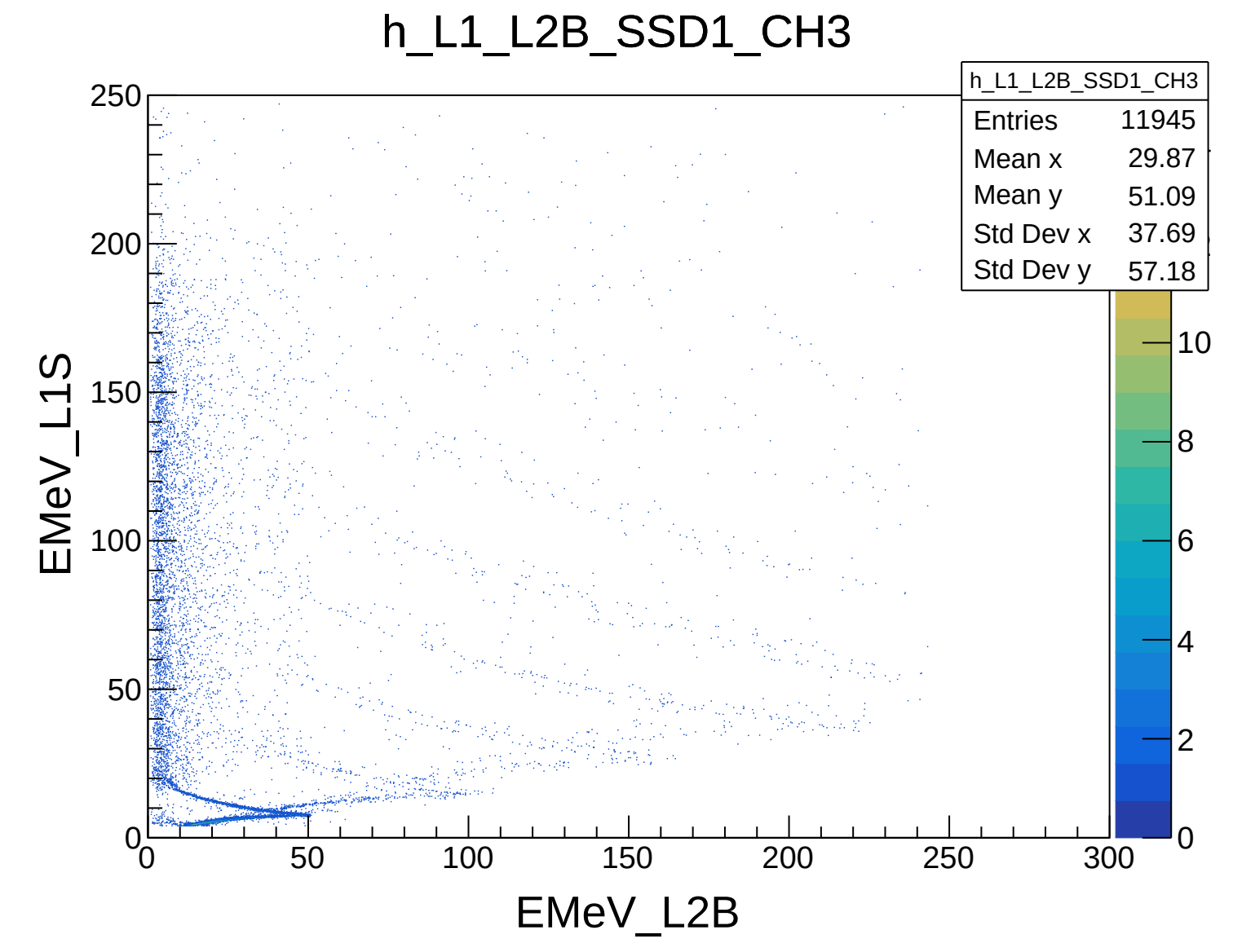
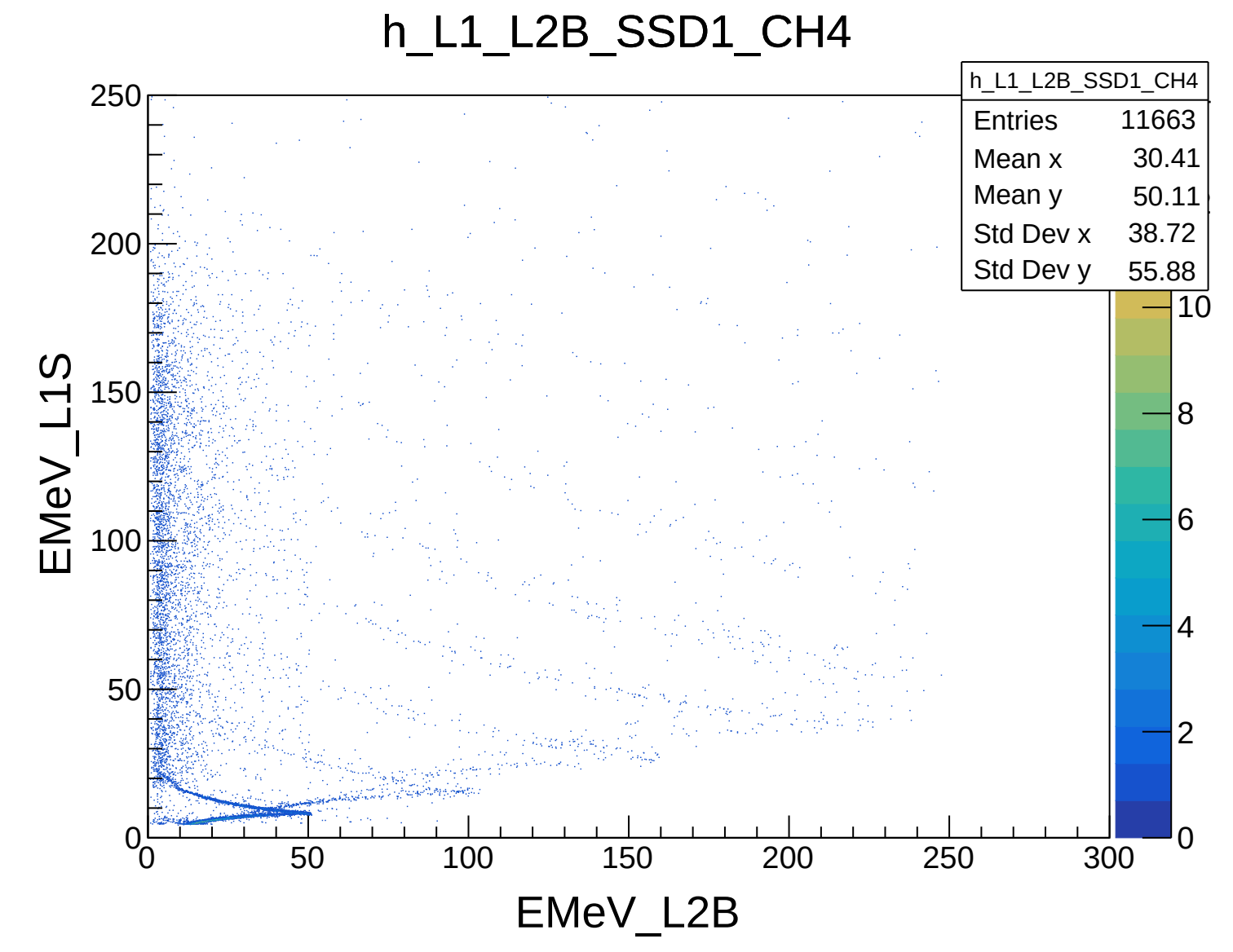
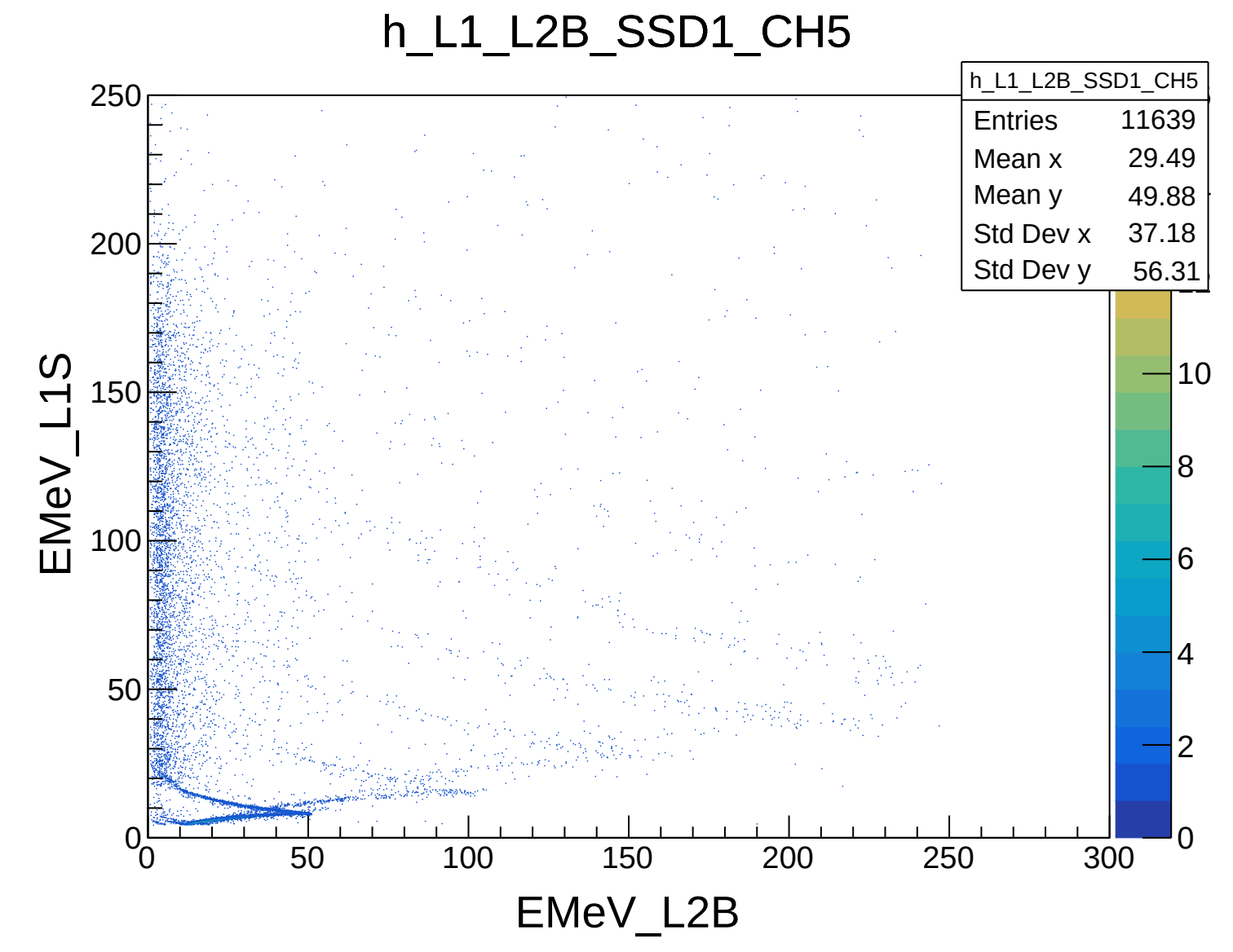

h_L1_L2B_SSD1_CH0
h_L1_L2B_SSD1_CH0
Entries 9278
Mean x 24.34
Mean y 44.23
Std Dev x 29.77
Std Dev y 53.12
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10

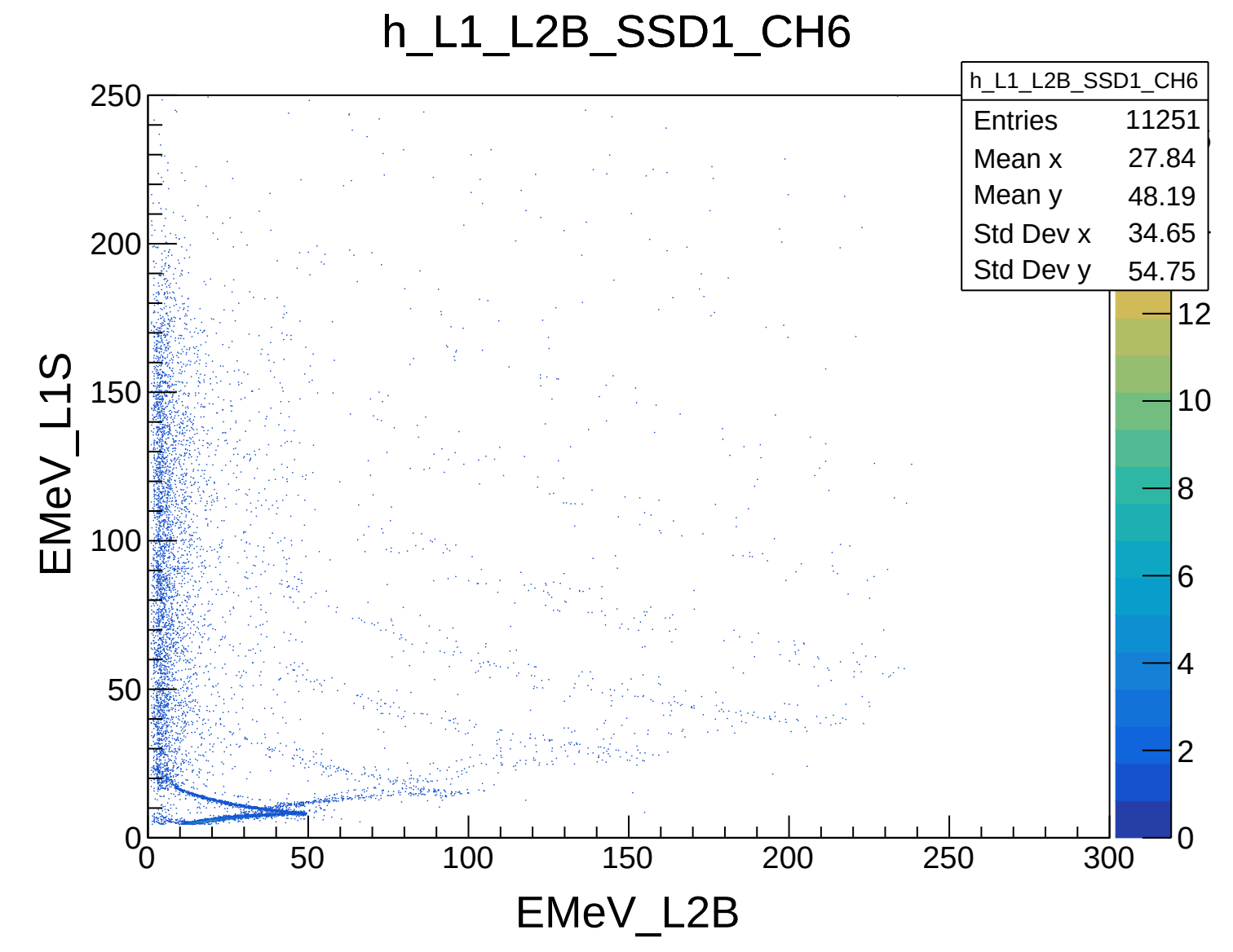

h_L1_L2B_SSD1_CH1
h_L1_L2B_SSD1_CH1
Entries 10992
Mean x 28.5
Mean y 45.59
Std Dev x 36.92
Std Dev y 53.36
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10

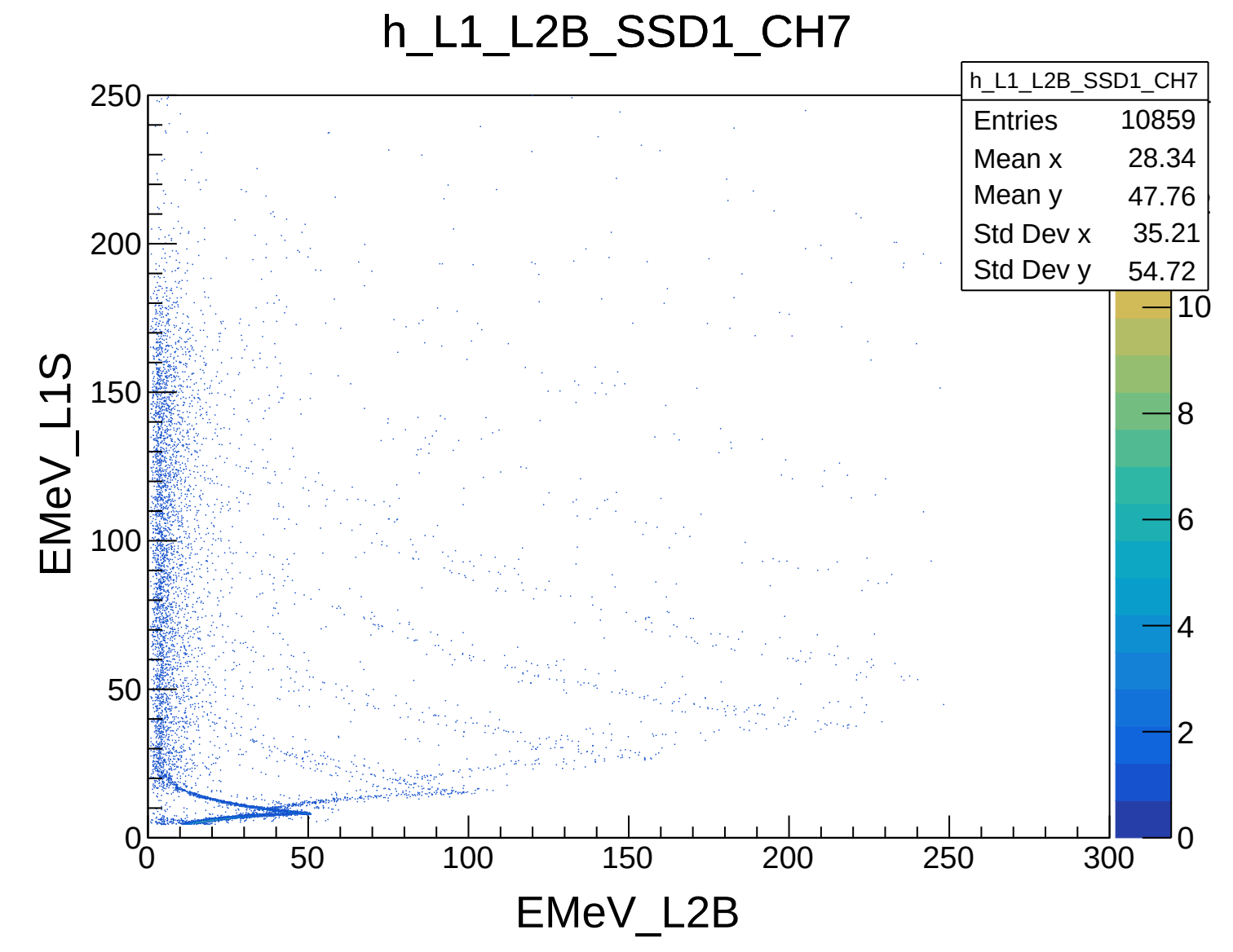

h_L1_L2B_SSD1_CH2
h_L1_L2B_SSD1_CH2
Entries 12037
Mean x 29.17
Mean y 50.8
Std Dev x 36.36
Std Dev y 56.74
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8

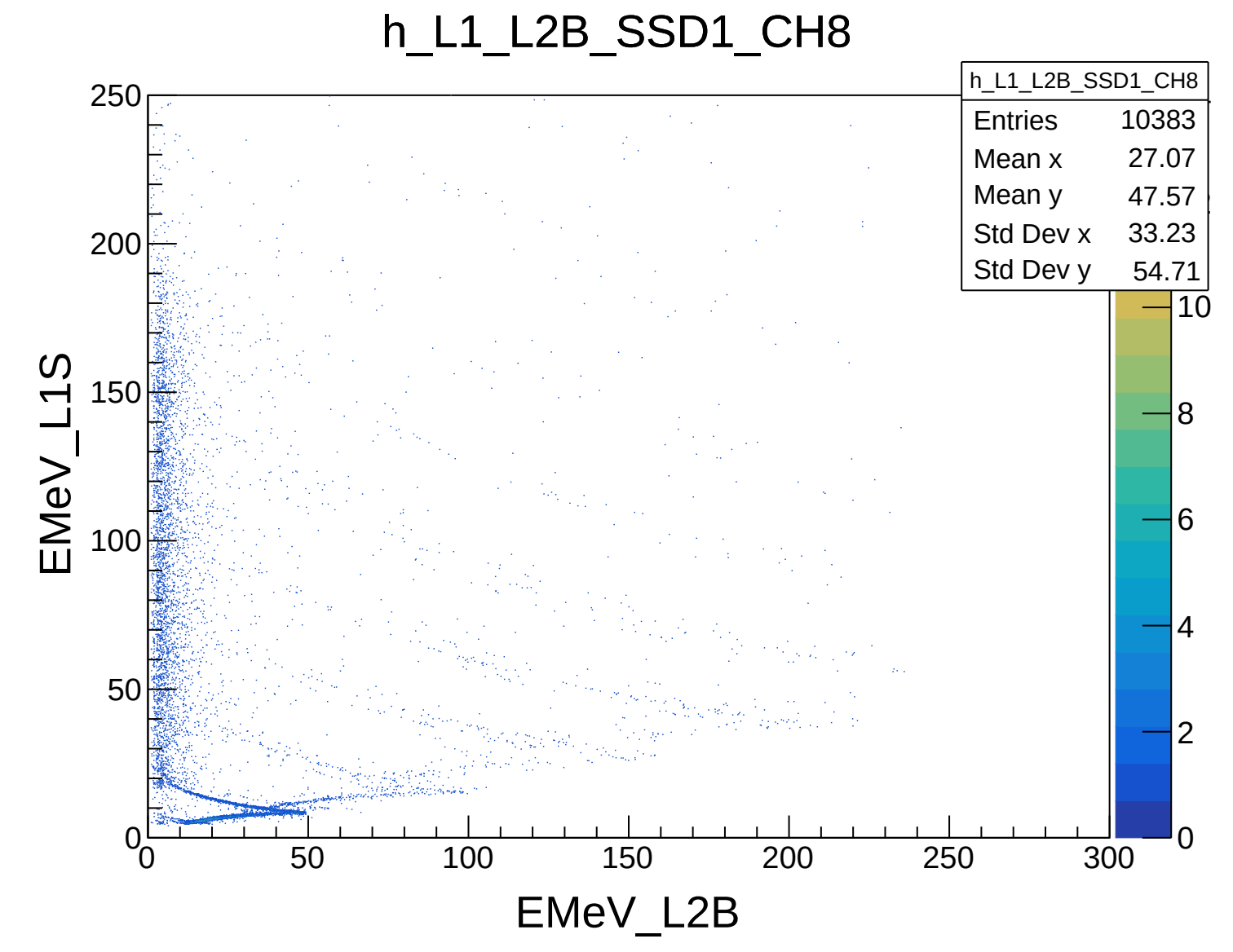

h_L1_L2B_SSD1_CH3
h_L1_L2B_SSD1_CH3
Entries 11945
Mean x 29.87
Mean y 51.09
Std Dev x 37.69
Std Dev y 57.18
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10

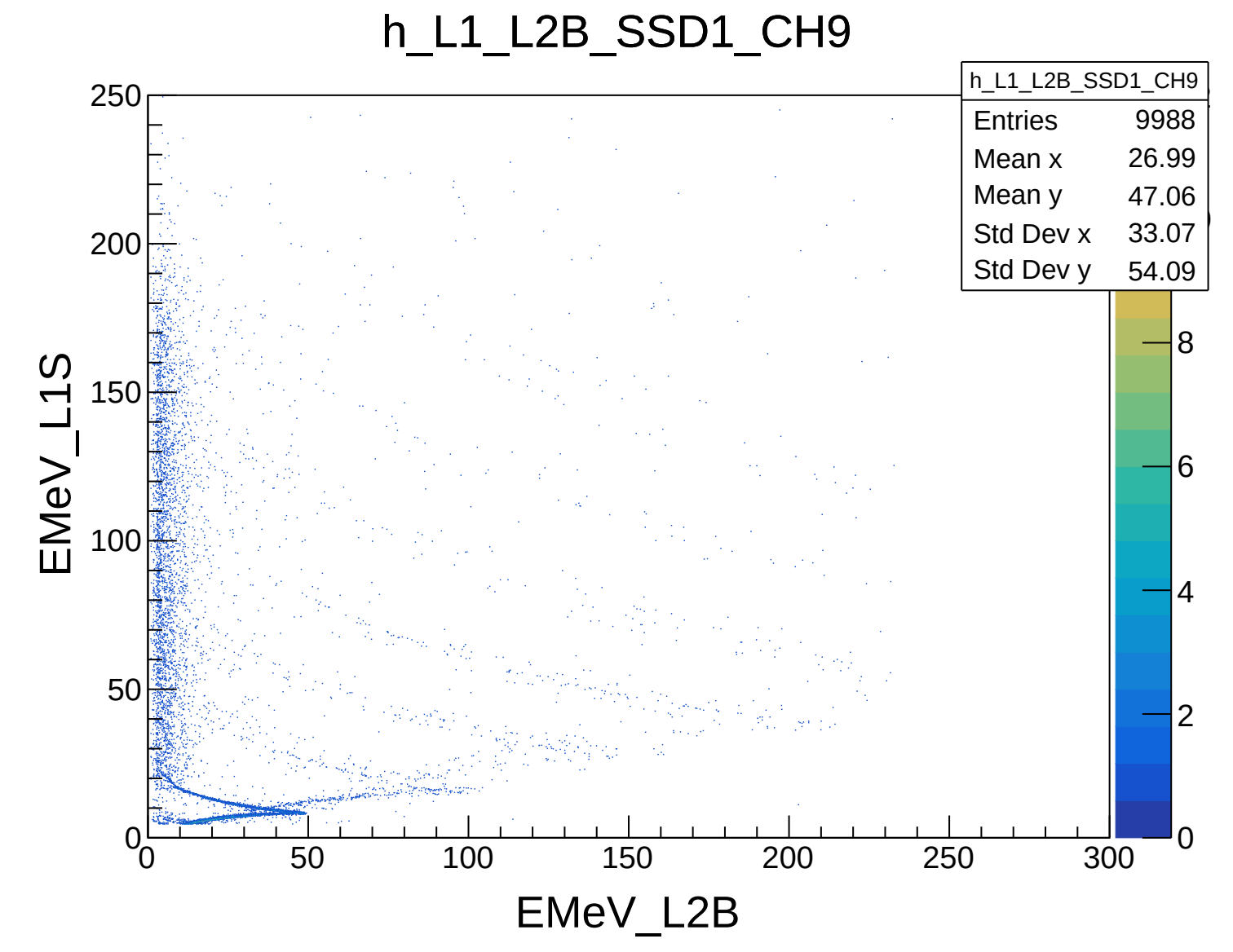

h_L1_L2B_SSD1_CH4
h_L1_L2B_SSD1_CH4
Entries 11663
Mean x 30.41
Mean y 50.11
Std Dev x 38.72
Std Dev y 55.88
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10

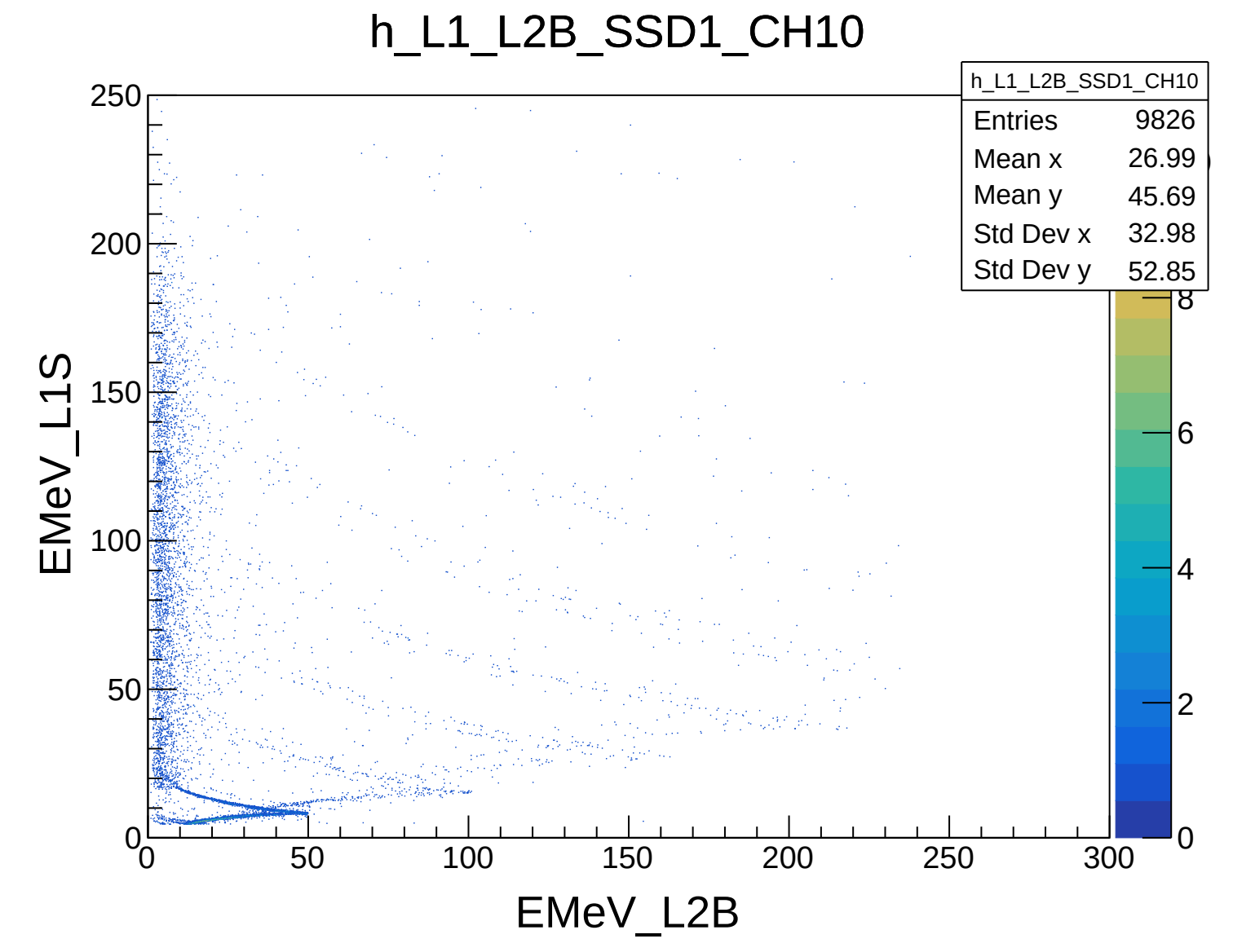

h_L1_L2B_SSD1_CH5
h_L1_L2B_SSD1_CH5
Entries 11639
Mean x 29.49
Mean y 49.88
Std Dev x 37.18
Std Dev y 56.31
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10

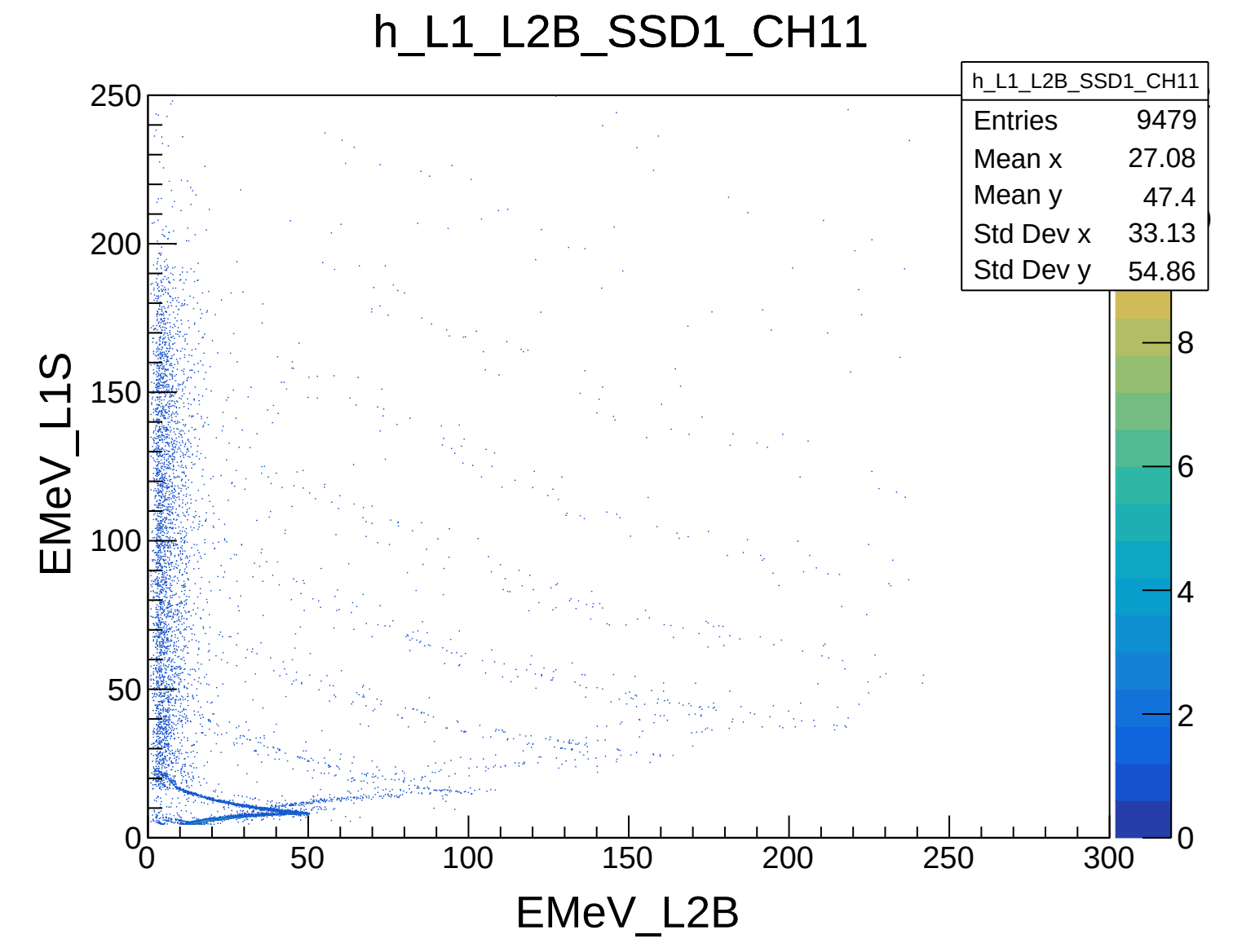

h_L1_L2B_SSD1_CH6
h_L1_L2B_SSD1_CH6
Entries 11251
Mean x 27.84
Mean y 48.19
Std Dev x 34.65
Std Dev y 54.75
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10
12

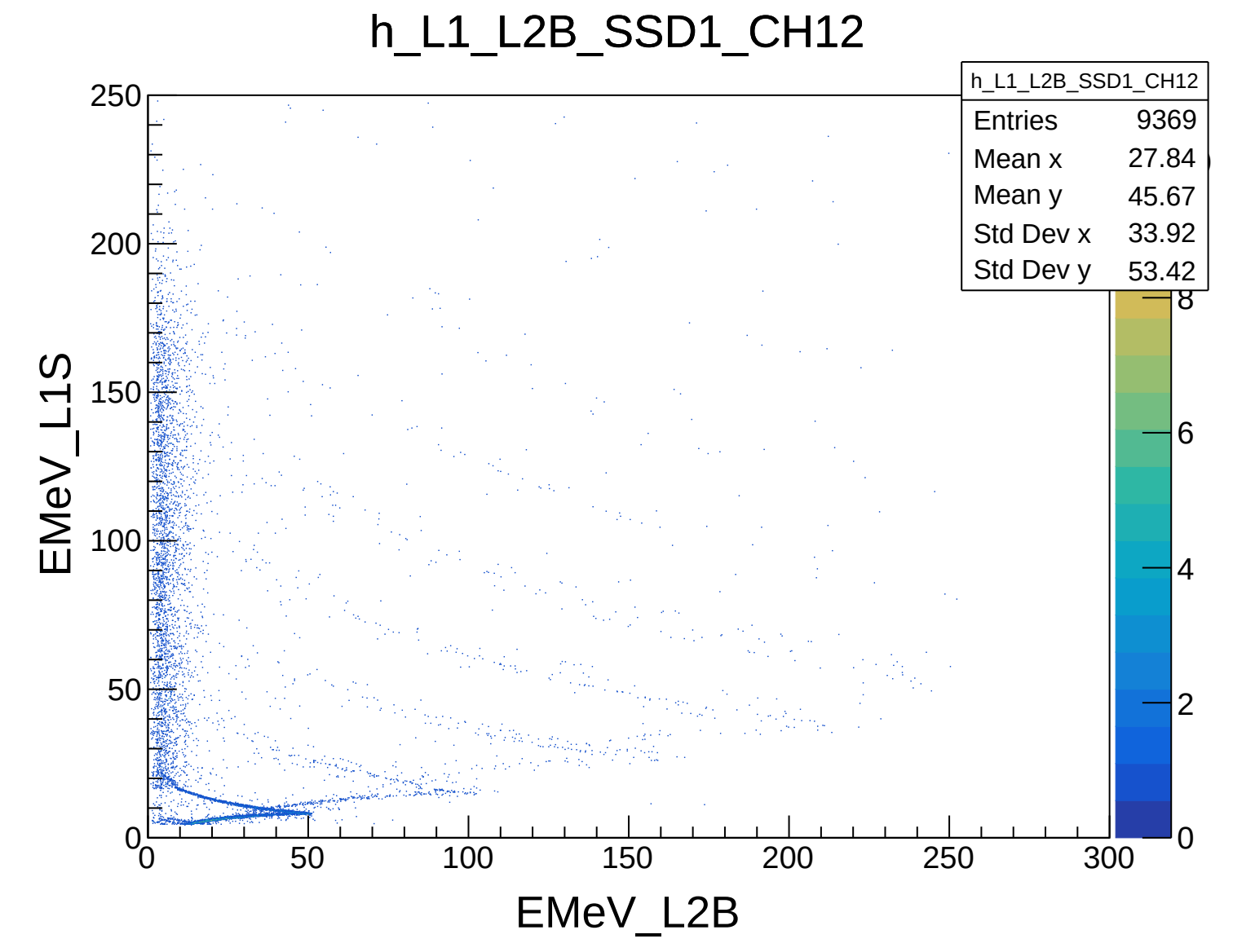

h_L1_L2B_SSD1_CH7
h_L1_L2B_SSD1_CH7
Entries 10859
Mean x 28.34
Mean y 47.76
Std Dev x 35.21
Std Dev y 54.72
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10

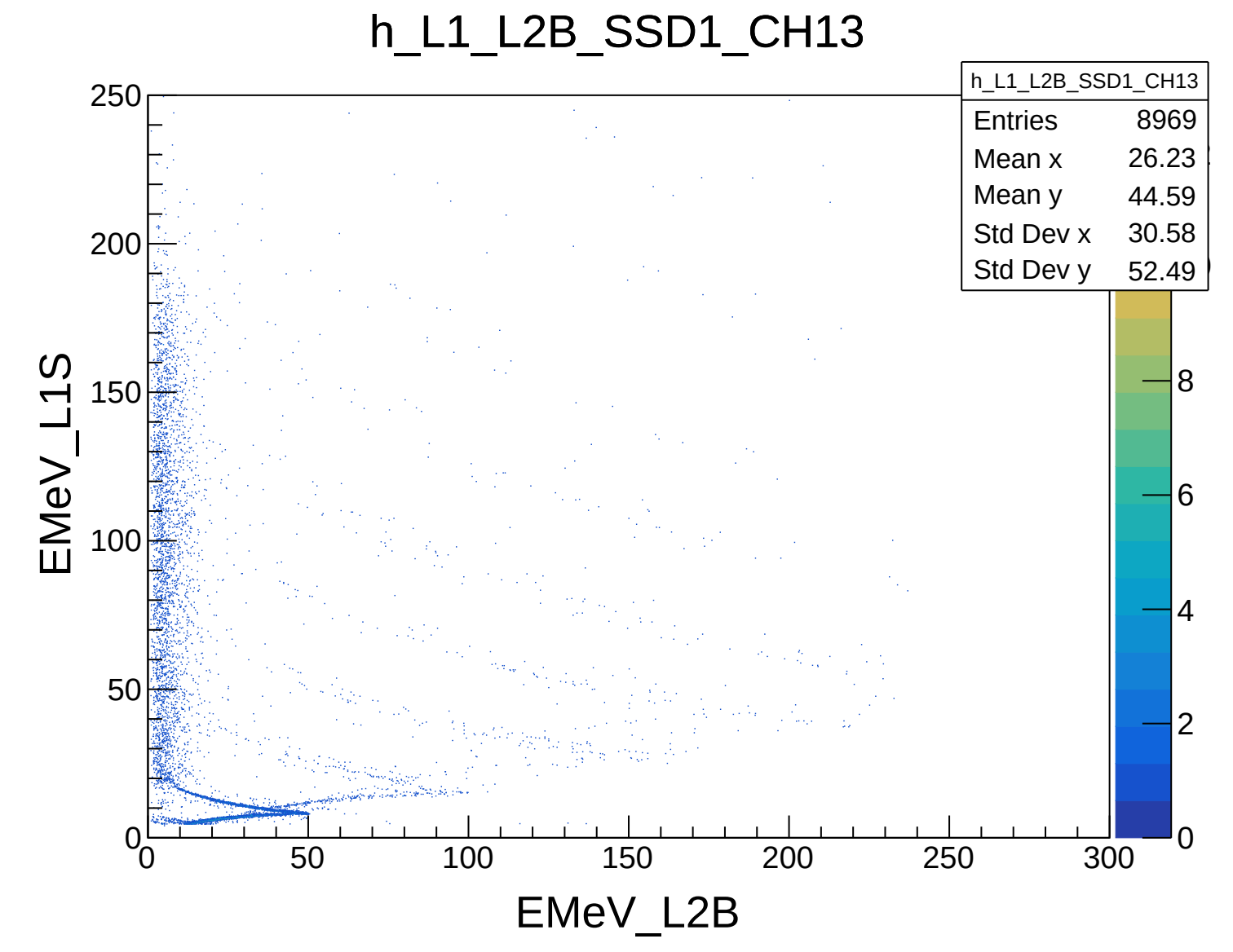

h_L1_L2B_SSD1_CH8
h_L1_L2B_SSD1_CH8
Entries 10383
Mean x 27.07
Mean y 47.57
Std Dev x 33.23
Std Dev y 54.71
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
2
4
6
8
10

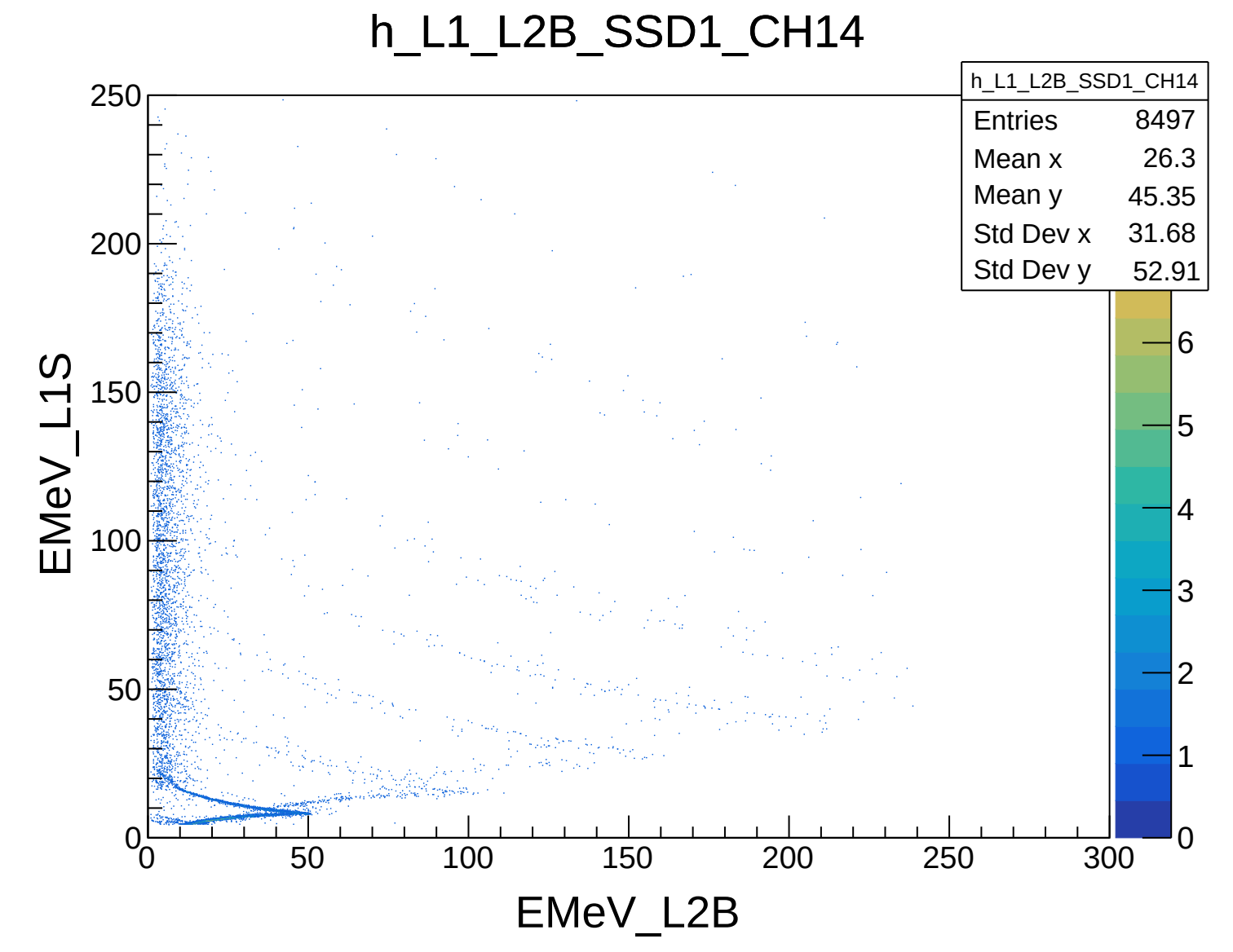

h_L1_L2B_SSD1_CH9
h_L1_L2B_SSD1_CH9
Entries 9988
Mean x 26.99
Mean y 47.06
Std Dev x 33.07
Std Dev y 54.09
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
2
4
6
8

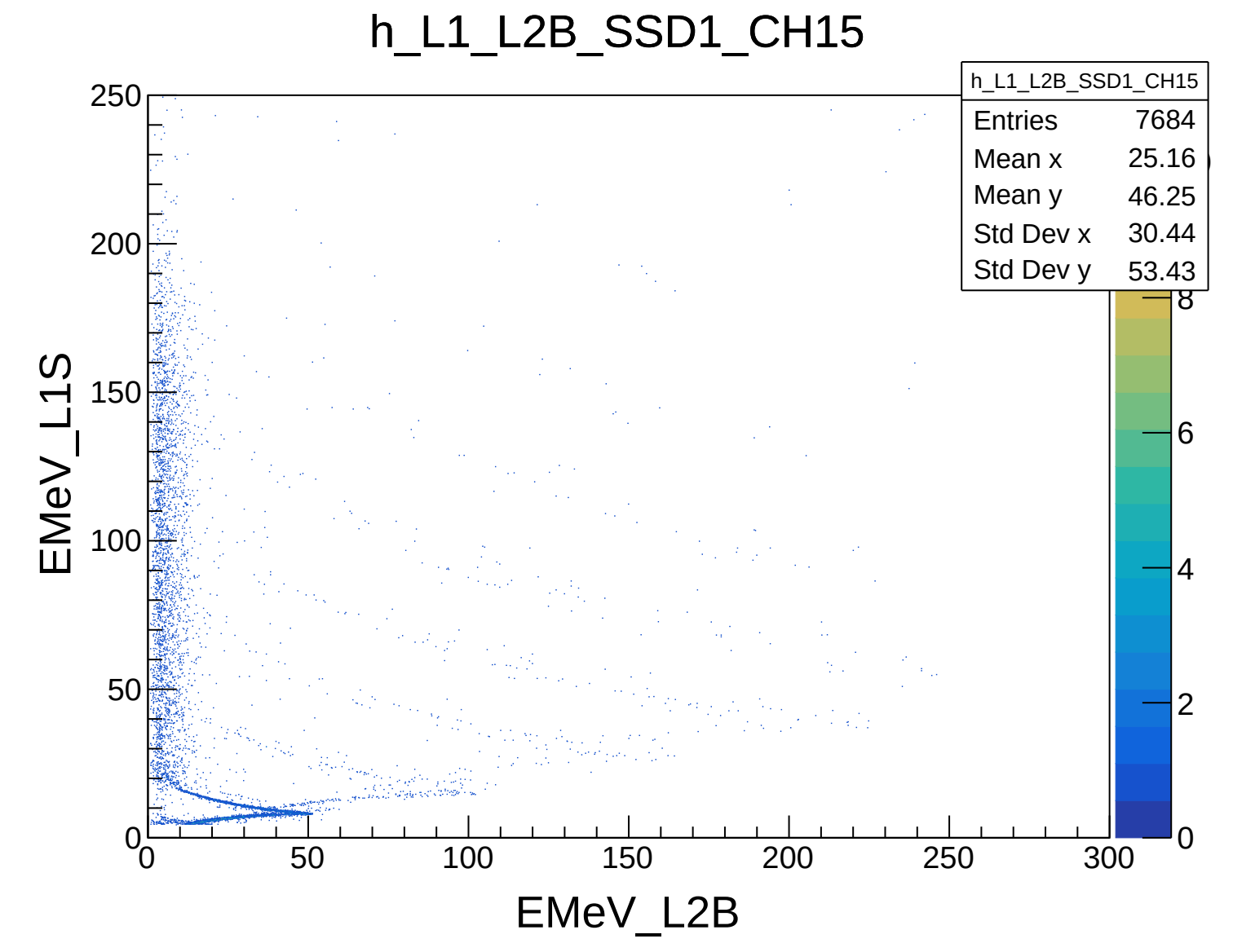

h_L1_L2B_SSD1_CH10
h_L1_L2B_SSD1_CH10
Entries 9826
Mean x 26.99
Mean y 45.69
Std Dev x 32.98
Std Dev y 52.85
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
2
4
6
8

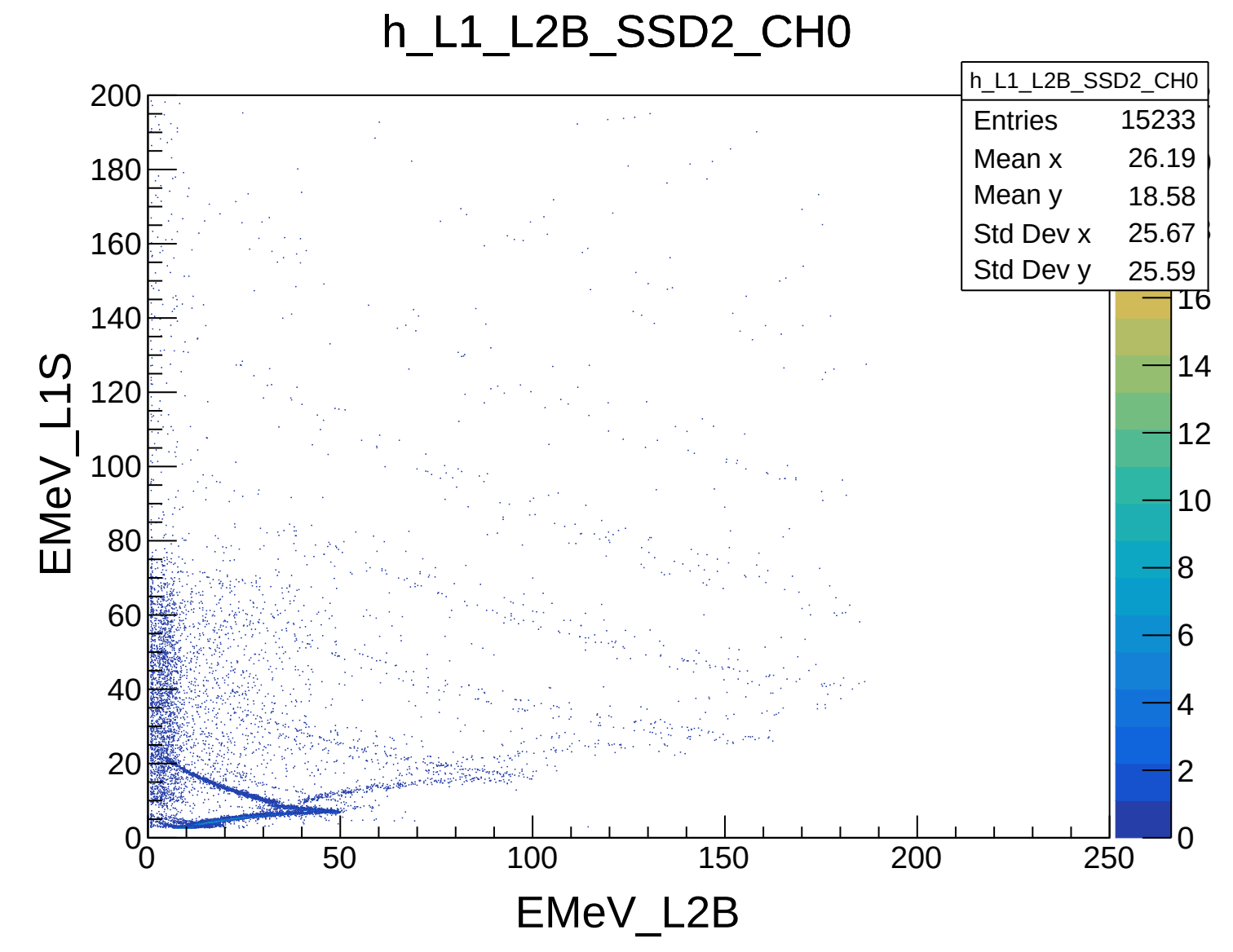

h_L1_L2B_SSD1_CH11
h_L1_L2B_SSD1_CH11
Entries 9479
Mean x 27.08
Mean y 47.4
Std Dev x 33.13
Std Dev y 54.86
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
2
4
6
8

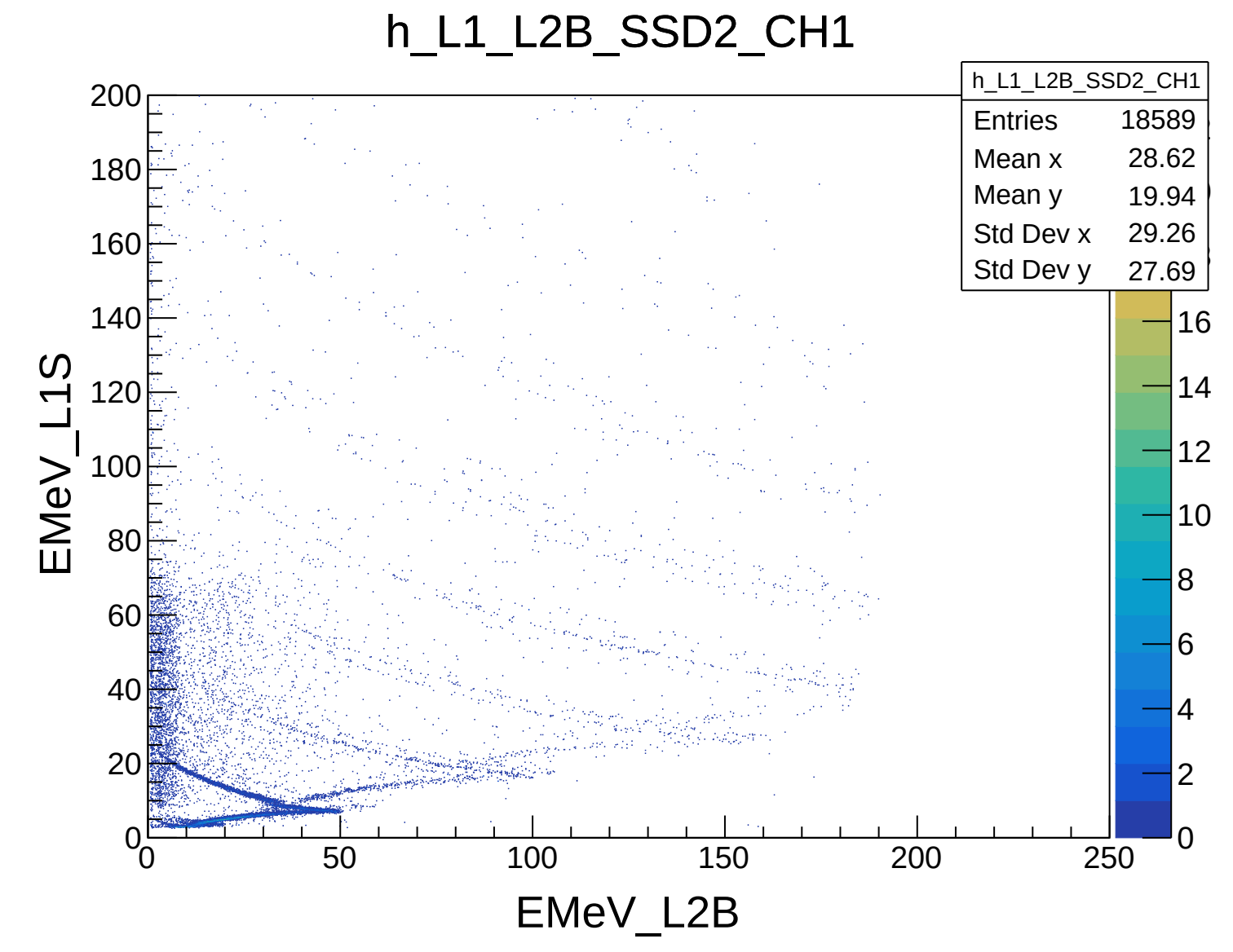

h_L1_L2B_SSD1_CH12
h_L1_L2B_SSD1_CH12
Entries 9369
Mean x 27.84
Mean y 45.67
Std Dev x 33.92
Std Dev y 53.42
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8

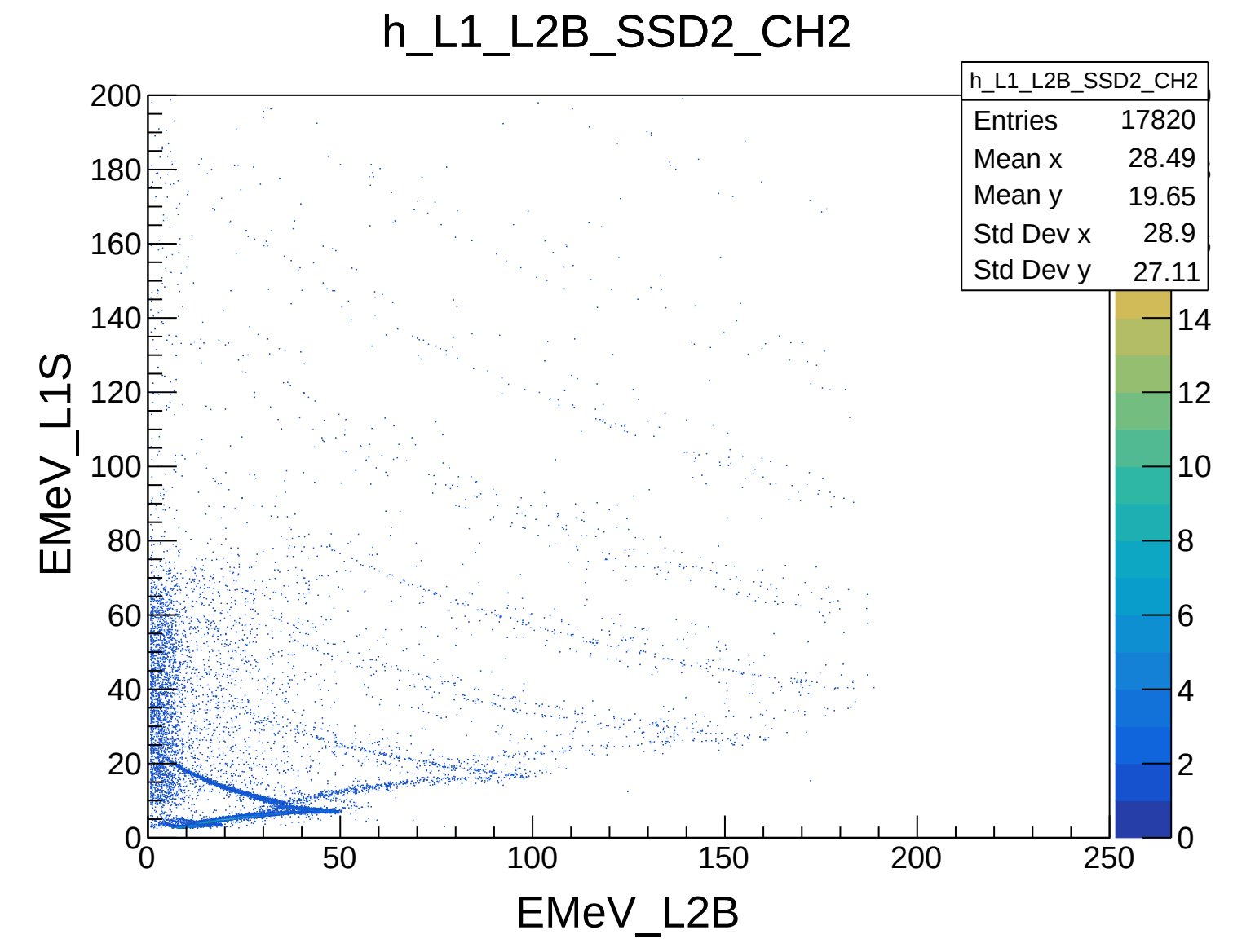

h_L1_L2B_SSD1_CH13
h_L1_L2B_SSD1_CH13
Entries 8969
Mean x 26.23
Mean y 44.59
Std Dev x 30.58
Std Dev y 52.49
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
2
4
6
8

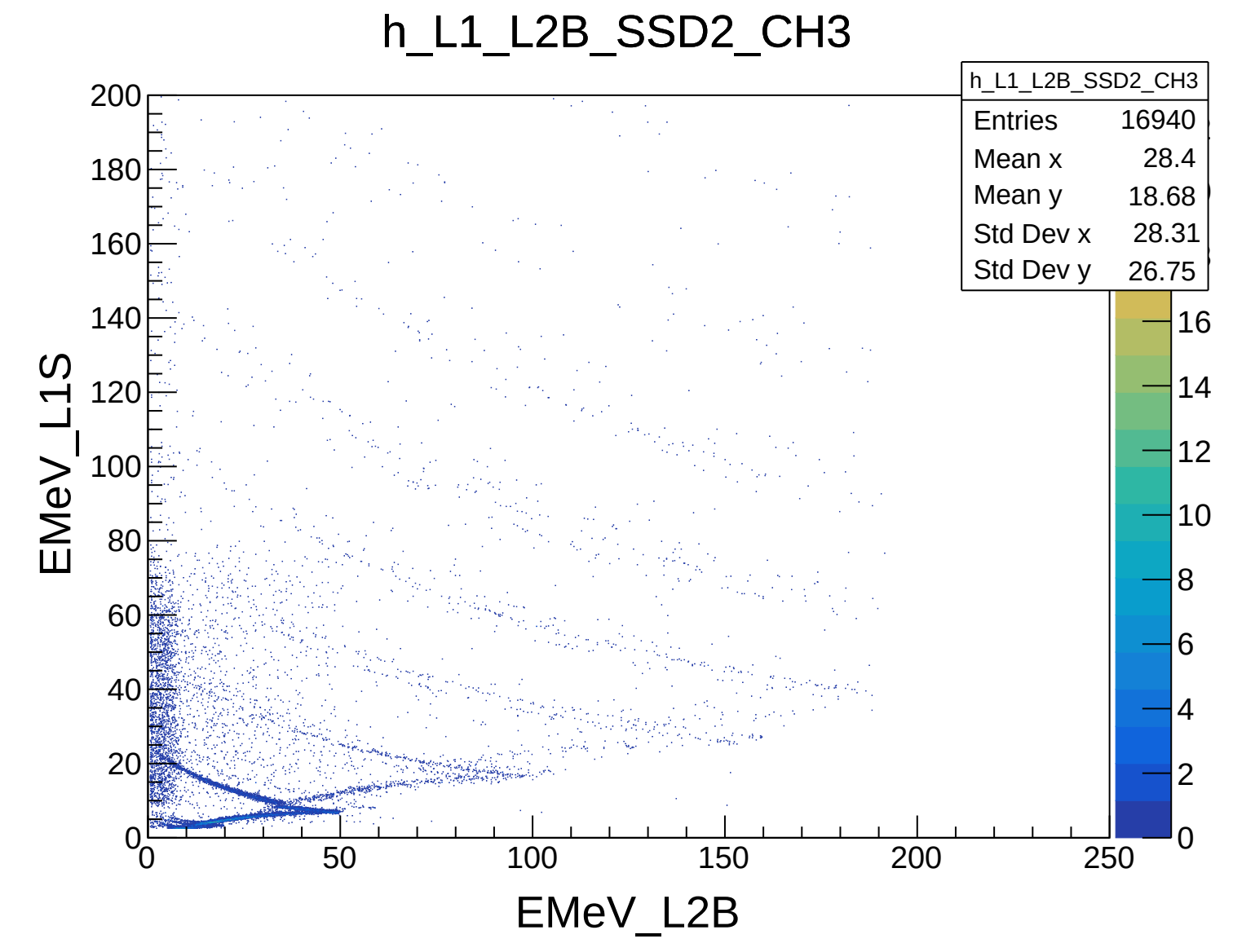

h_L1_L2B_SSD1_CH14
h_L1_L2B_SSD1_CH14
Entries 8497
Mean x 26.3
Mean y 45.35
Std Dev x 31.68
Std Dev y 52.91
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
1
2
3
4
5
6

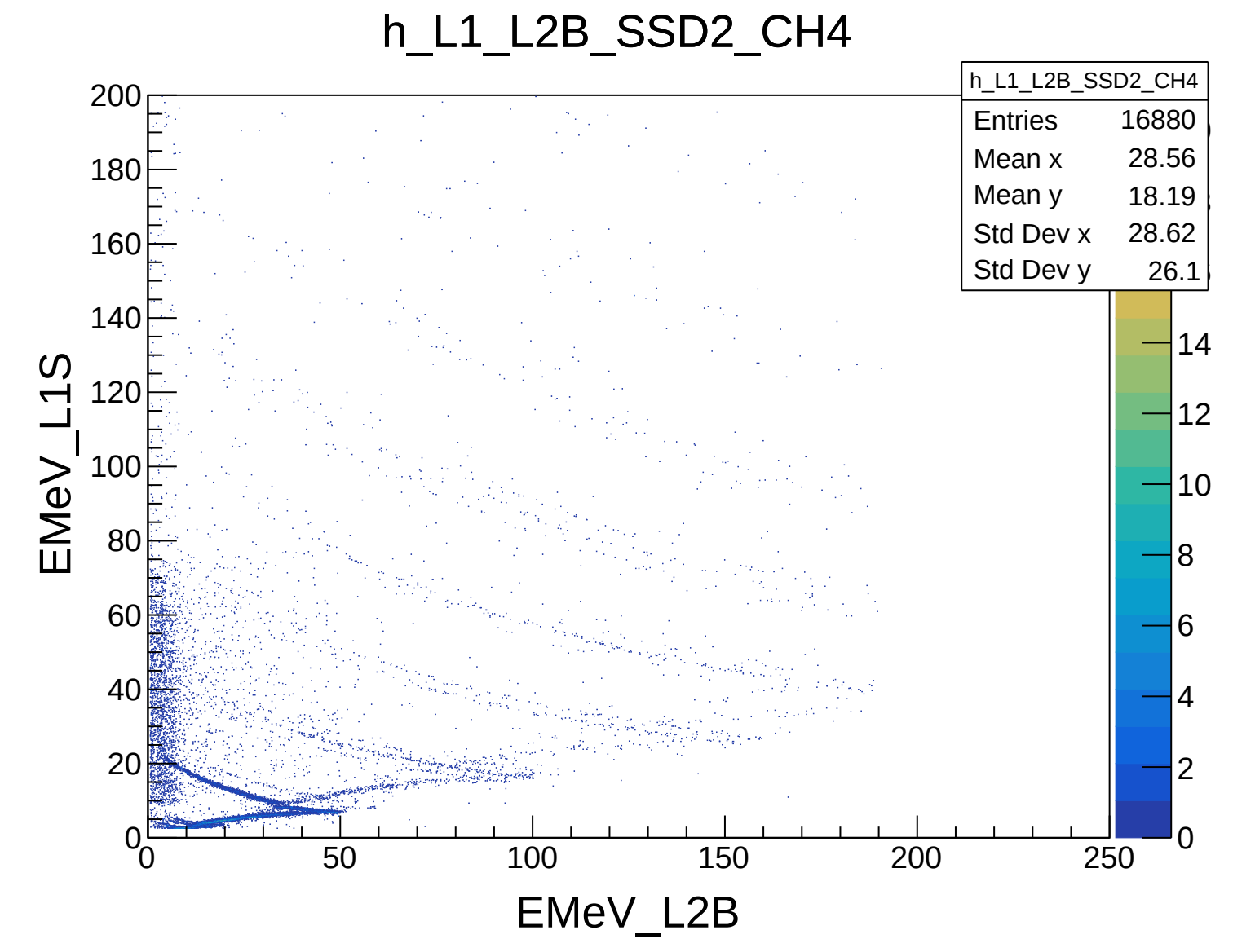

h_L1_L2B_SSD1_CH15
h_L1_L2B_SSD1_CH15
Entries 7684
Mean x 25.16
Mean y 46.25
Std Dev x 30.44
Std Dev y 53.43
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8

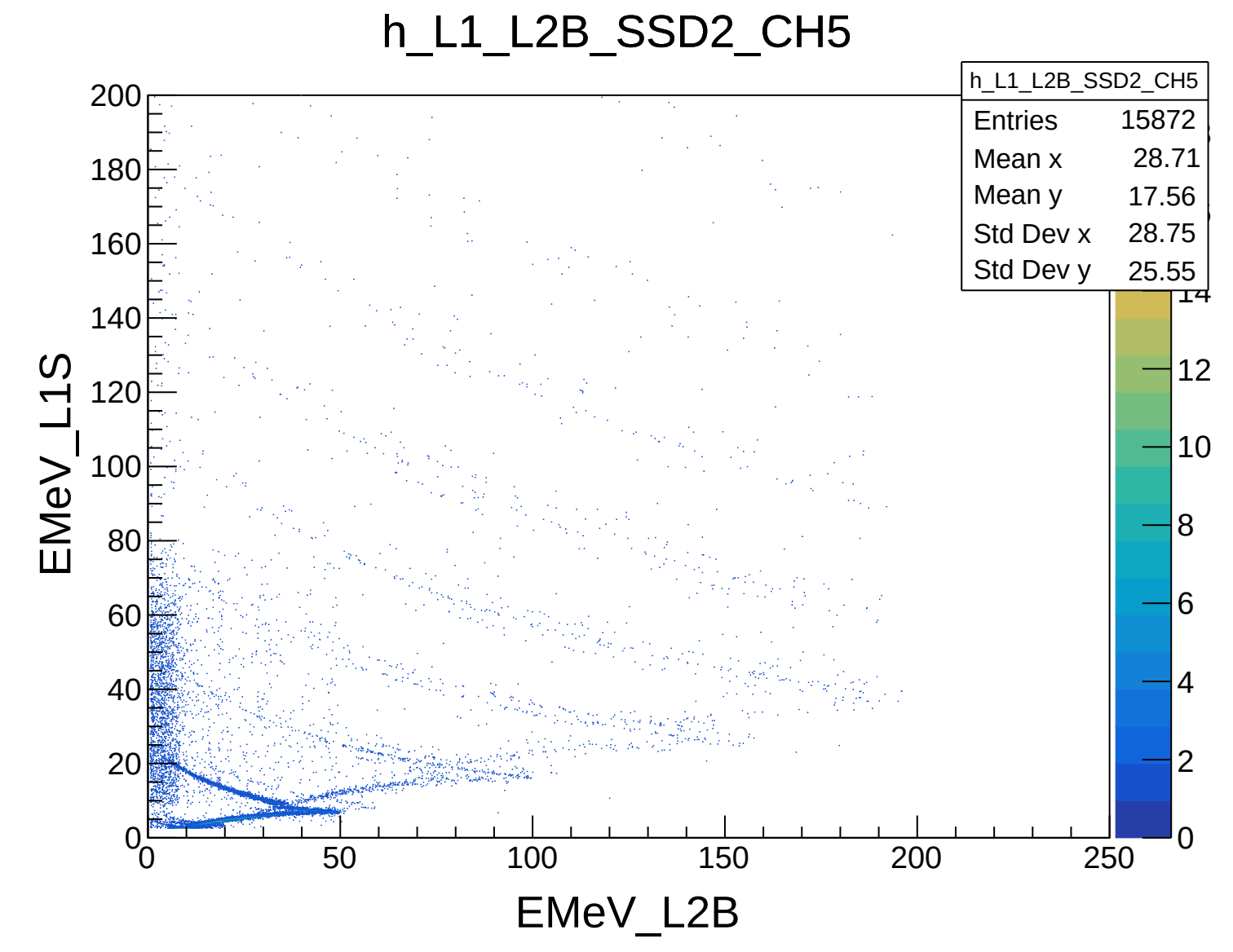

h_L1_L2B_SSD2_CH0
h_L1_L2B_SSD2_CH0
Entries 15233
Mean x 26.19
Mean y 18.58
Std Dev x 25.67
Std Dev y 25.59
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10
12
14
16

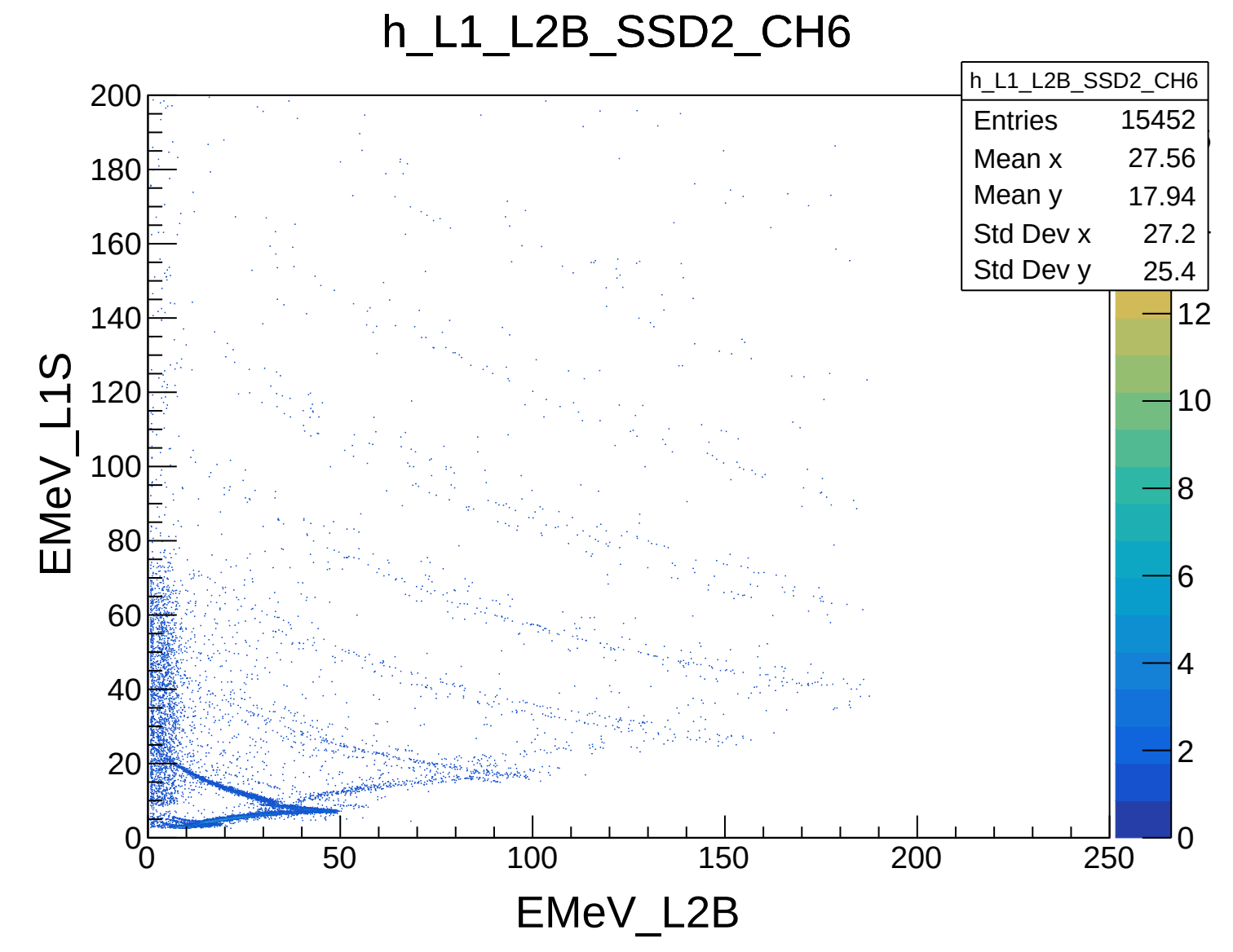

h_L1_L2B_SSD2_CH1
h_L1_L2B_SSD2_CH1
Entries 18589
Mean x 28.62
Mean y 19.94
Std Dev x 29.26
Std Dev y 27.69
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10
12
14
16

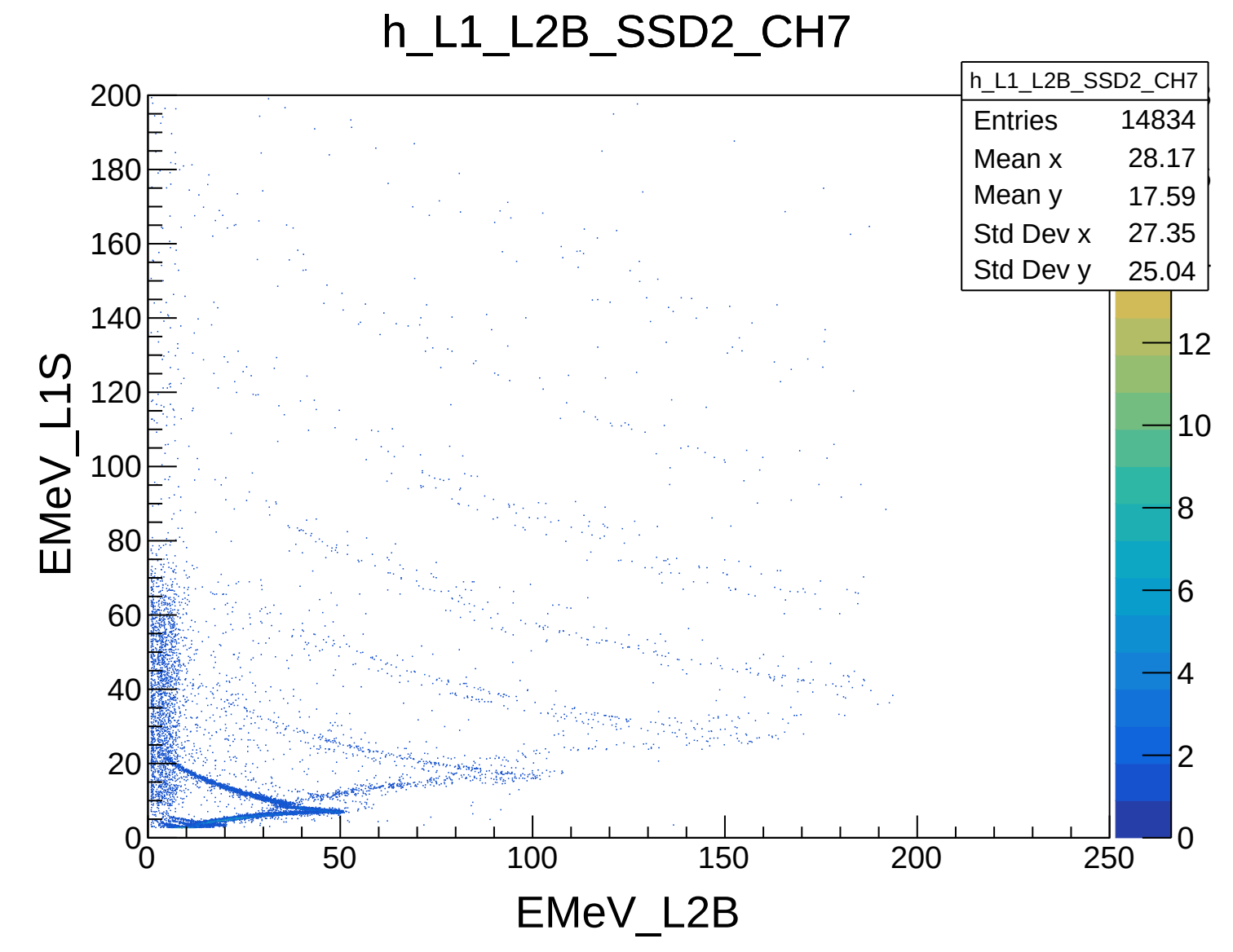

h_L1_L2B_SSD2_CH2
h_L1_L2B_SSD2_CH2
Entries 17820
Mean x 28.49
Mean y 19.65
Std Dev x 28.9
Std Dev y 27.11
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10
12
14

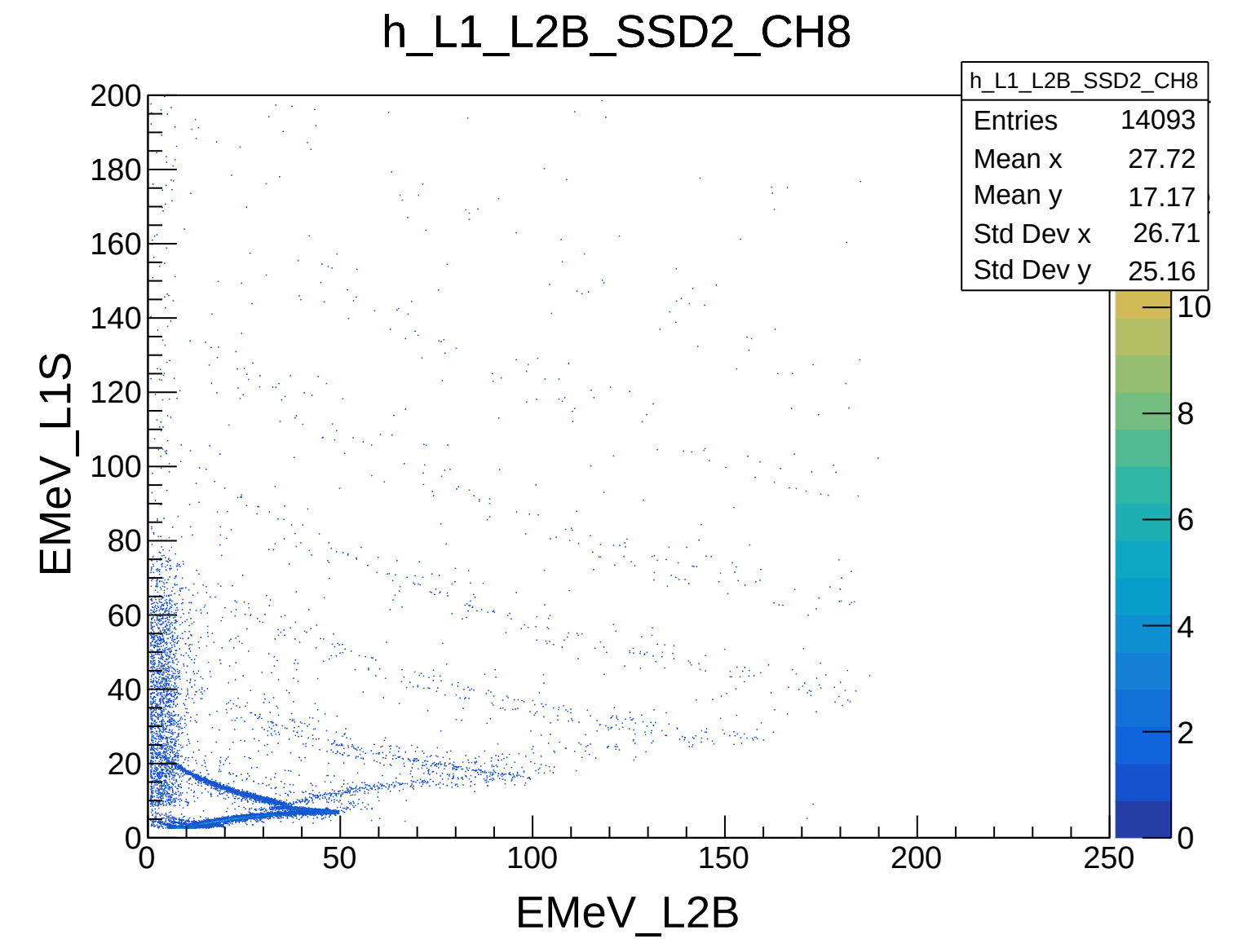

h_L1_L2B_SSD2_CH3
h_L1_L2B_SSD2_CH3
Entries 16940
Mean x 28.4
Mean y 18.68
Std Dev x 28.31
Std Dev y 26.75
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10
12
14
16

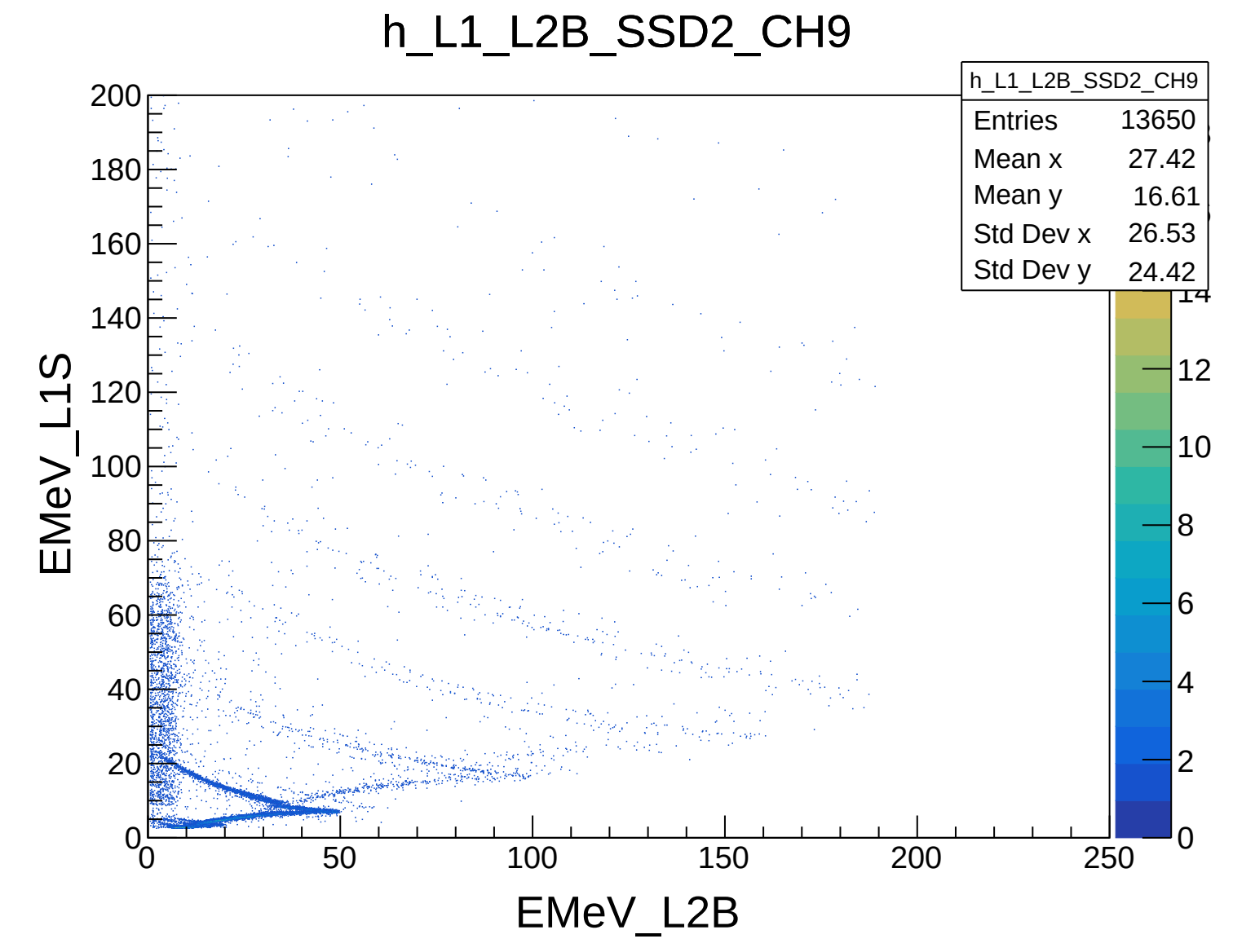

h_L1_L2B_SSD2_CH4
h_L1_L2B_SSD2_CH4
Entries 16880
Mean x 28.56
Mean y 18.19
Std Dev x 28.62
Std Dev y 26.1
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10
12
14

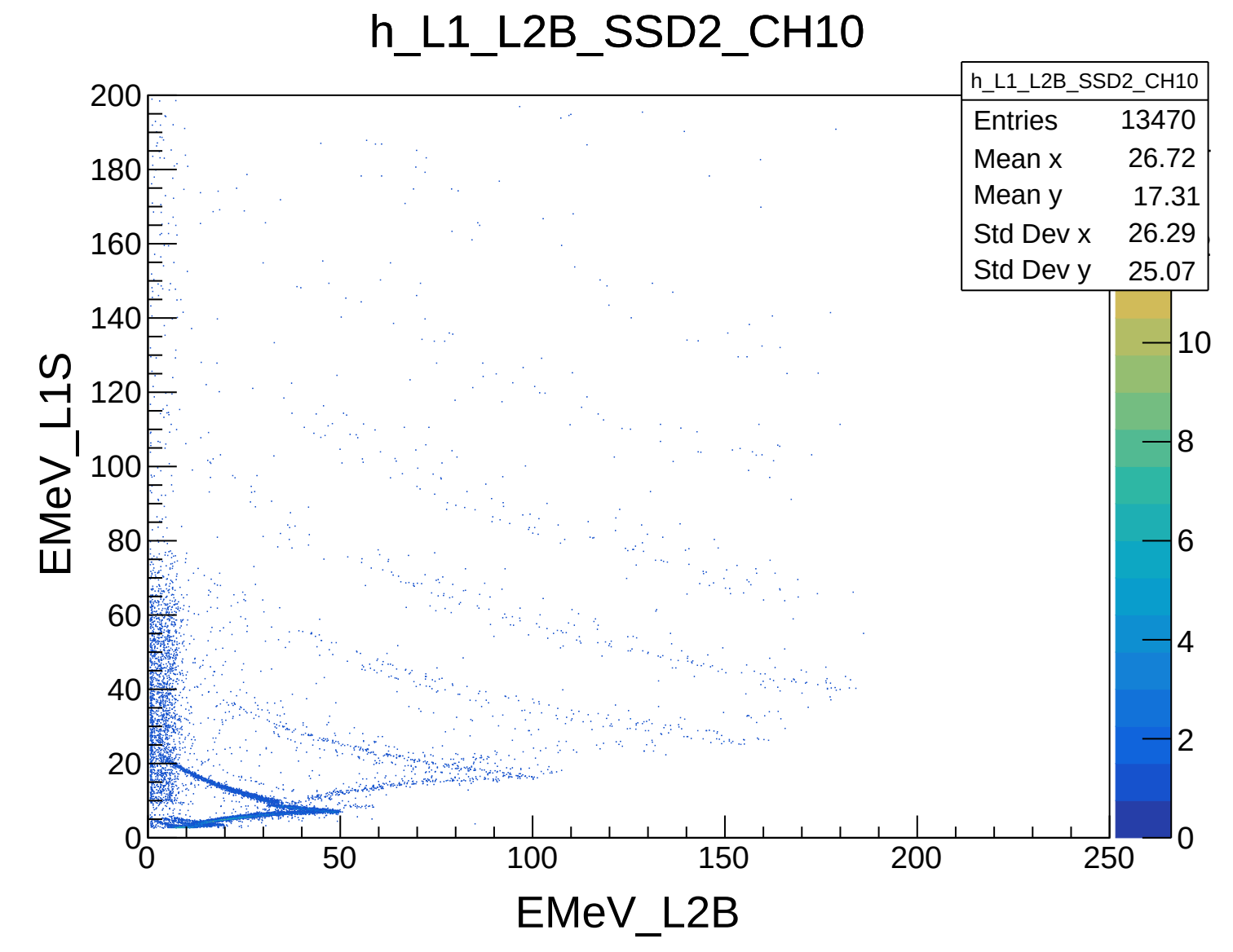

h_L1_L2B_SSD2_CH5
h_L1_L2B_SSD2_CH5
Entries 15872
Mean x 28.71
Mean y 17.56
Std Dev x 28.75
Std Dev y 25.55
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10
12
14

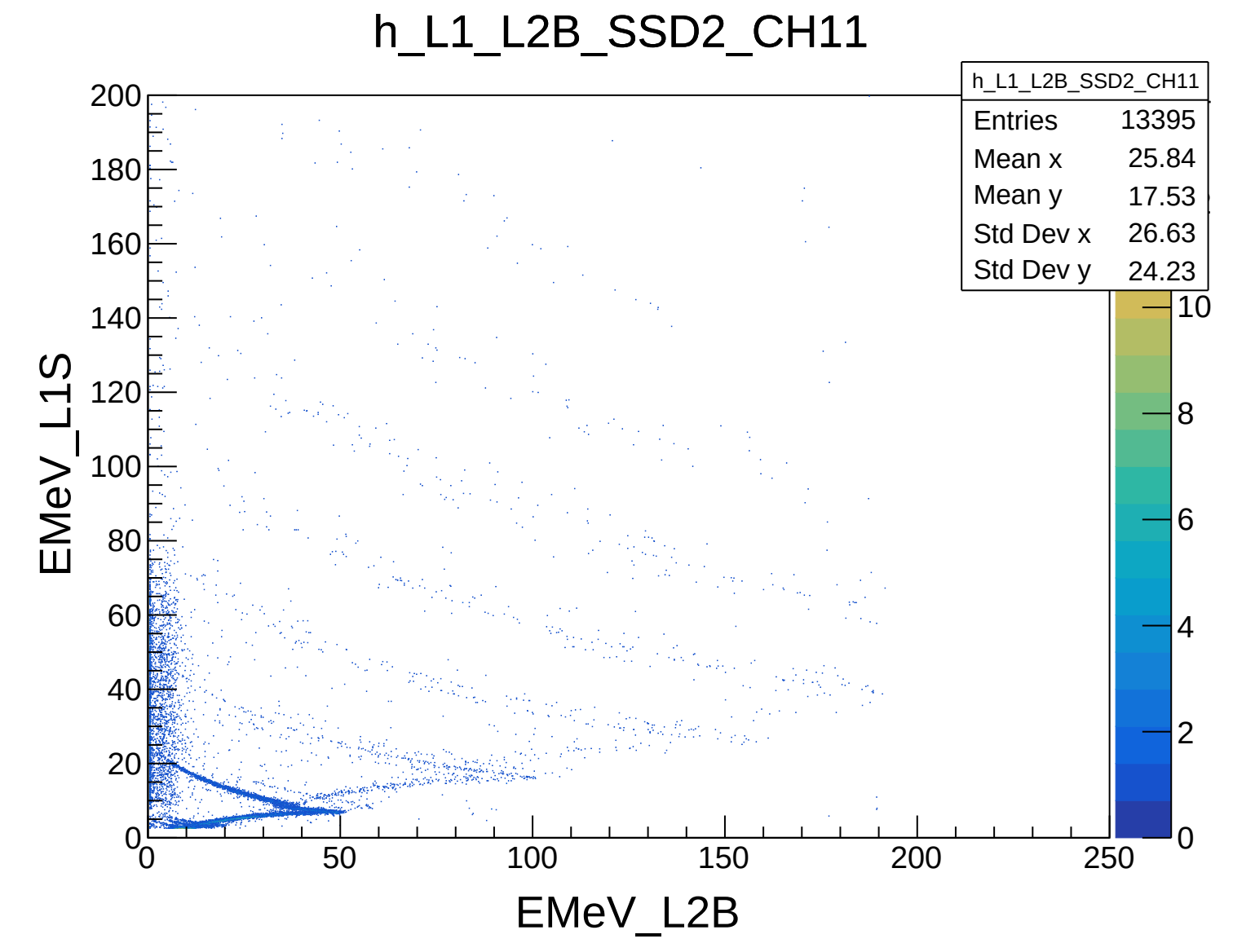

h_L1_L2B_SSD2_CH6
h_L1_L2B_SSD2_CH6
Entries 15452
Mean x 27.56
Mean y 17.94
Std Dev x 27.2
Std Dev y 25.4
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10
12

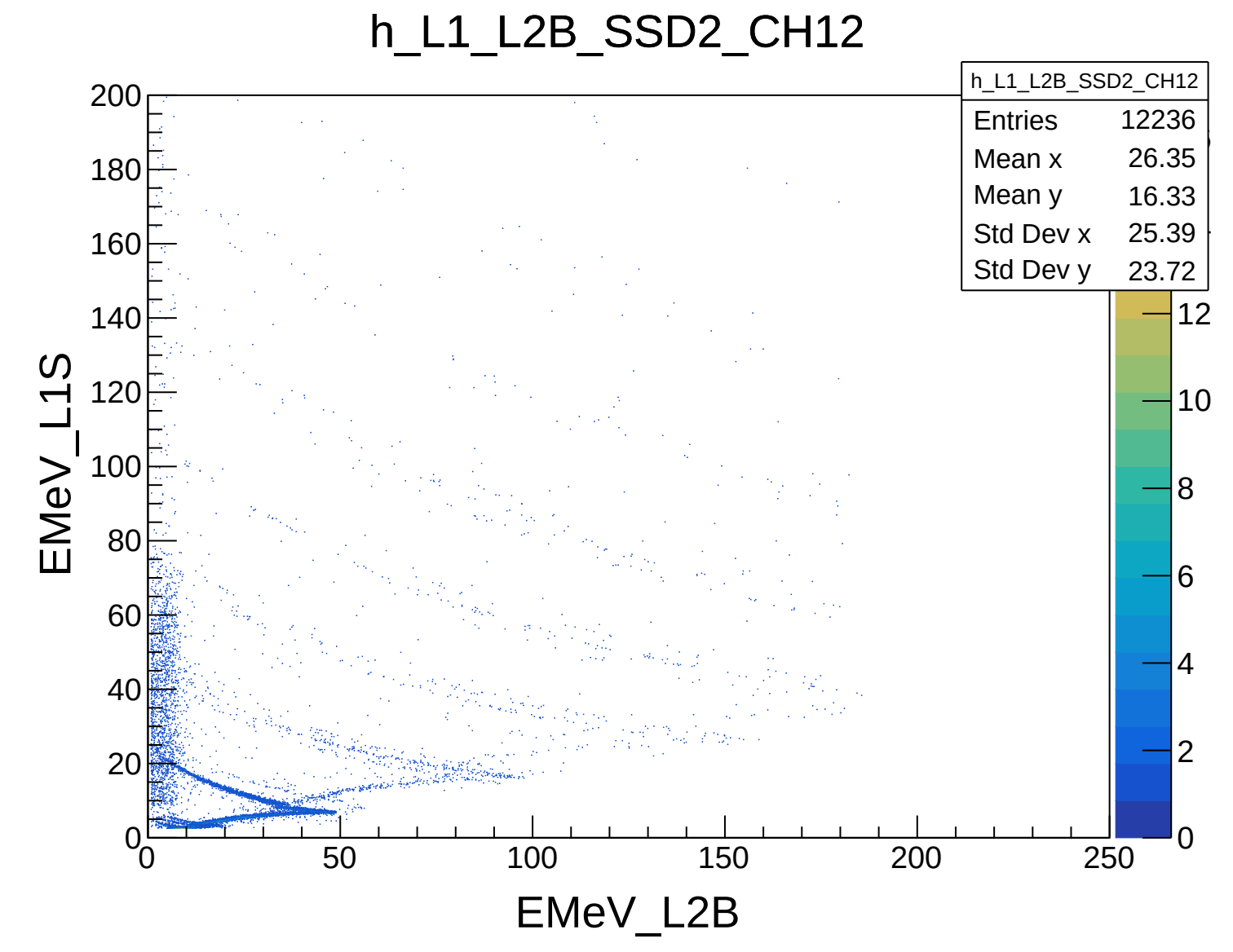

h_L1_L2B_SSD2_CH7
h_L1_L2B_SSD2_CH7
Entries 14834
Mean x 28.17
Mean y 17.59
Std Dev x 27.35
Std Dev y 25.04
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10
12

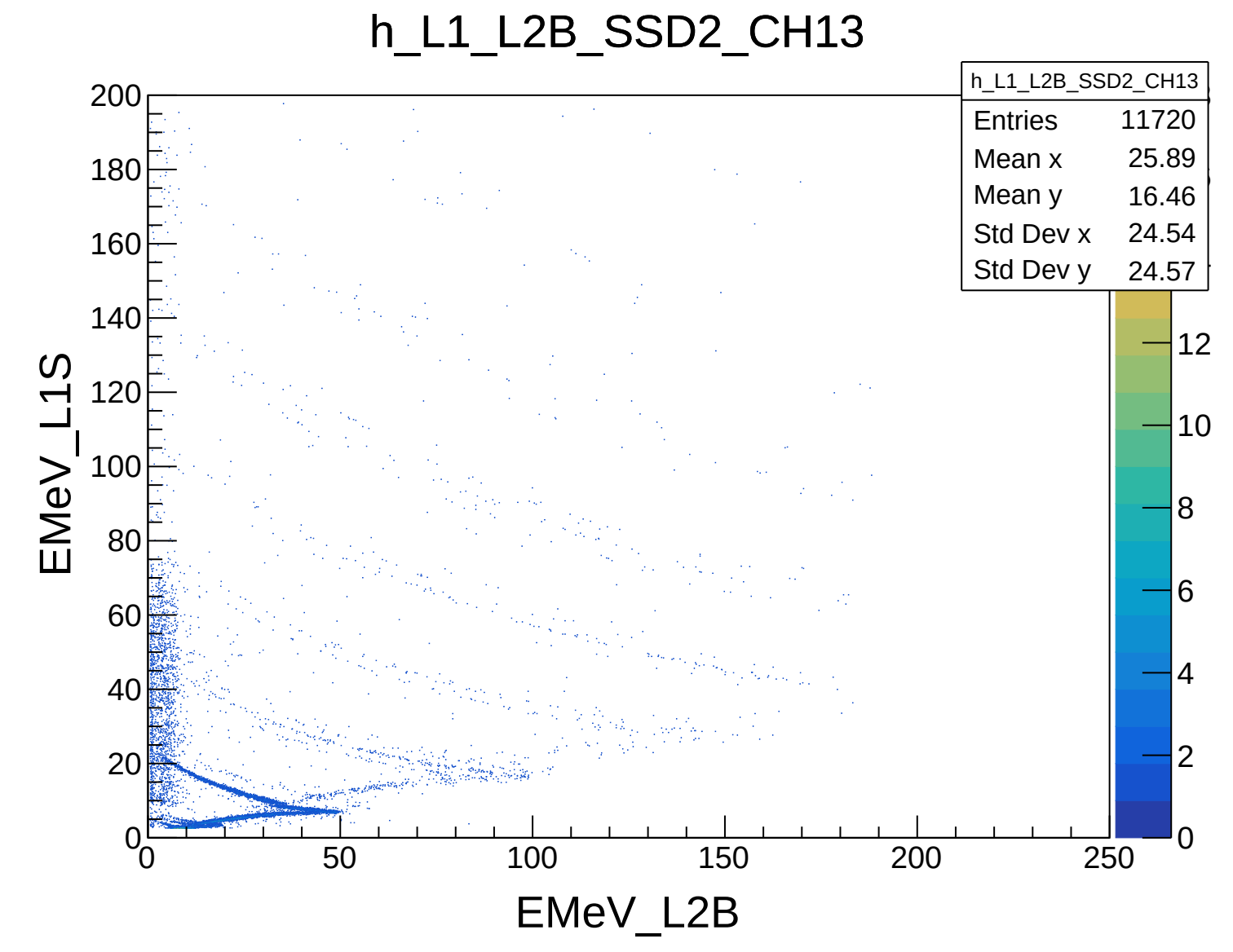

h_L1_L2B_SSD2_CH8
h_L1_L2B_SSD2_CH8
Entries 14093
Mean x 27.72
Mean y 17.17
Std Dev x 26.71
Std Dev y 25.16
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10

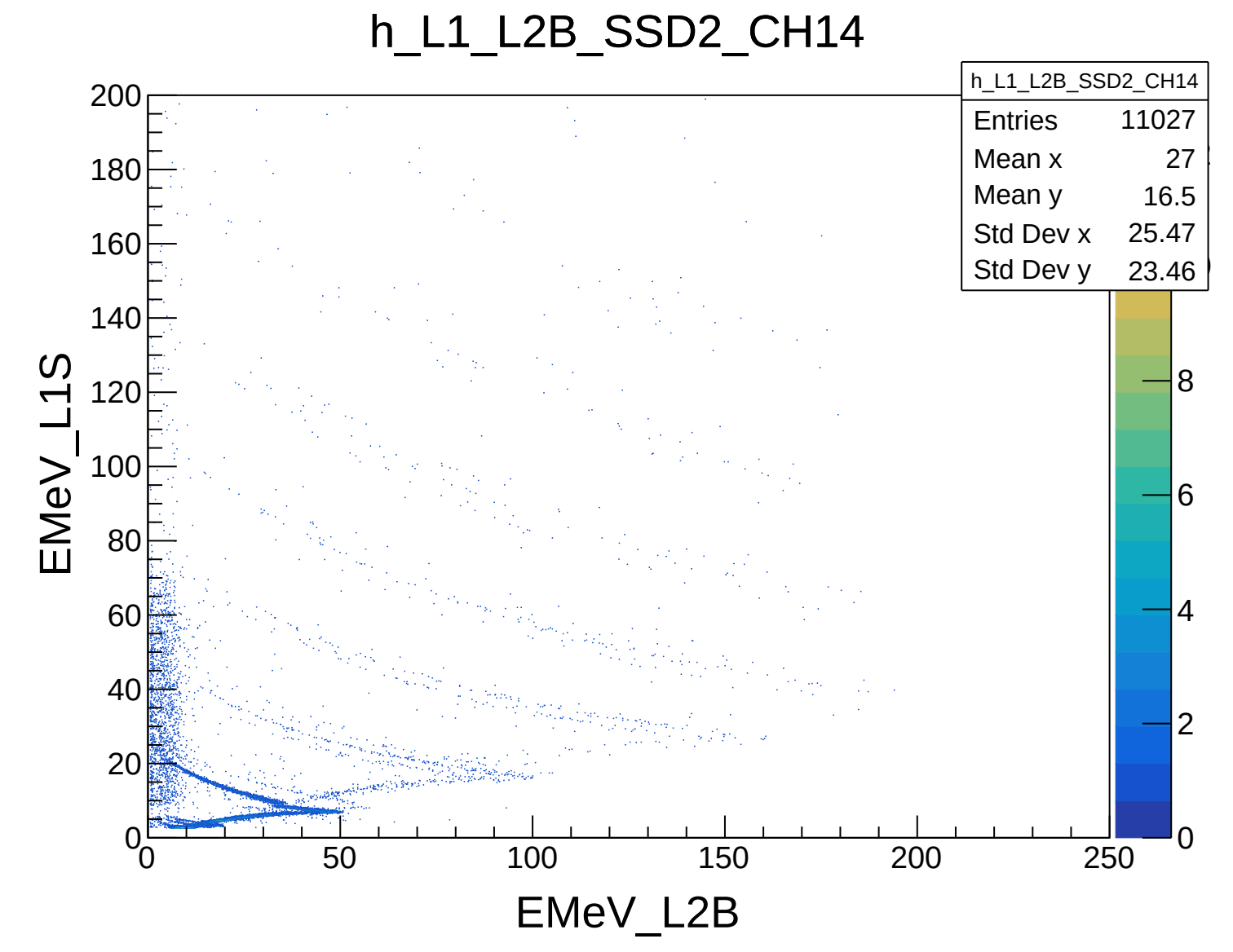

h_L1_L2B_SSD2_CH9
h_L1_L2B_SSD2_CH9
Entries 13650
Mean x 27.42
Mean y 16.61
Std Dev x 26.53
Std Dev y 24.42
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10
12
14

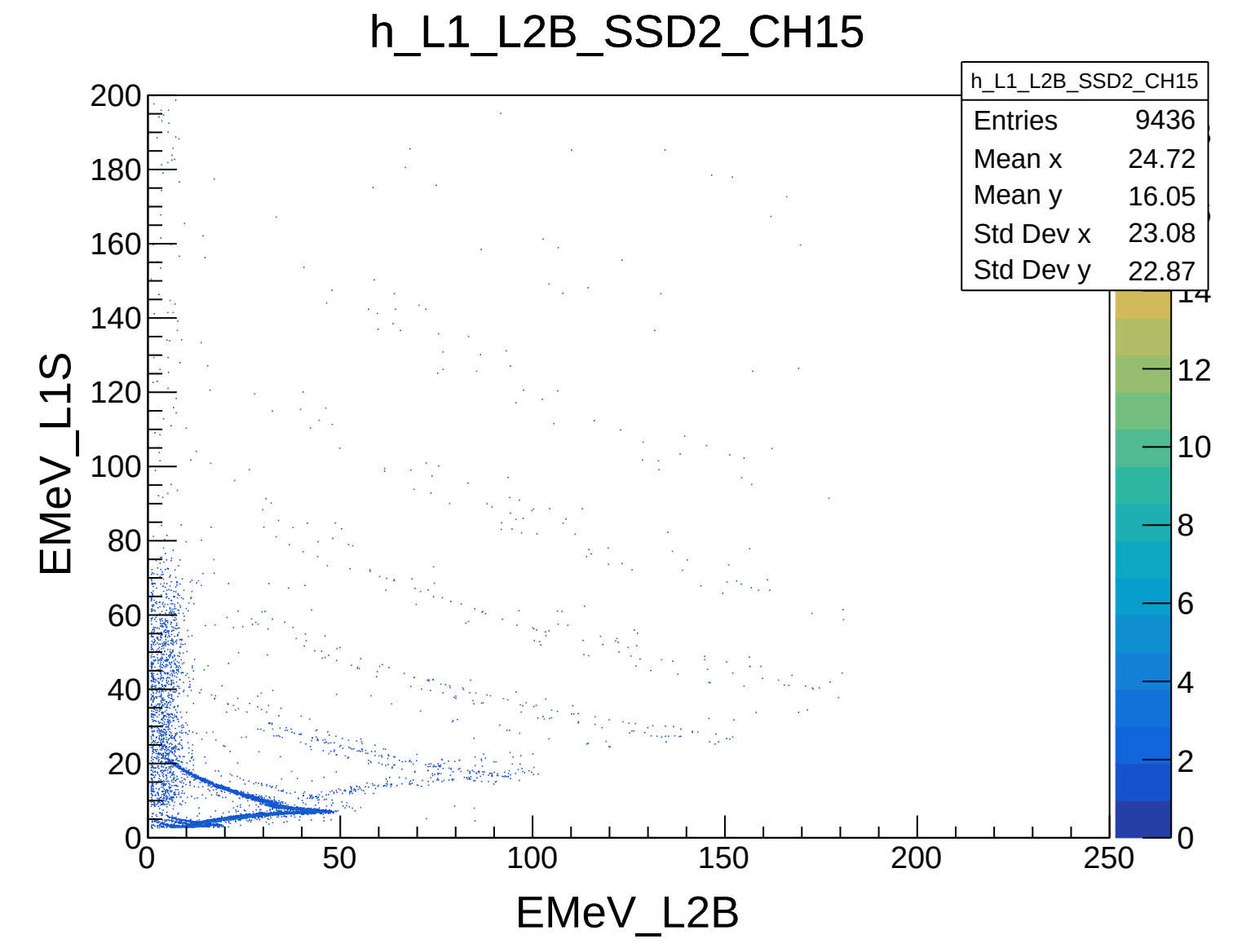

h_L1_L2B_SSD2_CH10
h_L1_L2B_SSD2_CH10
Entries 13470
Mean x 26.72
Mean y 17.31
Std Dev x 26.29
Std Dev y 25.07
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10

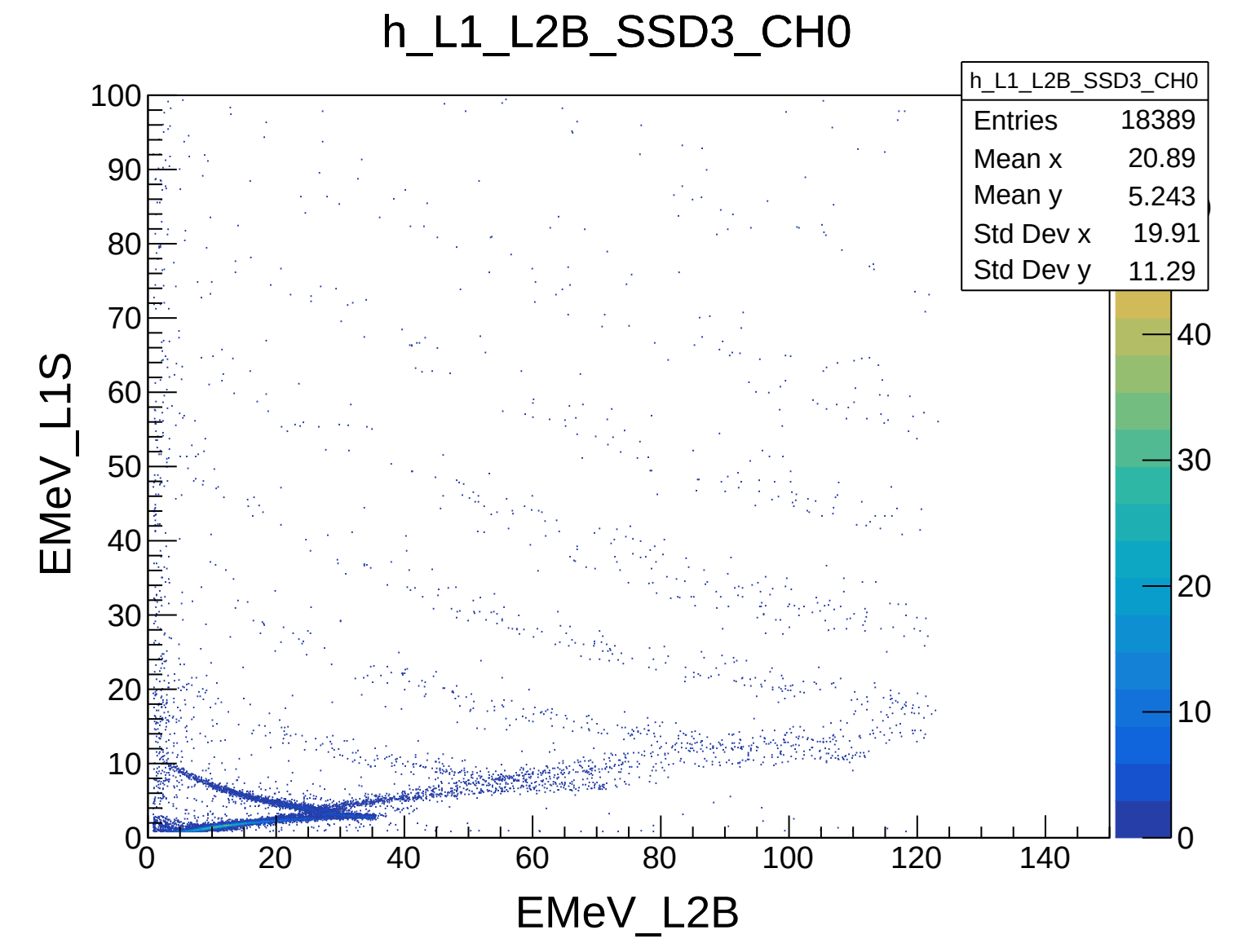

h_L1_L2B_SSD2_CH11
h_L1_L2B_SSD2_CH11
Entries 13395
Mean x 25.84
Mean y 17.53
Std Dev x 26.63
Std Dev y 24.23
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10

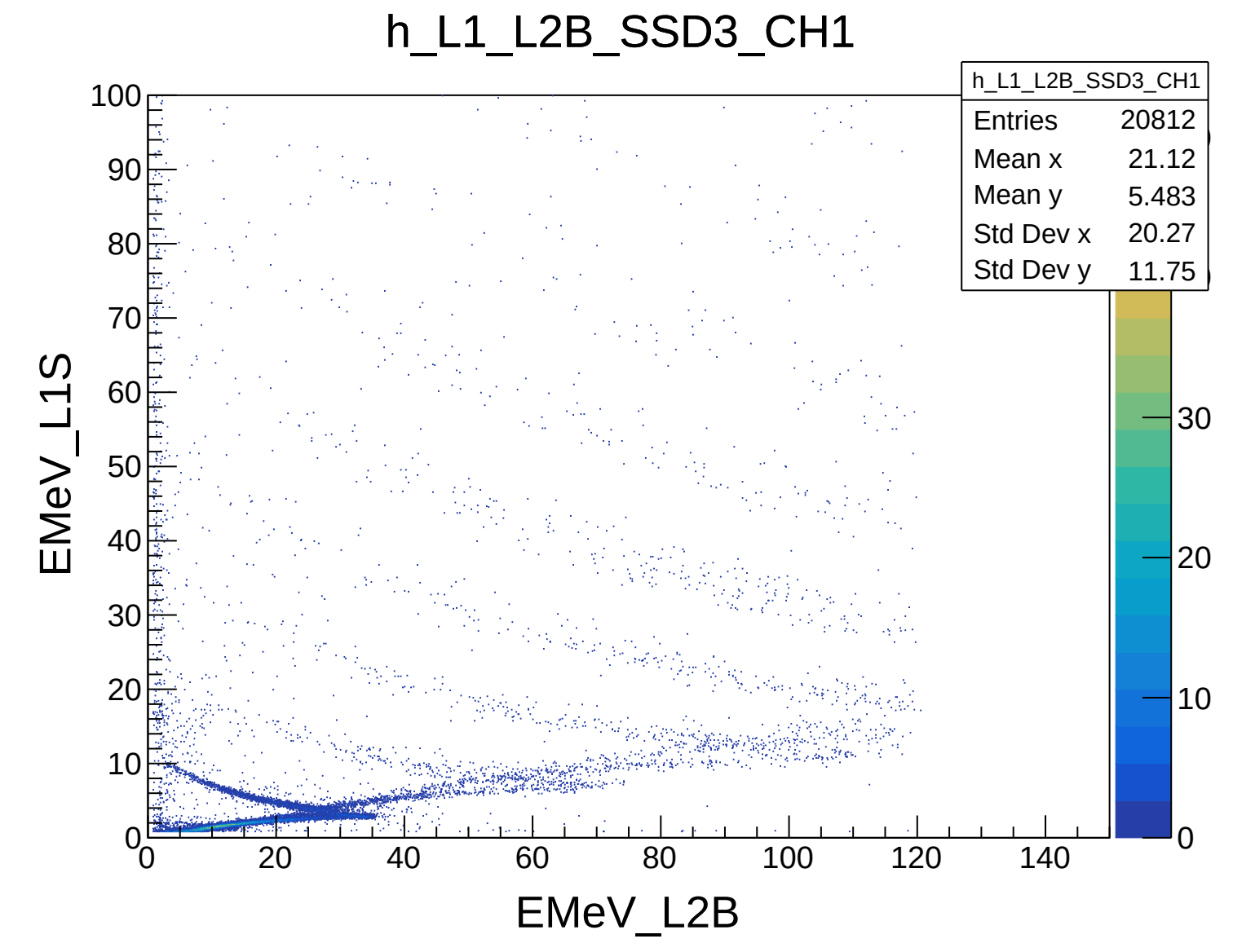

h_L1_L2B_SSD2_CH12
h_L1_L2B_SSD2_CH12
Entries 12236
Mean x 26.35
Mean y 16.33
Std Dev x 25.39
Std Dev y 23.72
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10
12

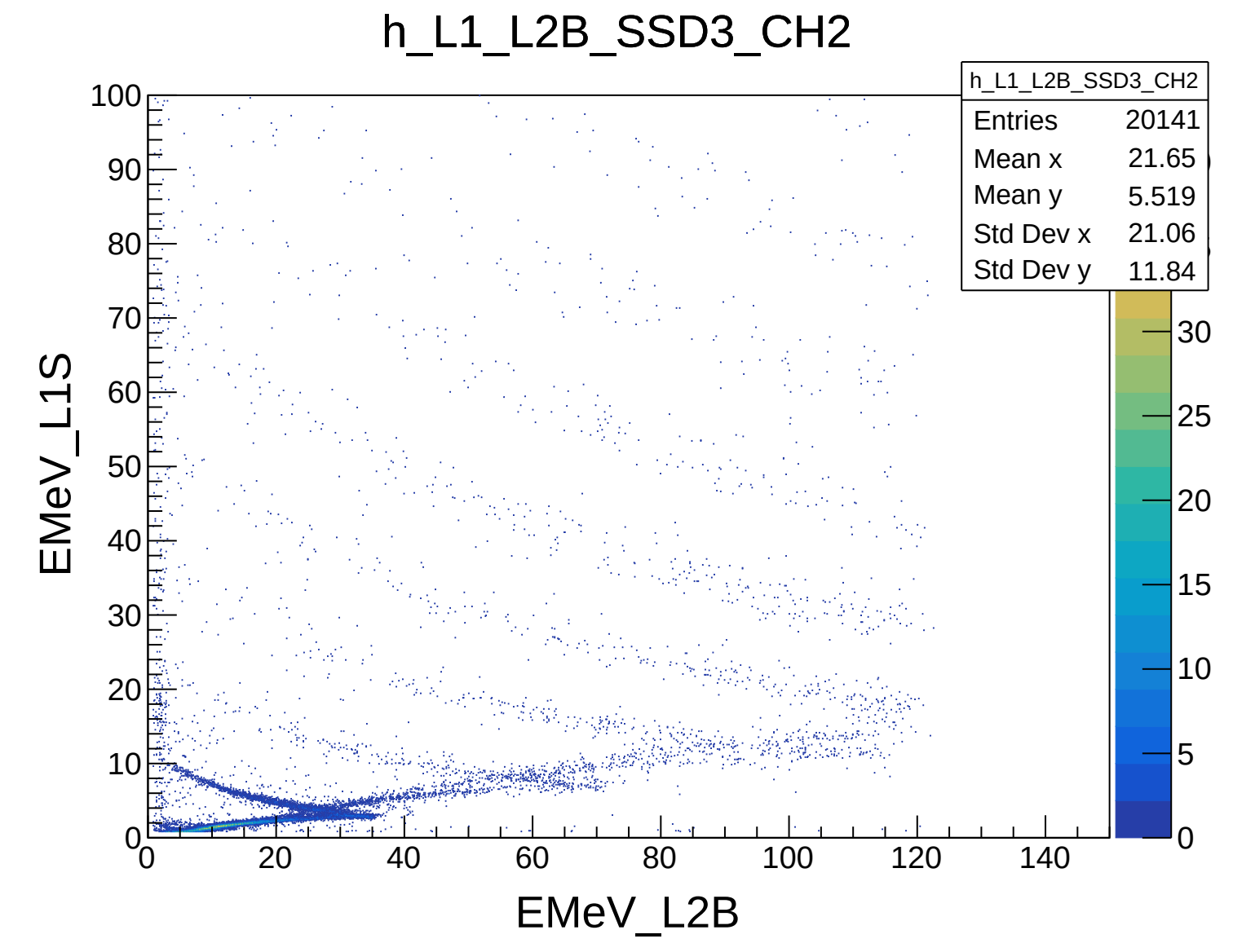

h_L1_L2B_SSD2_CH13
h_L1_L2B_SSD2_CH13
Entries 11720
Mean x 25.89
Mean y 16.46
Std Dev x 24.54
Std Dev y 24.57
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10
12

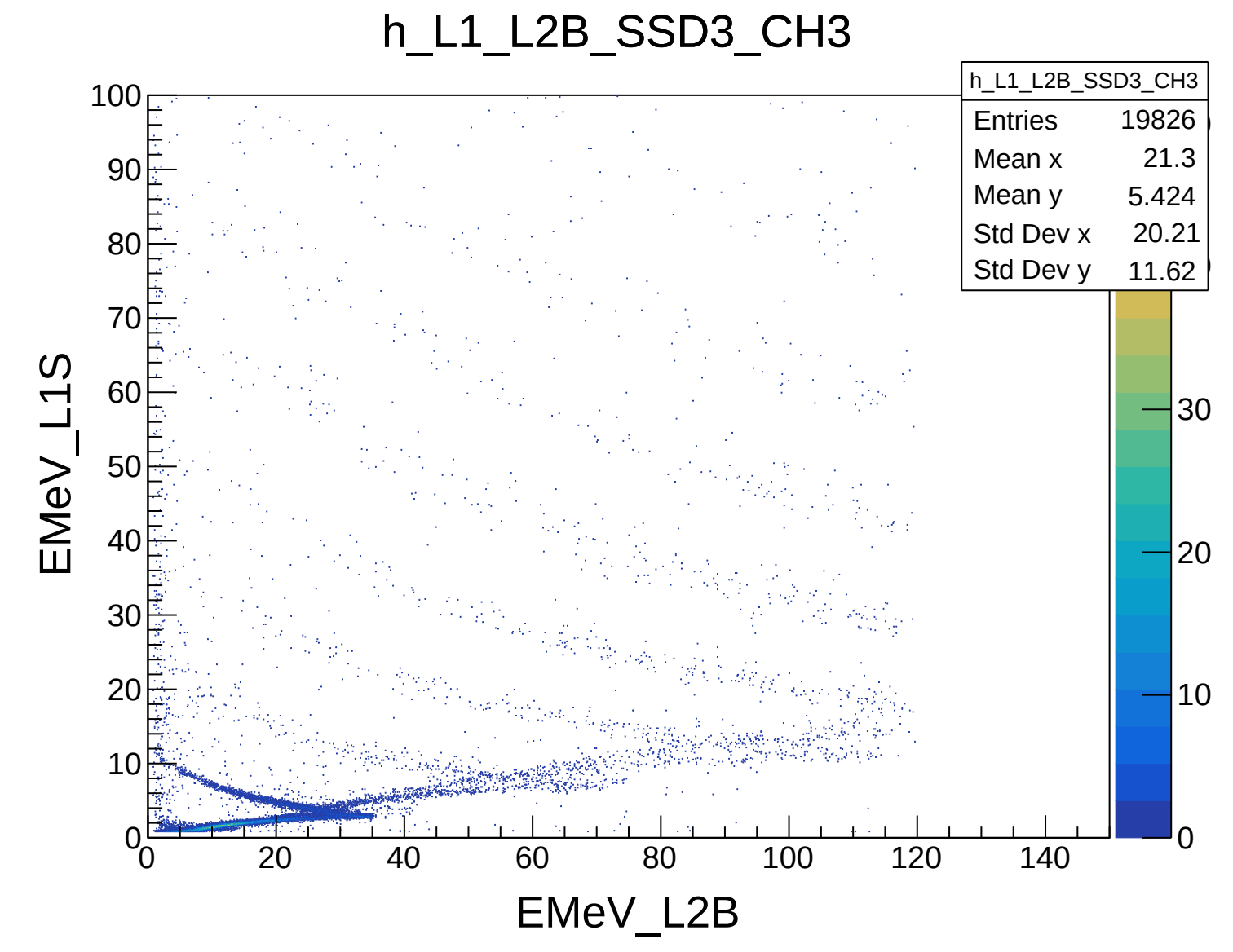

h_L1_L2B_SSD2_CH14
h_L1_L2B_SSD2_CH14
Entries 11027
Mean x 27
Mean y 16.5
Std Dev x 25.47
Std Dev y 23.46
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8

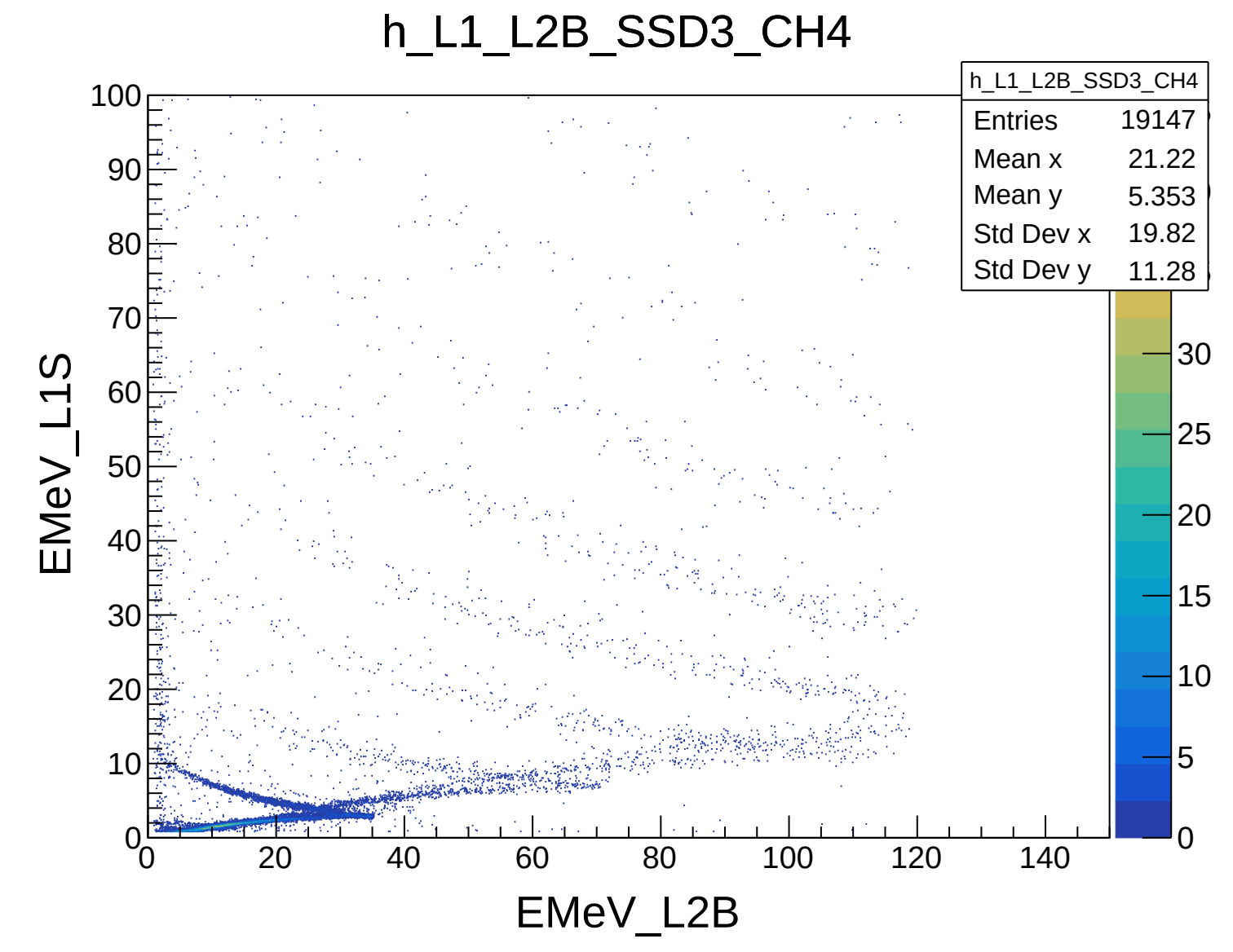

h_L1_L2B_SSD2_CH15
h_L1_L2B_SSD2_CH15
Entries 9436
Mean x 24.72
Mean y 16.05
Std Dev x 23.08
Std Dev y 22.87
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10
12
14

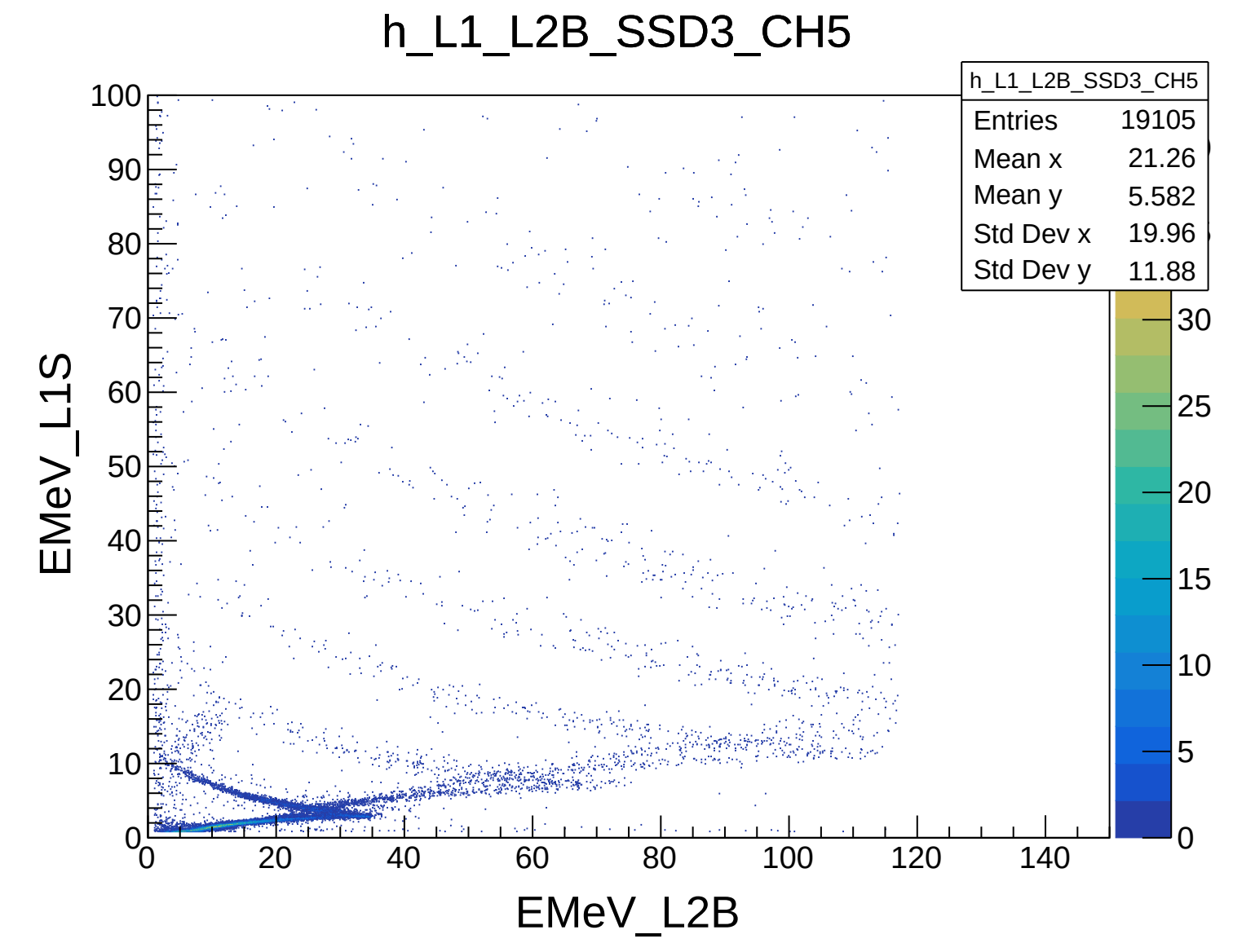

h_L1_L2B_SSD3_CH0
h_L1_L2B_SSD3_CH0
Entries 18389
Mean x 20.89
Mean y 5.243
Std Dev x 19.91
Std Dev y 11.29
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30
40

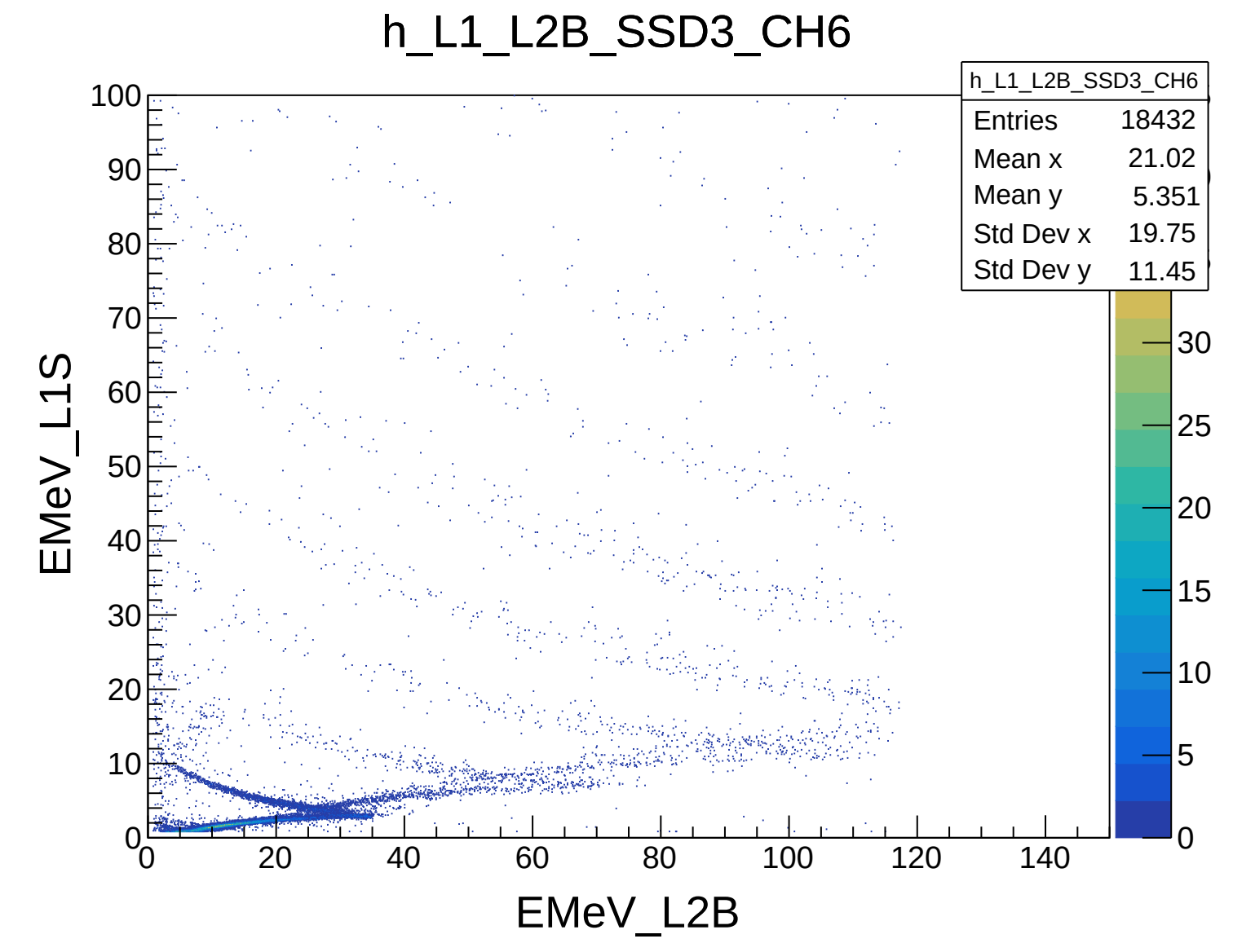

h_L1_L2B_SSD3_CH1
h_L1_L2B_SSD3_CH1
Entries 20812
Mean x 21.12
Mean y 5.483
Std Dev x 20.27
Std Dev y 11.75
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30

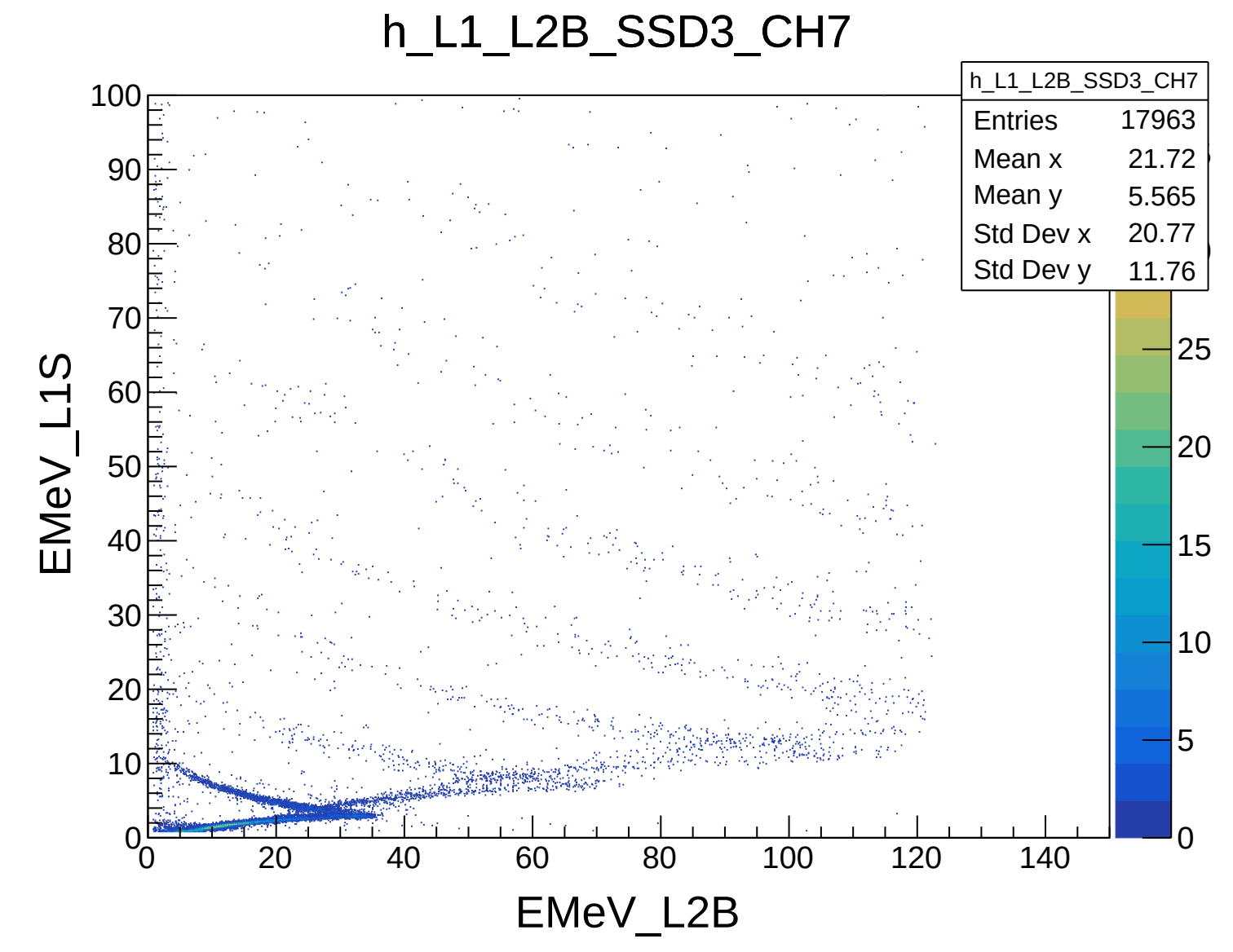

h_L1_L2B_SSD3_CH2
h_L1_L2B_SSD3_CH2
Entries 20141
Mean x 21.65
Mean y 5.519
Std Dev x 21.06
Std Dev y 11.84
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25
30

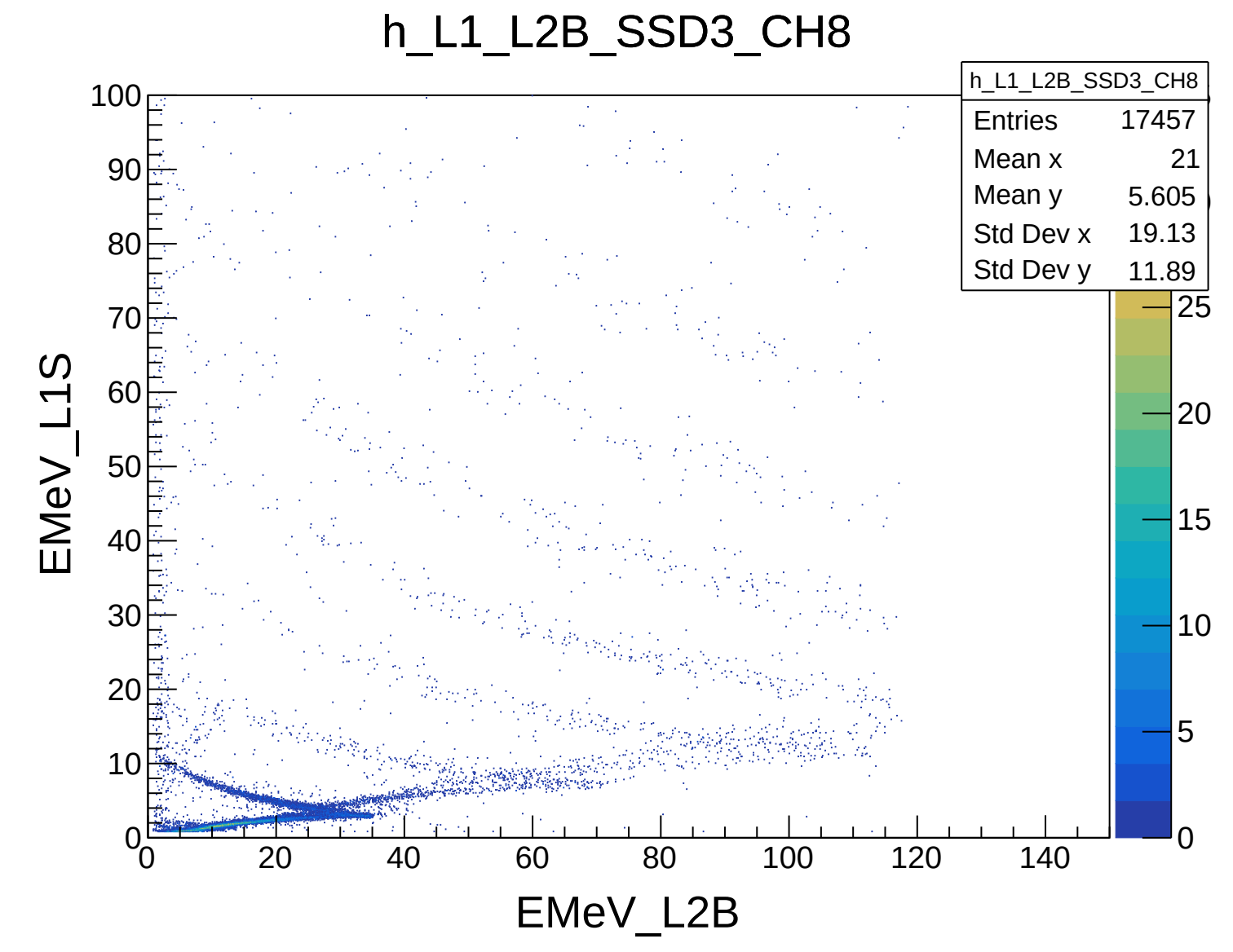

h_L1_L2B_SSD3_CH3
h_L1_L2B_SSD3_CH3
Entries 19826
Mean x 21.3
Mean y 5.424
Std Dev x 20.21
Std Dev y 11.62
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30

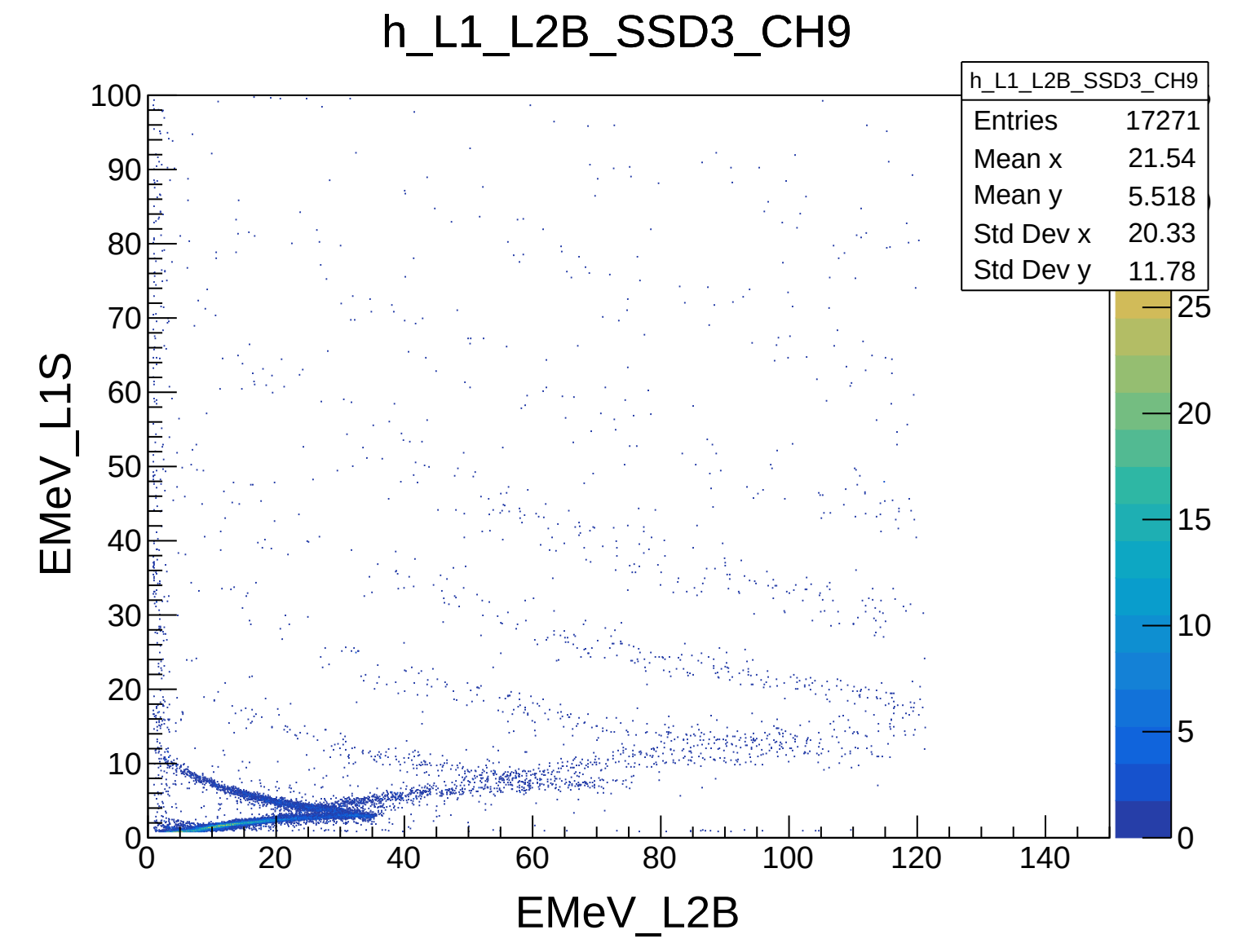

h_L1_L2B_SSD3_CH4
h_L1_L2B_SSD3_CH4
Entries 19147
Mean x 21.22
Mean y 5.353
Std Dev x 19.82
Std Dev y 11.28
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25
30

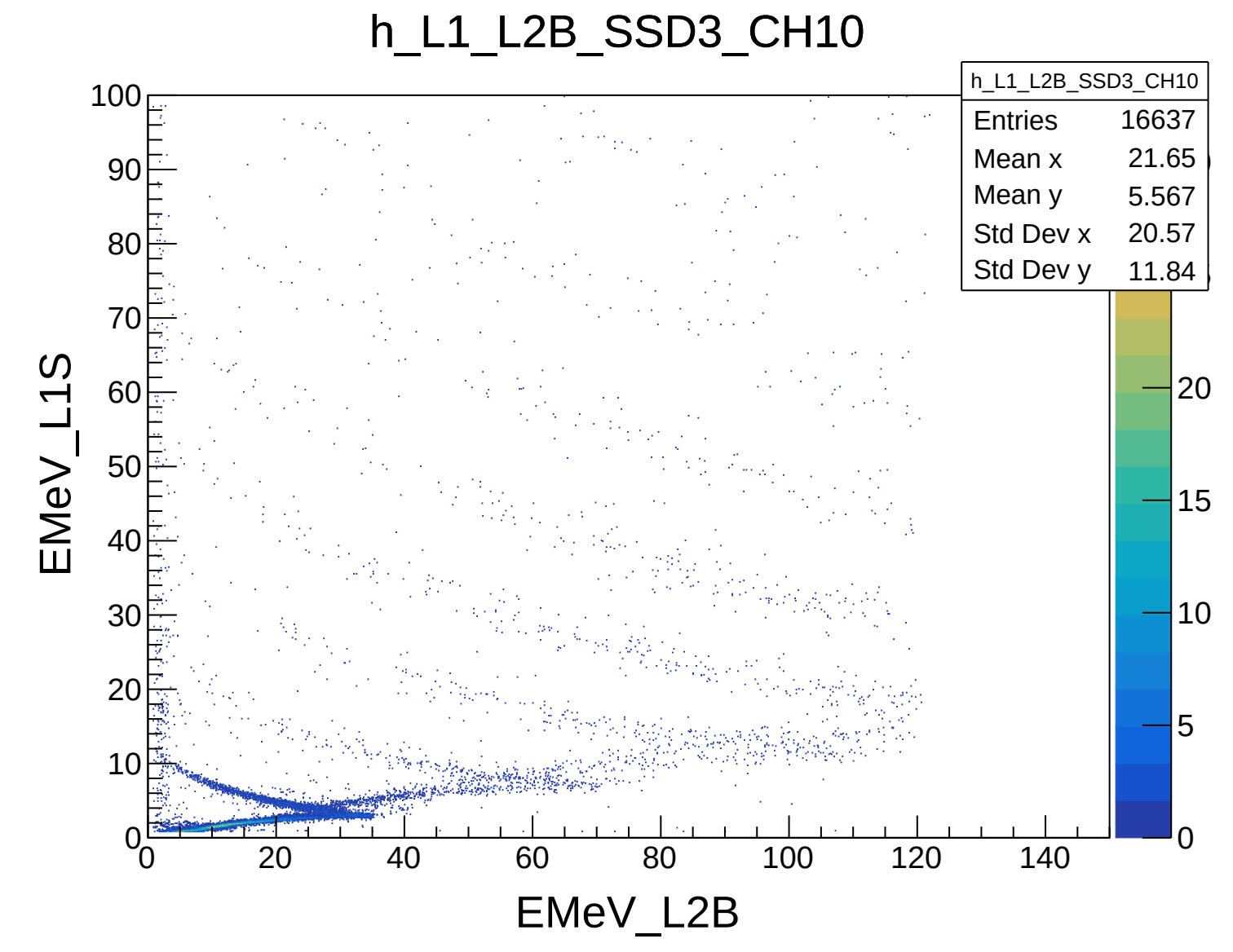

h_L1_L2B_SSD3_CH5
h_L1_L2B_SSD3_CH5
Entries 19105
Mean x 21.26
Mean y 5.582
Std Dev x 19.96
Std Dev y 11.88
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25
30

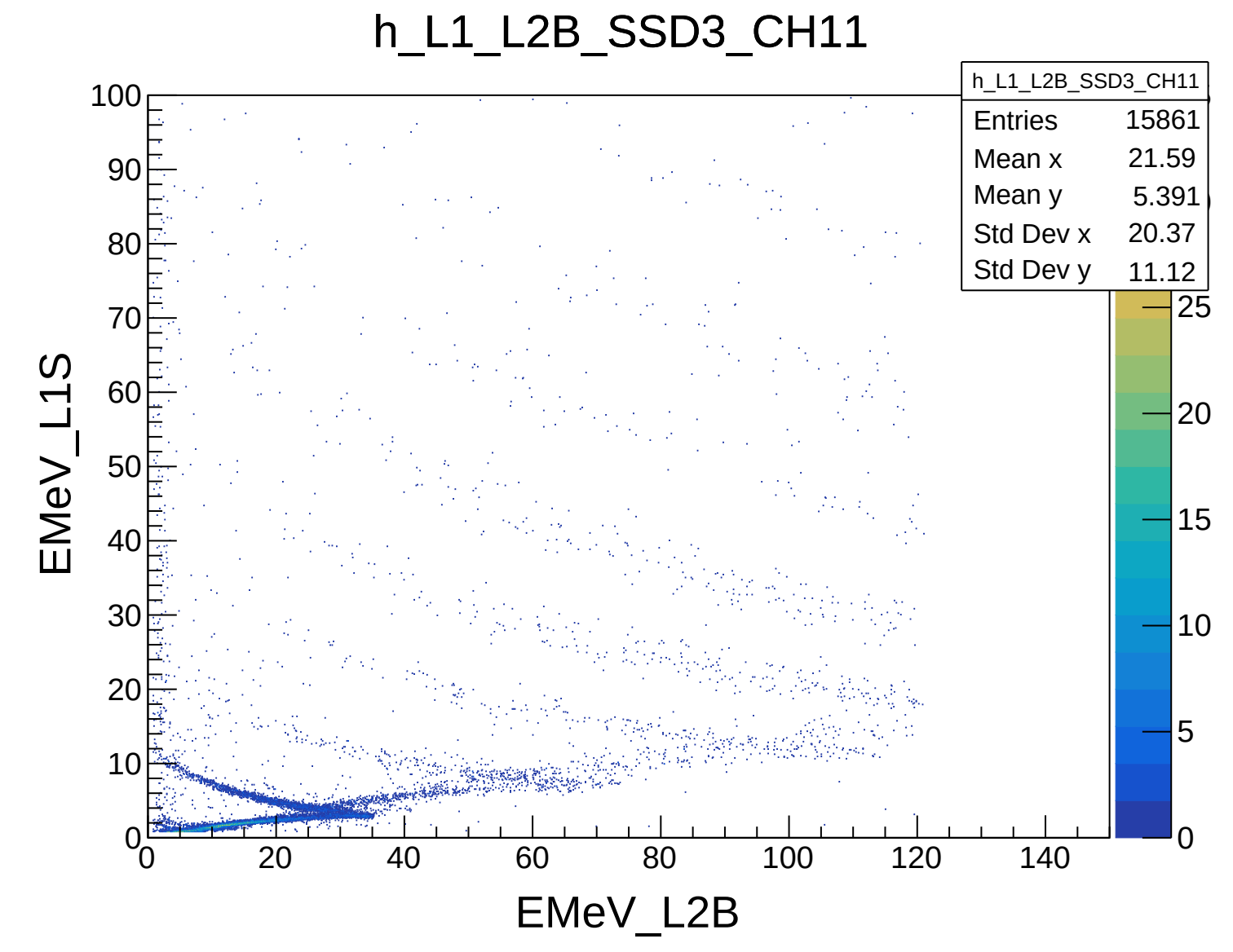

h_L1_L2B_SSD3_CH6
h_L1_L2B_SSD3_CH6
Entries 18432
Mean x 21.02
Mean y 5.351
Std Dev x 19.75
Std Dev y 11.45
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25
30

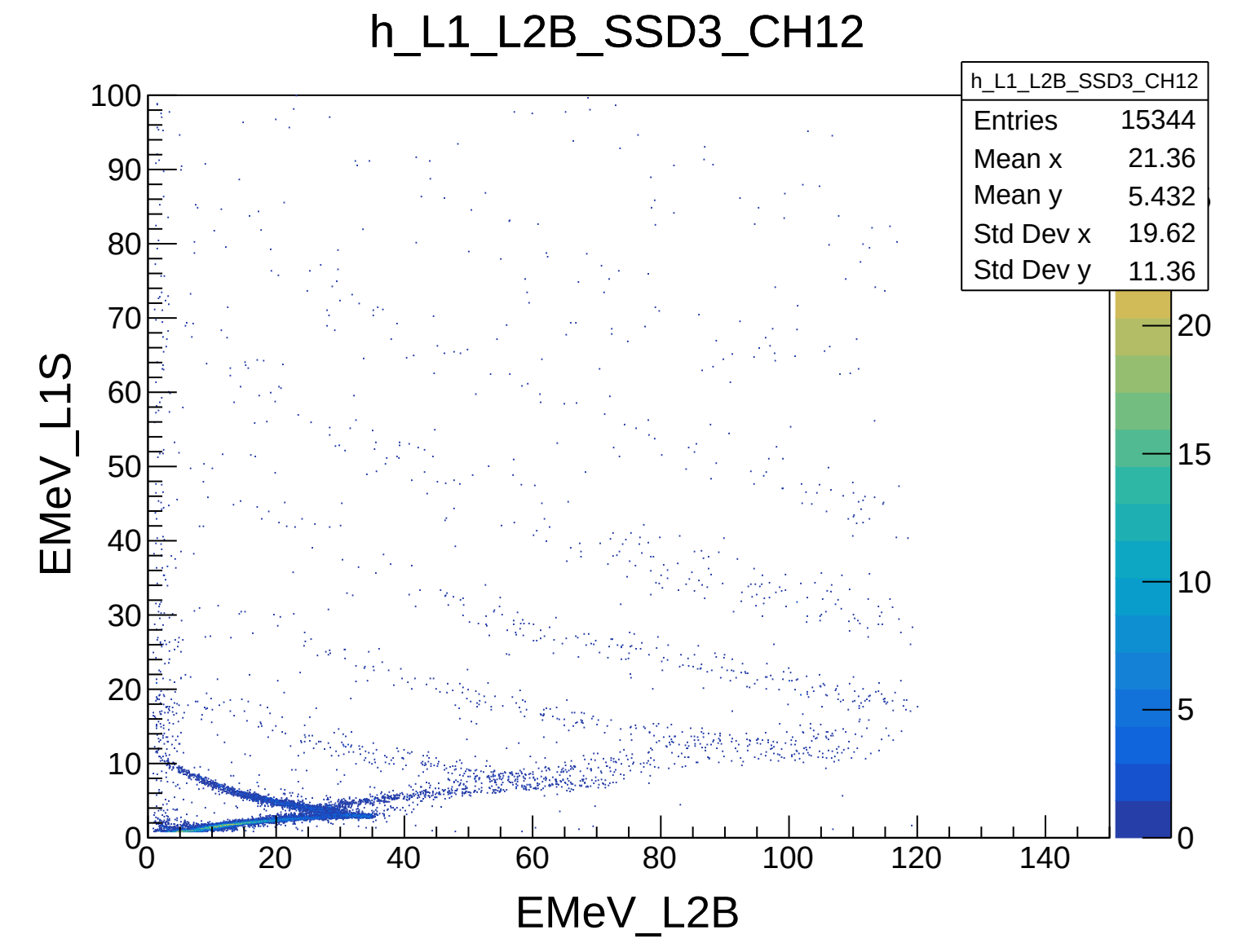

h_L1_L2B_SSD3_CH7
h_L1_L2B_SSD3_CH7
Entries 17963
Mean x 21.72
Mean y 5.565
Std Dev x 20.77
Std Dev y 11.76
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25

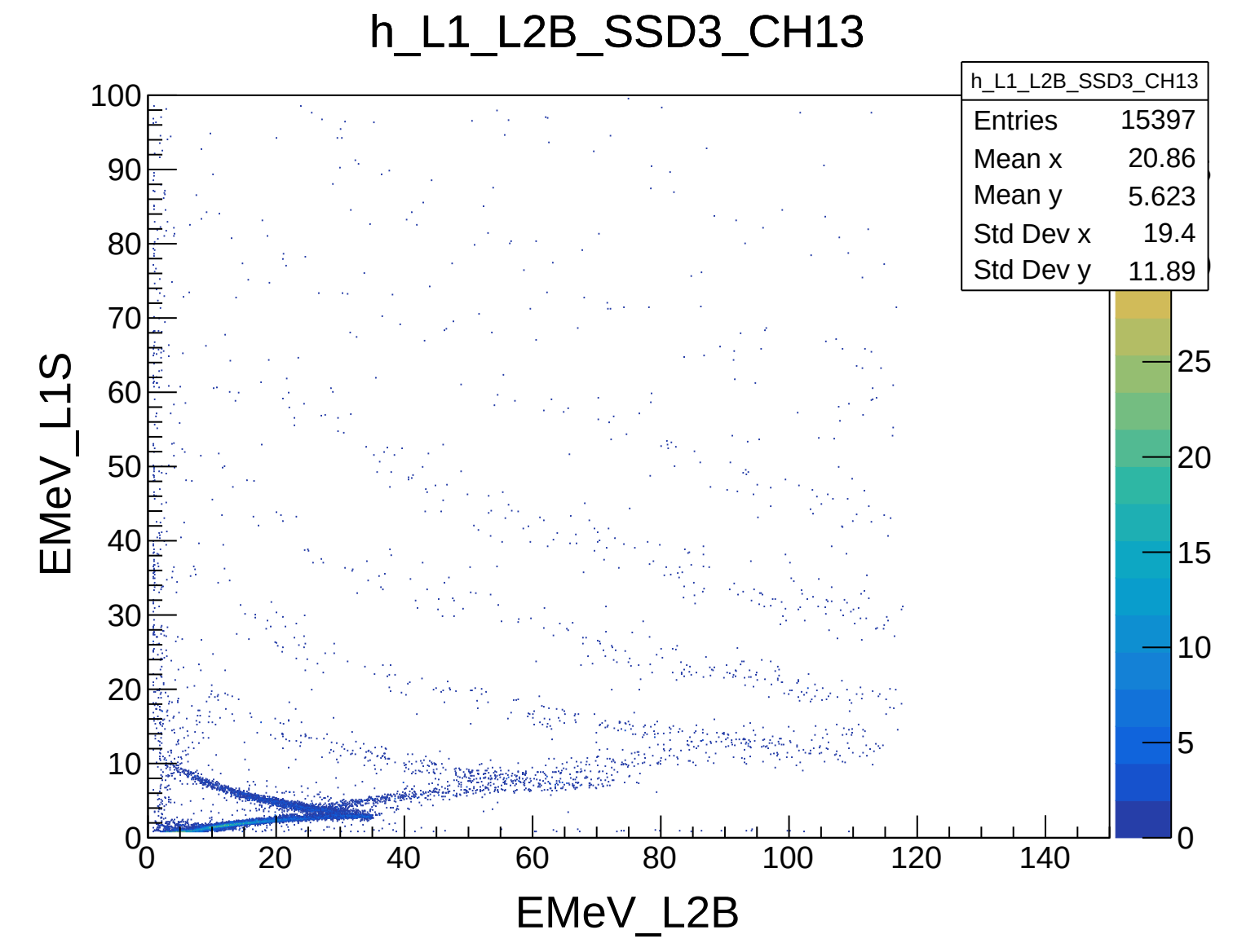

h_L1_L2B_SSD3_CH8
h_L1_L2B_SSD3_CH8
Entries 17457
Mean x 21
Mean y 5.605
Std Dev x 19.13
Std Dev y 11.89
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25

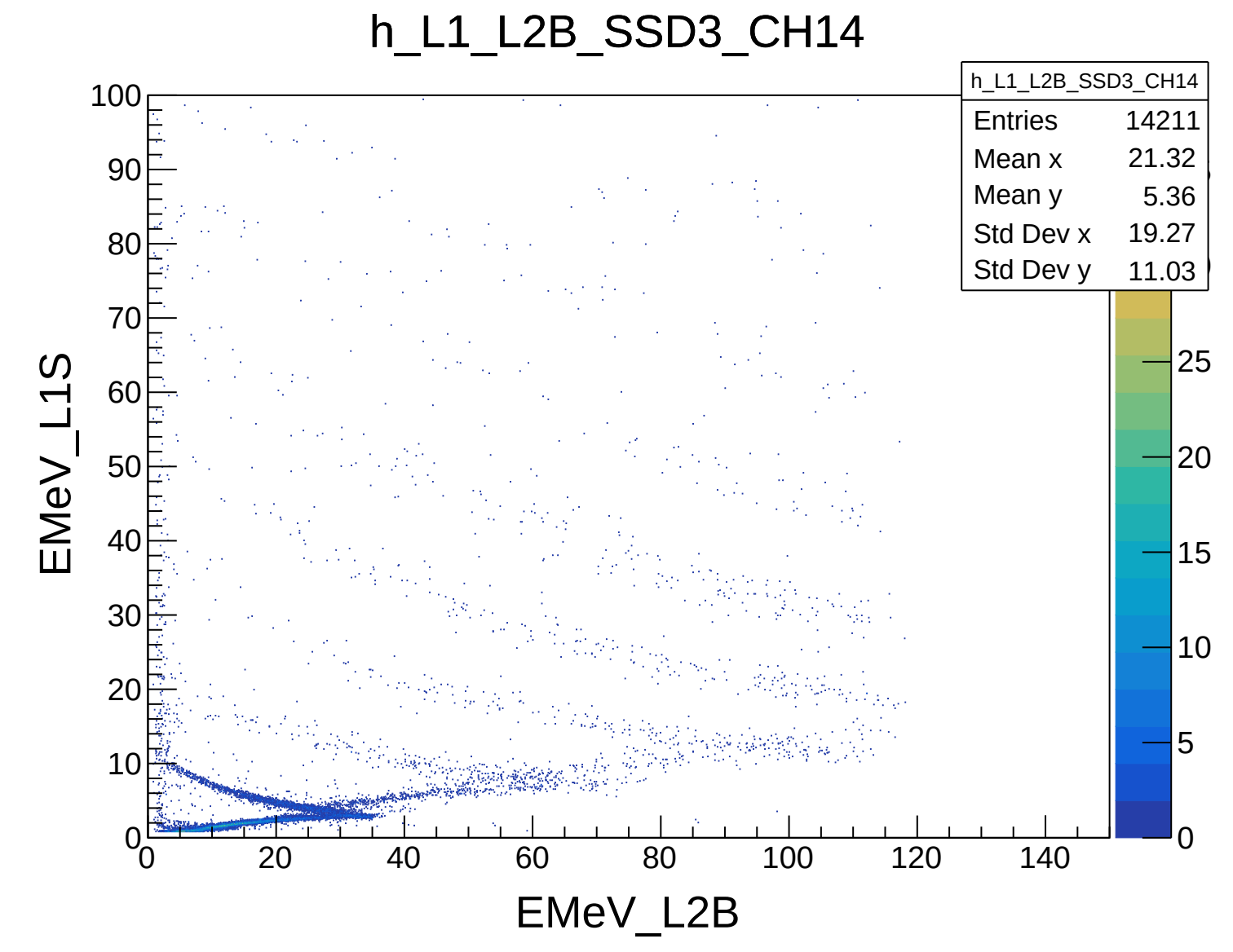

h_L1_L2B_SSD3_CH9
h_L1_L2B_SSD3_CH9
Entries 17271
Mean x 21.54
Mean y 5.518
Std Dev x 20.33
Std Dev y 11.78
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25

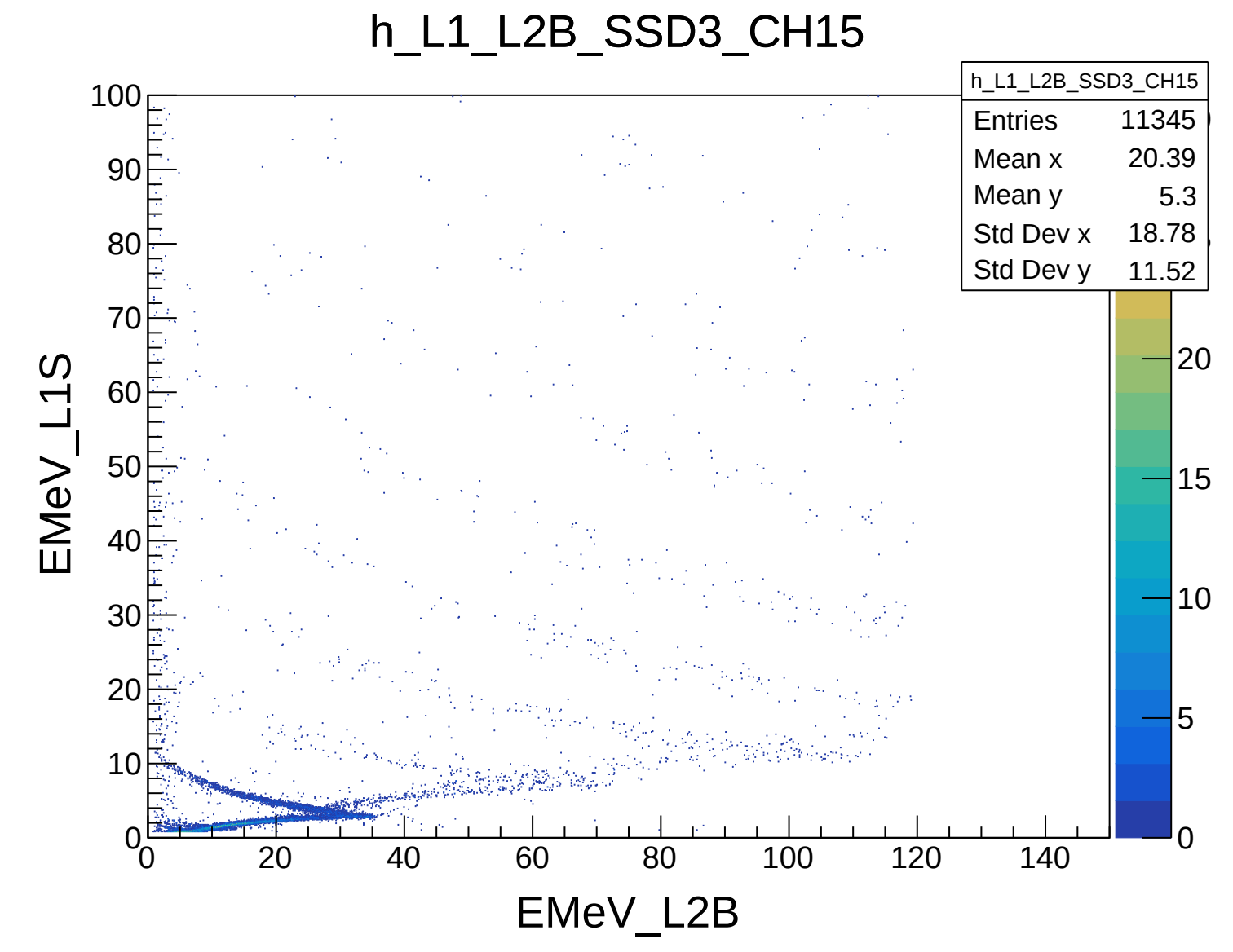

h_L1_L2B_SSD3_CH10
h_L1_L2B_SSD3_CH10
Entries 16637
Mean x 21.65
Mean y 5.567
Std Dev x 20.57
Std Dev y 11.84
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20

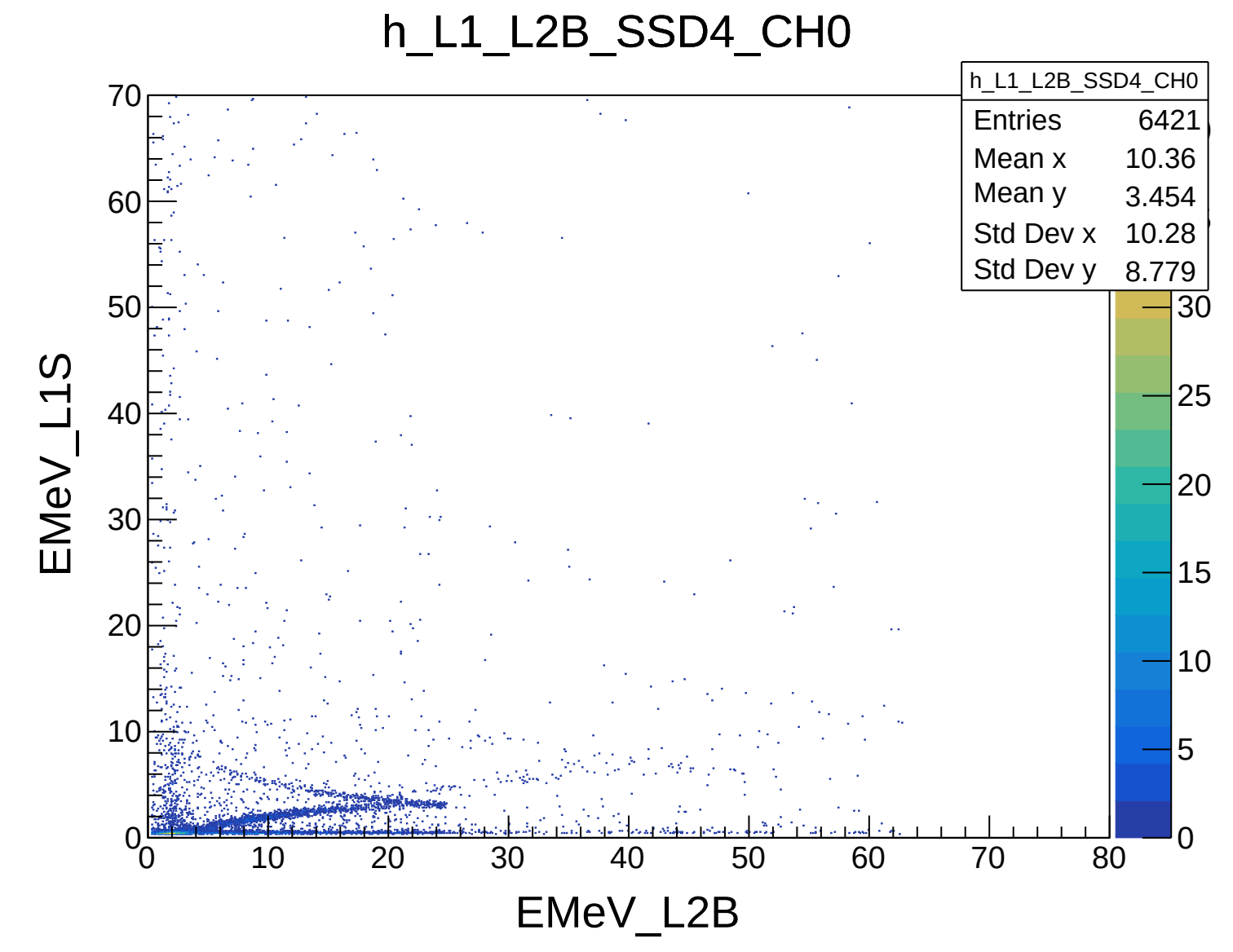

h_L1_L2B_SSD3_CH11
h_L1_L2B_SSD3_CH11
Entries 15861
Mean x 21.59
Mean y 5.391
Std Dev x 20.37
Std Dev y 11.12
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25

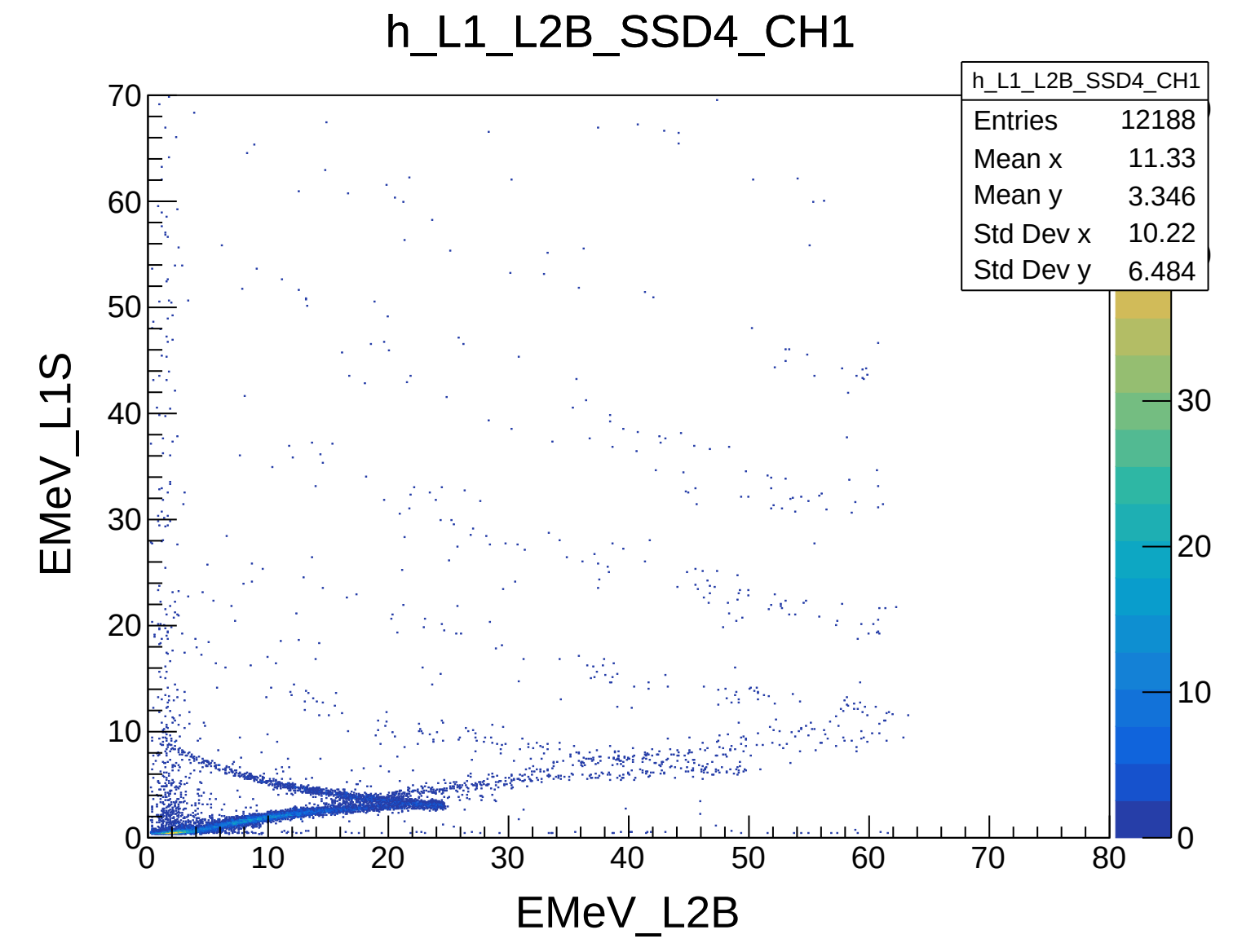

h_L1_L2B_SSD3_CH12
h_L1_L2B_SSD3_CH12
Entries 15344
Mean x 21.36
Mean y 5.432
Std Dev x 19.62
Std Dev y 11.36
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20

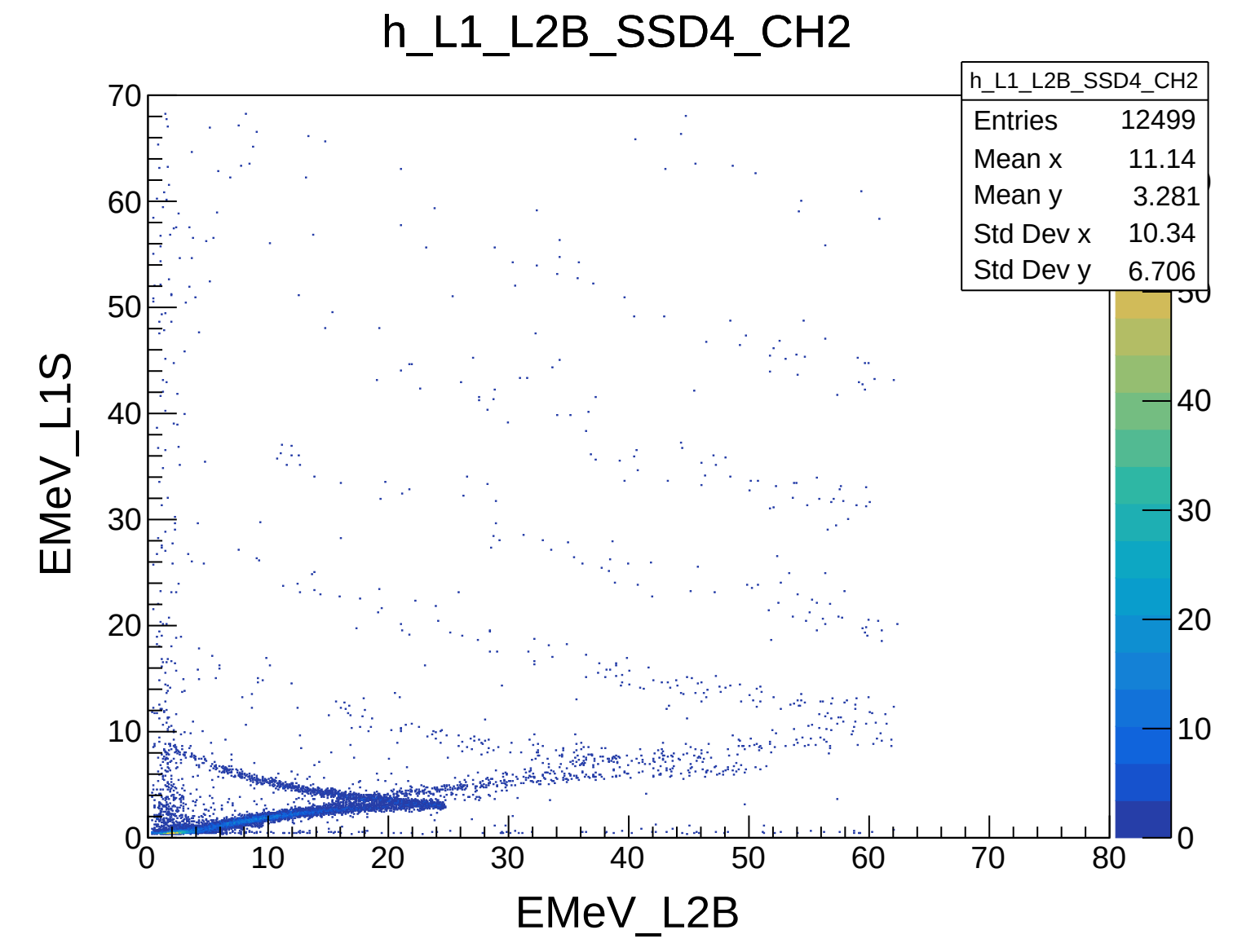

h_L1_L2B_SSD3_CH13
h_L1_L2B_SSD3_CH13
Entries 15397
Mean x 20.86
Mean y 5.623
Std Dev x 19.4
Std Dev y 11.89
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25

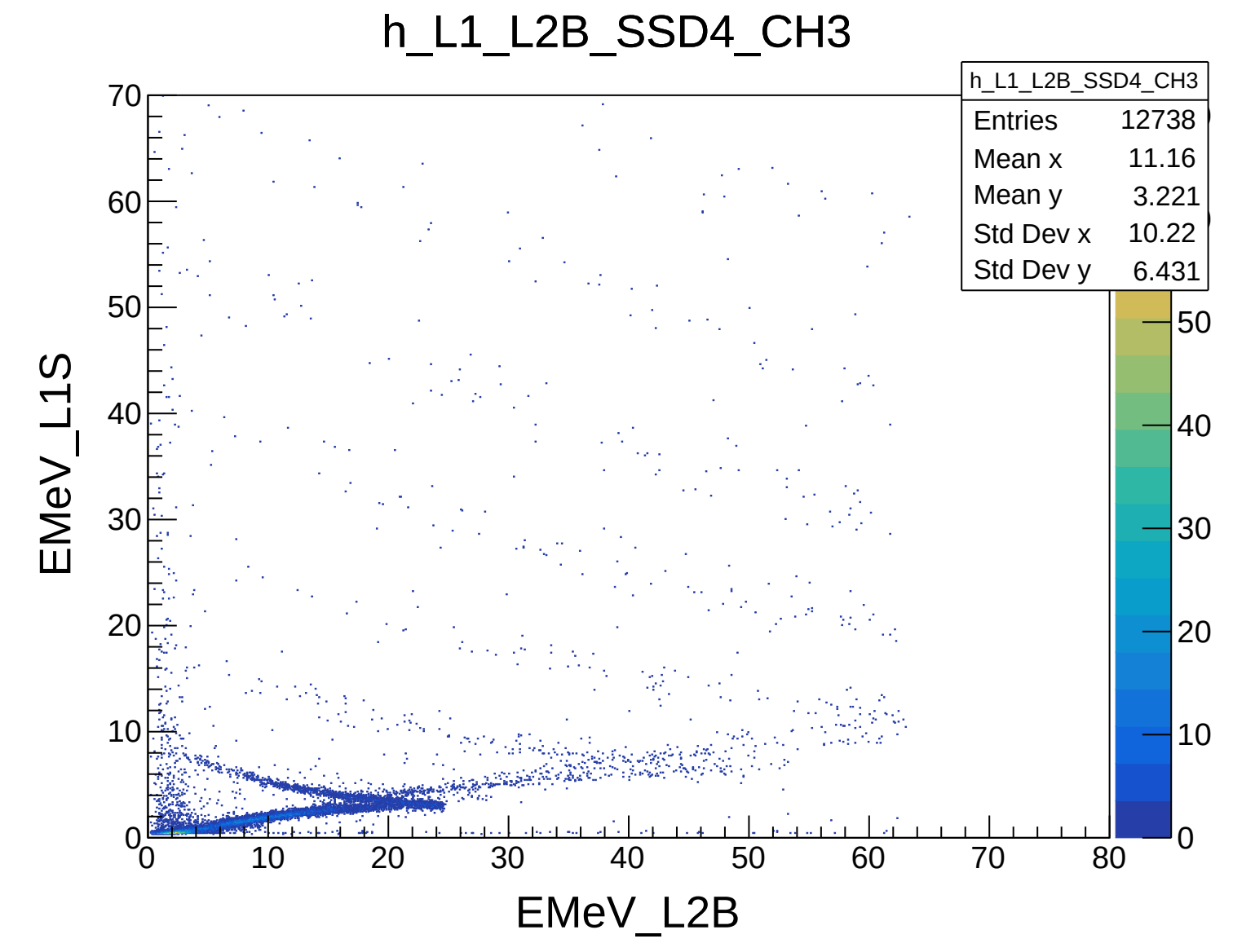

h_L1_L2B_SSD3_CH14
h_L1_L2B_SSD3_CH14
Entries 14211
Mean x 21.32
Mean y 5.36
Std Dev x 19.27
Std Dev y 11.03
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25

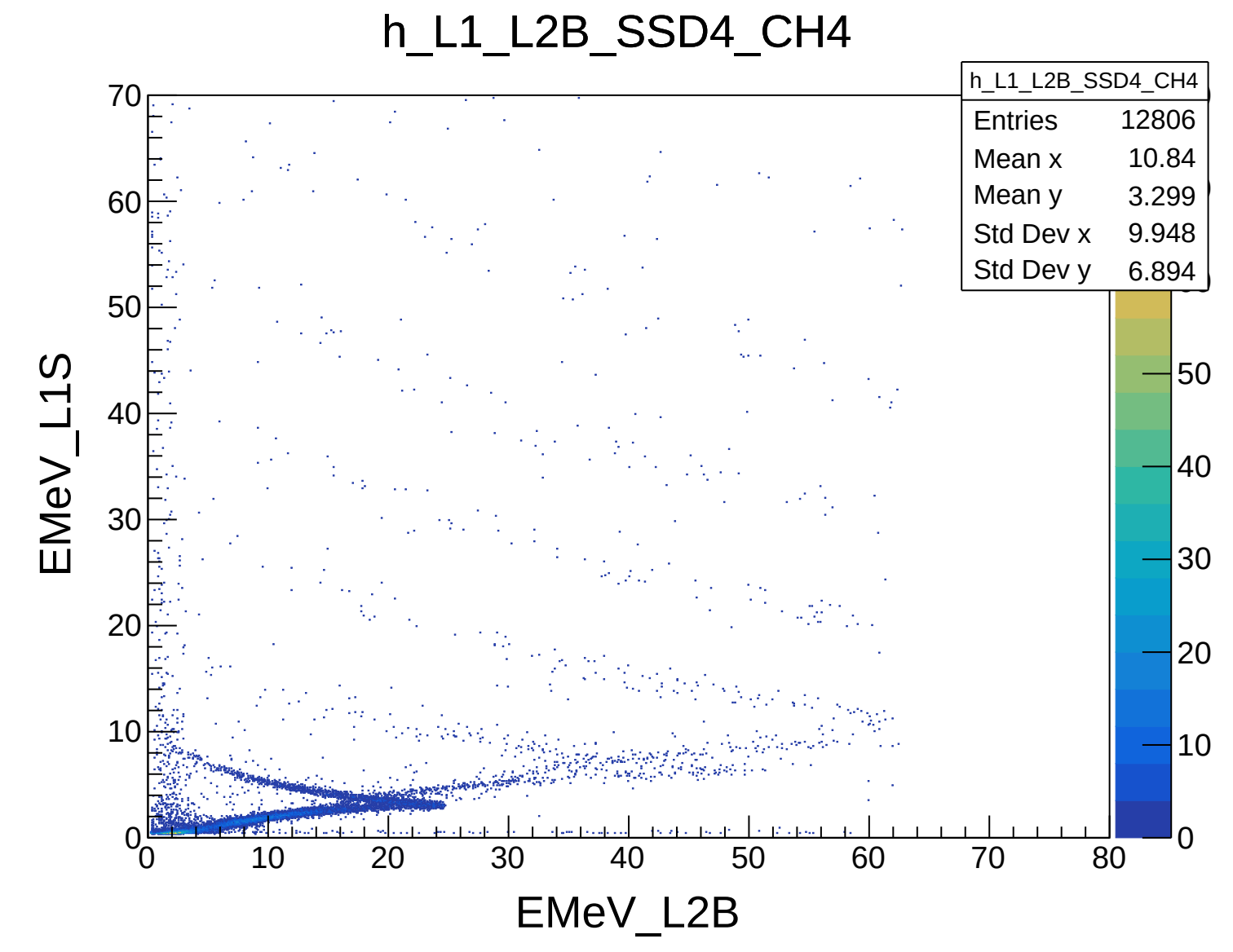

h_L1_L2B_SSD3_CH15
h_L1_L2B_SSD3_CH15
Entries 11345
Mean x 20.39
Mean y 5.3
Std Dev x 18.78
Std Dev y 11.52
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20

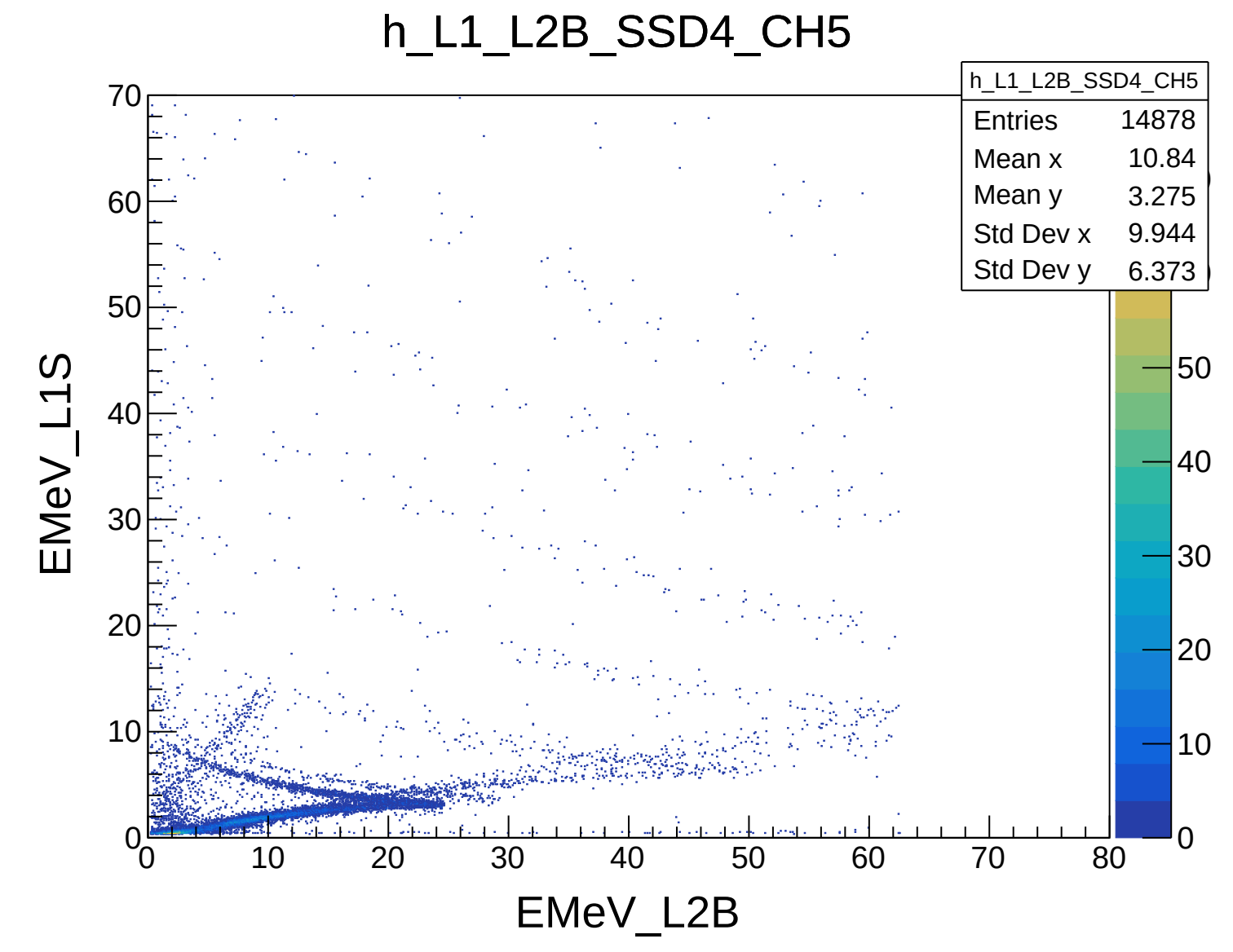

h_L1_L2B_SSD4_CH0
h_L1_L2B_SSD4_CH0
Entries 6421
Mean x 10.36
Mean y 3.454
Std Dev x 10.28
Std Dev y 8.779
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
0
5
10
15
20
25
30

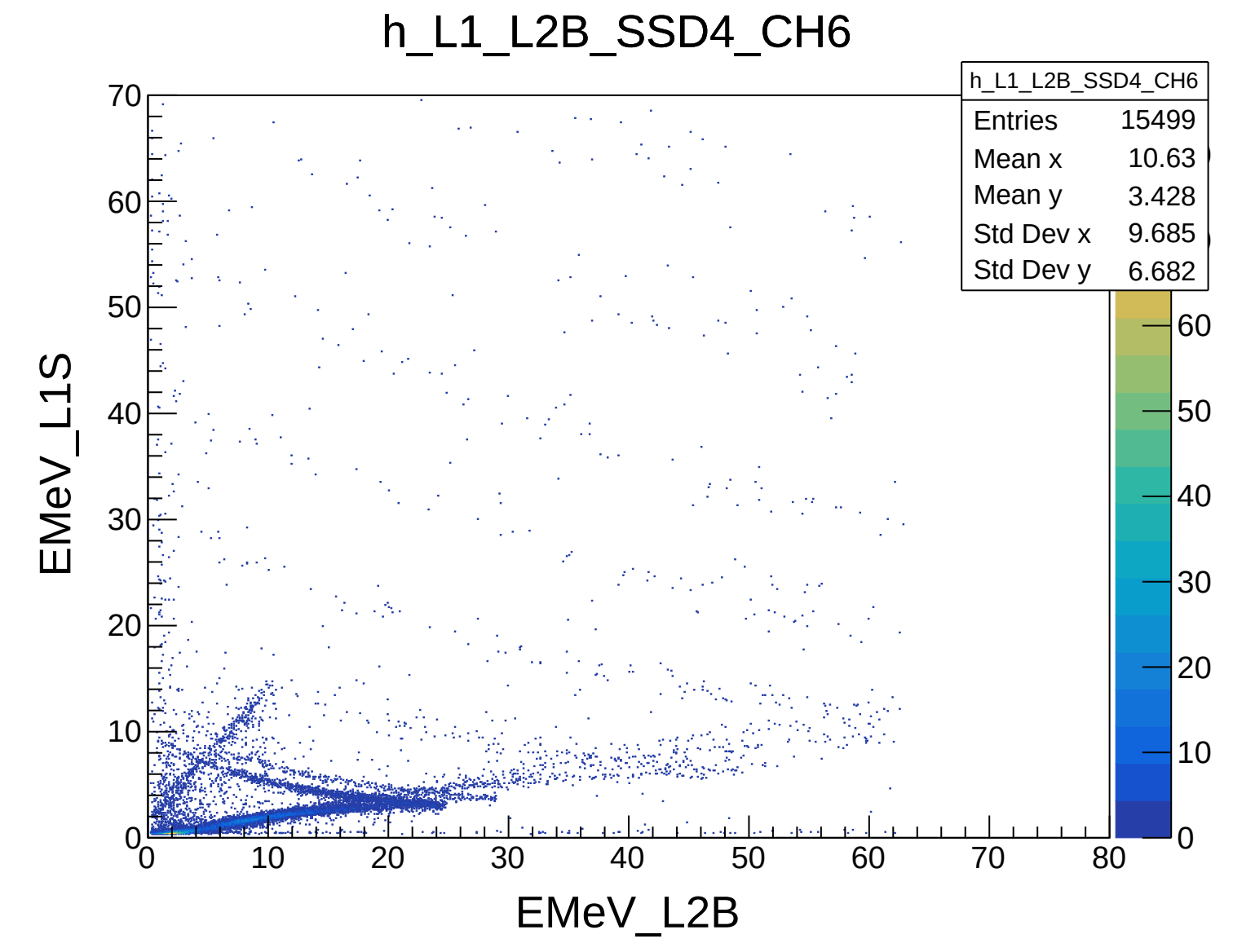

h_L1_L2B_SSD4_CH1
h_L1_L2B_SSD4_CH1
Entries 12188
Mean x 11.33
Mean y 3.346
Std Dev x 10.22
Std Dev y 6.484
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

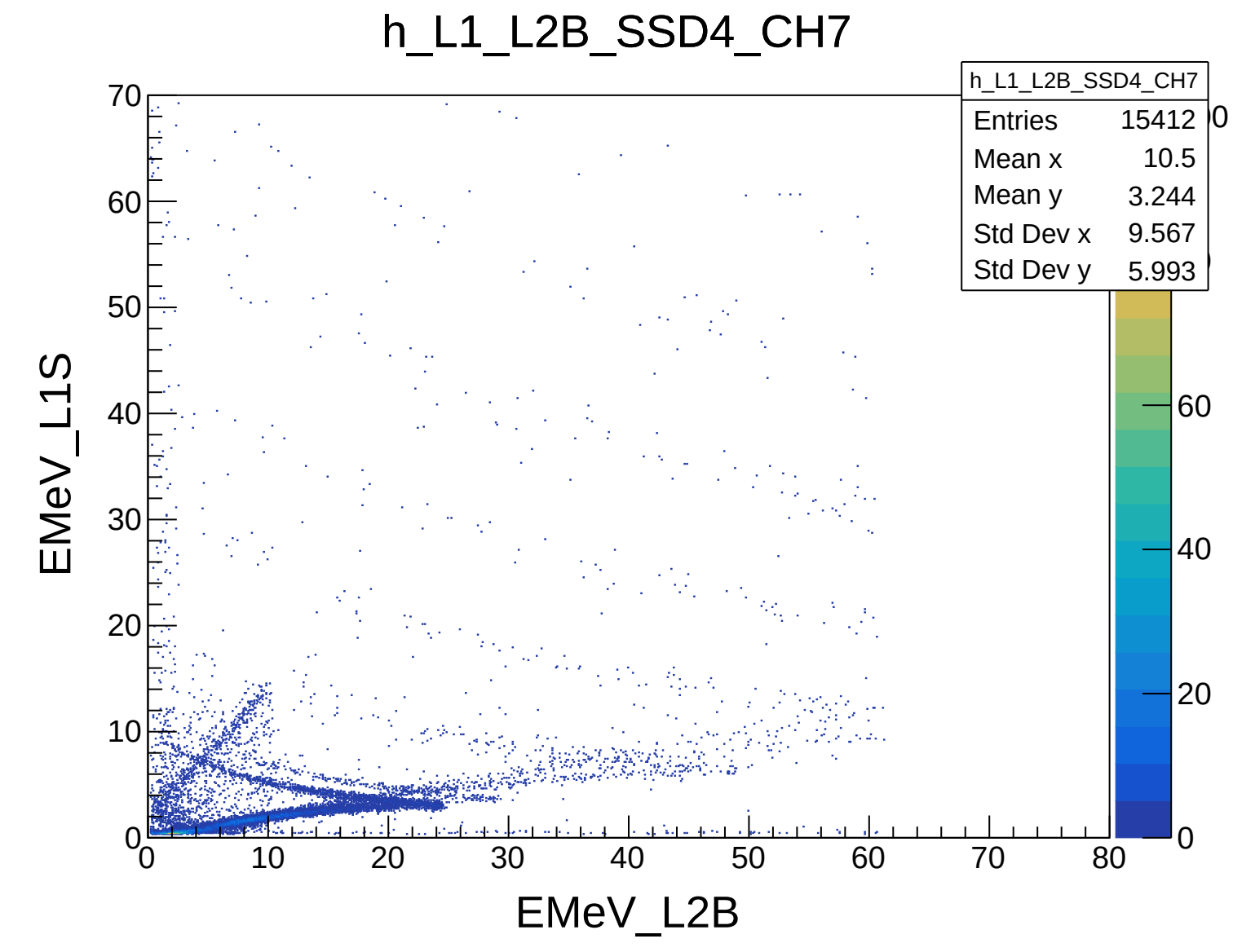

h_L1_L2B_SSD4_CH2
h_L1_L2B_SSD4_CH2
Entries 12499
Mean x 11.14
Mean y 3.281
Std Dev x 10.34
Std Dev y 6.706
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

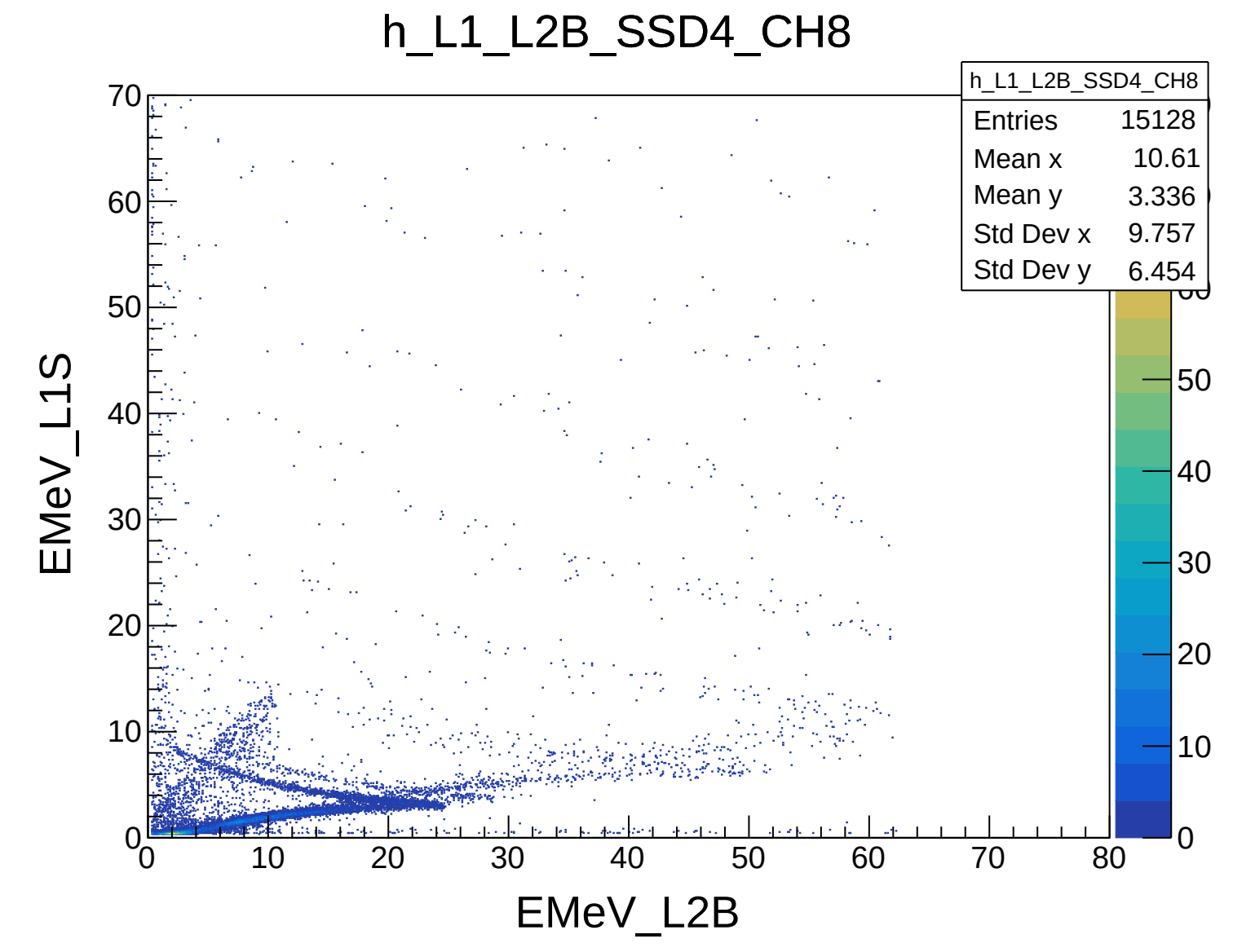

h_L1_L2B_SSD4_CH3
h_L1_L2B_SSD4_CH3
Entries 12738
Mean x 11.16
Mean y 3.221
Std Dev x 10.22
Std Dev y 6.431
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

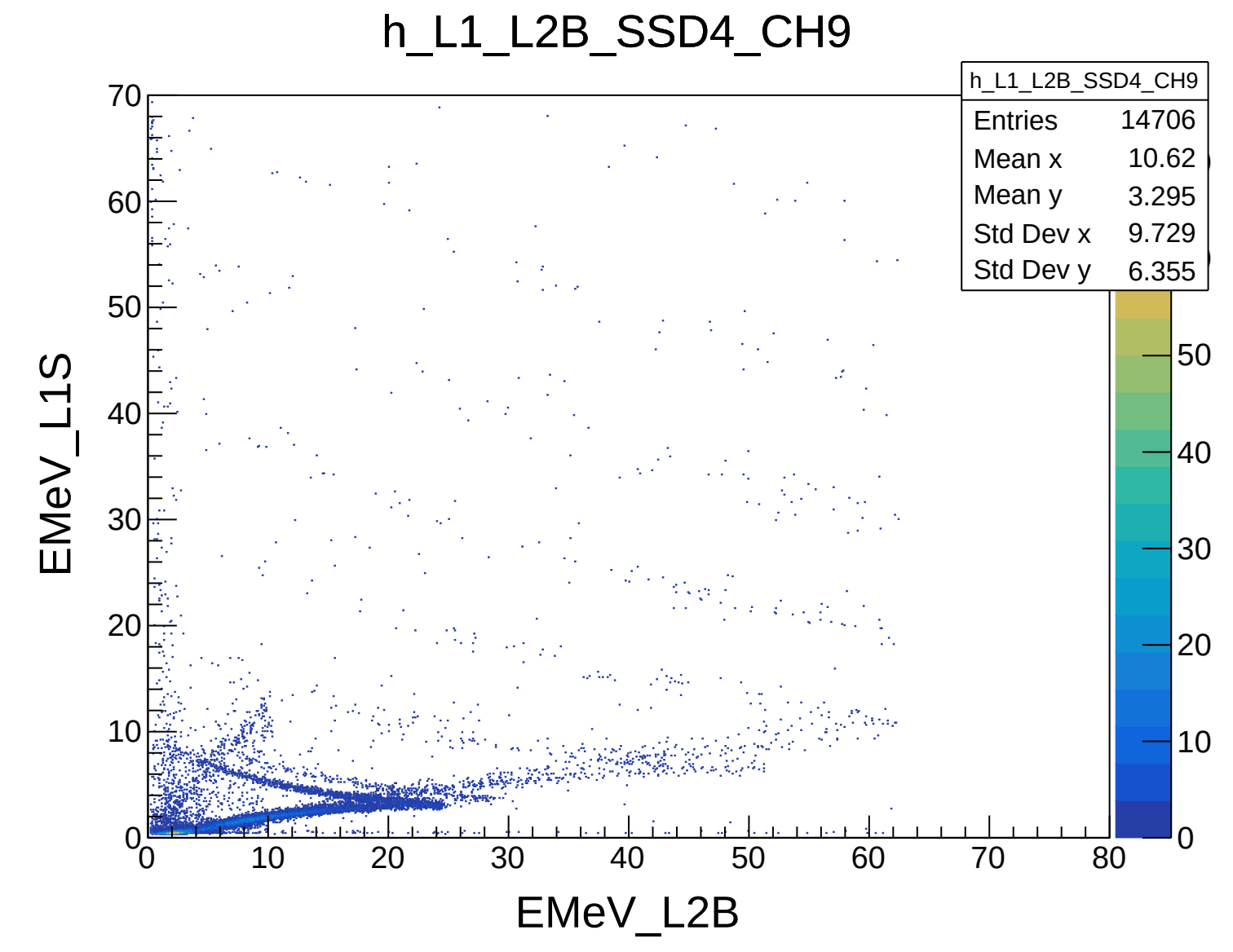

h_L1_L2B_SSD4_CH4
h_L1_L2B_SSD4_CH4
Entries 12806
Mean x 10.84
Mean y 3.299
Std Dev x 9.948
Std Dev y 6.894
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

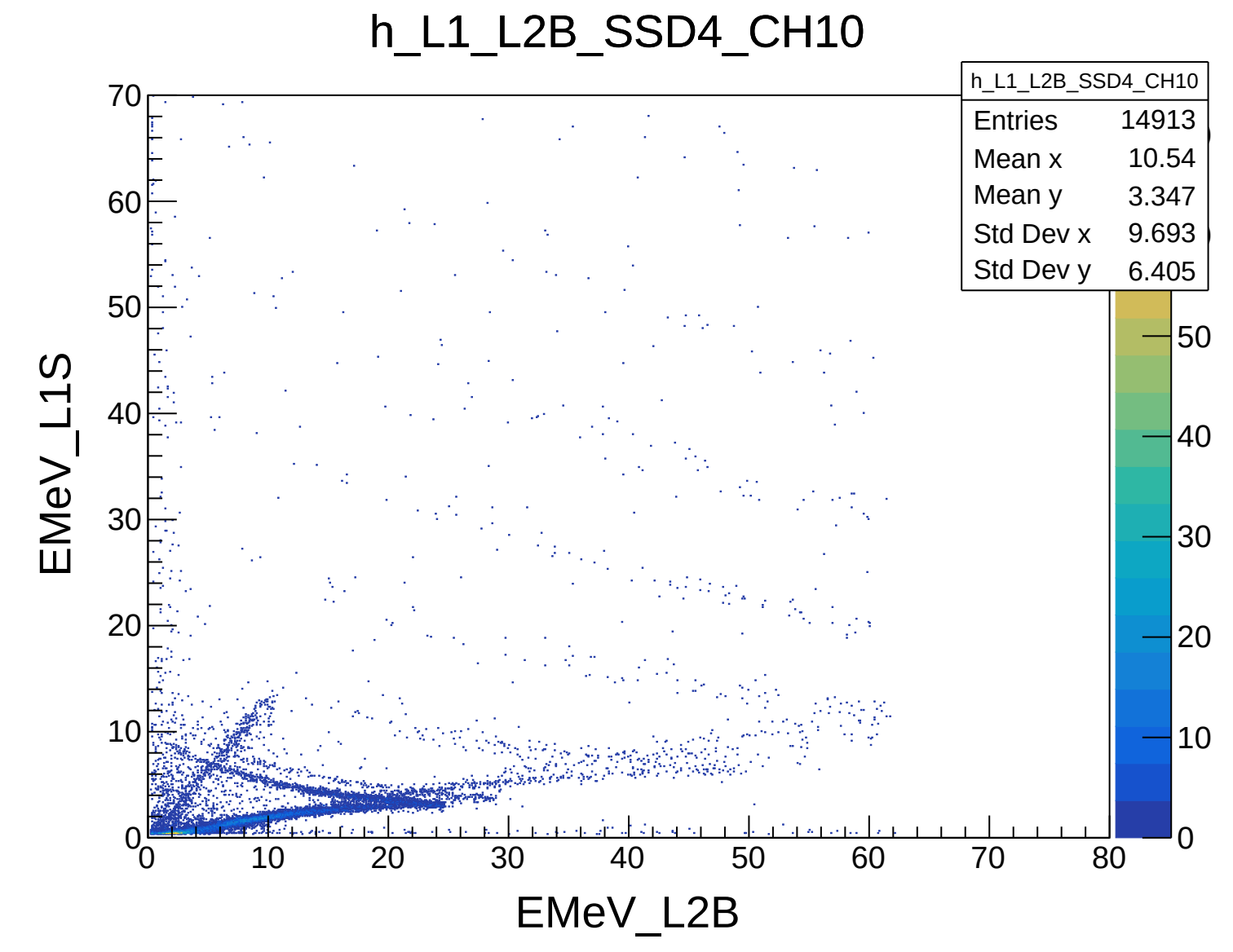

h_L1_L2B_SSD4_CH5
h_L1_L2B_SSD4_CH5
Entries 14878
Mean x 10.84
Mean y 3.275
Std Dev x 9.944
Std Dev y 6.373
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

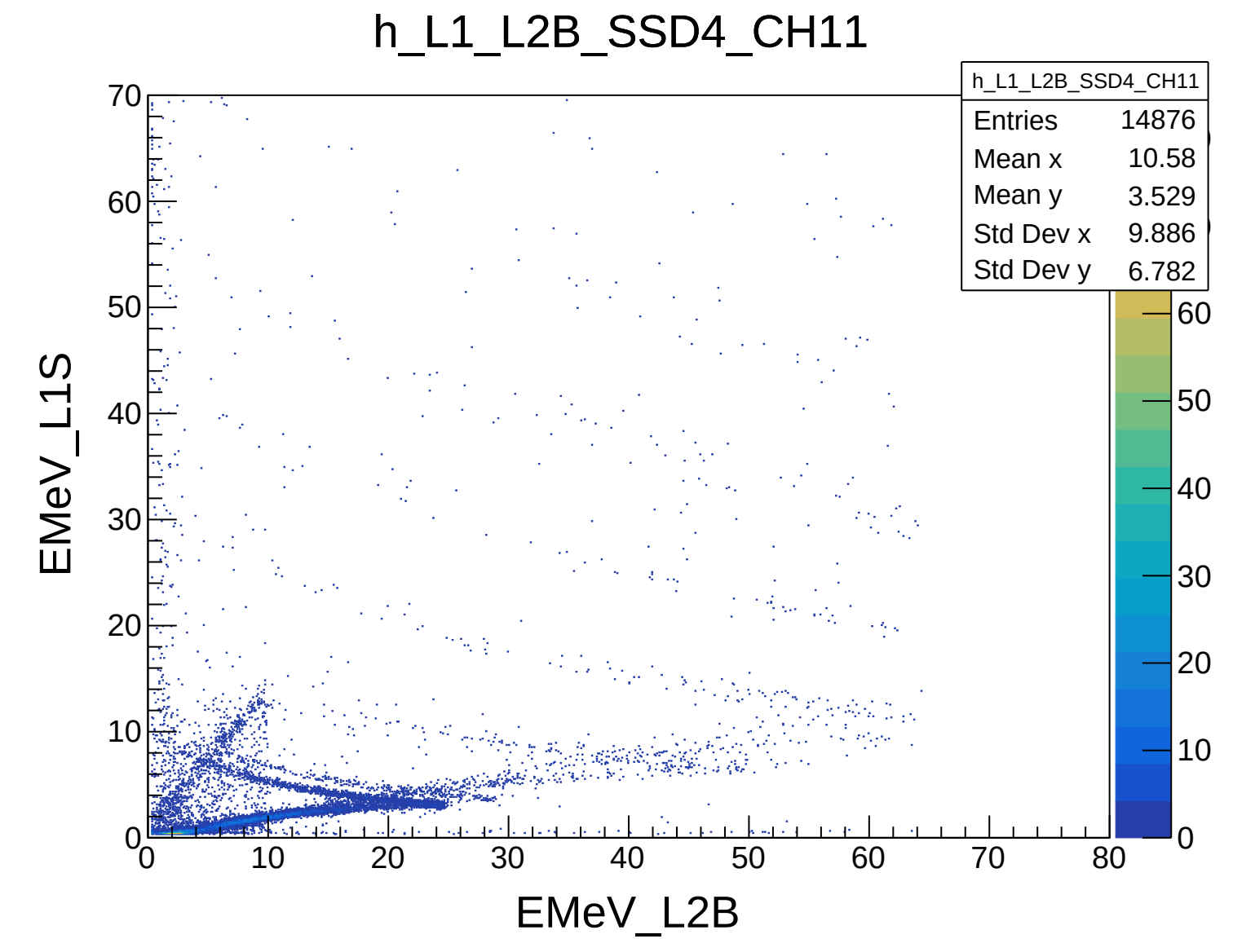

h_L1_L2B_SSD4_CH6
h_L1_L2B_SSD4_CH6
Entries 15499
Mean x 10.63
Mean y 3.428
Std Dev x 9.685
Std Dev y 6.682
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

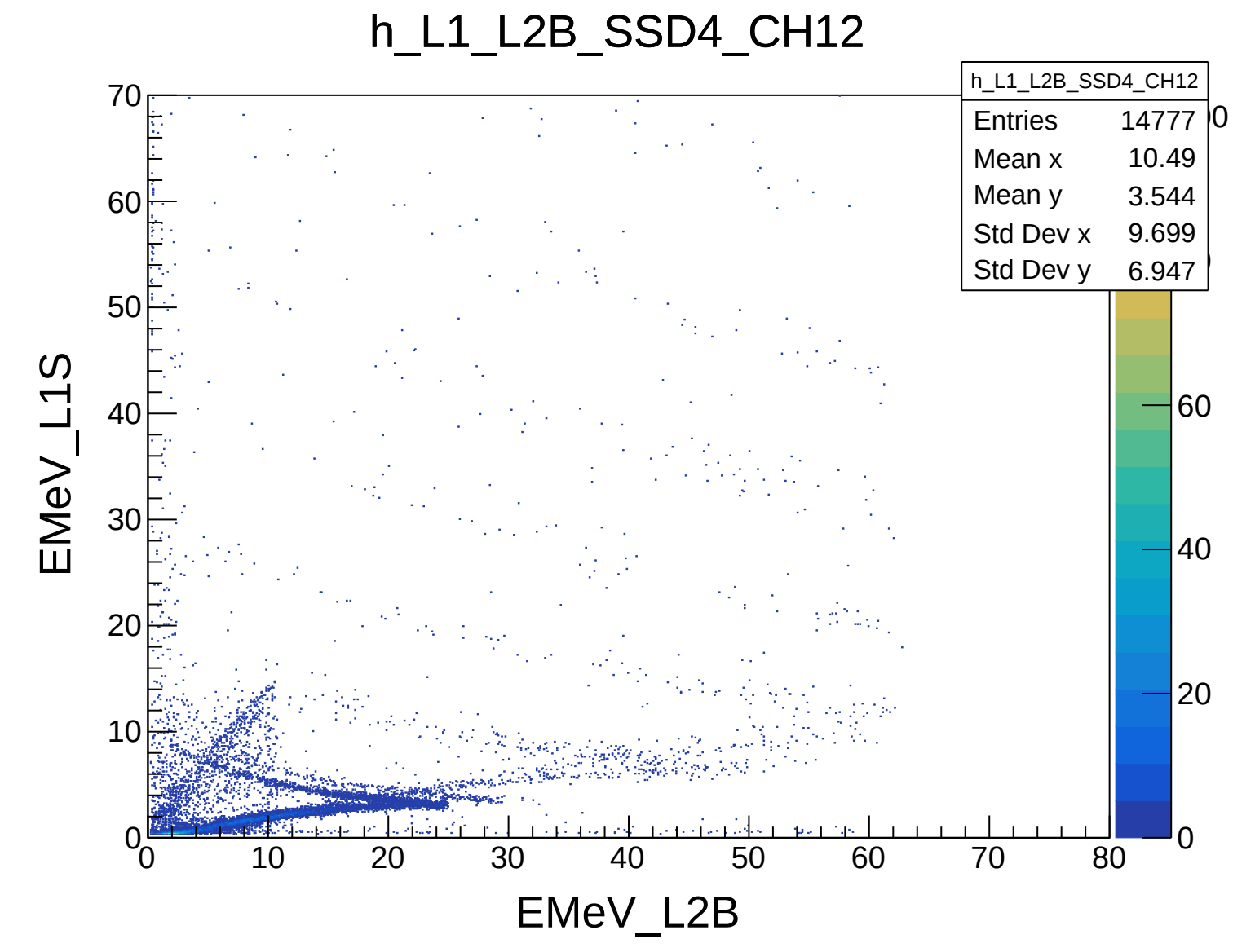

h_L1_L2B_SSD4_CH7
h_L1_L2B_SSD4_CH7
Entries 15412
Mean x 10.5
Mean y 3.244
Std Dev x 9.567
Std Dev y 5.993
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

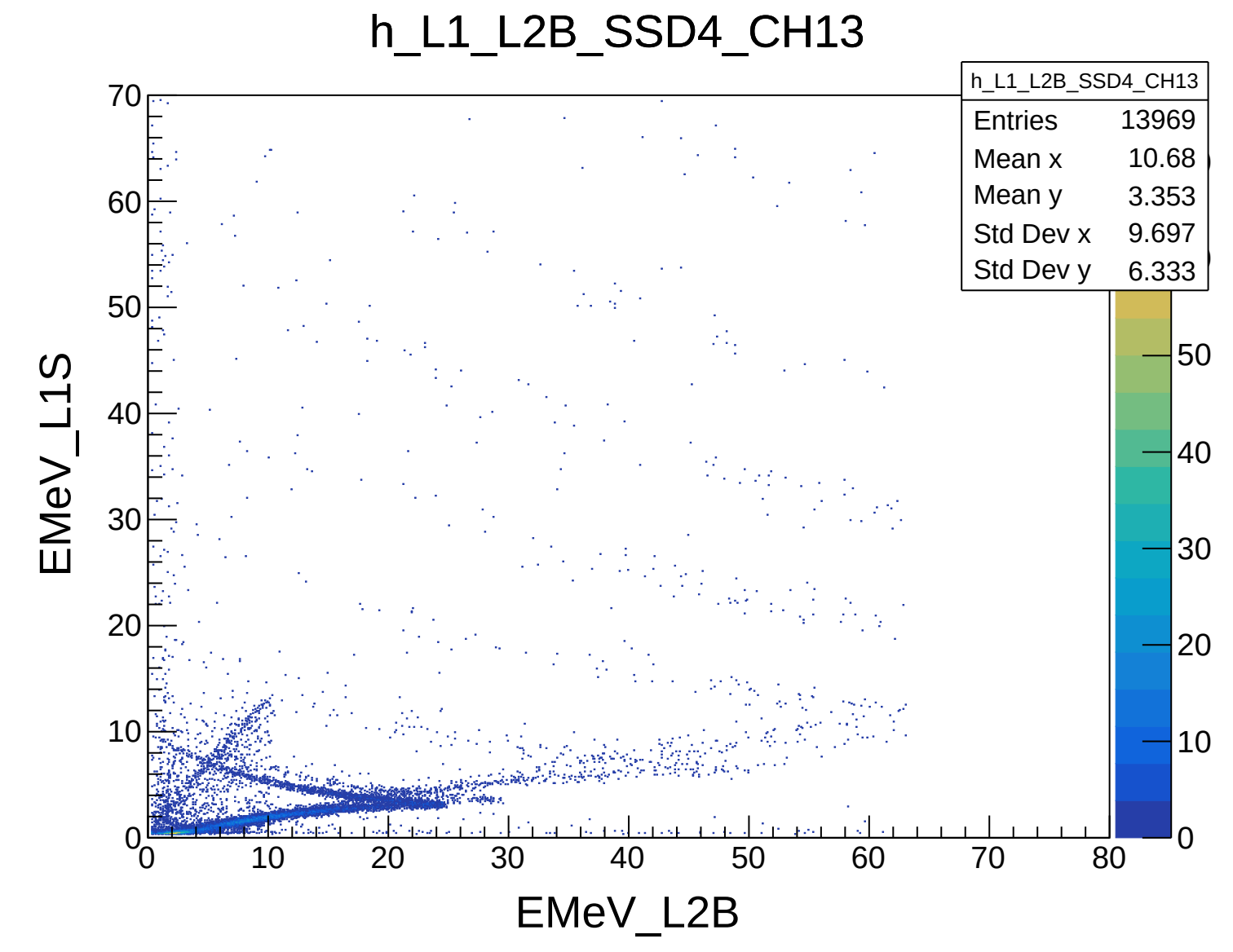

h_L1_L2B_SSD4_CH8
h_L1_L2B_SSD4_CH8
Entries 15128
Mean x 10.61
Mean y 3.336
Std Dev x 9.757
Std Dev y 6.454
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

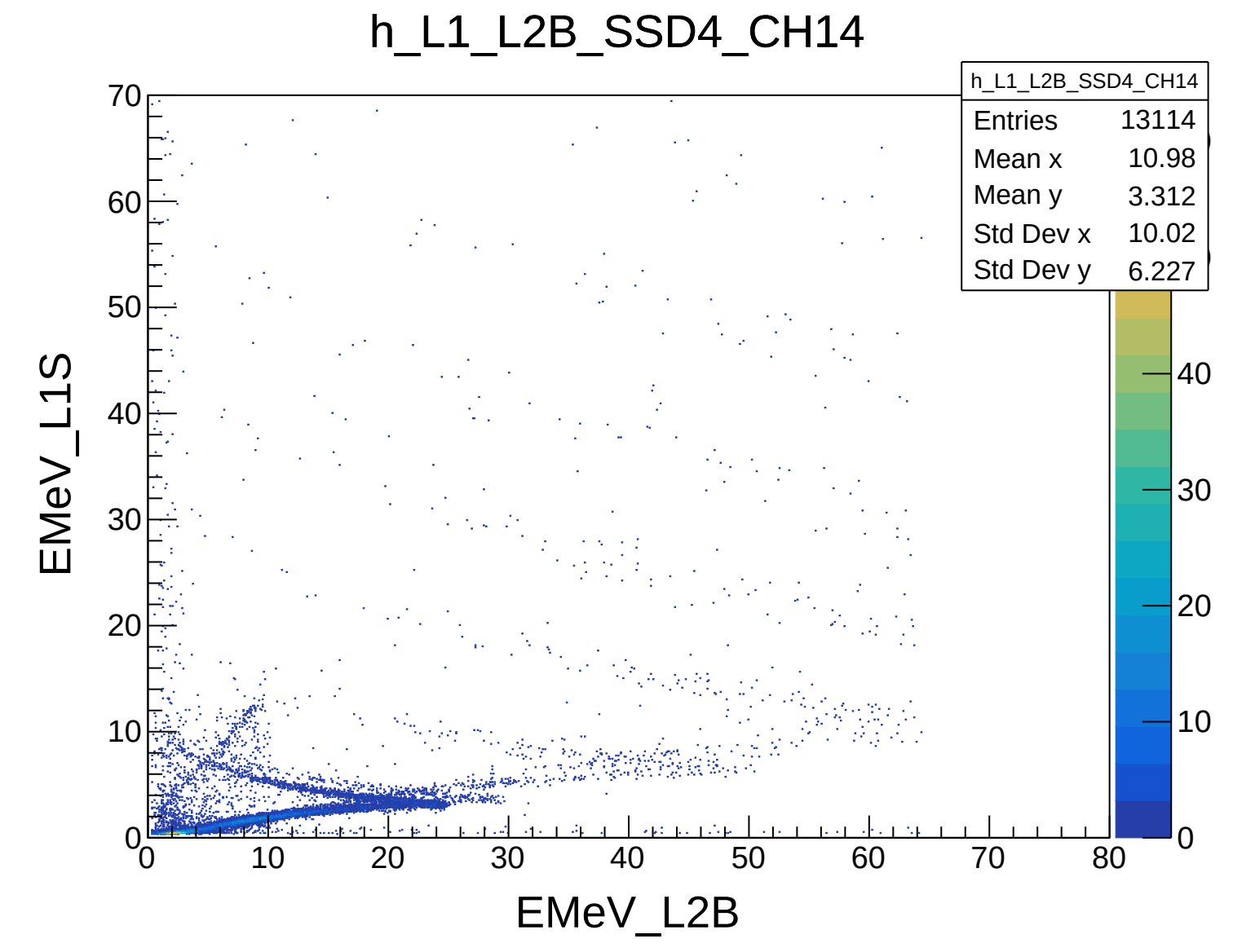

h_L1_L2B_SSD4_CH9
h_L1_L2B_SSD4_CH9
Entries 14706
Mean x 10.62
Mean y 3.295
Std Dev x 9.729
Std Dev y 6.355
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

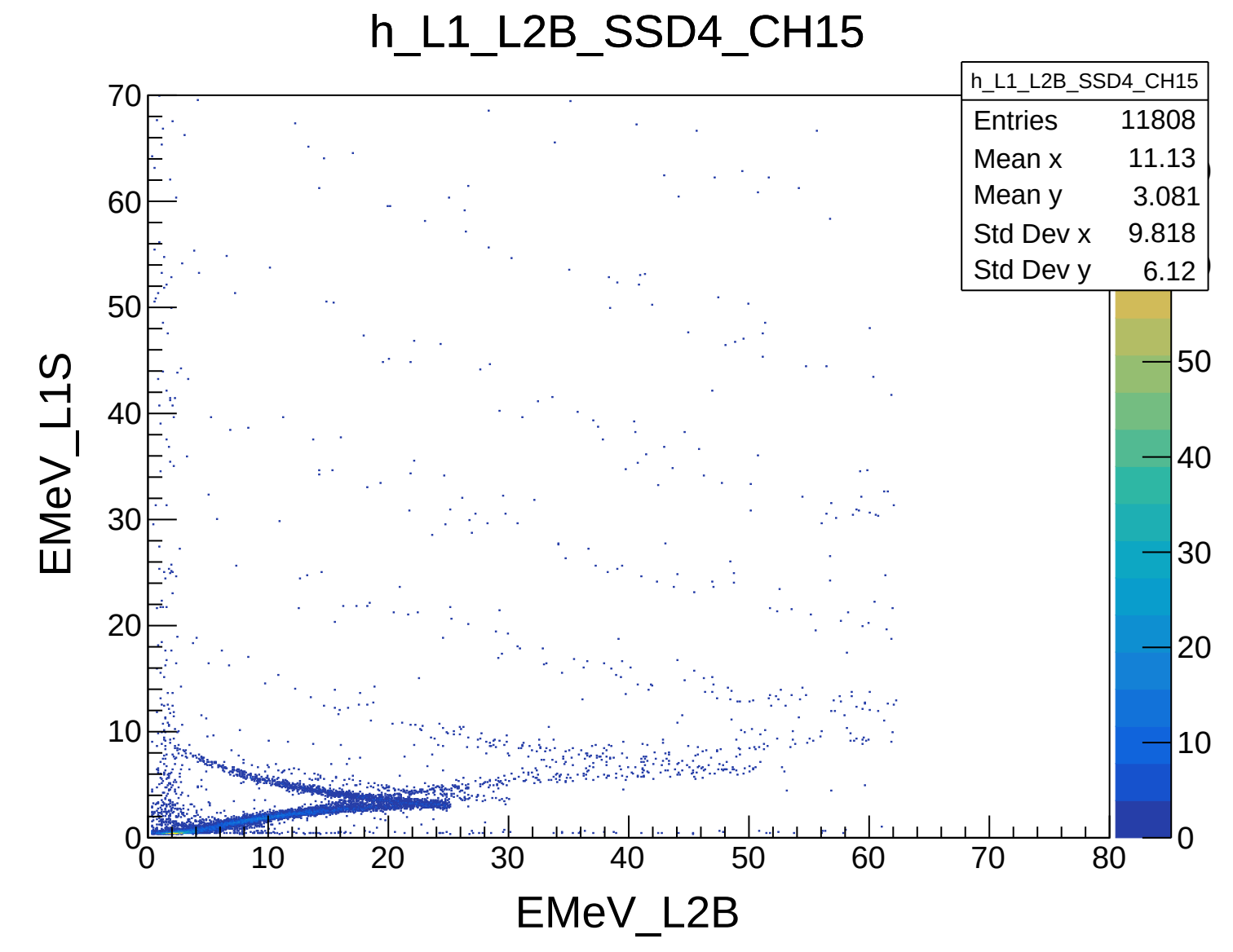

h_L1_L2B_SSD4_CH10
h_L1_L2B_SSD4_CH10
Entries 14913
Mean x 10.54
Mean y 3.347
Std Dev x 9.693
Std Dev y 6.405
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80


h_L1_L2B_SSD4_CH11
h_L1_L2B_SSD4_CH11
Entries 14876
Mean x 10.58
Mean y 3.529
Std Dev x 9.886
Std Dev y 6.782
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80


h_L1_L2B_SSD4_CH12
h_L1_L2B_SSD4_CH12
Entries 14777
Mean x 10.49
Mean y 3.544
Std Dev x 9.699
Std Dev y 6.947
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80


h_L1_L2B_SSD4_CH13
h_L1_L2B_SSD4_CH13
Entries 13969
Mean x 10.68
Mean y 3.353
Std Dev x 9.697
Std Dev y 6.333
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80


h_L1_L2B_SSD4_CH14
h_L1_L2B_SSD4_CH14
Entries 13114
Mean x 10.98
Mean y 3.312
Std Dev x 10.02
Std Dev y 6.227
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80


h_L1_L2B_SSD4_CH15
h_L1_L2B_SSD4_CH15
Entries 11808
Mean x 11.13
Mean y 3.081
Std Dev x 9.818
Std Dev y 6.12
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80