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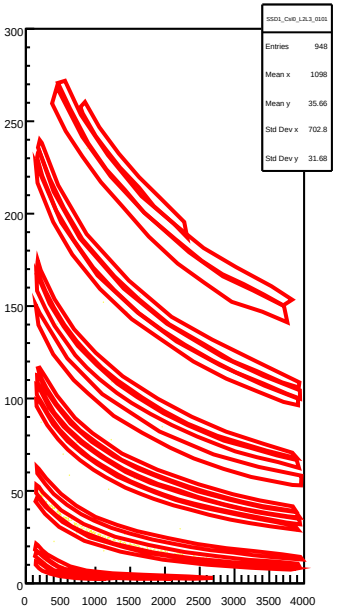
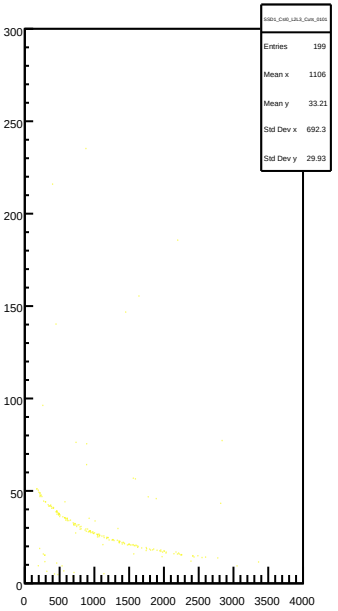
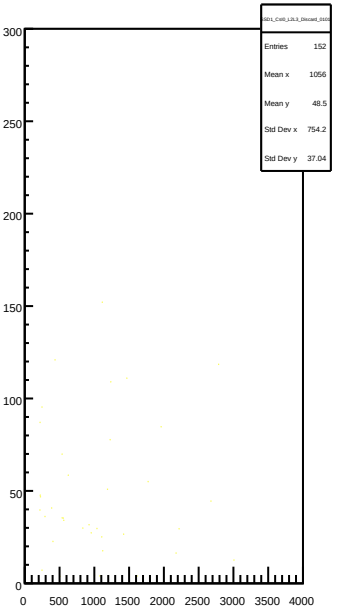


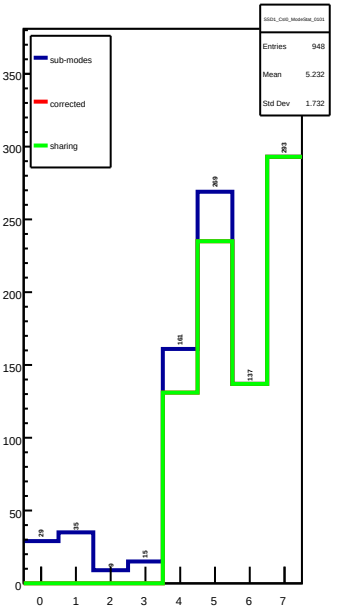
SSD1_CsI0_L2L3_Cuts_0101



SSD1_CsI0_L2L3_Discard_0101



SSD1_CsI0_ModeStat_0101



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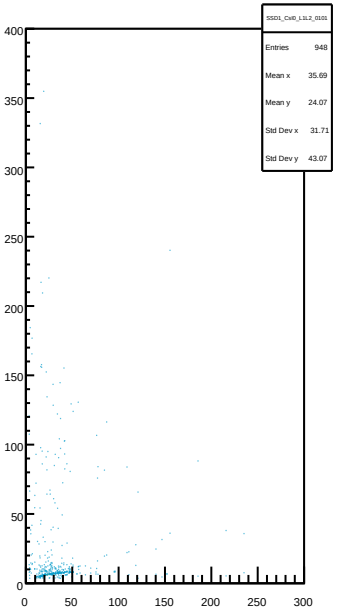

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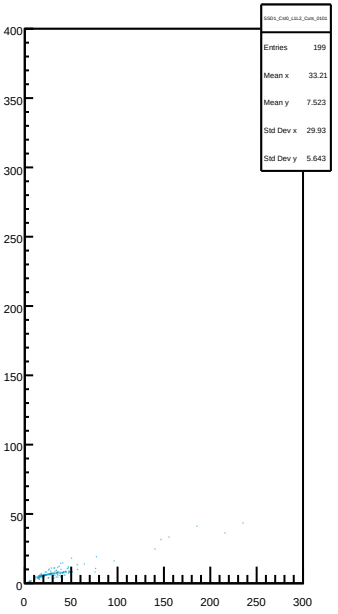

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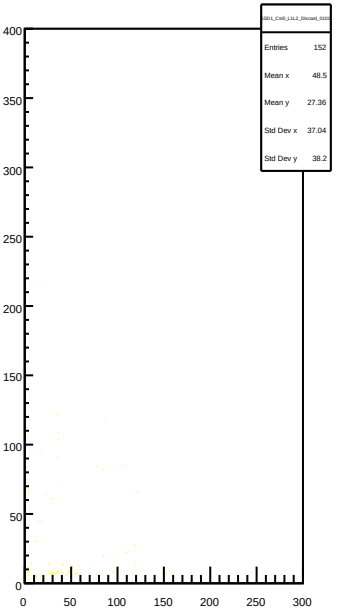
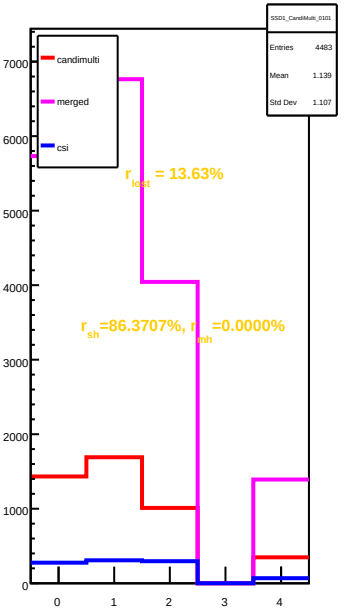


SSD1_CandiMulti_0101



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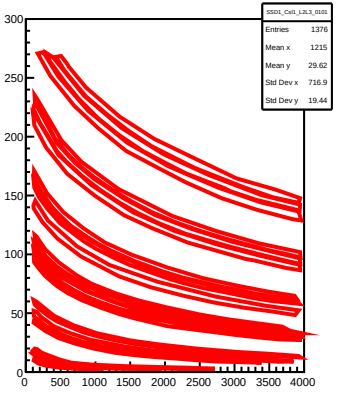
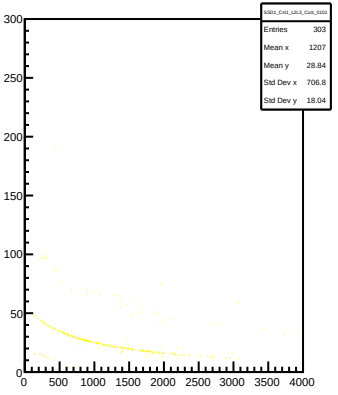


SSD1_CsI1_L2L3_Cuts_0101



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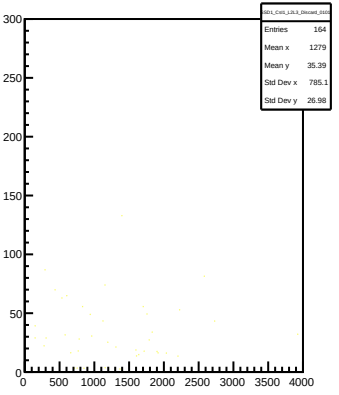
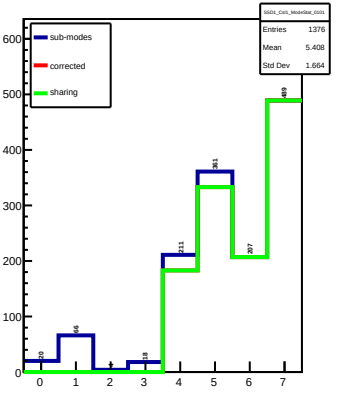


SSD1_CsI1_ModeStat_0101



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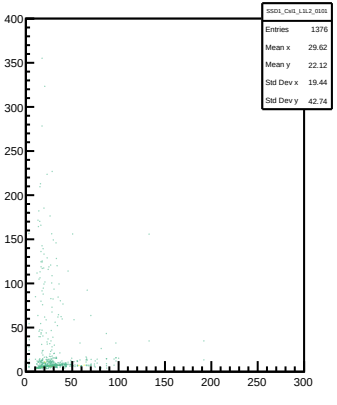
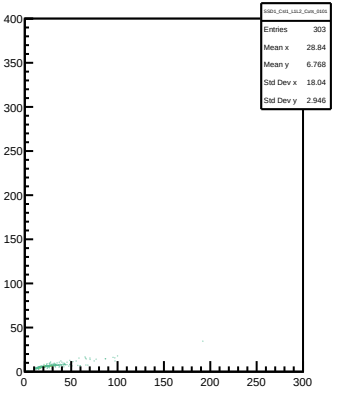
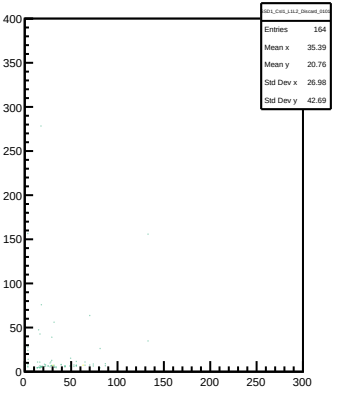


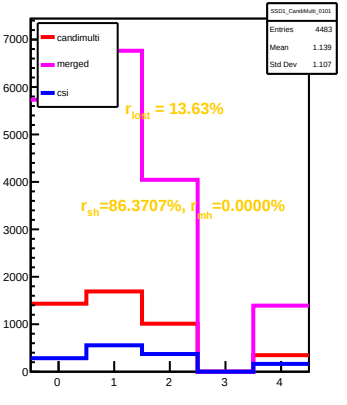
SSD1_CsI1_L1L2_Cuts_0101



SSD1_CsI1_L1L2_Discard_0101



SSD1_CandiMulti_0101



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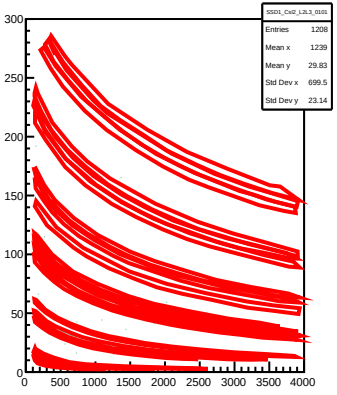
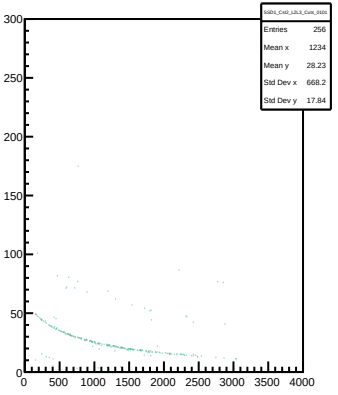


SSD1_CsI2_L2L3_Cuts_0101



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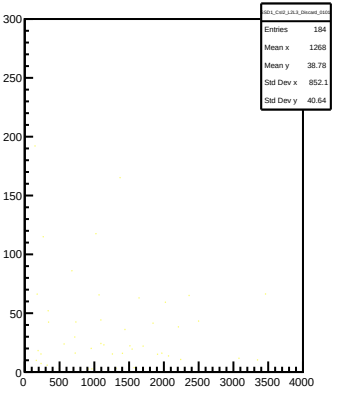

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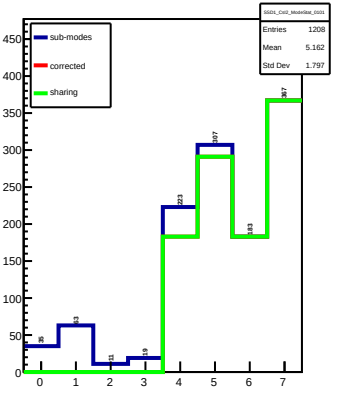

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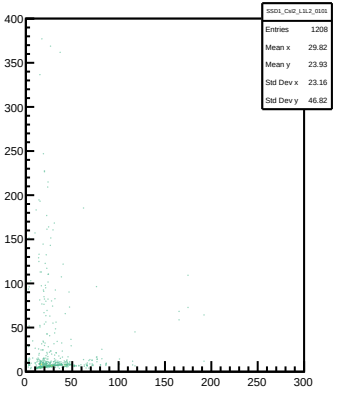

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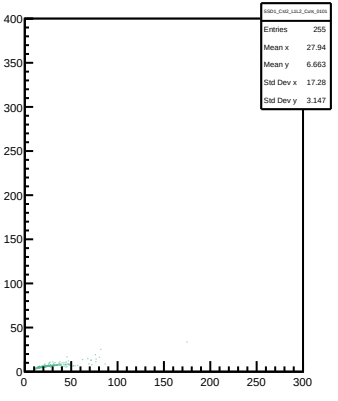

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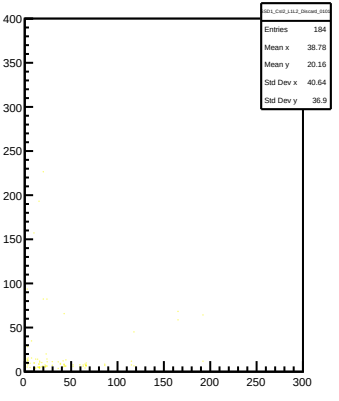
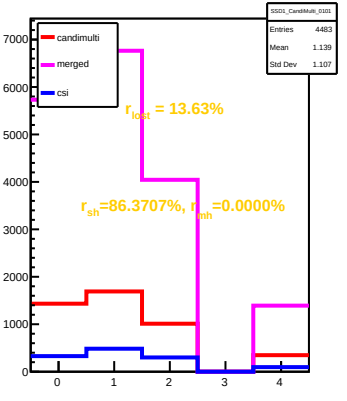


SSD1_CandiMulti_0101



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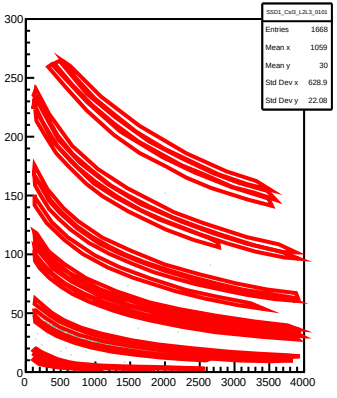
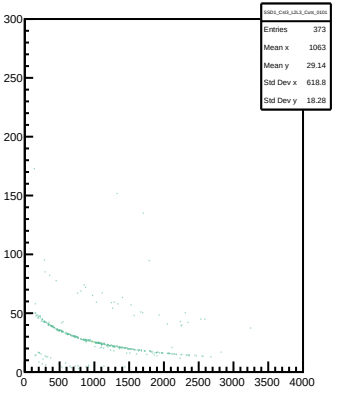


SSD1_CsI3_L2L3_Cuts_0101



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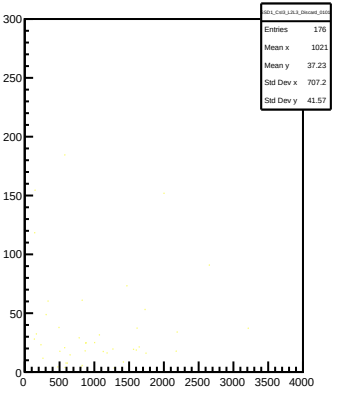

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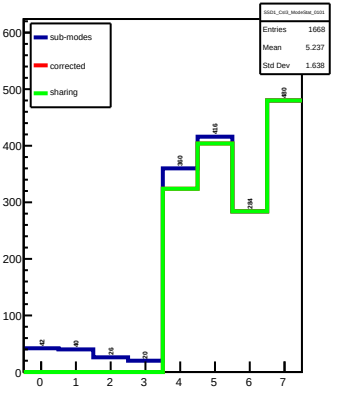

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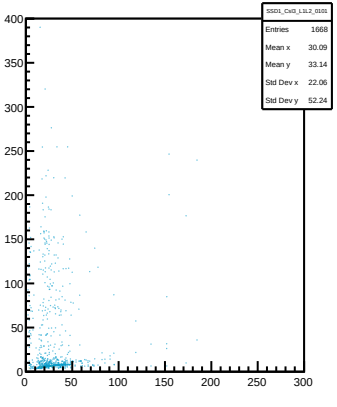
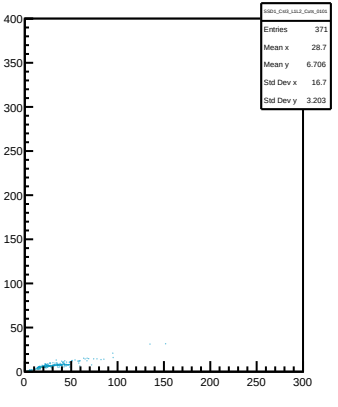
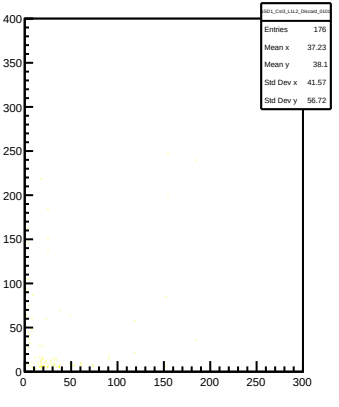


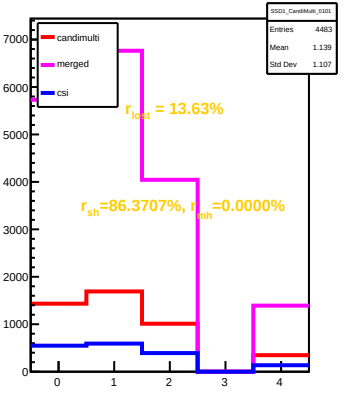
SSD1_CsI3_L1L2_Cuts_0101



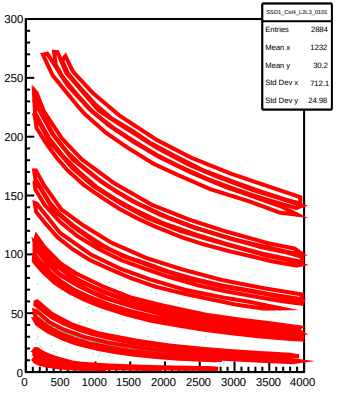
SSD1_CsI3_L1L2_Discard_0101



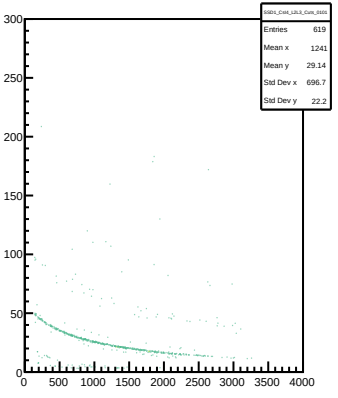
SSD1_CandiMulti_0101



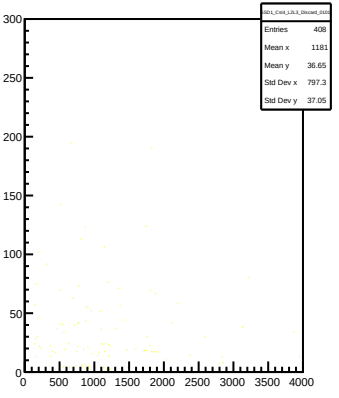
SSD1_CsI4_L2L3_0101



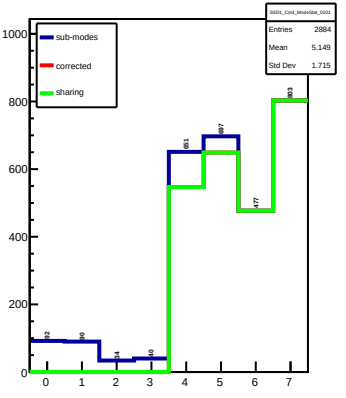
SSD1_CsI4_L2L3_Cuts_0101



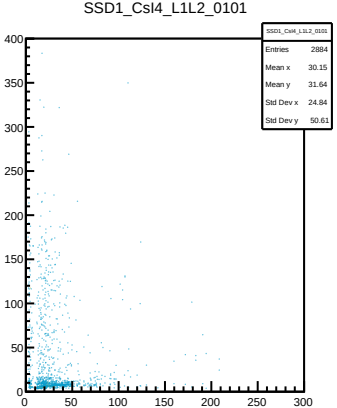
SSD1_CsI4_L2L3_Discard_0101



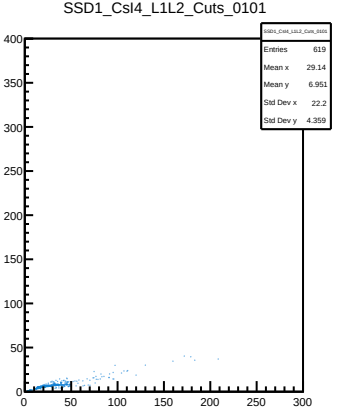
SSD1_CsI4_ModeStat_0101



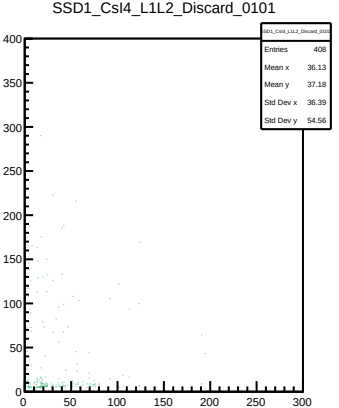
SSD1_CsI4_L1L2_0101



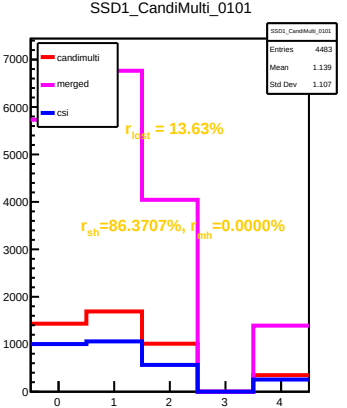
SSD1_CsI4_L1L2_Cuts_0101



SSD1_CsI4_L1L2_Discard_0101



SSD1_CandiMulti_0101



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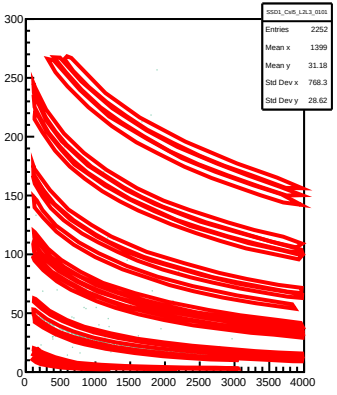
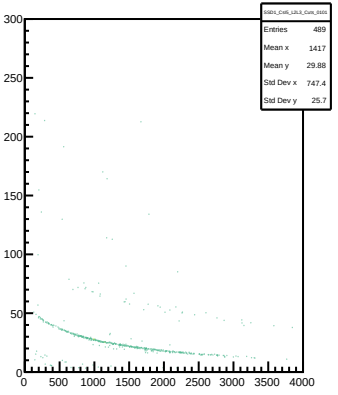
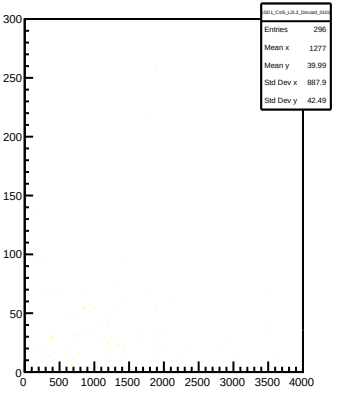


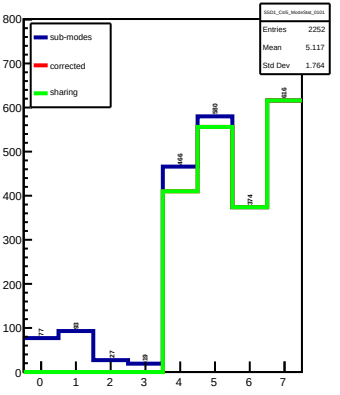
SSD1_CsI5_L2L3_Cuts_0101



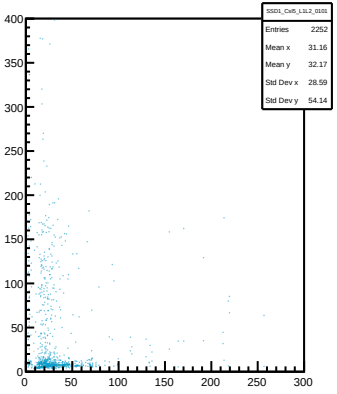
SSD1_CsI5_L2L3_Discard_0101



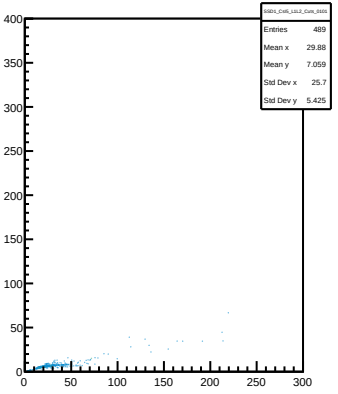
SSD1_CsI5_ModeStat_0101



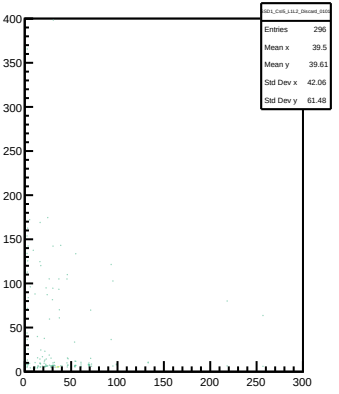
SSD1_CsI5_L1L2_0101



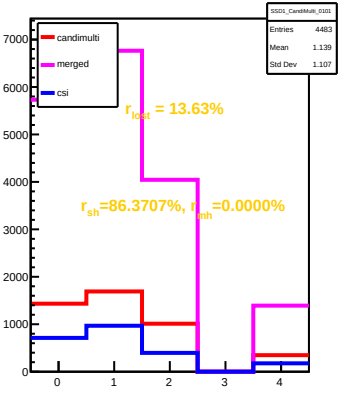
SSD1_CsI5_L1L2_Cuts_0101



SSD1_CsI5_L1L2_Discard_0101



SSD1_CandiMulti_0101



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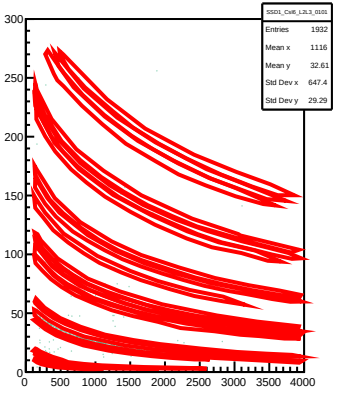
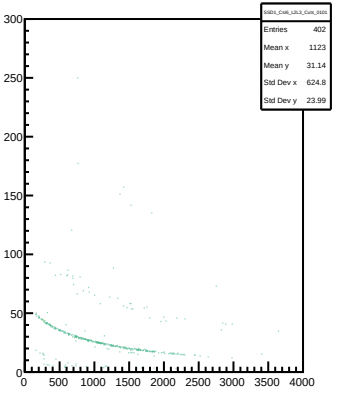
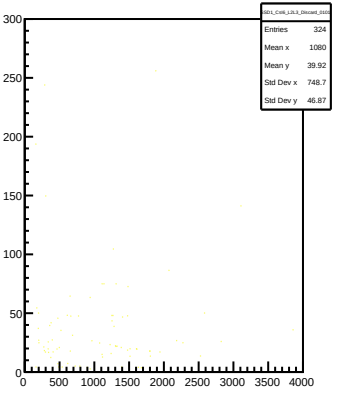


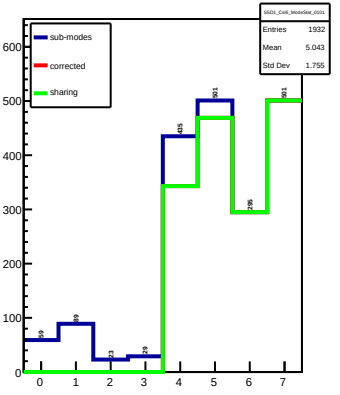
SSD1_CsI6_L2L3_Cuts_0101



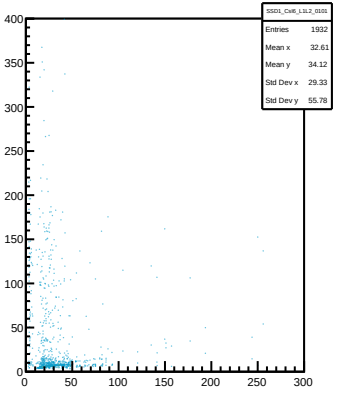
SSD1_CsI6_L2L3_Discard_0101



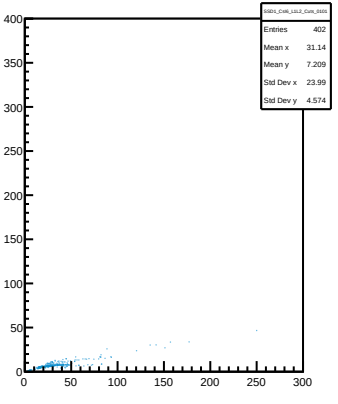
SSD1_CsI6_ModeStat_0101



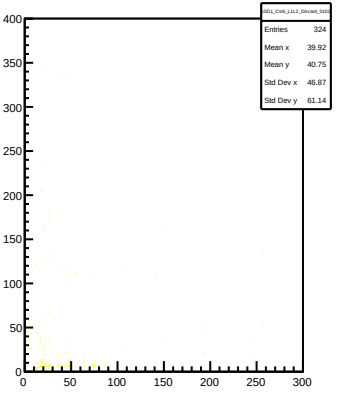
SSD1_CsI6_L1L2_0101



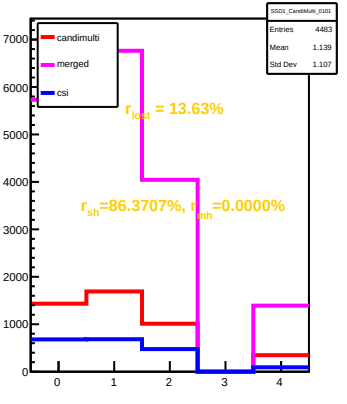
SSD1_CsI6_L1L2_Cuts_0101



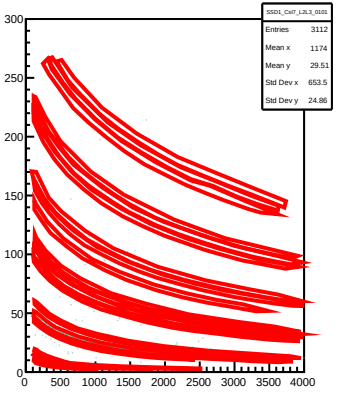
SSD1_CsI6_L1L2_Discard_0101



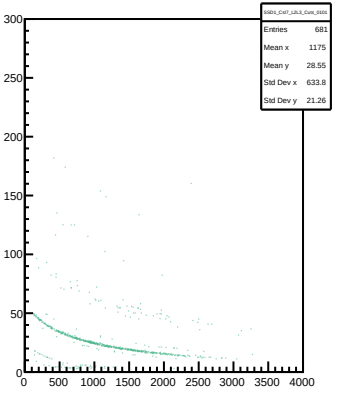
SSD1_CandiMulti_0101



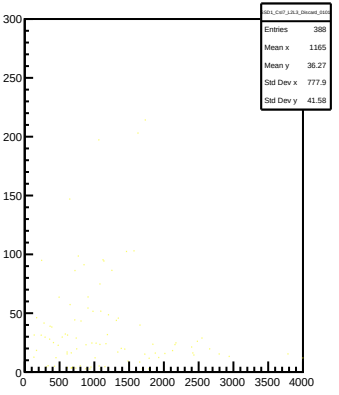
SSD1_CsI7_L2L3_0101



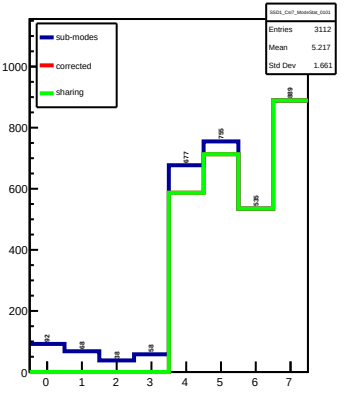
SSD1_CsI7_L2L3_Cuts_0101



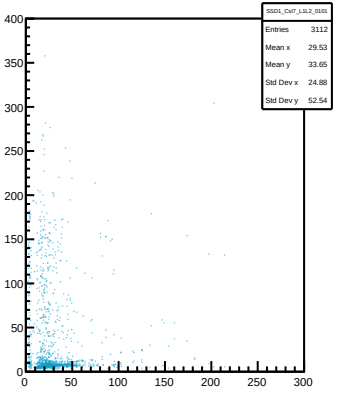
SSD1_CsI7_L2L3_Discard_0101



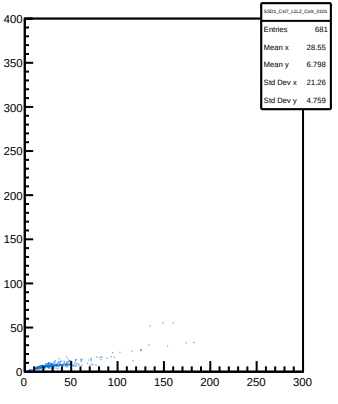
SSD1_CsI7_ModeStat_0101



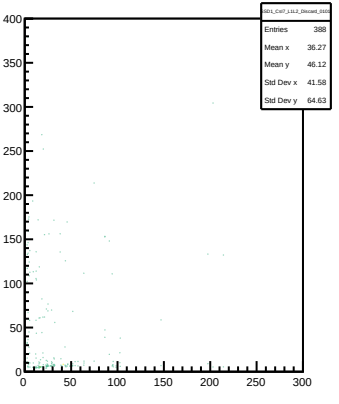
SSD1_CsI7_L1L2_0101



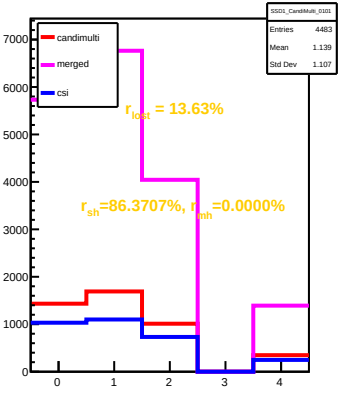
SSD1_CsI7_L1L2_Cuts_0101



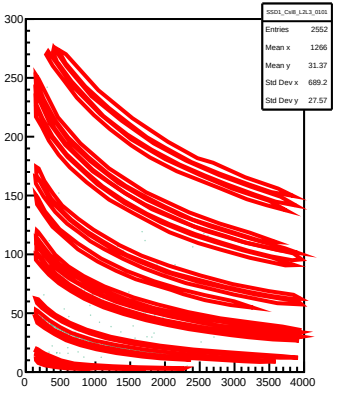
SSD1_CsI7_L1L2_Discard_0101



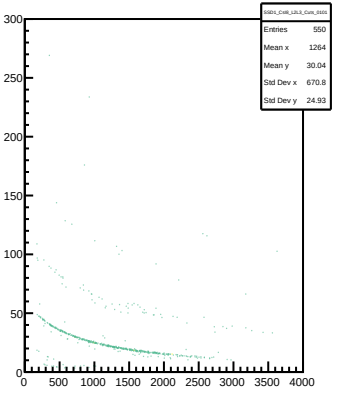
SSD1_CandiMulti_0101



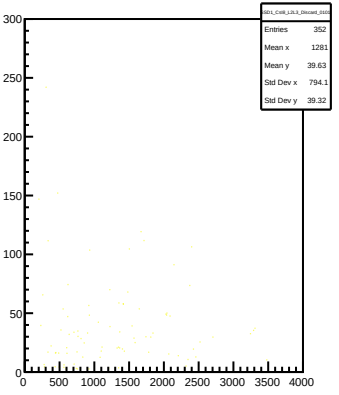
SSD1_CsI8_L2L3_0101



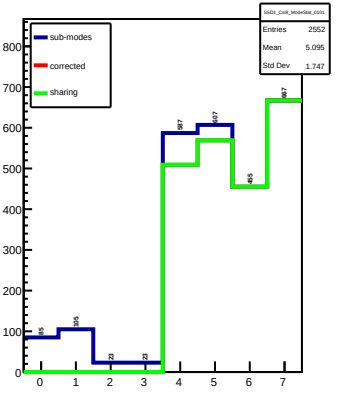
SSD1_CsI8_L2L3_Cuts_0101



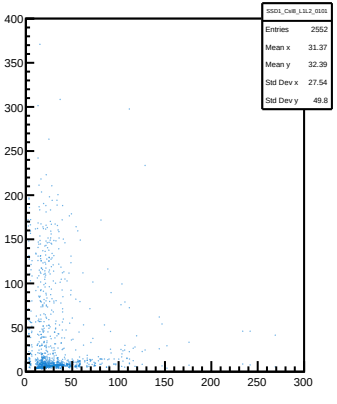
SSD1_CsI8_L2L3_Discard_0101



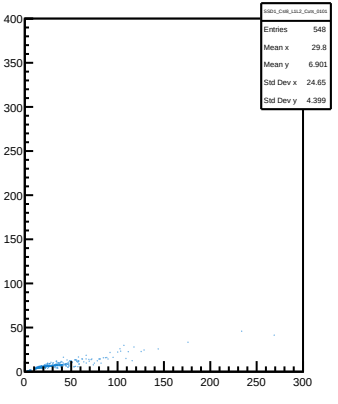
SSD1_CsI8_ModeStat_0101



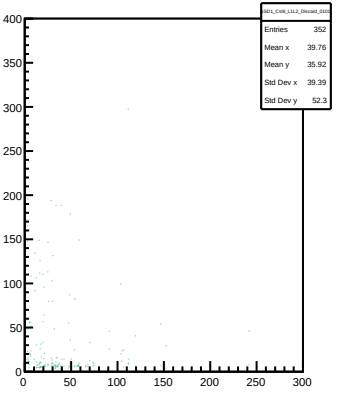
SSD1_CsI8_L1L2_0101



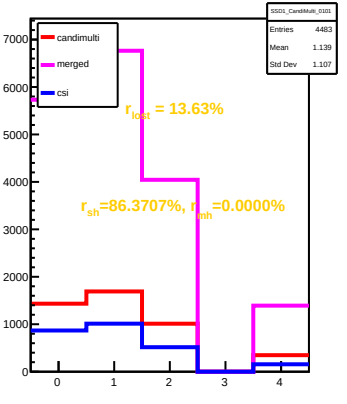
SSD1_CsI8_L1L2_Cuts_0101

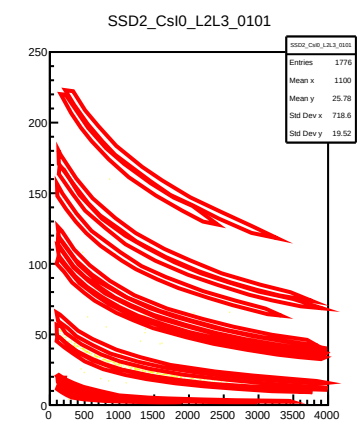


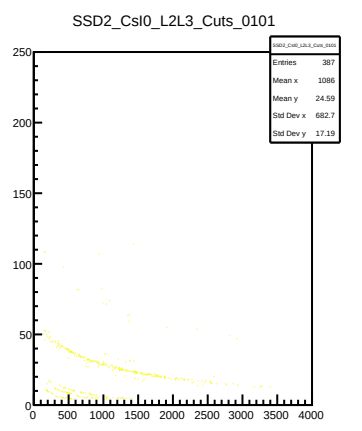
SSD1_CsI8_L1L2_Discard_0101

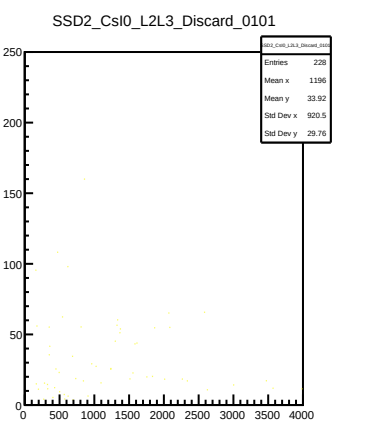


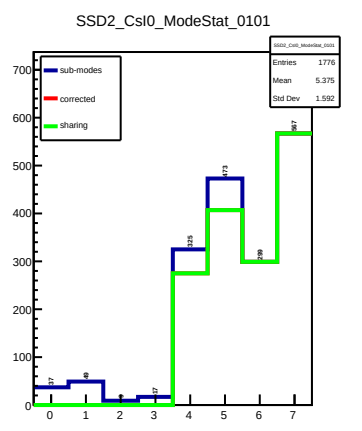
SSD1_CandiMulti_0101

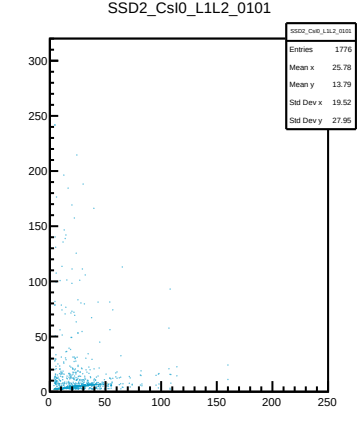


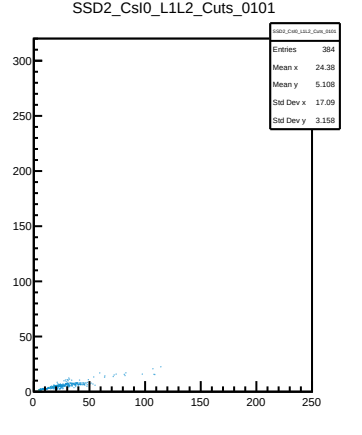

SSD2_CsI0_L2L3_0101
Entries 1776
Mean x 1100
Mean y 25.78
Std Dev x 718.6
Std Dev y 19.52

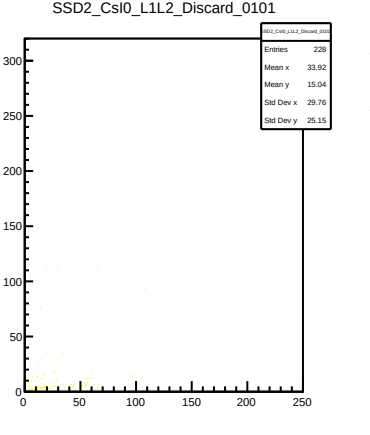

SSD2_CsI0_L2L3_Cuts_0101
Entries 387
Mean x 1086
Mean y 24.59
Std Dev x 682.7
Std Dev y 17.19

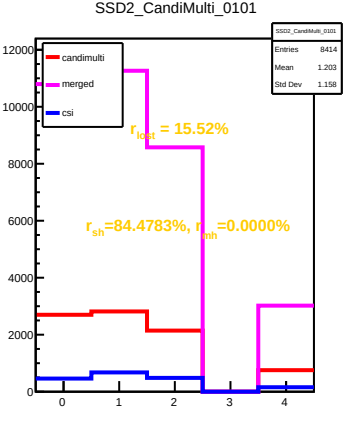

SSD2_CsI0_L2L3_Discard_0101
Entries 228
Mean x 1196
Mean y 33.92
Std Dev x 920.5
Std Dev y 29.76


SSD2_CsI0_ModeStat_0101
sub-modes
corrected
sharing
Entries 1776
Mean 5.375
Std Dev 1.592
37
49
8
17
225
473
289
567

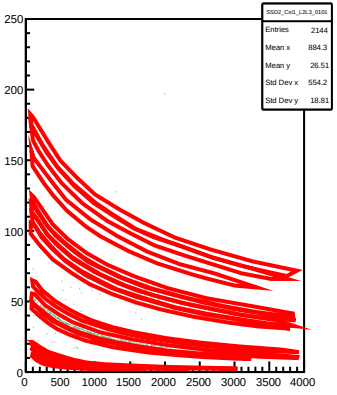

SSD2_CsI0_L1L2_0101
Entries 1776
Mean x 25.78
Mean y 13.79
Std Dev x 19.52
Std Dev y 27.95


SSD2_CsI0_L1L2_Cuts_0101
Entries 384
Mean x 24.38
Mean y 5.108
Std Dev x 17.09
Std Dev y 3.158

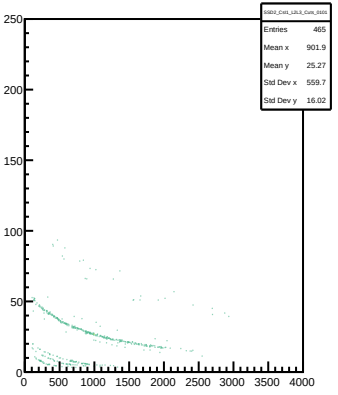

SSD2_CsI0_L1L2_Discard_0101
Entries 228
Mean x 33.92
Mean y 15.04
Std Dev x 29.76
Std Dev y 25.15


SSD2_CandiMulti_0101
candimulti
merged
csi
Entries 8414
Mean 1.203
Std Dev 1.158
r_leak = 15.52%
r_sh=84.4783%, r_mh=0.0000%

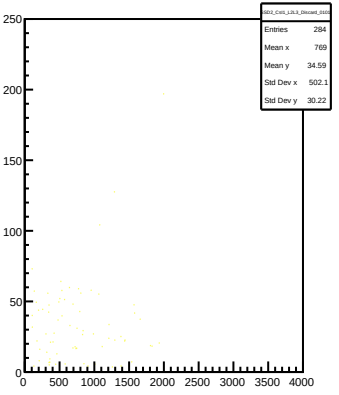
SSD2_CsI1_L2L3_0101



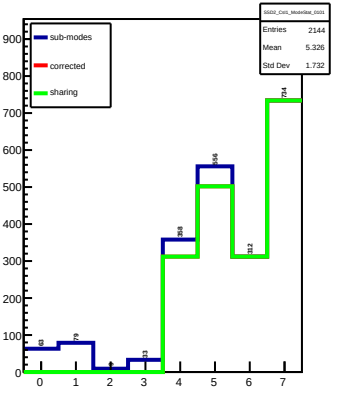
SSD2_CsI1_L2L3_Cuts_0101



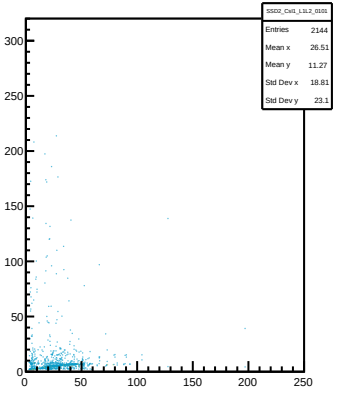
SSD2_CsI1_L2L3_Discard_0101



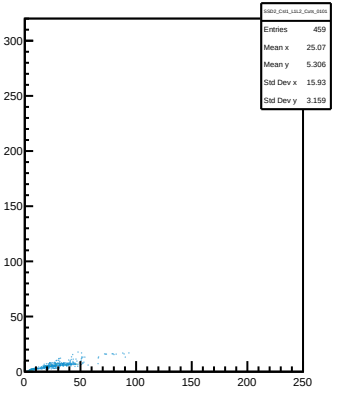
SSD2_CsI1_ModeStat_0101



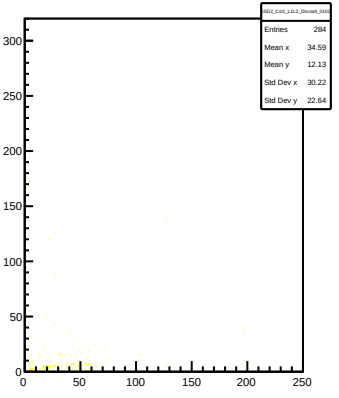
SSD2_CsI1_L1L2_0101



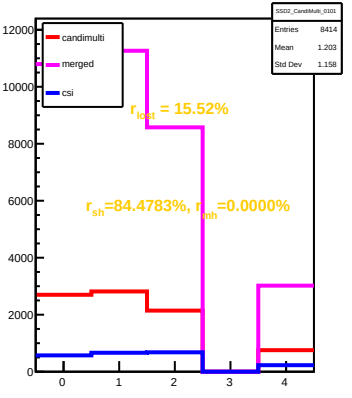
SSD2_CsI1_L1L2_Cuts_0101



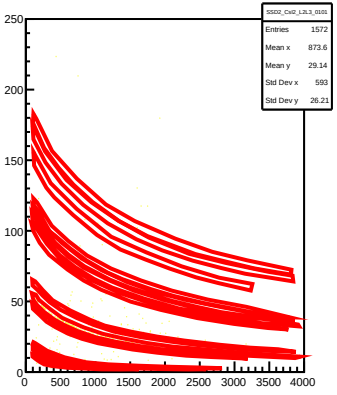
SSD2_CsI1_L1L2_Discard_0101



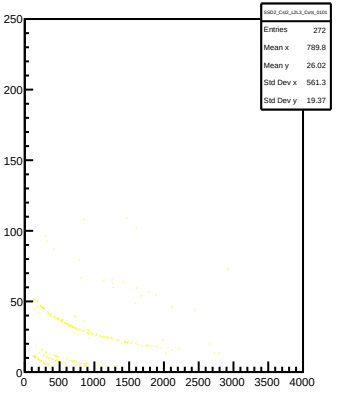
SSD2_CandiMulti_0101



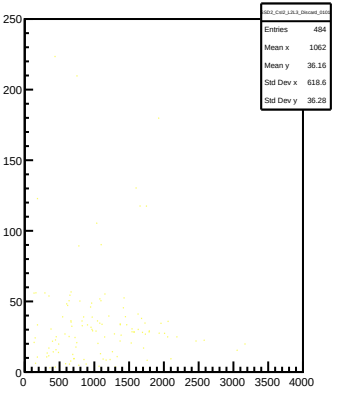
SSD2_CsI2_L2L3_0101



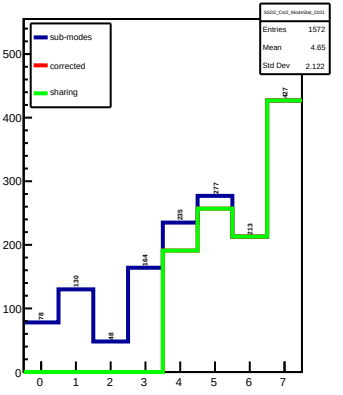
SSD2_CsI2_L2L3_Cuts_0101



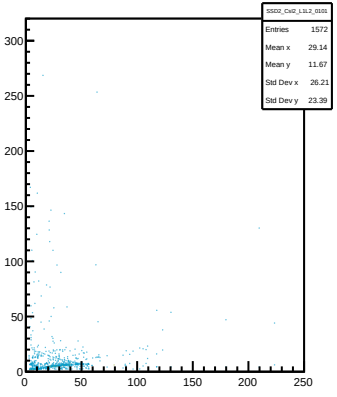
SSD2_CsI2_L2L3_Discard_0101



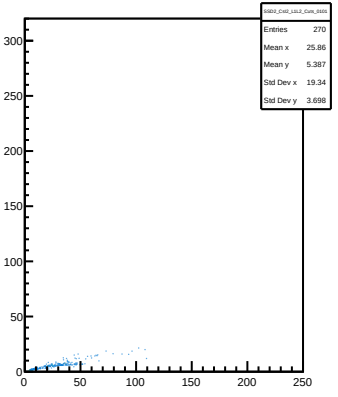
SSD2_CsI2_ModeStat_0101



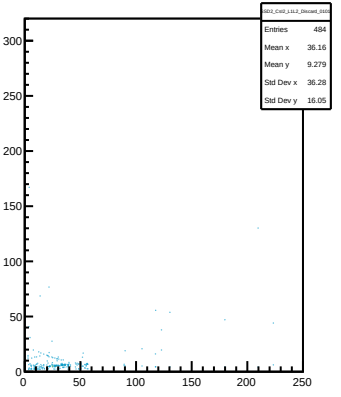
SSD2_CsI2_L1L2_0101



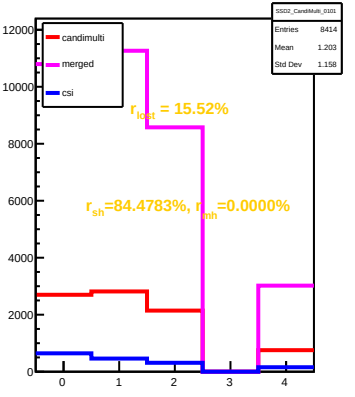
SSD2_CsI2_L1L2_Cuts_0101



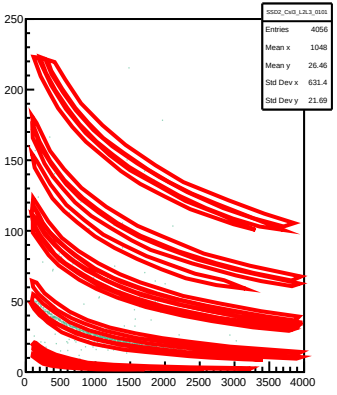
SSD2_CsI2_L1L2_Discard_0101



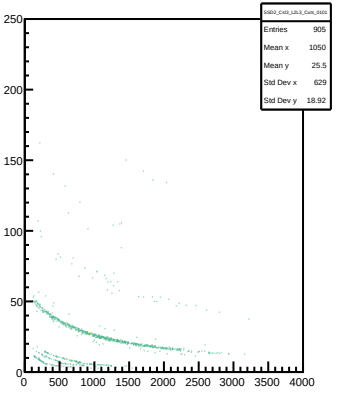
SSD2_CandiMulti_0101



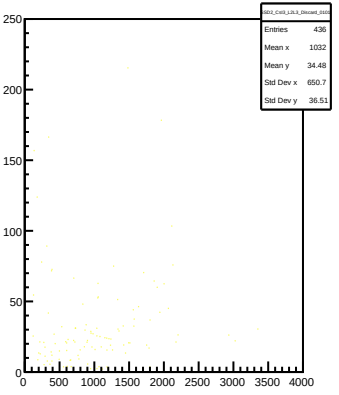
SSD2_CsI3_L2L3_0101



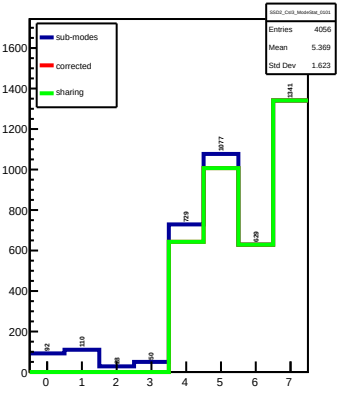
SSD2_CsI3_L2L3_Cuts_0101



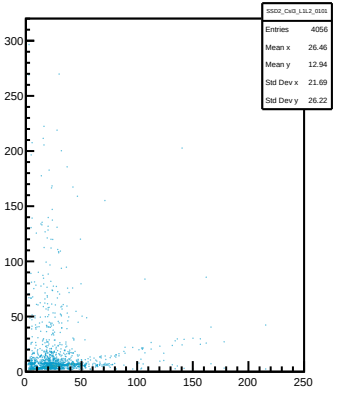
SSD2_CsI3_L2L3_Discard_0101



SSD2_CsI3_ModeStat_0101



SSD2_CsI3_L1L2_0101



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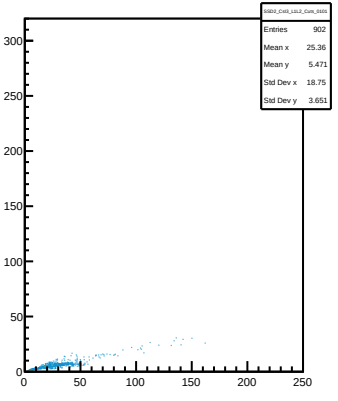

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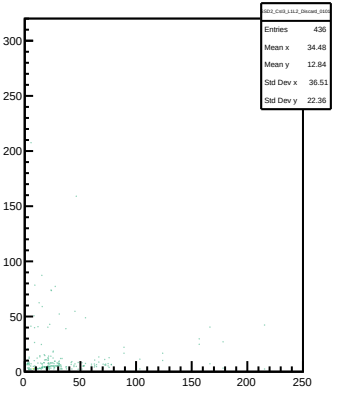
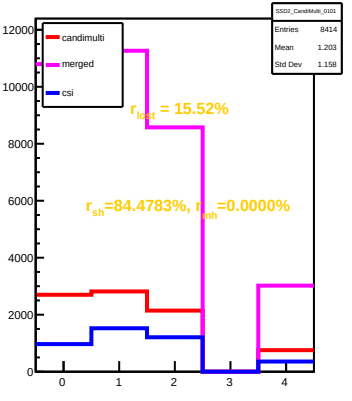
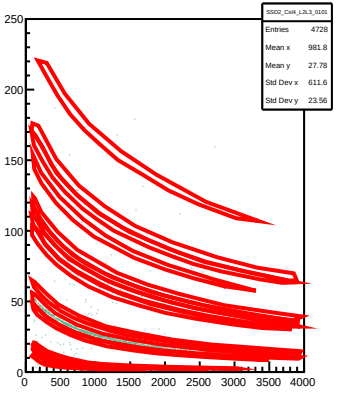


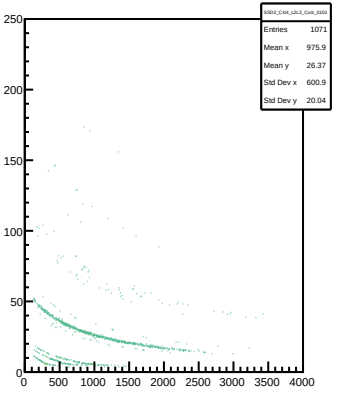
SSD2_CandiMulti_0101



SSD2_CsI4_L2L3_0101



SSD2_CsI4_L2L3_Cuts_0101



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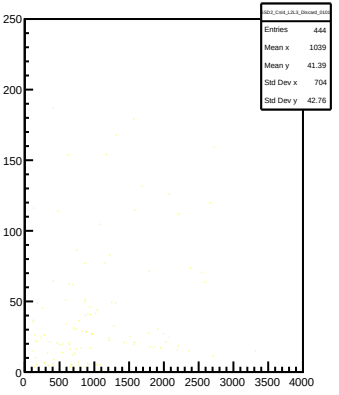

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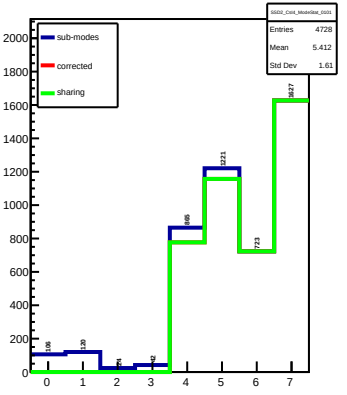

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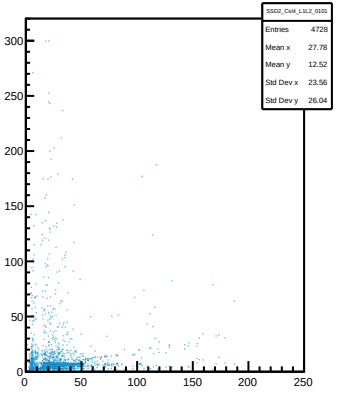
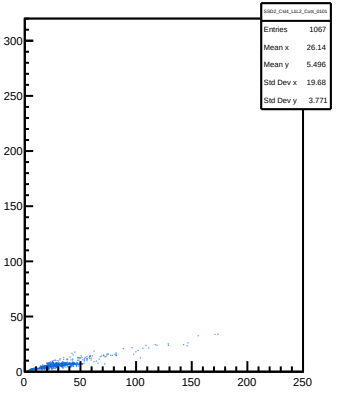
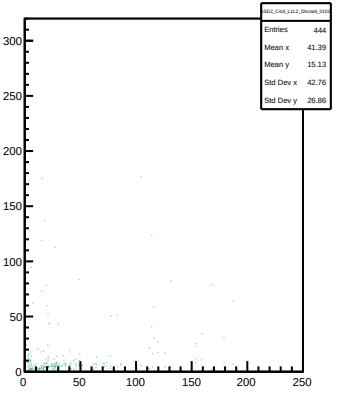


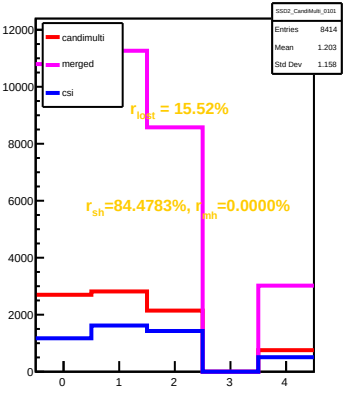
SSD2_CsI4_L1L2_Cuts_0101



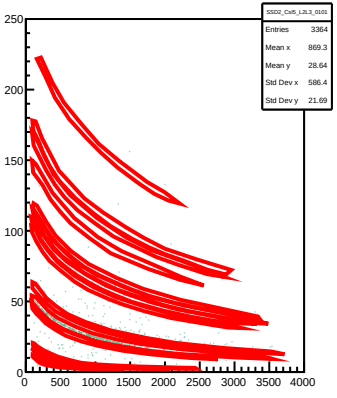
SSD2_CsI4_L1L2_Discard_0101



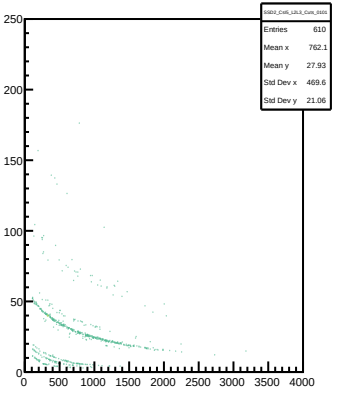
SSD2_CandiMulti_0101



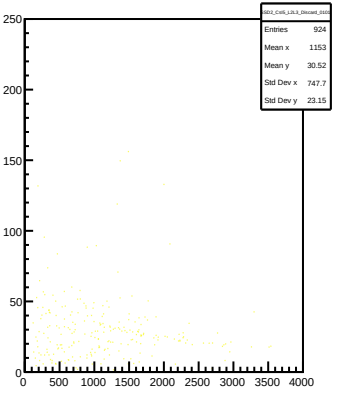
SSD2_CsI5_L2L3_0101



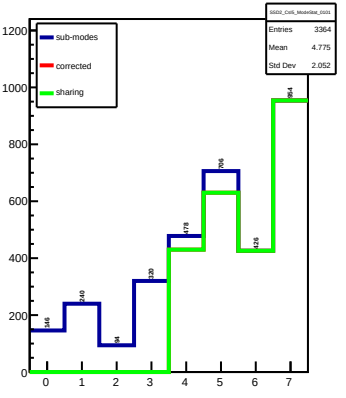
SSD2_CsI5_L2L3_Cuts_0101



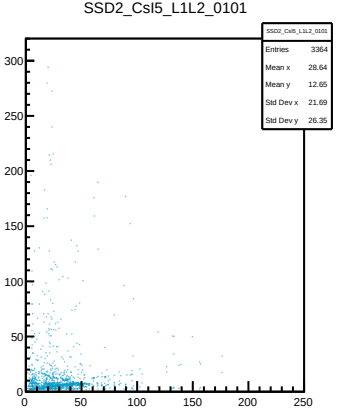
SSD2_CsI5_L2L3_Discard_0101



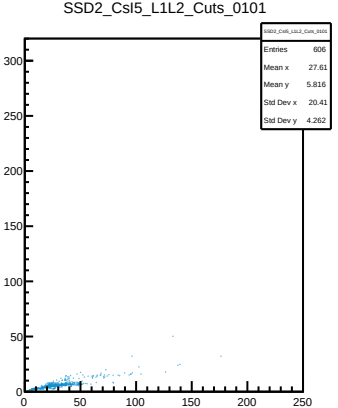
SSD2_CsI5_ModeStat_0101



SSD2_CsI5_L1L2_0101



SSD2_CsI5_L1L2_Cuts_0101



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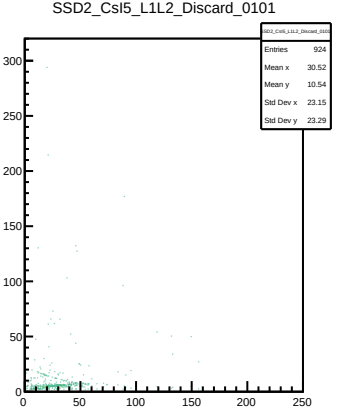
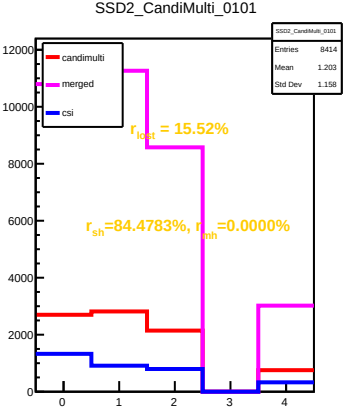


SSD2_CandiMulti_0101



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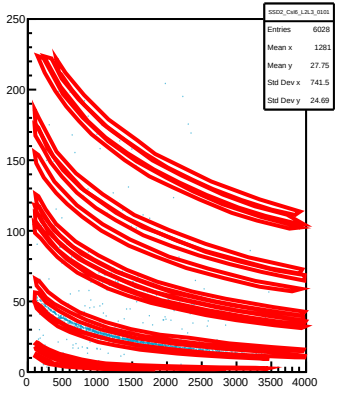
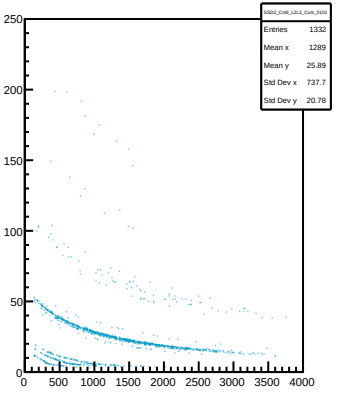
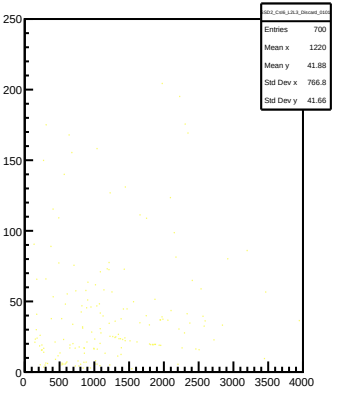


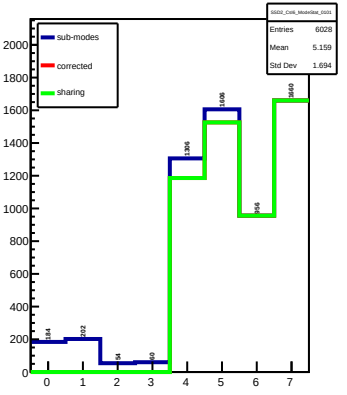
SSD2_CsI6_L2L3_Cuts_0101



SSD2_CsI6_L2L3_Discard_0101



SSD2_CsI6_ModeStat_0101



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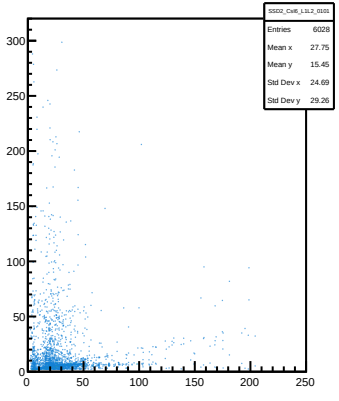
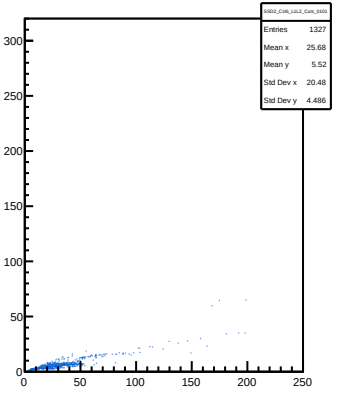


SSD2_CsI6_L1L2_Cuts_0101



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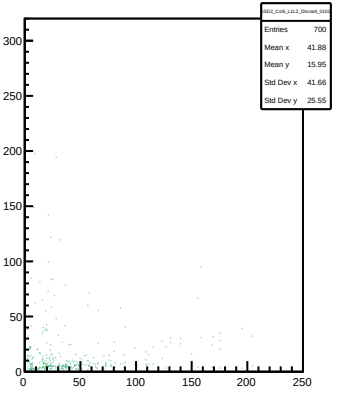
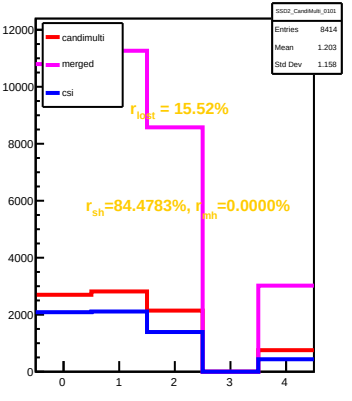


SSD2_CandiMulti_0101



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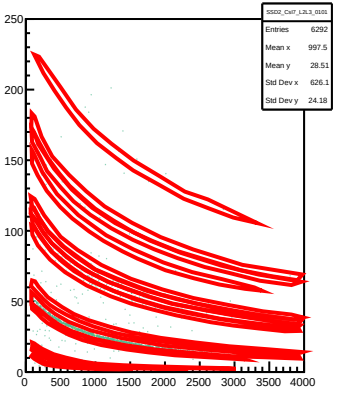
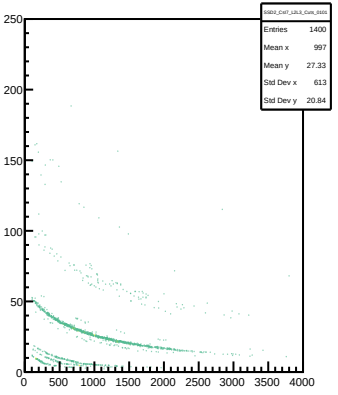
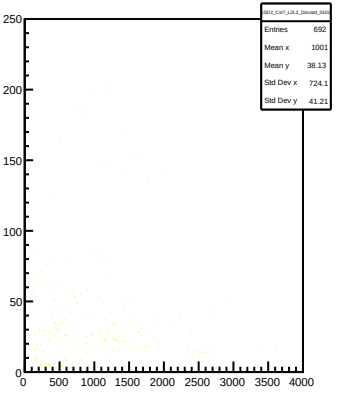


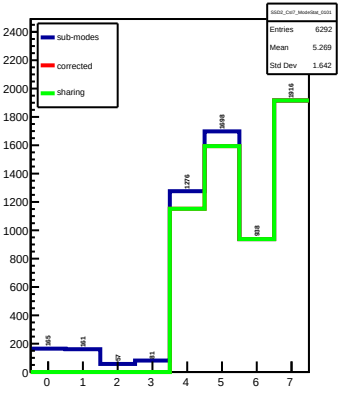
SSD2_CsI7_L2L3_Cuts_0101



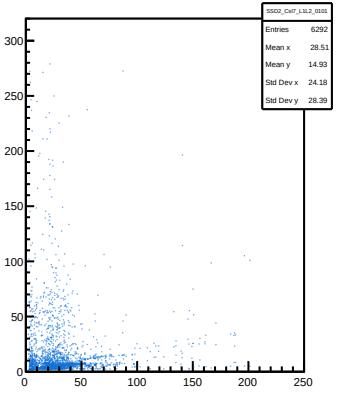
SSD2_CsI7_L2L3_Discard_0101



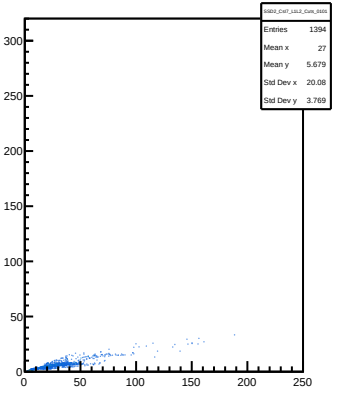
SSD2_CsI7_ModeStat_0101



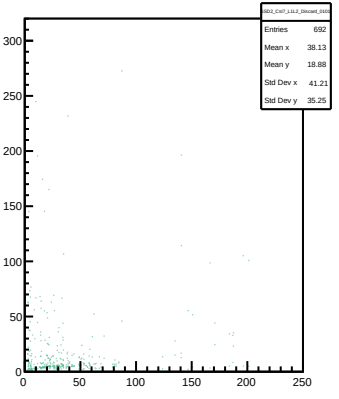
SSD2_CsI7_L1L2_0101



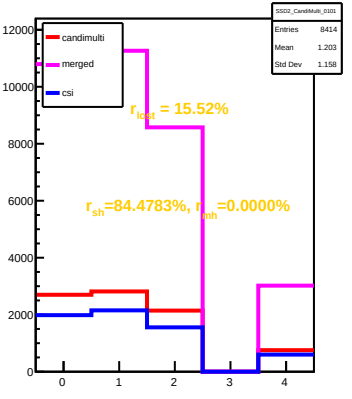
SSD2_CsI7_L1L2_Cuts_0101



SSD2_CsI7_L1L2_Discard_0101



SSD2_CandiMulti_0101



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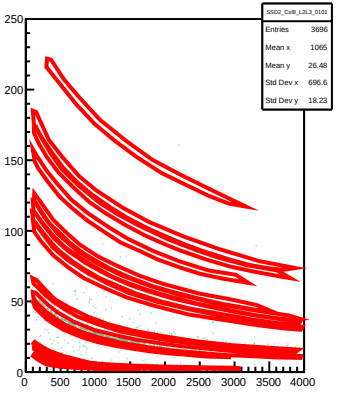
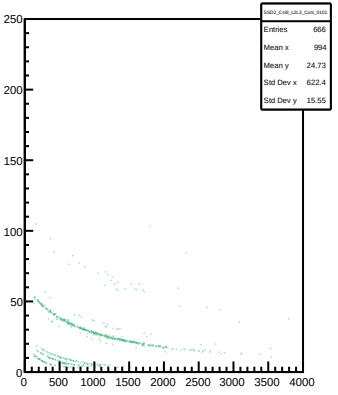
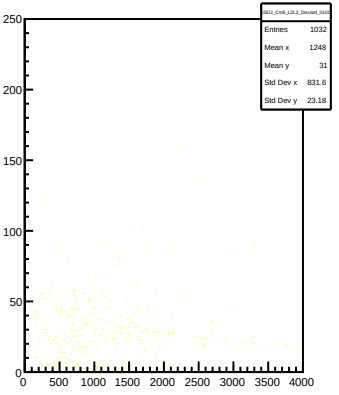


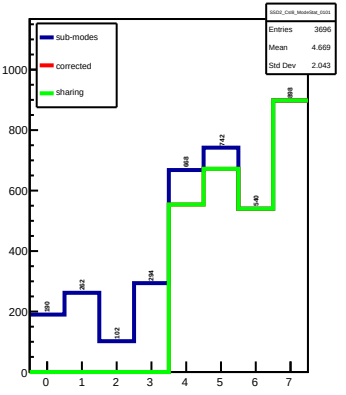
SSD2_CsI8_L2L3_Cuts_0101



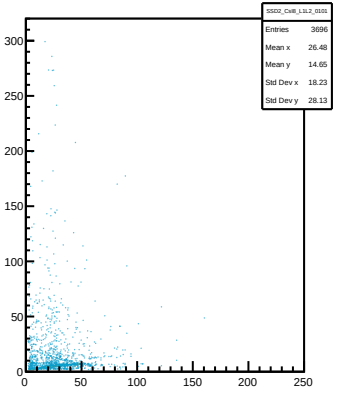
SSD2_CsI8_L2L3_Discard_0101



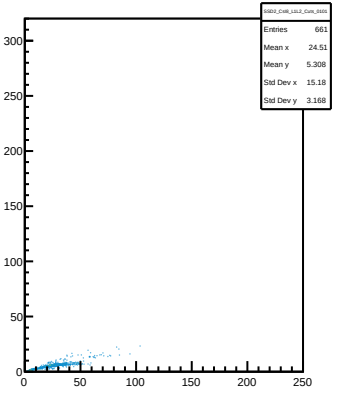
SSD2_CsI8_ModeStat_0101



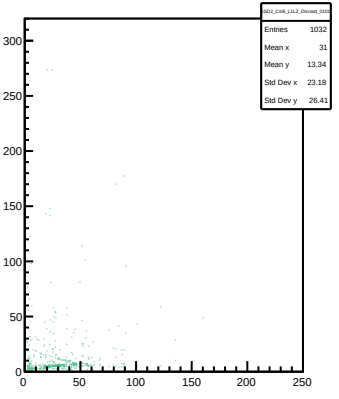
SSD2_CsI8_L1L2_0101



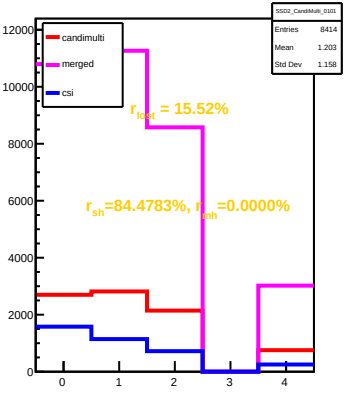
SSD2_CsI8_L1L2_Cuts_0101



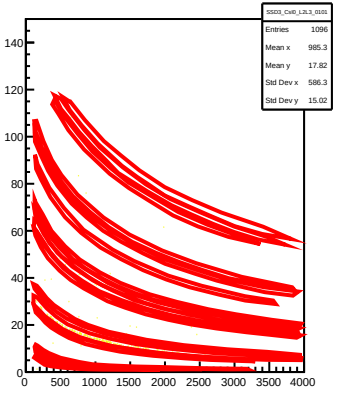
SSD2_CsI8_L1L2_Discard_0101



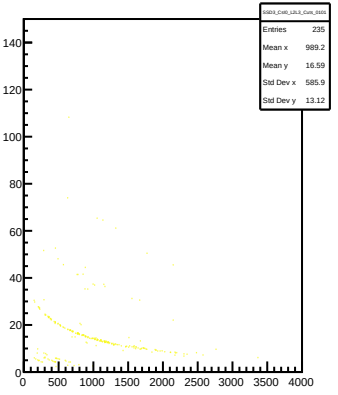
SSD2_CandiMulti_0101



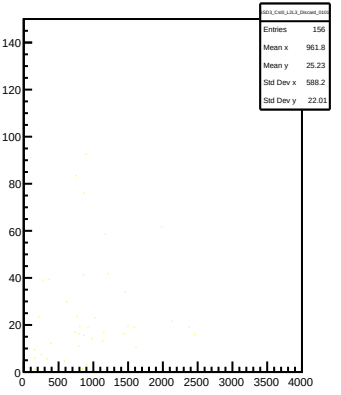
SSD3_CsI0_L2L3_0101



SSD3_CsI0_L2L3_Cuts_0101



SSD3_CsI0_L2L3_Discard_0101



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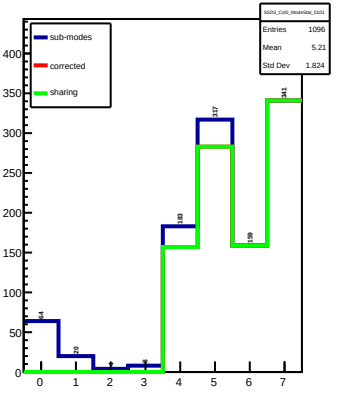

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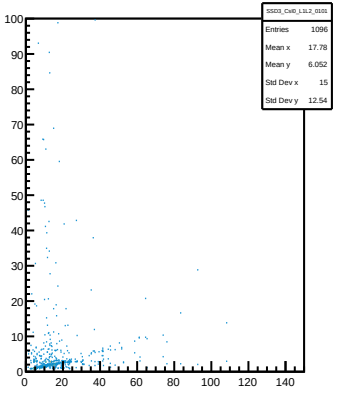

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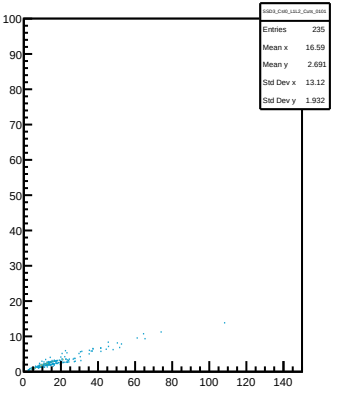

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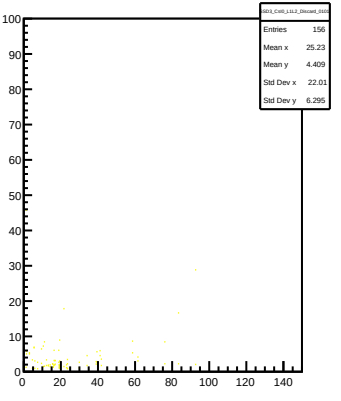
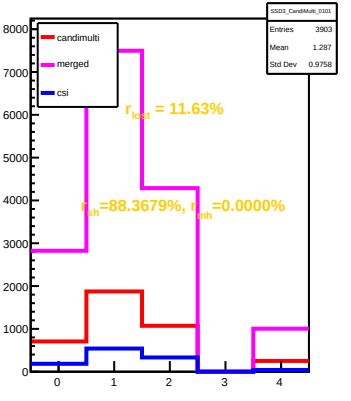


SSD3_CandiMulti_0101



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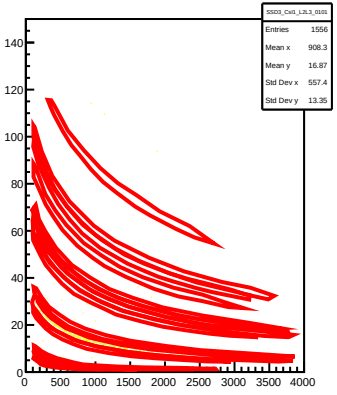

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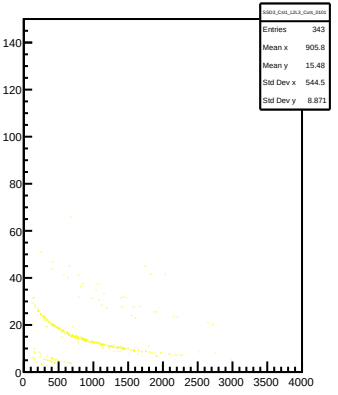

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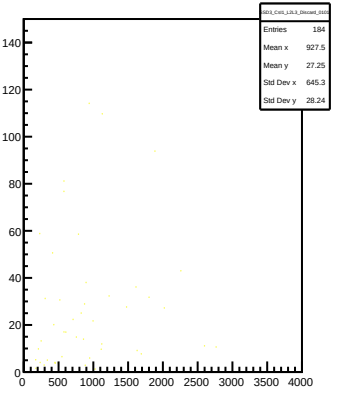

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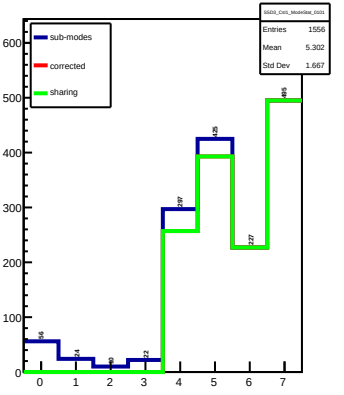

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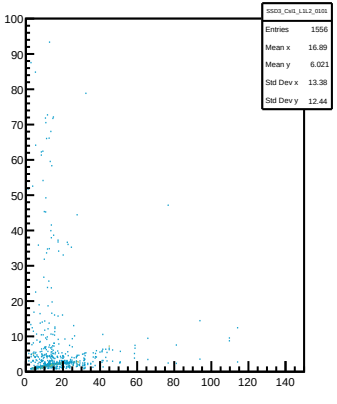

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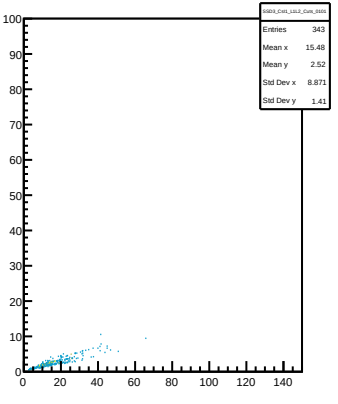
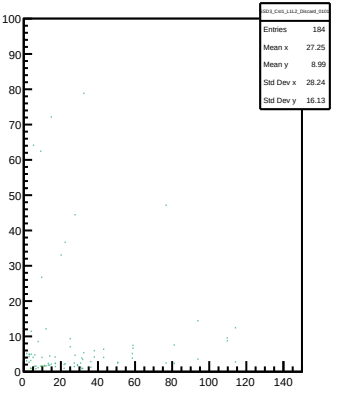


SSD3_CsI1_L1L2_Discard_0101



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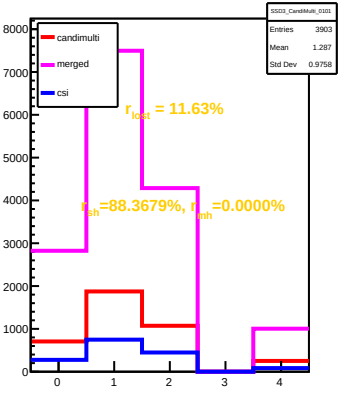

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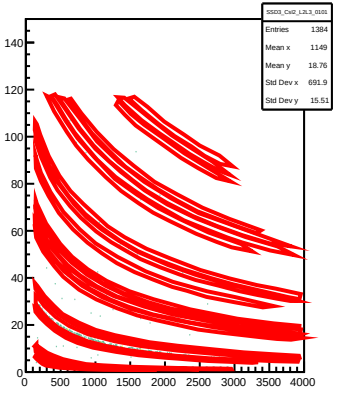
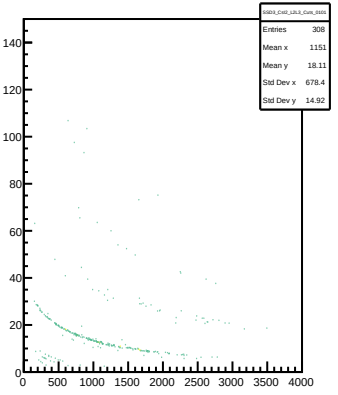


SSD3_CsI2_L2L3_Cuts_0101



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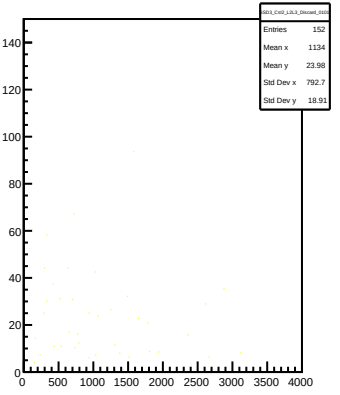

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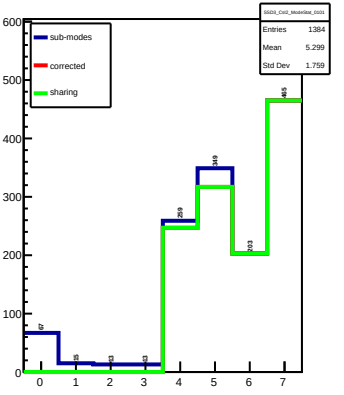

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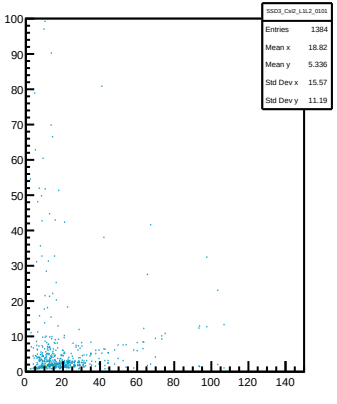

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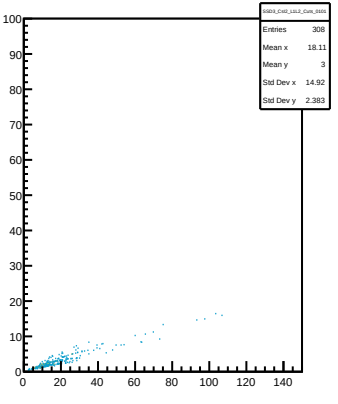

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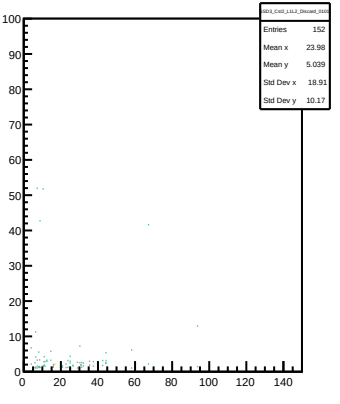

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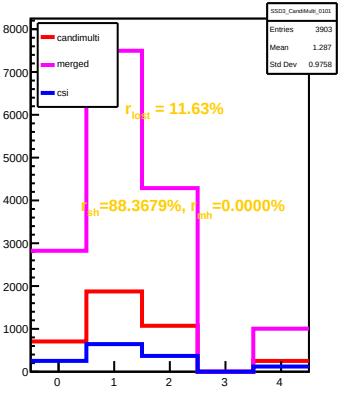

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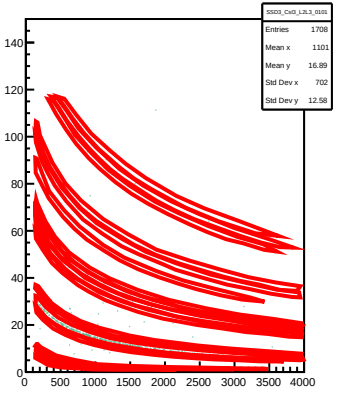
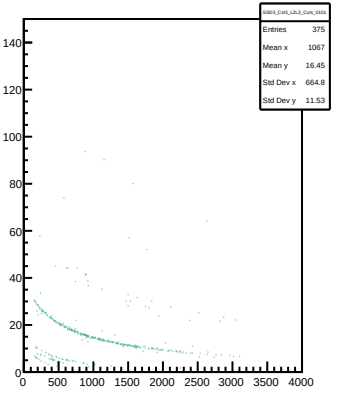


SSD3_CsI3_L2L3_Cuts_0101



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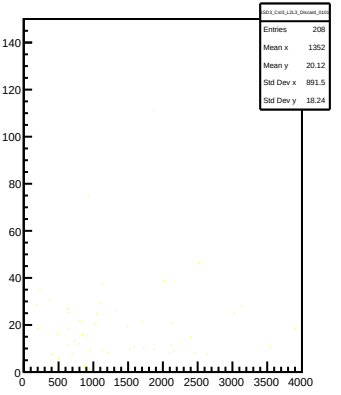

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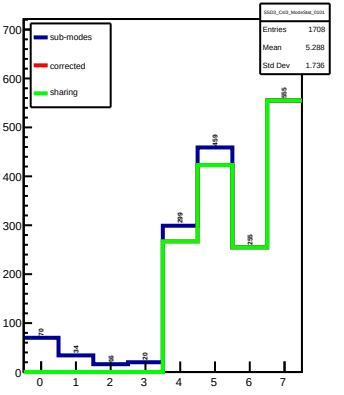

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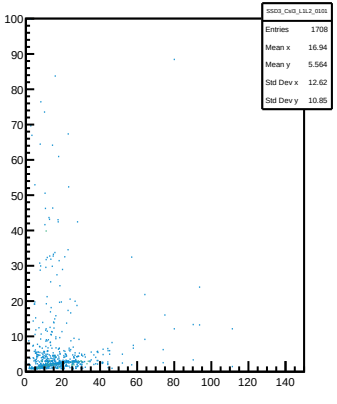
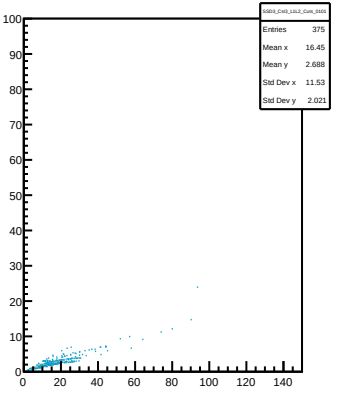
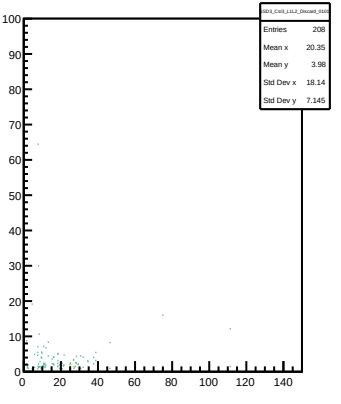


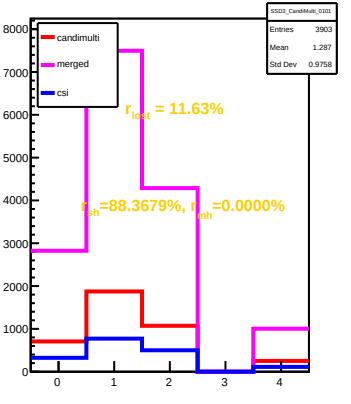
SSD3_CsI3_L1L2_Cuts_0101



SSD3_CsI3_L1L2_Discard_0101



SSD3_CandiMulti_0101



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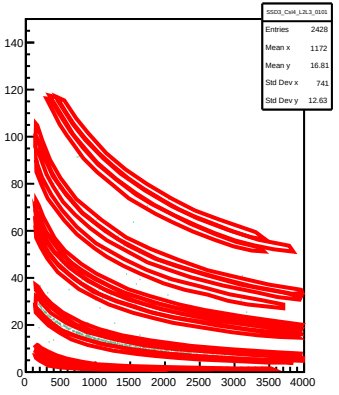
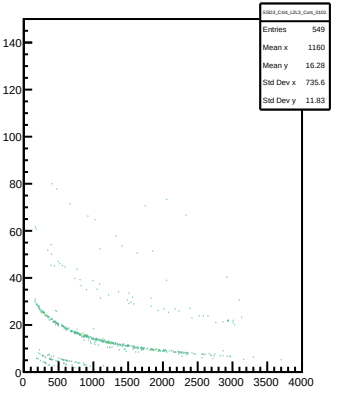
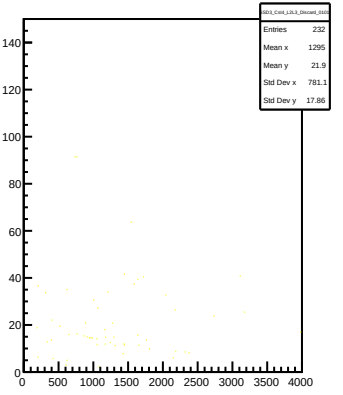


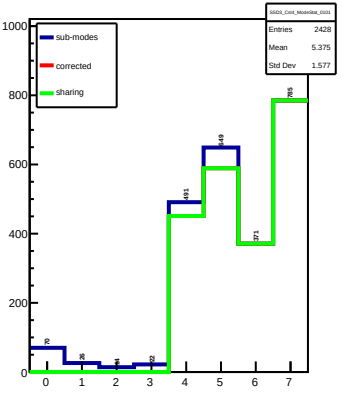
SSD3_CsI4_L2L3_Cuts_0101



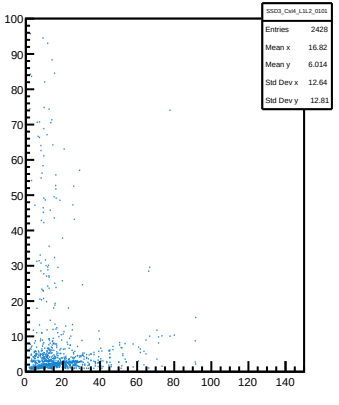
SSD3_CsI4_L2L3_Discard_0101



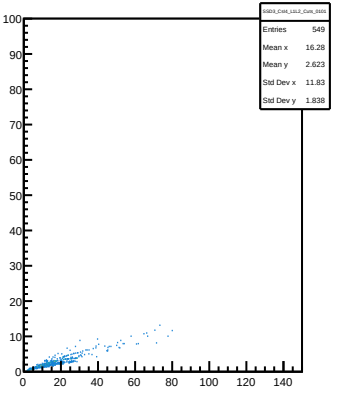
SSD3_CsI4_ModeStat_0101



SSD3_CsI4_L1L2_0101



SSD3_CsI4_L1L2_Cuts_0101



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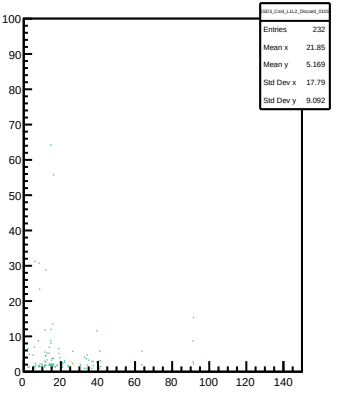

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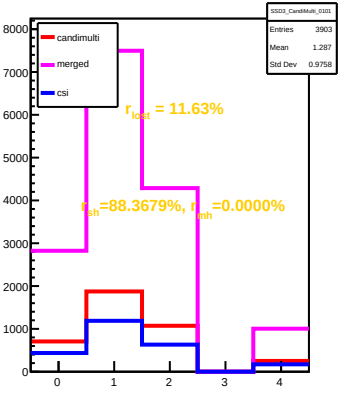
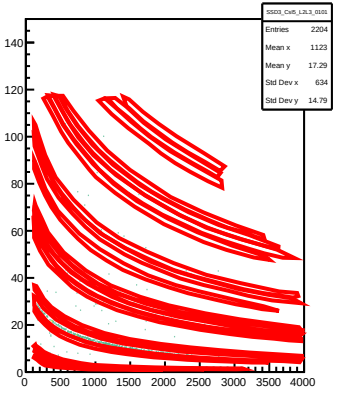
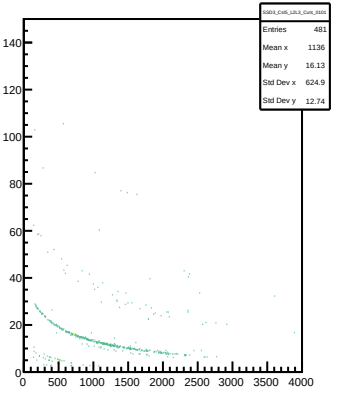


SSD3_CsI5_L2L3_0101



SSD3_CsI5_L2L3_Cuts_0101



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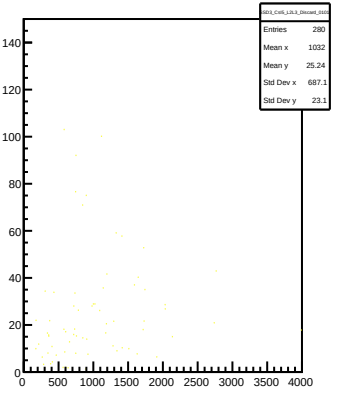
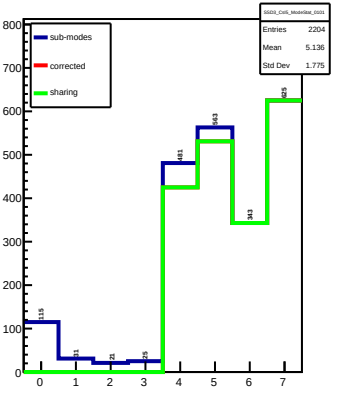
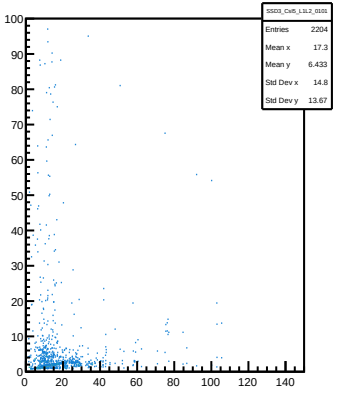


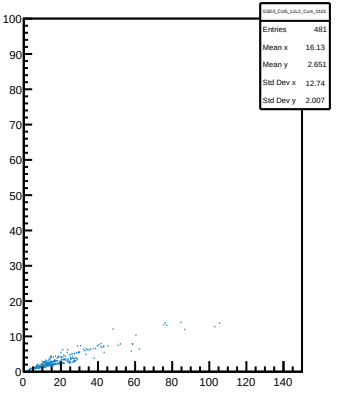
SSD3_CsI5_ModeStat_0101



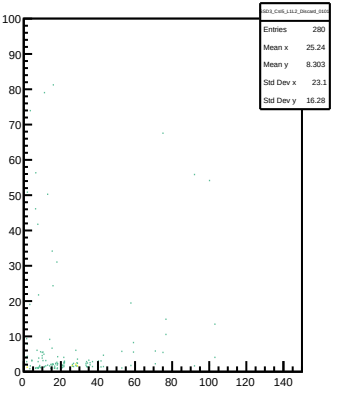
SSD3_CsI5_L1L2_0101



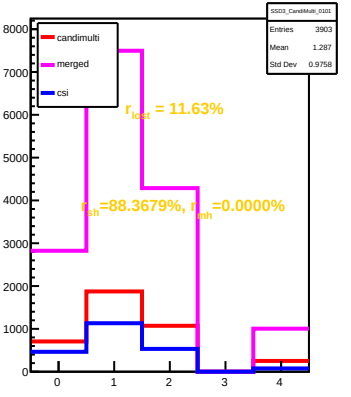
SSD3_CsI5_L1L2_Cuts_0101



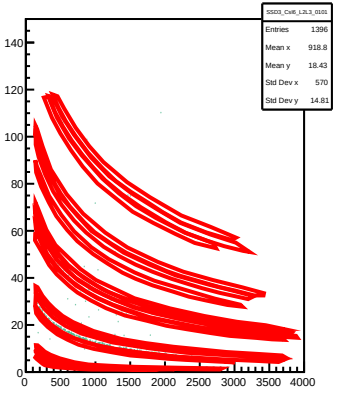
SSD3_CsI5_L1L2_Discard_0101



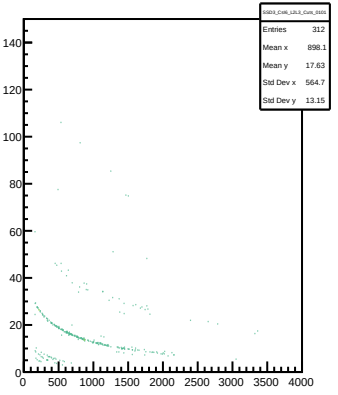
SSD3_CandiMulti_0101



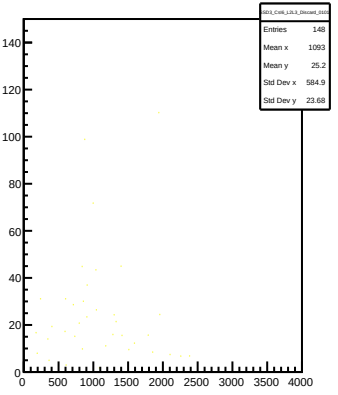
SSD3_CsI6_L2L3_0101



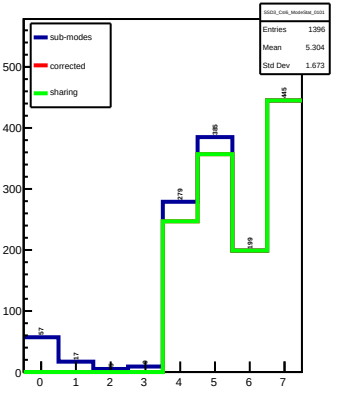
SSD3_CsI6_L2L3_Cuts_0101



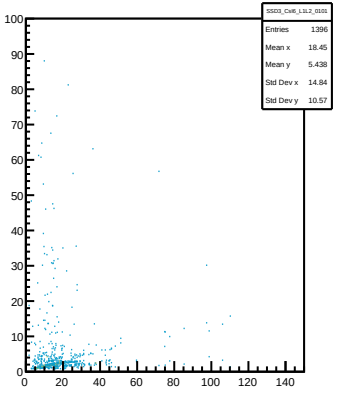
SSD3_CsI6_L2L3_Discard_0101



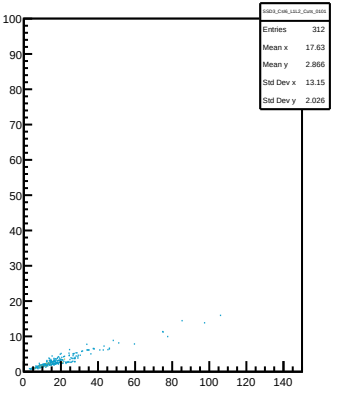
SSD3_CsI6_ModeStat_0101



SSD3_CsI6_L1L2_0101



SSD3_CsI6_L1L2_Cuts_0101



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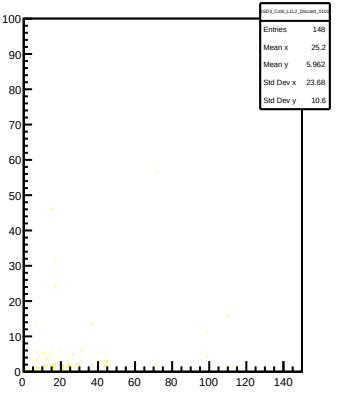
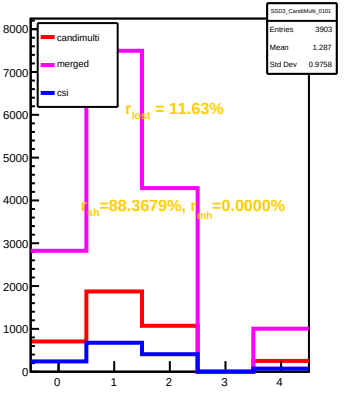
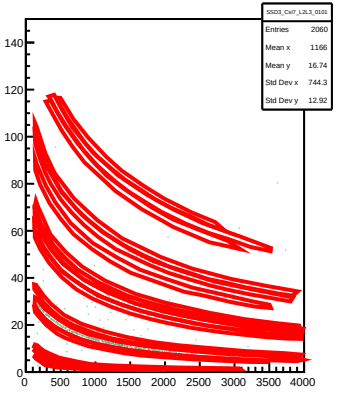


SSD3_CandiMulti_0101



SSD3_CsI7_L2L3_0101



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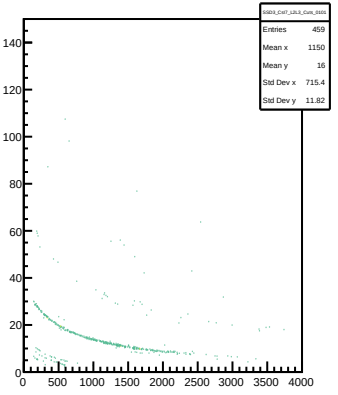
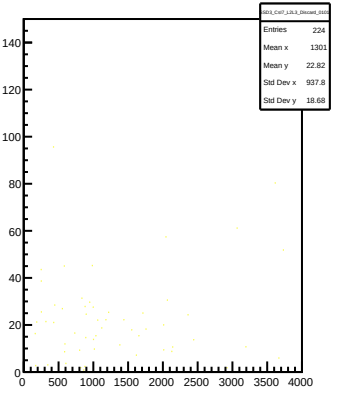
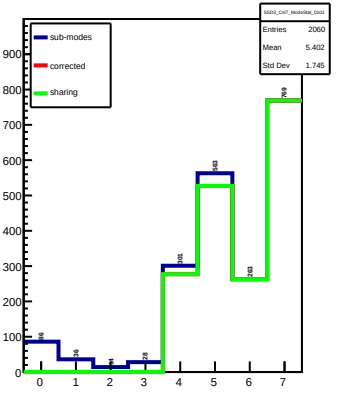


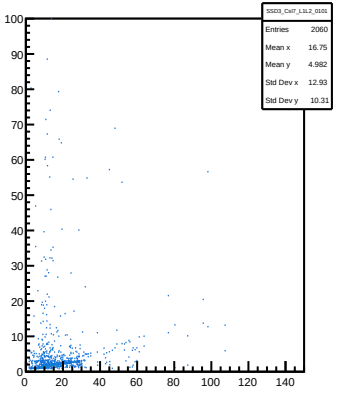
SSD3_CsI7_L2L3_Discard_0101



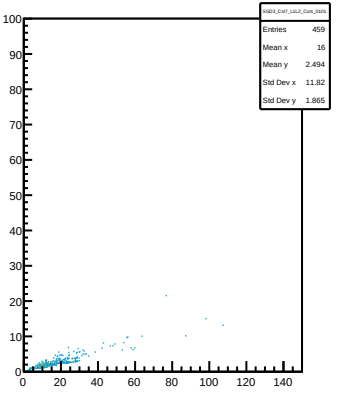
SSD3_CsI7_ModeStat_0101



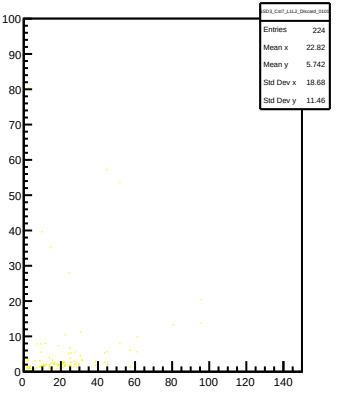
SSD3_CsI7_L1L2_0101



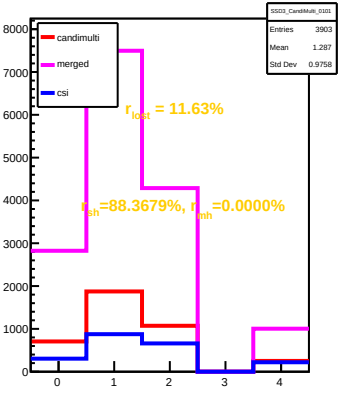
SSD3_CsI7_L1L2_Cuts_0101



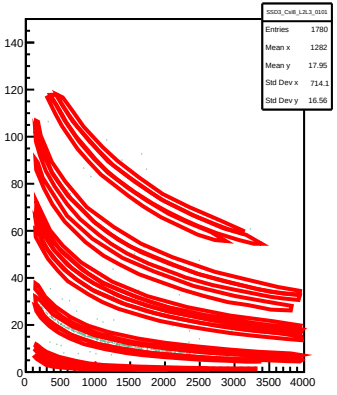
SSD3_CsI7_L1L2_Discard_0101



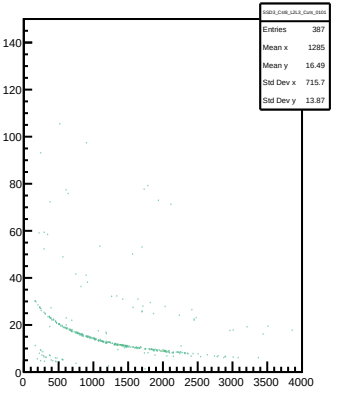
SSD3_CandiMulti_0101



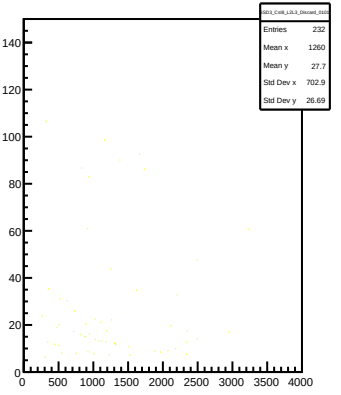
SSD3_CsI8_L2L3_0101



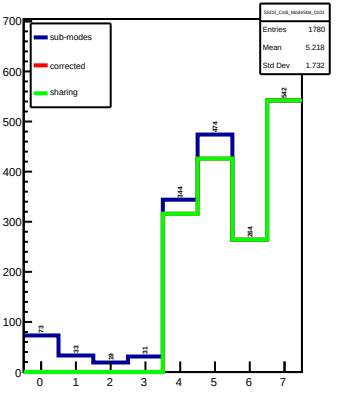
SSD3_CsI8_L2L3_Cuts_0101



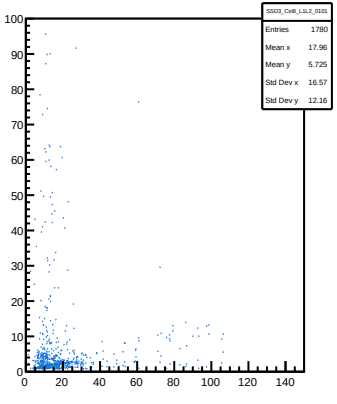
SSD3_CsI8_L2L3_Discard_0101



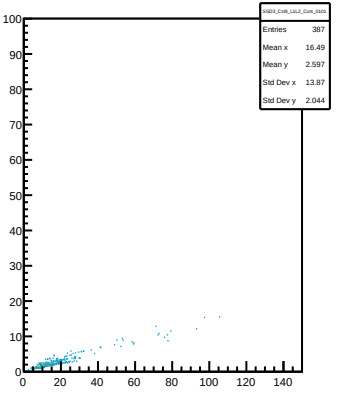
SSD3_CsI8_ModeStat_0101



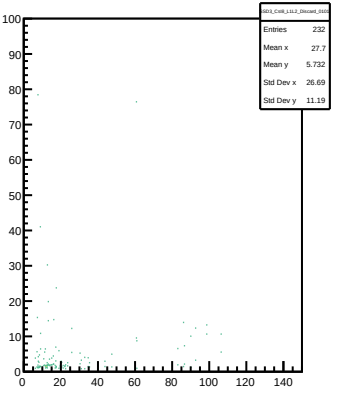
SSD3_CsI8_L1L2_0101



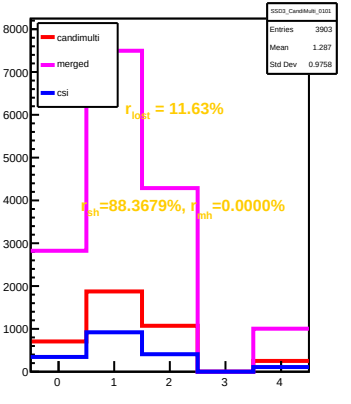
SSD3_CsI8_L1L2_Cuts_0101



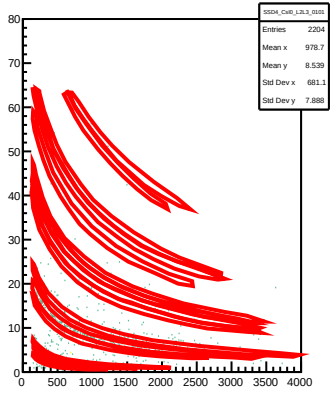
SSD3_CsI8_L1L2_Discard_0101



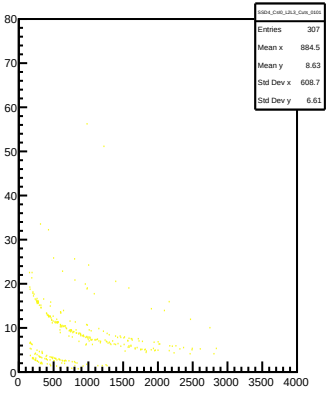
SSD3_CandiMulti_0101



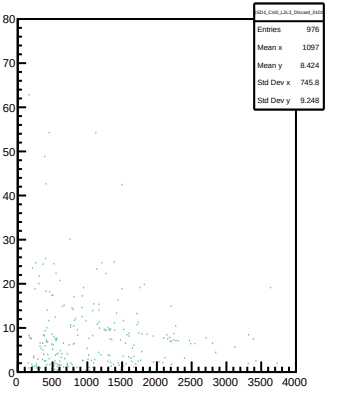
SSD4_CsI0_L2L3_0101



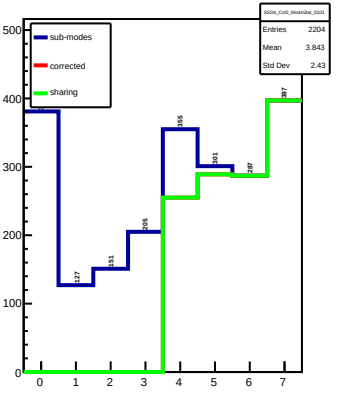
SSD4_CsI0_L2L3_Cuts_0101



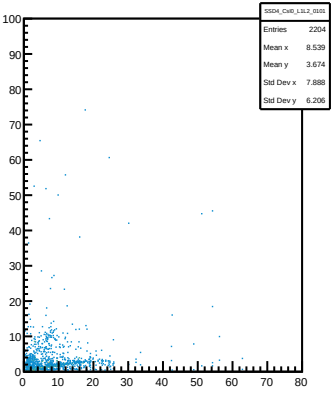
SSD4_CsI0_L2L3_Discard_0101



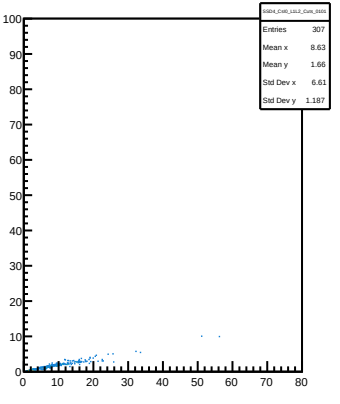
SSD4_CsI0_ModeStat_0101



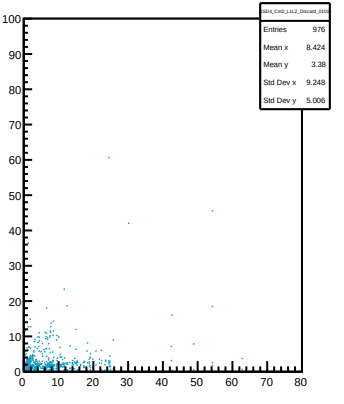
SSD4_CsI0_L1L2_0101



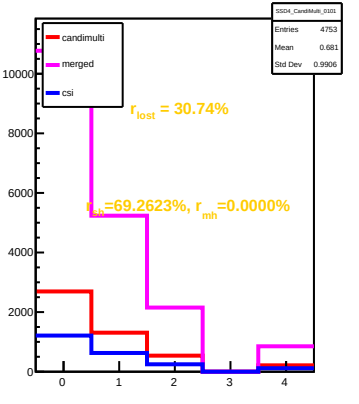
SSD4_CsI0_L1L2_Cuts_0101



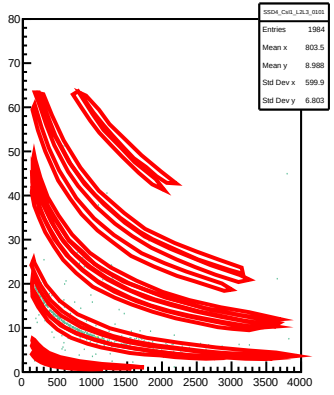
SSD4_CsI0_L1L2_Discard_0101



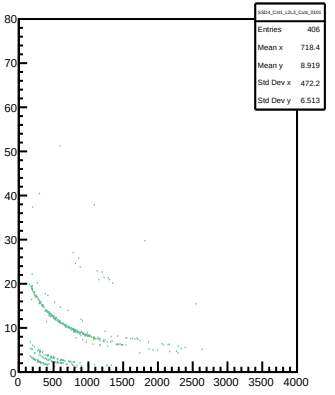
SSD4_CandiMulti_0101



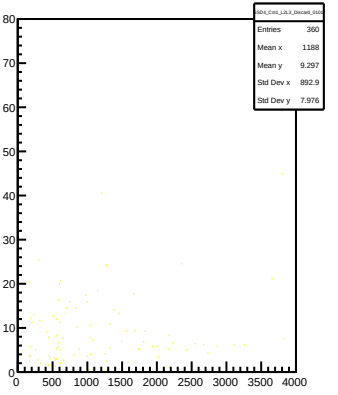
SSD4_CsI1_L2L3_0101



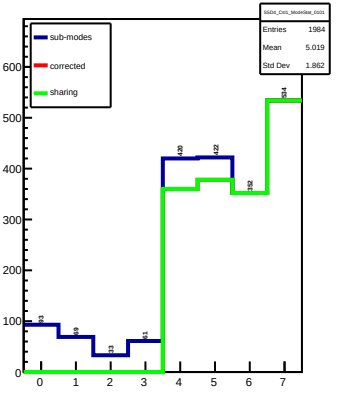
SSD4_CsI1_L2L3_Cuts_0101



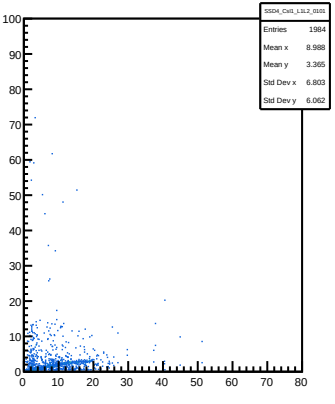
SSD4_CsI1_L2L3_Discard_0101



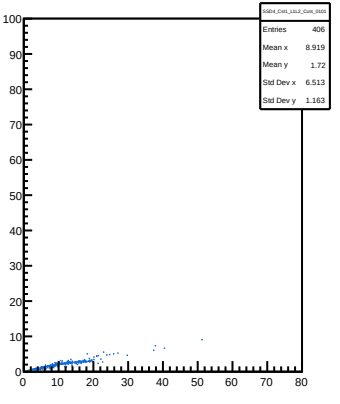
SSD4_CsI1_ModeStat_0101



SSD4_CsI1_L1L2_0101



SSD4_CsI1_L1L2_Cuts_0101



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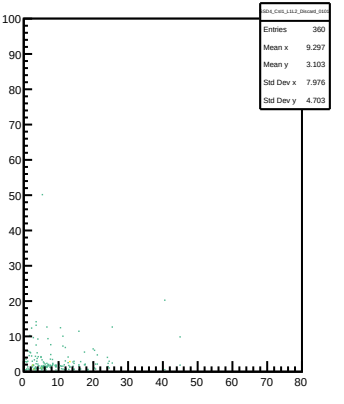
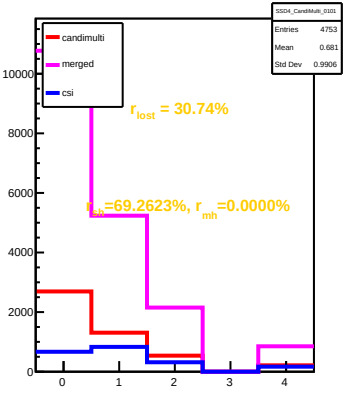
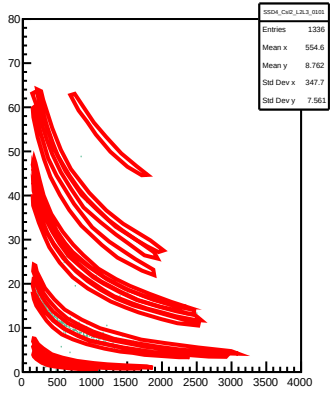


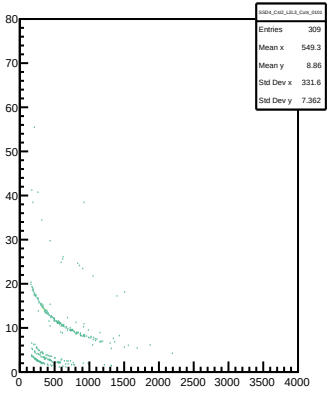
SSD4_CandiMulti_0101



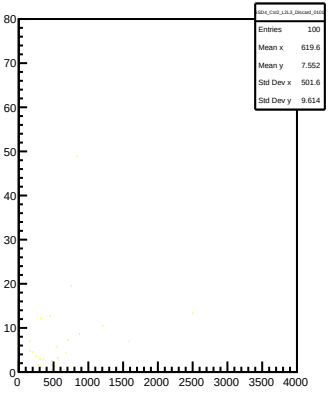
SSD4_CsI2_L2L3_0101



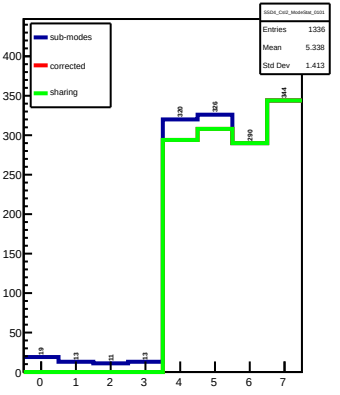
SSD4_CsI2_L2L3_Cuts_0101



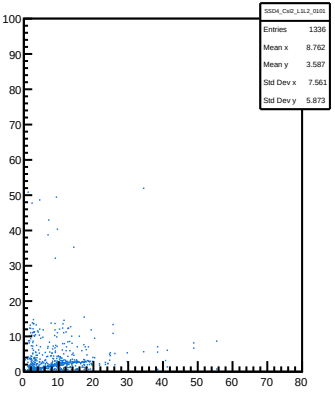
SSD4_CsI2_L2L3_Discard_0101



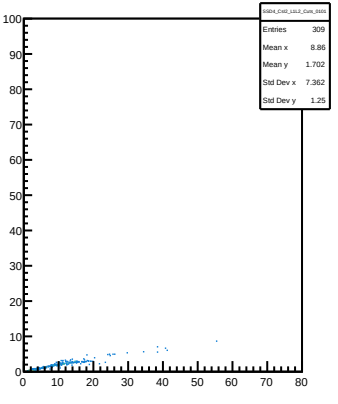
SSD4_CsI2_ModeStat_0101



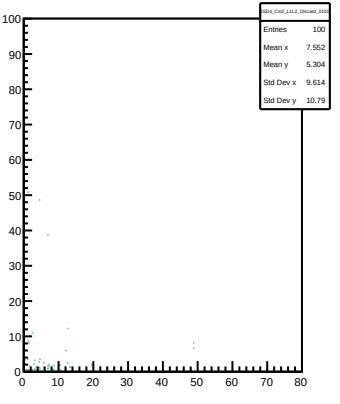
SSD4_CsI2_L1L2_0101



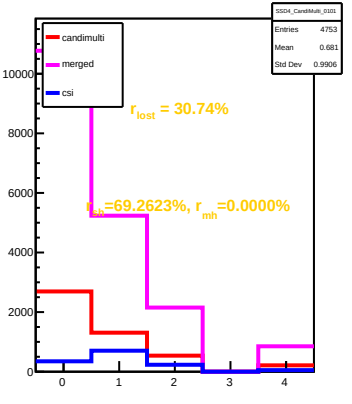
SSD4_CsI2_L1L2_Cuts_0101



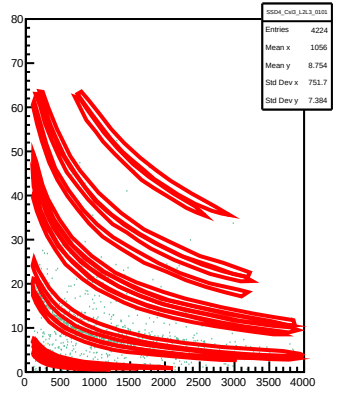
SSD4_CsI2_L1L2_Discard_0101



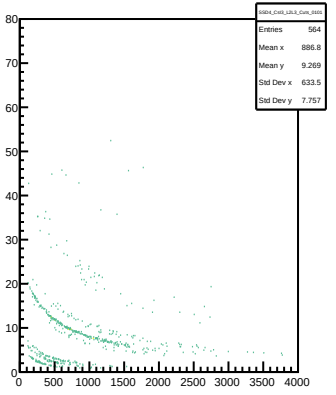
SSD4_CandiMulti_0101



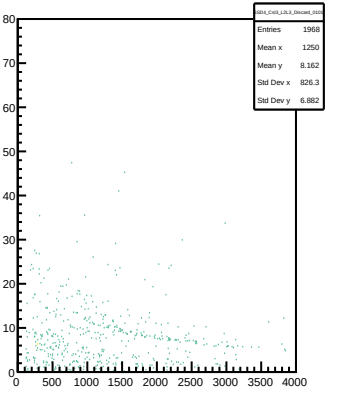
SSD4_CsI3_L2L3_0101



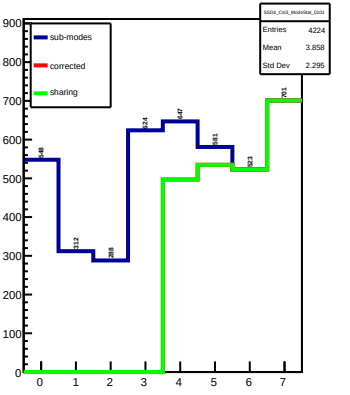
SSD4_CsI3_L2L3_Cuts_0101



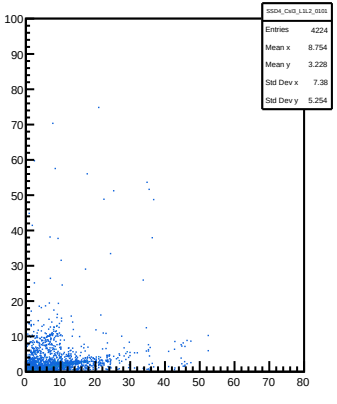
SSD4_CsI3_L2L3_Discard_0101



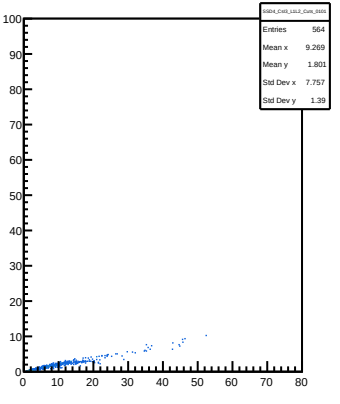
SSD4_CsI3_ModeStat_0101



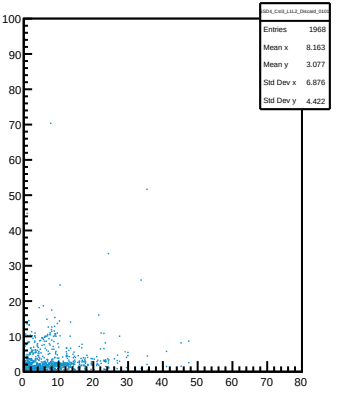
SSD4_CsI3_L1L2_0101



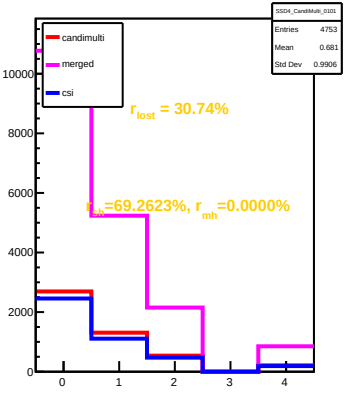
SSD4_CsI3_L1L2_Cuts_0101

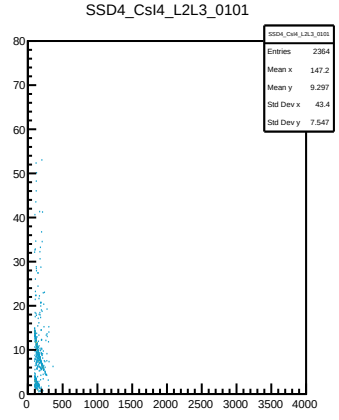


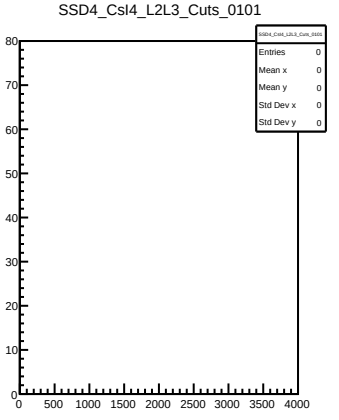
SSD4_CsI3_L1L2_Discard_0101

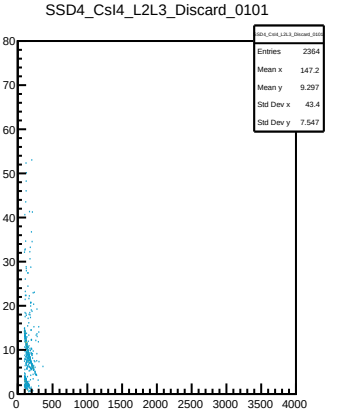


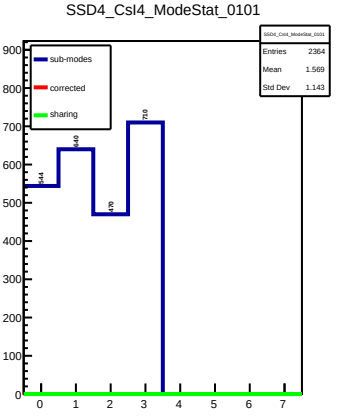
SSD4_CandiMulti_0101

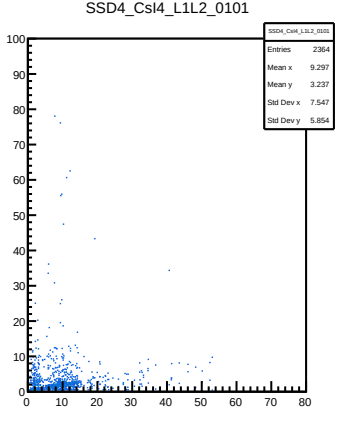


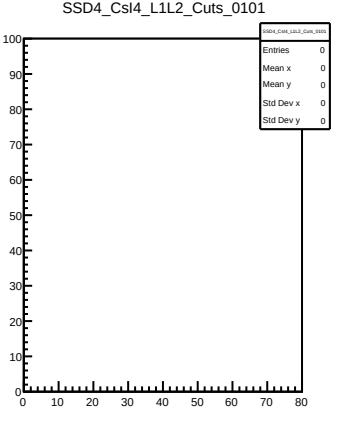

SSD4_CsI4_L2L3_0101
Entries 2364
Mean x 147.2
Mean y 9.297
Std Dev x 43.4
Std Dev y 7.547

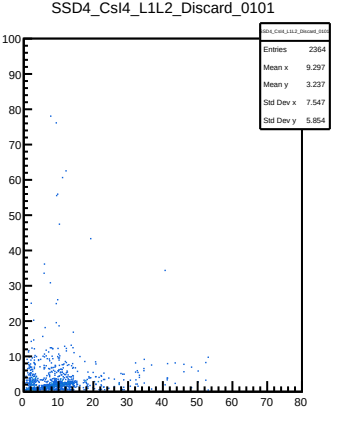

SSD4_CsI4_L2L3_Cuts_0101
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0

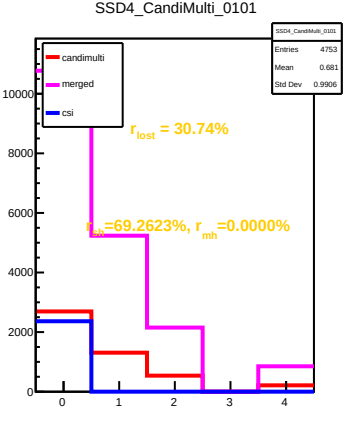

SSD4_CsI4_L2L3_Discard_0101
Entries 2364
Mean x 147.2
Mean y 9.297
Std Dev x 43.4
Std Dev y 7.547


SSD4_CsI4_ModeStat_0101
sub-modes
corrected
sharing
544
640
478
710
Entries 2364
Mean 1.569
Std Dev 1.143

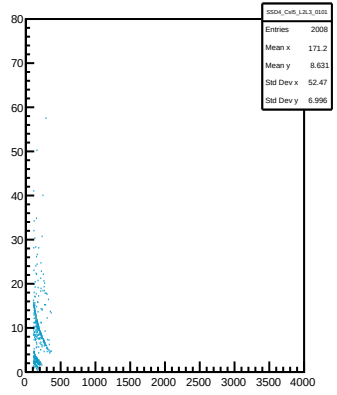

SSD4_CsI4_L1L2_0101
Entries 2364
Mean x 9.297
Mean y 3.237
Std Dev x 7.547
Std Dev y 5.854


SSD4_CsI4_L1L2_Cuts_0101
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0

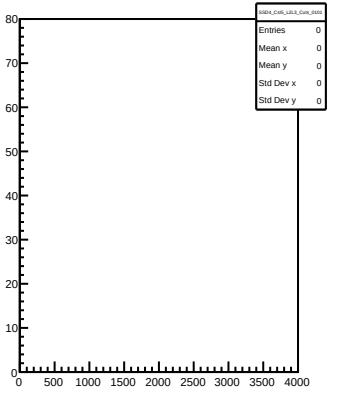

SSD4_CsI4_L1L2_Discard_0101
Entries 2364
Mean x 9.297
Mean y 3.237
Std Dev x 7.547
Std Dev y 5.854


SSD4_CandiMulti_0101
candimulti
merged
csi
r_lost = 30.74%
r_ms=69.2623%, r_mh=0.0000%
Entries 4753
Mean 0.681
Std Dev 0.9906

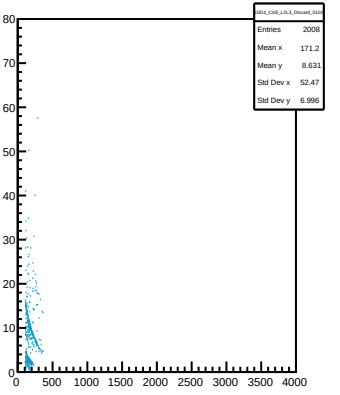
SSD4_CsI5_L2L3_0101



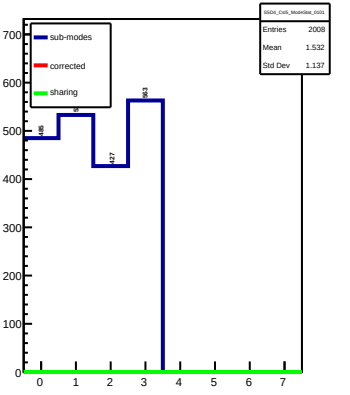
SSD4_CsI5_L2L3_Cuts_0101



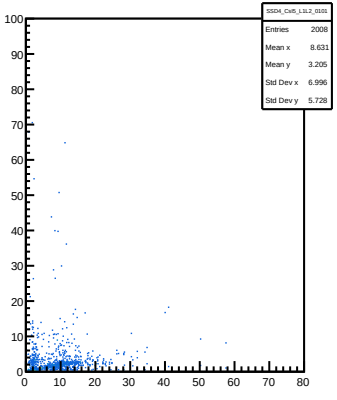
SSD4_CsI5_L2L3_Discard_0101



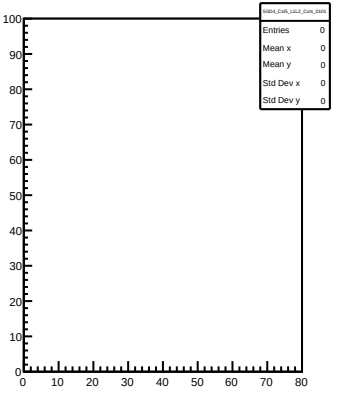
SSD4_CsI5_ModeStat_0101



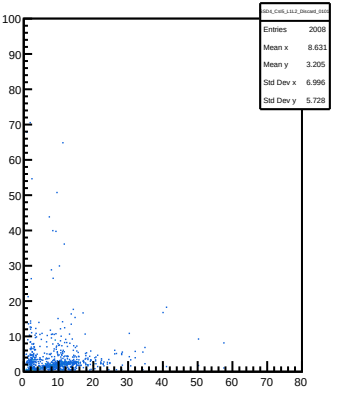
SSD4_CsI5_L1L2_0101



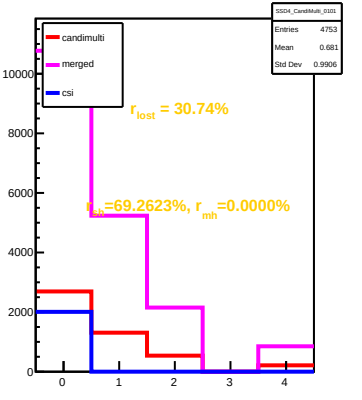
SSD4_CsI5_L1L2_Cuts_0101



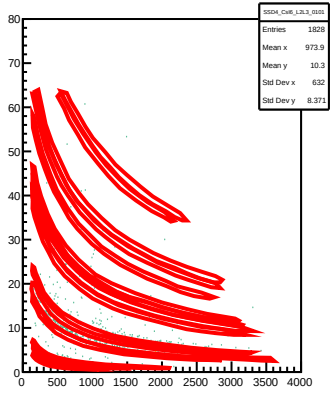
SSD4_CsI5_L1L2_Discard_0101



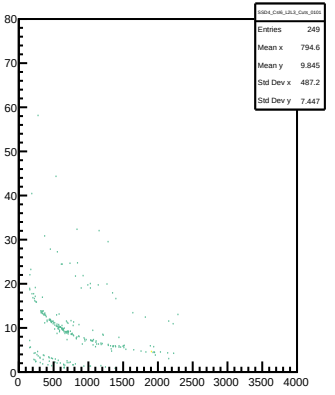
SSD4_CandiMulti_0101



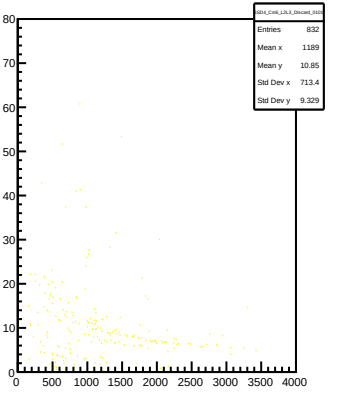
SSD4_CsI6_L2L3_0101



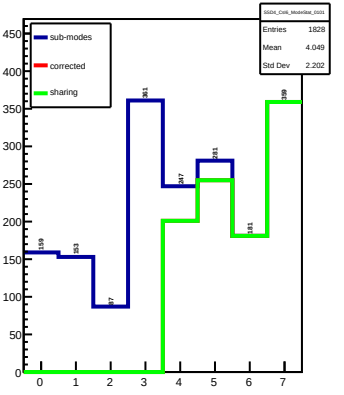
SSD4_CsI6_L2L3_Cuts_0101



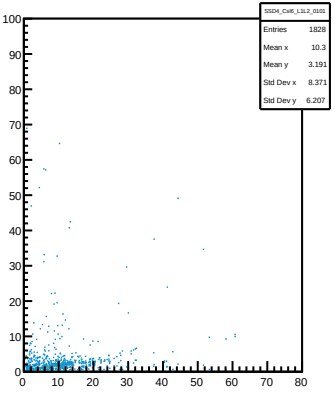
SSD4_CsI6_L2L3_Discard_0101



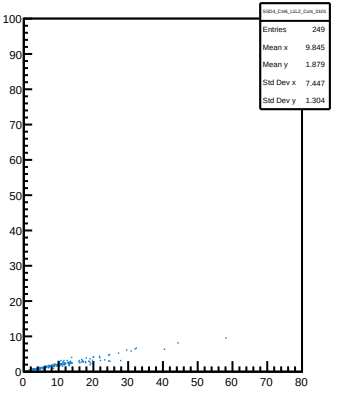
SSD4_CsI6_ModeStat_0101



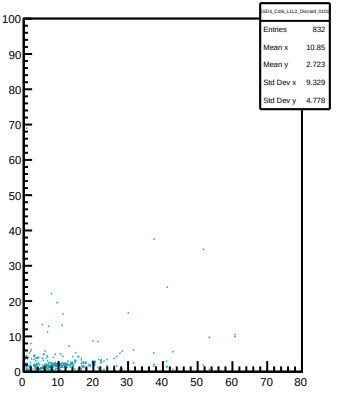
SSD4_CsI6_L1L2_0101



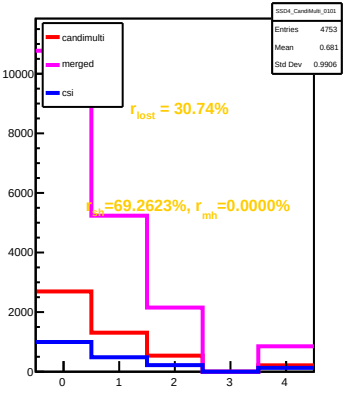
SSD4_CsI6_L1L2_Cuts_0101



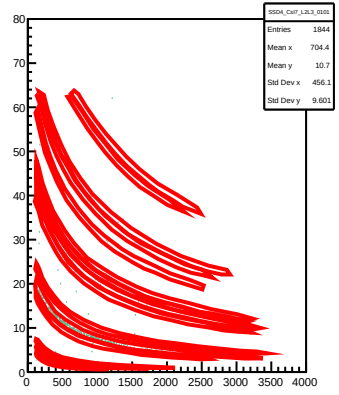
SSD4_CsI6_L1L2_Discard_0101



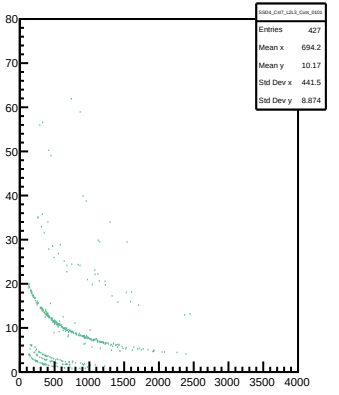
SSD4_CandiMulti_0101



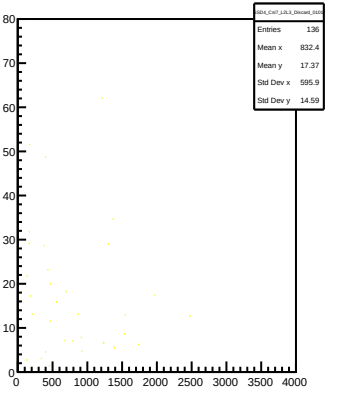
SSD4_CsI7_L2L3_0101



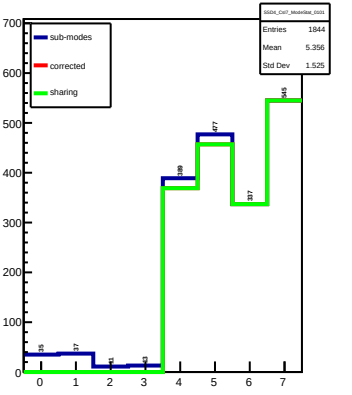
SSD4_CsI7_L2L3_Cuts_0101



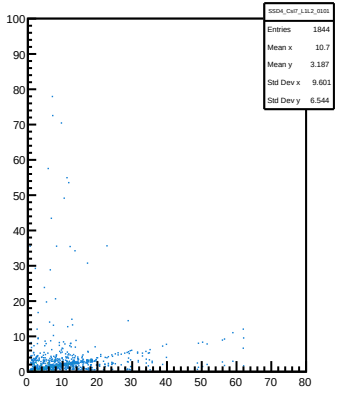
SSD4_CsI7_L2L3_Discard_0101



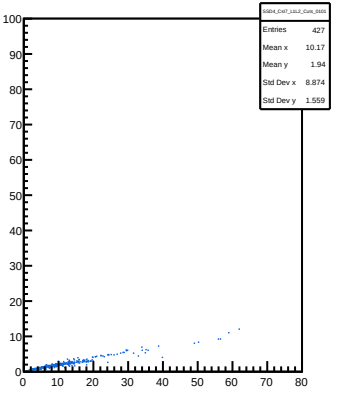
SSD4_CsI7_ModeStat_0101



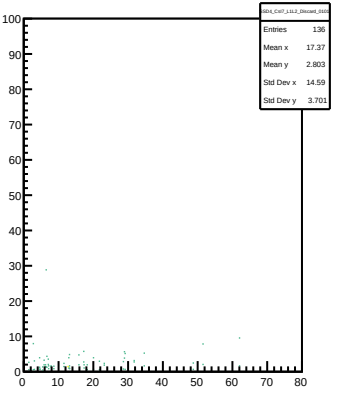
SSD4_CsI7_L1L2_0101



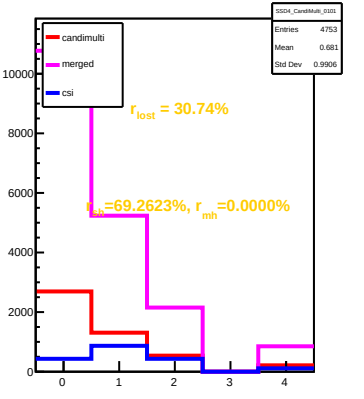
SSD4_CsI7_L1L2_Cuts_0101



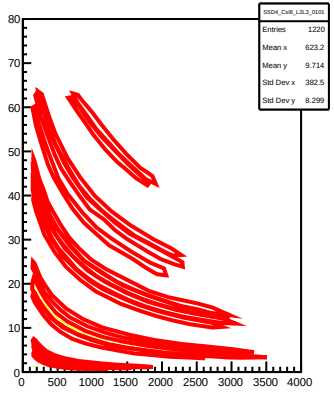
SSD4_CsI7_L1L2_Discard_0101



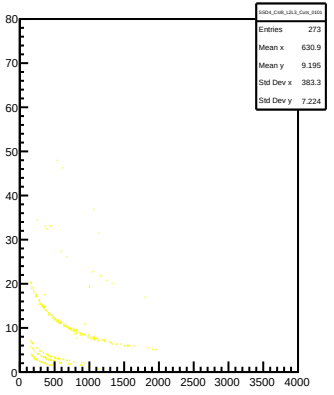
SSD4_CandiMulti_0101



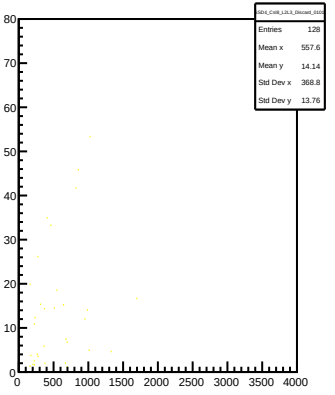
SSD4_CsI8_L2L3_0101



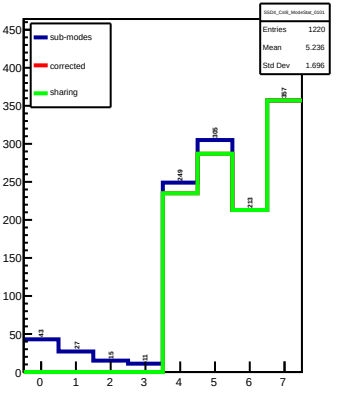
SSD4_CsI8_L2L3_Cuts_0101



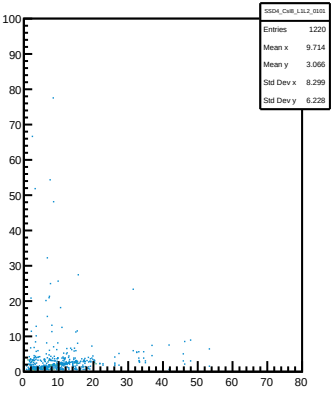
SSD4_CsI8_L2L3_Discard_0101



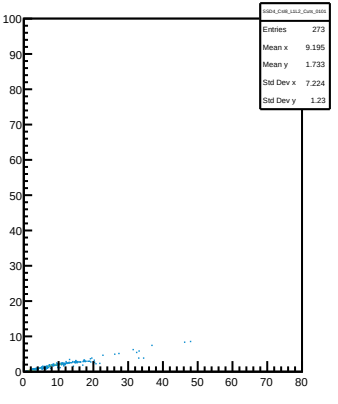
SSD4_CsI8_ModeStat_0101



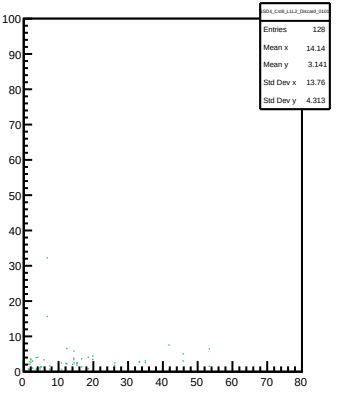
SSD4_CsI8_L1L2_0101



SSD4_CsI8_L1L2_Cuts_0101



SSD4_CsI8_L1L2_Discard_0101



SSD4_CandiMulti_0101