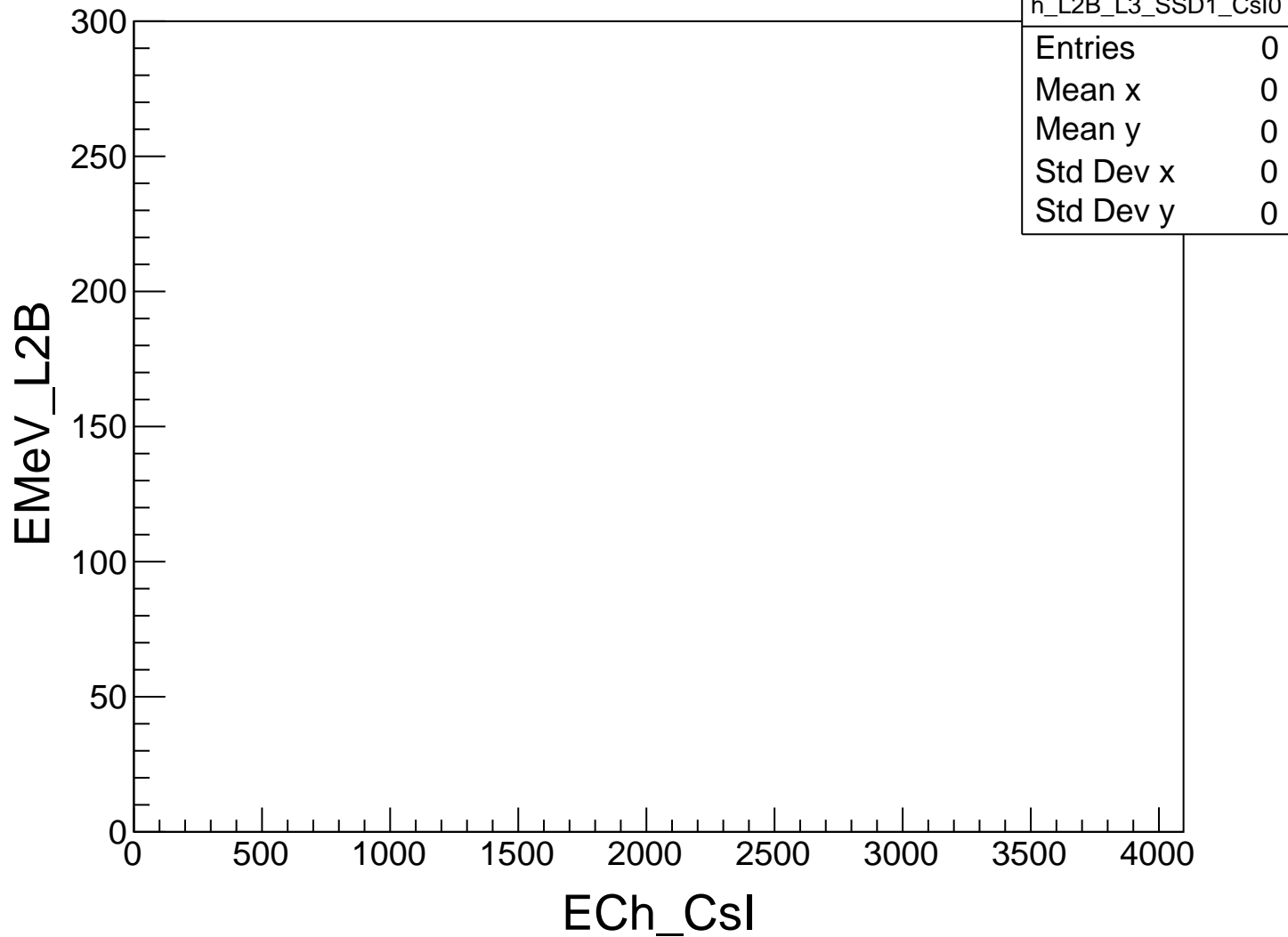
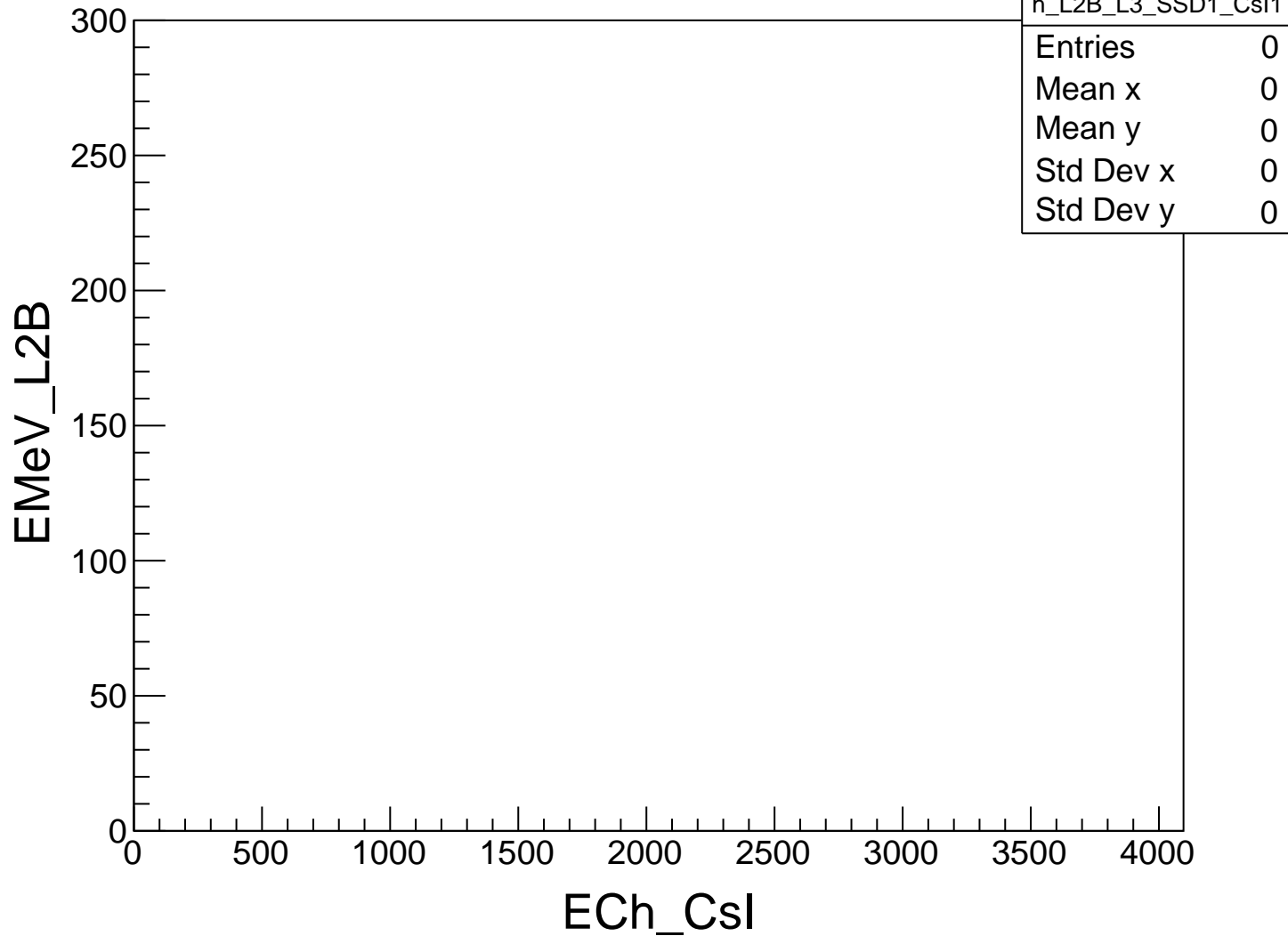


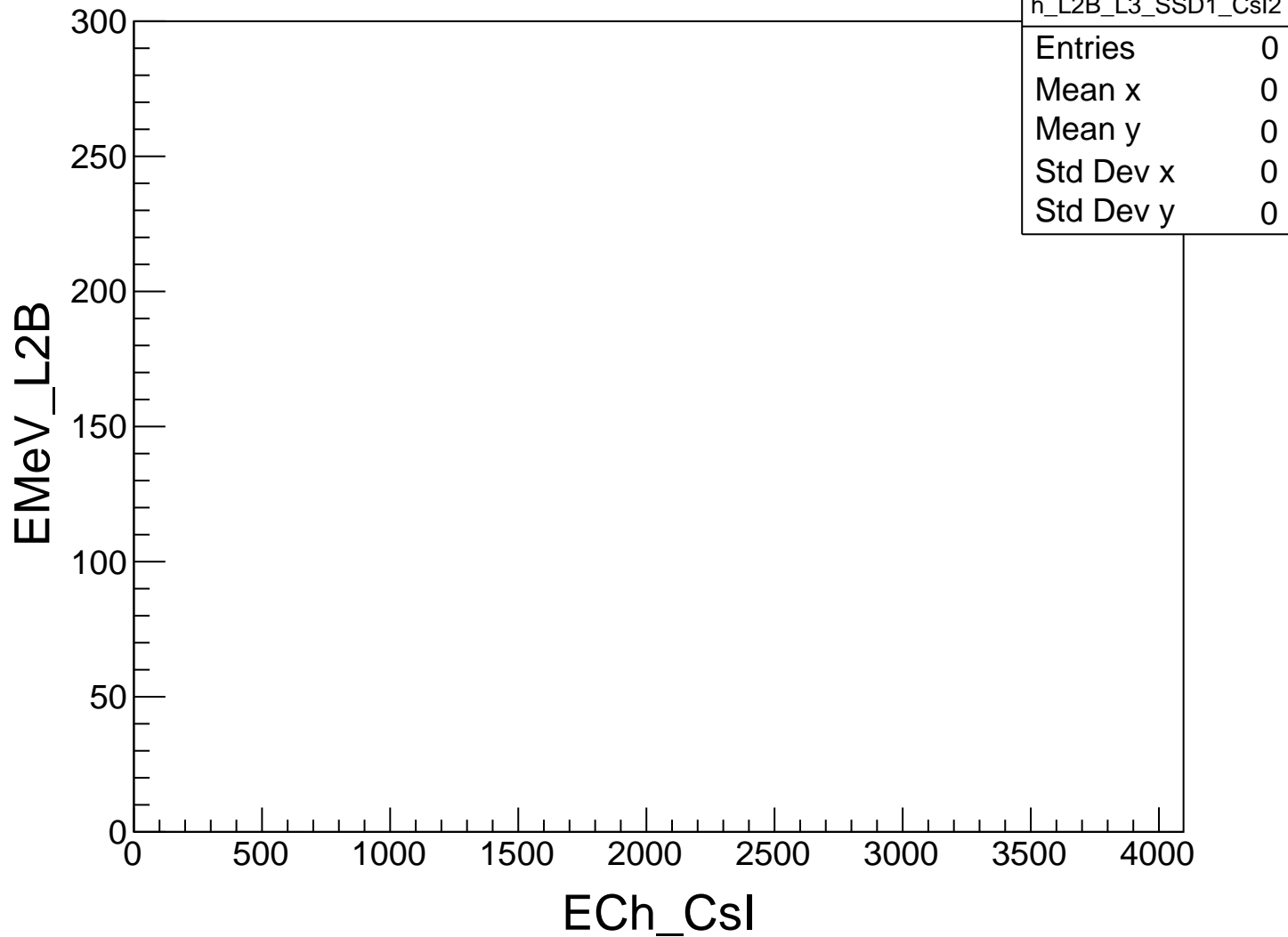
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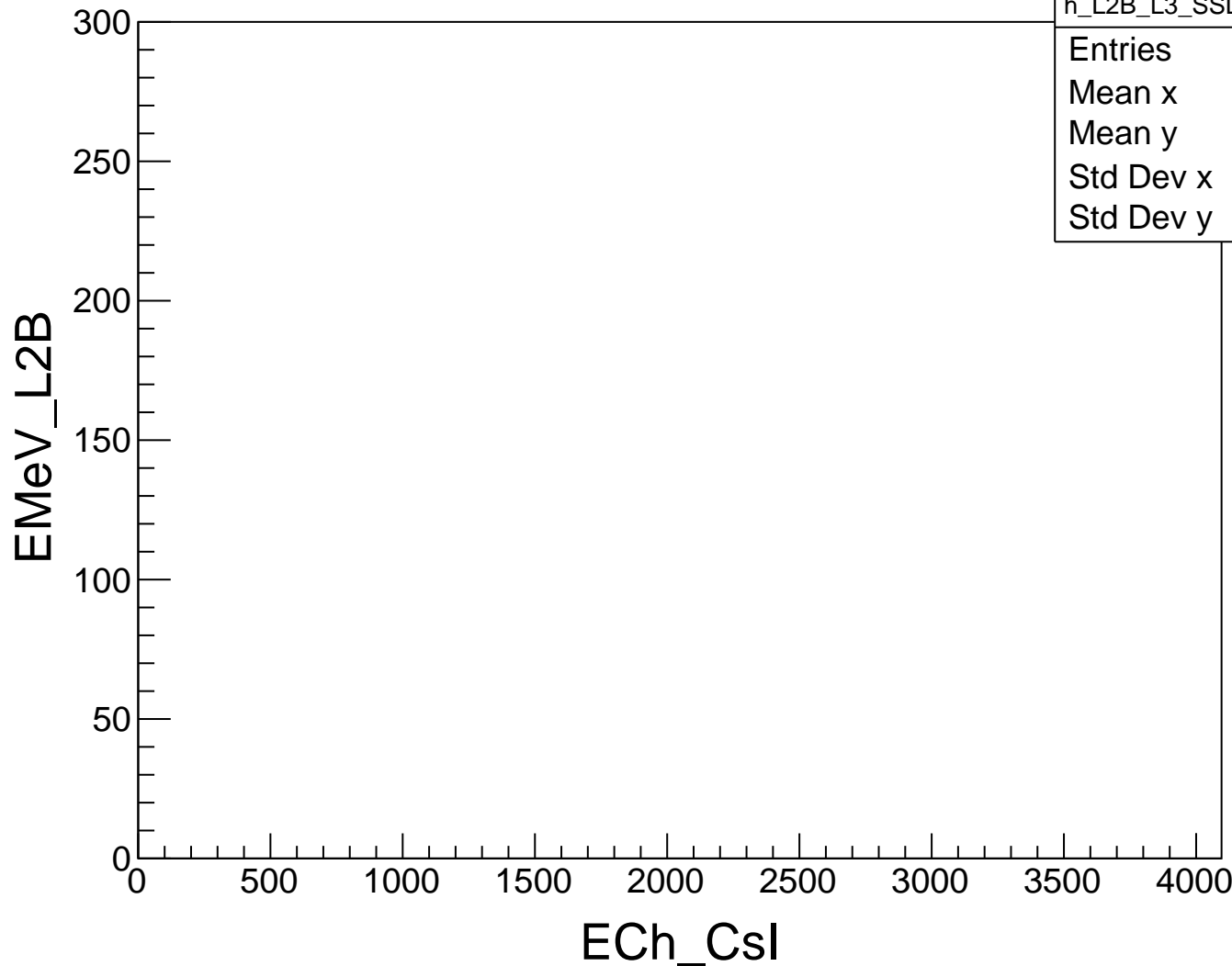
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h_L2B_L3_SSD1_CsI2

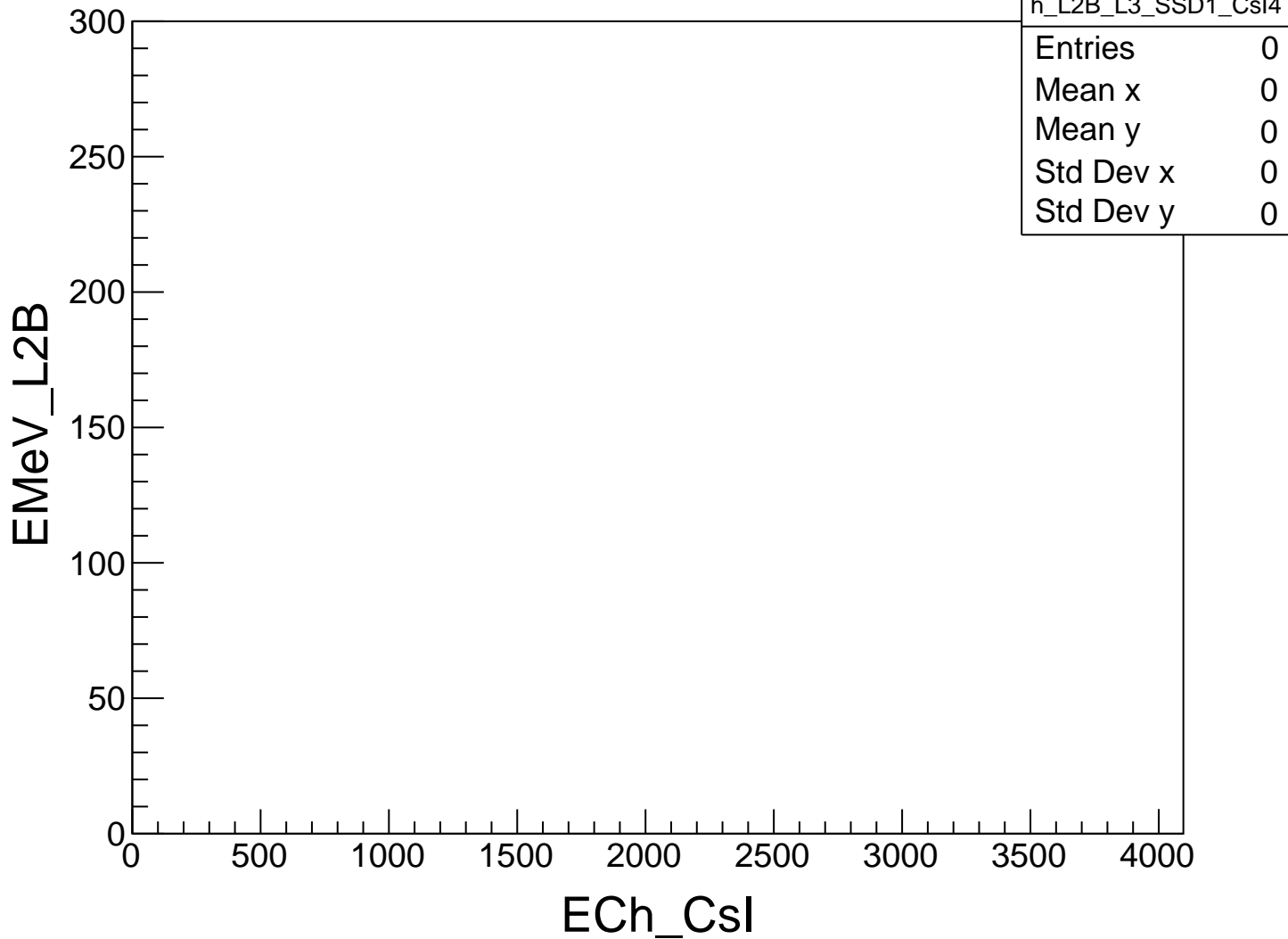


h_L2B_L3_SSD1_CsI3

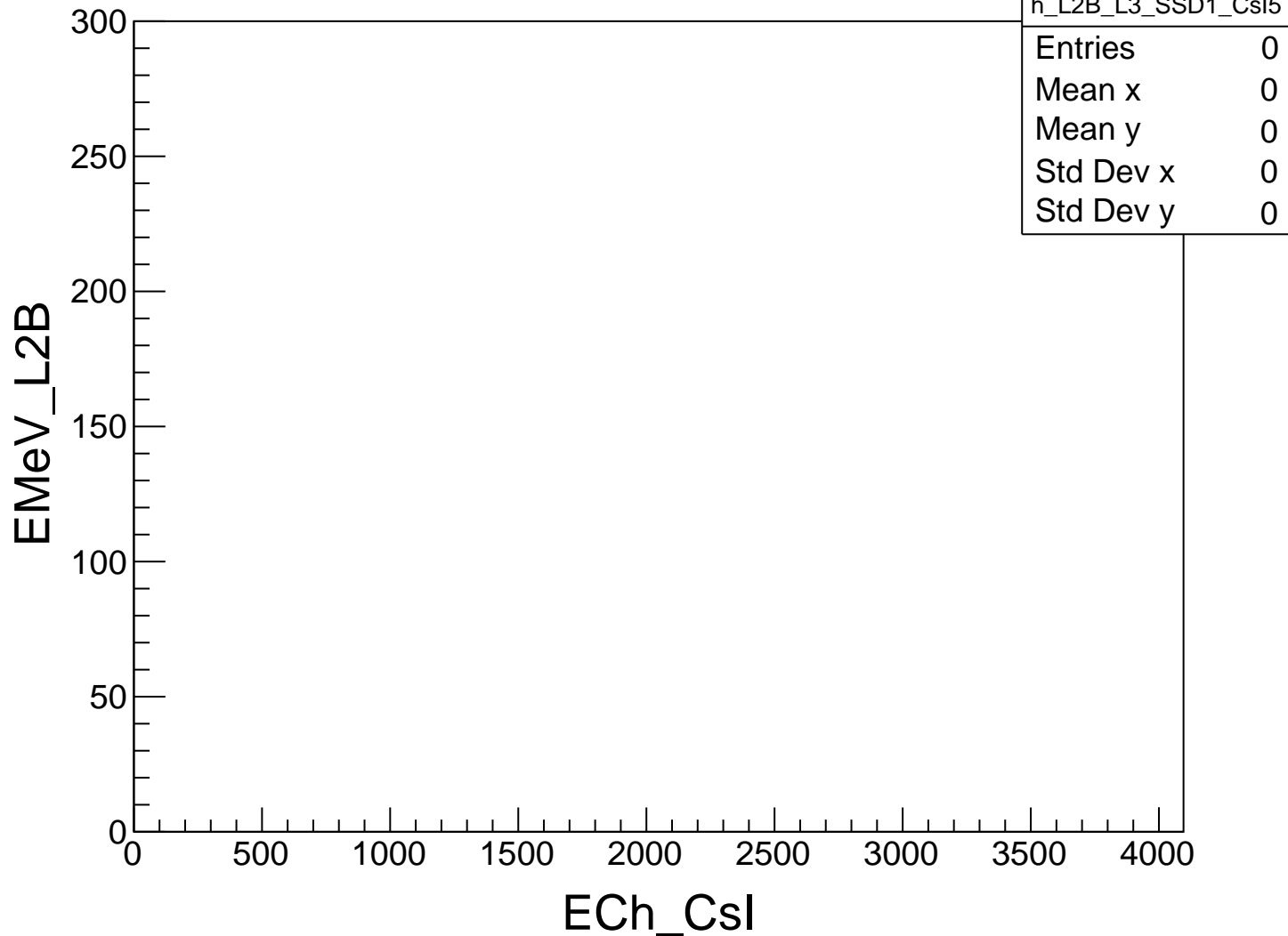


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Mean y	0
Std Dev x	0
Std Dev y	0

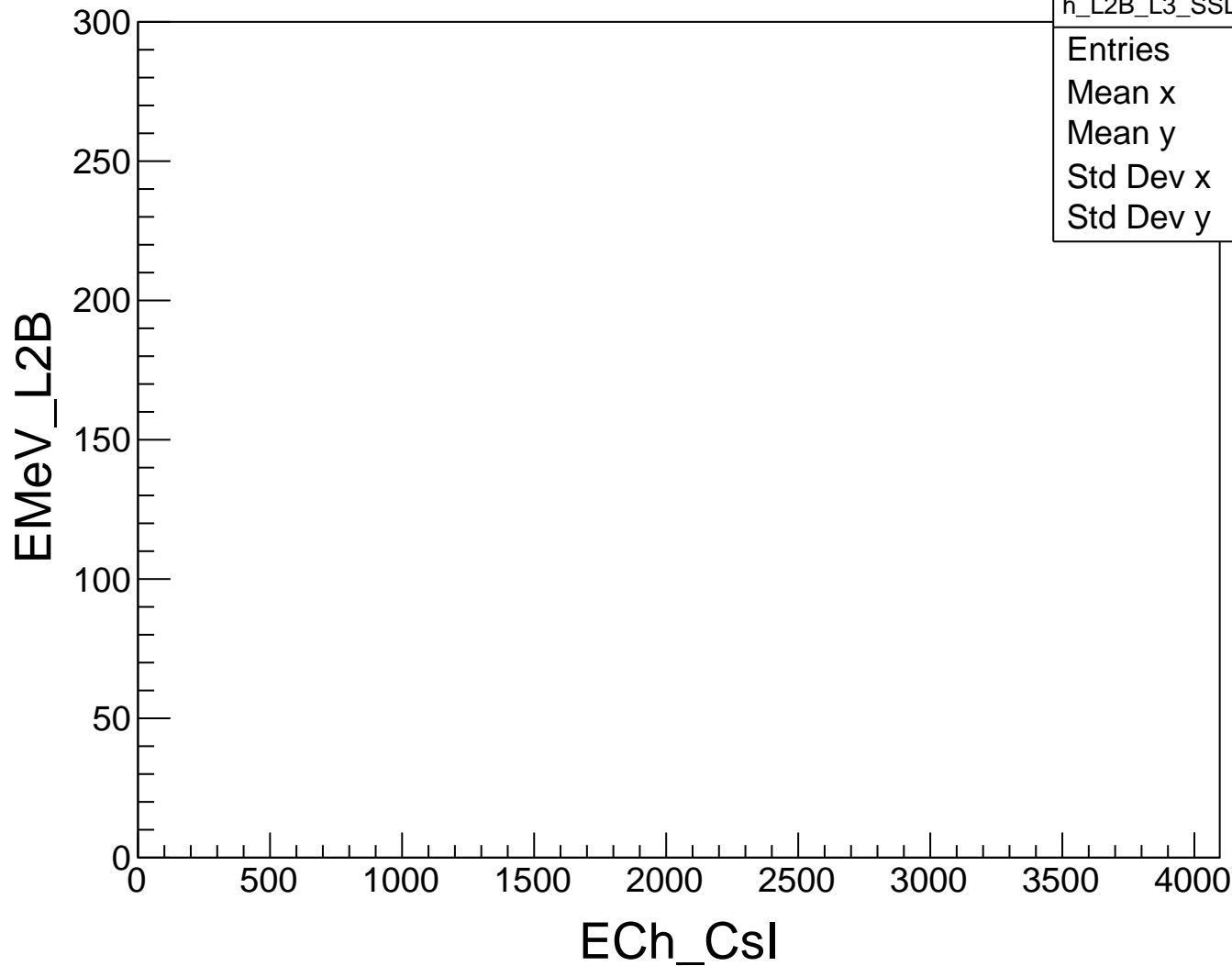
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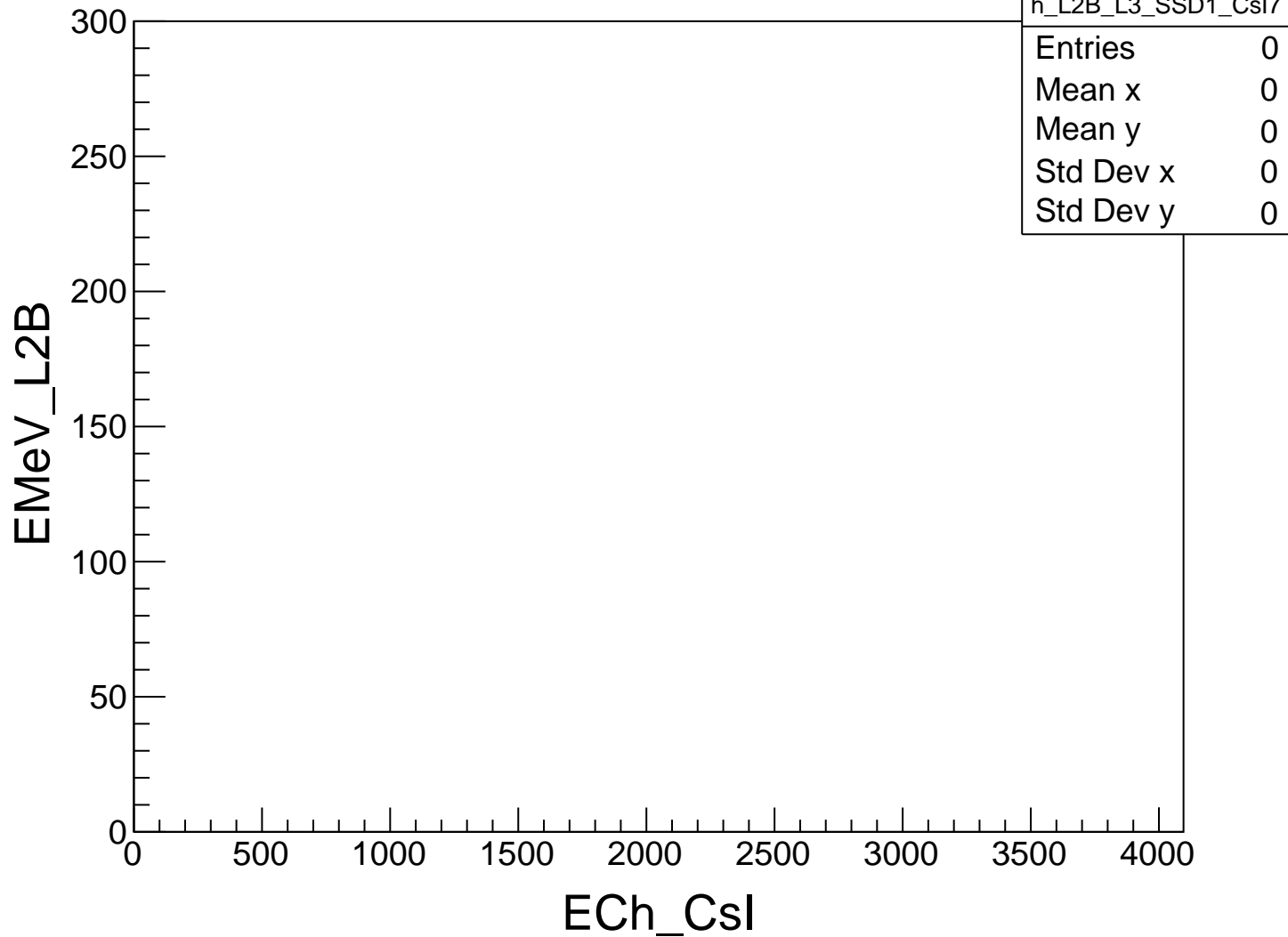
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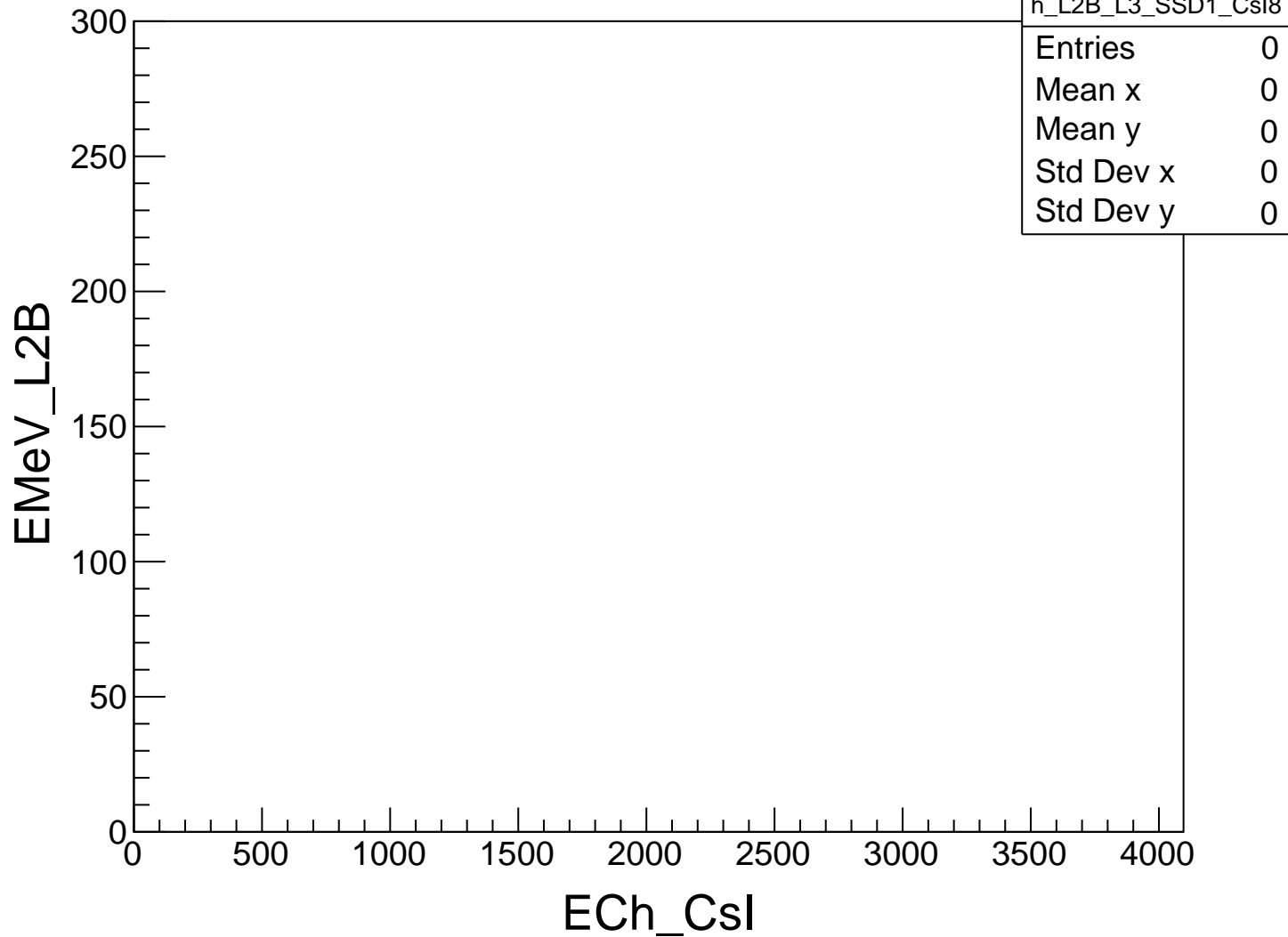
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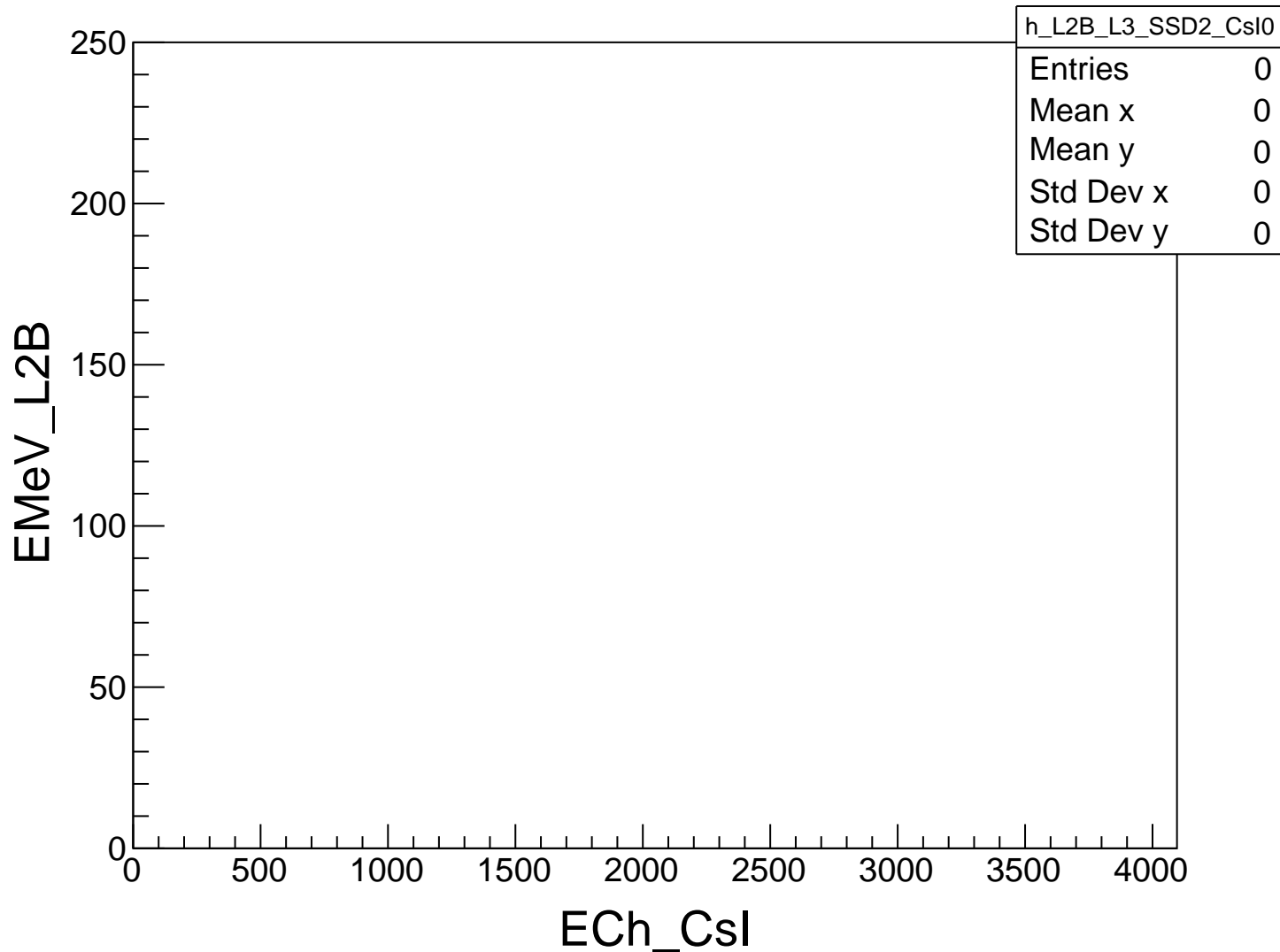
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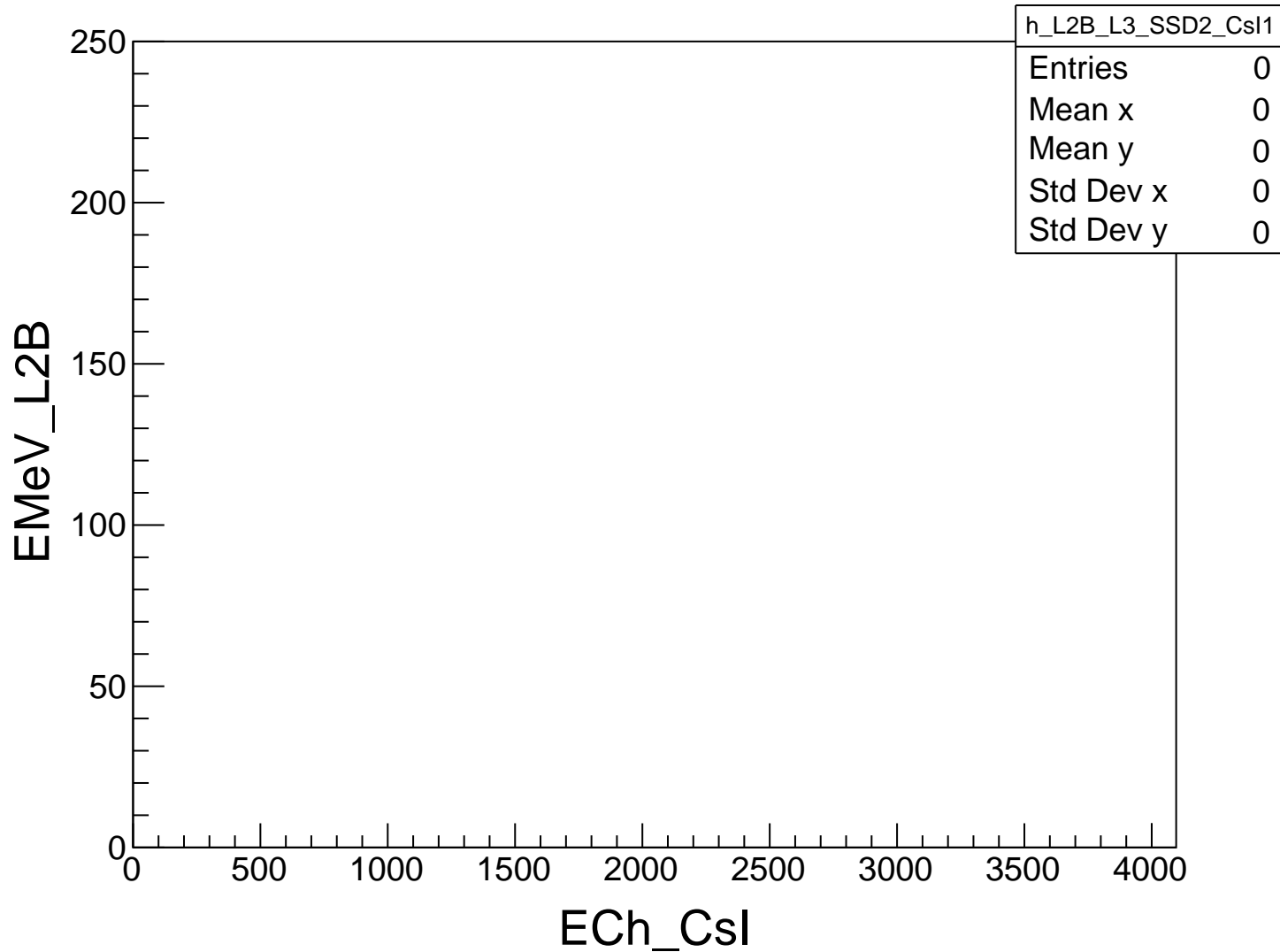
h_L2B_L3_SSD1_CsI8



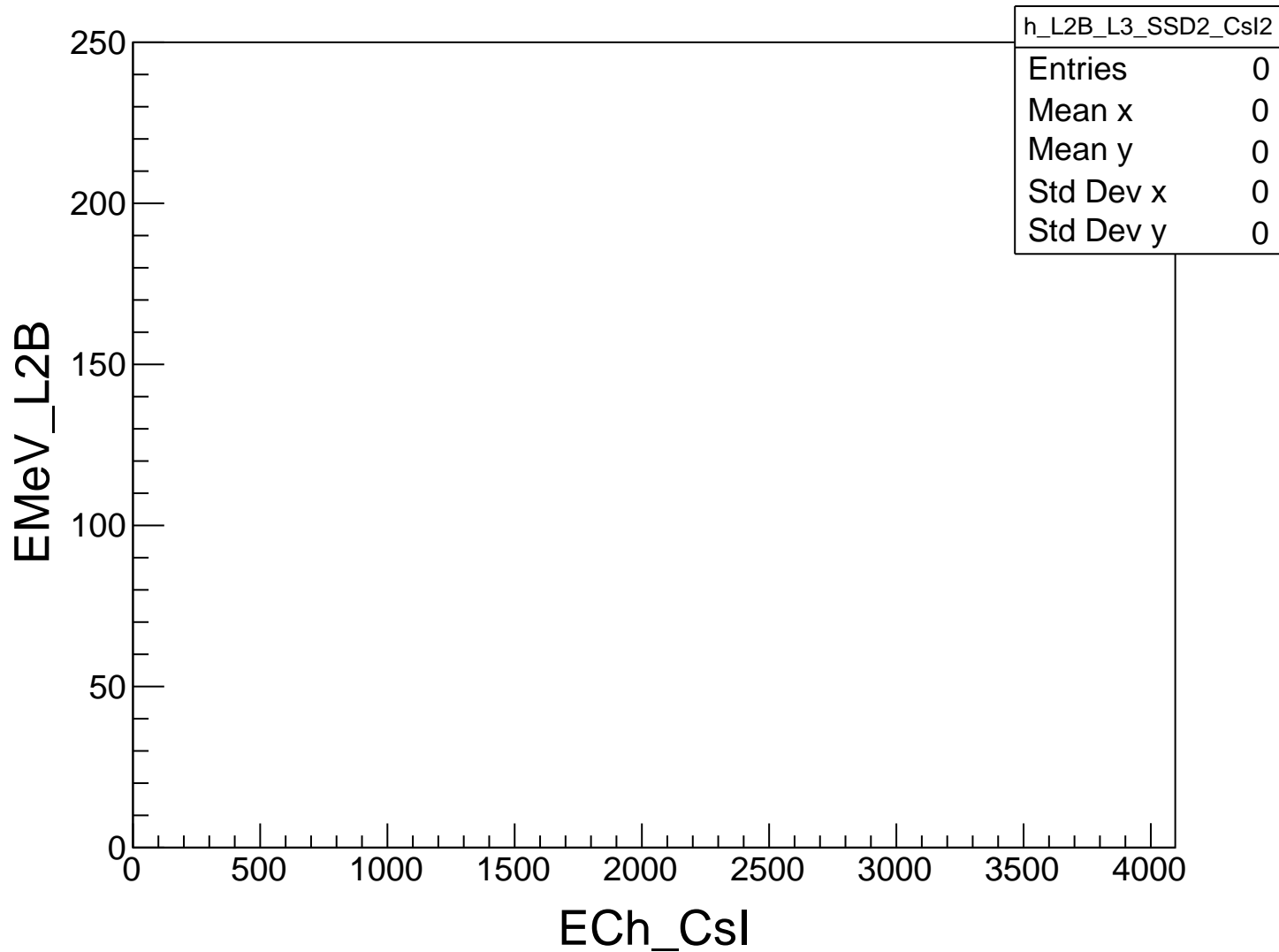
h_L2B_L3_SSD2_CsI0



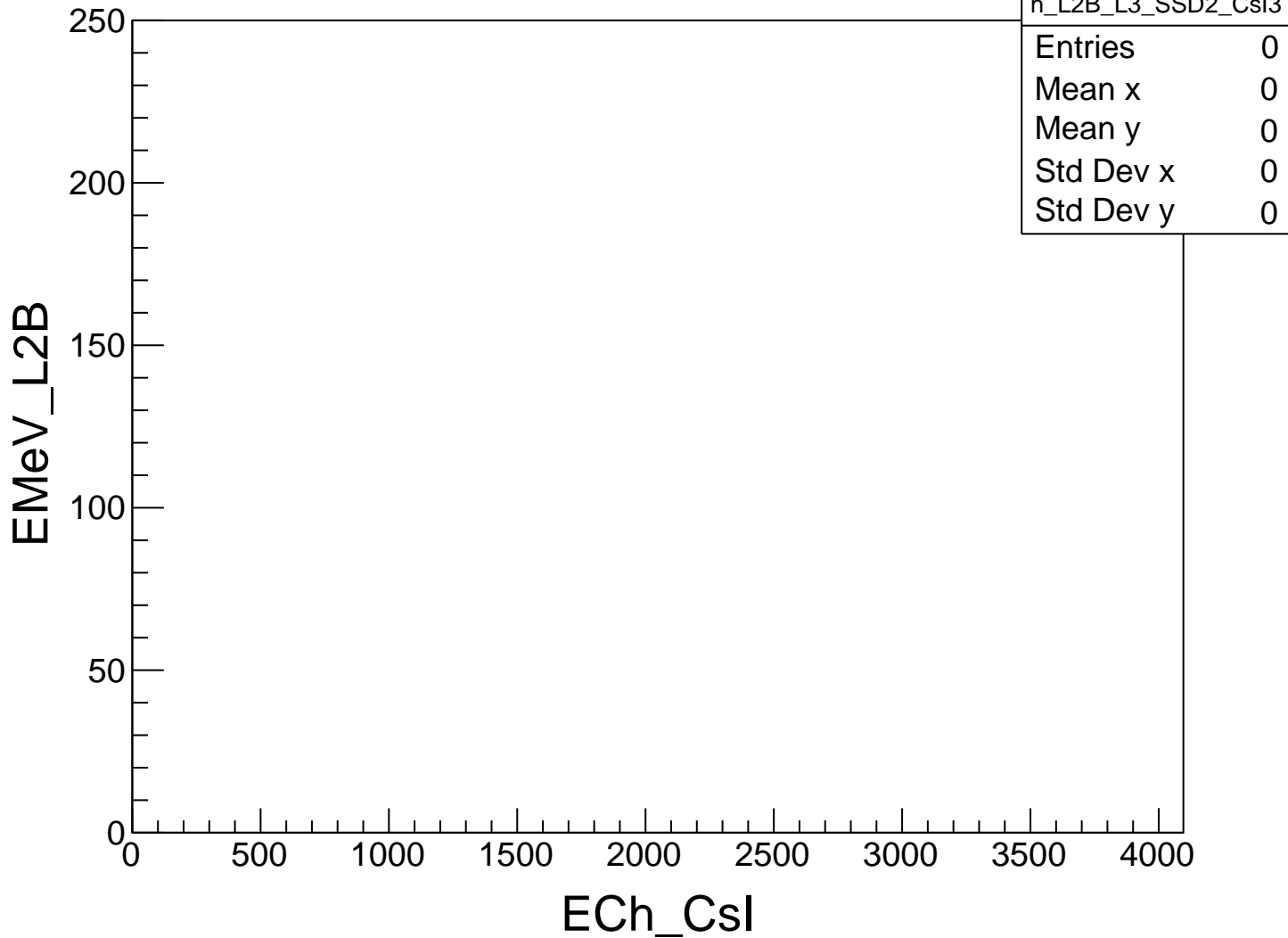
h_L2B_L3_SSD2_CsI1



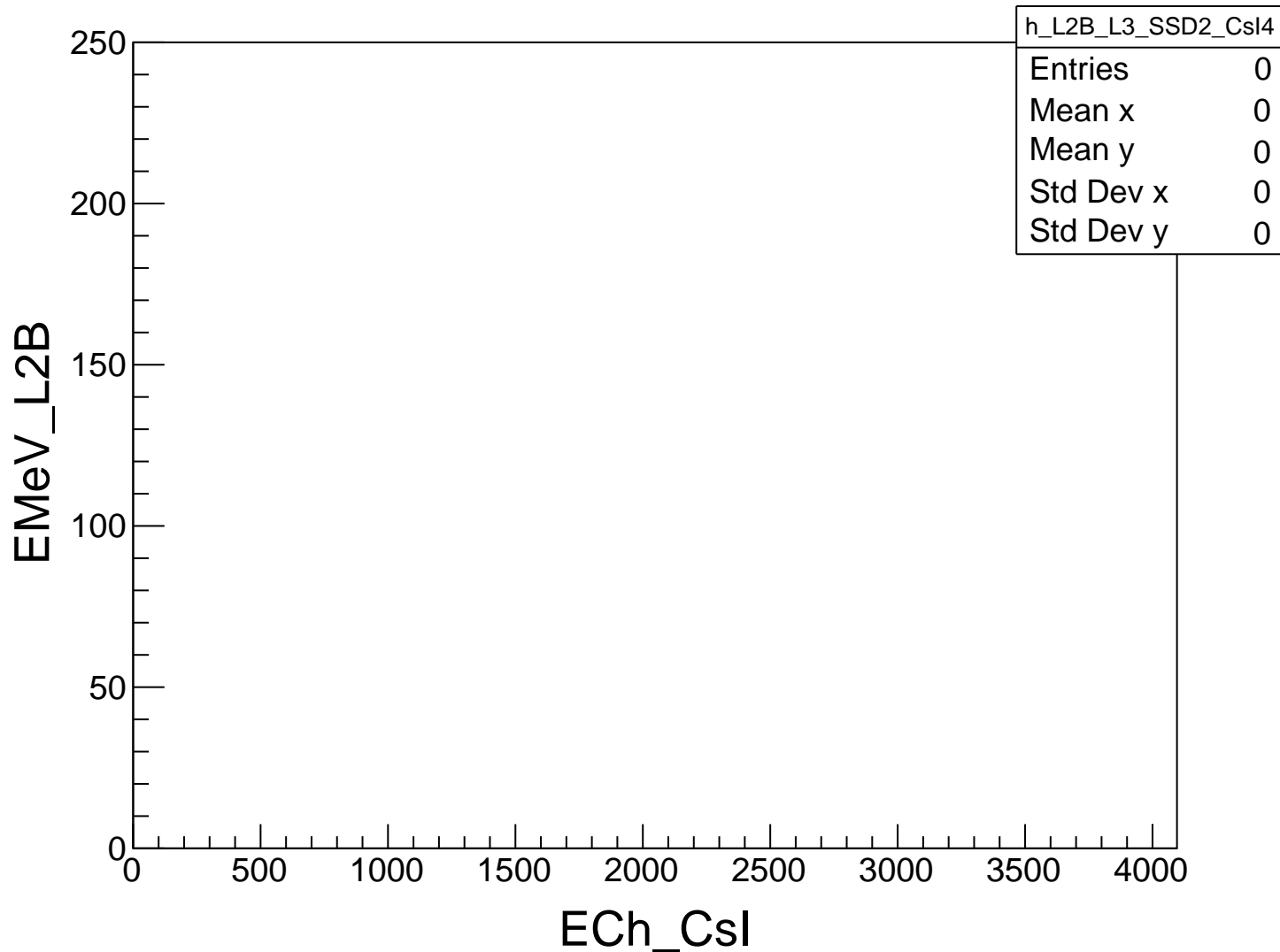
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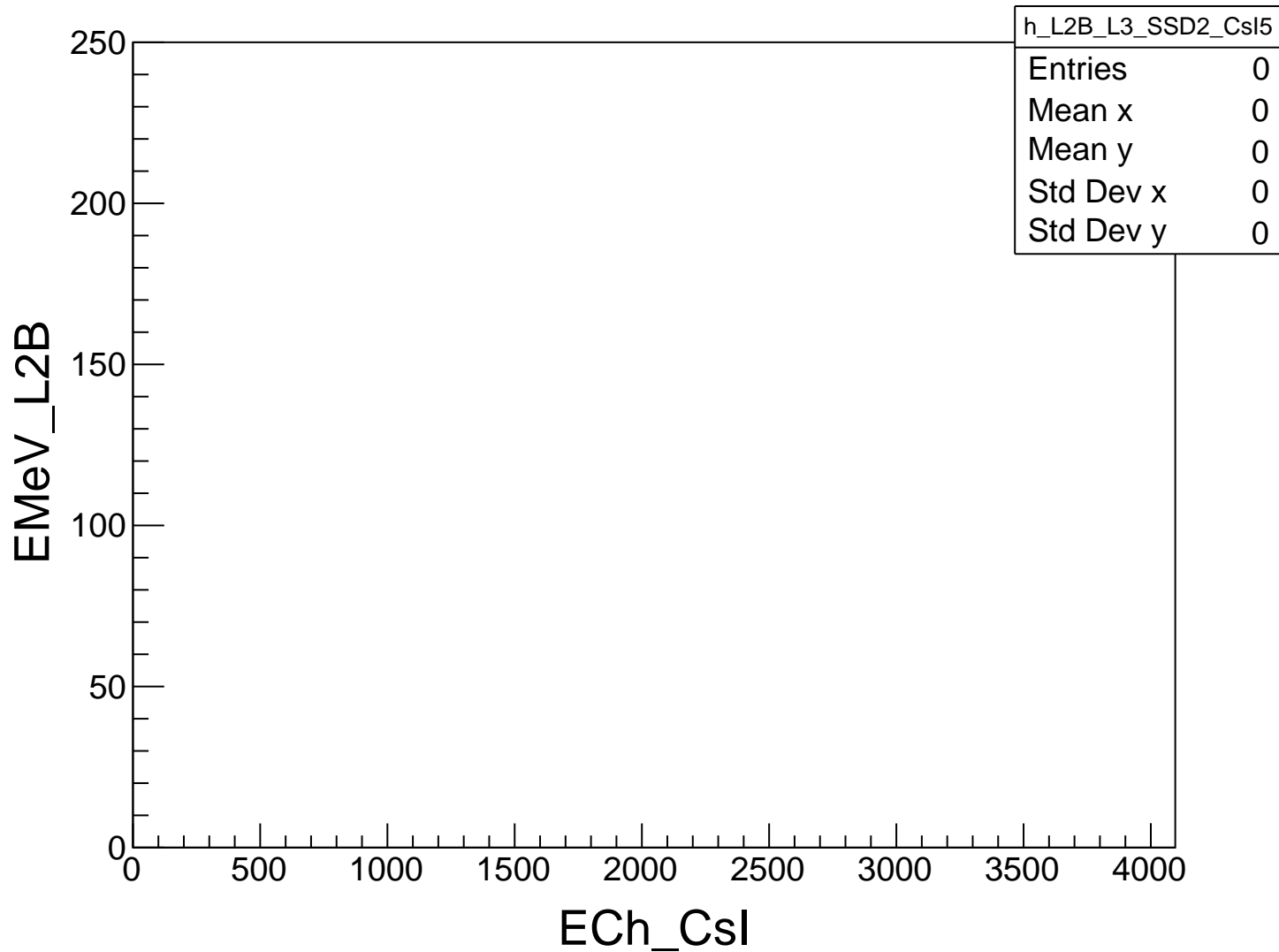
h_L2B_L3_SSD2_CsI3



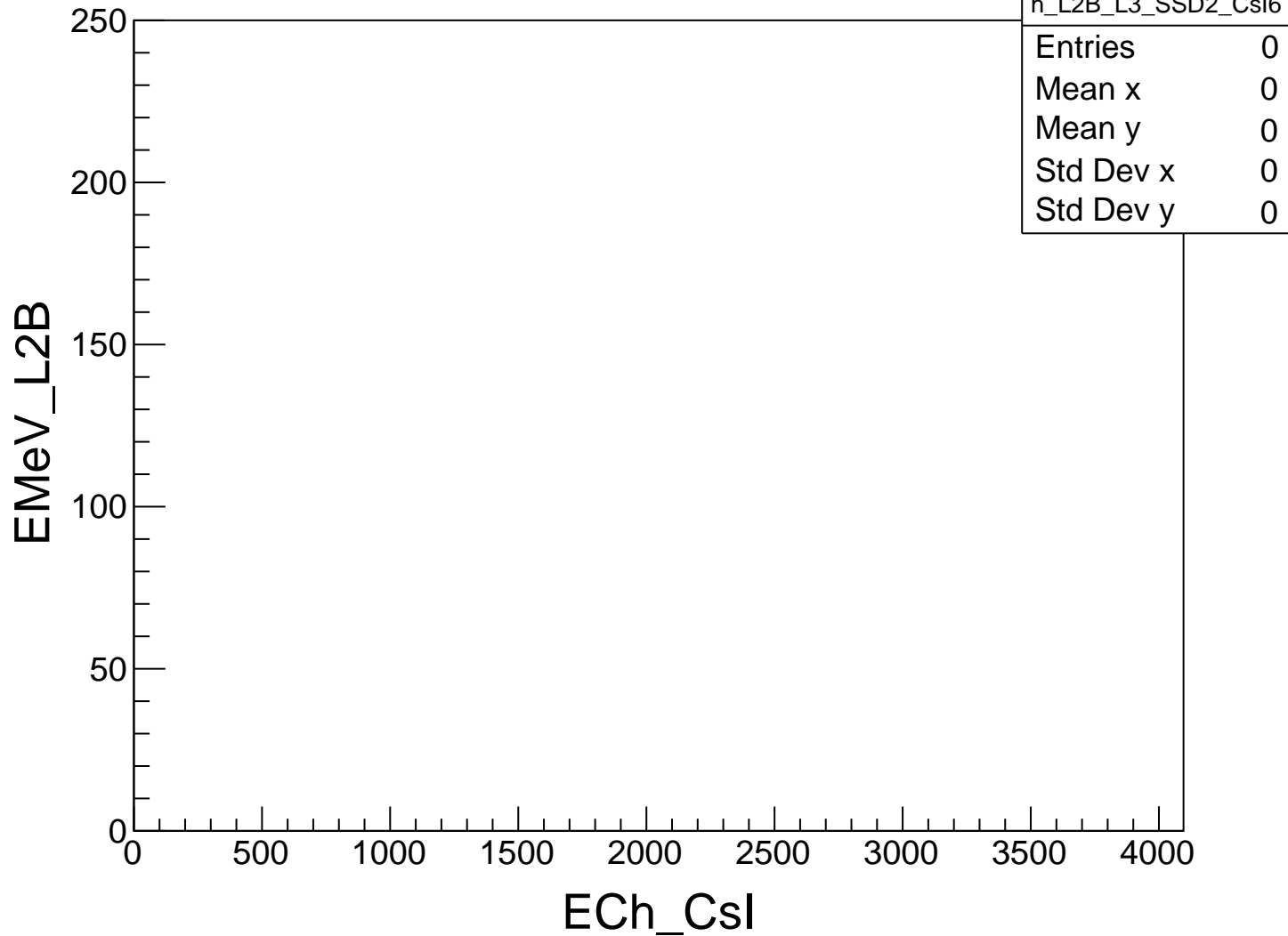
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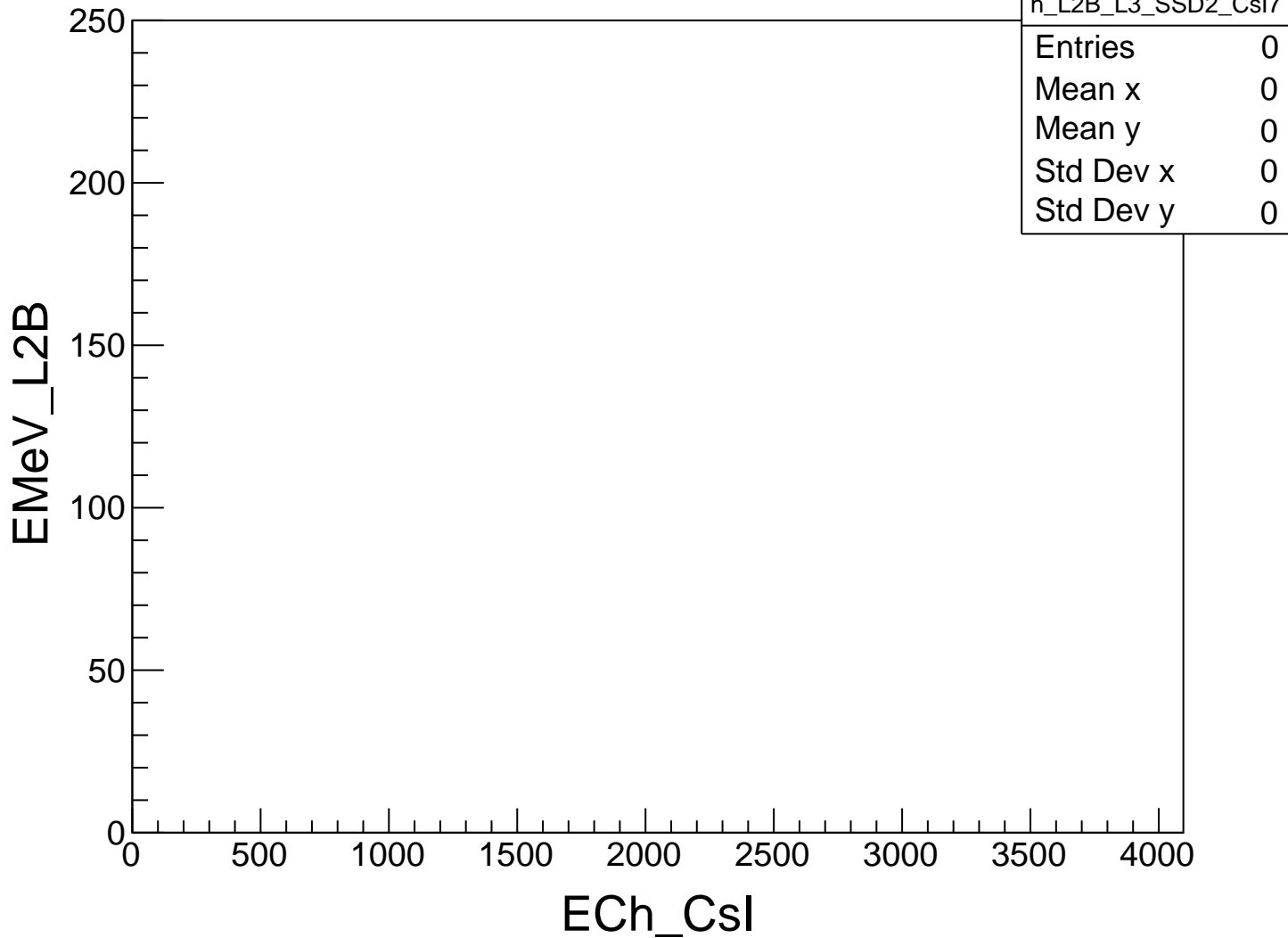
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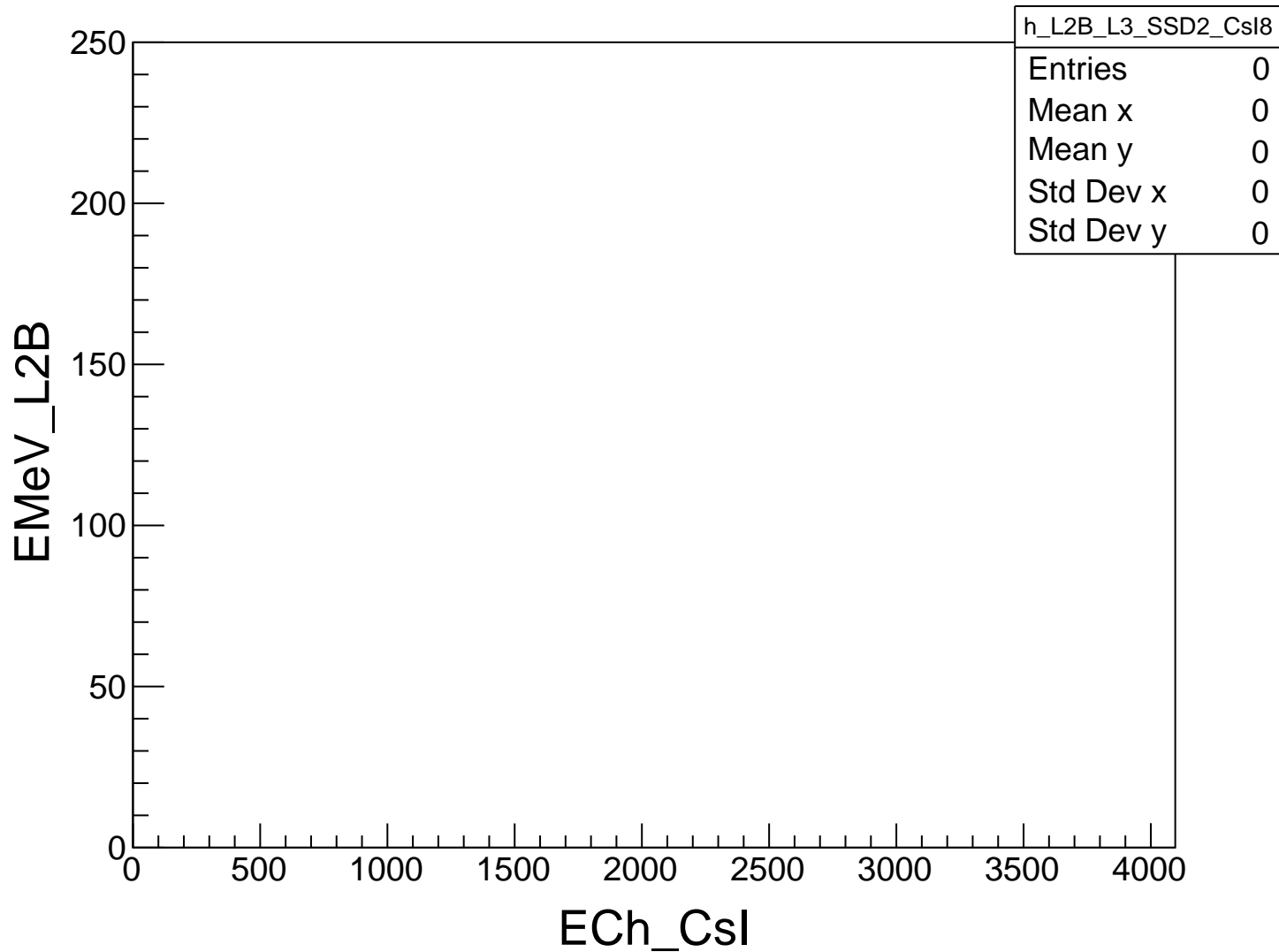
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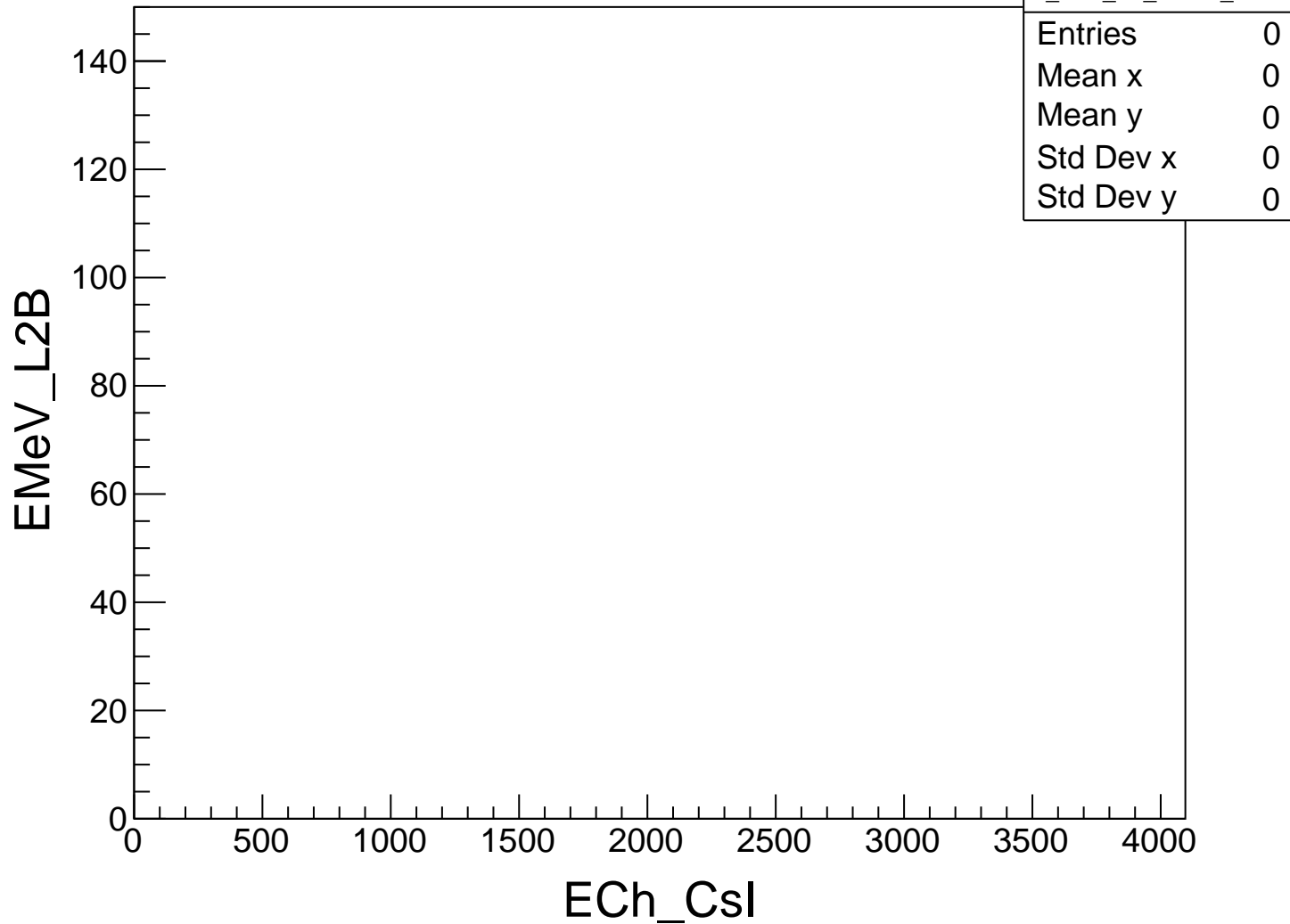
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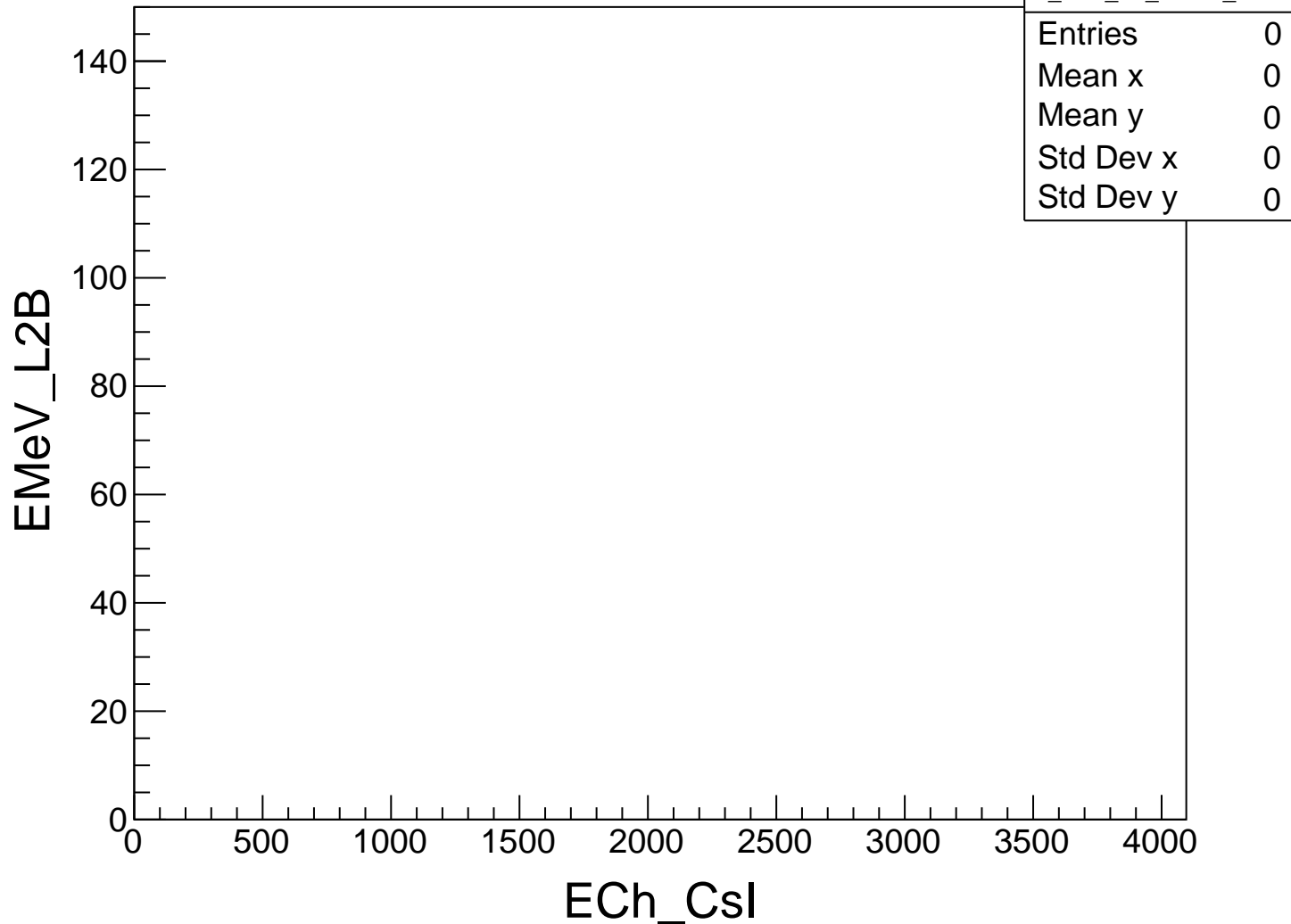
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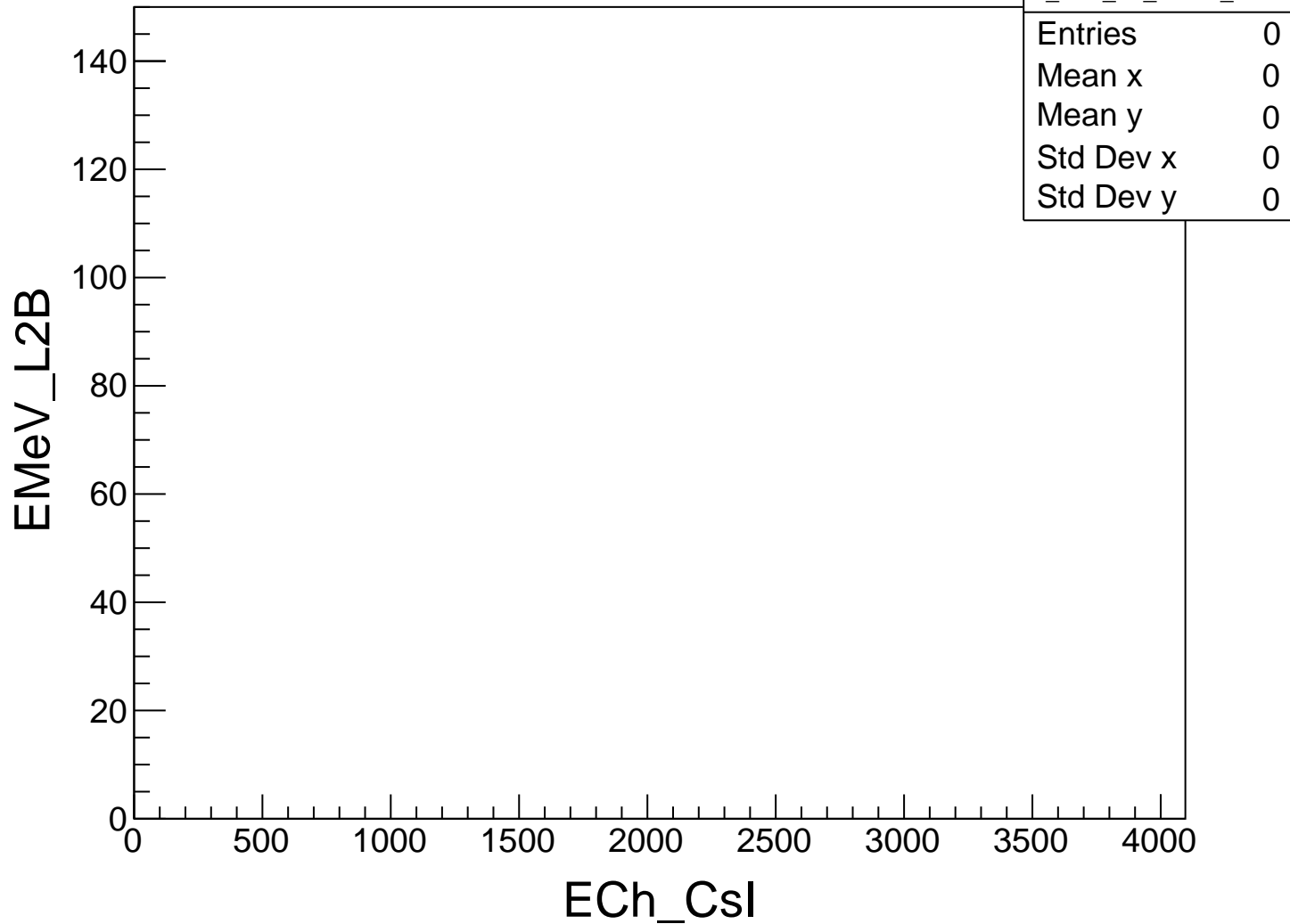
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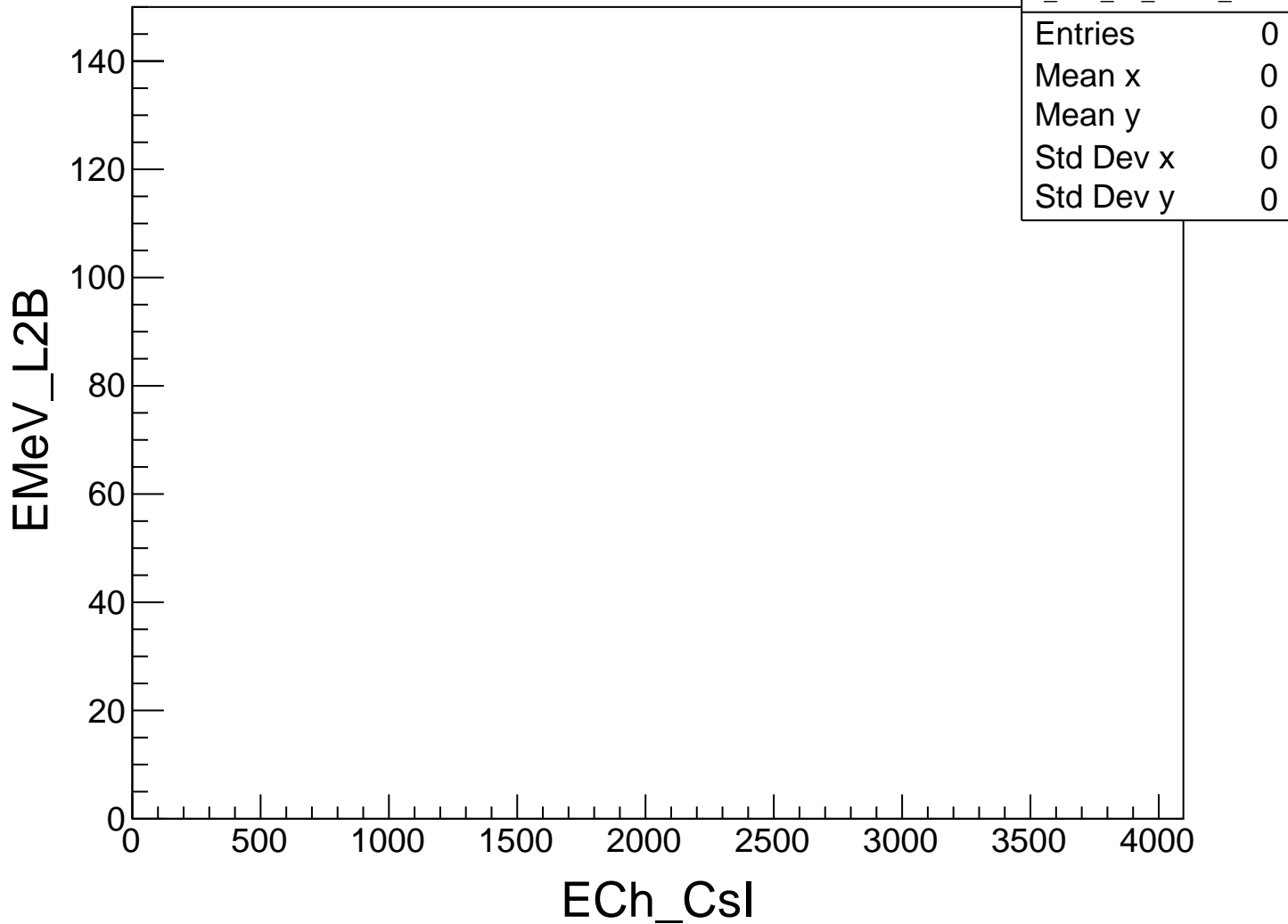
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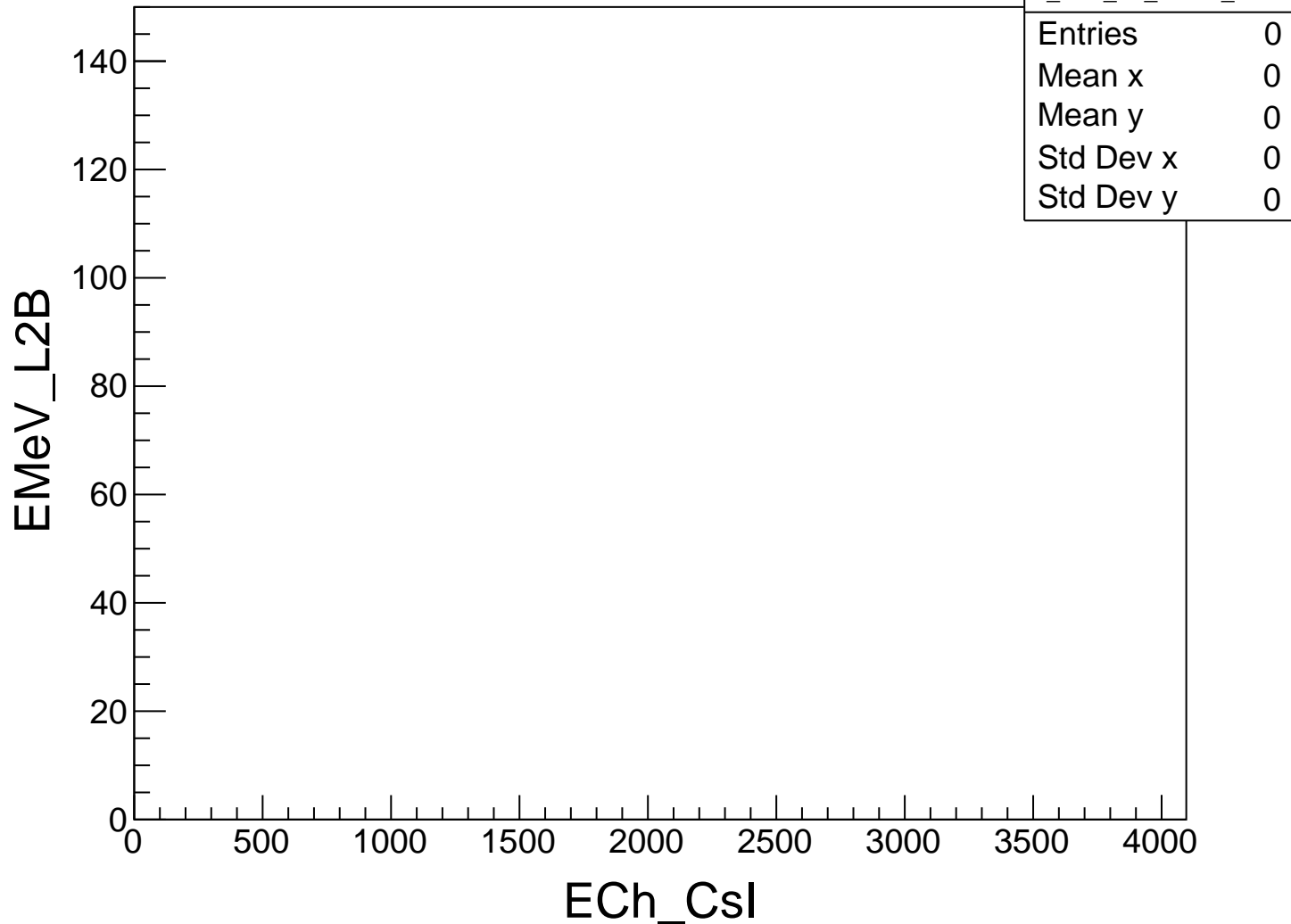
h_L2B_L3_SSD3_CsI2



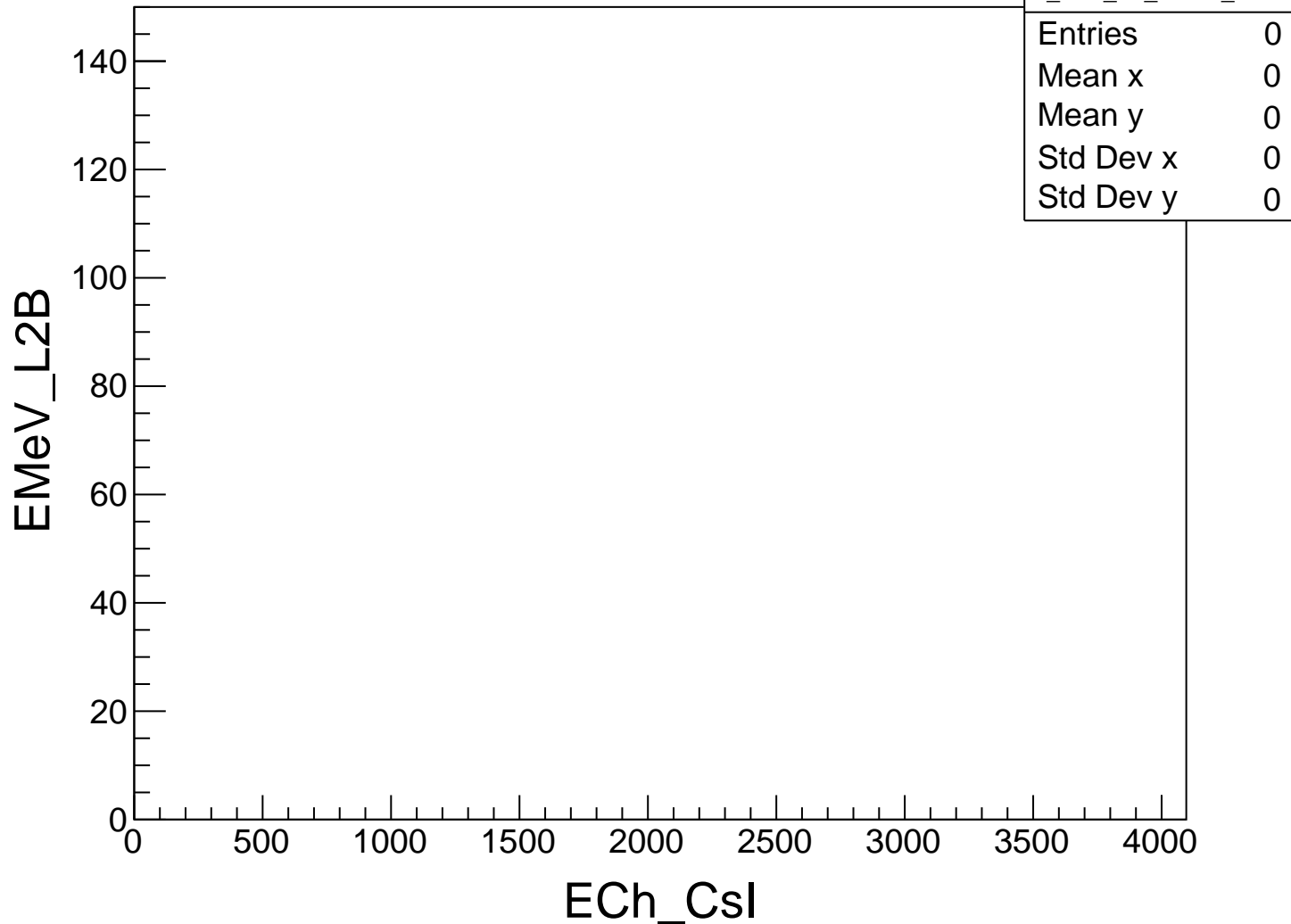
h_L2B_L3_SSD3_CsI3



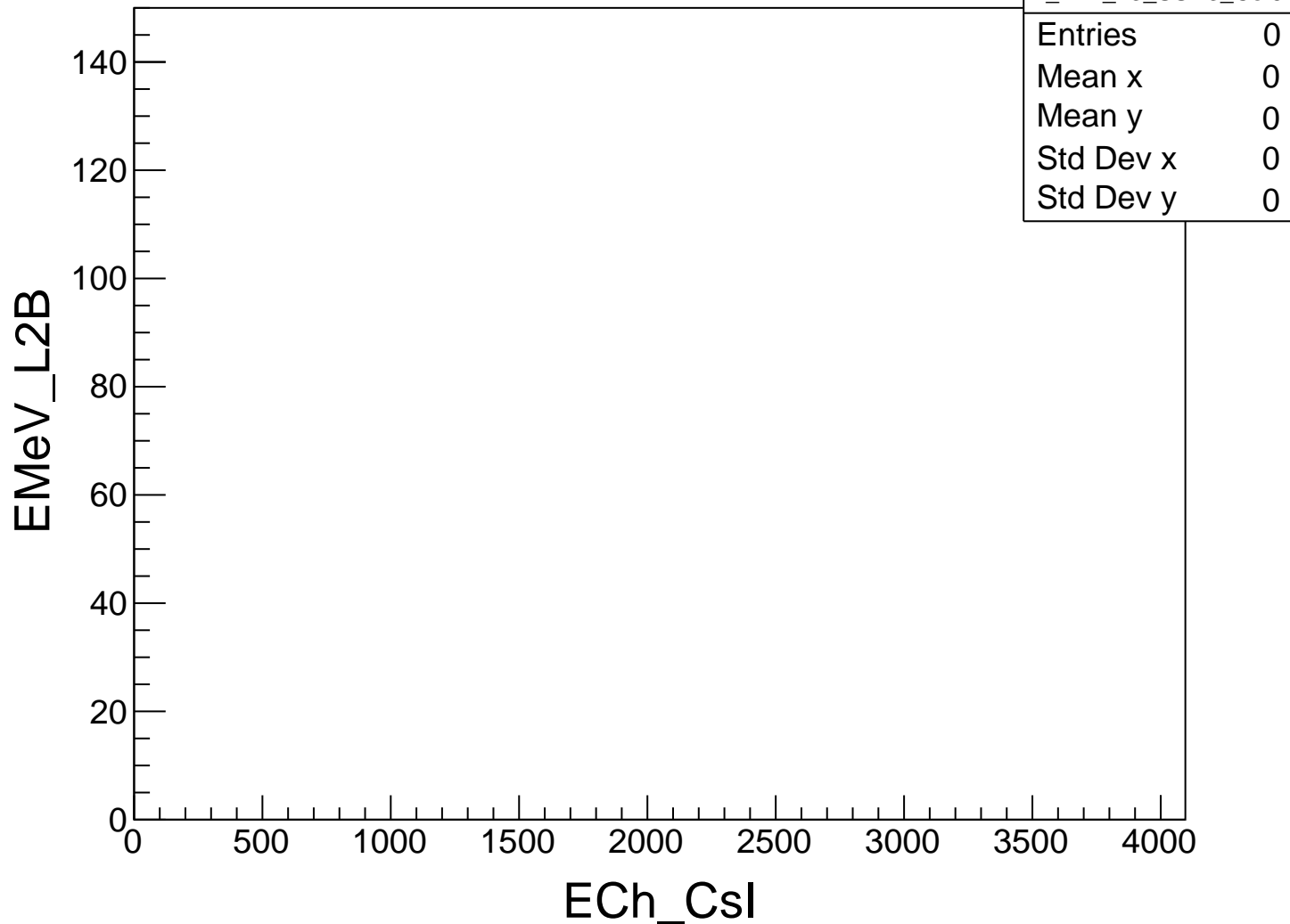
h_L2B_L3_SSD3_CsI4



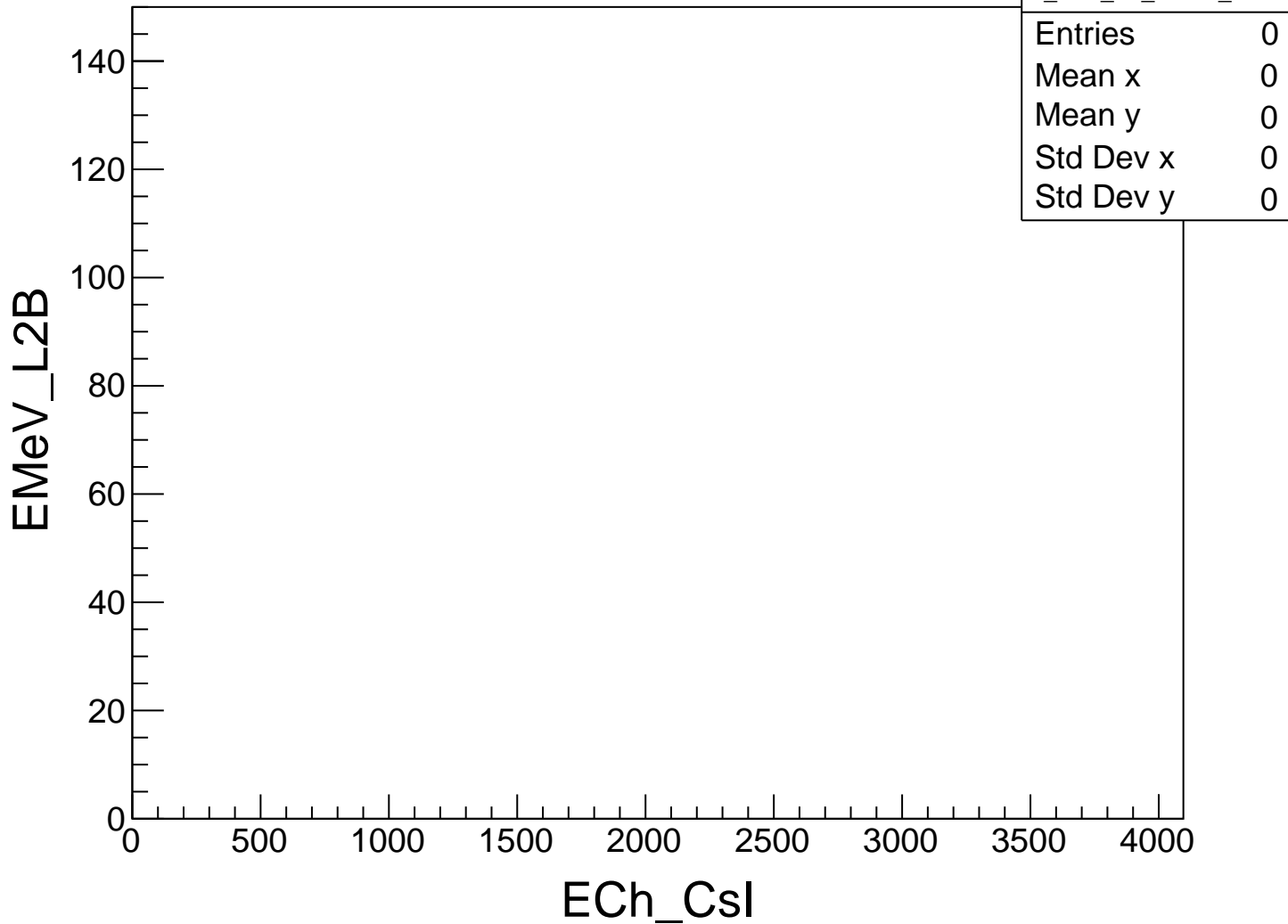
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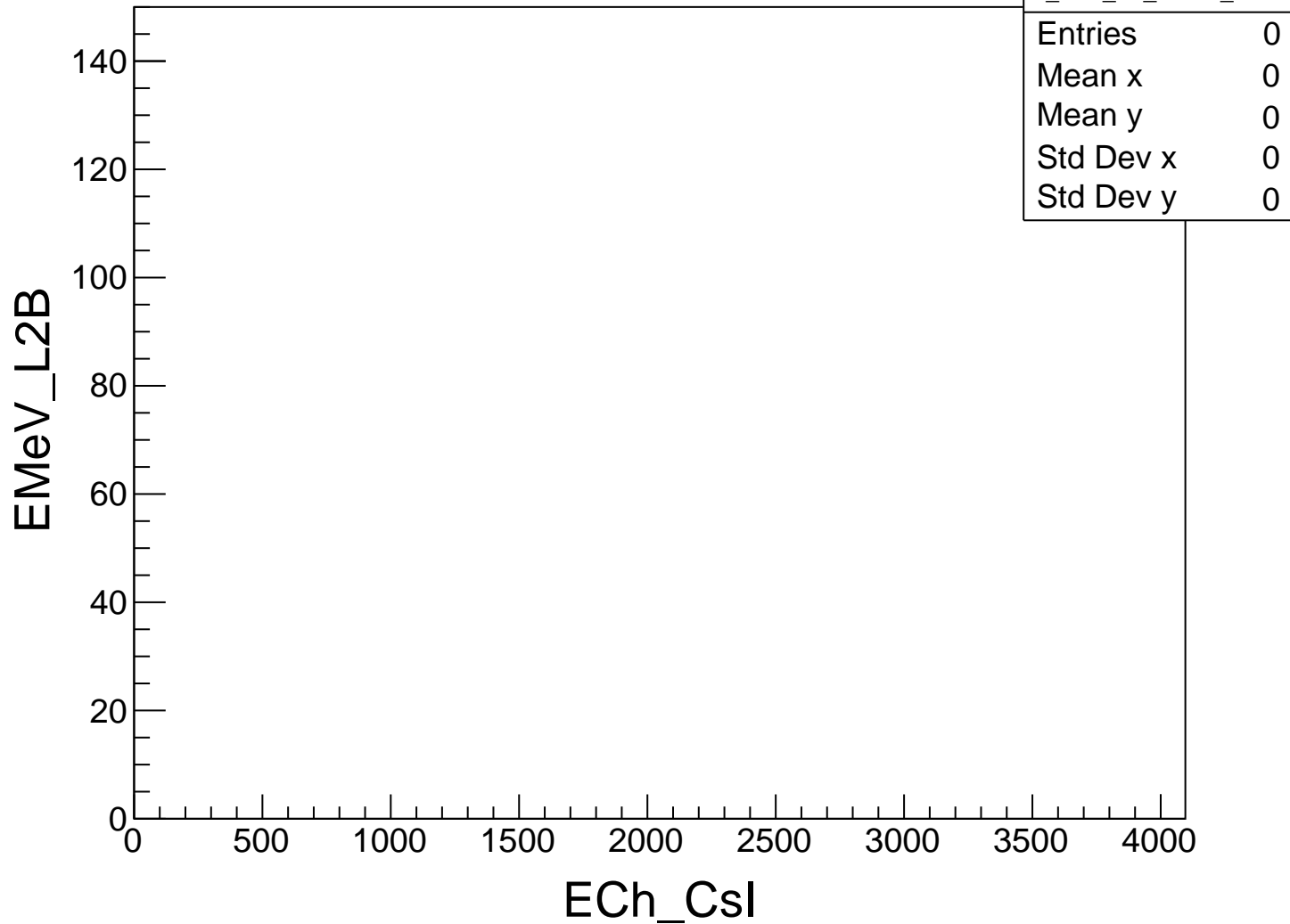
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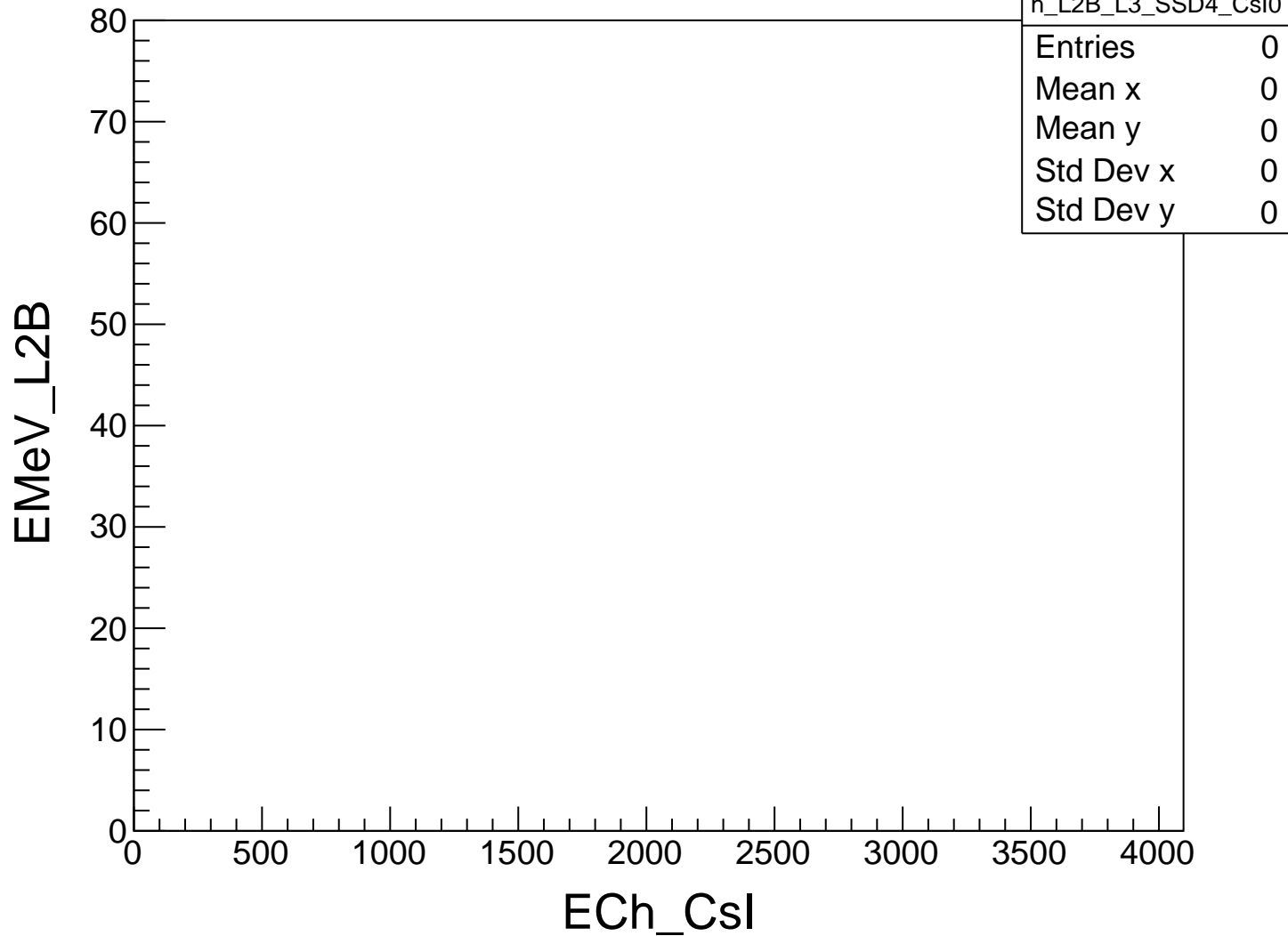
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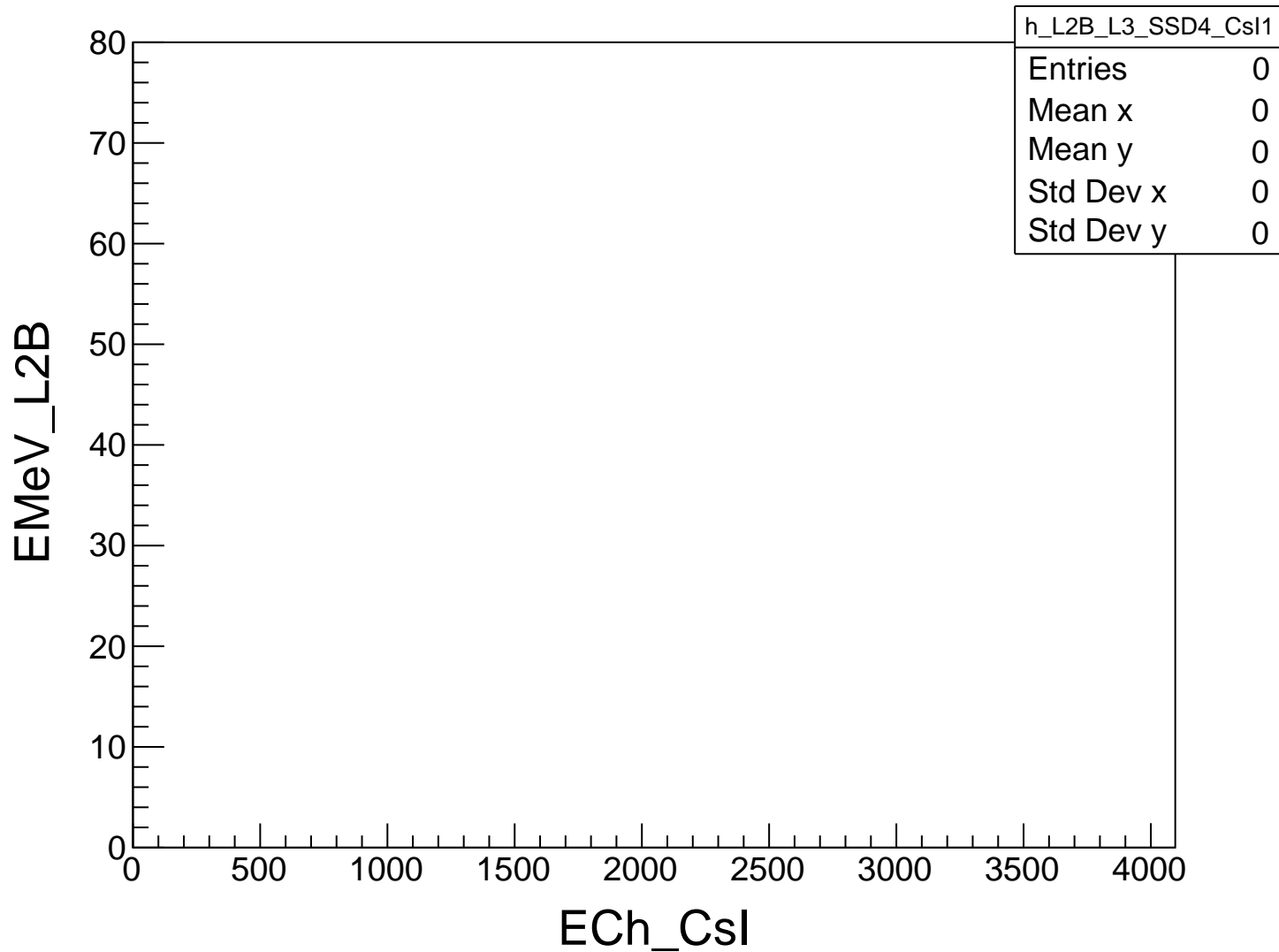
h_L2B_L3_SSD3_CsI8



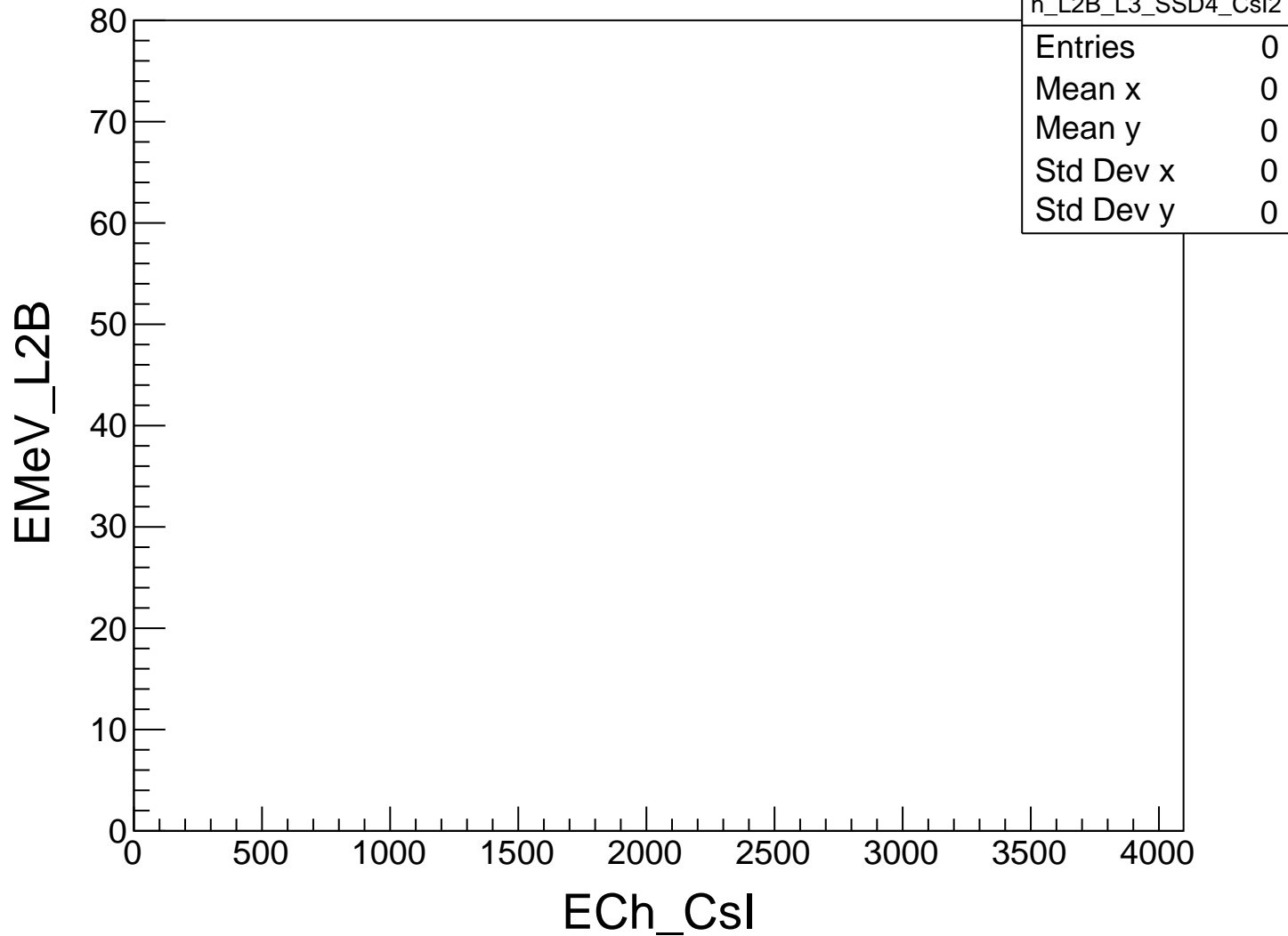
h_L2B_L3_SSD4_CsI0



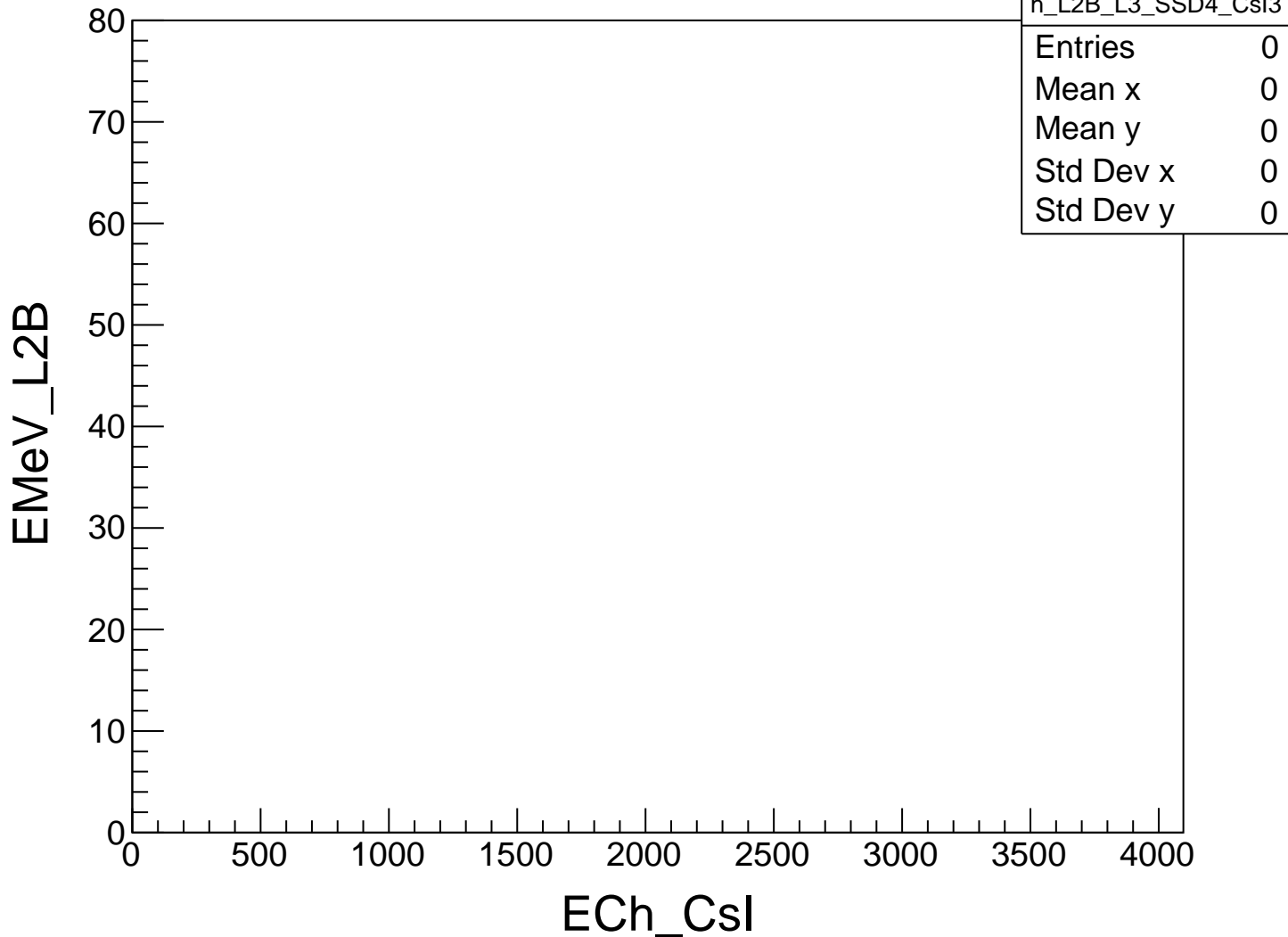
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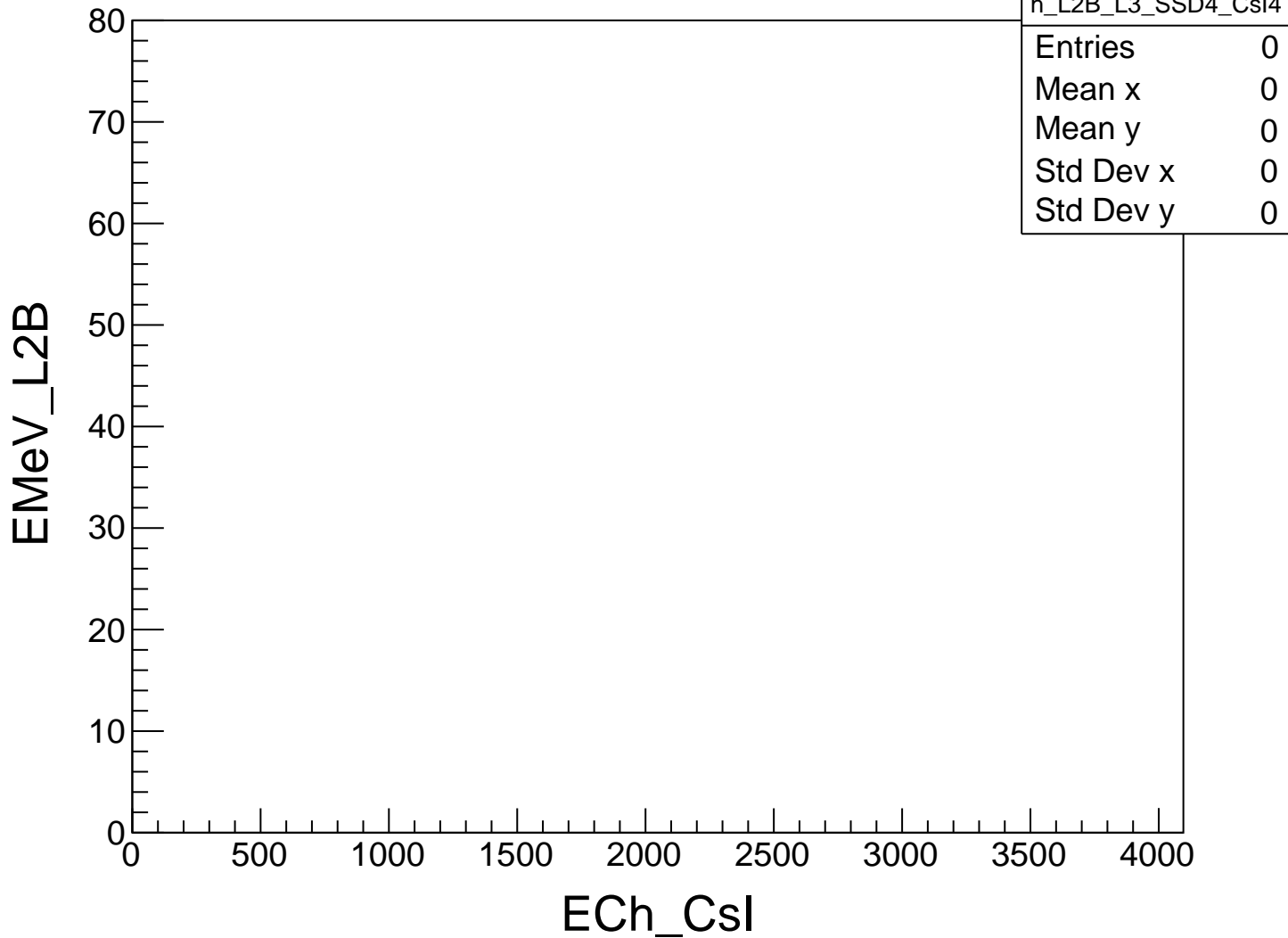
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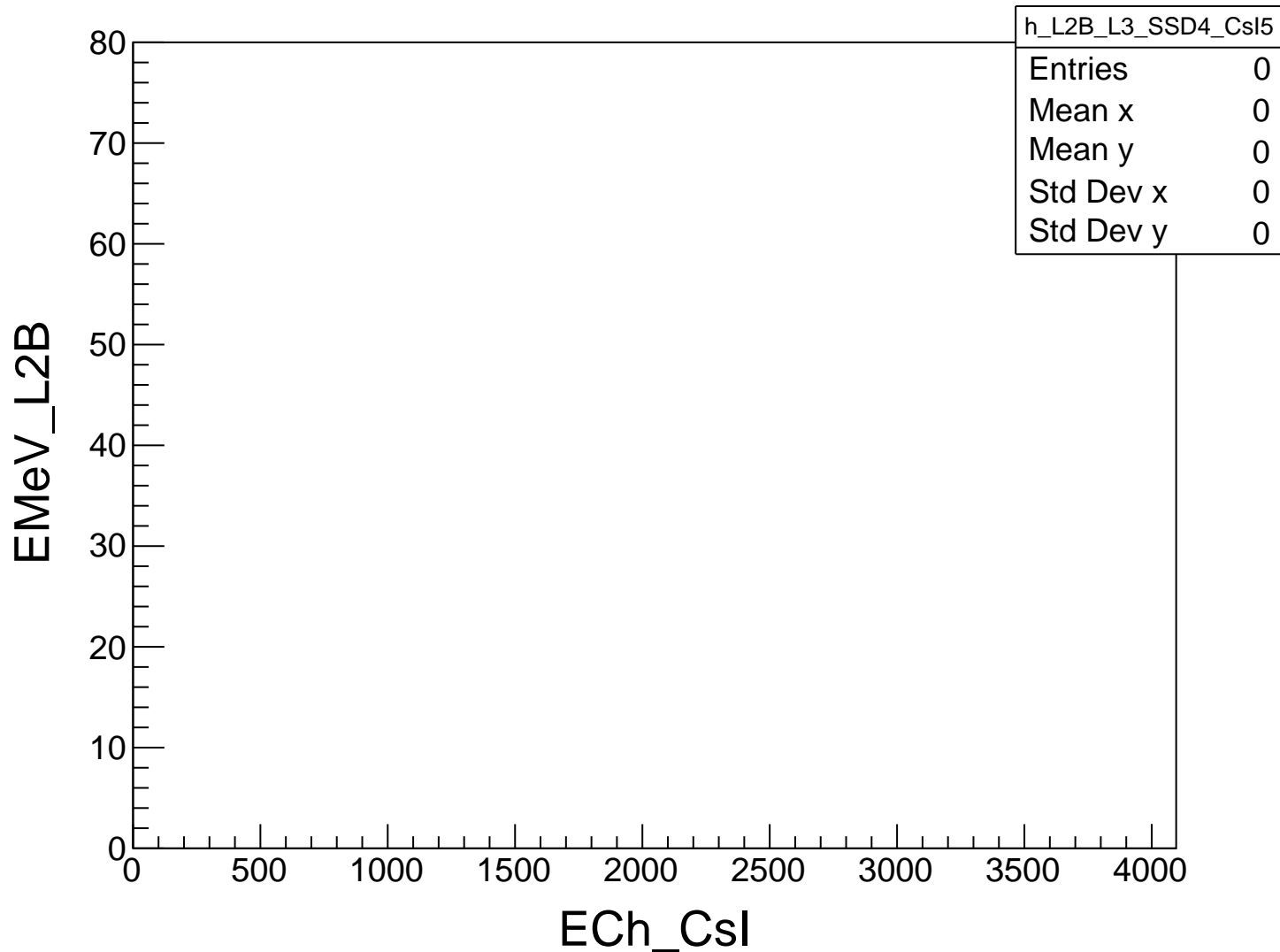
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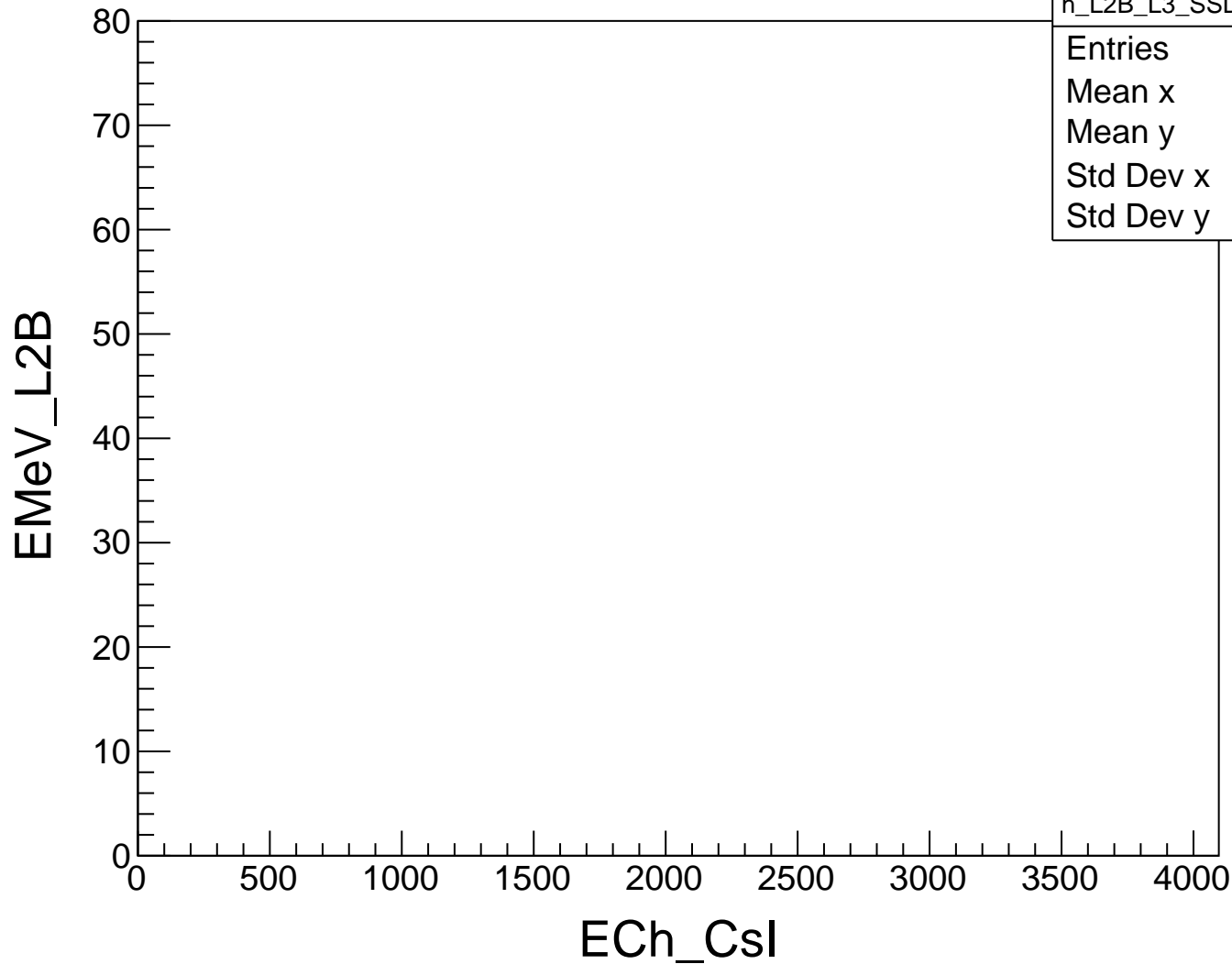
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h_L2B_L3_SSD4_CsI5

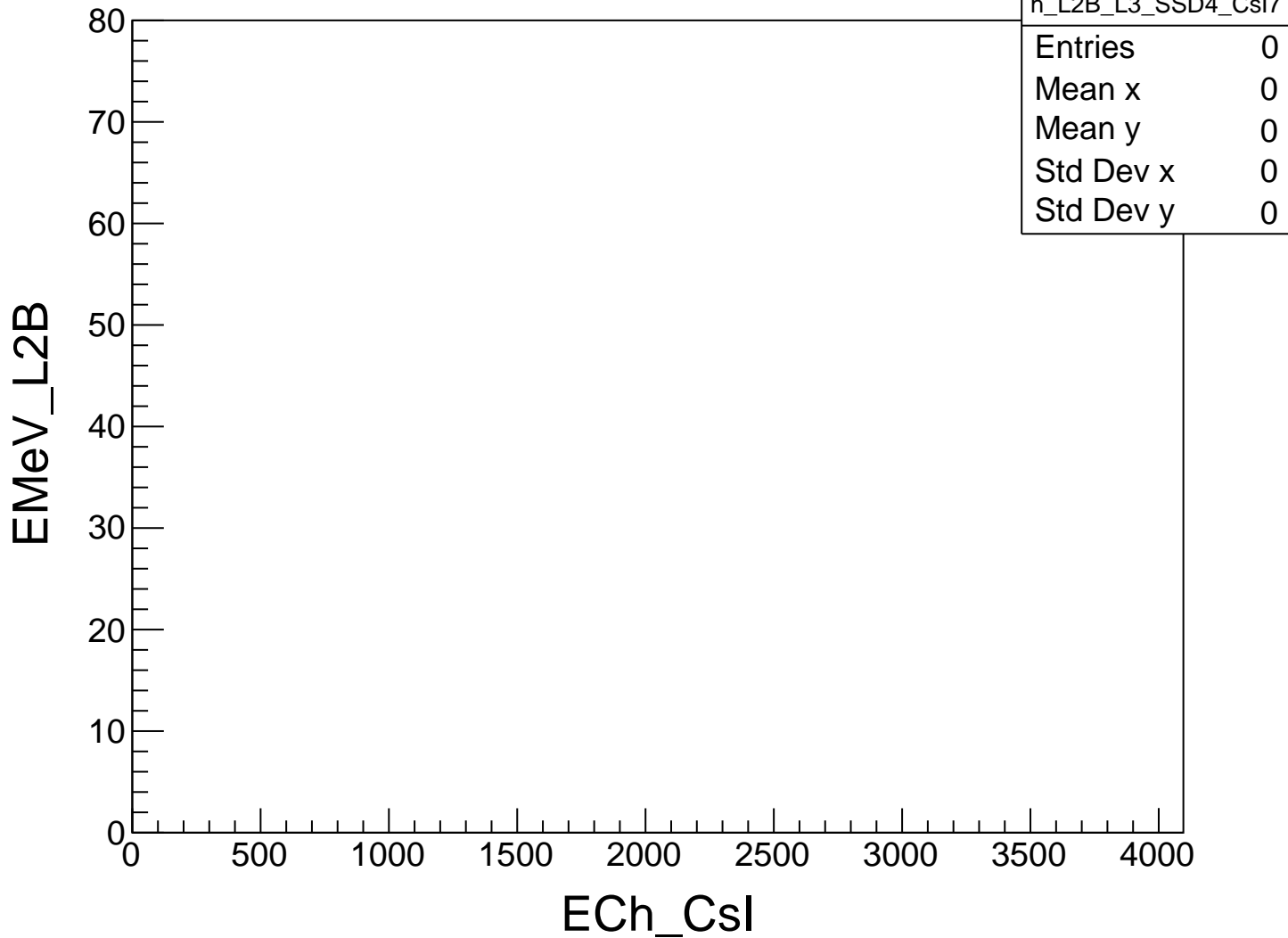


h_L2B_L3_SSD4_CsI6



h_L2B_L3_SSD4_CsI6	
Entries	0
Mean x	0
Mean y	0
Std Dev x	0
Std Dev y	0

h_L2B_L3_SSD4_CsI7



h_L2B_L3_SSD4_CsI8

