

h_L1_L2F_SSD1_CH2 h_L1_L2F_SSD1_CH2 250 20022 **Entries** 34.18 Mean x Mean y 48.2 42.07 Std Dev x 200 Std Dev y 55.26 12 EMeV_L1S 150 10 8 100 6 50

EMeV_L2F

200

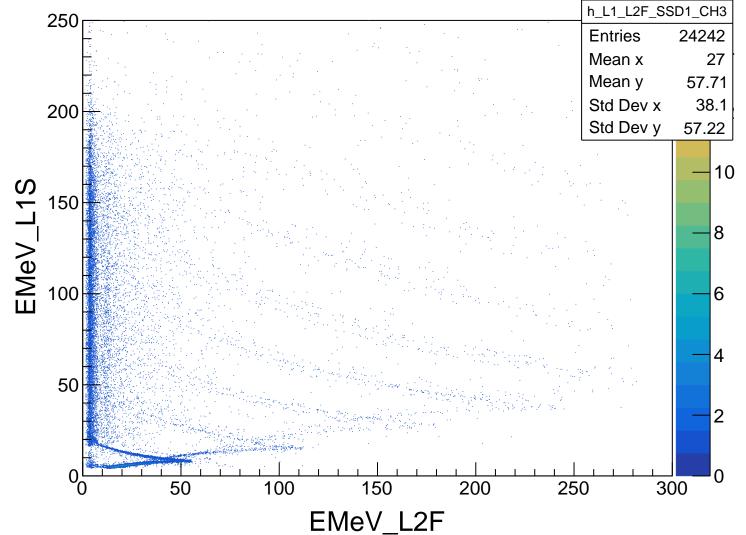
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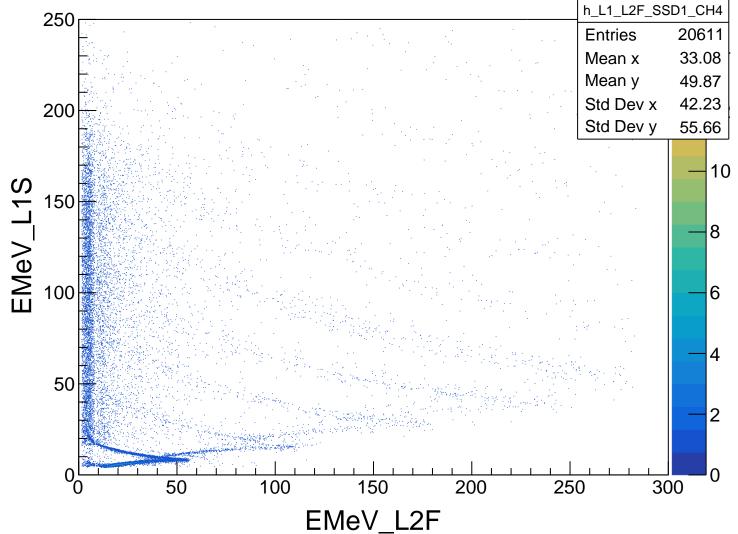
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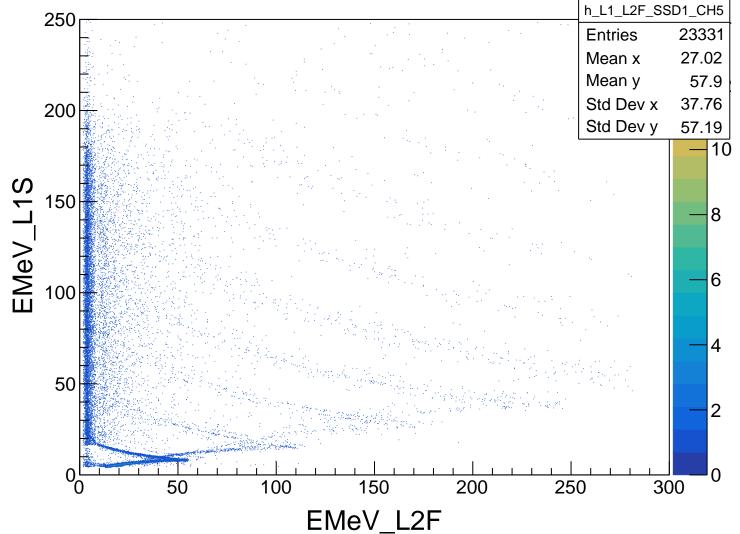
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50

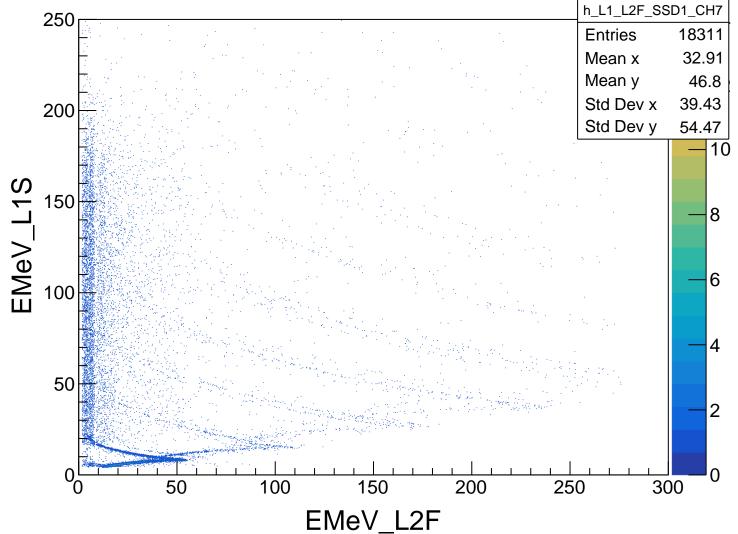
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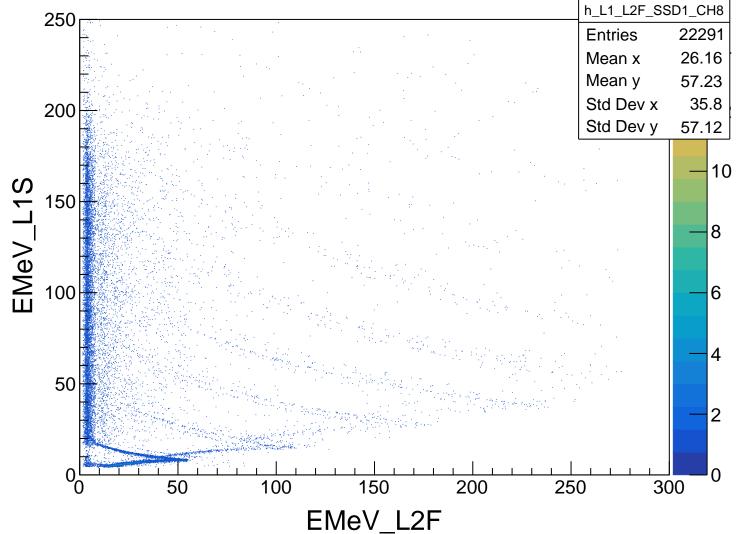


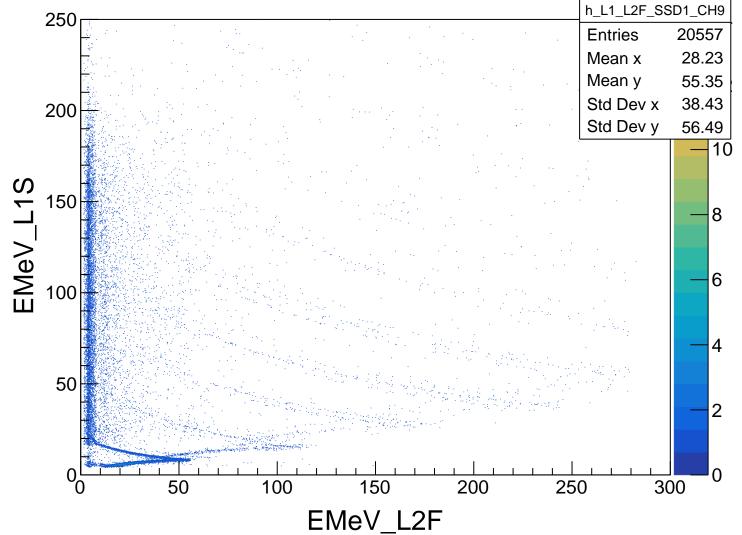


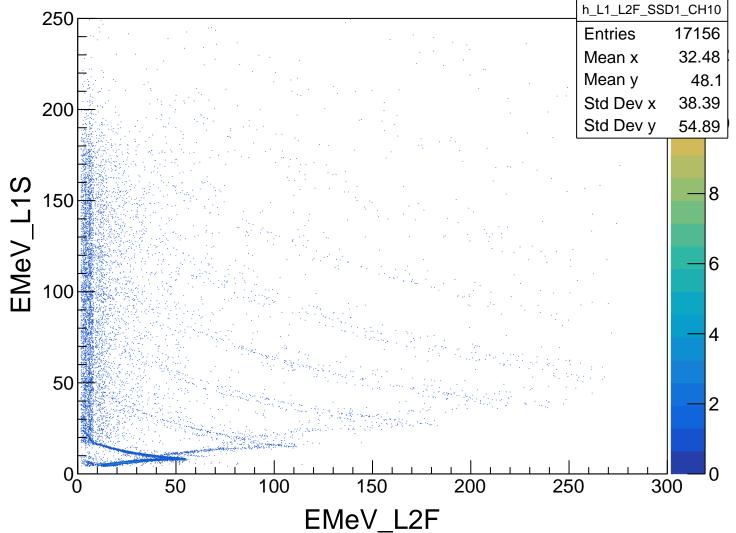


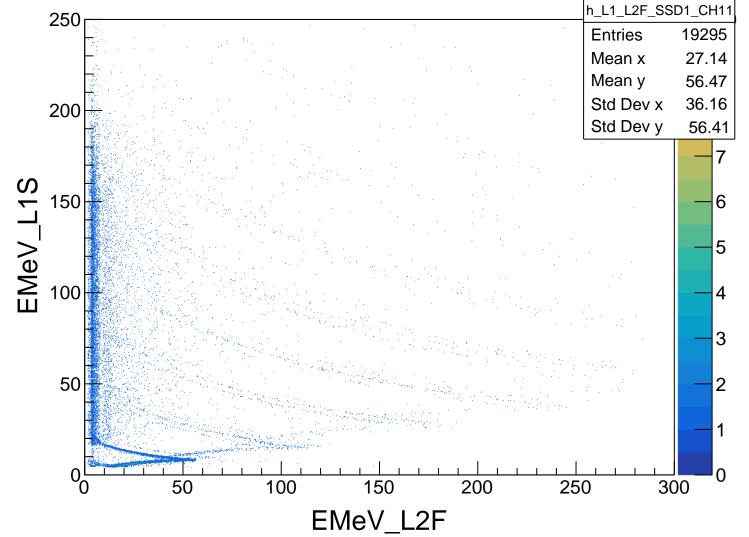
h_L1_L2F_SSD1_CH6 h_L1_L2F_SSD1_CH6 250 21754 **Entries** Mean x 29.36 Mean y 54.21 40.2 Std Dev x 200 Std Dev y 56.66 EMeV_L1S 10 150 8 100 6 4 50 300 50 150 200 250 100 EMeV_L2F

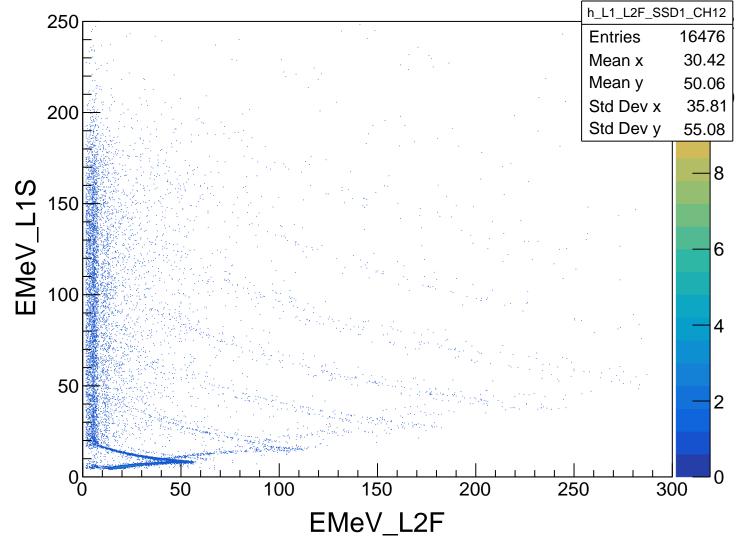


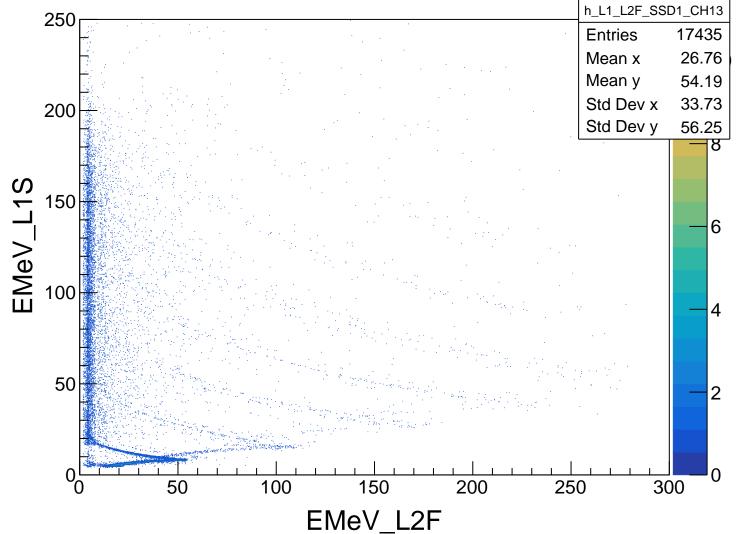












h_L1_L2F_SSD1_CH14 h_L1_L2F_SSD1_CH14 **Entries** 14006 Mean x 32.28 46.86 Mean y 36.74 Std Dev x Std Dev y 54.25 6

200

250

300



100

150

250

200

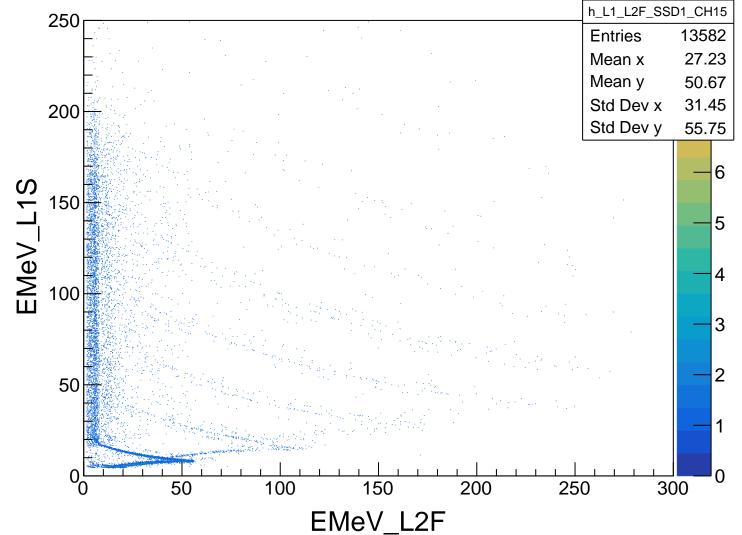
150

100

50

50

EMeV_L1S



h_L1_L2F_SSD2_CH0 h_L1_L2F_SSD2_CH0 200 **Entries** 4366 Mean x 11.22 180 Mean y 34.65 12.83 Std Dev x 160 Std Dev y 28.1 5 140 EMeV_L1S 120 4 100 3 80 60 40 20 50 100 150 200 250 EMeV_L2F

h_L1_L2F_SSD2_CH1 h_L1_L2F_SSD2_CH1 **Entries** 3735 Mean x 8.487 Mean y 33.36 10.66 Std Dev x Std Dev y 27.44 8 6 4

200

180

160

140

120

100

80

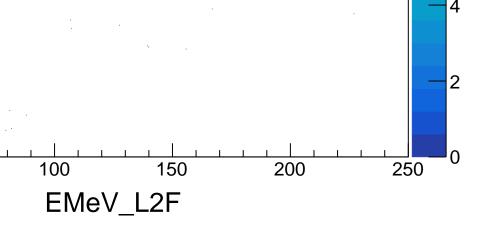
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40

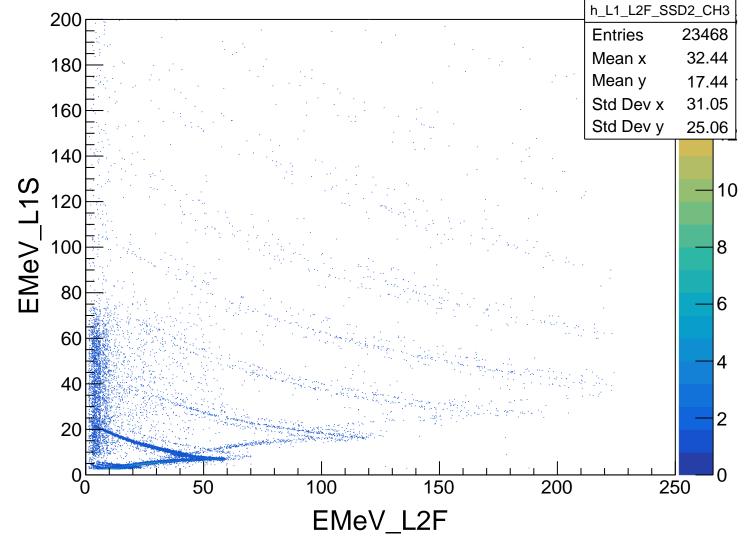
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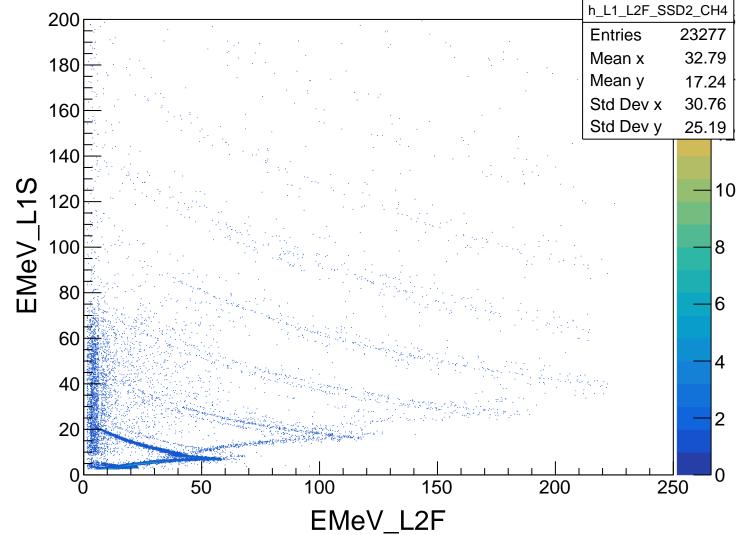
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EMeV_L1S

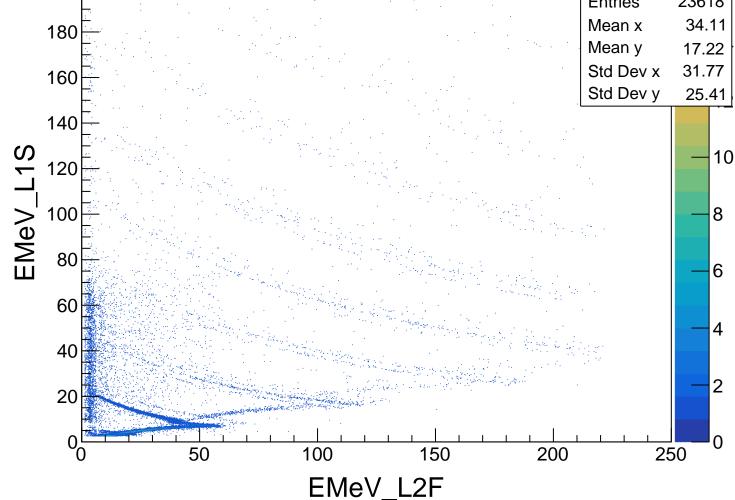


h_L1_L2F_SSD2_CH2 h_L1_L2F_SSD2_CH2 **Entries** Mean x 32.37 Mean y 17.27 Std Dev x 30.58 Std Dev y 24.95 EMeV_L1S EMeV_L2F

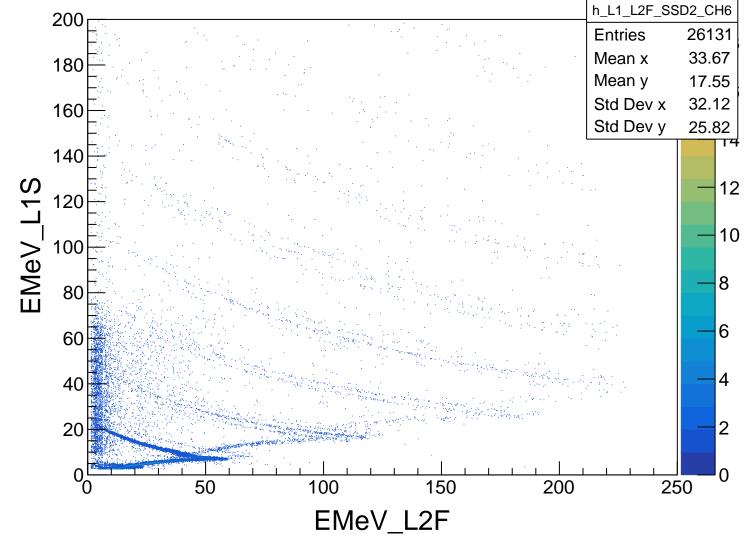


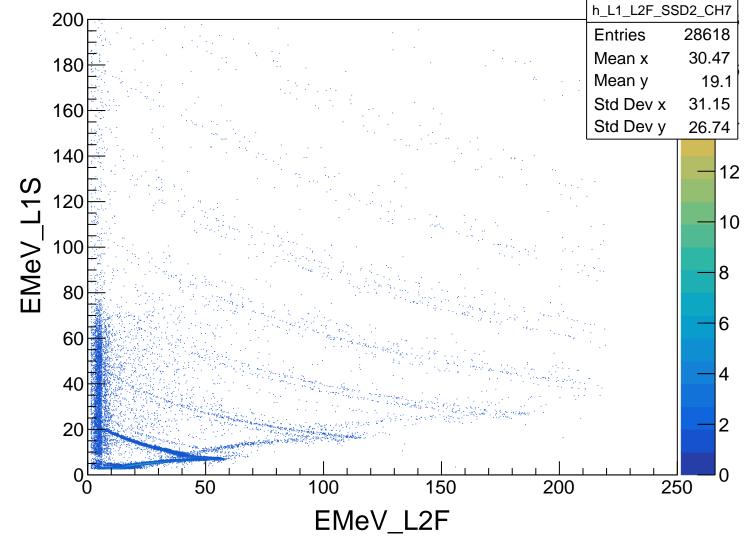


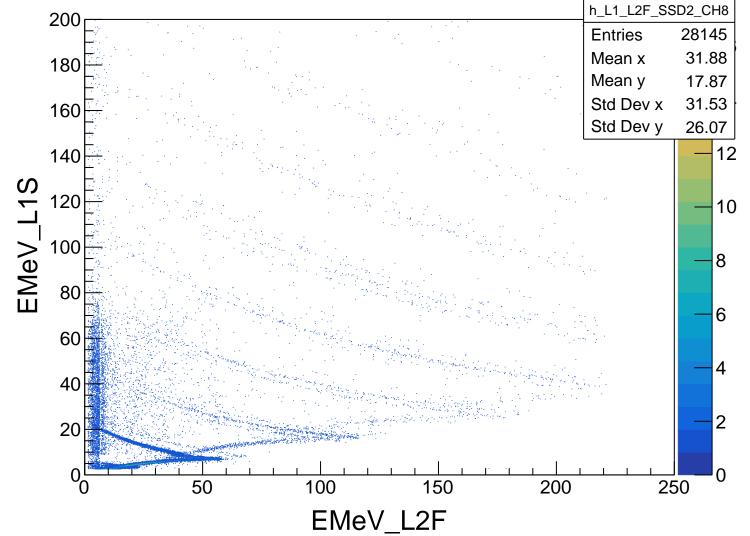
h_L1_L2F_SSD2_CH5 h_L1_L2F_SSD2_CH5 **Entries** 23618 Mean x 34.11 Mean y 17.22 31.77 Std Dev x Std Dev y 25.41 8



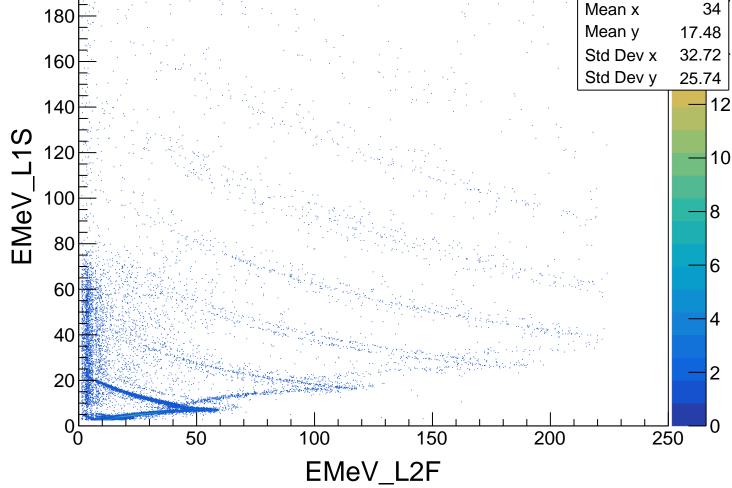
200







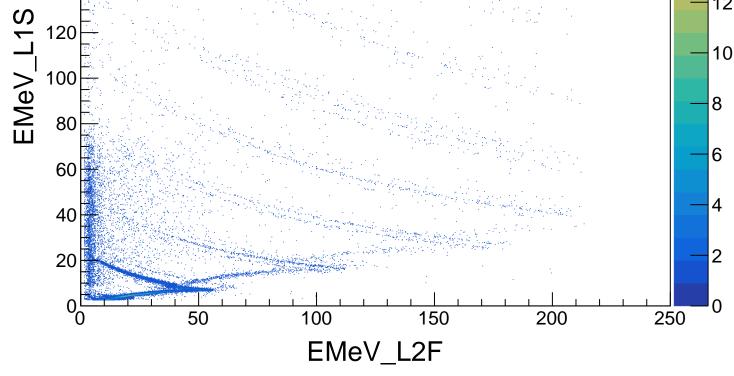
h_L1_L2F_SSD2_CH9 h_L1_L2F_SSD2_CH9 **Entries** 27098 Mean x Mean y Std Dev x Std Dev y



200

h_L1_L2F_SSD2_CH10 h_L1_L2F_SSD2_CH10 **Entries** Mean x 34.08 Mean y 17.46 Std Dev x 32.59 Std Dev y 26.12 EMeV_L1S EMeV_L2F

h_L1_L2F_SSD2_CH11 h_L1_L2F_SSD2_CH11 **Entries** 28399 Mean x 32.32 Mean y 17.42 30.91 Std Dev x Std Dev y 26.17 12 8 6

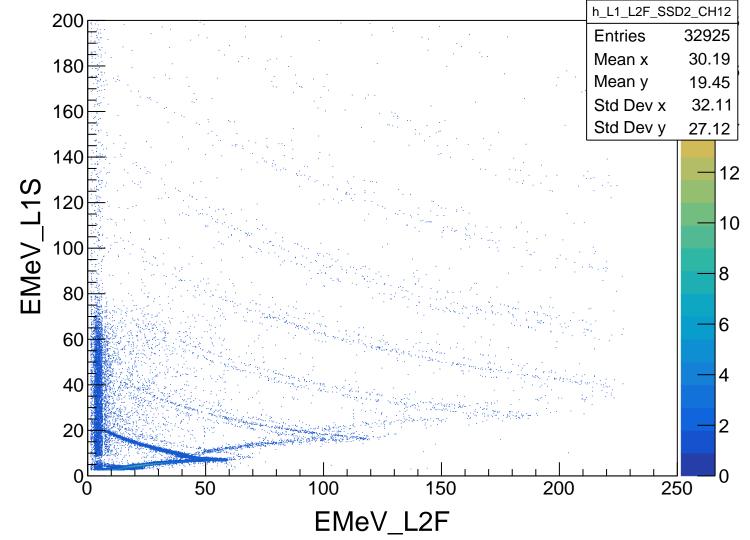


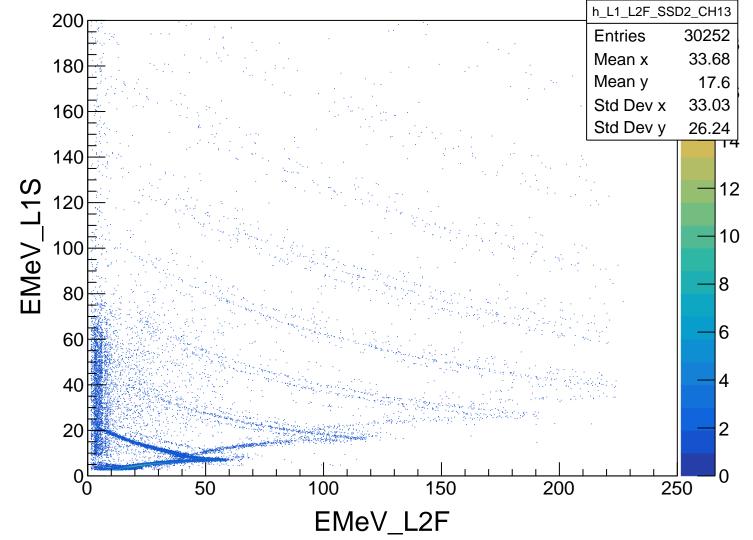
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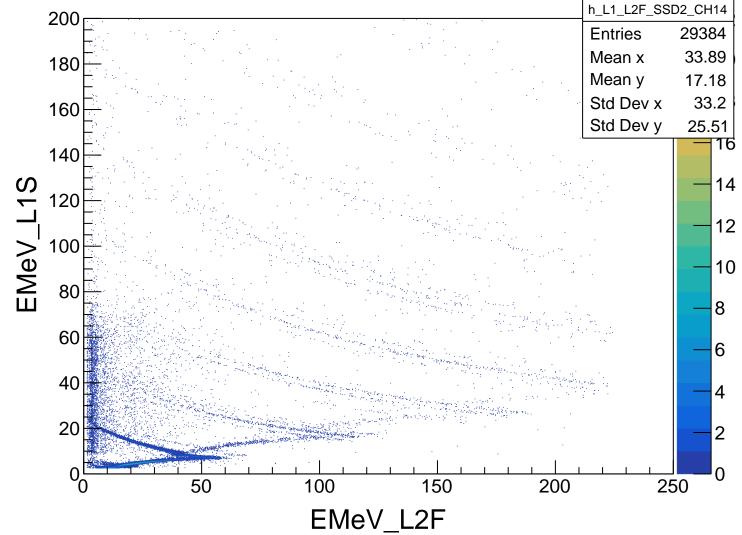
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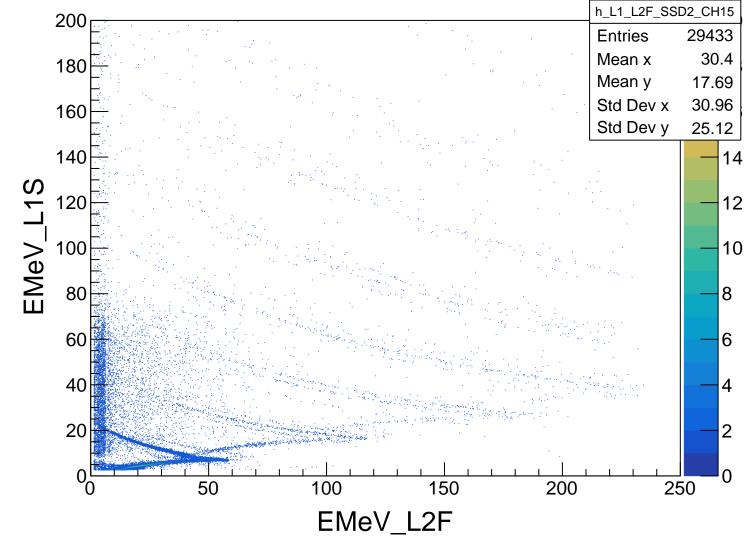
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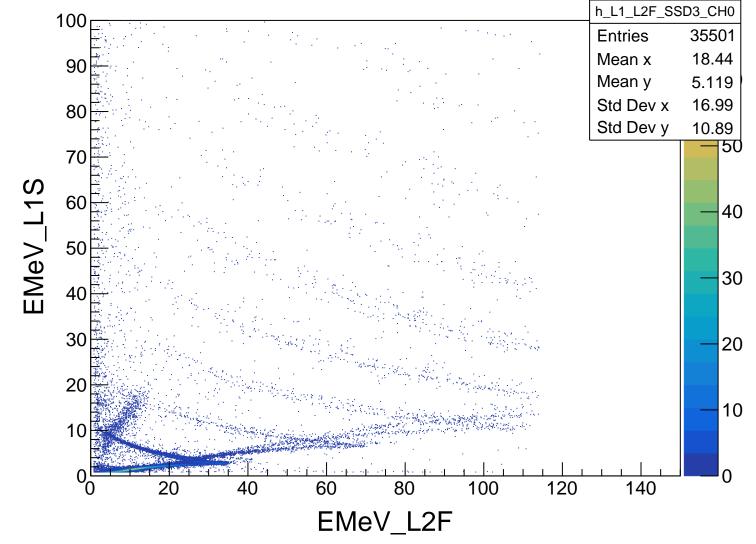
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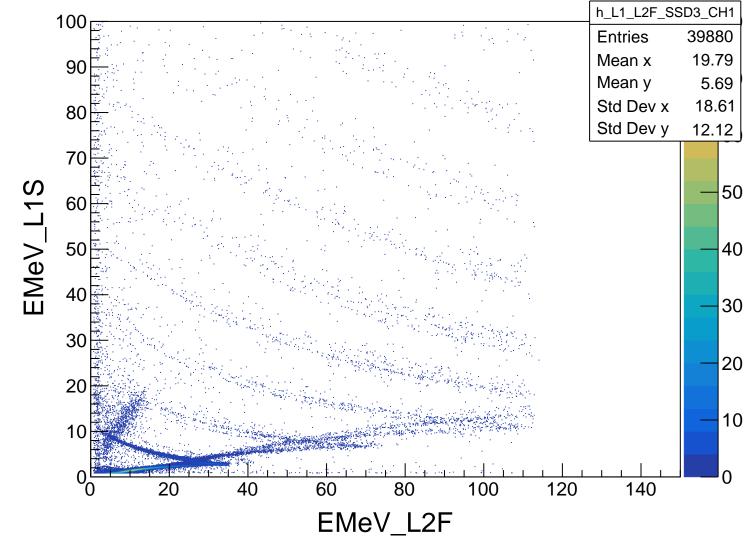


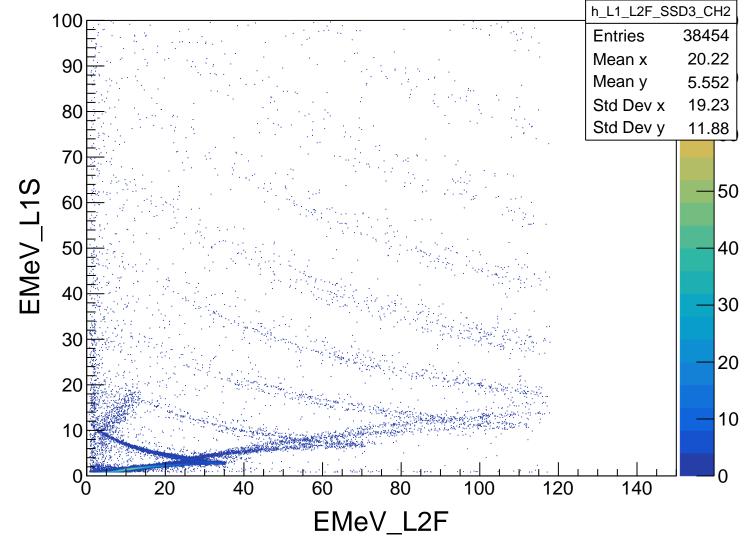


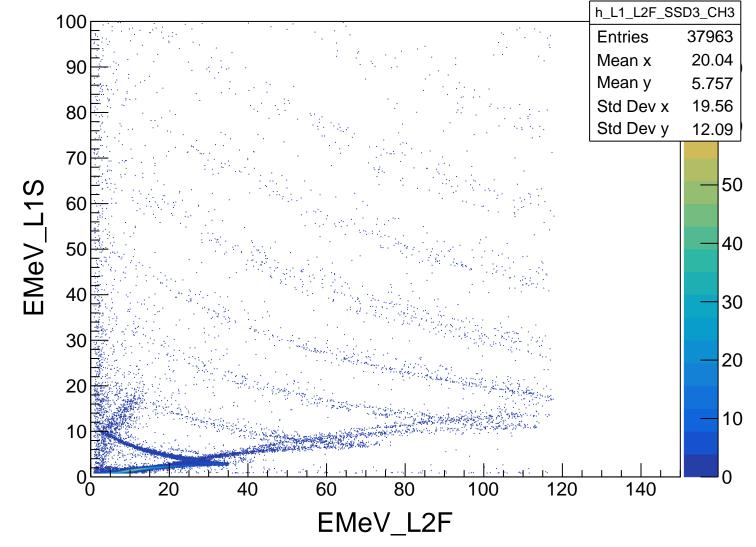


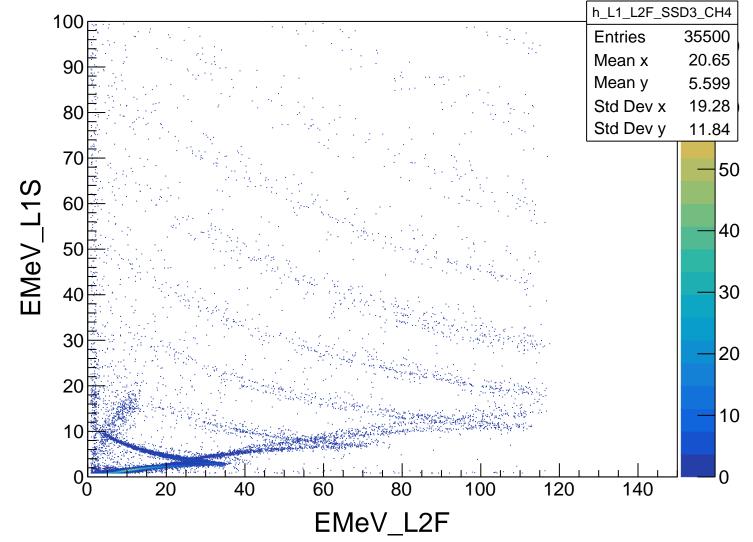


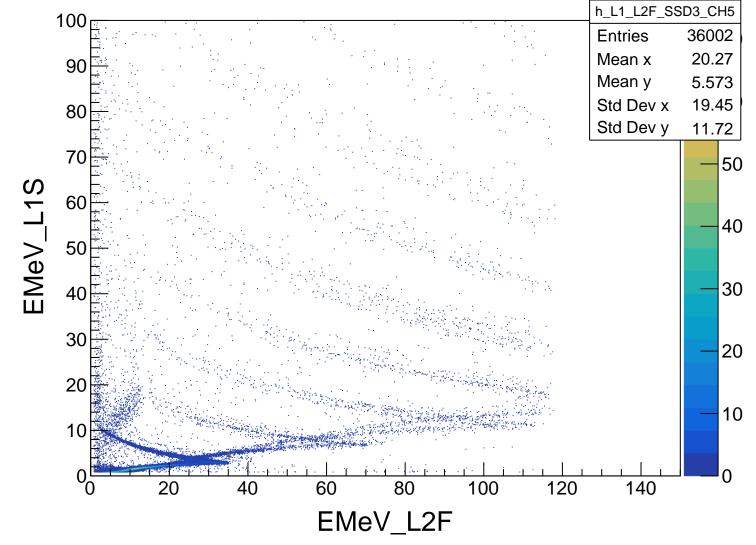


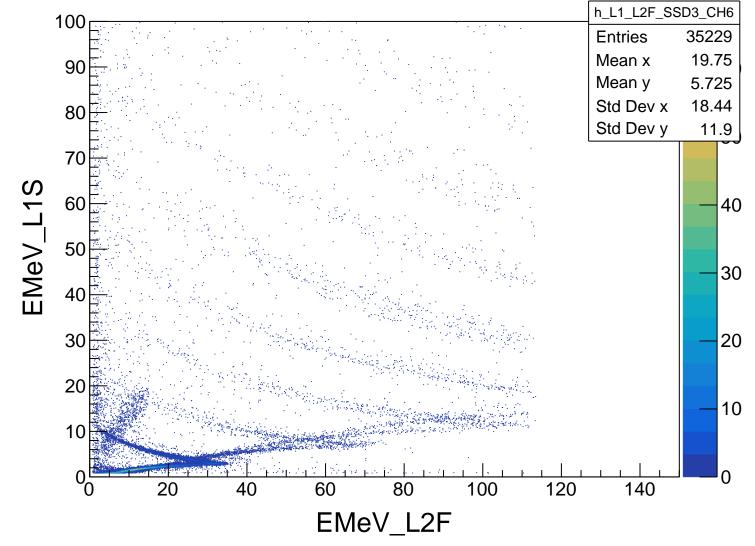


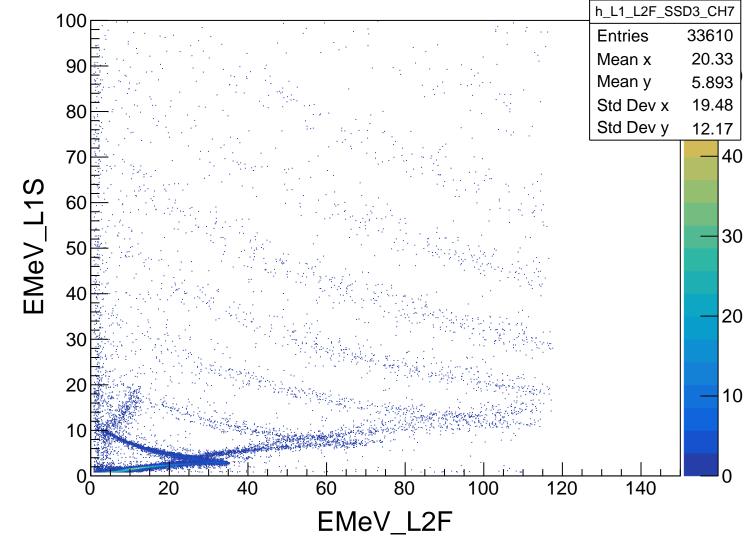


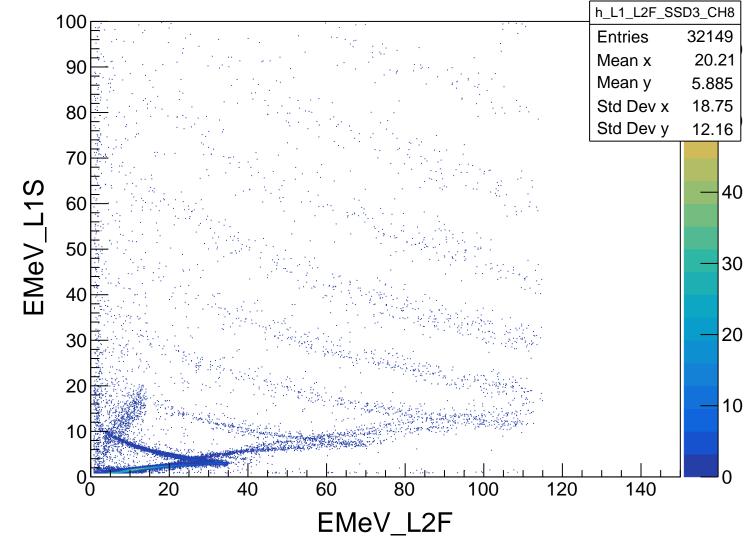


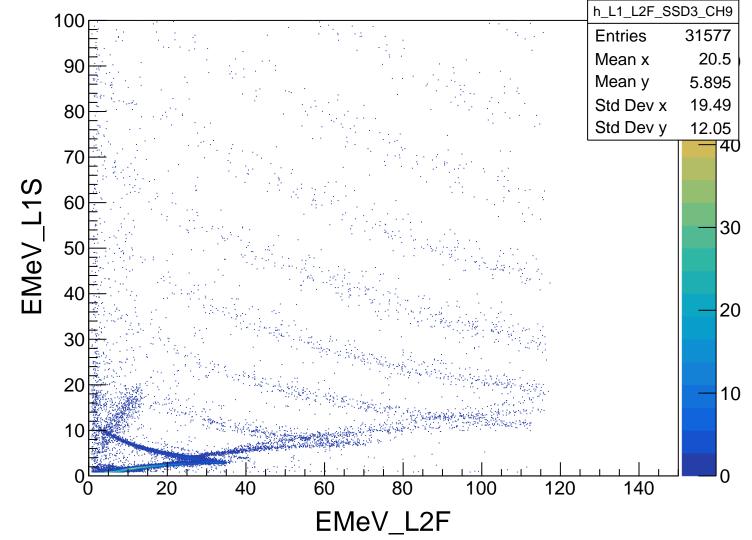


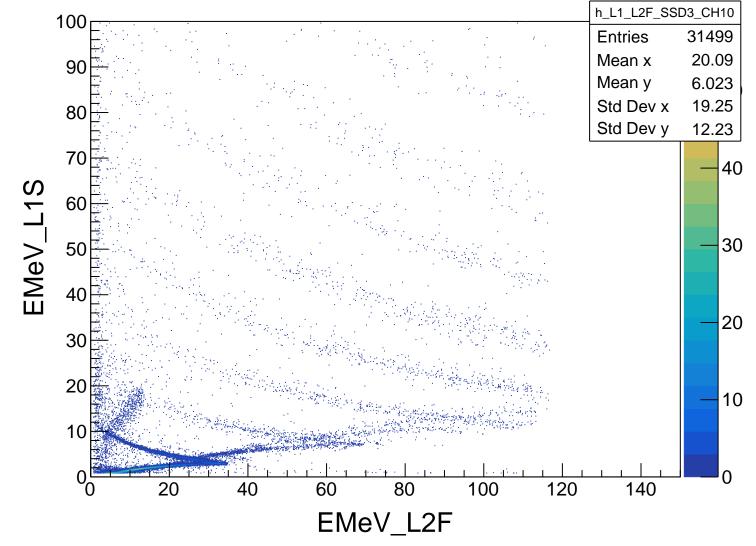


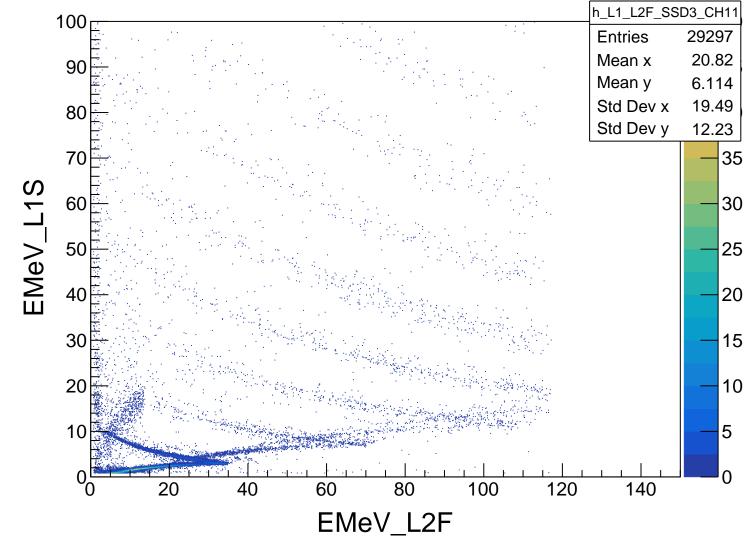


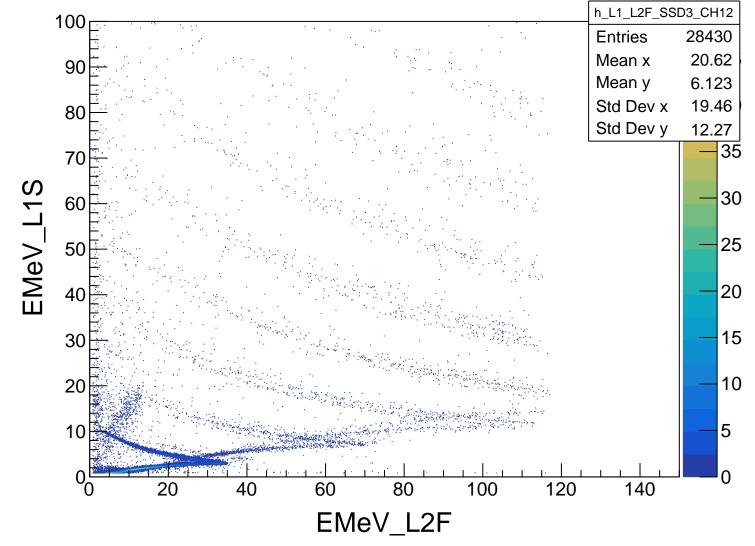


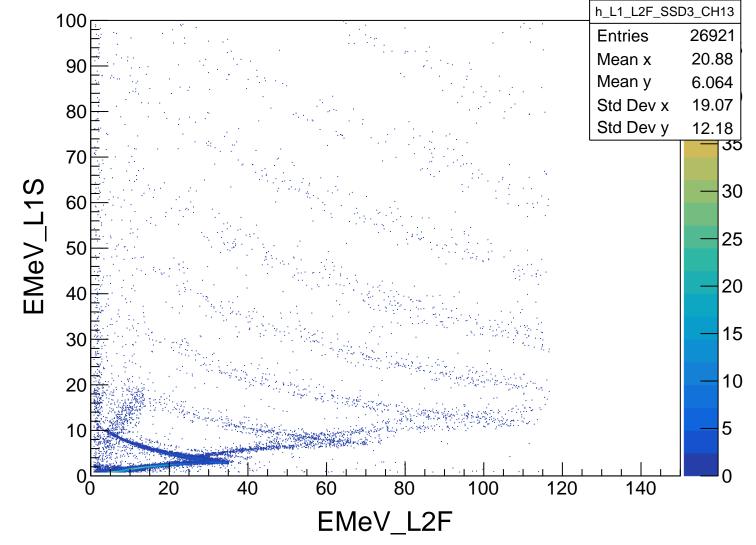


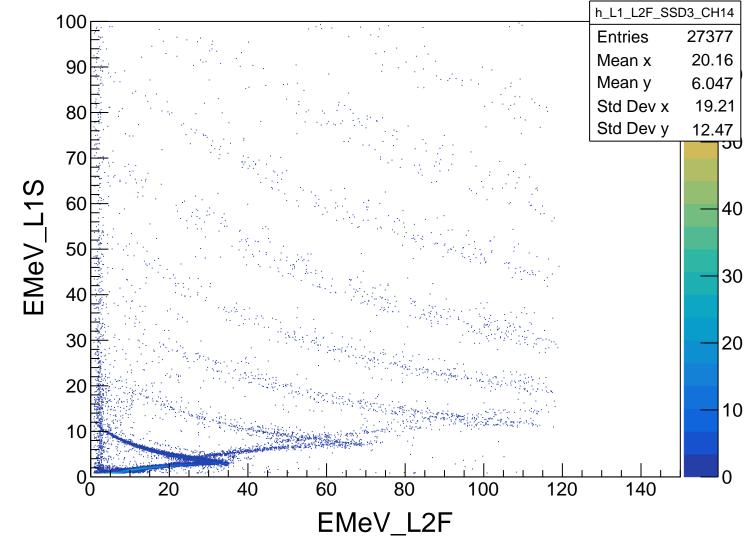


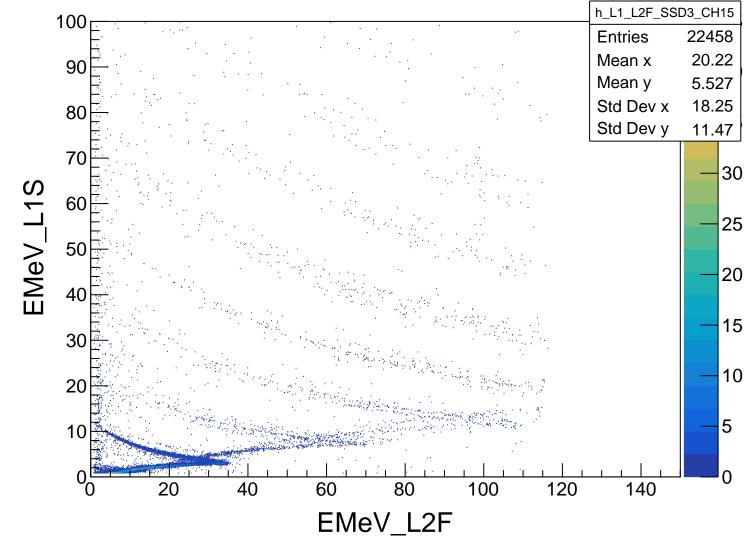


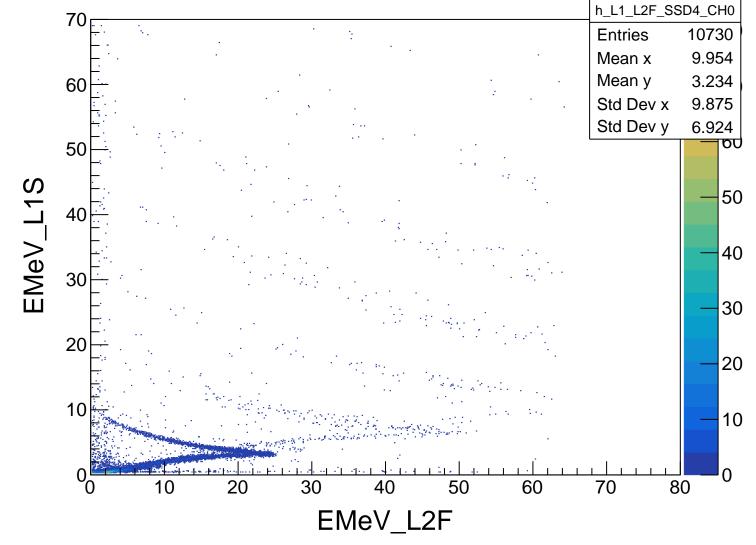












h_L1_L2F_SSD4_CH1 h_L1_L2F_SSD4_CH1 70 **Entries** 11987 Mean x 9.686 3.039 Mean y 60 9.57 Std Dev x Std Dev y 6.18 50 80 EMeV_L1S 40 60 30 40 20 20 80 60 70 20 30 40 50 EMeV_L2F

h_L1_L2F_SSD4_CH2 h_L1_L2F_SSD4_CH2 **Entries** 13506 Mean x 9.177 Mean y 3.035 60 9.663 Std Dev x Std Dev y 6.7 50 80 EMeV_L1S 40 60 30 40 20 20 10 80 30 70 20 40 50 60 EMeV_L2F

h_L1_L2F_SSD4_CH3 h_L1_L2F_SSD4_CH3 70 **Entries** 14139 Mean x 9.263 3.099 Mean y 60 9.936 Std Dev x Std Dev y 6.64 TU0 50 EMeV_L1S 80 40 60 30 40 20 10 20 80 70 20 30 40 50 60 10 EMeV_L2F

h_L1_L2F_SSD4_CH4 h_L1_L2F_SSD4_CH4 70_E **Entries** 14913 Mean x 9.263 Mean y 3.317 60 9.763 0 Std Dev x Std Dev y 7.27 50 80 EMeV_L1S 40 60 30 40 20 20 10 80 30 70 10 20 40 50 60 EMeV_L2F

h_L1_L2F_SSD4_CH5 h_L1_L2F_SSD4_CH5 70 **Entries** 14438 9.698 Mean x 3.21 Mean y 60 9.897 Std Dev x Std Dev y 6.682 50 80 EMeV_L1S 40 60 30 40 20 20 10 80 30 70 20 40 50 60 EMeV_L2F

h_L1_L2F_SSD4_CH6 h_L1_L2F_SSD4_CH6 **Entries** Mean x 9.517 3.213 0 Mean y 9.902 Std Dev x Std Dev y 6.721 EMeV_L1S EMeV_L2F

h_L1_L2F_SSD4_CH7 h_L1_L2F_SSD4_CH7 **Entries** Mean x 8.819 Mean y 3.196 Std Dev x 9.599 Std Dev y 7.031 0 EMeV_L1S EMeV_L2F

h_L1_L2F_SSD4_CH8 h_L1_L2F_SSD4_CH8 70₁ **Entries** 18442 Mean x 8.786 Mean y 3.28 60 Std Dev x 9.471 7.152_{0} Std Dev y 50 EMeV_L1S 100 40 80 30 60 20 40 10 20 80 30 50 70 10 20 40 60 EMeV_L2F

h_L1_L2F_SSD4_CH9 h_L1_L2F_SSD4_CH9 70_F **Entries** 17976 Mean x 9.347 0 Mean y 3.494 60 Std Dev x 9.658 Std Dev y 7.297 0 50 EMeV_L1S 80 40 60 30 40 20 20 10 80 30 70 10 20 40 50 60 EMeV_L2F

h_L1_L2F_SSD4_CH10 h_L1_L2F_SSD4_CH10 70_F **Entries** 20131 8.923 Mean x Mean y 3.273 60 9.646 Std Dev x Std Dev y 6.982 50 100 EMeV_L1S 40 80 30 60 20 40 10 20 80 30 70 10 20 40 50 60 EMeV_L2F

h_L1_L2F_SSD4_CH11 h_L1_L2F_SSD4_CH11 **Entries** Mean x 9.074 Mean y 3.362 9.696 Std Dev x Std Dev y 7.104 EMeV_L1S EMeV_L2F

h_L1_L2F_SSD4_CH12 h_L1_L2F_SSD4_CH12 **Entries** Mean x 8.354 3.07 Mean y 9.387 Std Dev x Std Dev y 6.511 0

EMeV_L1S



h_L1_L2F_SSD4_CH13 h_L1_L2F_SSD4_CH13 **Entries** Mean x 19.54 Mean y 14.6 Std Dev x 16.67 Std Dev y 17.67 EMeV_L1S EMeV_L2F

h_L1_L2F_SSD4_CH14 h_L1_L2F_SSD4_CH14 **Entries** Mean x 17.3 Mean y 14.58 Std Dev x 16.38 Std Dev y 17.27 EMeV_L1S EMeV_L2F

h_L1_L2F_SSD4_CH15 h_L1_L2F_SSD4_CH15 **Entries** Mean x 8.544 0 Mean y 2.924 Std Dev x 9.097 Std Dev y 5.737 0 EMeV_L1S EMeV_L2F