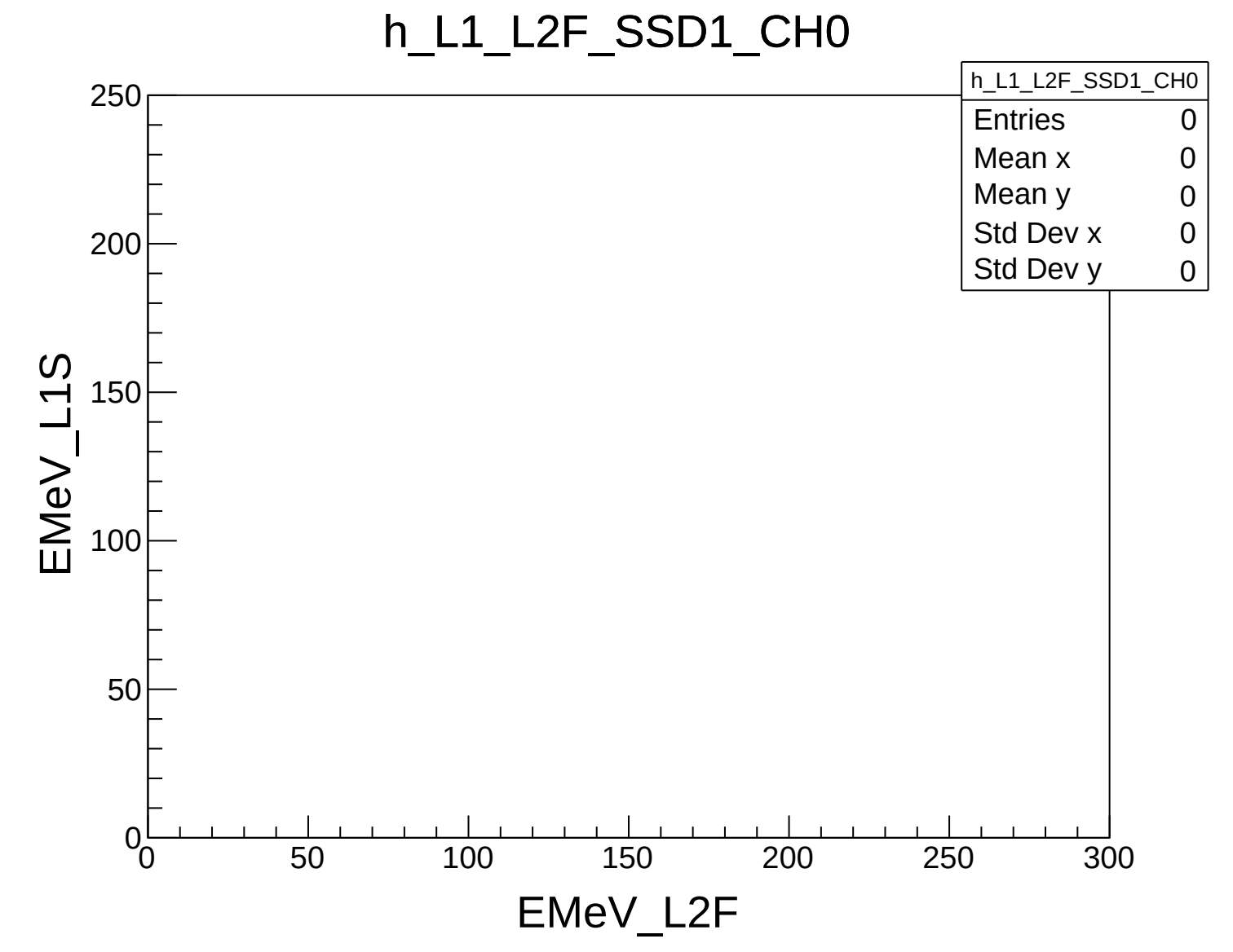
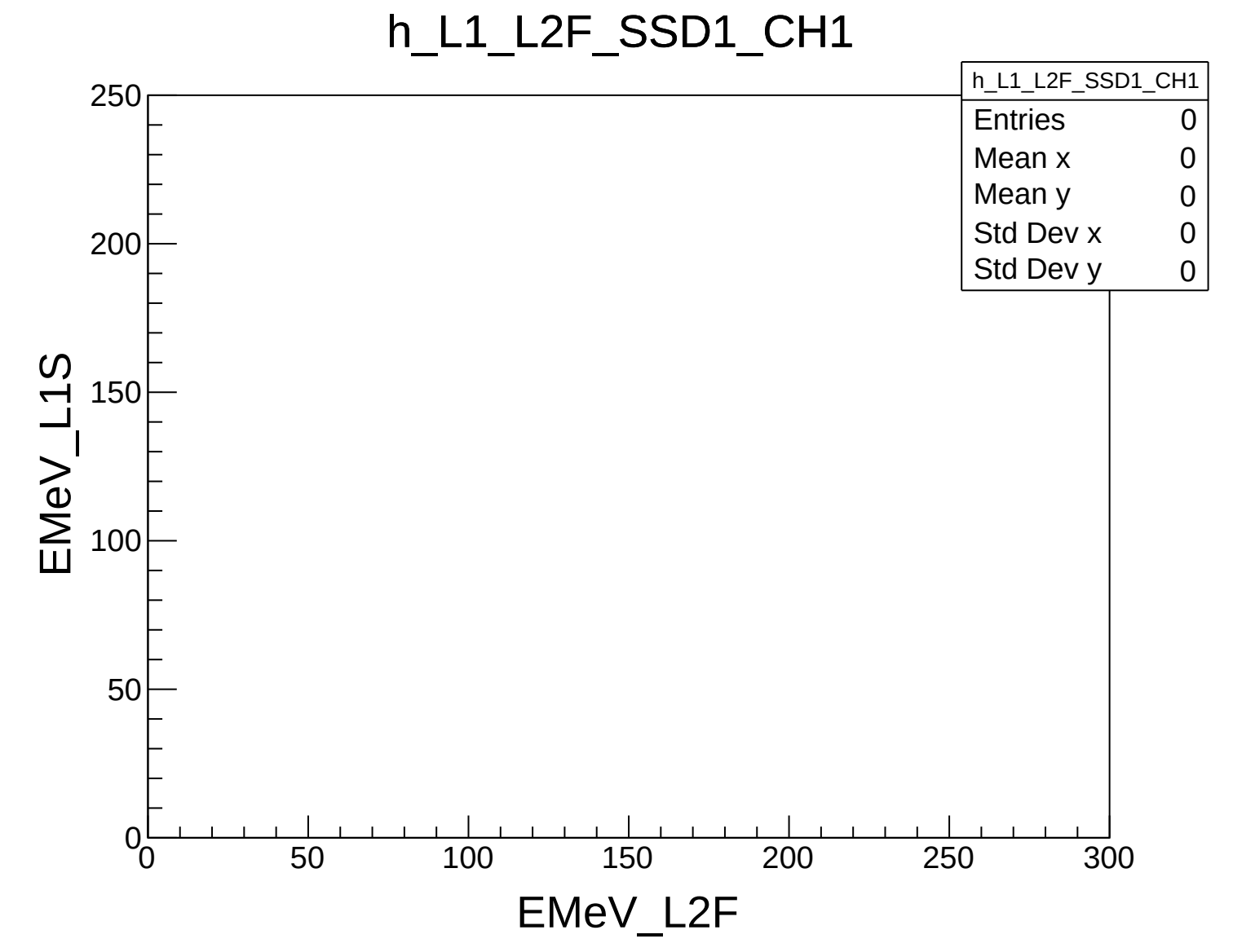
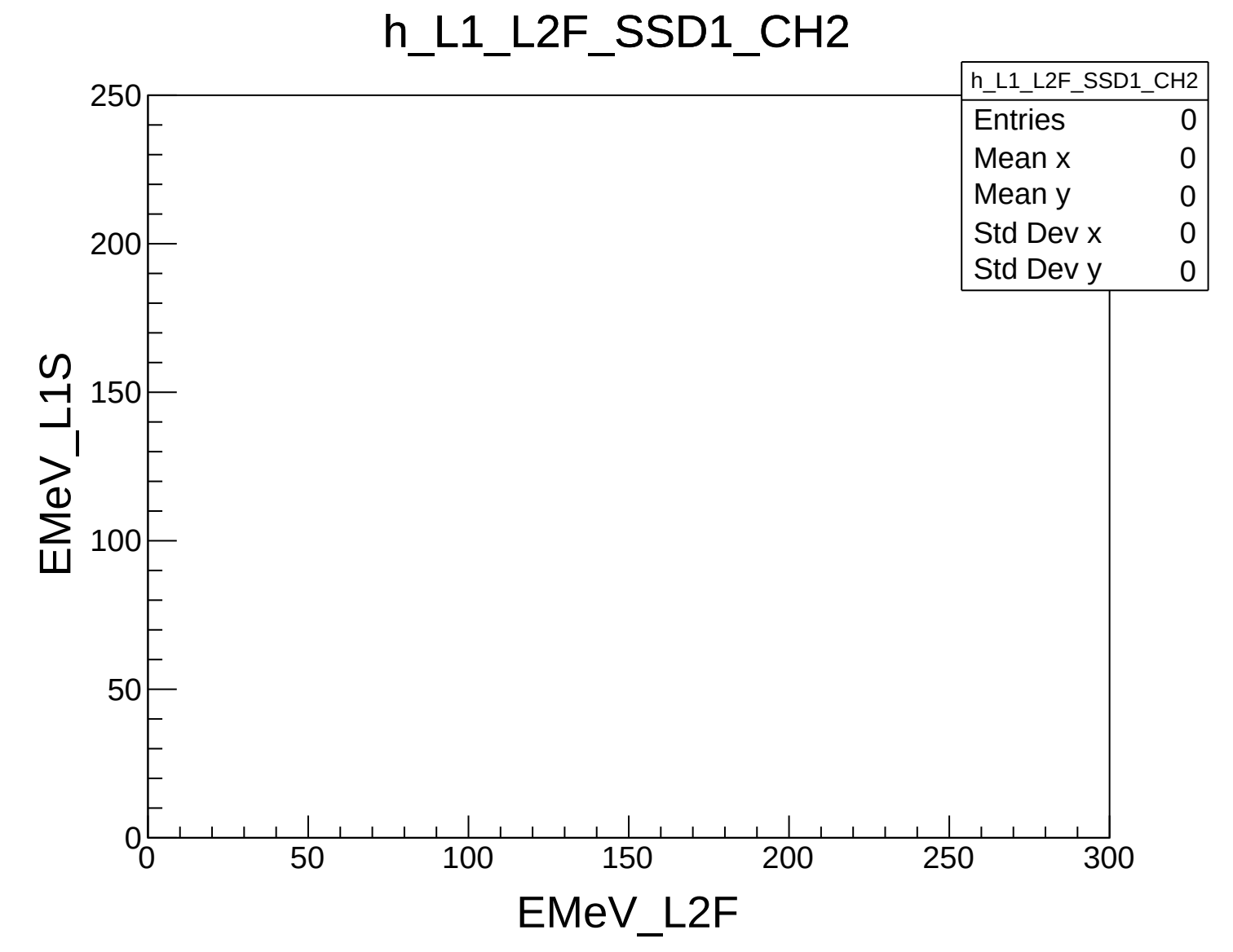
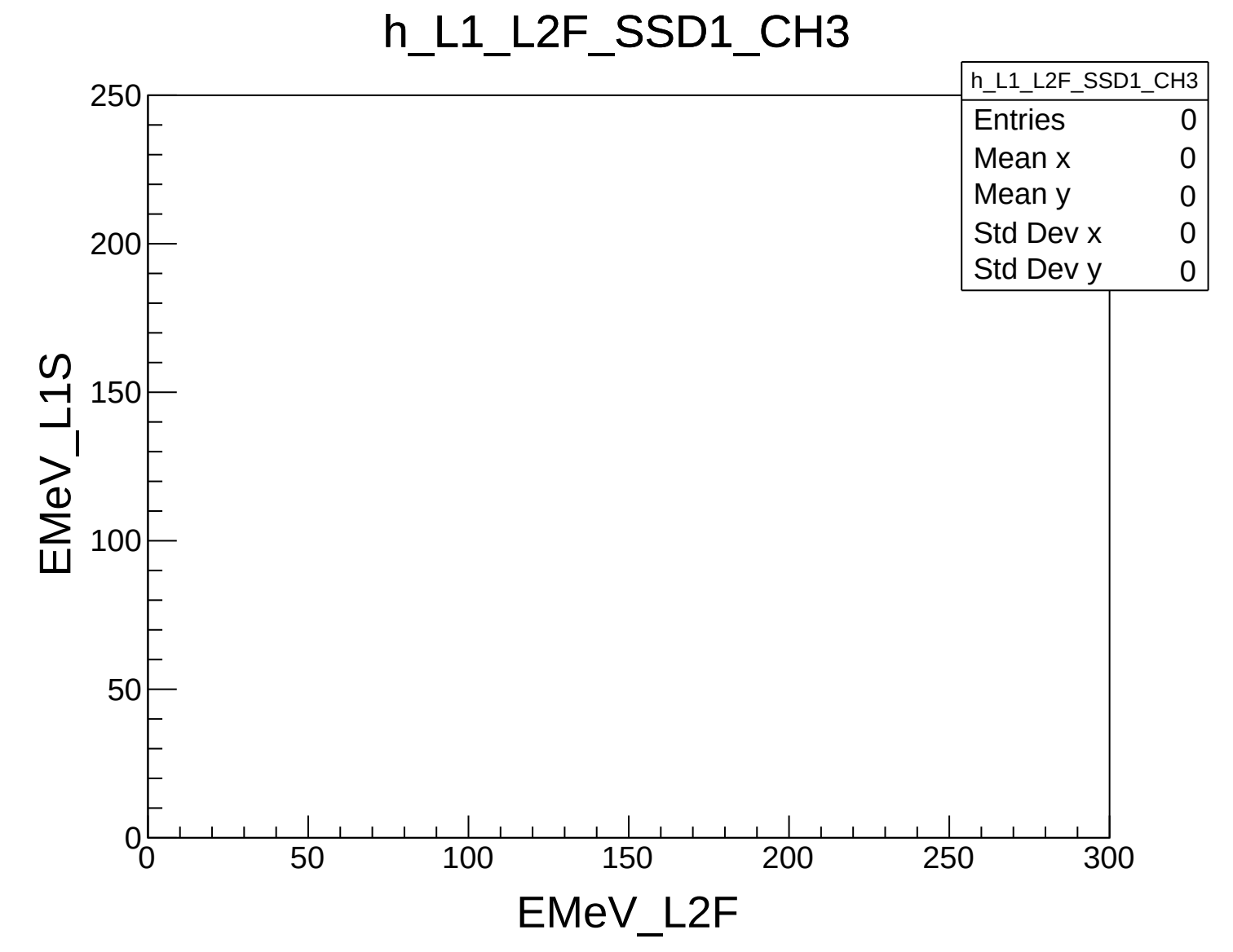
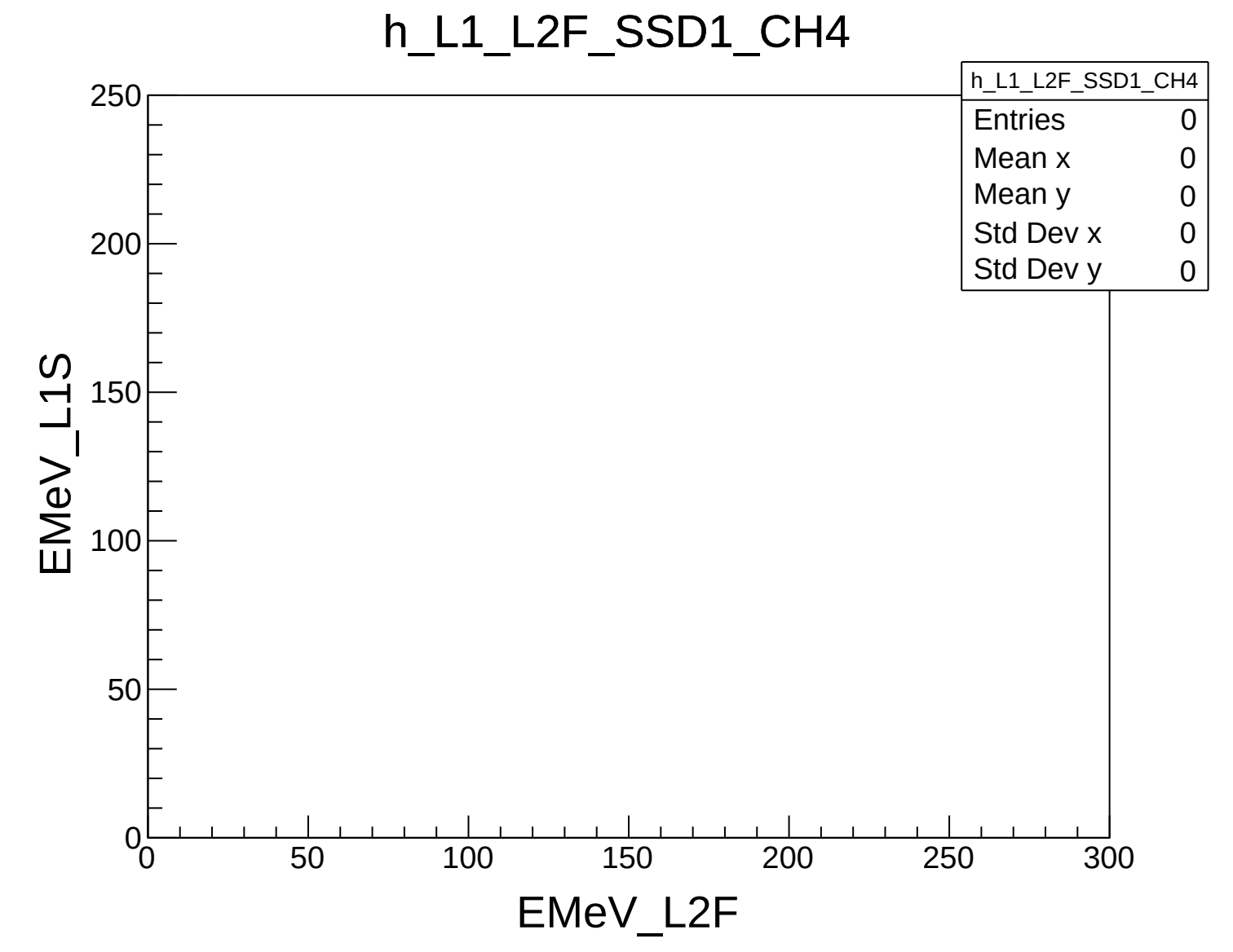
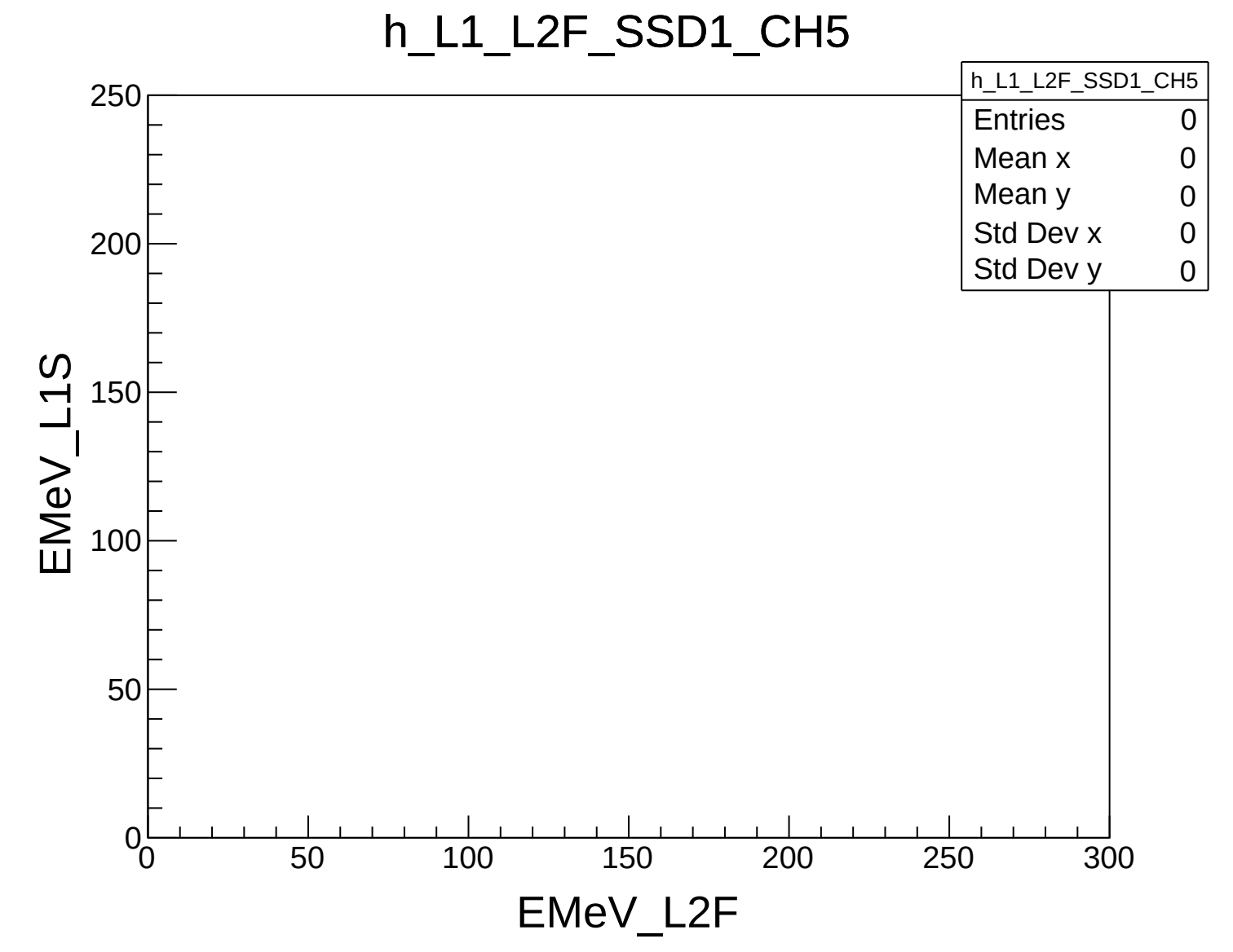

h_L1_L2F_SSD1_CH0
h_L1_L2F_SSD1_CH0
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

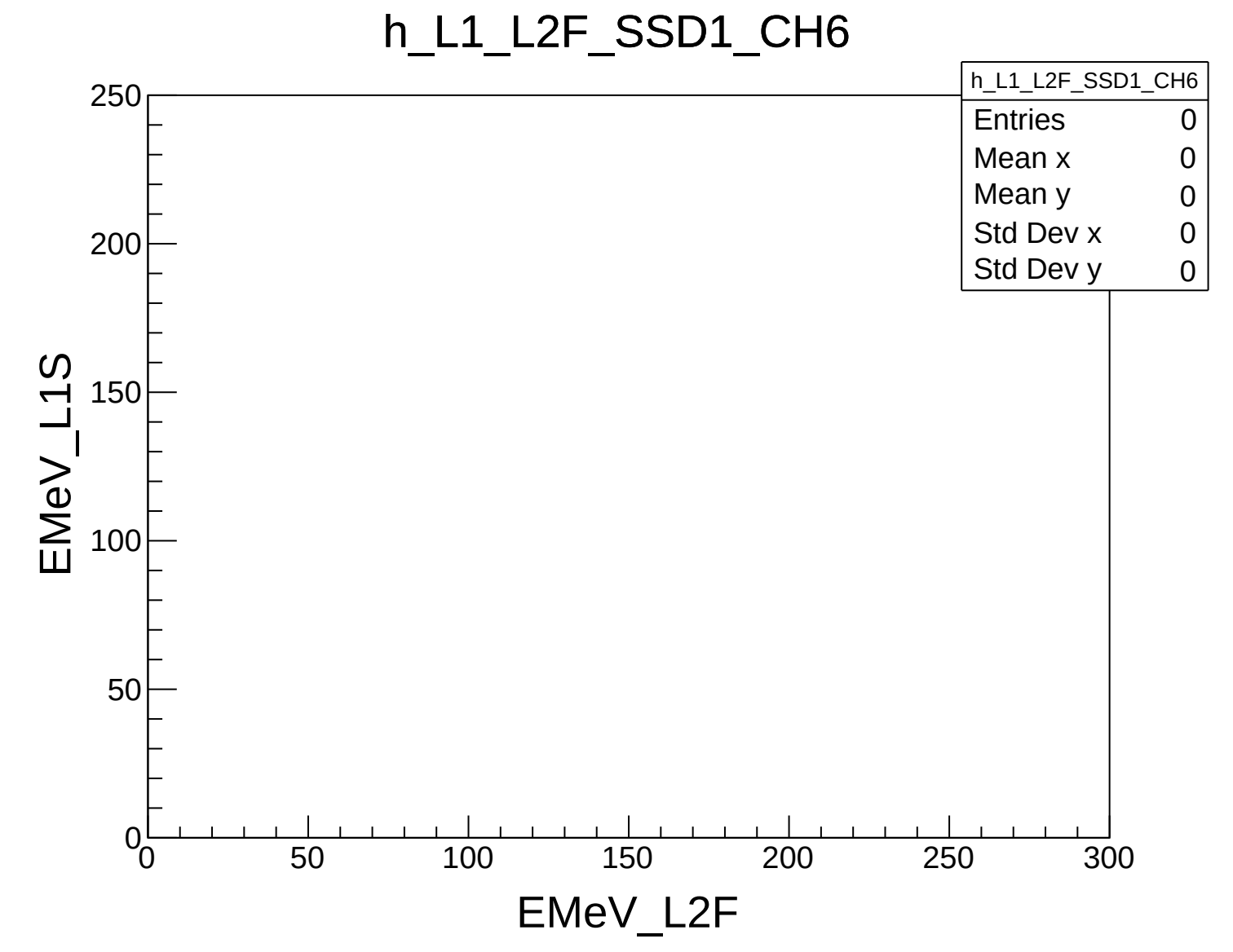

h_L1_L2F_SSD1_CH1
h_L1_L2F_SSD1_CH1
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

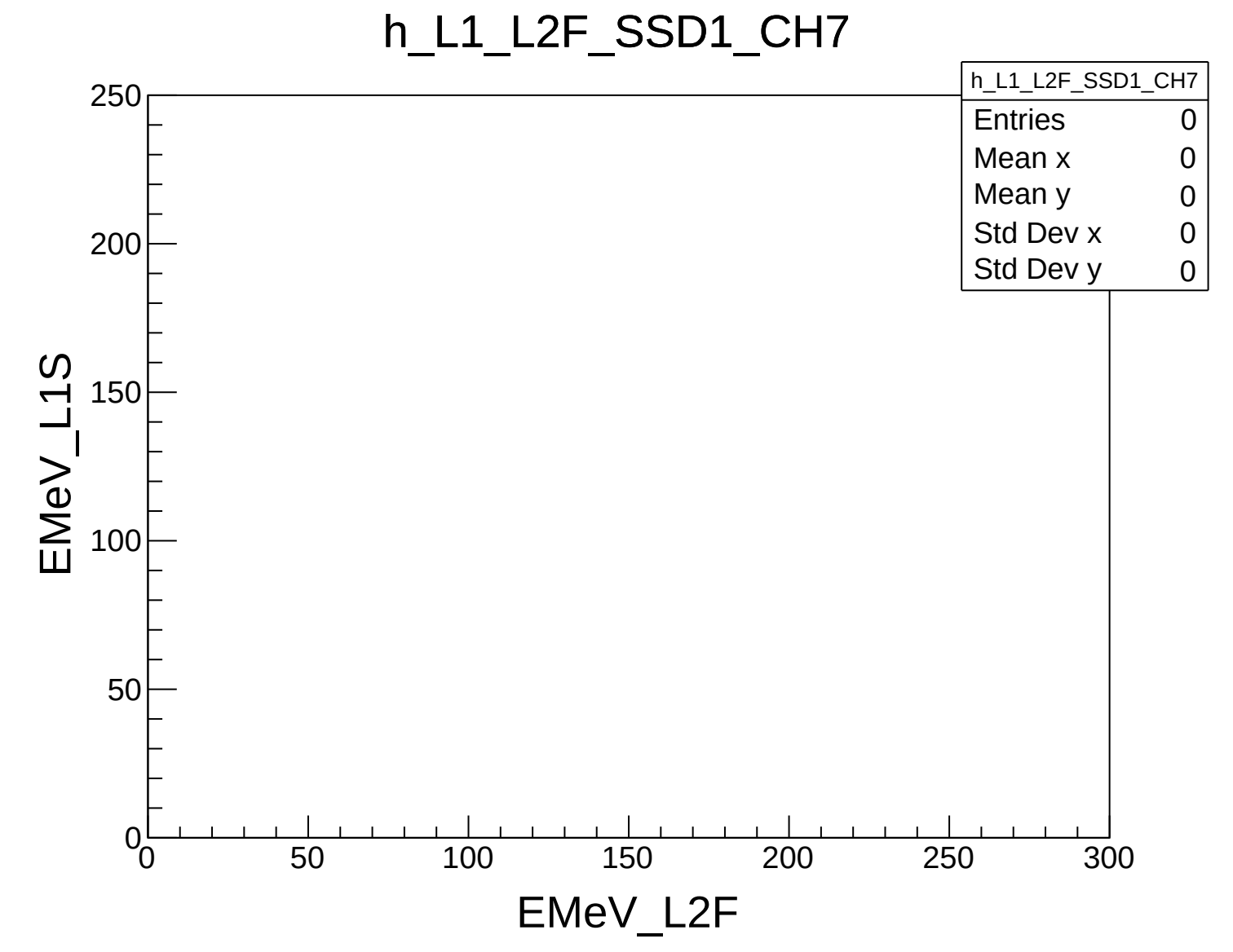

h_L1_L2F_SSD1_CH2
h_L1_L2F_SSD1_CH2
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

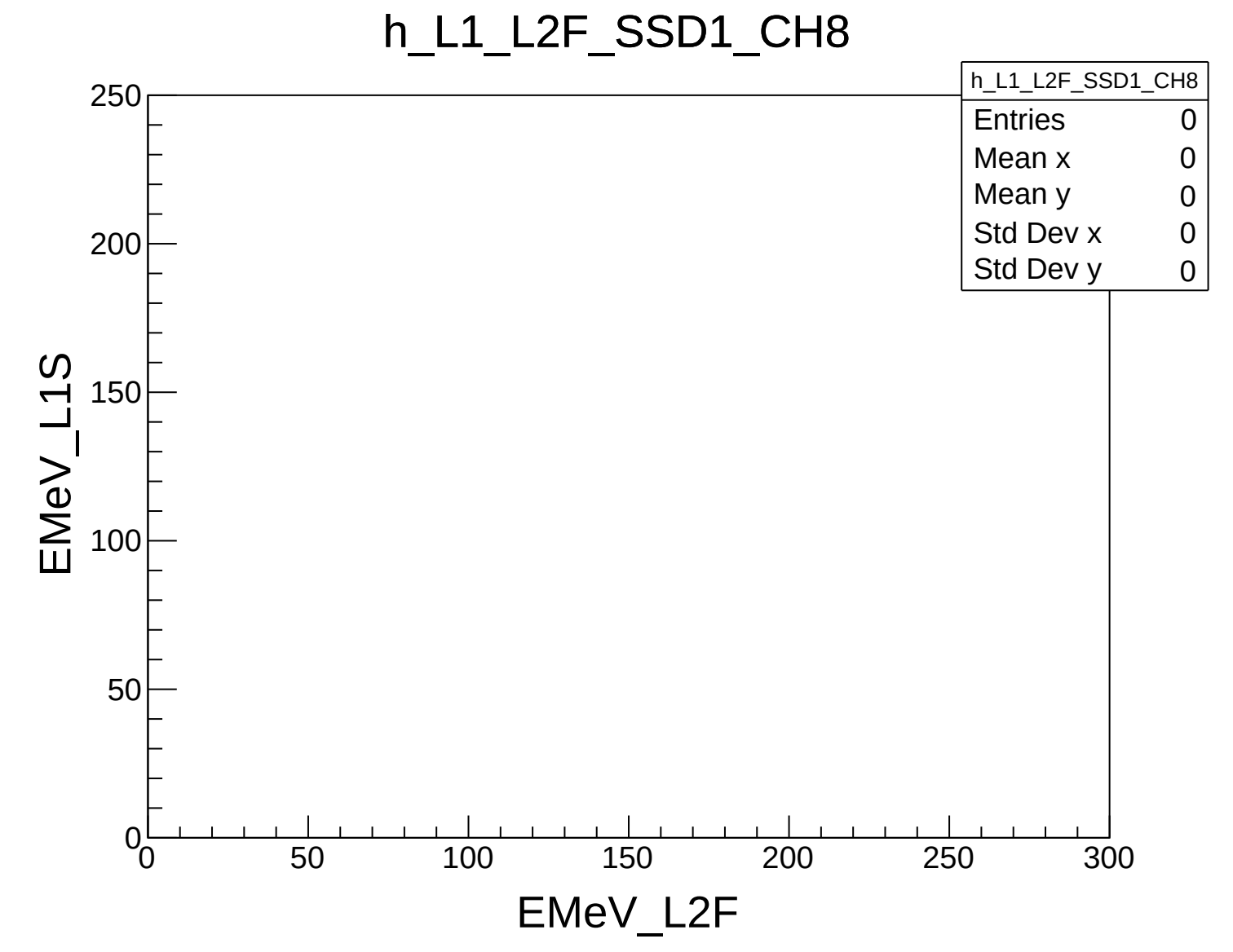

h_L1_L2F_SSD1_CH3
h_L1_L2F_SSD1_CH3
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

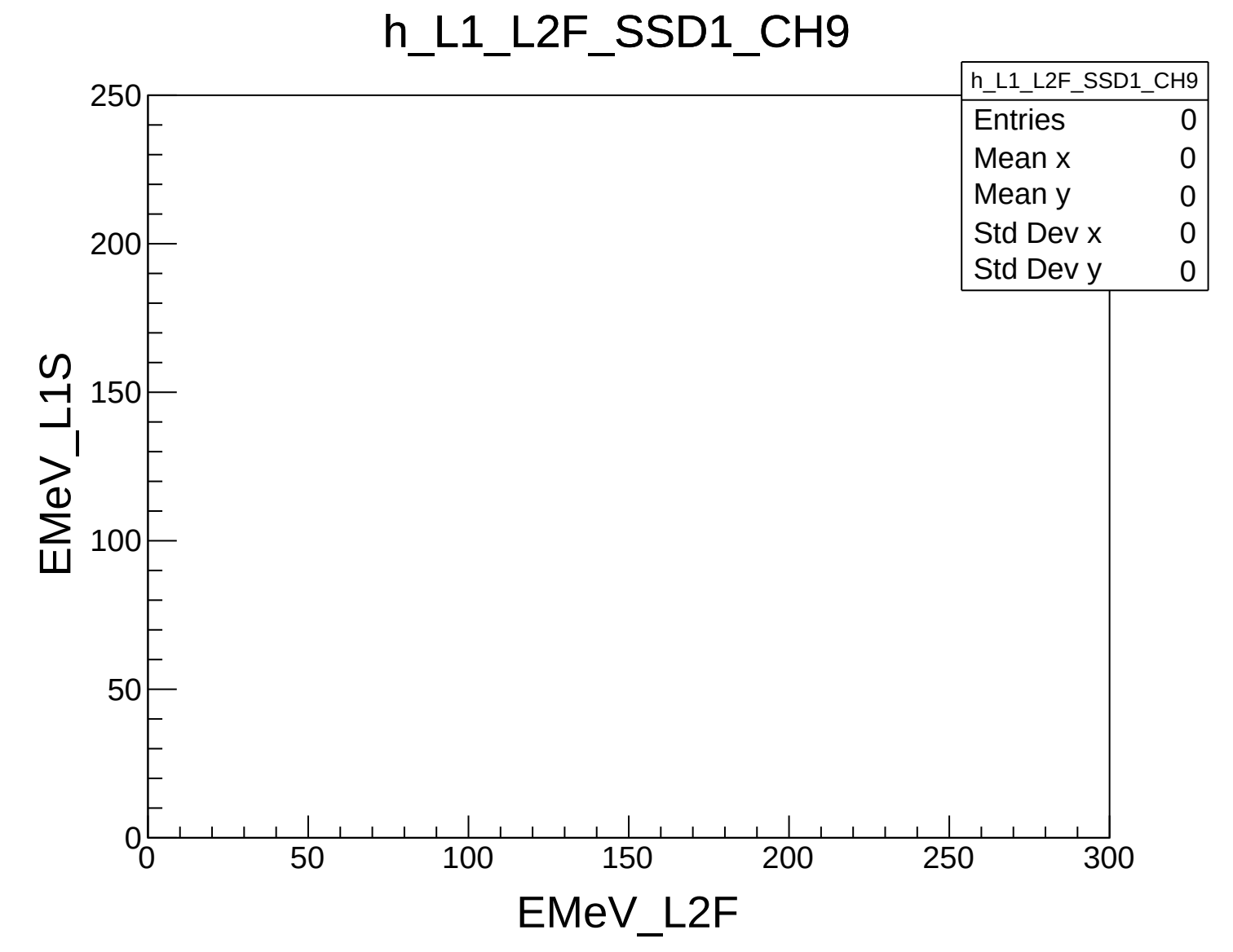

h_L1_L2F_SSD1_CH4
h_L1_L2F_SSD1_CH4
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

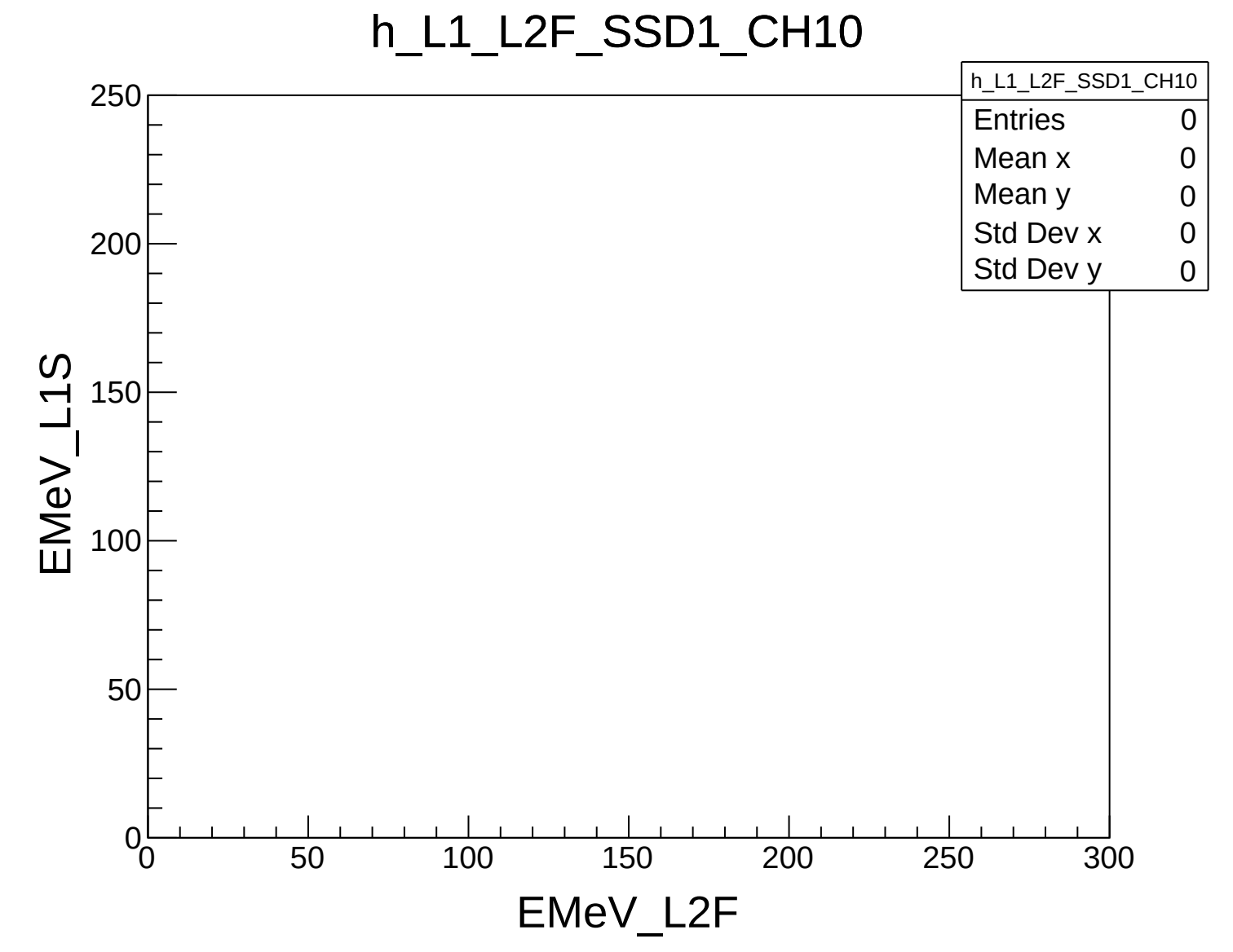

h_L1_L2F_SSD1_CH5
h_L1_L2F_SSD1_CH5
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

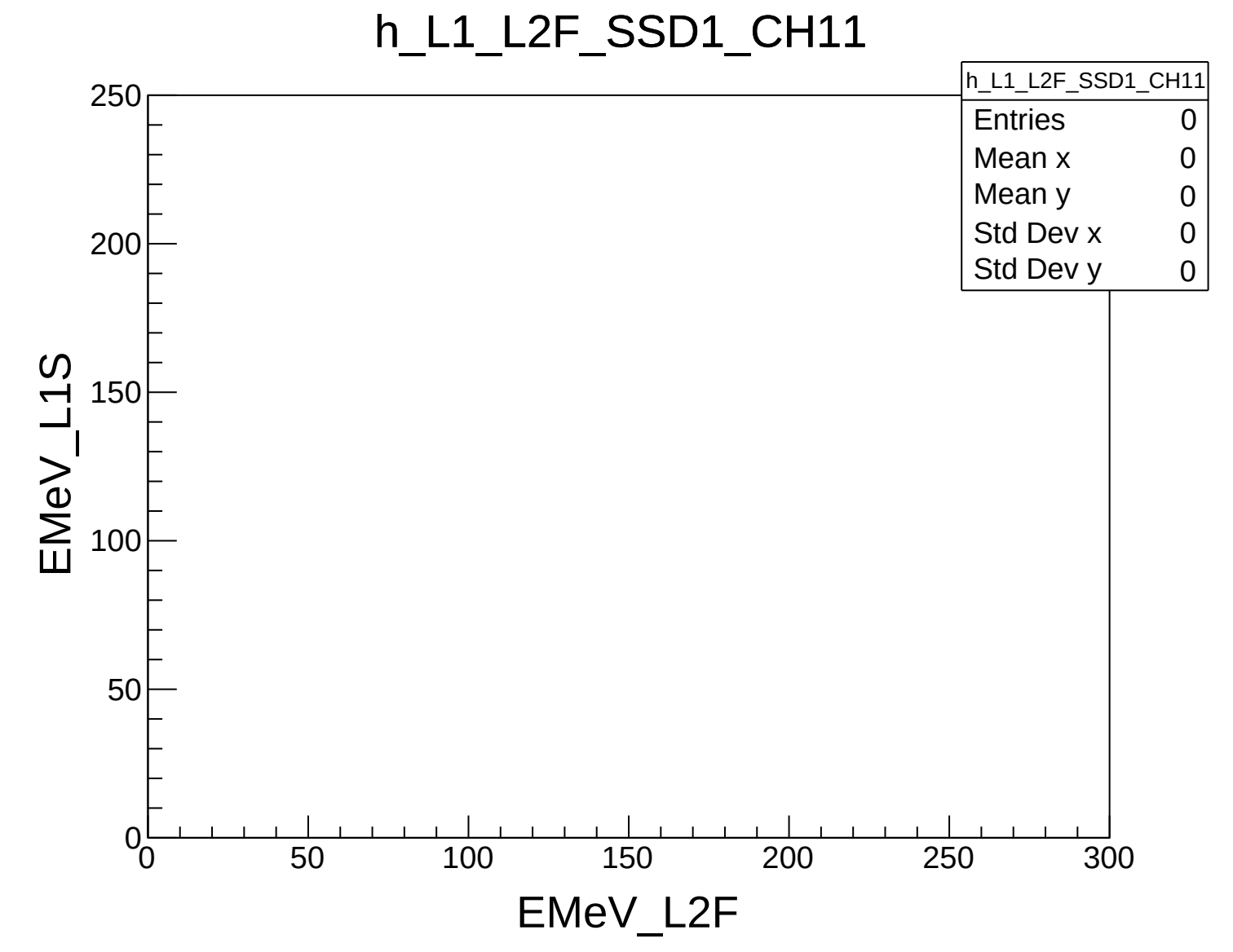

h_L1_L2F_SSD1_CH6
h_L1_L2F_SSD1_CH6
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

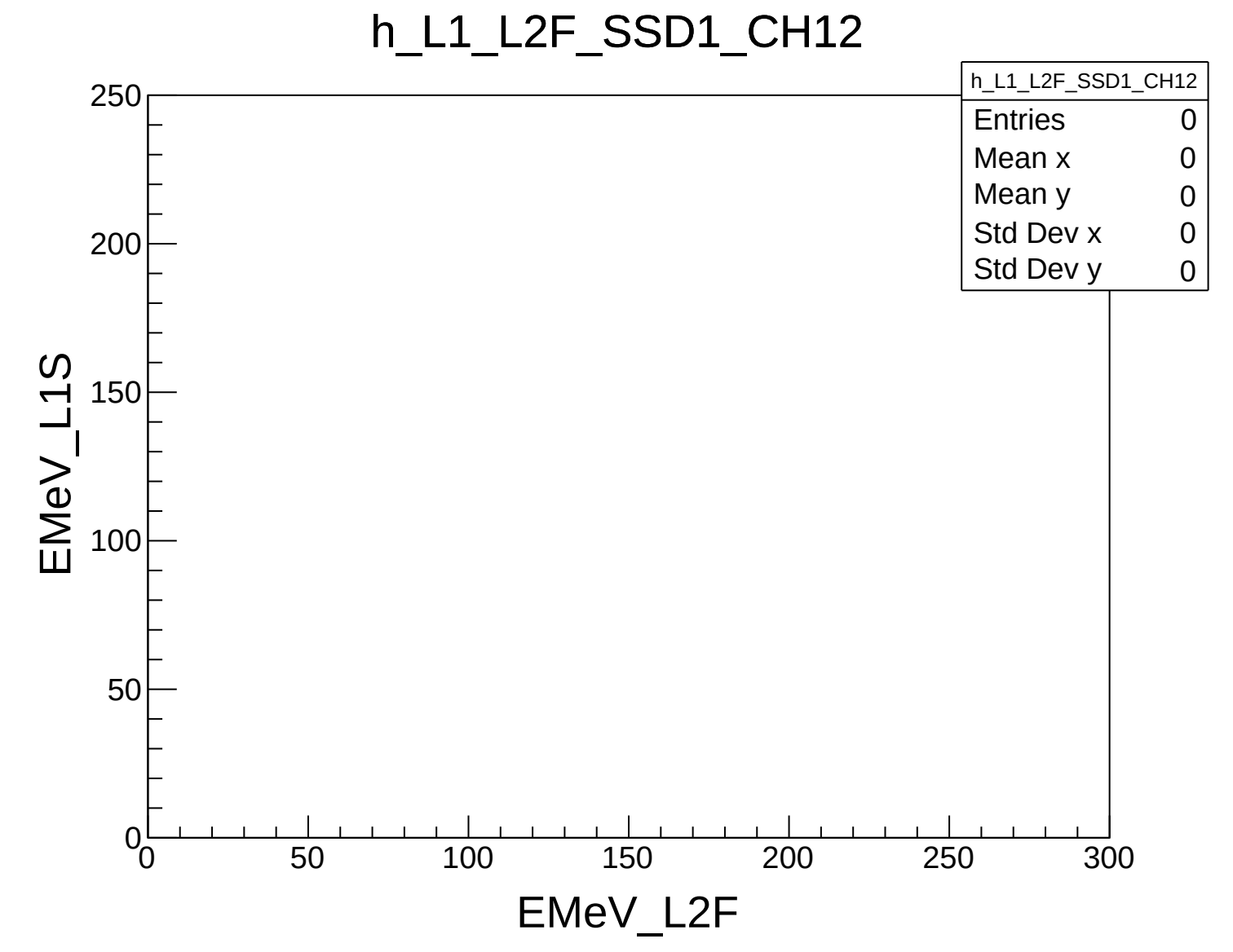

h_L1_L2F_SSD1_CH7
h_L1_L2F_SSD1_CH7
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

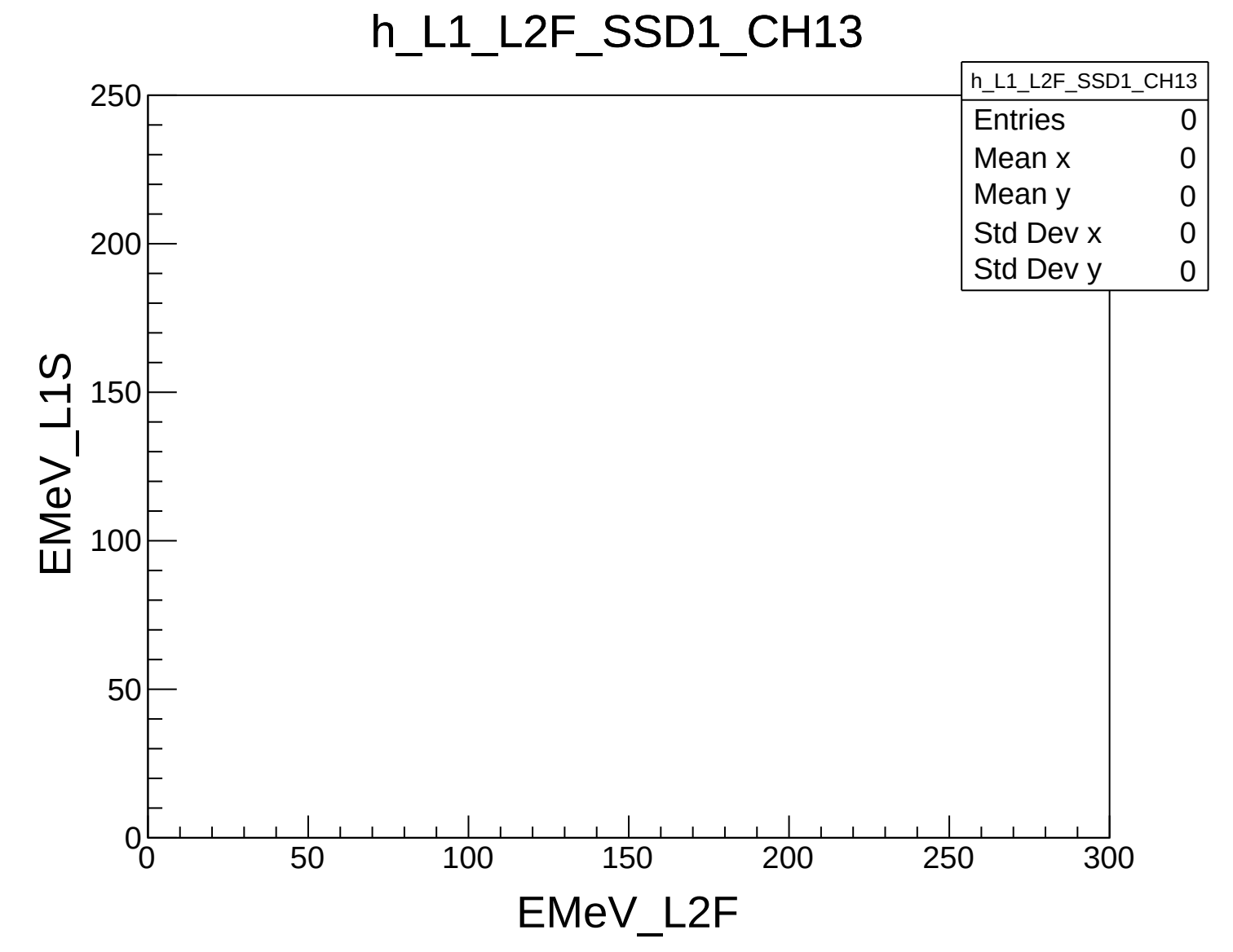

h_L1_L2F_SSD1_CH8
h_L1_L2F_SSD1_CH8
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

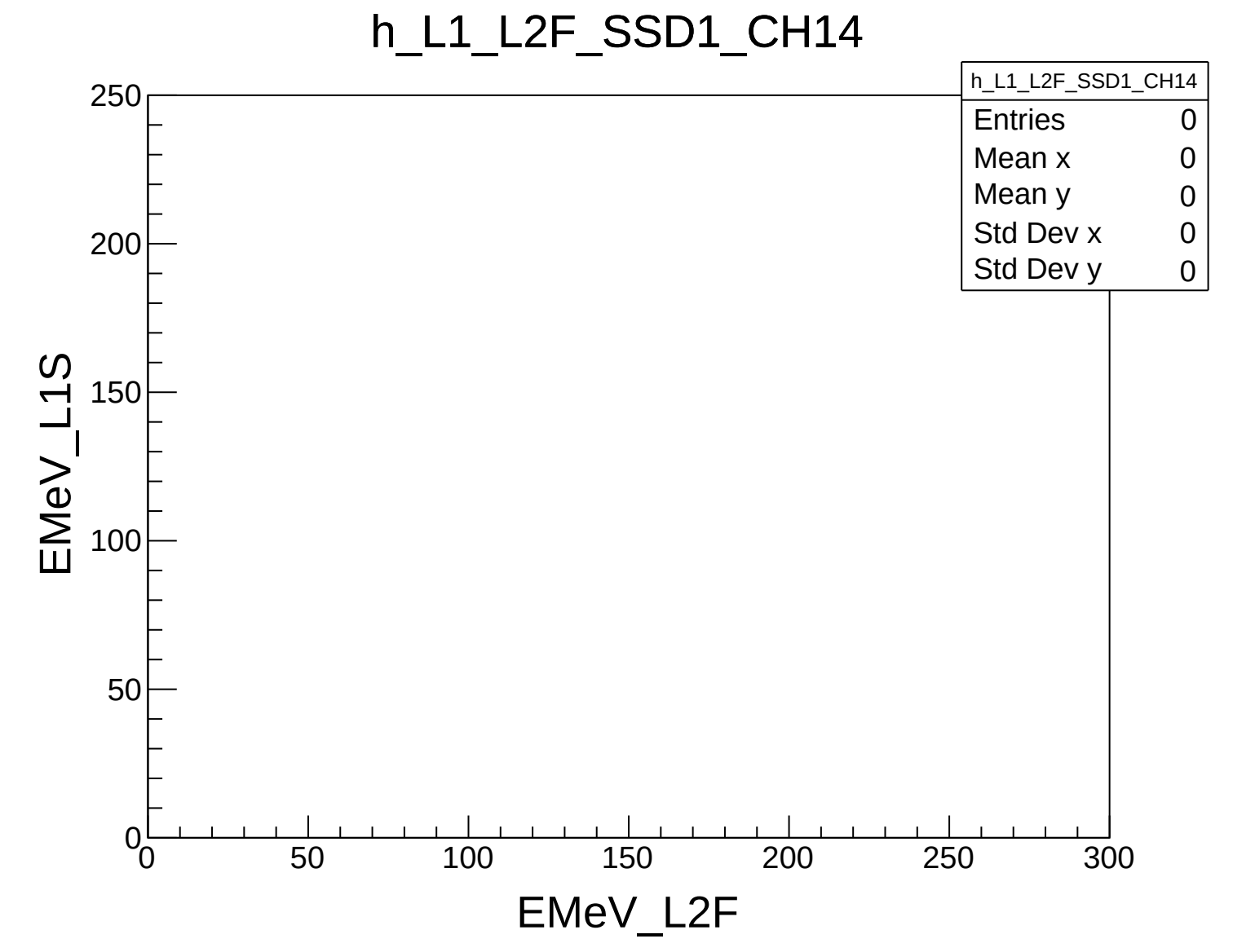

h_L1_L2F_SSD1_CH9
h_L1_L2F_SSD1_CH9
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

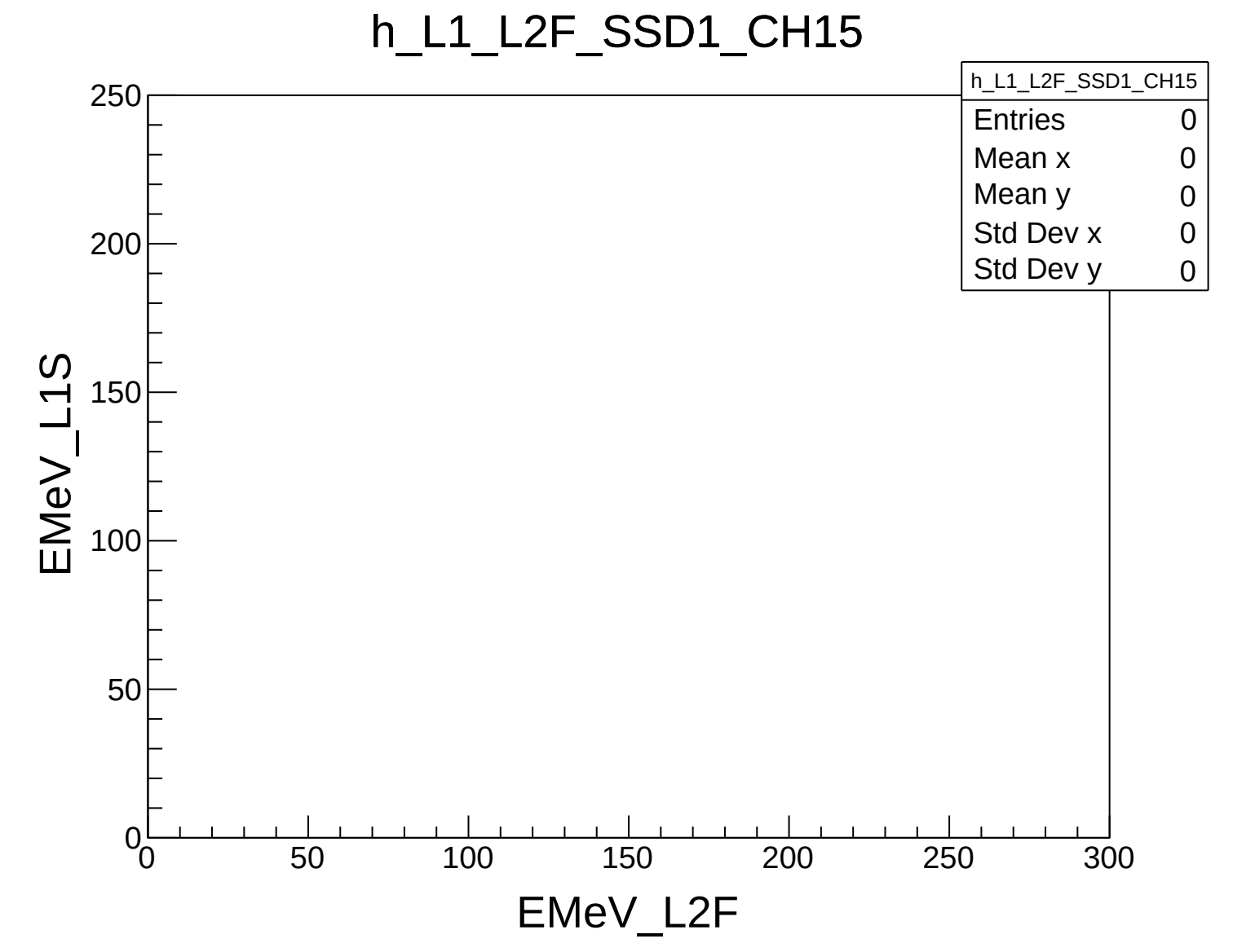

h_L1_L2F_SSD1_CH10
h_L1_L2F_SSD1_CH10
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

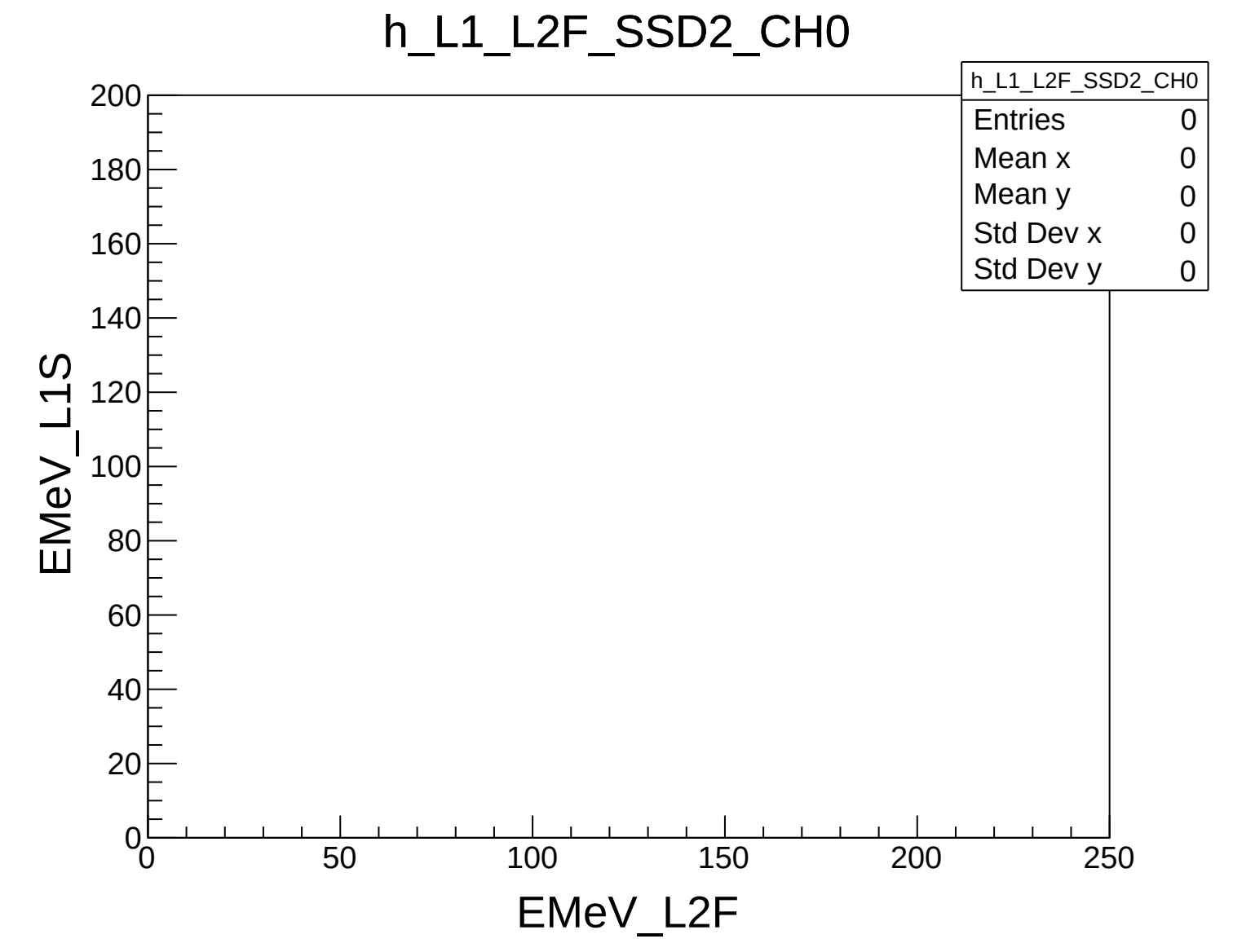

h_L1_L2F_SSD1_CH11
h_L1_L2F_SSD1_CH11
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

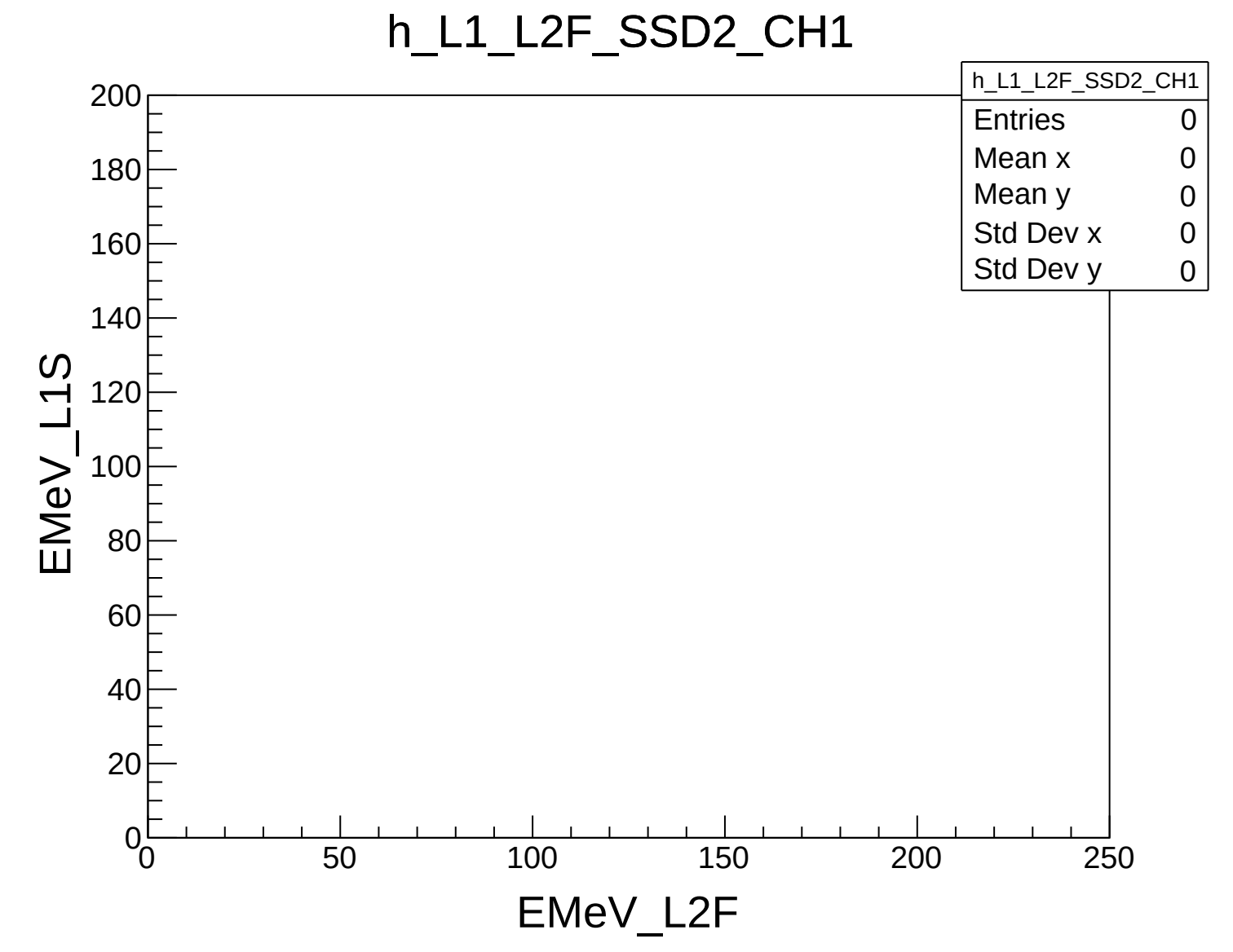

h_L1_L2F_SSD1_CH12
h_L1_L2F_SSD1_CH12
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

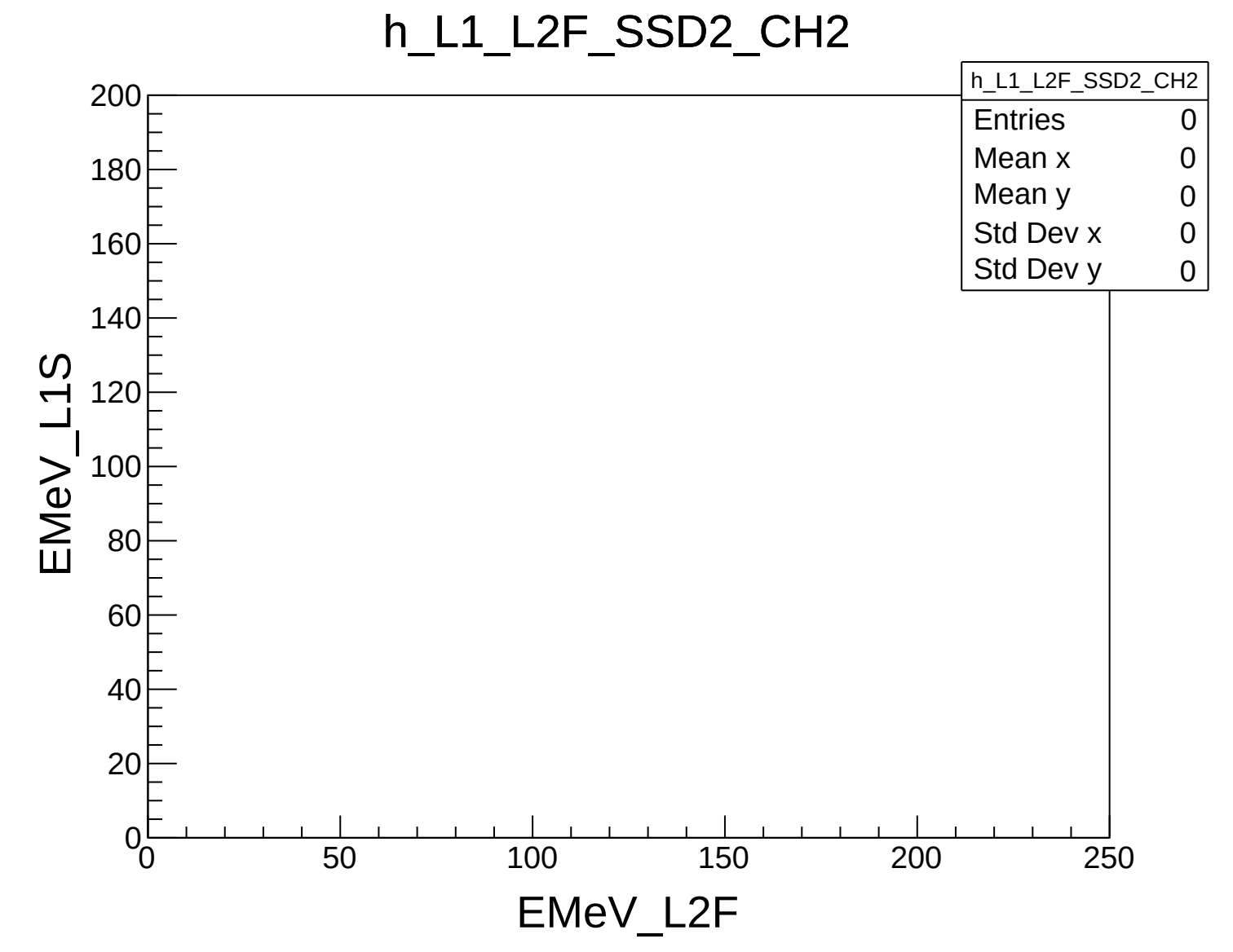

h_L1_L2F_SSD1_CH13
h_L1_L2F_SSD1_CH13
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

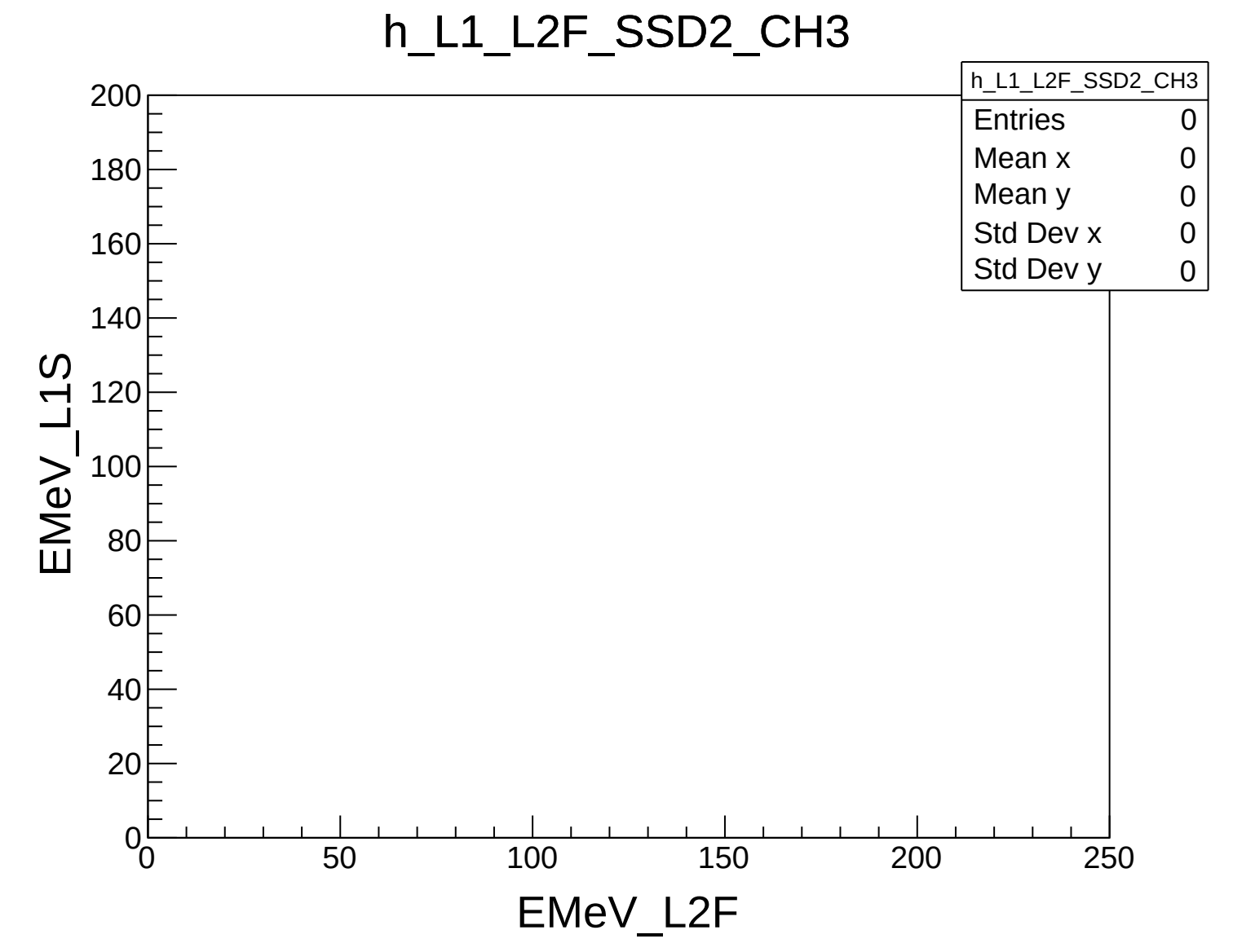

h_L1_L2F_SSD1_CH14
h_L1_L2F_SSD1_CH14
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

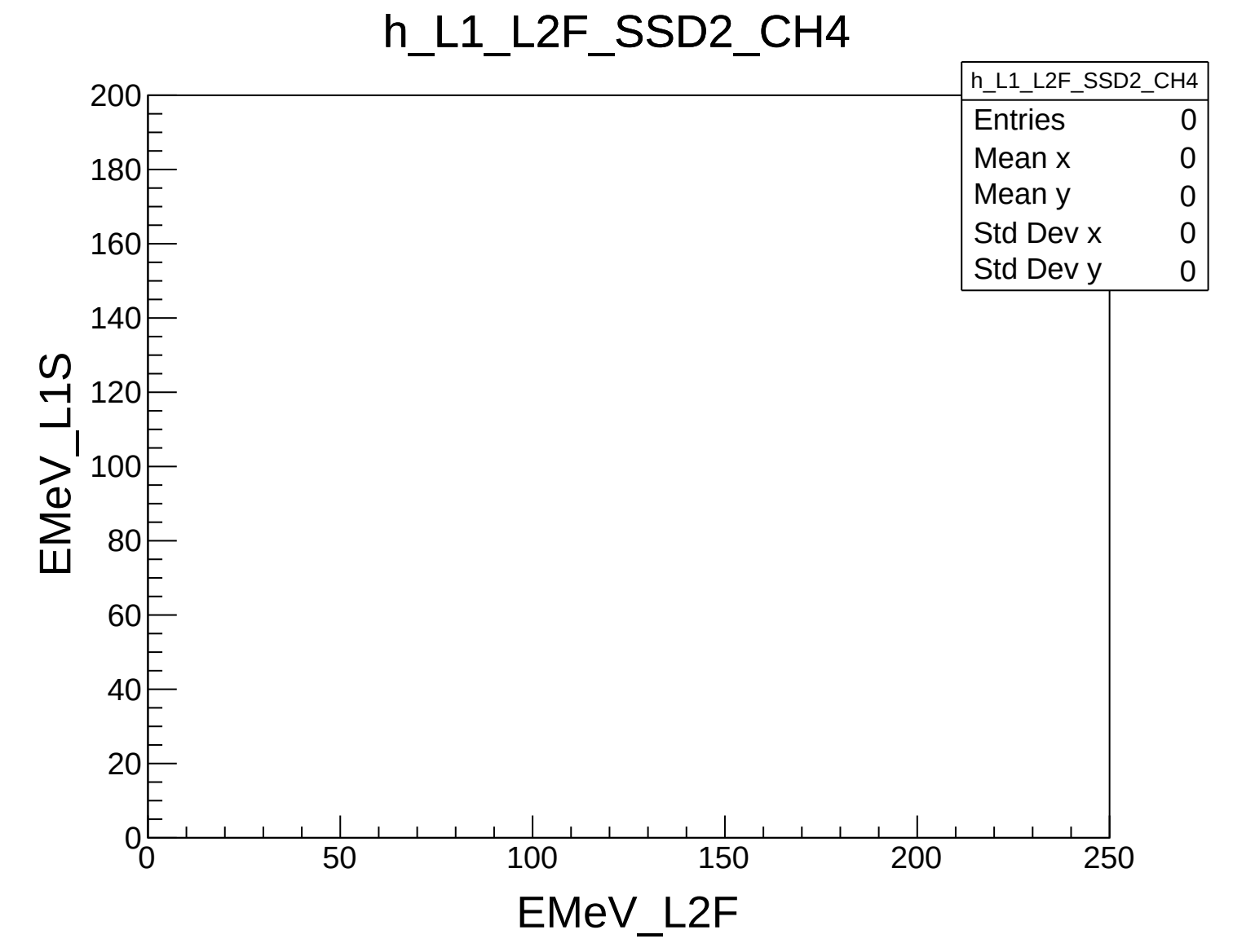

h_L1_L2F_SSD1_CH15
h_L1_L2F_SSD1_CH15
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300

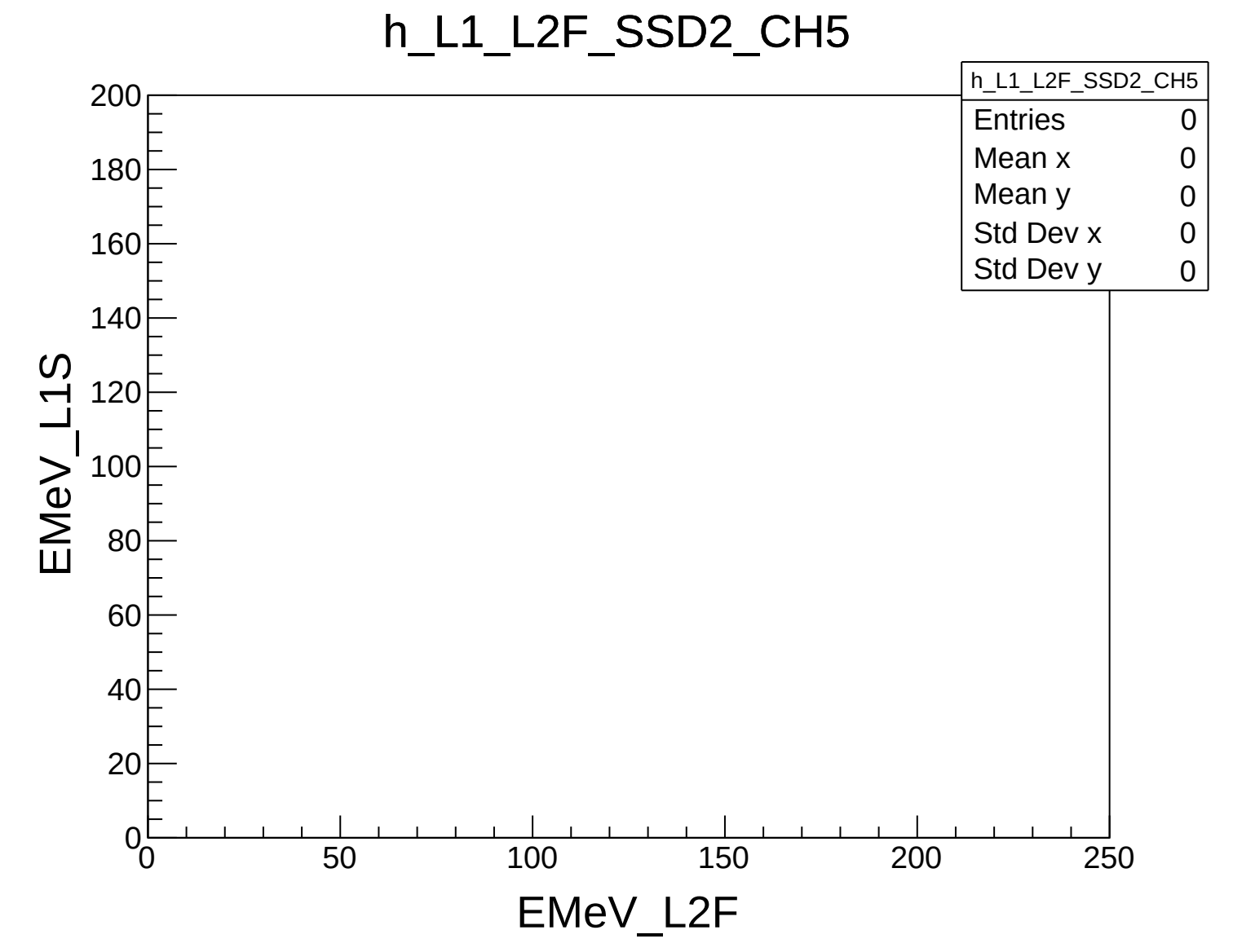

h_L1_L2F_SSD2_CH0
h_L1_L2F_SSD2_CH0
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

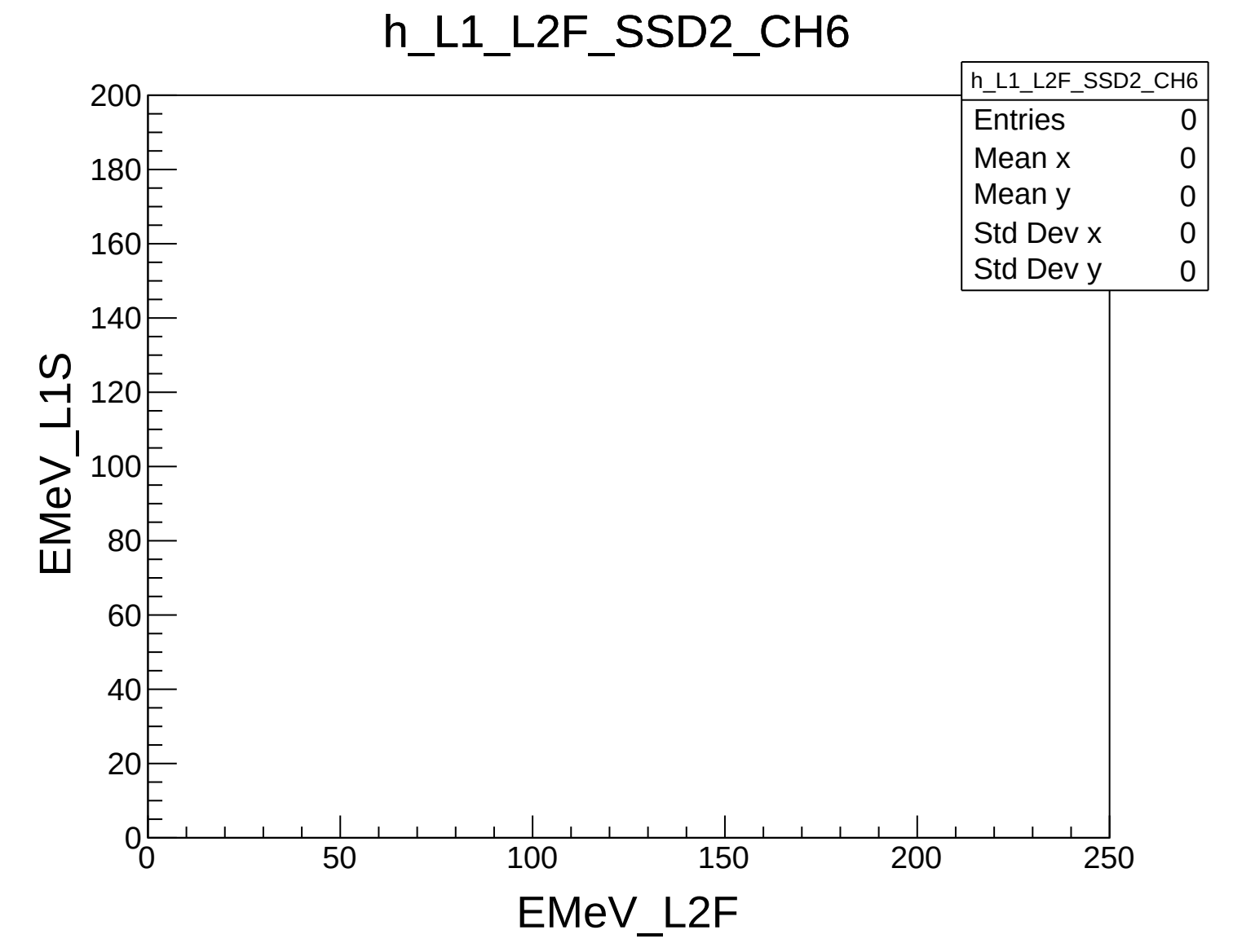

h_L1_L2F_SSD2_CH1
h_L1_L2F_SSD2_CH1
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

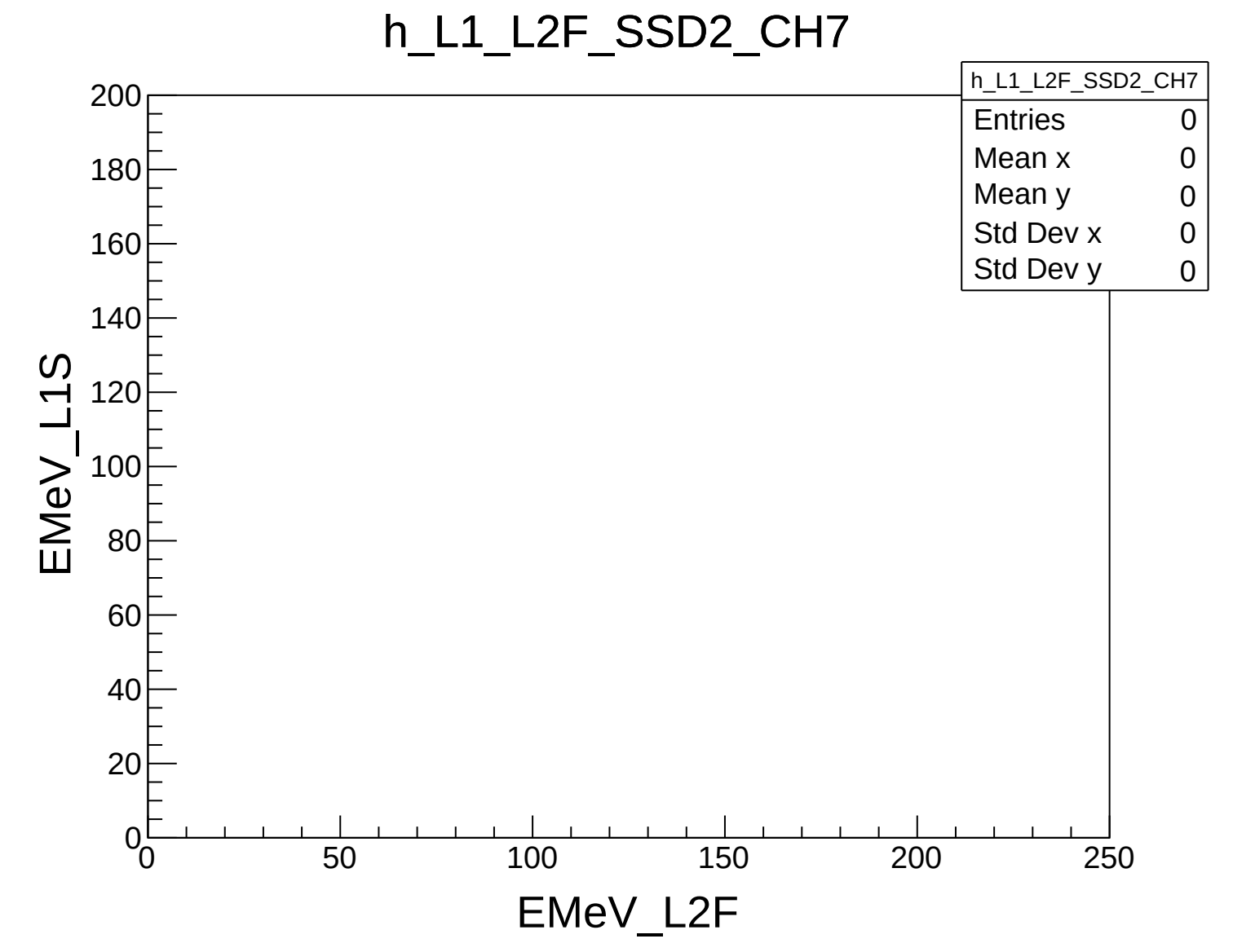

h_L1_L2F_SSD2_CH2
h_L1_L2F_SSD2_CH2
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

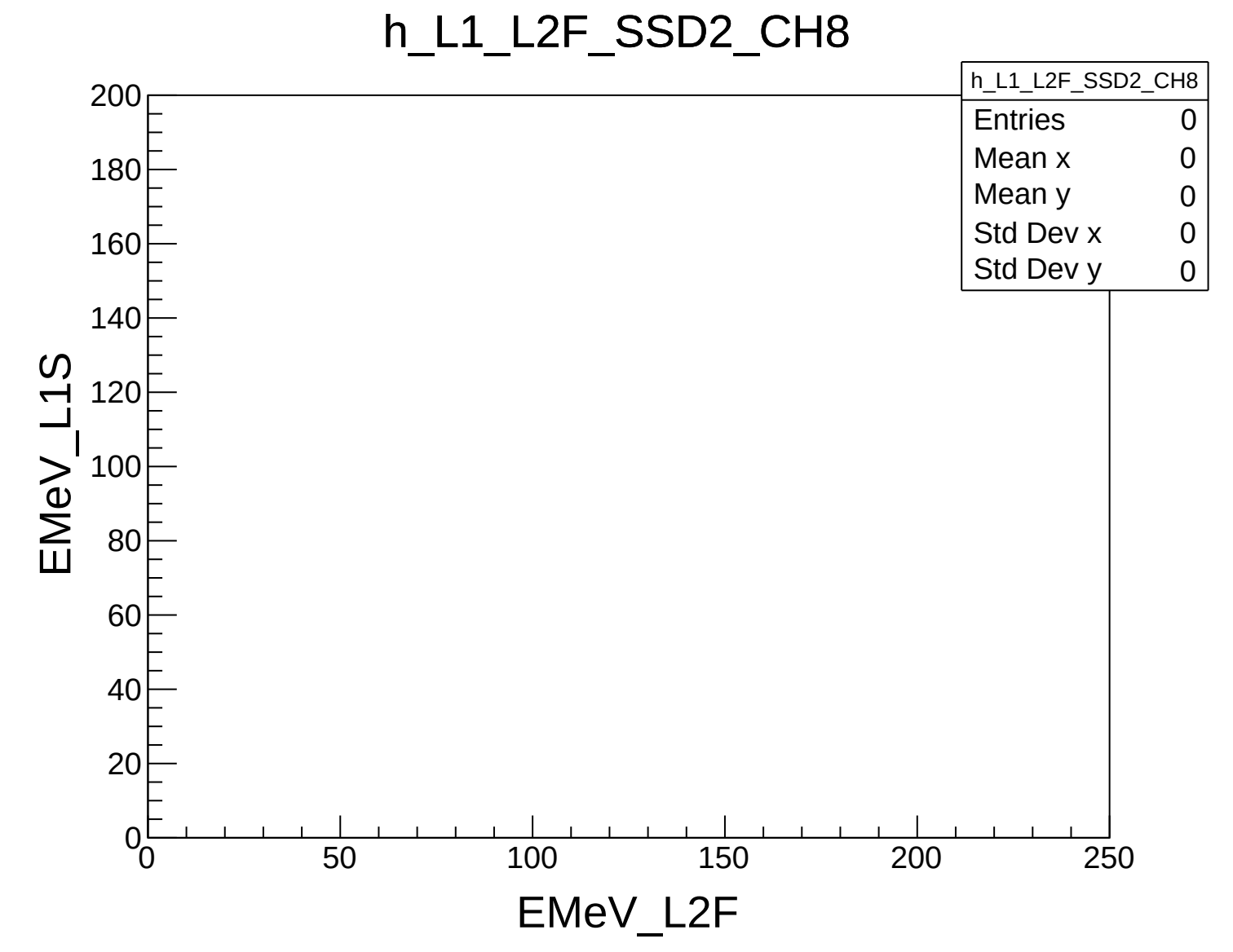

h_L1_L2F_SSD2_CH3
h_L1_L2F_SSD2_CH3
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

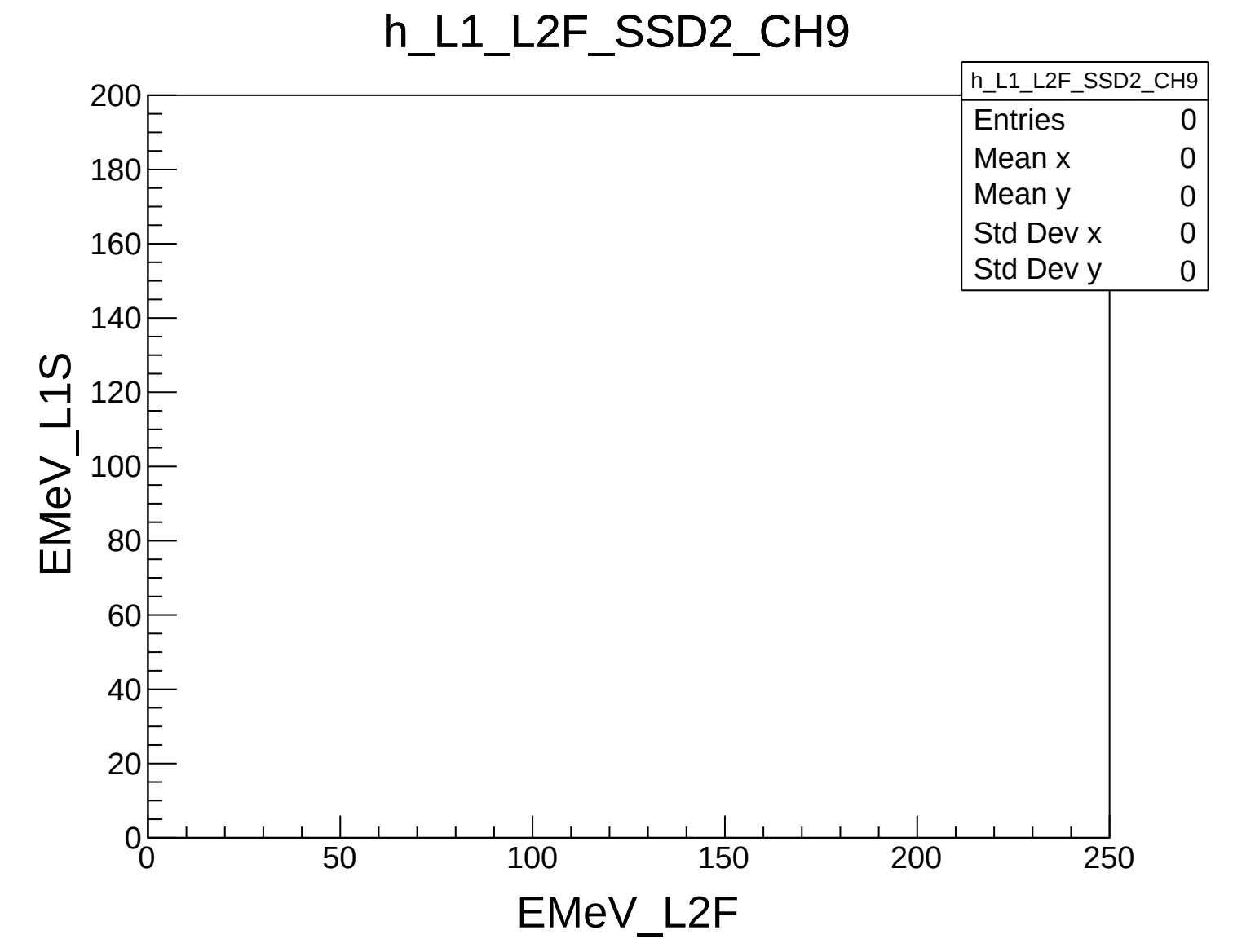

h_L1_L2F_SSD2_CH4
h_L1_L2F_SSD2_CH4
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

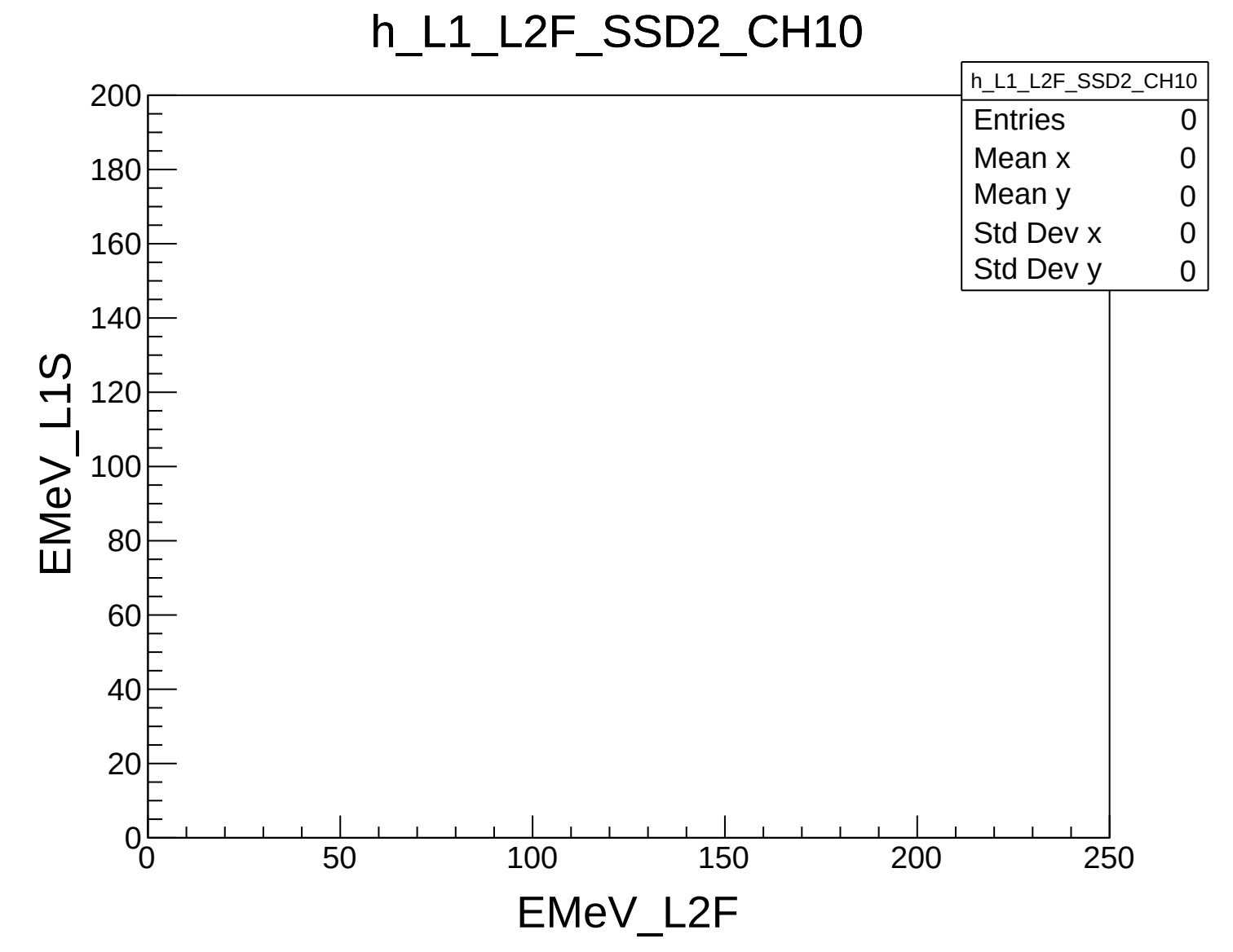

h_L1_L2F_SSD2_CH5
h_L1_L2F_SSD2_CH5
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

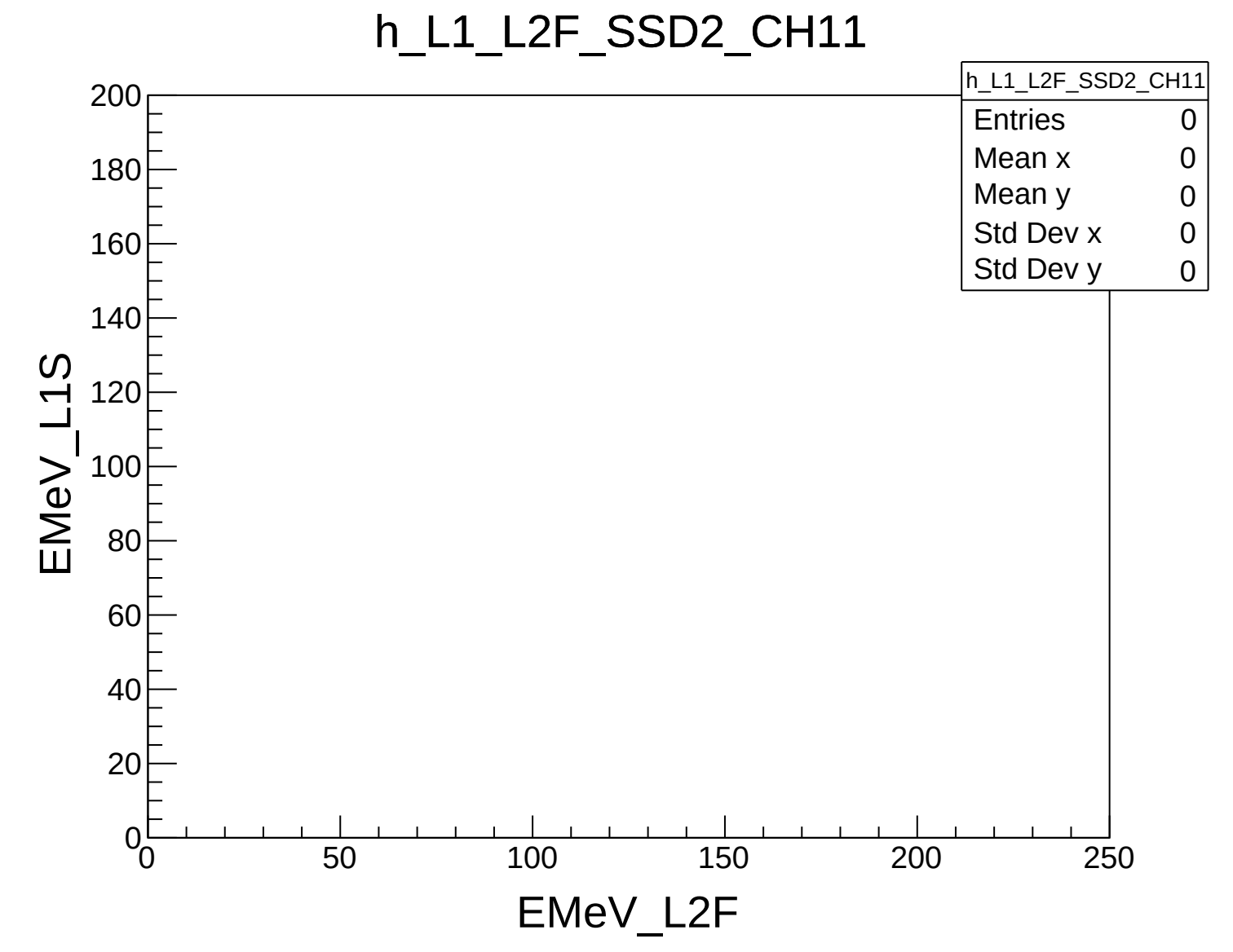

h_L1_L2F_SSD2_CH6
h_L1_L2F_SSD2_CH6
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

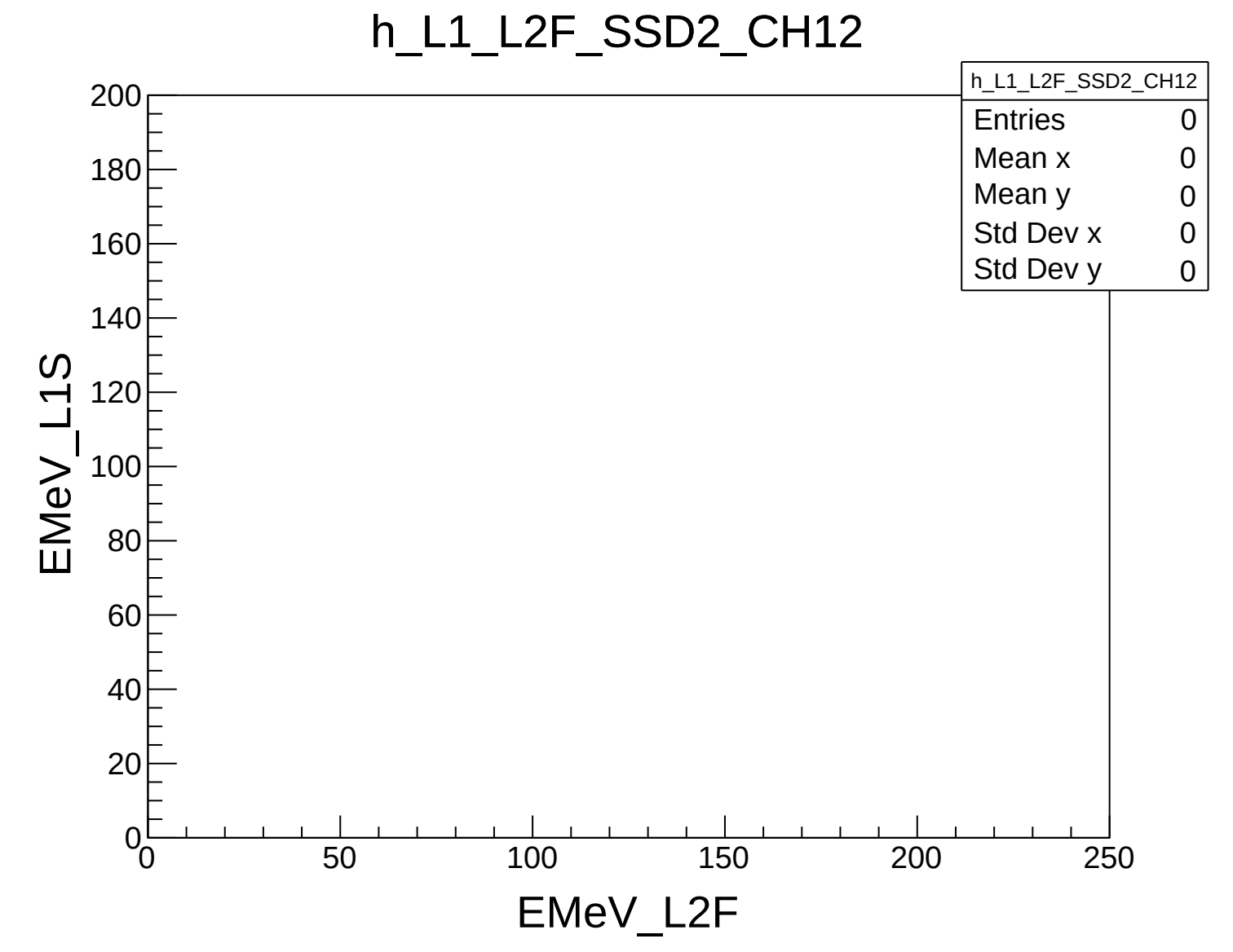

h_L1_L2F_SSD2_CH7
h_L1_L2F_SSD2_CH7
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

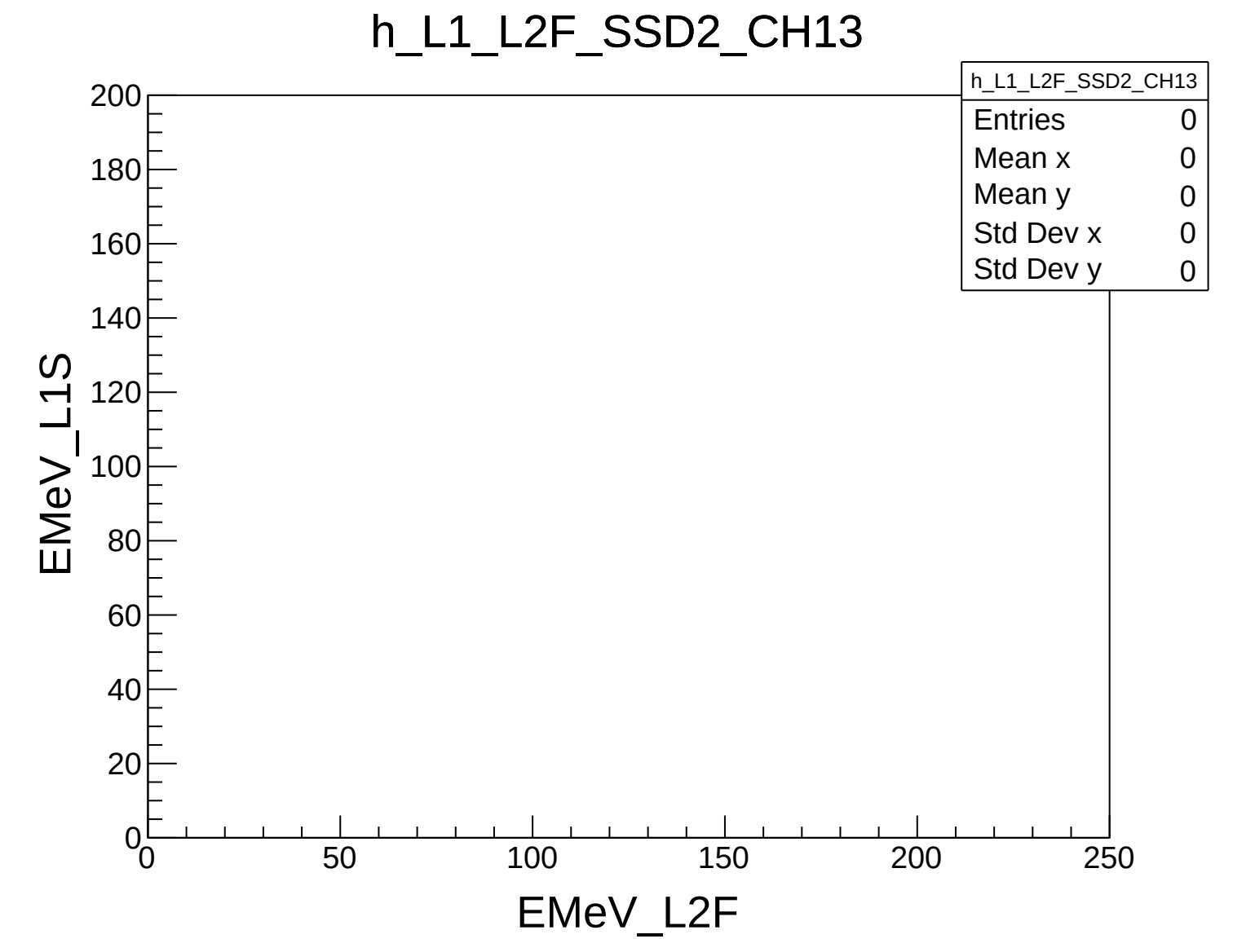

h_L1_L2F_SSD2_CH8
h_L1_L2F_SSD2_CH8
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

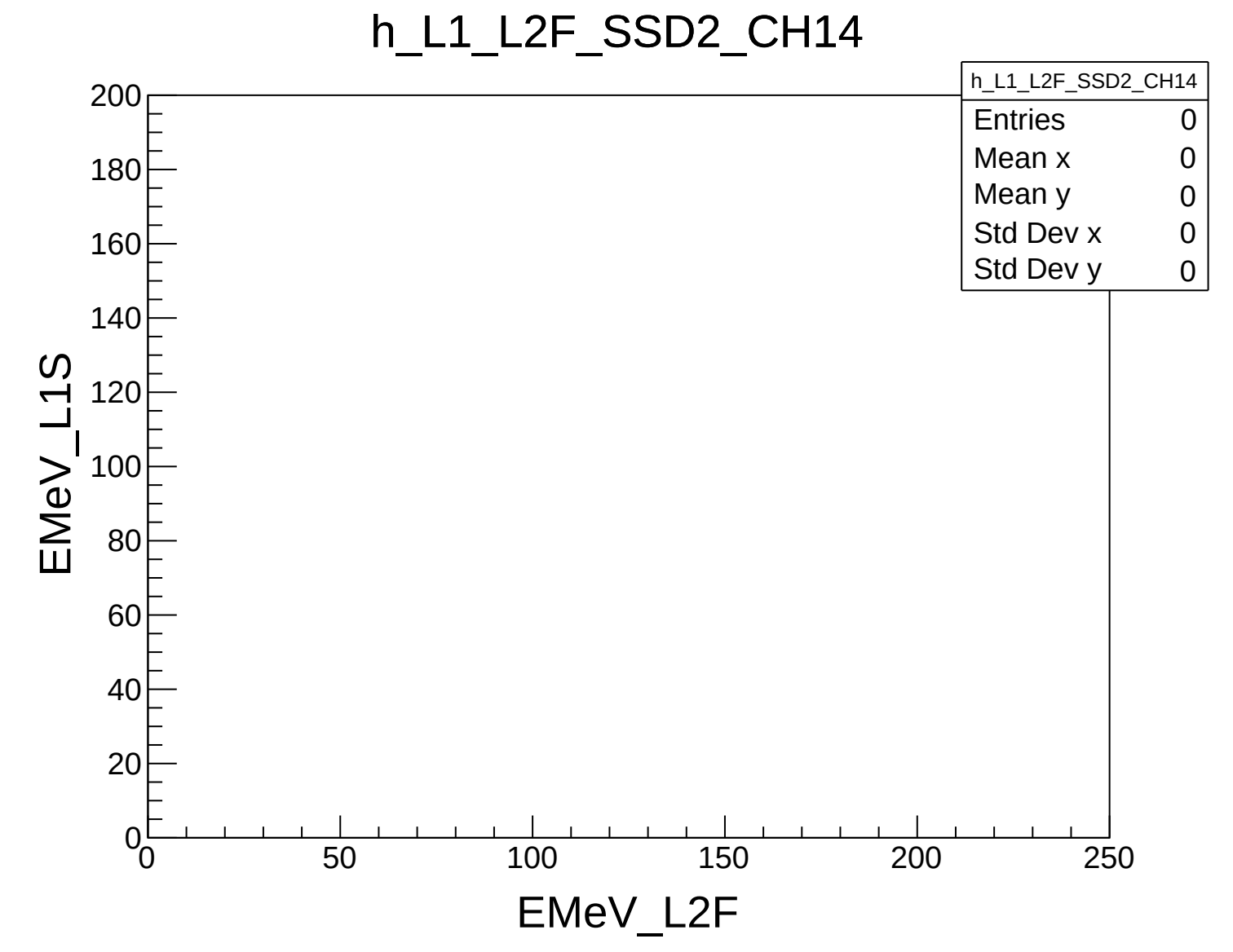

h_L1_L2F_SSD2_CH9
h_L1_L2F_SSD2_CH9
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

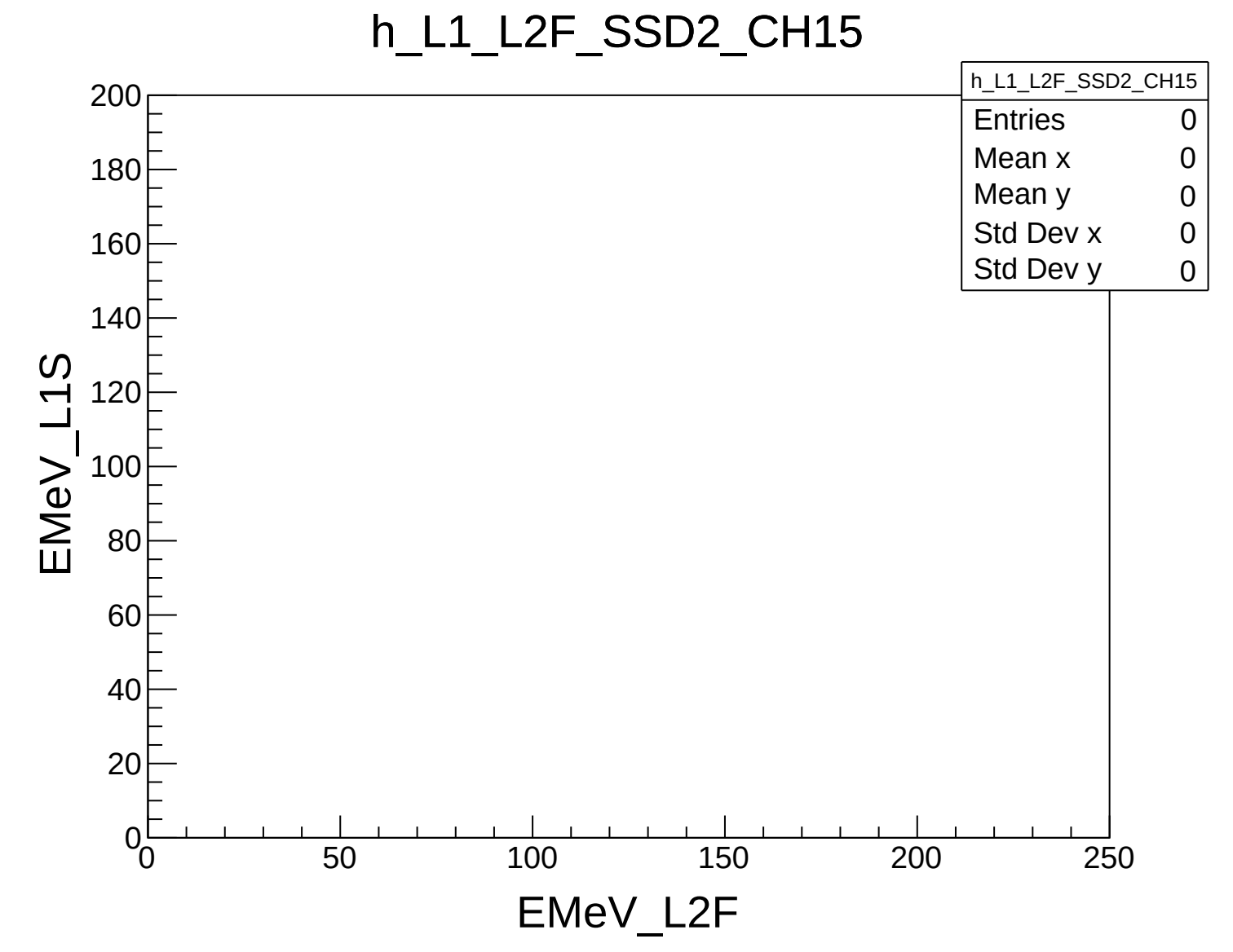

h_L1_L2F_SSD2_CH10
h_L1_L2F_SSD2_CH10
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

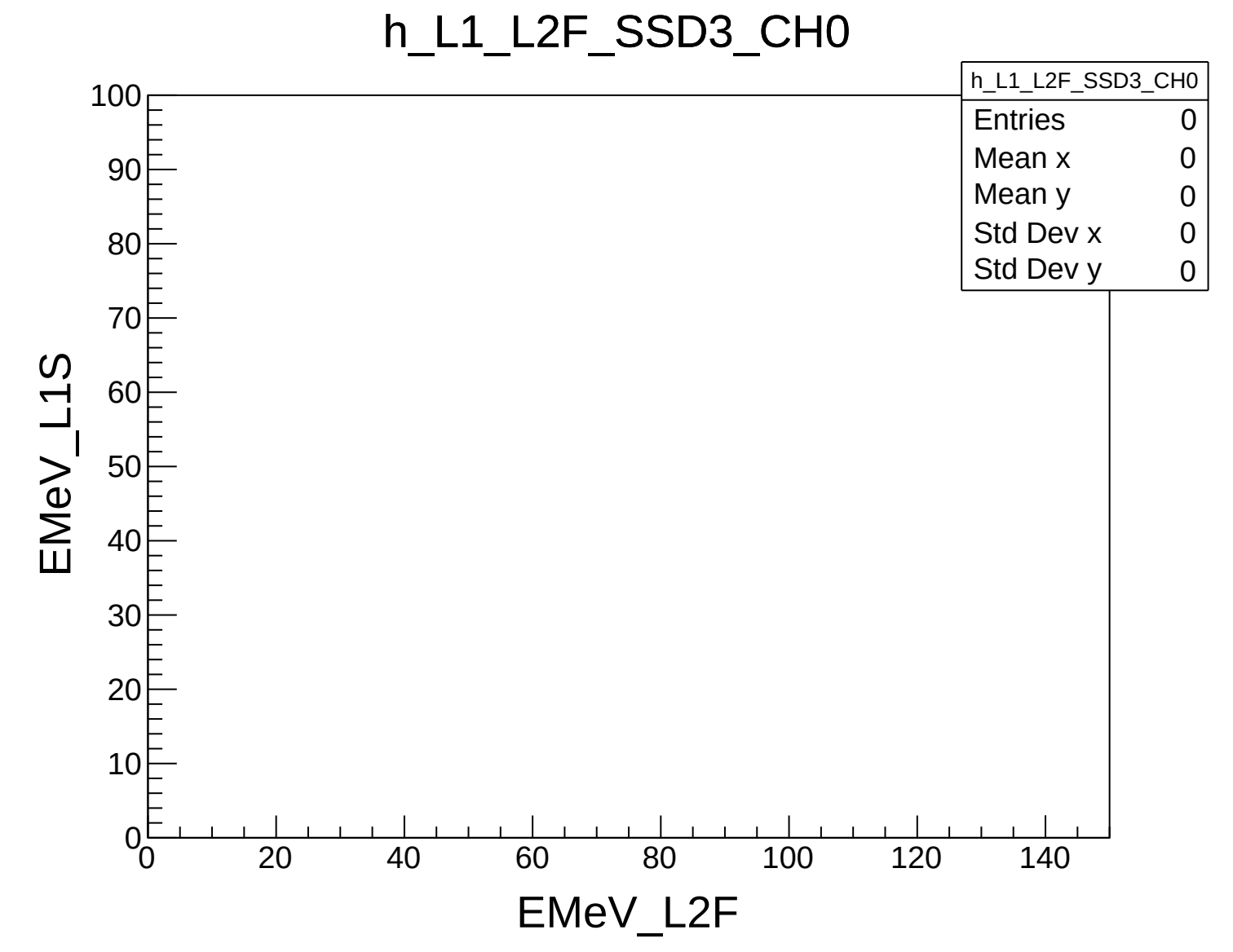

h_L1_L2F_SSD2_CH11
h_L1_L2F_SSD2_CH11
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

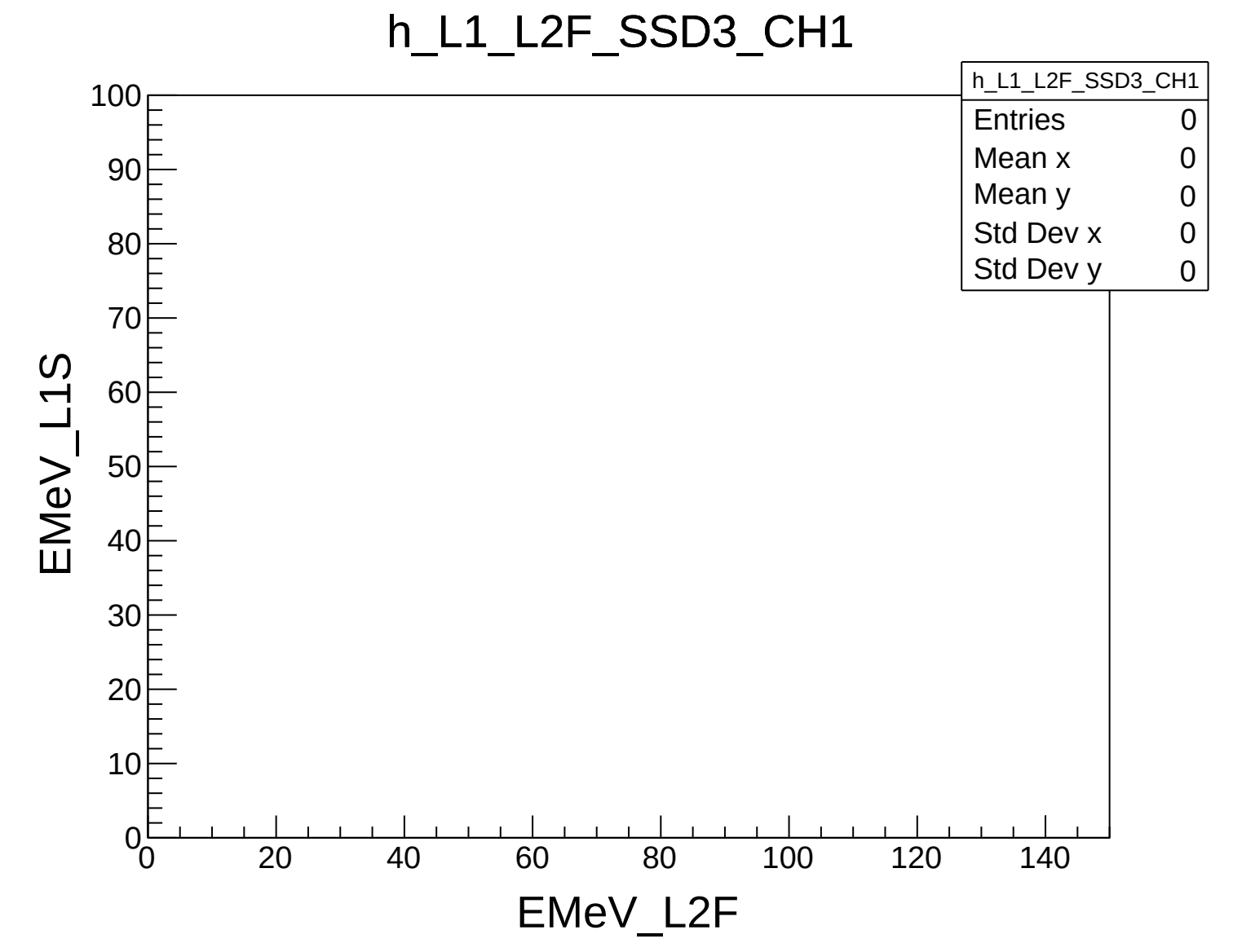

h_L1_L2F_SSD2_CH12
h_L1_L2F_SSD2_CH12
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

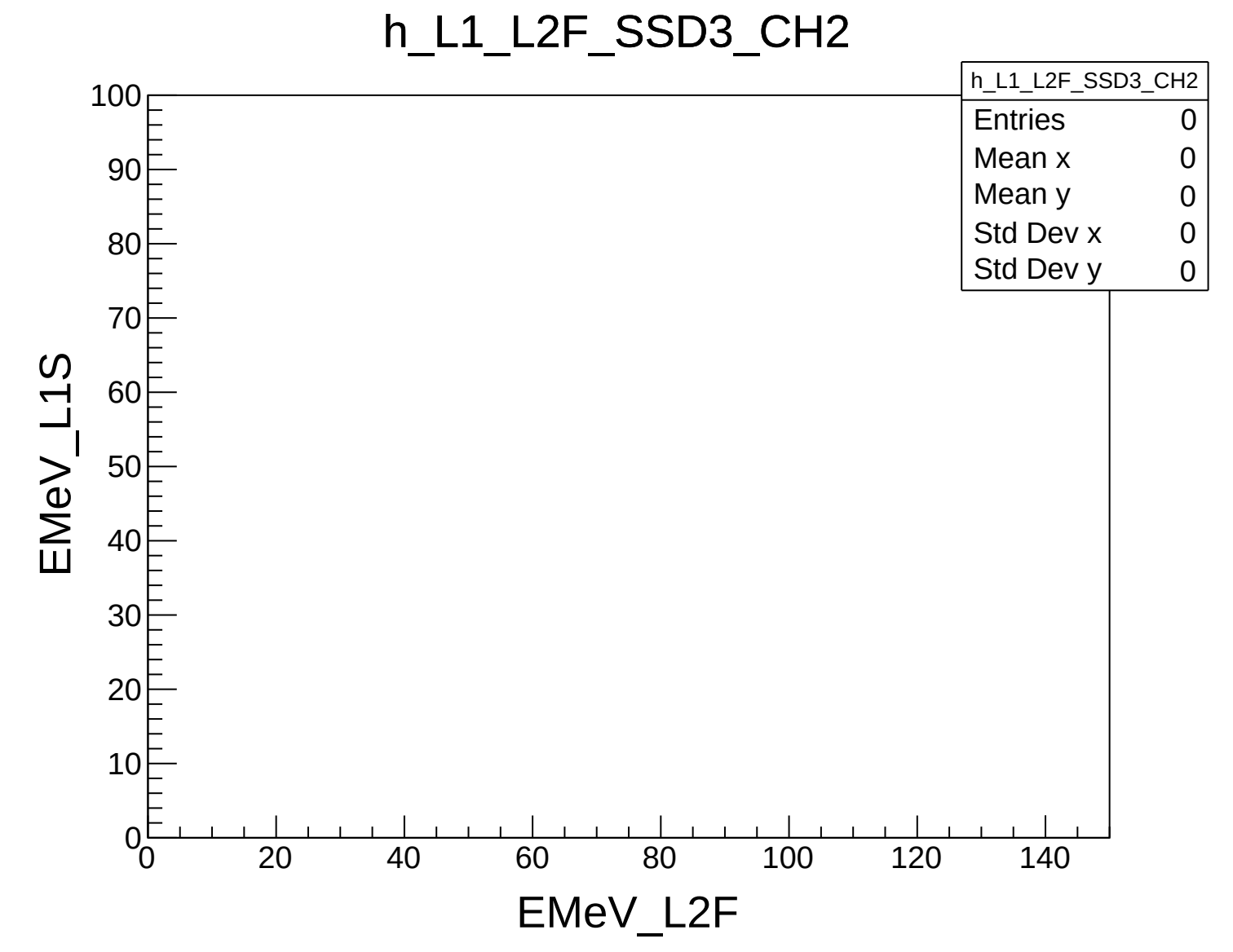

h_L1_L2F_SSD2_CH13
h_L1_L2F_SSD2_CH13
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

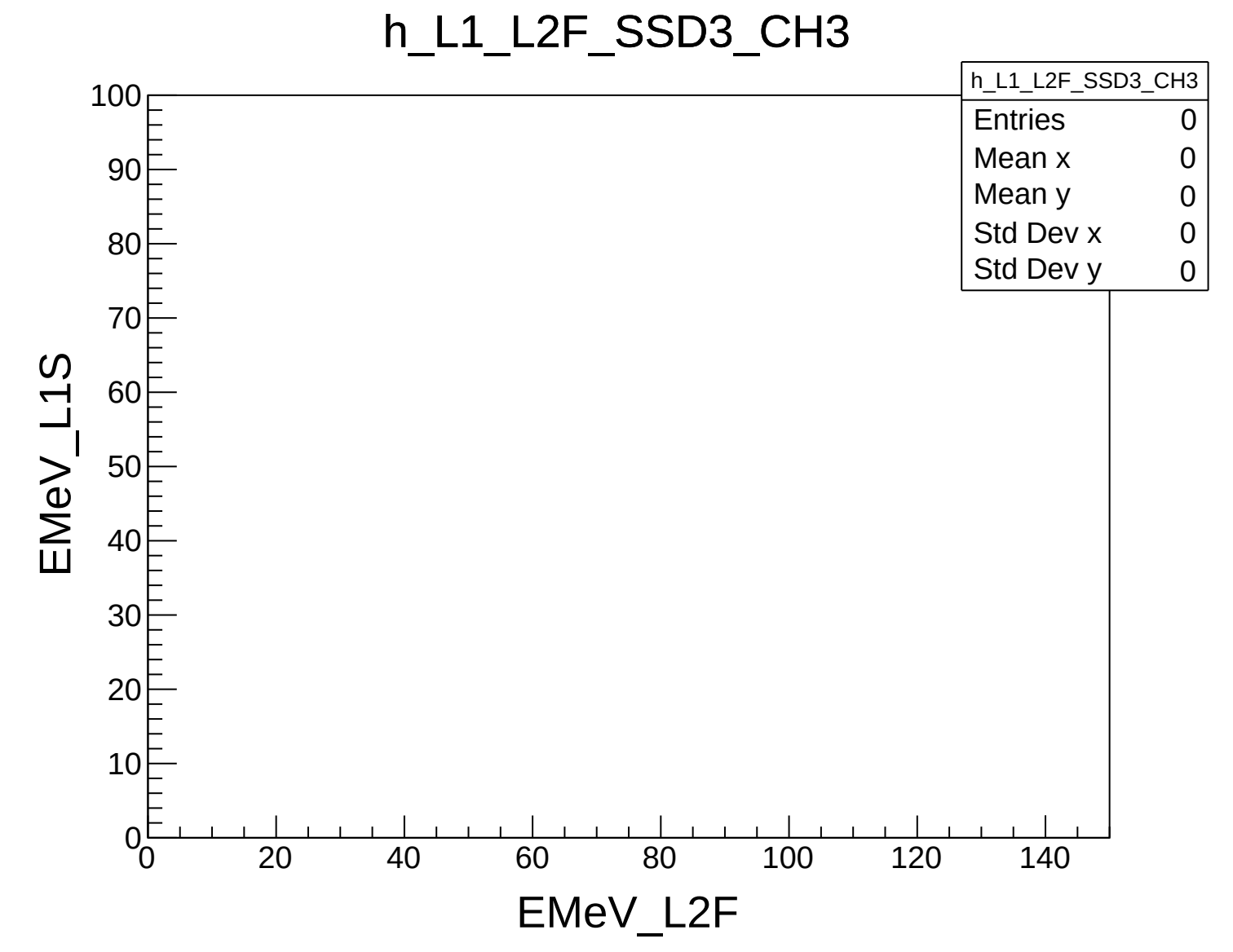

h_L1_L2F_SSD2_CH14
h_L1_L2F_SSD2_CH14
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

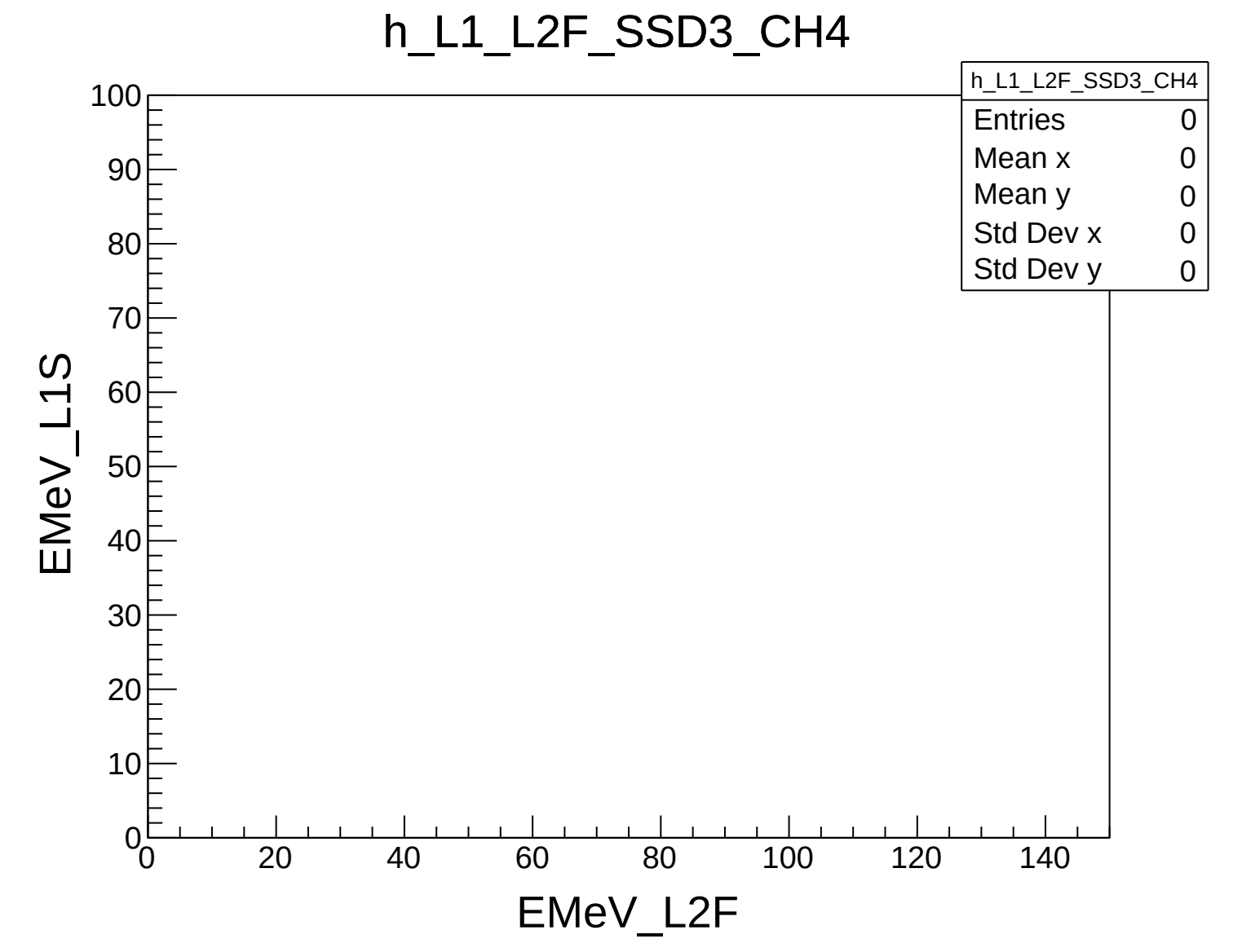

h_L1_L2F_SSD2_CH15
h_L1_L2F_SSD2_CH15
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250

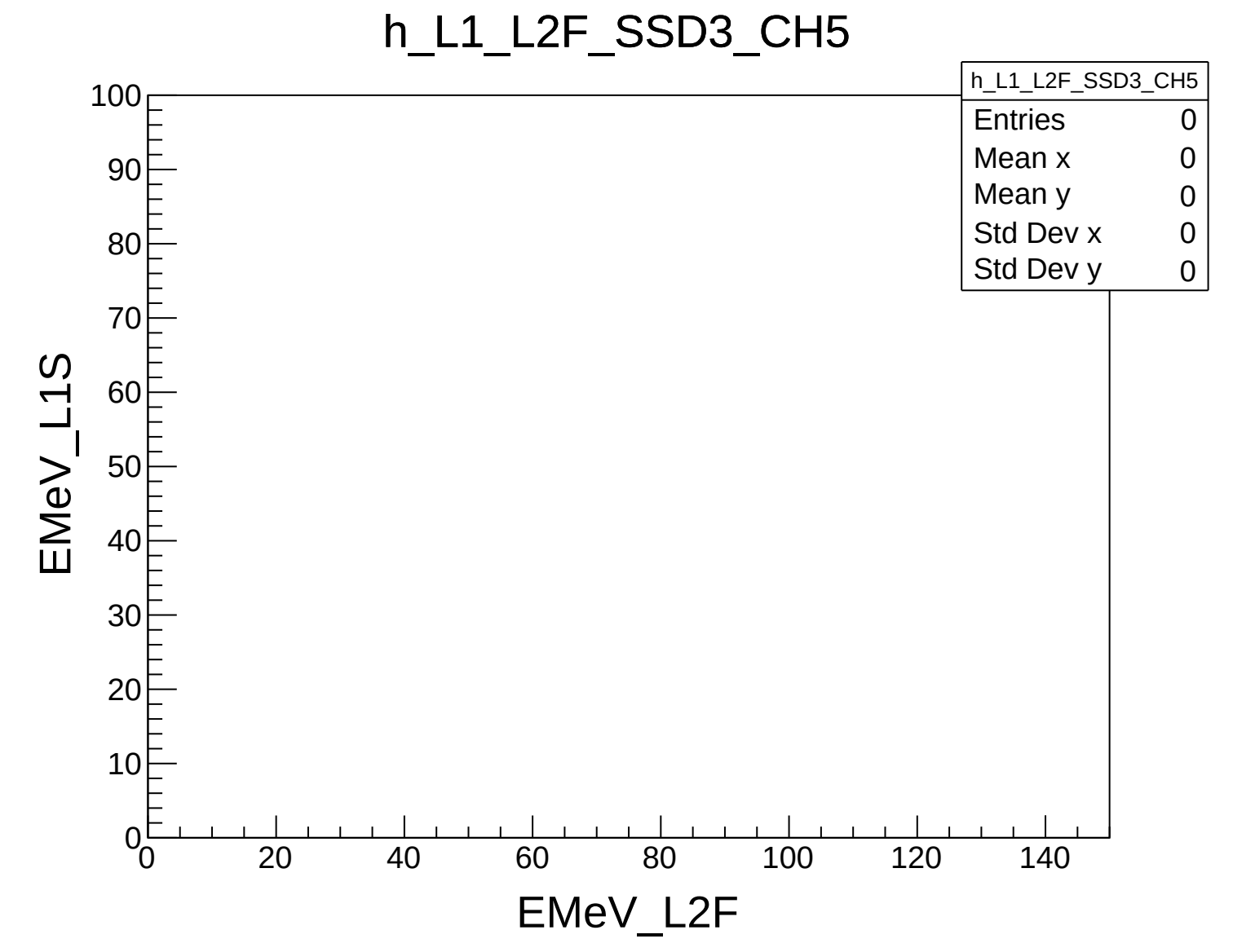

h_L1_L2F_SSD3_CH0
h_L1_L2F_SSD3_CH0
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

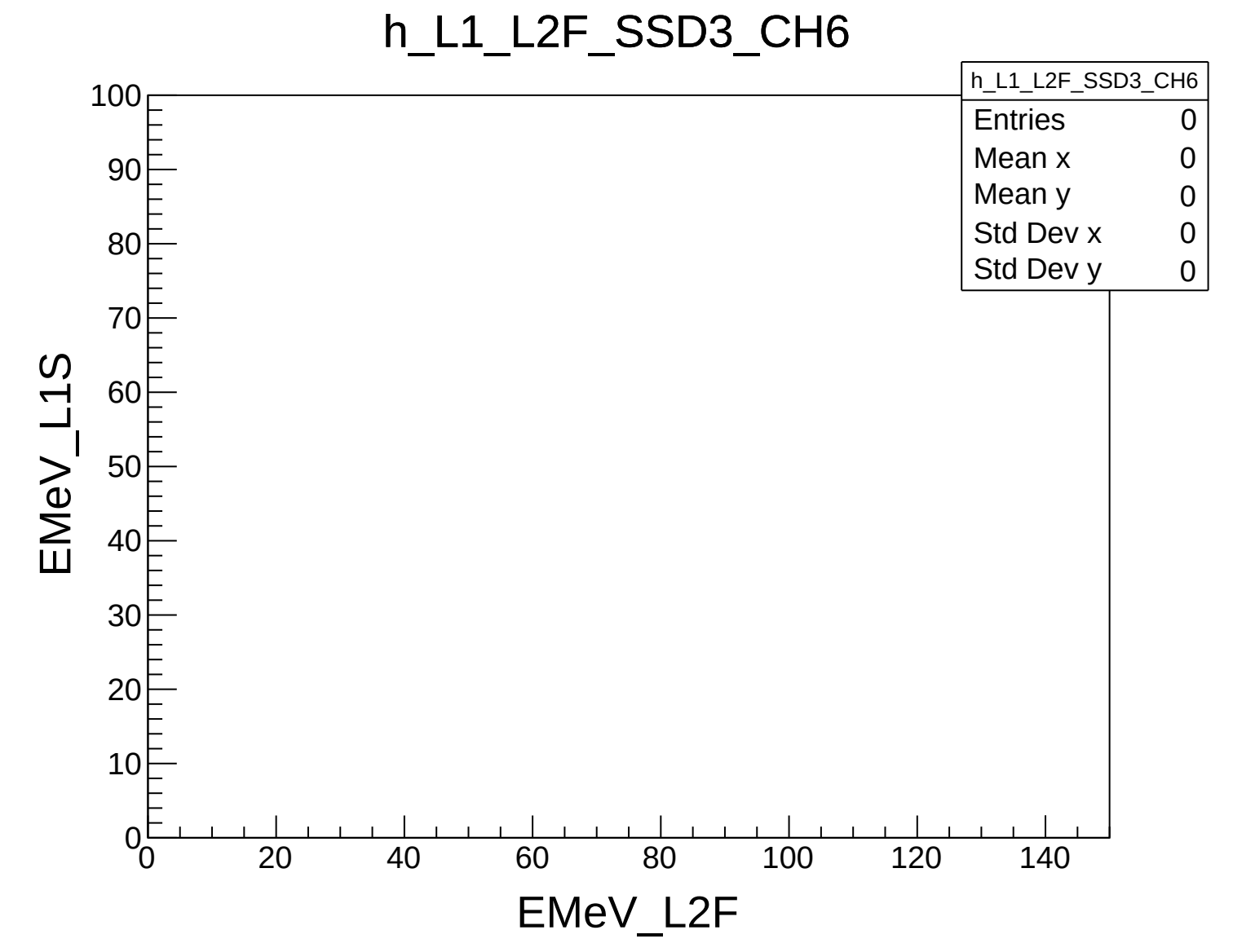

h_L1_L2F_SSD3_CH1
h_L1_L2F_SSD3_CH1
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

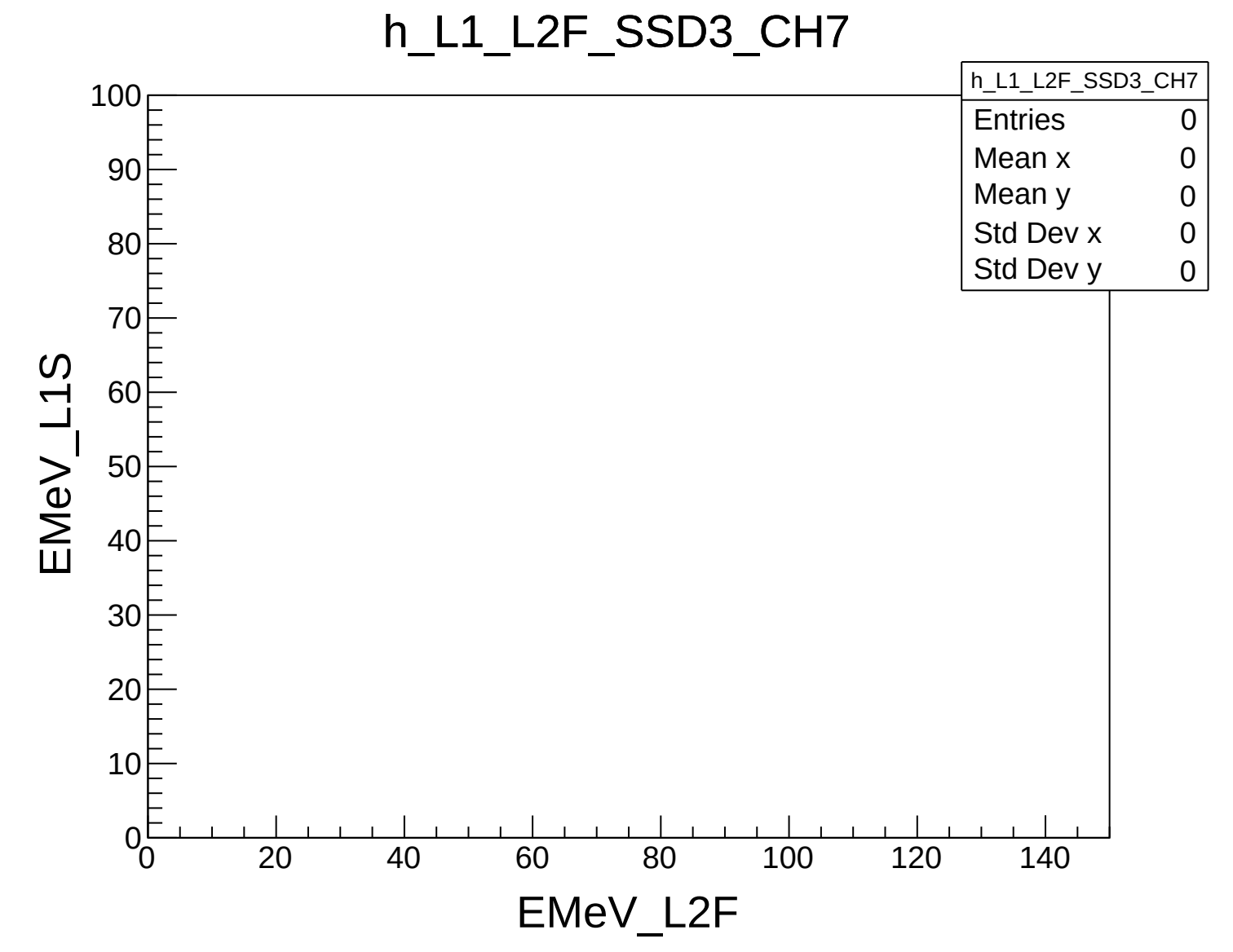

h_L1_L2F_SSD3_CH2
h_L1_L2F_SSD3_CH2
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

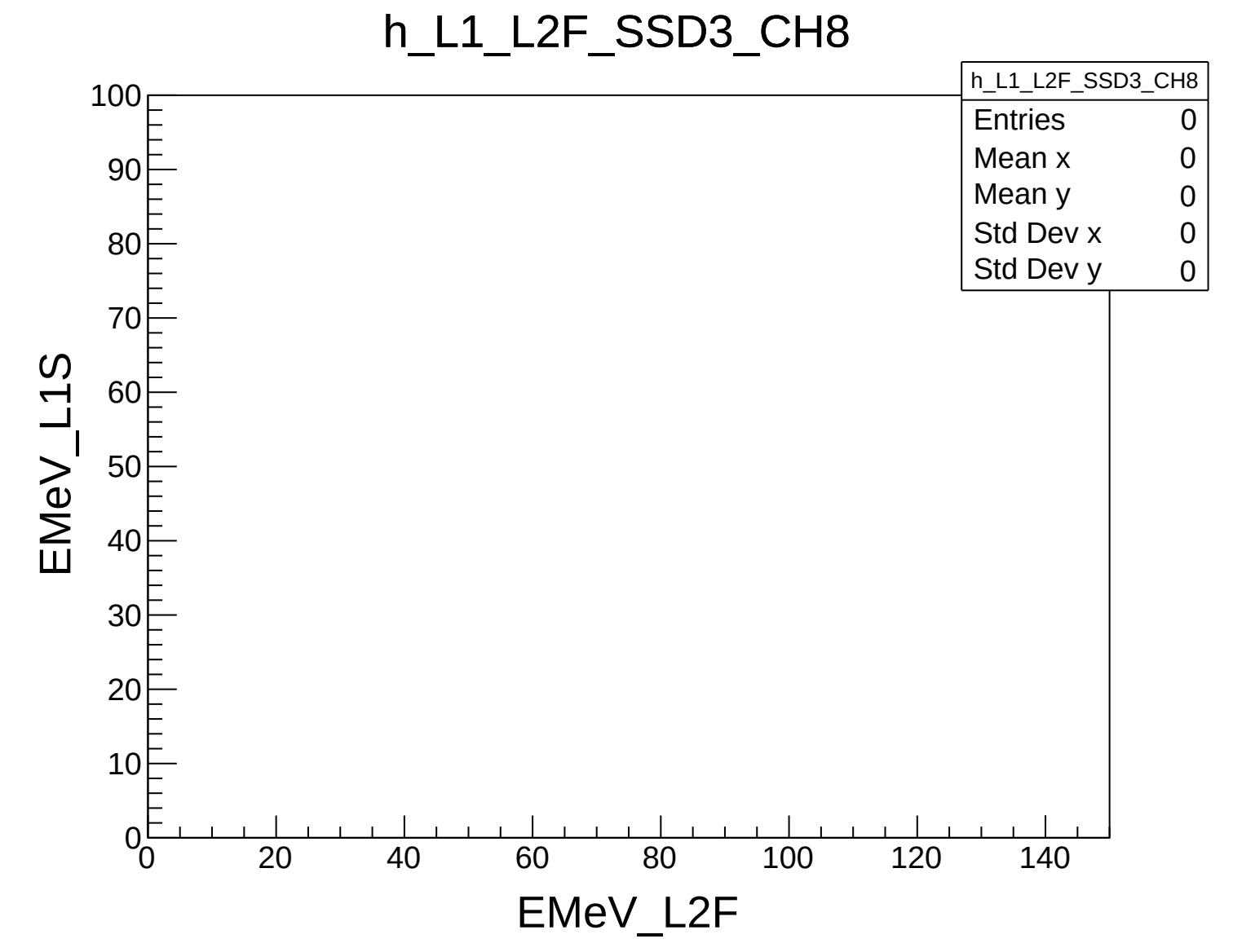

h_L1_L2F_SSD3_CH3
h_L1_L2F_SSD3_CH3
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

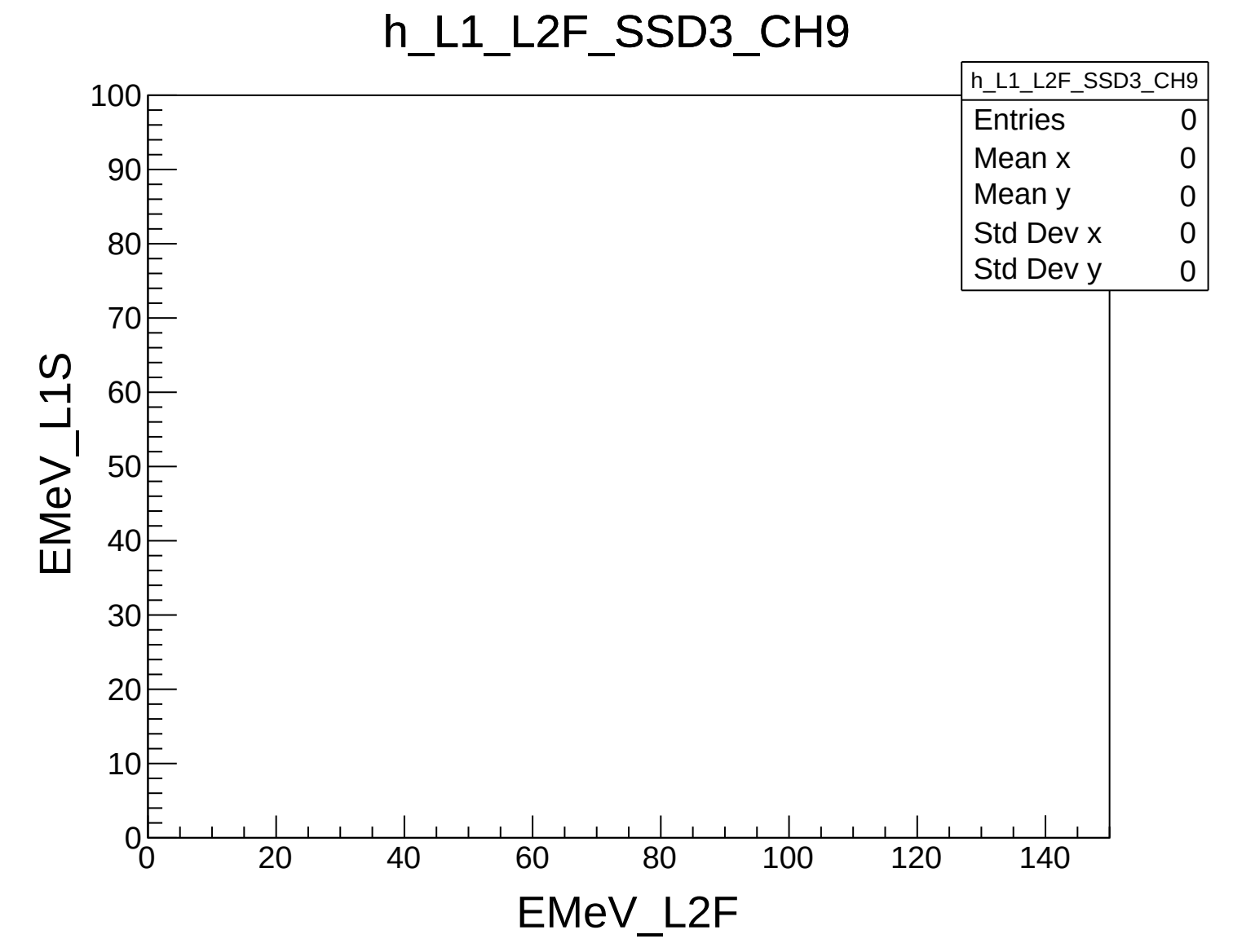

h_L1_L2F_SSD3_CH4
h_L1_L2F_SSD3_CH4
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

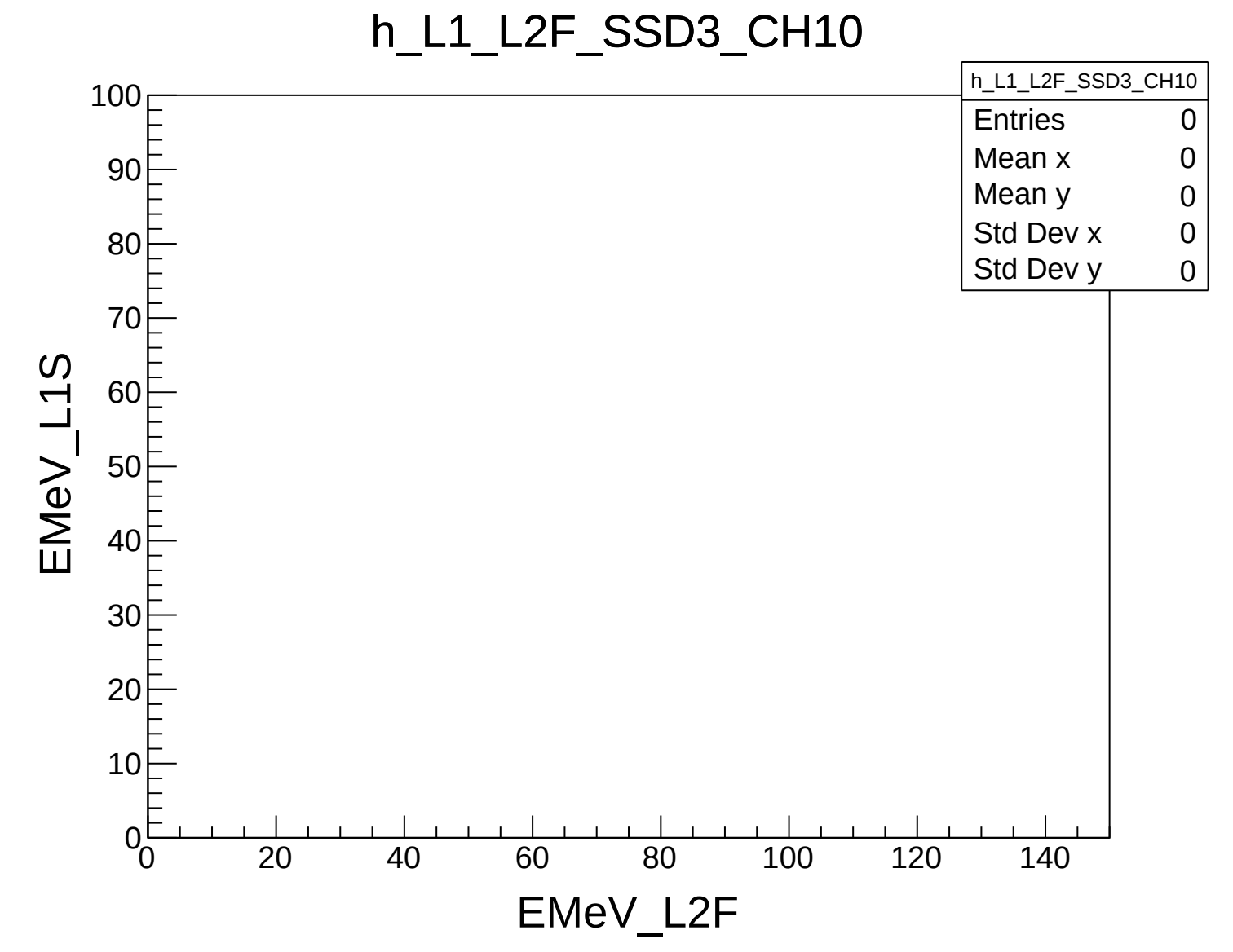

h_L1_L2F_SSD3_CH5
h_L1_L2F_SSD3_CH5
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

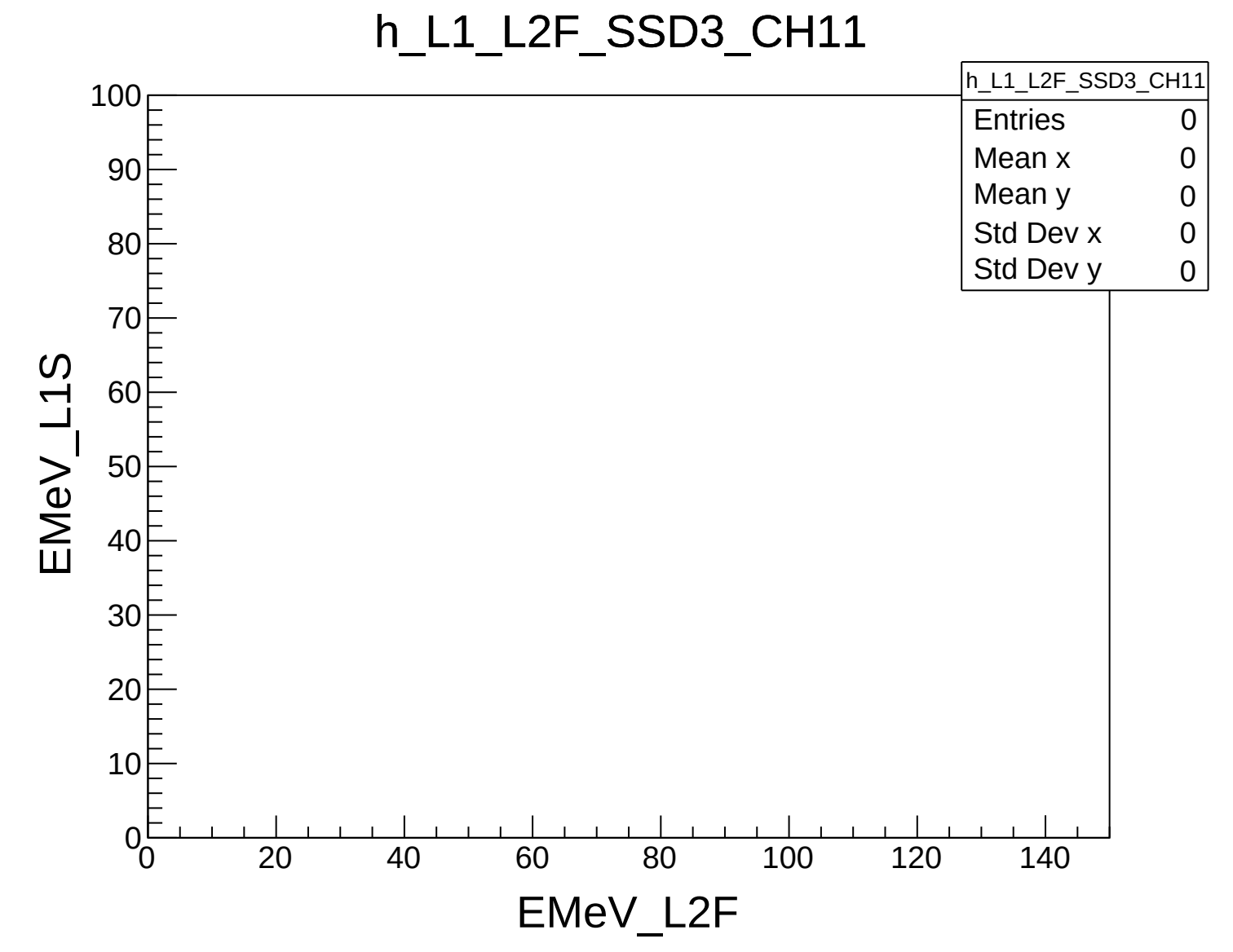

h_L1_L2F_SSD3_CH6
h_L1_L2F_SSD3_CH6
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

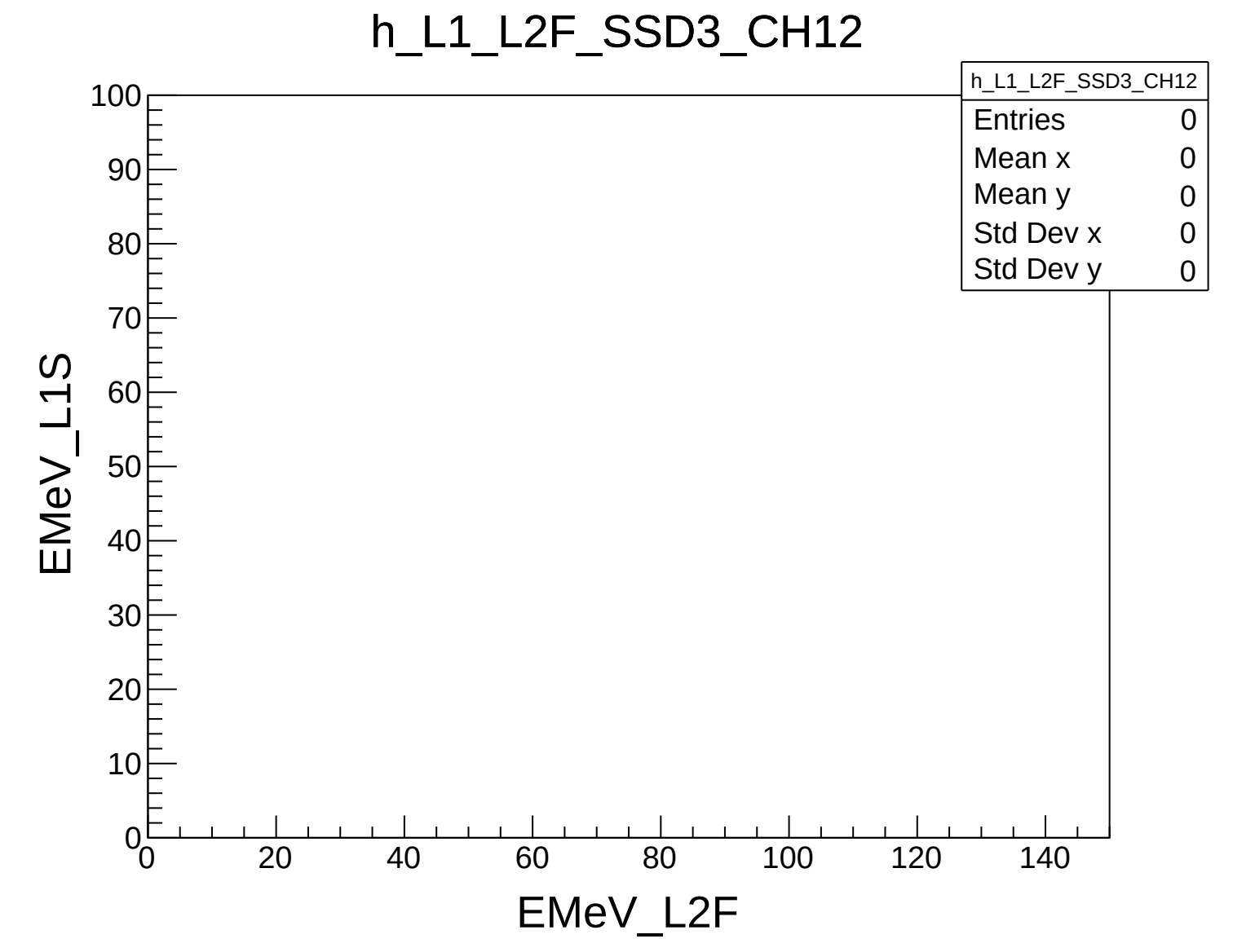

h_L1_L2F_SSD3_CH7
h_L1_L2F_SSD3_CH7
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

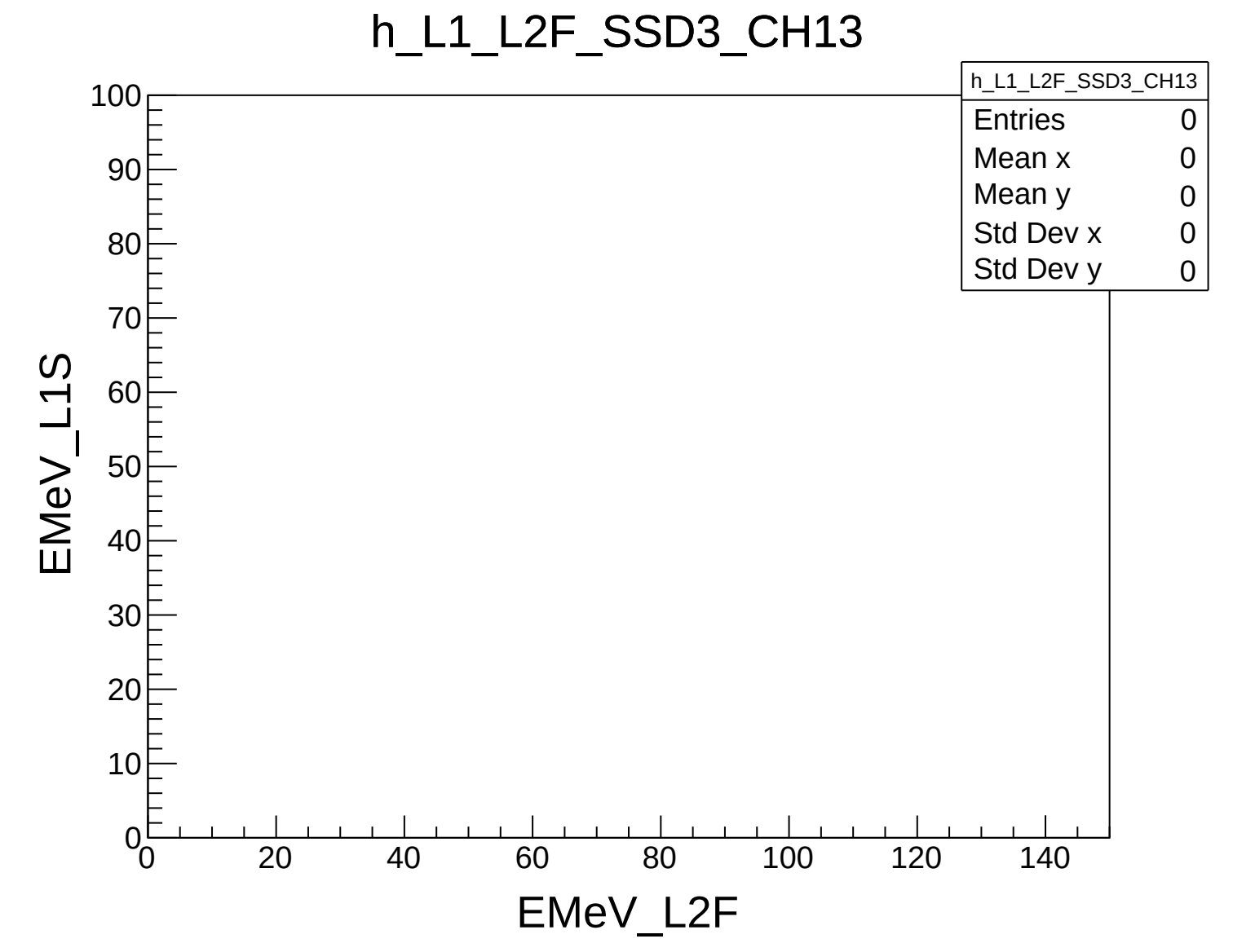

h_L1_L2F_SSD3_CH8
h_L1_L2F_SSD3_CH8
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

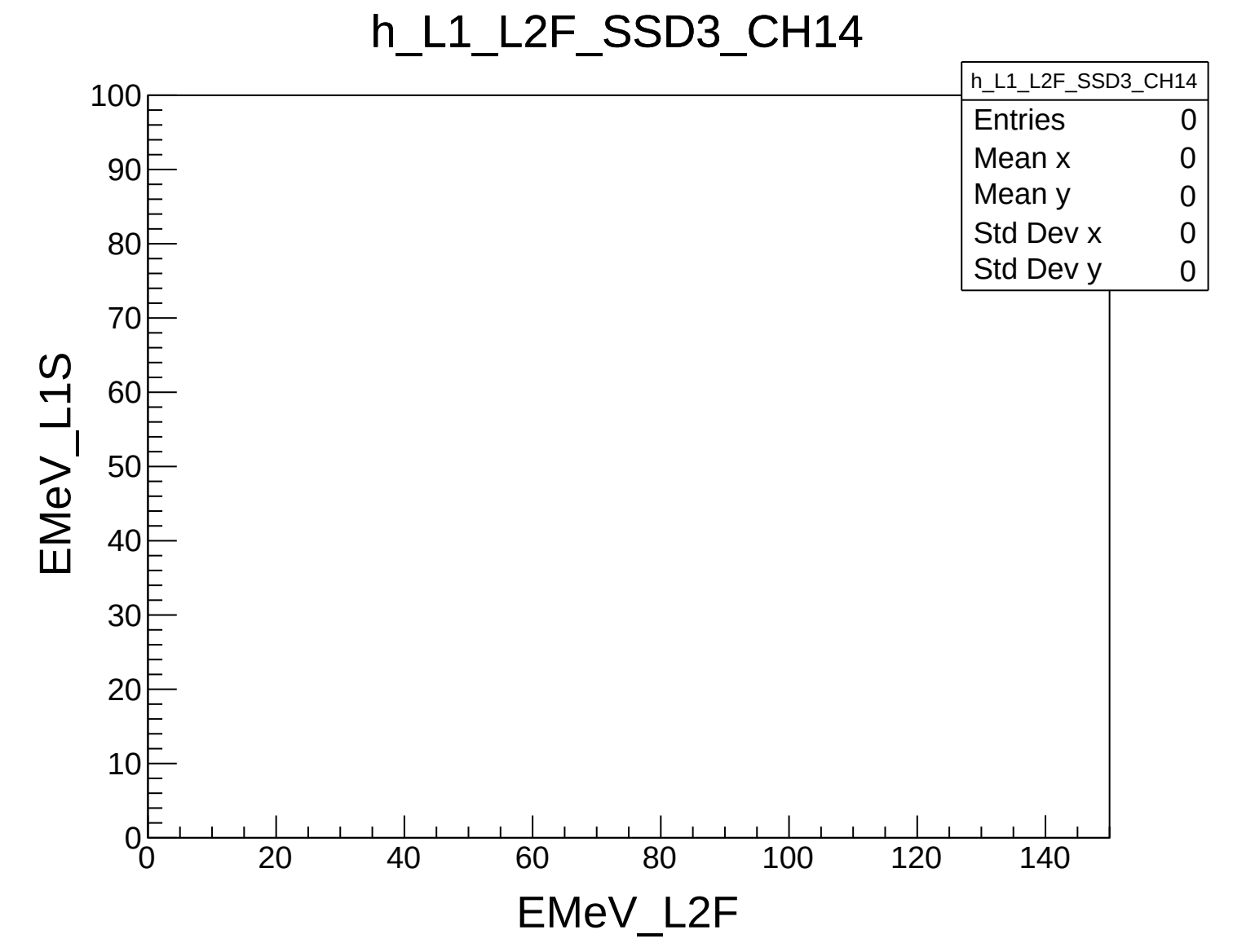

h_L1_L2F_SSD3_CH9
h_L1_L2F_SSD3_CH9
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

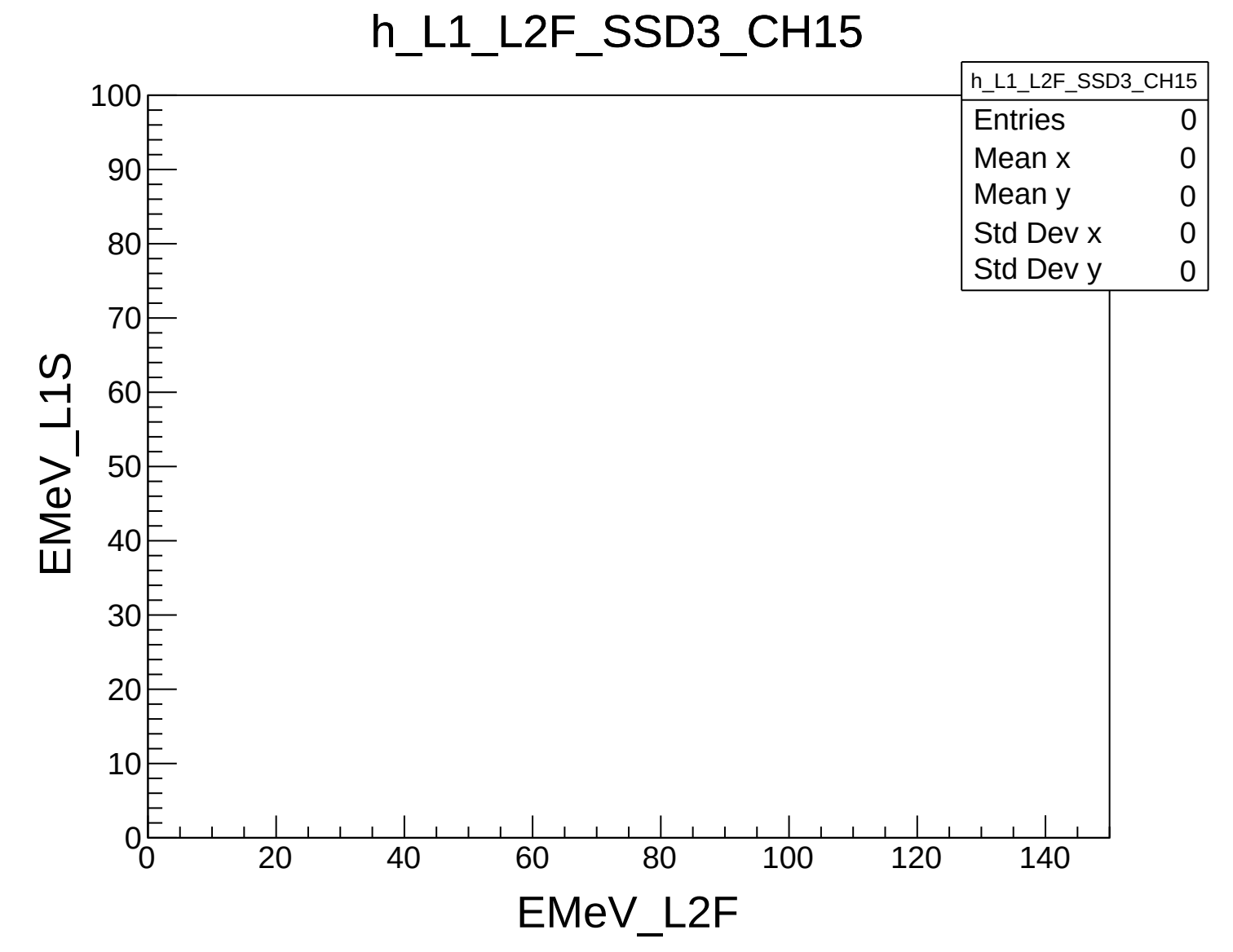

h_L1_L2F_SSD3_CH10
h_L1_L2F_SSD3_CH10
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

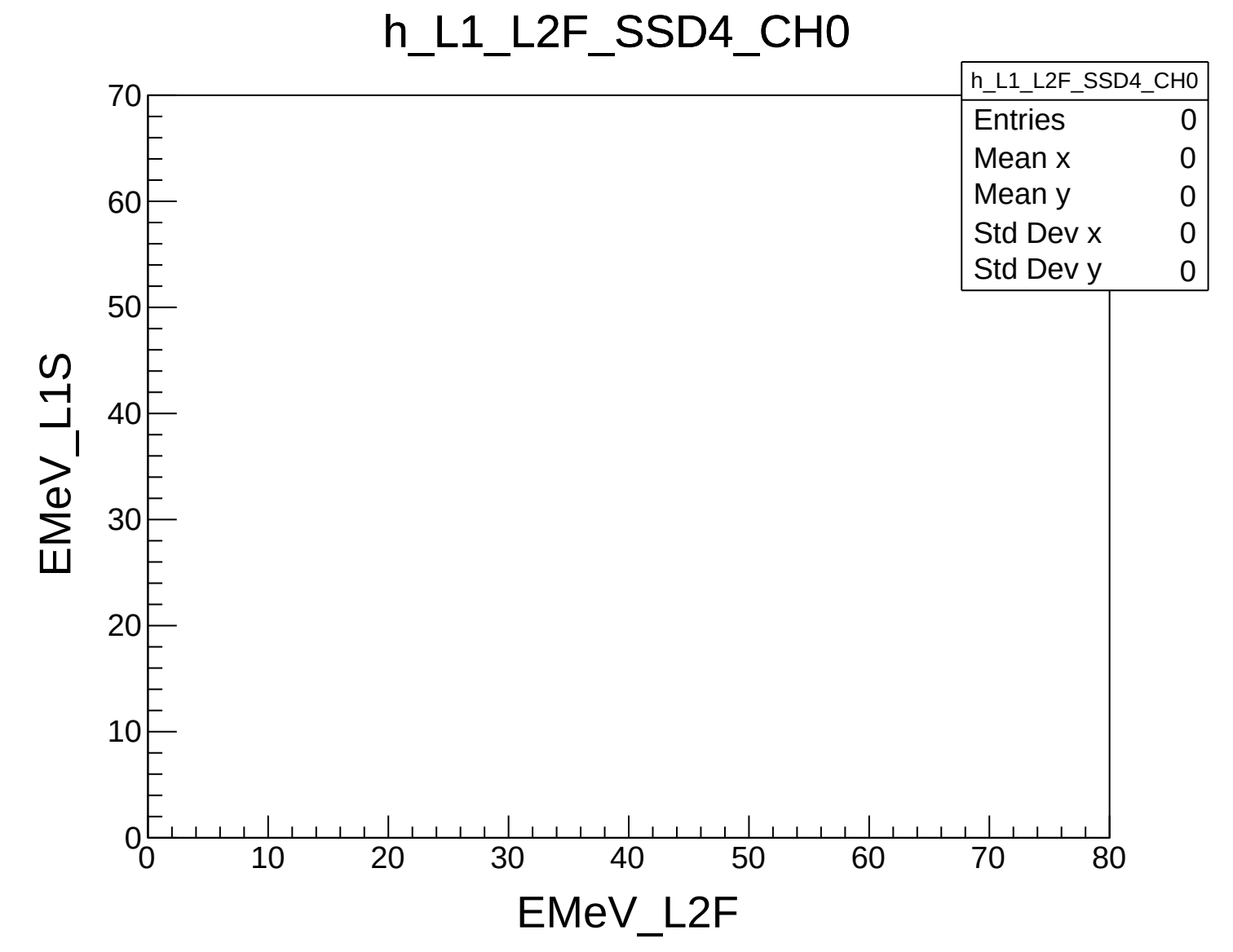

h_L1_L2F_SSD3_CH11
h_L1_L2F_SSD3_CH11
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

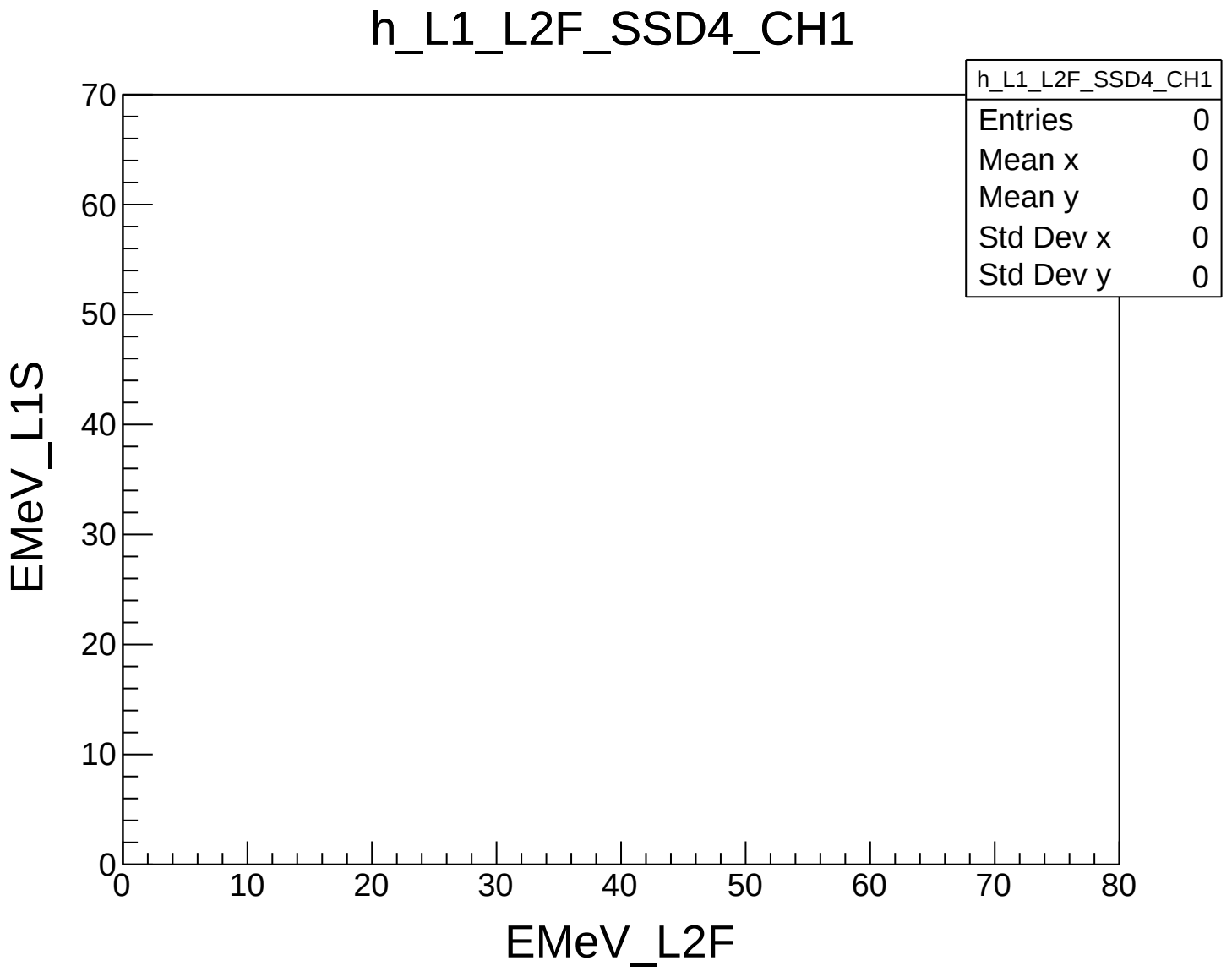

h_L1_L2F_SSD3_CH12
h_L1_L2F_SSD3_CH12
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

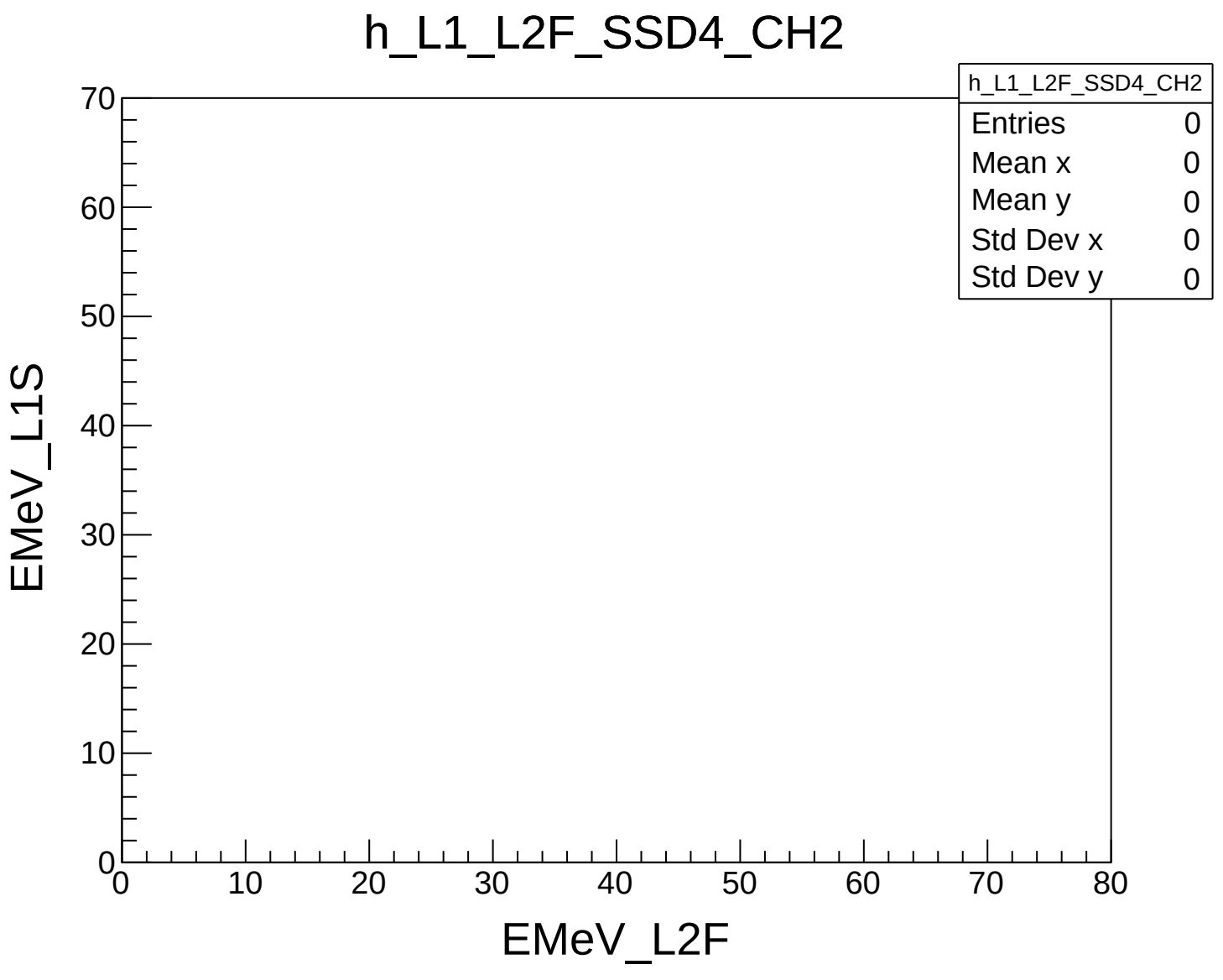

h_L1_L2F_SSD3_CH13
h_L1_L2F_SSD3_CH13
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

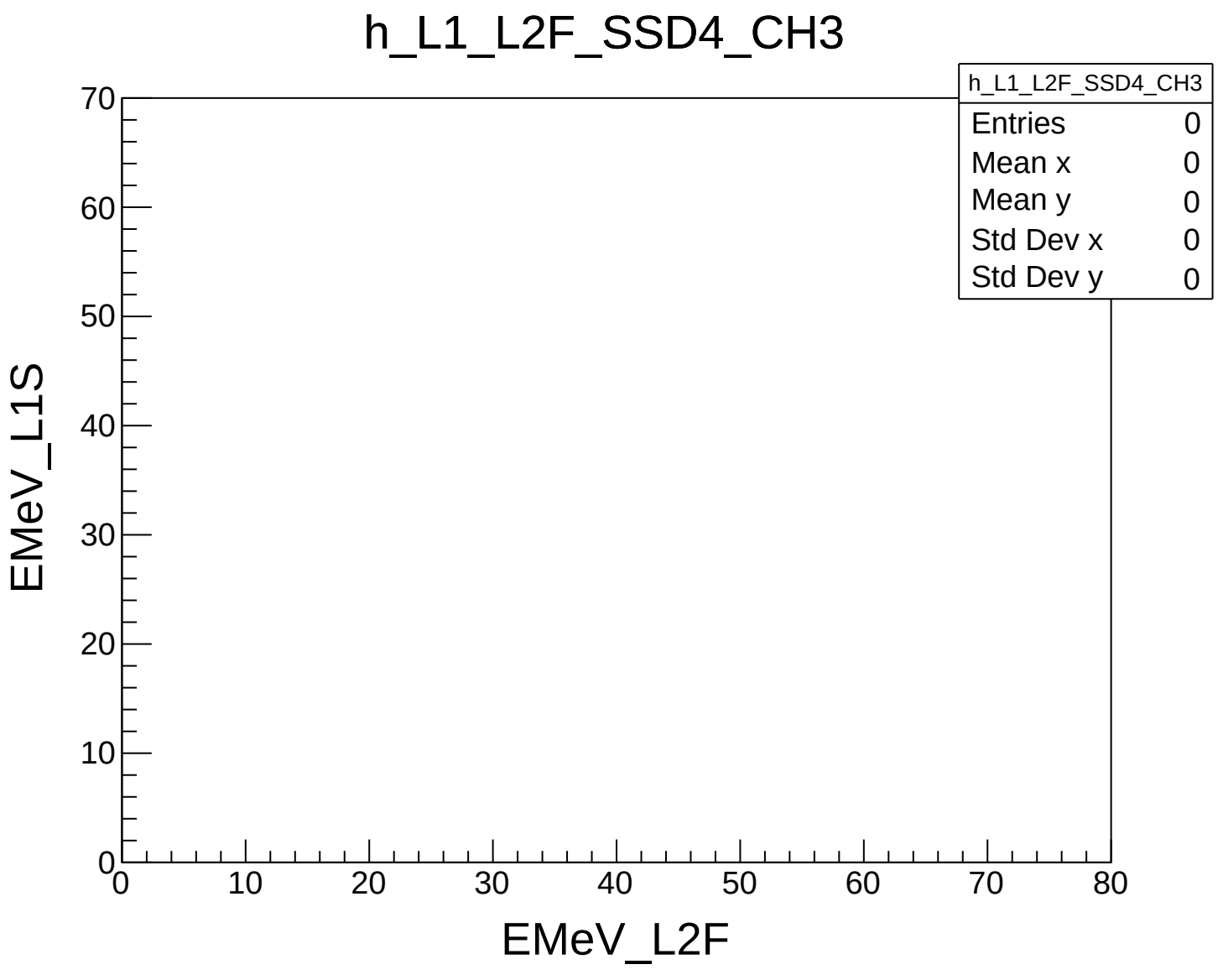

h_L1_L2F_SSD3_CH14
h_L1_L2F_SSD3_CH14
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

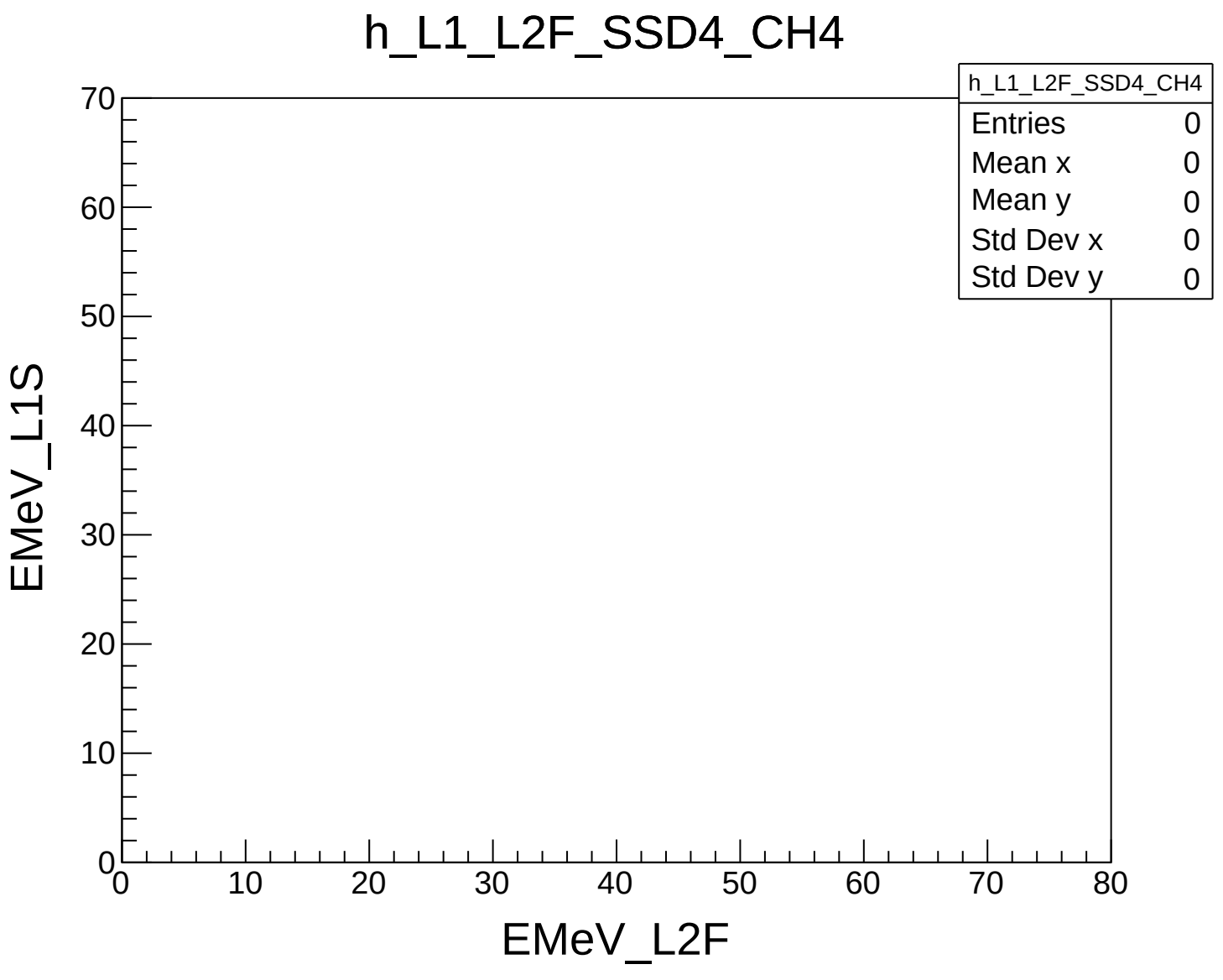

h_L1_L2F_SSD3_CH15
h_L1_L2F_SSD3_CH15
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140

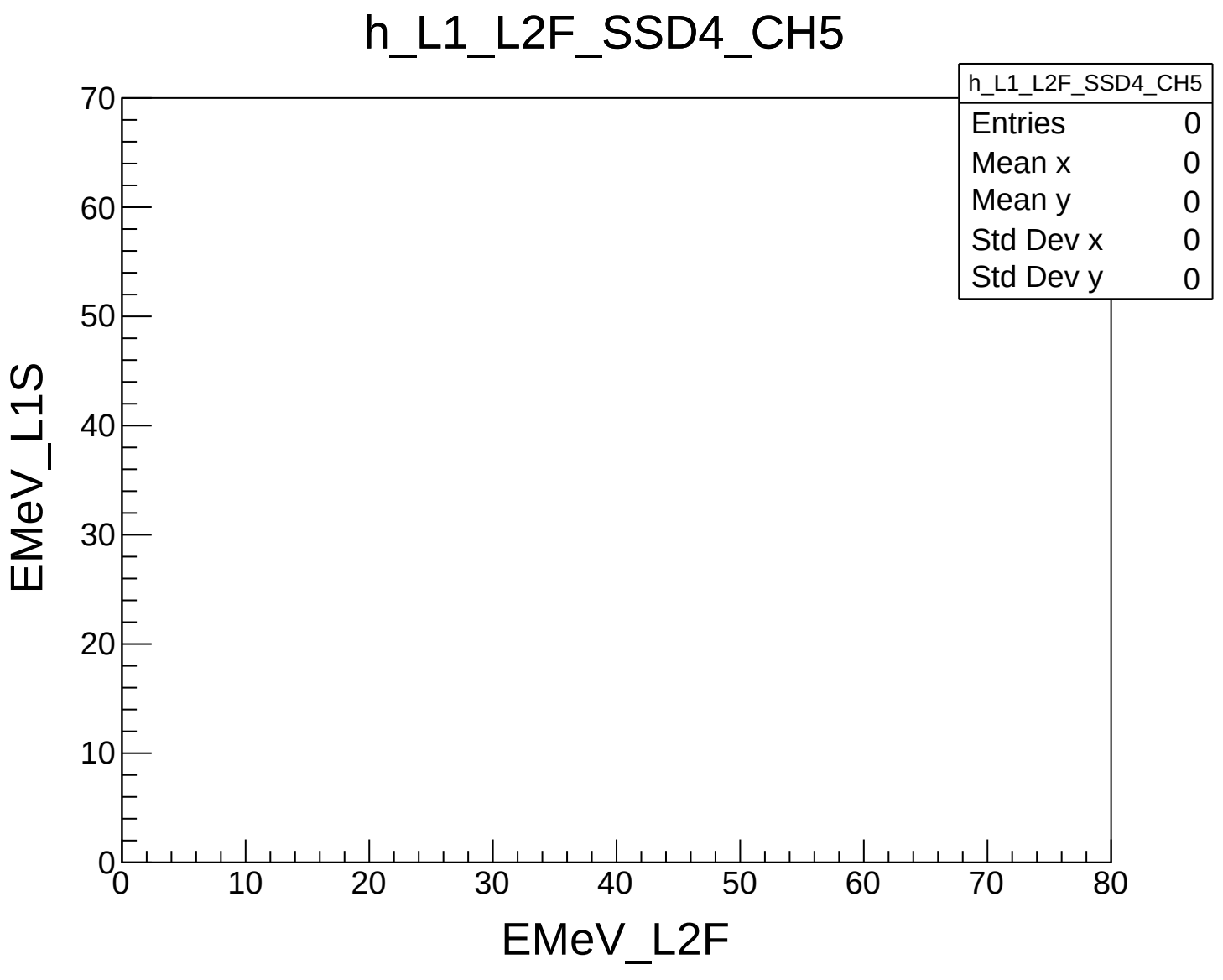

h_L1_L2F_SSD4_CH0
h_L1_L2F_SSD4_CH0
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

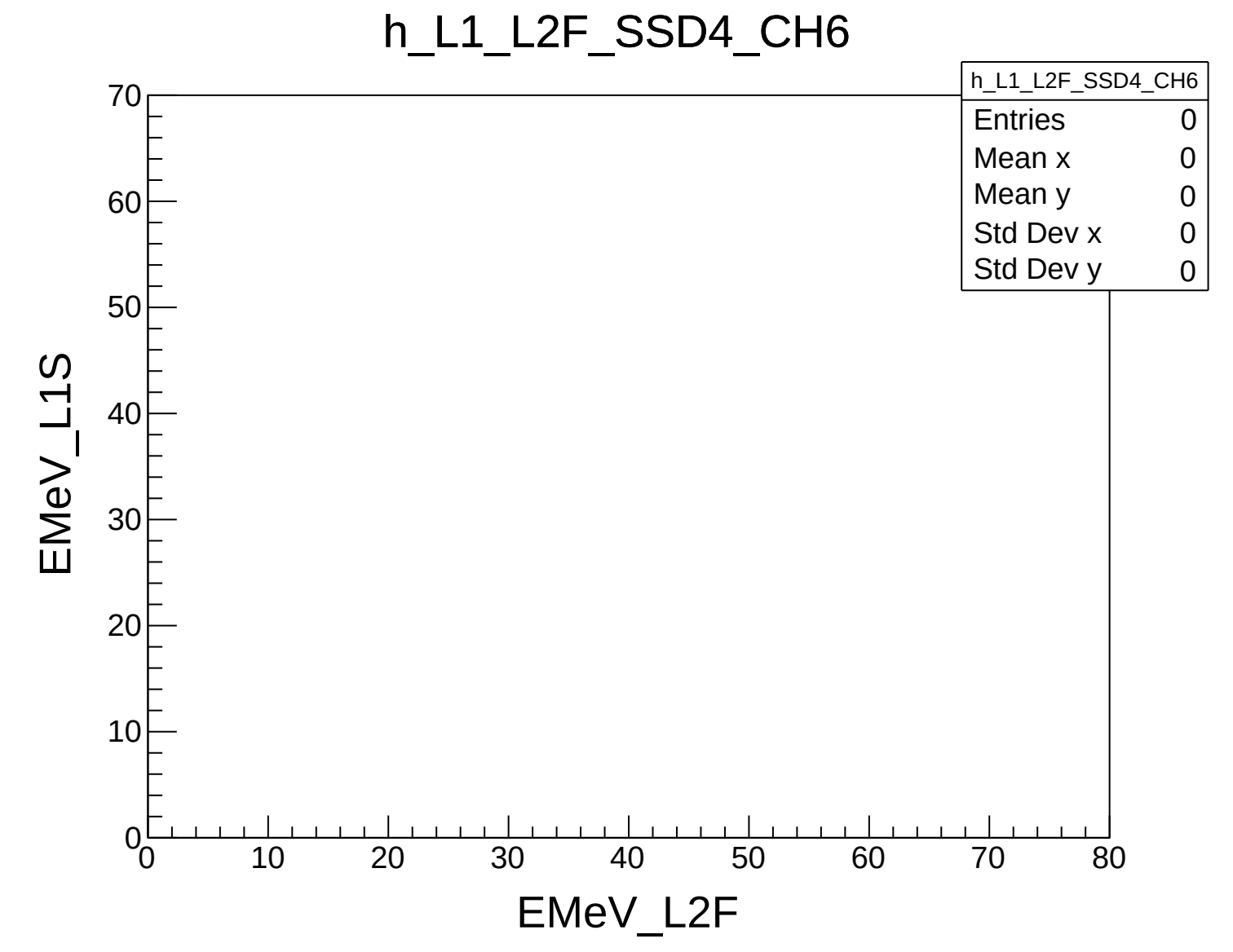

h_L1_L2F_SSD4_CH1
h_L1_L2F_SSD4_CH1
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

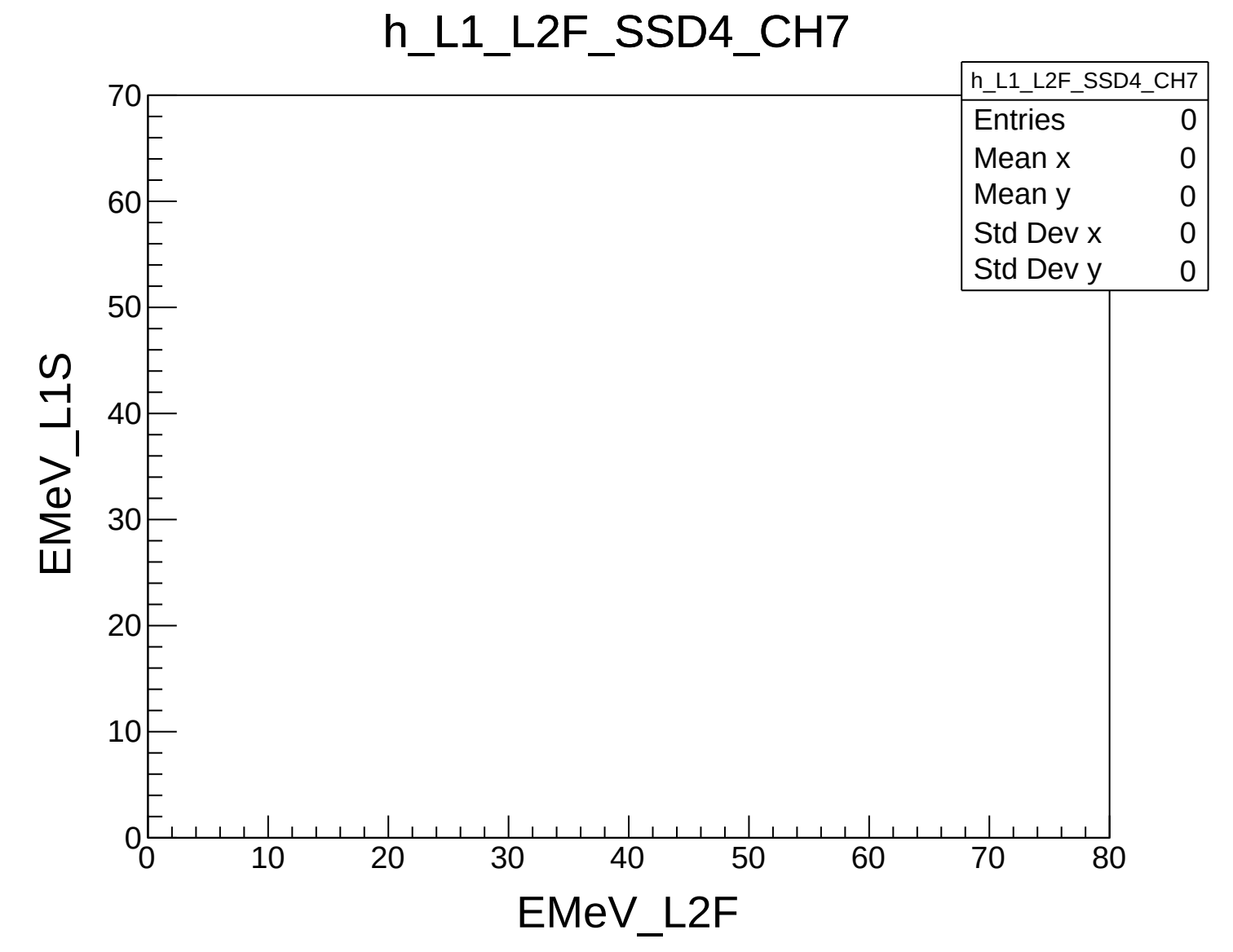

h_L1_L2F_SSD4_CH2
h_L1_L2F_SSD4_CH2
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

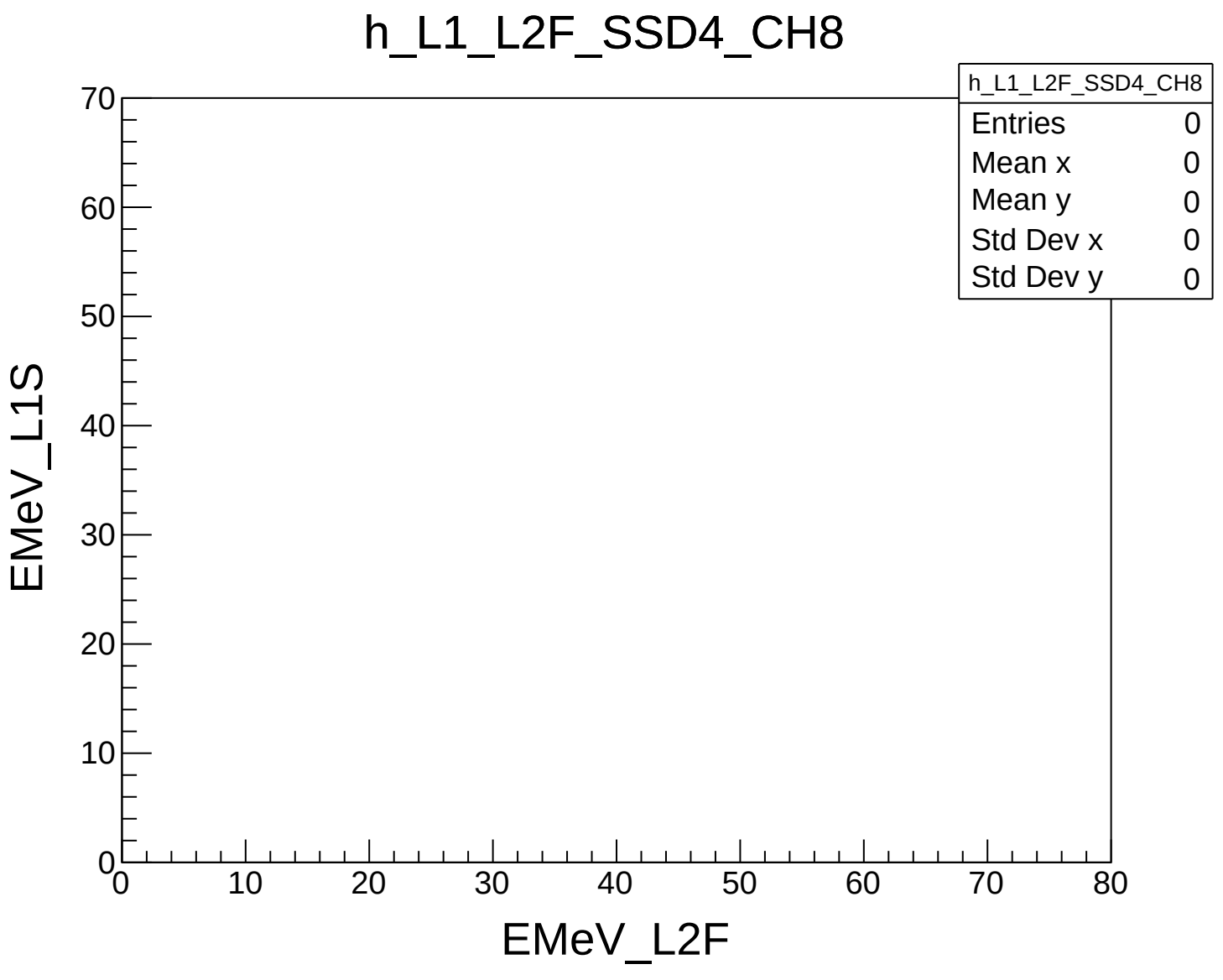

h_L1_L2F_SSD4_CH3
h_L1_L2F_SSD4_CH3
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

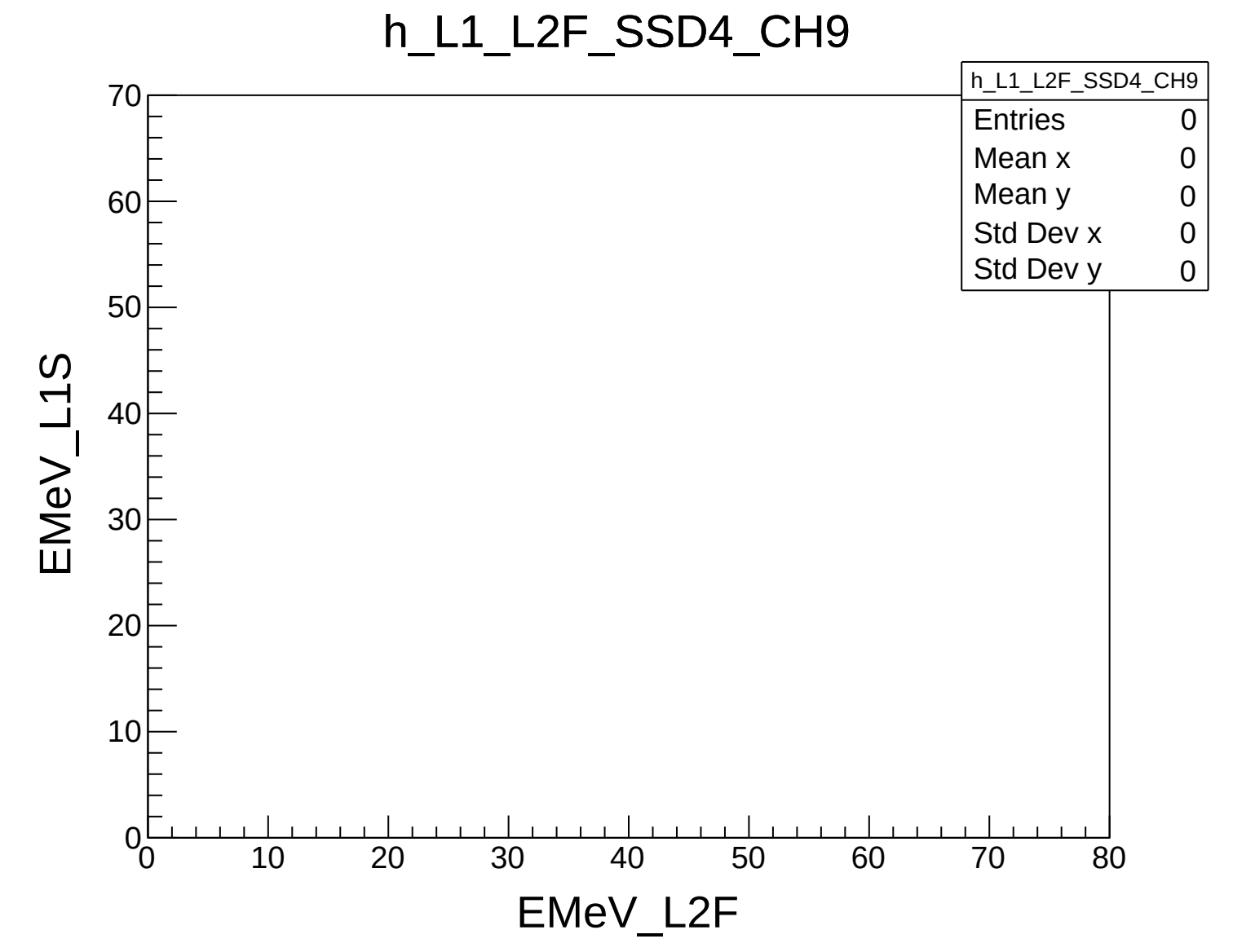

h_L1_L2F_SSD4_CH4
h_L1_L2F_SSD4_CH4
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

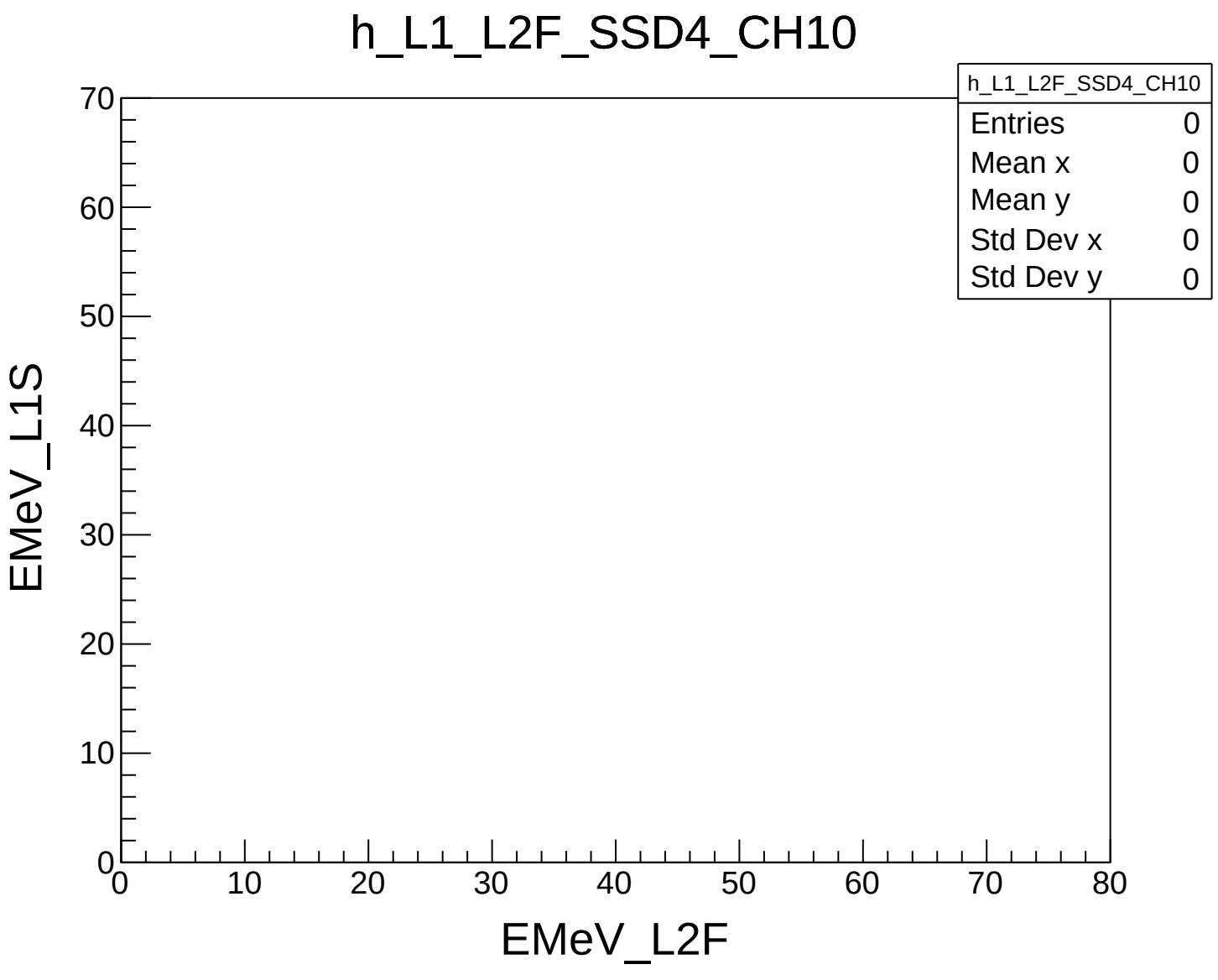

h_L1_L2F_SSD4_CH5
h_L1_L2F_SSD4_CH5
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

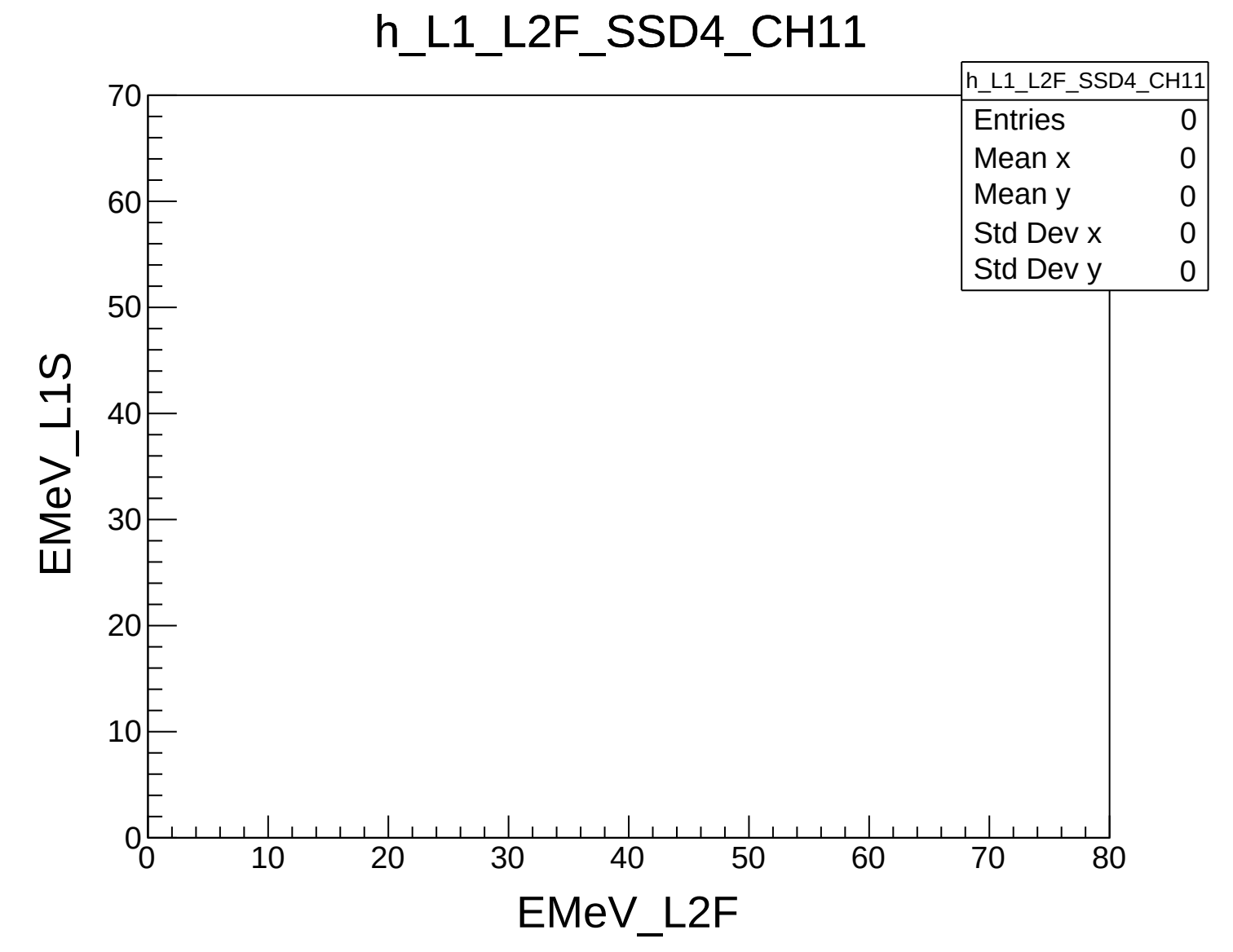

h_L1_L2F_SSD4_CH6
h_L1_L2F_SSD4_CH6
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

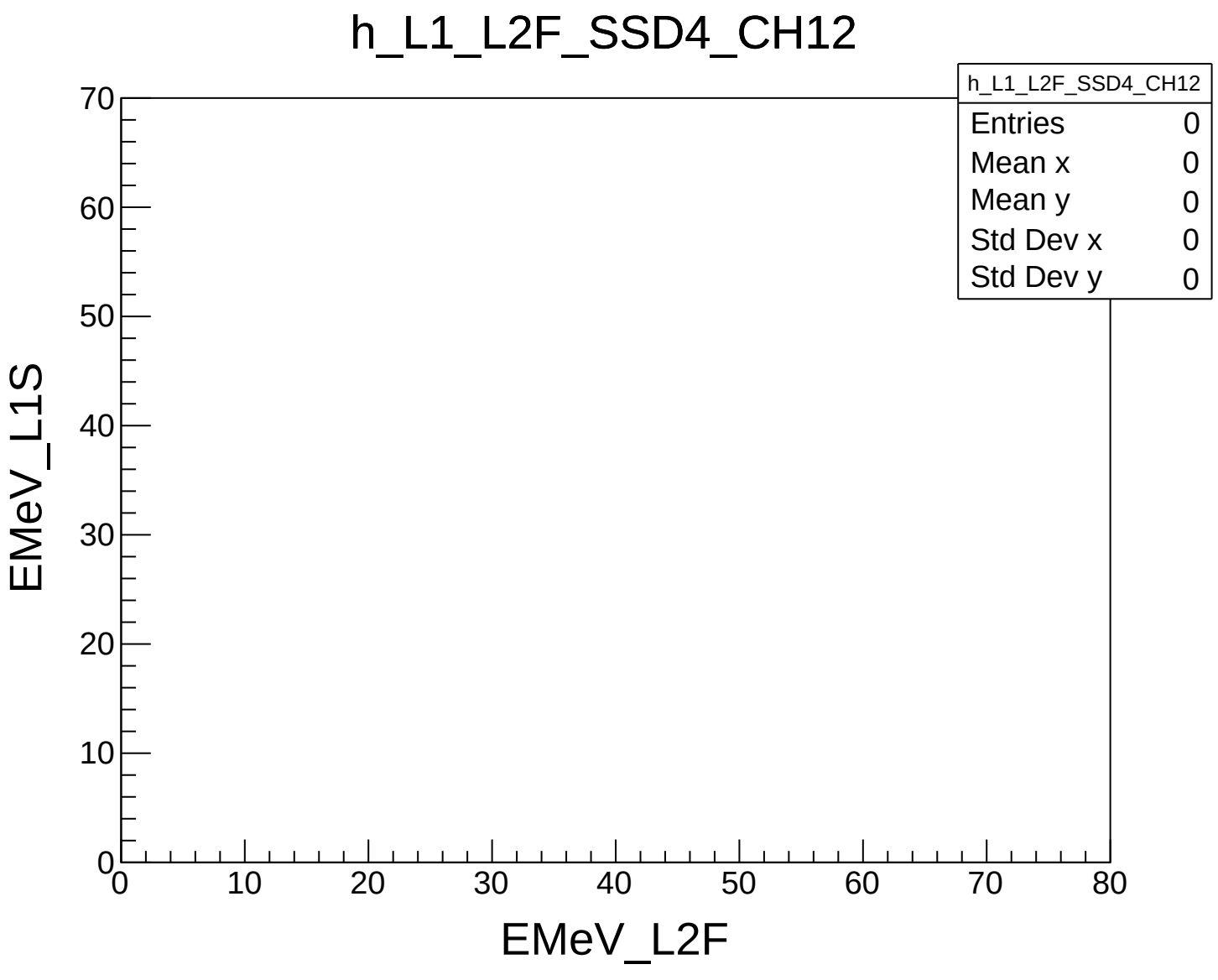

h_L1_L2F_SSD4_CH7
h_L1_L2F_SSD4_CH7
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

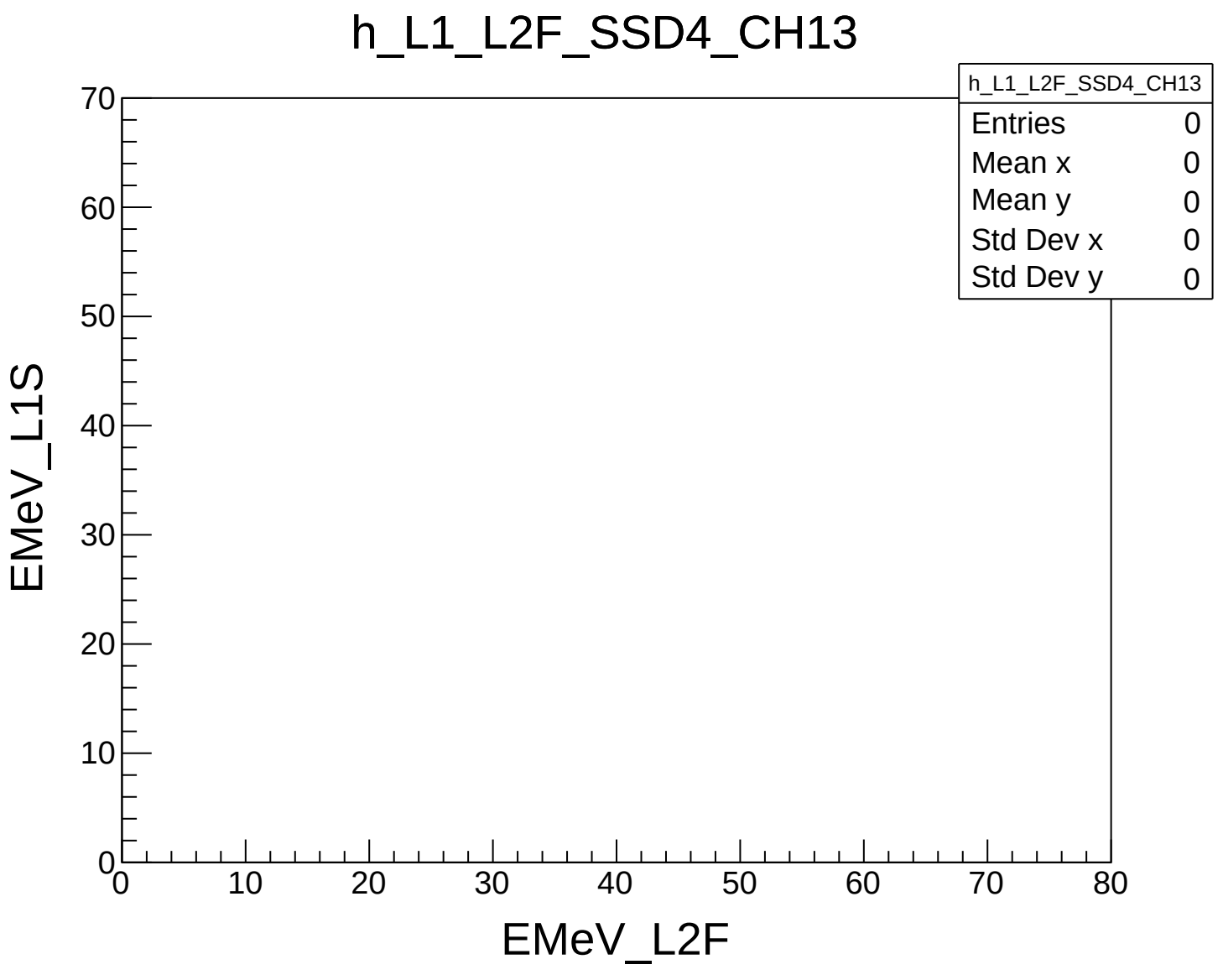

h_L1_L2F_SSD4_CH8
h_L1_L2F_SSD4_CH8
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

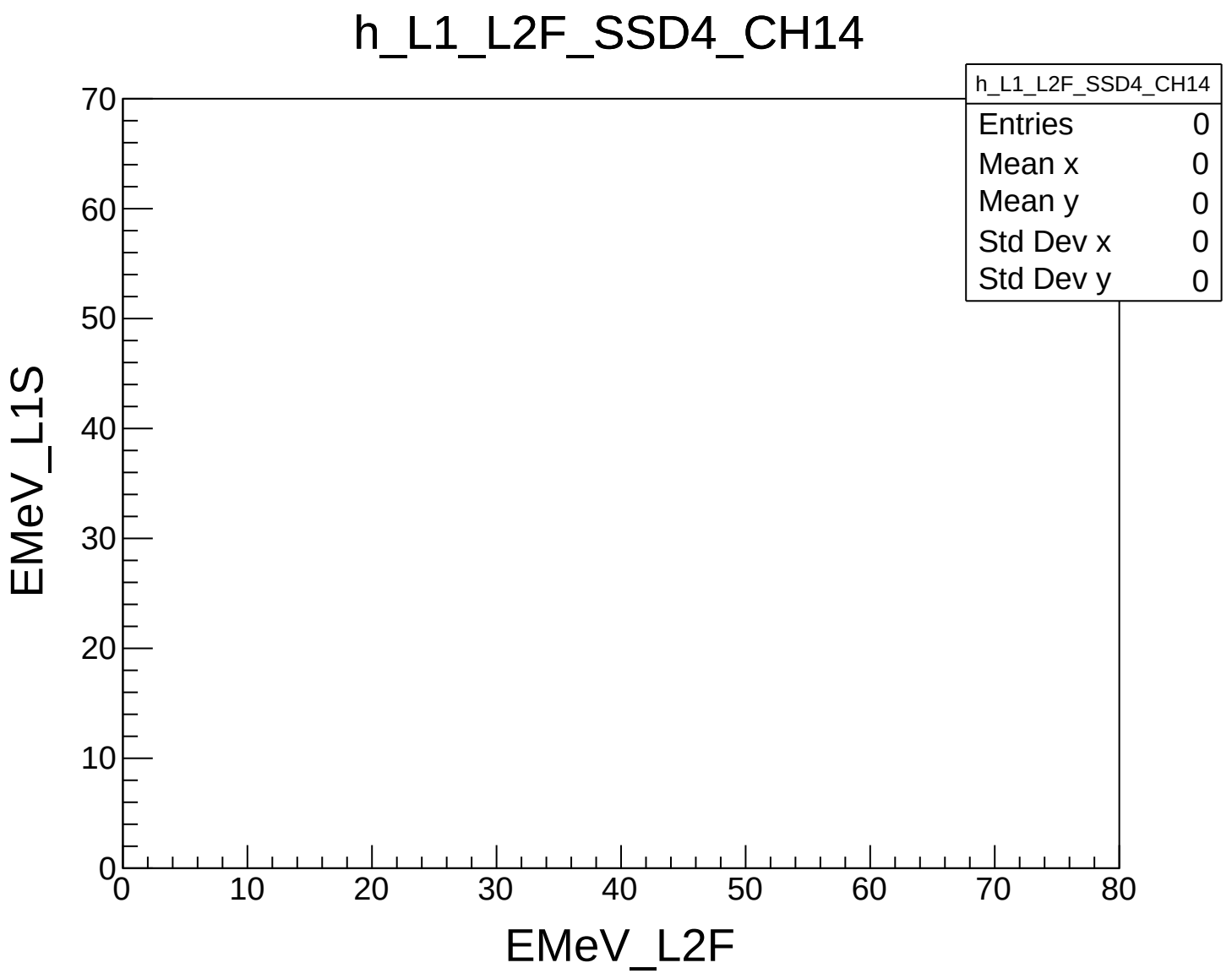

h_L1_L2F_SSD4_CH9
h_L1_L2F_SSD4_CH9
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

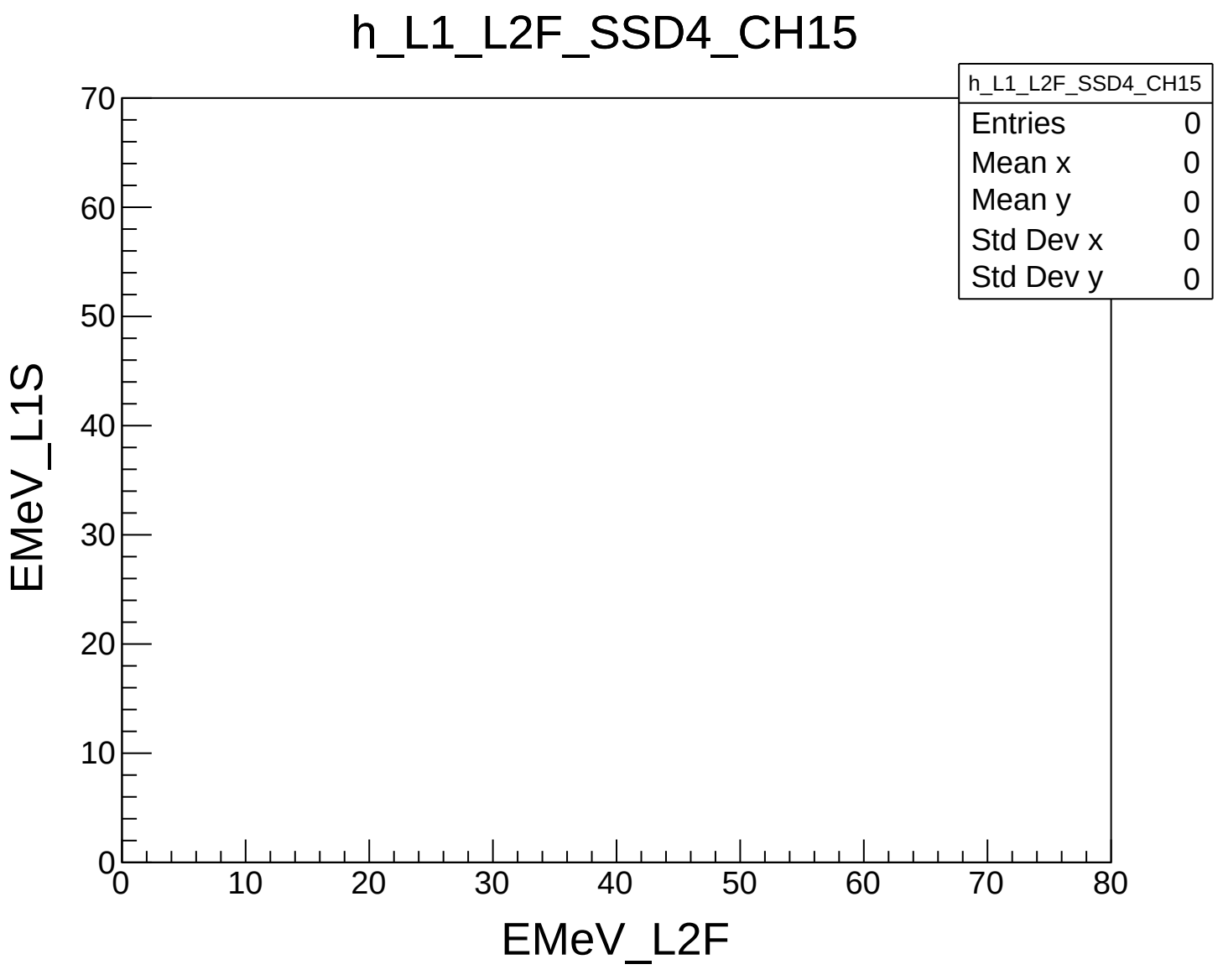

h_L1_L2F_SSD4_CH10
h_L1_L2F_SSD4_CH10
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80


h_L1_L2F_SSD4_CH11
h_L1_L2F_SSD4_CH11
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80


h_L1_L2F_SSD4_CH12
h_L1_L2F_SSD4_CH12
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80


h_L1_L2F_SSD4_CH13
h_L1_L2F_SSD4_CH13
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80


h_L1_L2F_SSD4_CH14
h_L1_L2F_SSD4_CH14
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80


h_L1_L2F_SSD4_CH15
h_L1_L2F_SSD4_CH15
Entries 0
Mean x 0
Mean y 0
Std Dev x 0
Std Dev y 0
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80