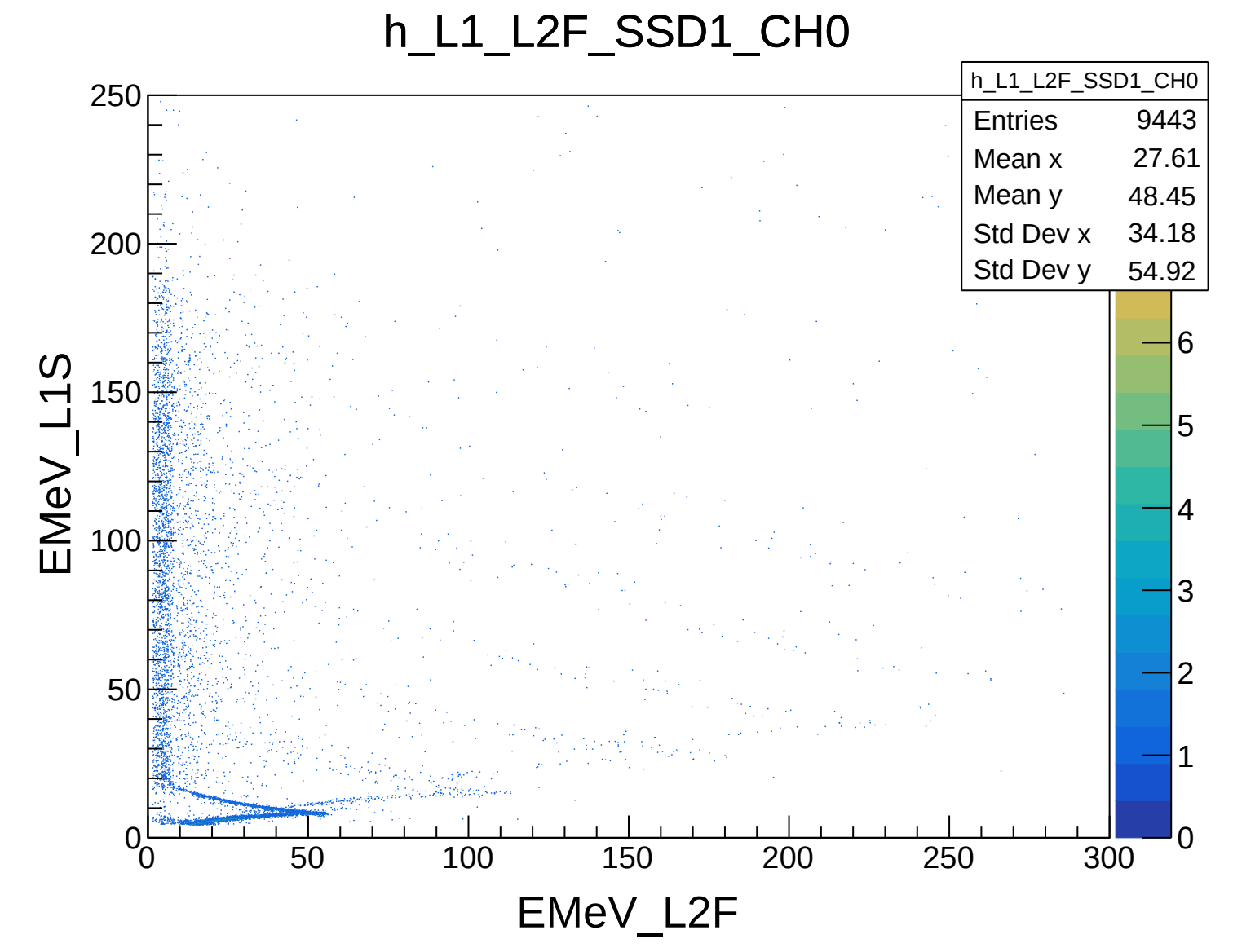
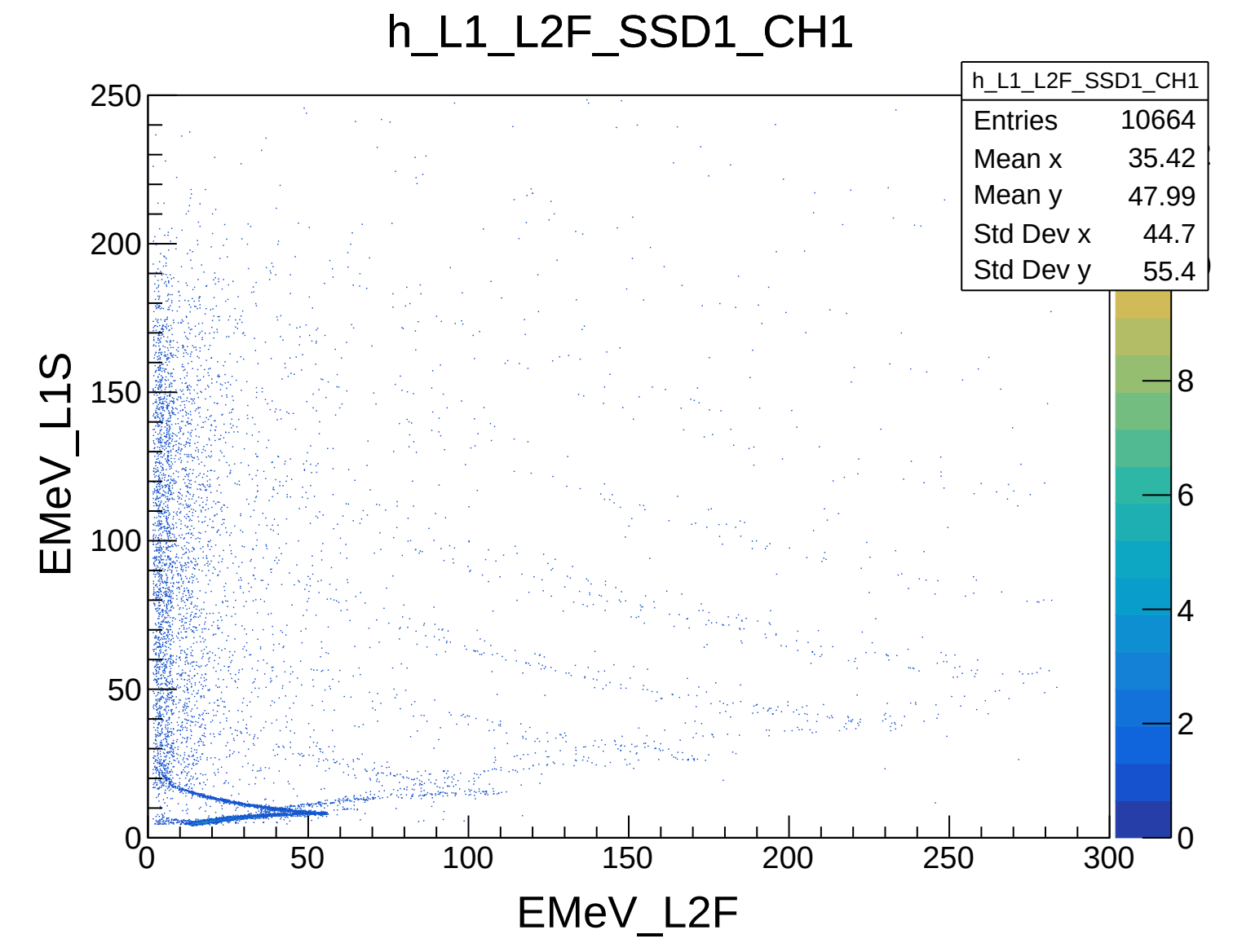
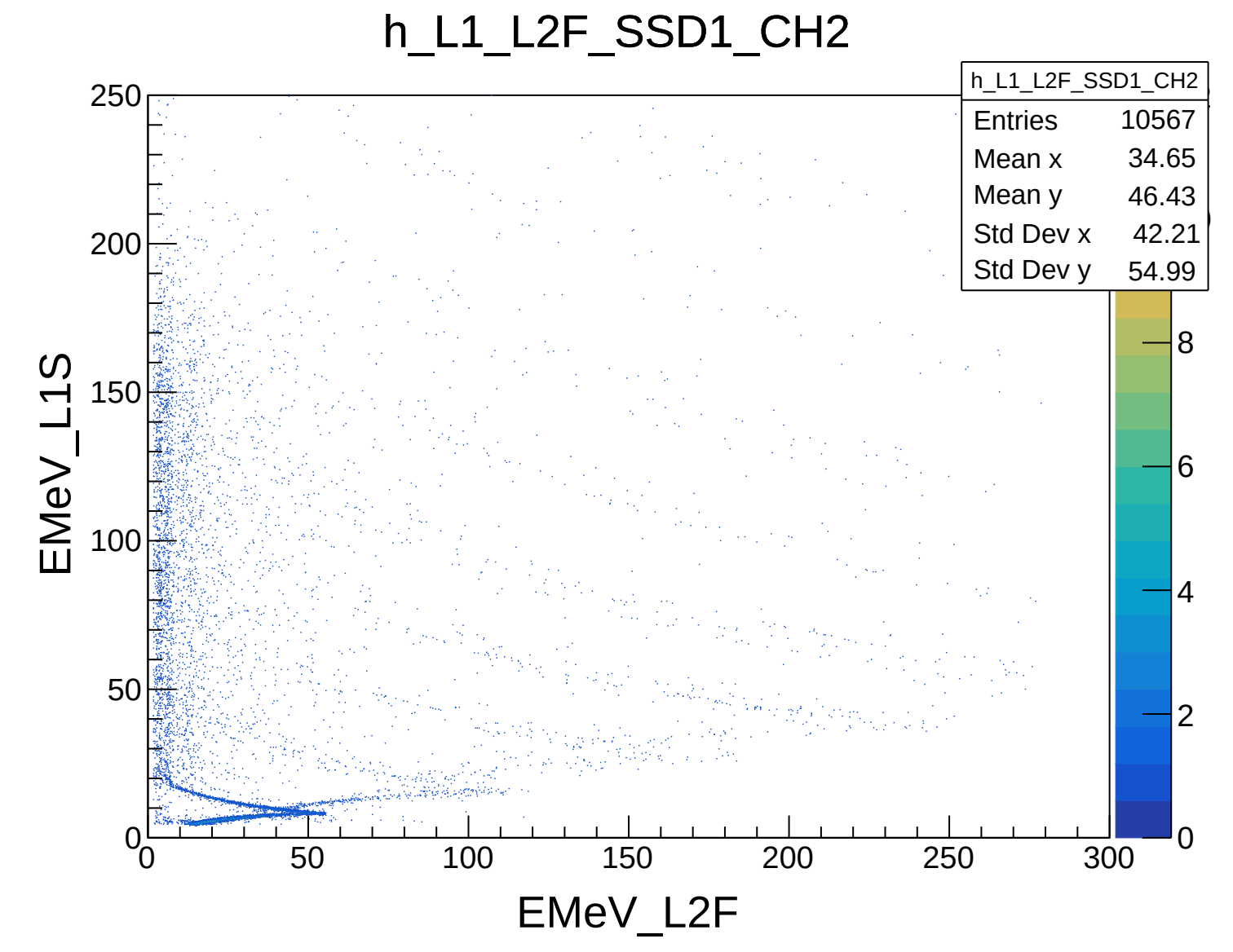
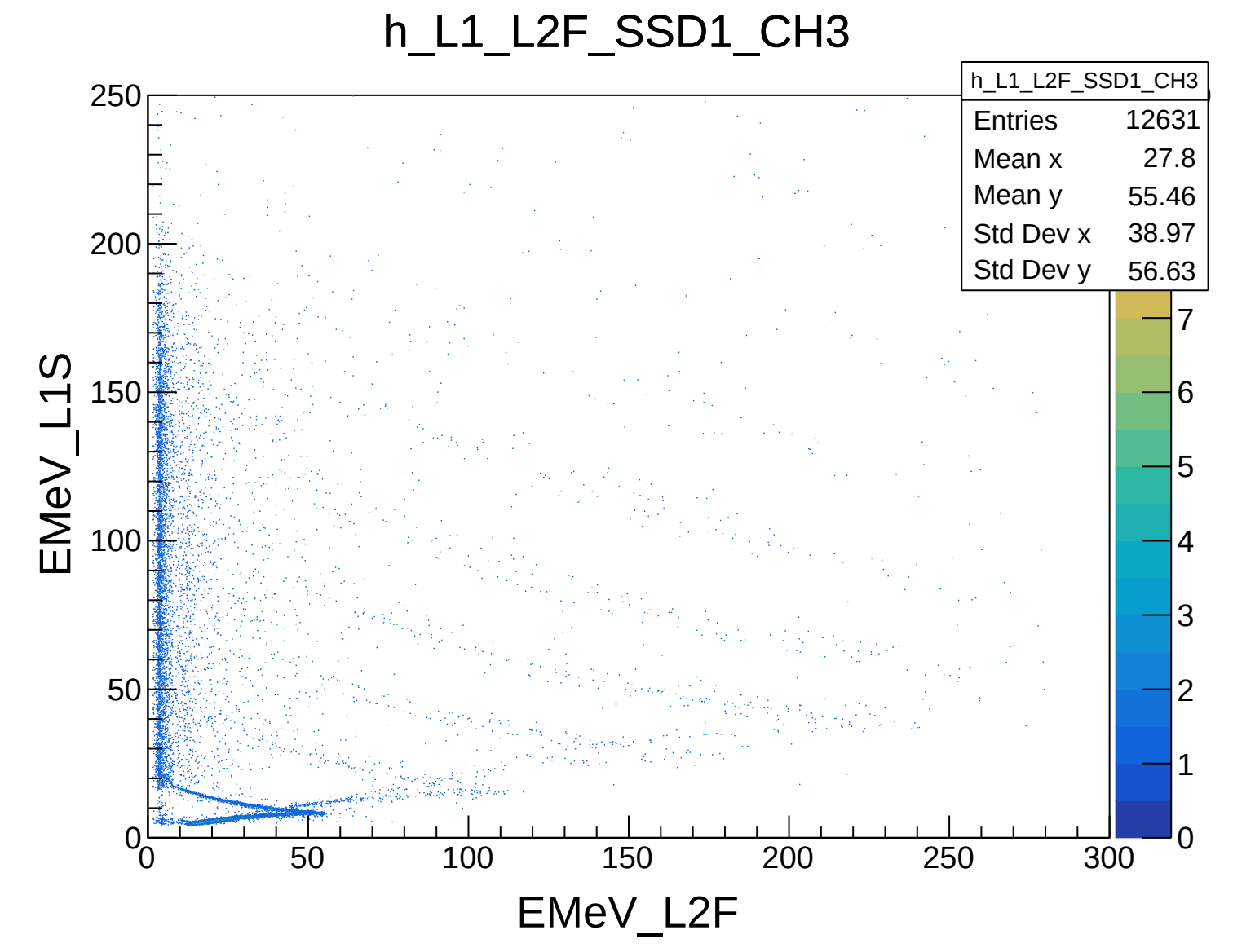
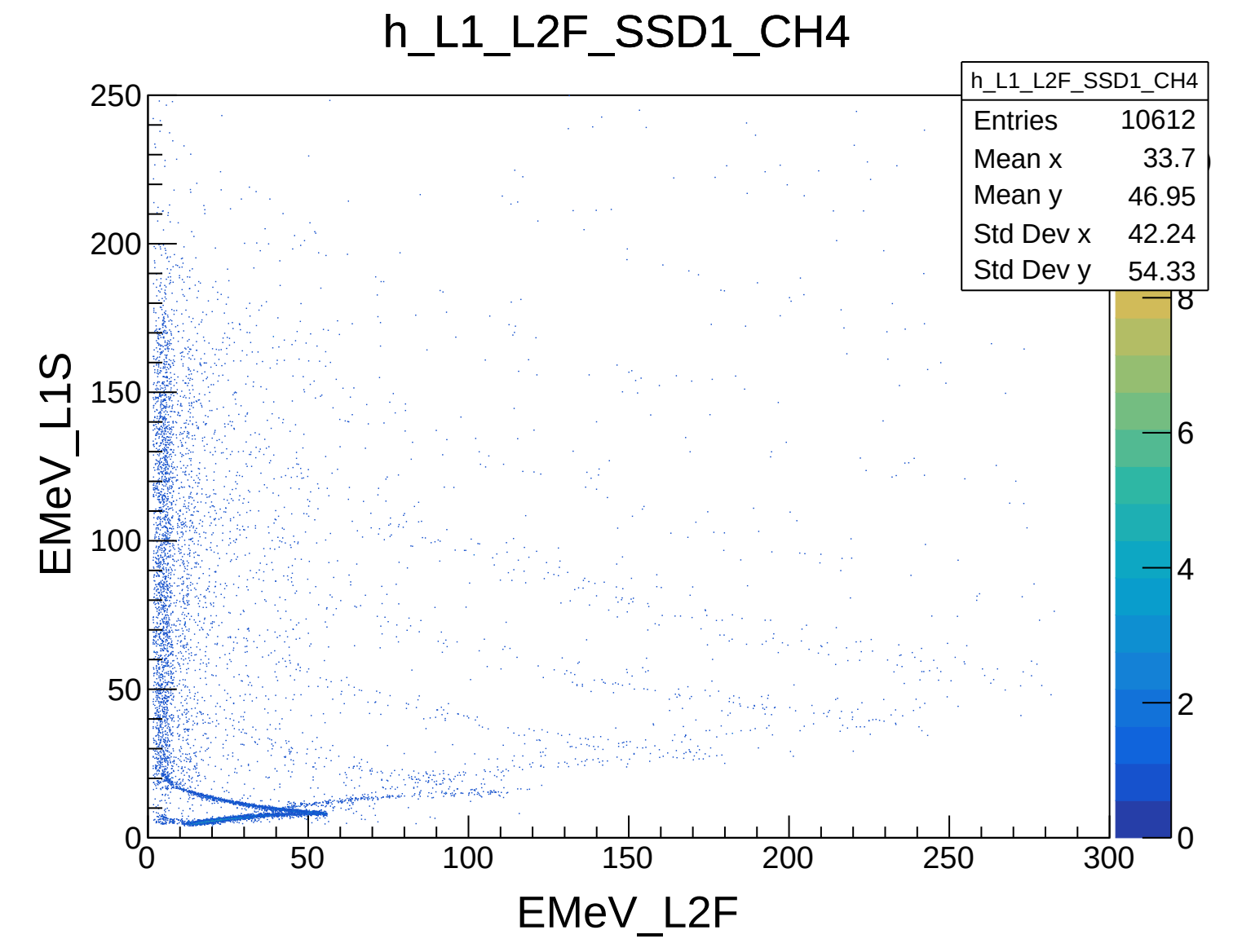
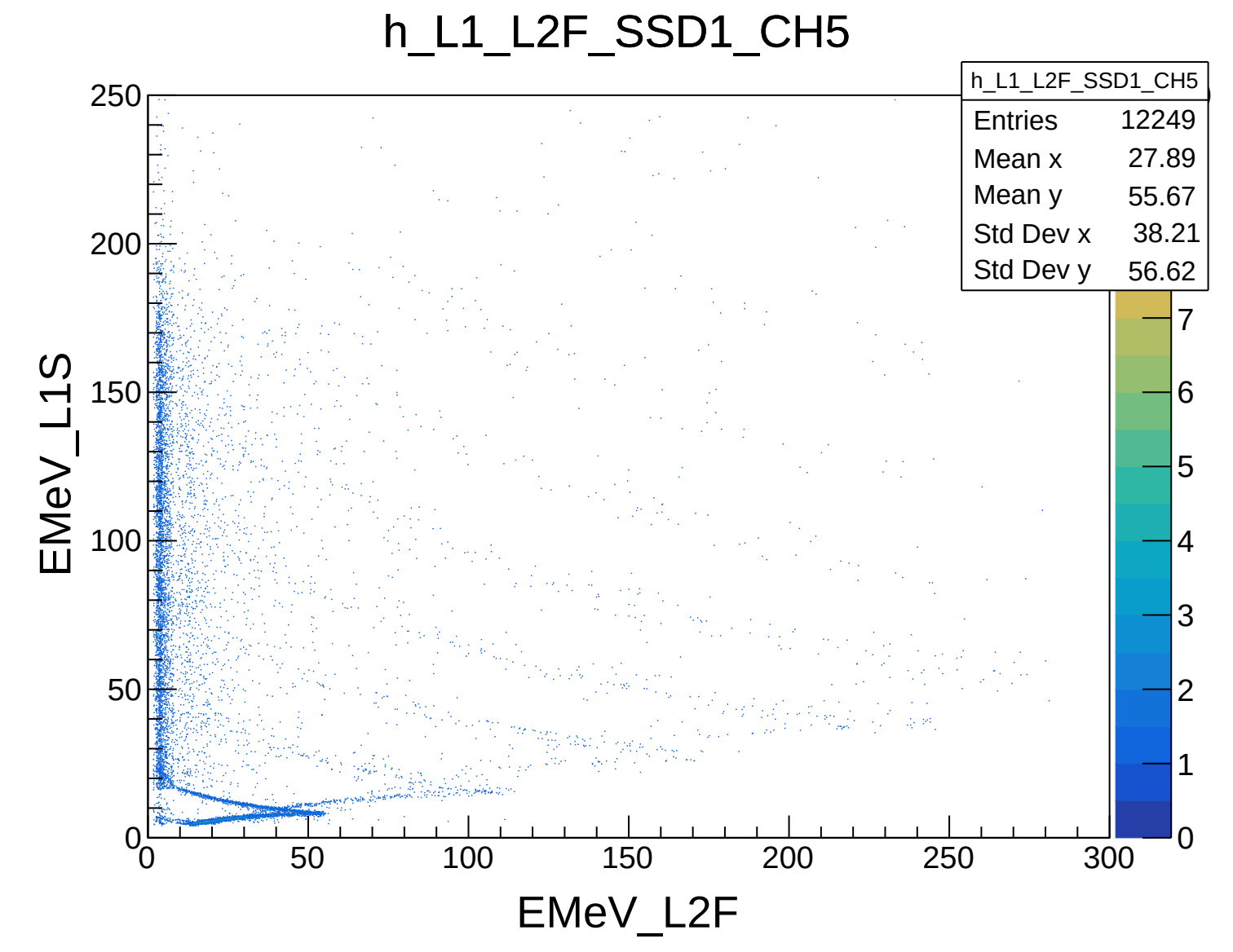

h_L1_L2F_SSD1_CH0
h_L1_L2F_SSD1_CH0
Entries 9443
Mean x 27.61
Mean y 48.45
Std Dev x 34.18
Std Dev y 54.92
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
1
2
3
4
5
6

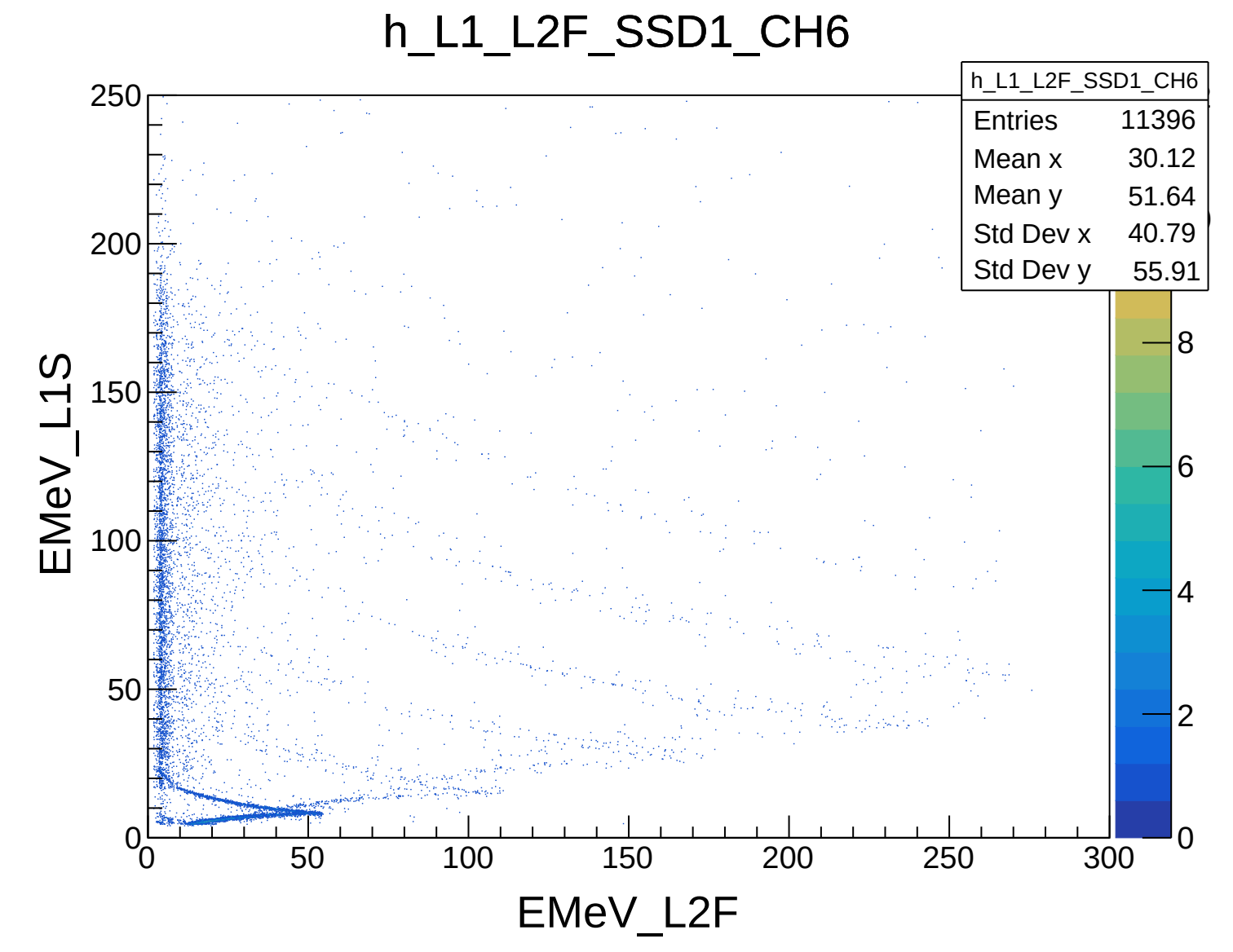

h_L1_L2F_SSD1_CH1
h_L1_L2F_SSD1_CH1
Entries 10664
Mean x 35.42
Mean y 47.99
Std Dev x 44.7
Std Dev y 55.4
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
0
2
4
6
8

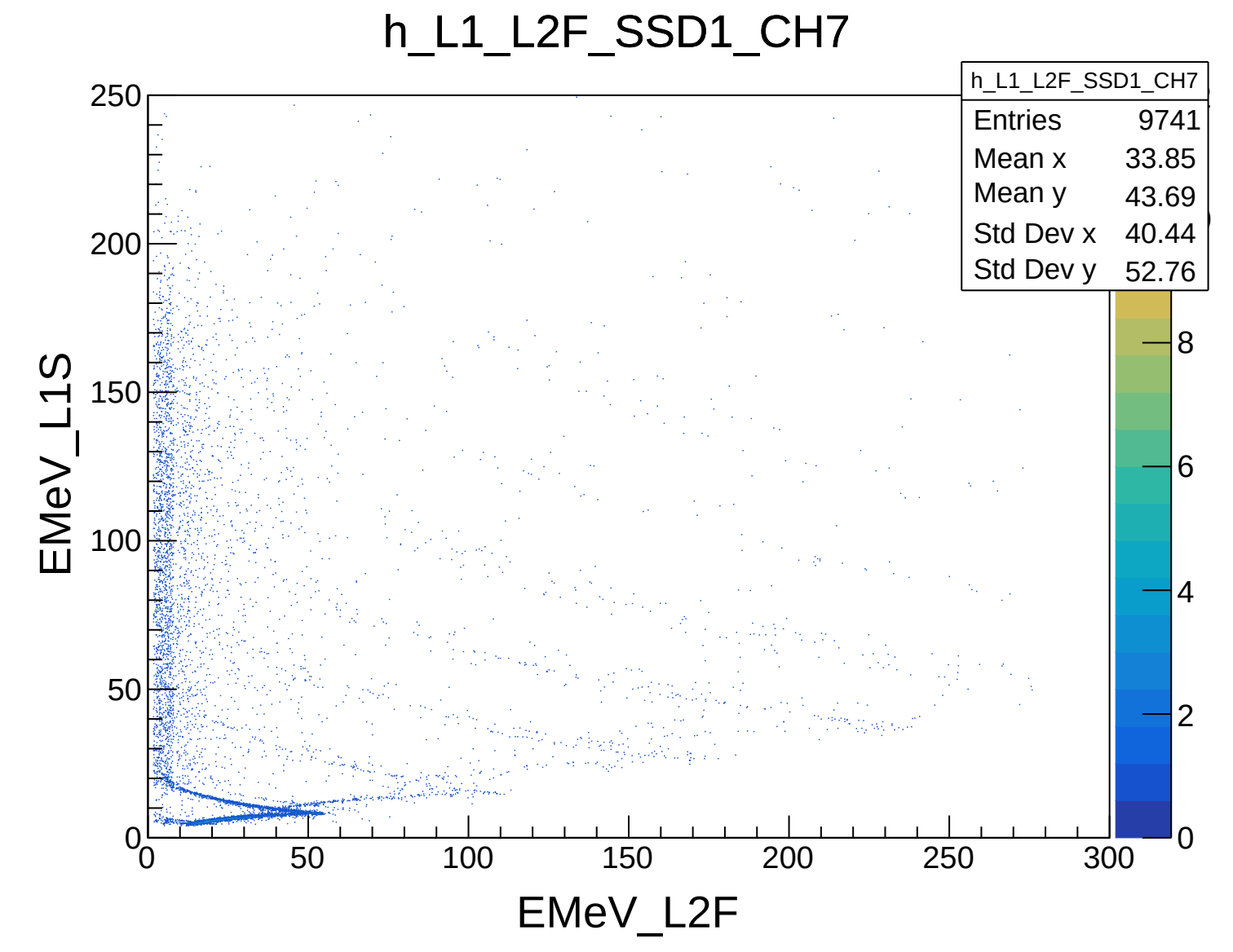

h_L1_L2F_SSD1_CH2
h_L1_L2F_SSD1_CH2
Entries 10567
Mean x 34.65
Mean y 46.43
Std Dev x 42.21
Std Dev y 54.99
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
0
2
4
6
8

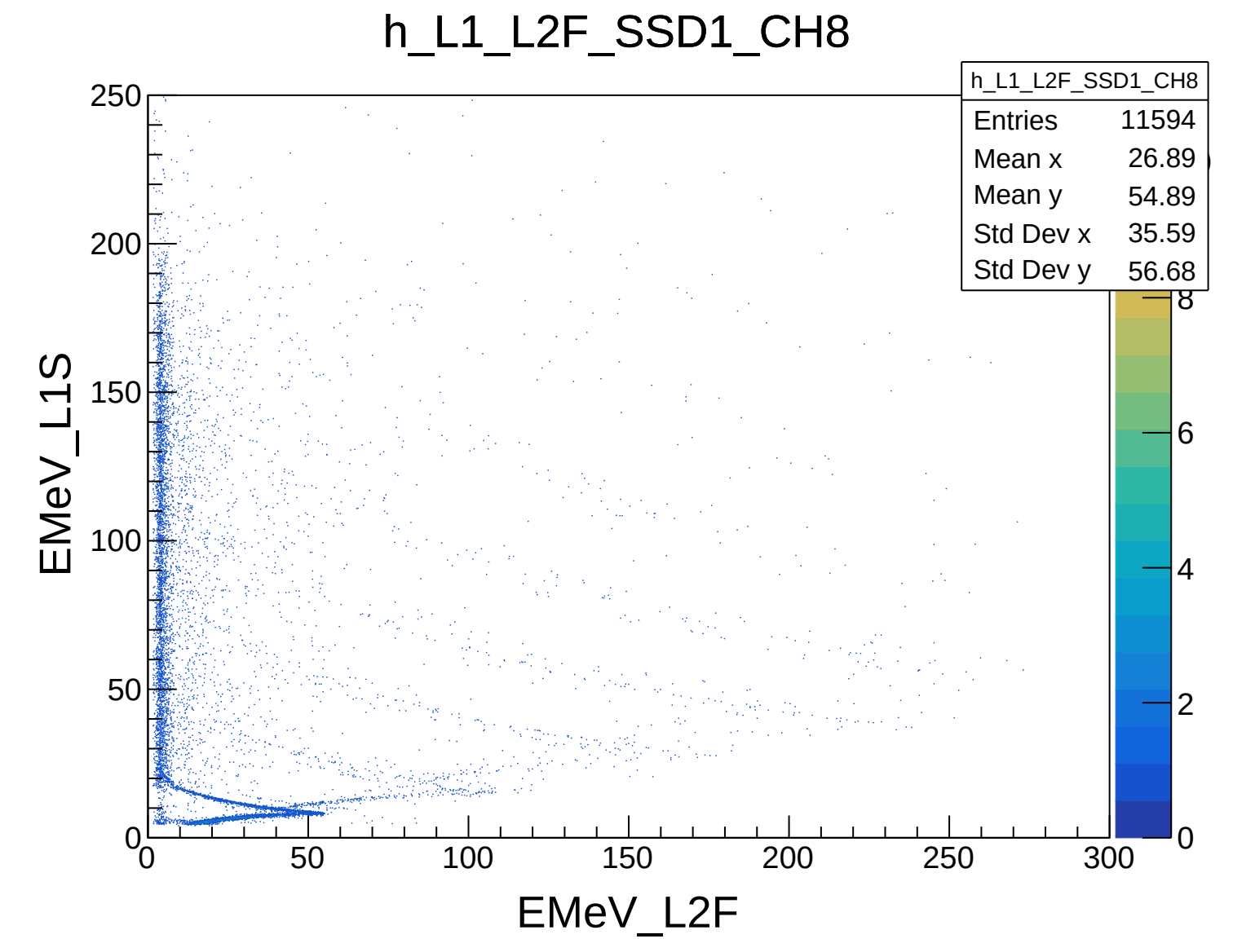

h_L1_L2F_SSD1_CH3
h_L1_L2F_SSD1_CH3
Entries 12631
Mean x 27.8
Mean y 55.46
Std Dev x 38.97
Std Dev y 56.63
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
0
1
2
3
4
5
6
7

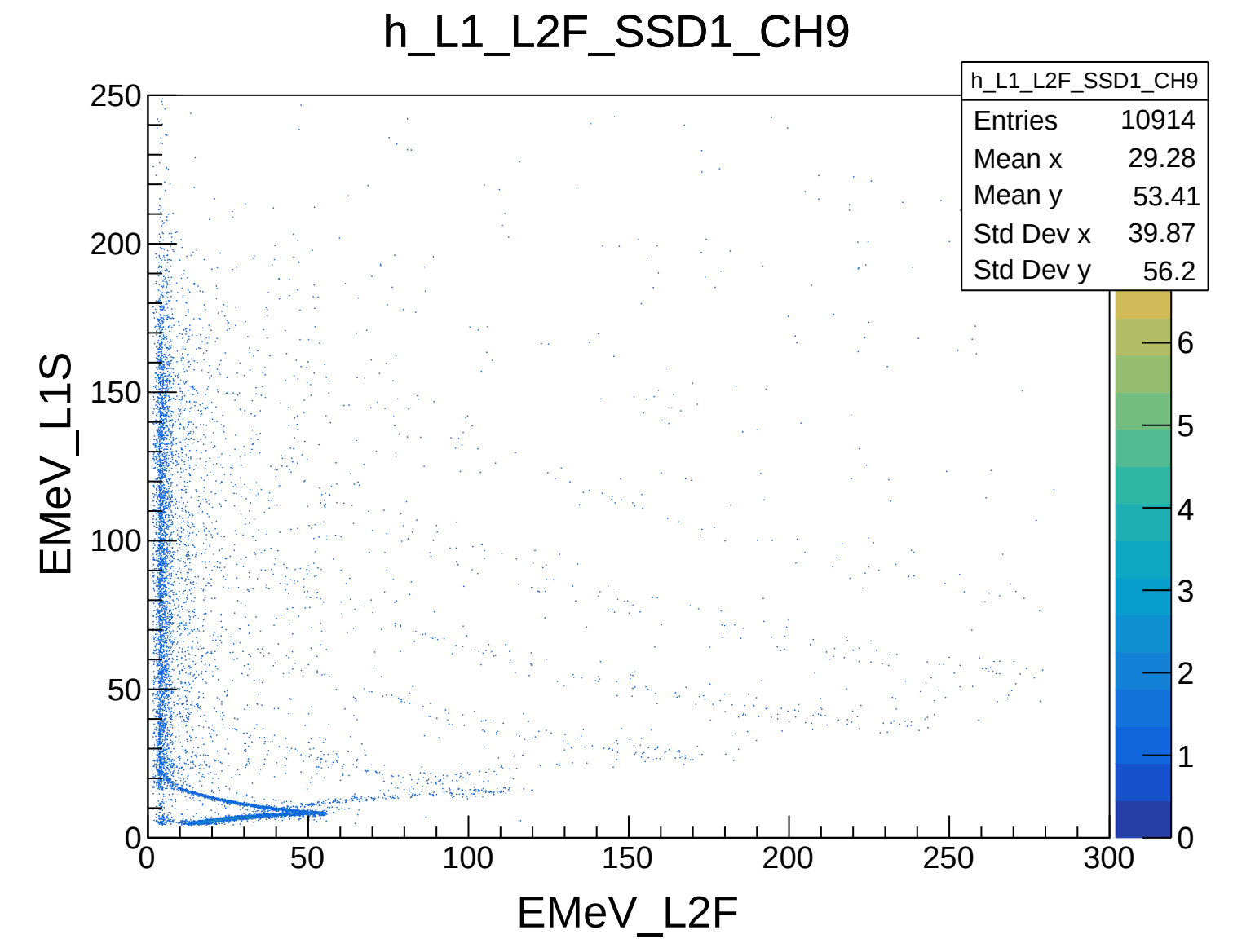

h_L1_L2F_SSD1_CH4
h_L1_L2F_SSD1_CH4
Entries 10612
Mean x 33.7
Mean y 46.95
Std Dev x 42.24
Std Dev y 54.33
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
0
2
4
6
8

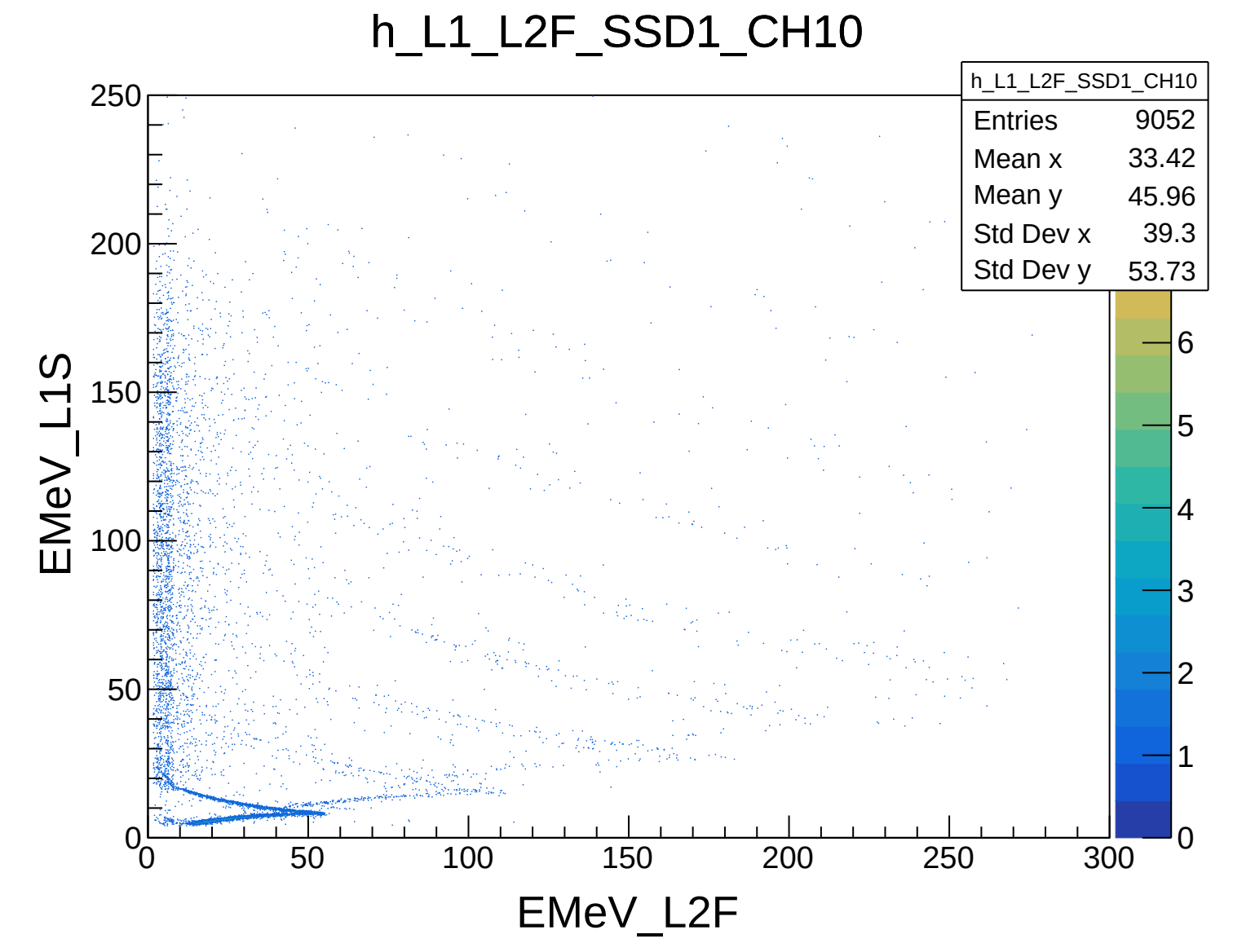

h_L1_L2F_SSD1_CH5
h_L1_L2F_SSD1_CH5
Entries 12249
Mean x 27.89
Mean y 55.67
Std Dev x 38.21
Std Dev y 56.62
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
0
1
2
3
4
5
6
7

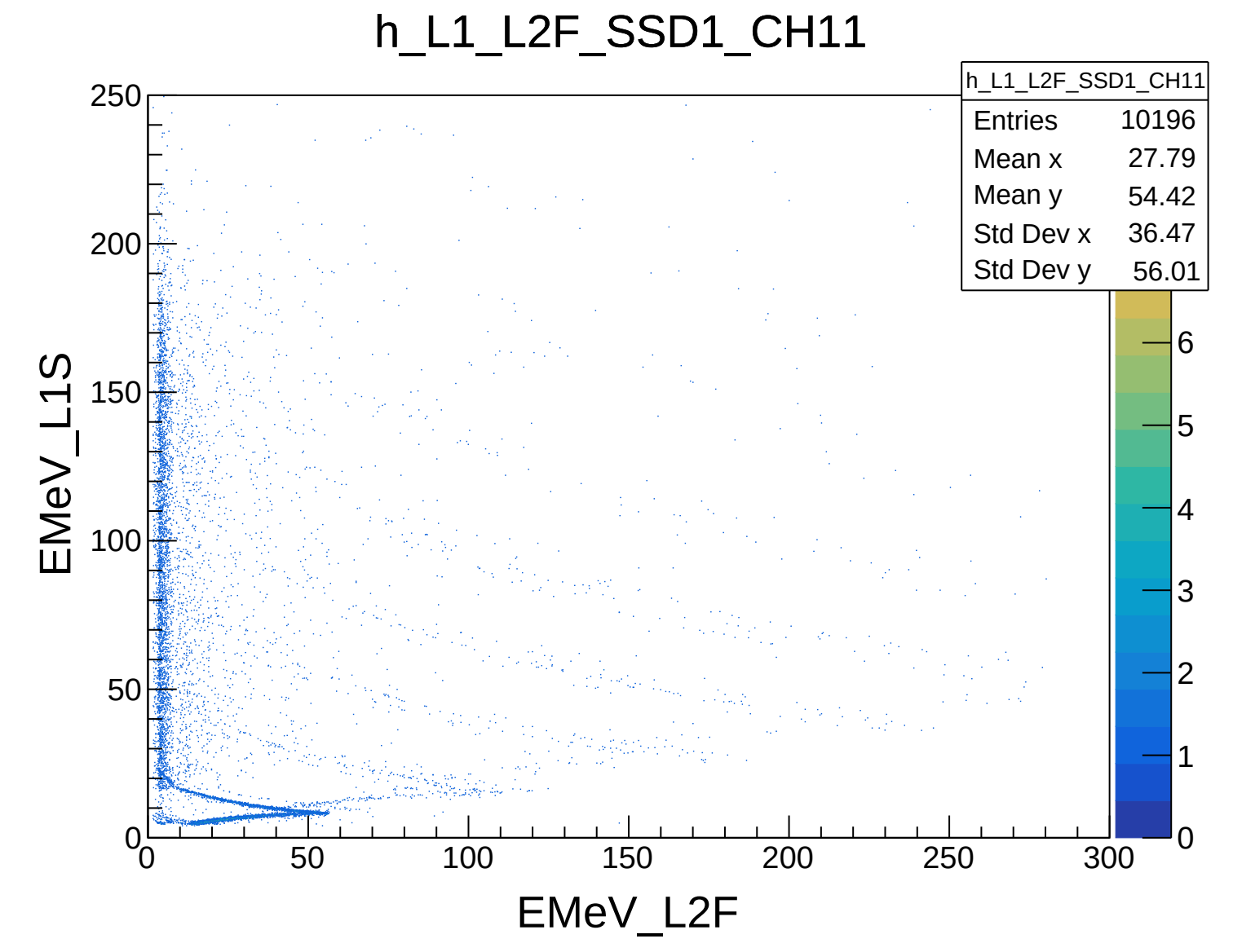

h_L1_L2F_SSD1_CH6
h_L1_L2F_SSD1_CH6
Entries 11396
Mean x 30.12
Mean y 51.64
Std Dev x 40.79
Std Dev y 55.91
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
0
2
4
6
8

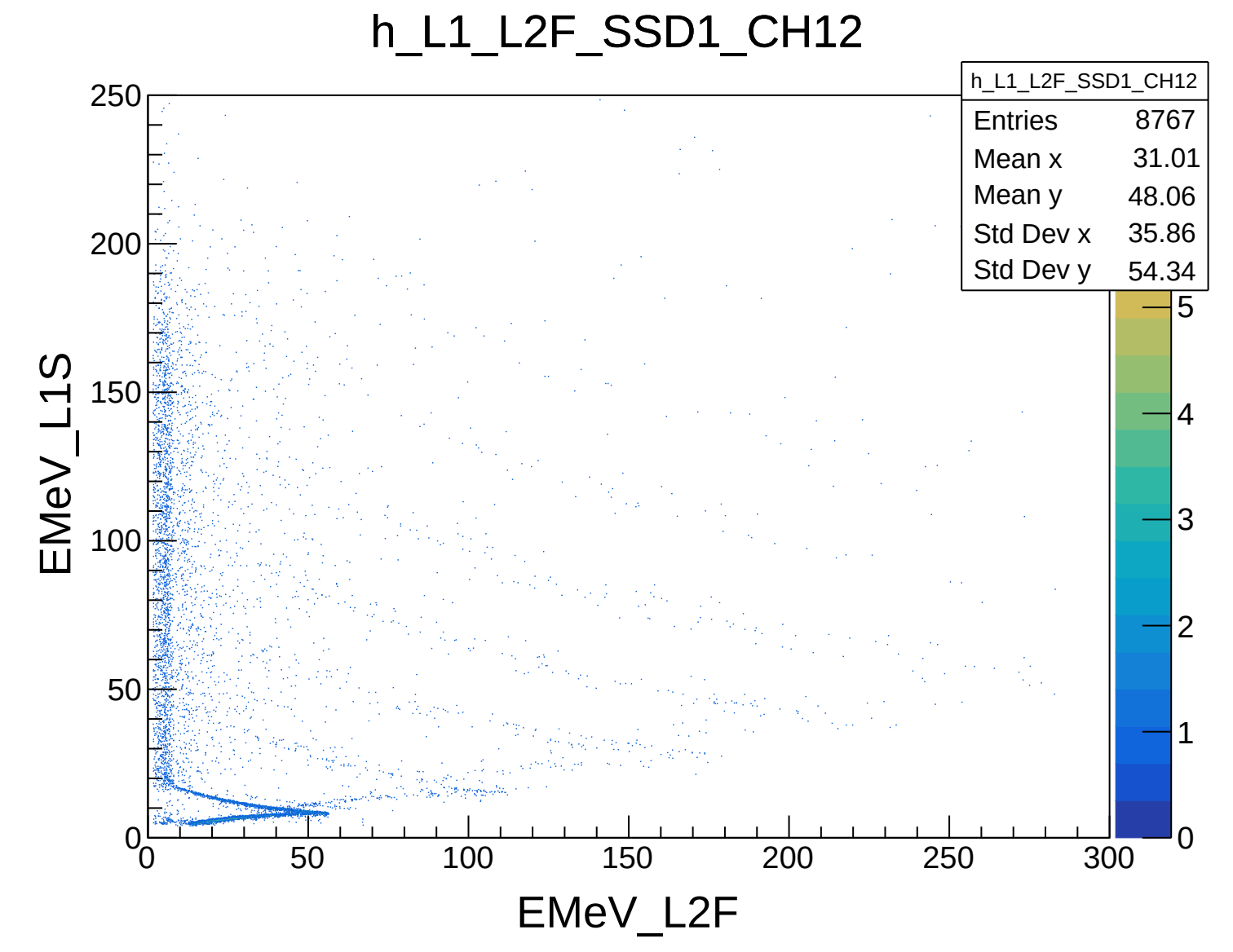

h_L1_L2F_SSD1_CH7
h_L1_L2F_SSD1_CH7
Entries 9741
Mean x 33.85
Mean y 43.69
Std Dev x 40.44
Std Dev y 52.76
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
0
2
4
6
8

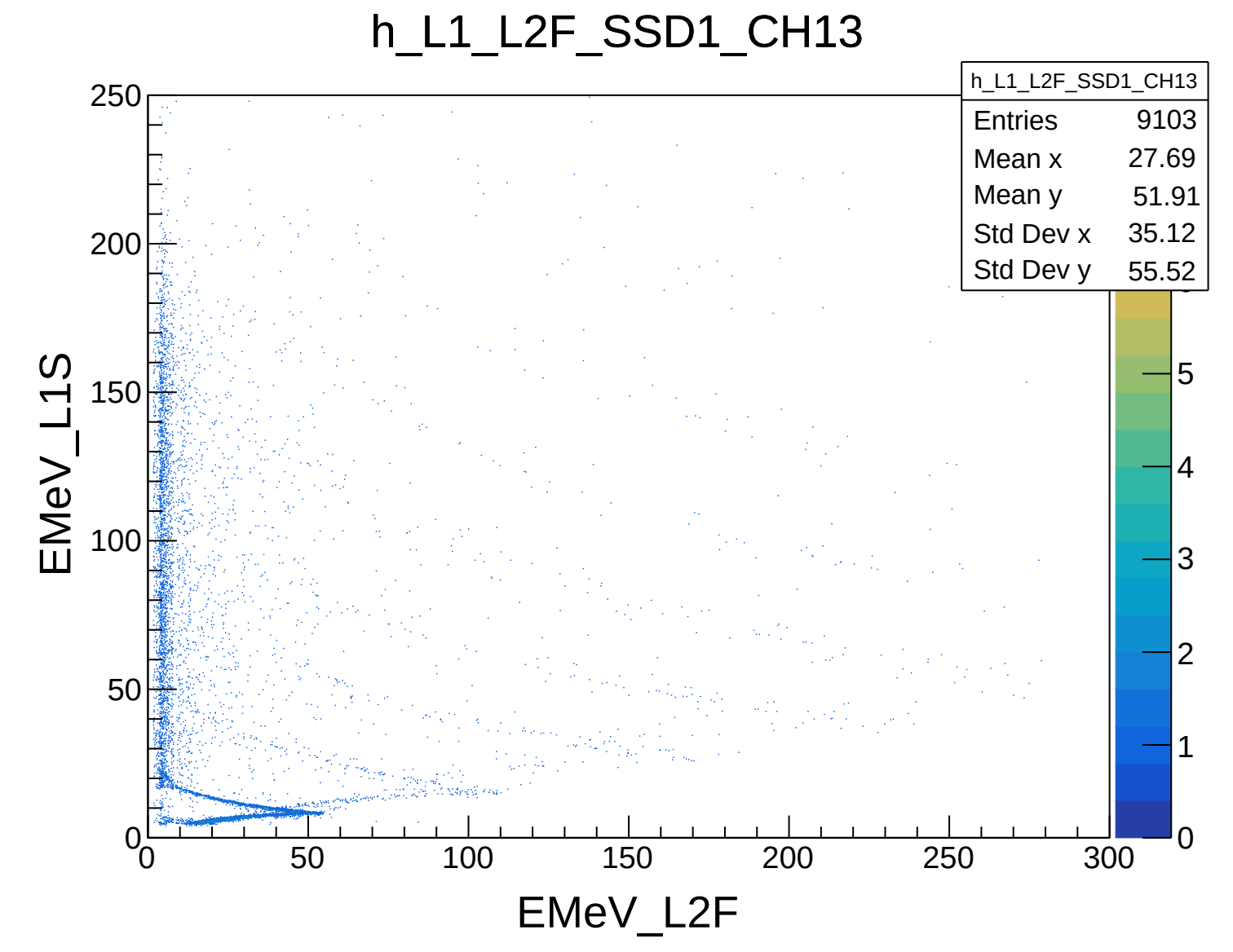

h_L1_L2F_SSD1_CH8
h_L1_L2F_SSD1_CH8
Entries 11594
Mean x 26.89
Mean y 54.89
Std Dev x 35.59
Std Dev y 56.68
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
0
2
4
6
8

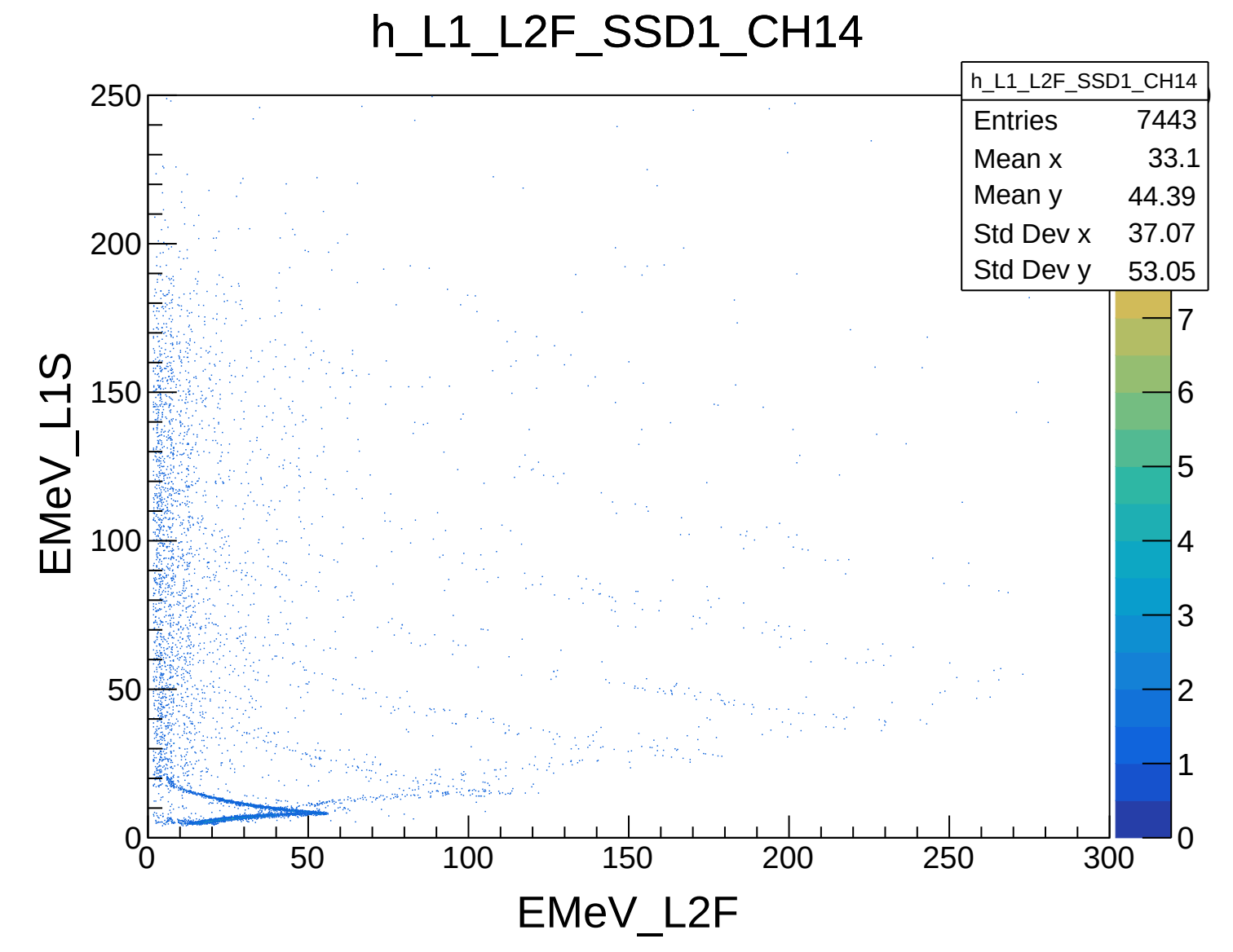

h_L1_L2F_SSD1_CH9
h_L1_L2F_SSD1_CH9
Entries 10914
Mean x 29.28
Mean y 53.41
Std Dev x 39.87
Std Dev y 56.2
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
0
1
2
3
4
5
6

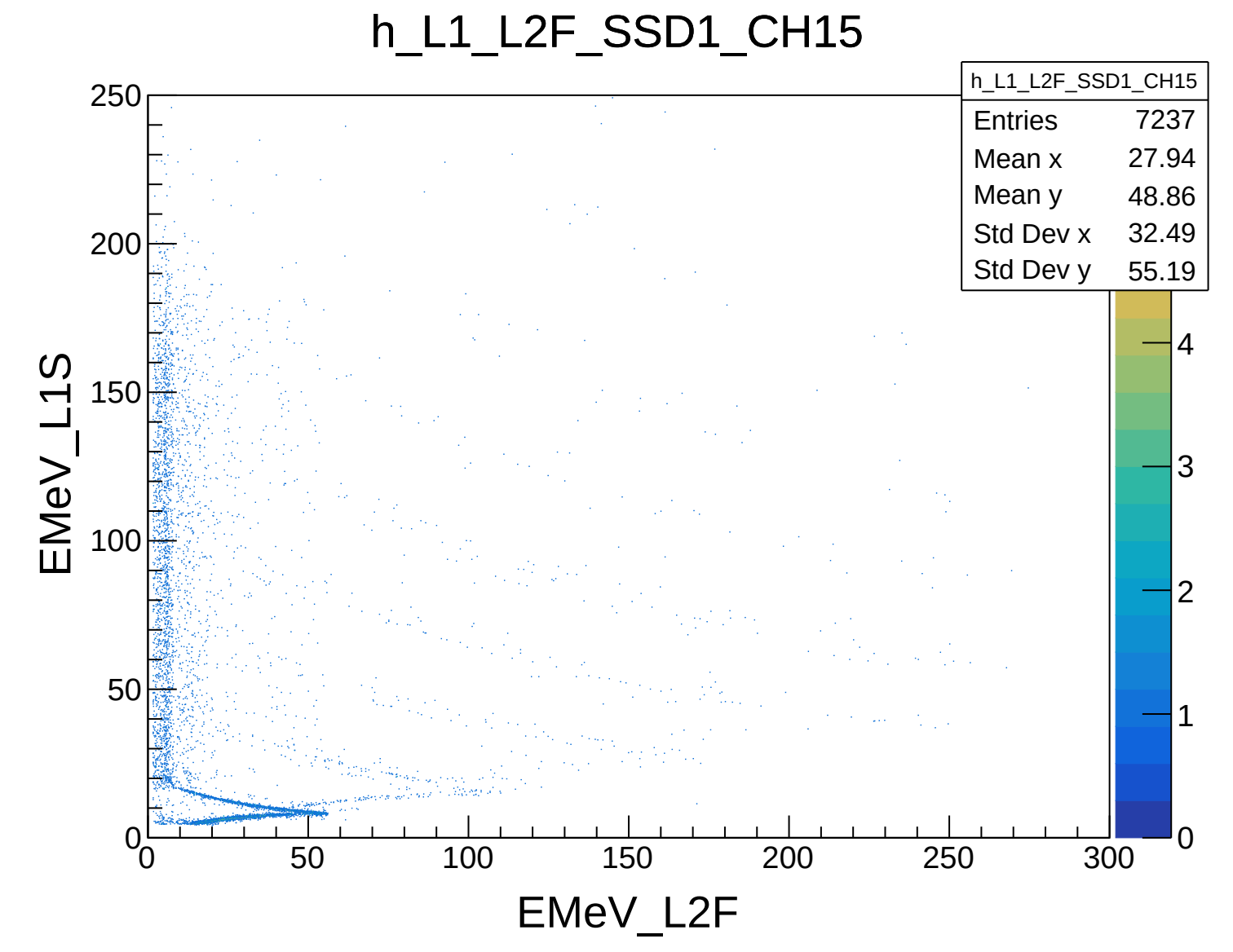

h_L1_L2F_SSD1_CH10
h_L1_L2F_SSD1_CH10
Entries 9052
Mean x 33.42
Mean y 45.96
Std Dev x 39.3
Std Dev y 53.73
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
0
1
2
3
4
5
6

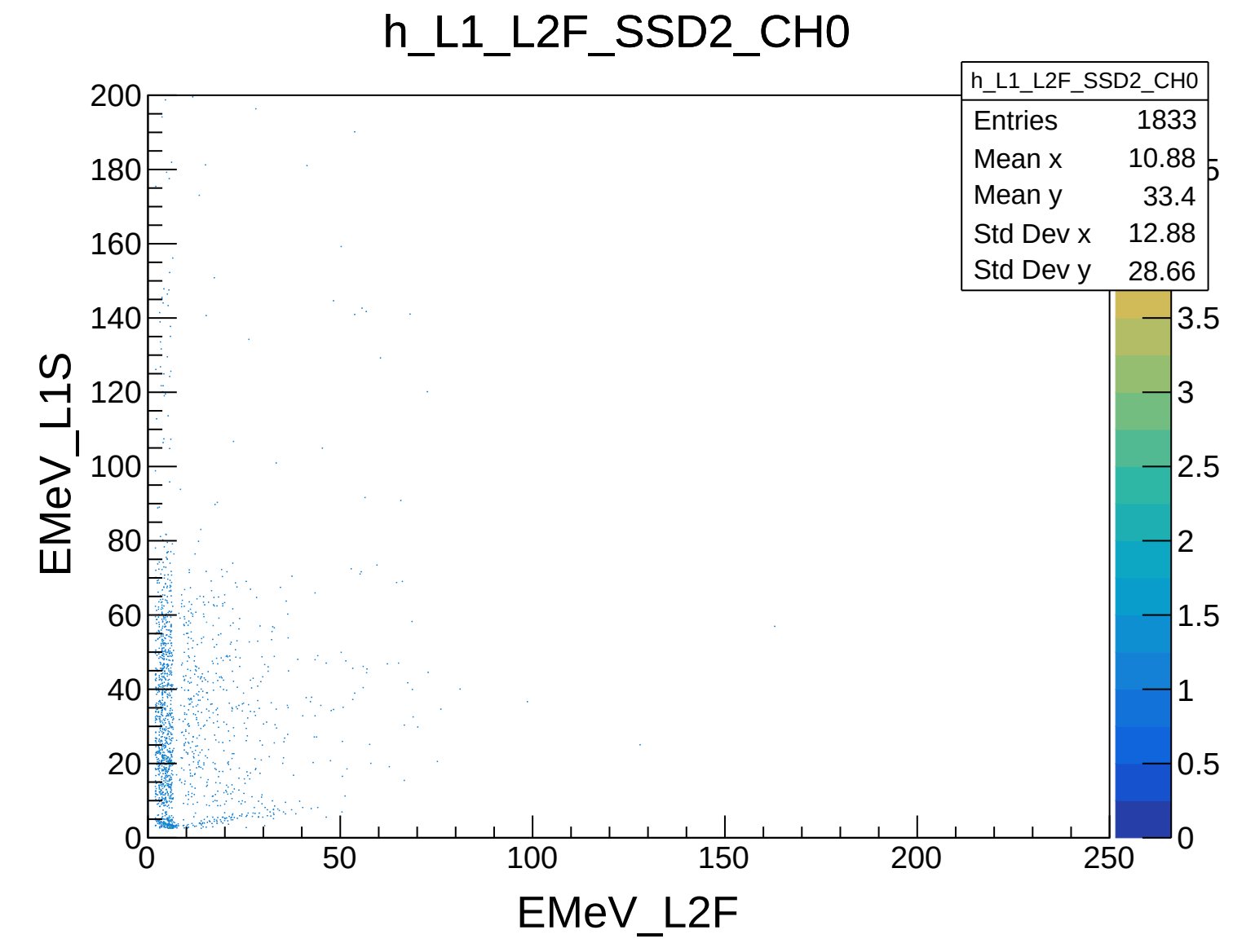

h_L1_L2F_SSD1_CH11
h_L1_L2F_SSD1_CH11
Entries 10196
Mean x 27.79
Mean y 54.42
Std Dev x 36.47
Std Dev y 56.01
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
1
2
3
4
5
6

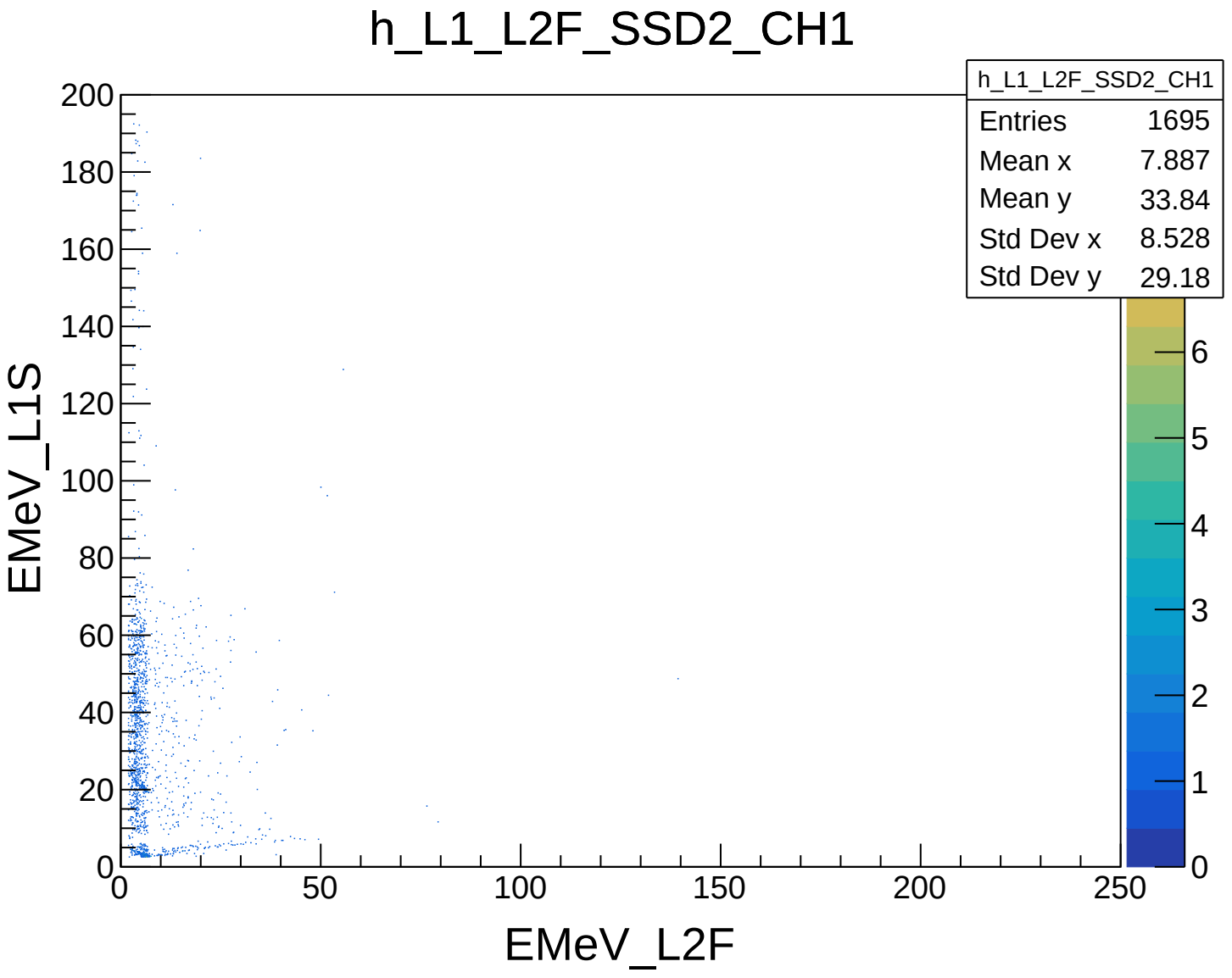

h_L1_L2F_SSD1_CH12
h_L1_L2F_SSD1_CH12
Entries 8767
Mean x 31.01
Mean y 48.06
Std Dev x 35.86
Std Dev y 54.34
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
0
1
2
3
4
5

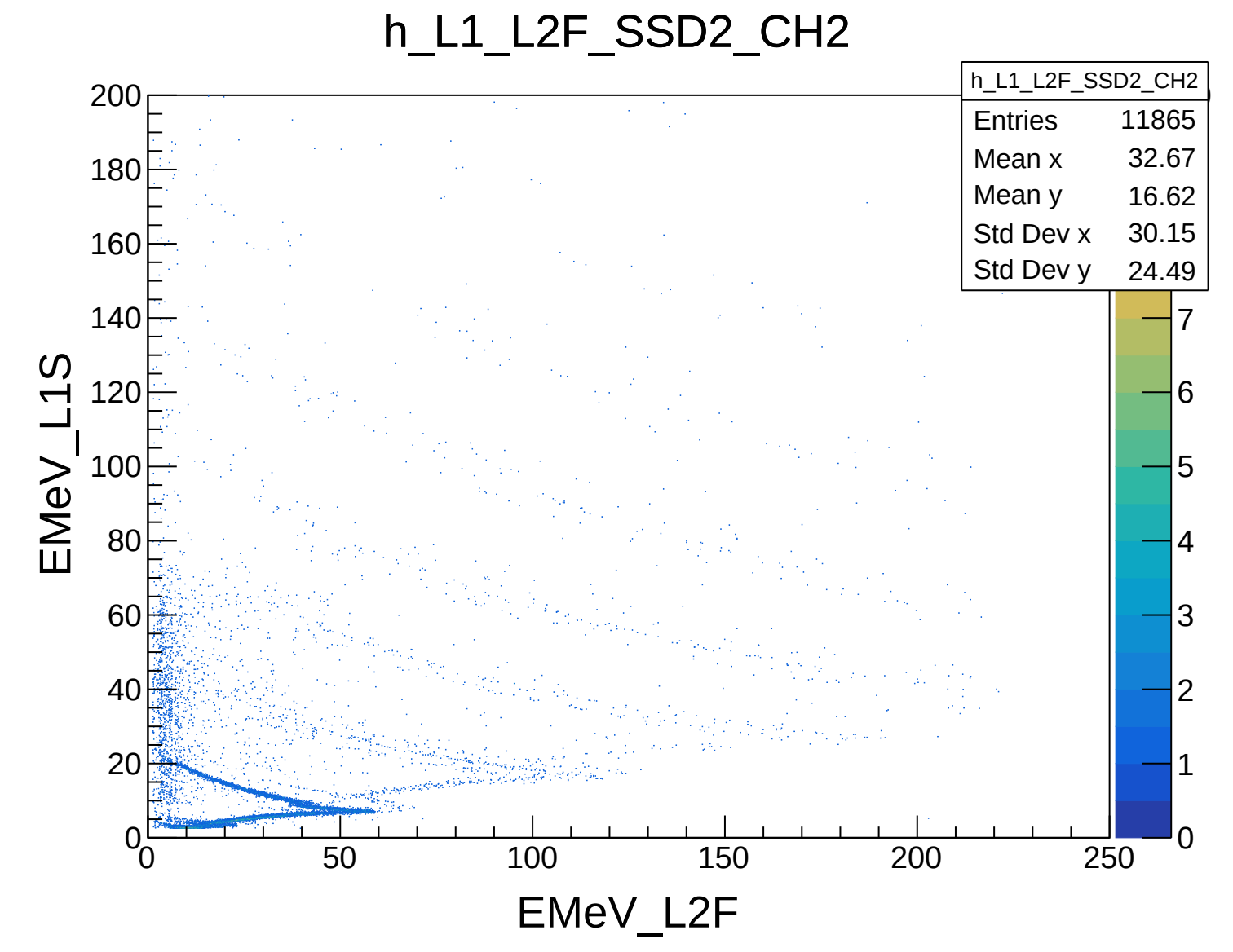

h_L1_L2F_SSD1_CH13
h_L1_L2F_SSD1_CH13
Entries 9103
Mean x 27.69
Mean y 51.91
Std Dev x 35.12
Std Dev y 55.52
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
1
2
3
4
5

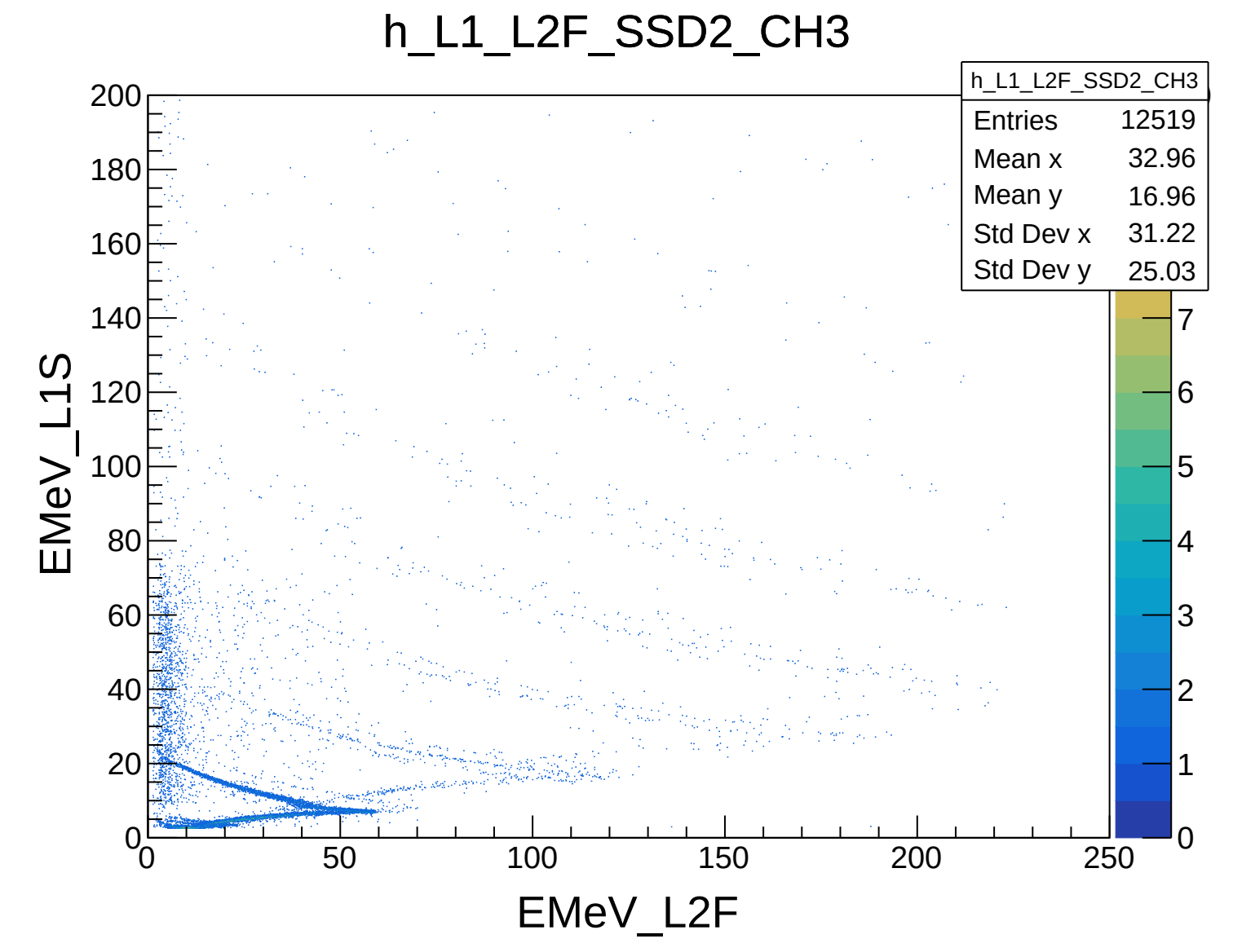

h_L1_L2F_SSD1_CH14
h_L1_L2F_SSD1_CH14
Entries 7443
Mean x 33.1
Mean y 44.39
Std Dev x 37.07
Std Dev y 53.05
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
0
1
2
3
4
5
6
7

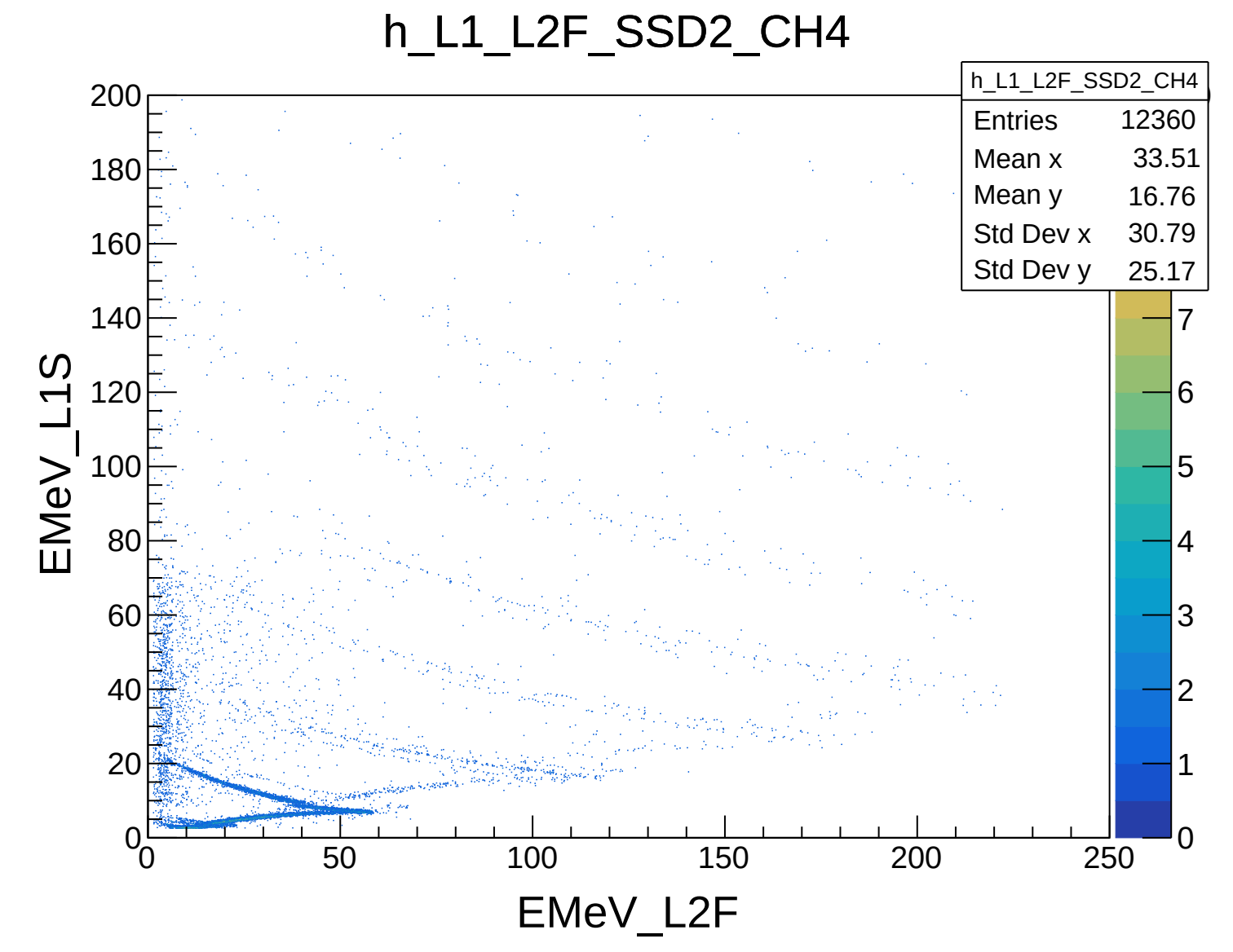

h_L1_L2F_SSD1_CH15
h_L1_L2F_SSD1_CH15
Entries 7237
Mean x 27.94
Mean y 48.86
Std Dev x 32.49
Std Dev y 55.19
EMeV_L1S
EMeV_L2F
0
50
100
150
200
250
300
0
1
2
3
4

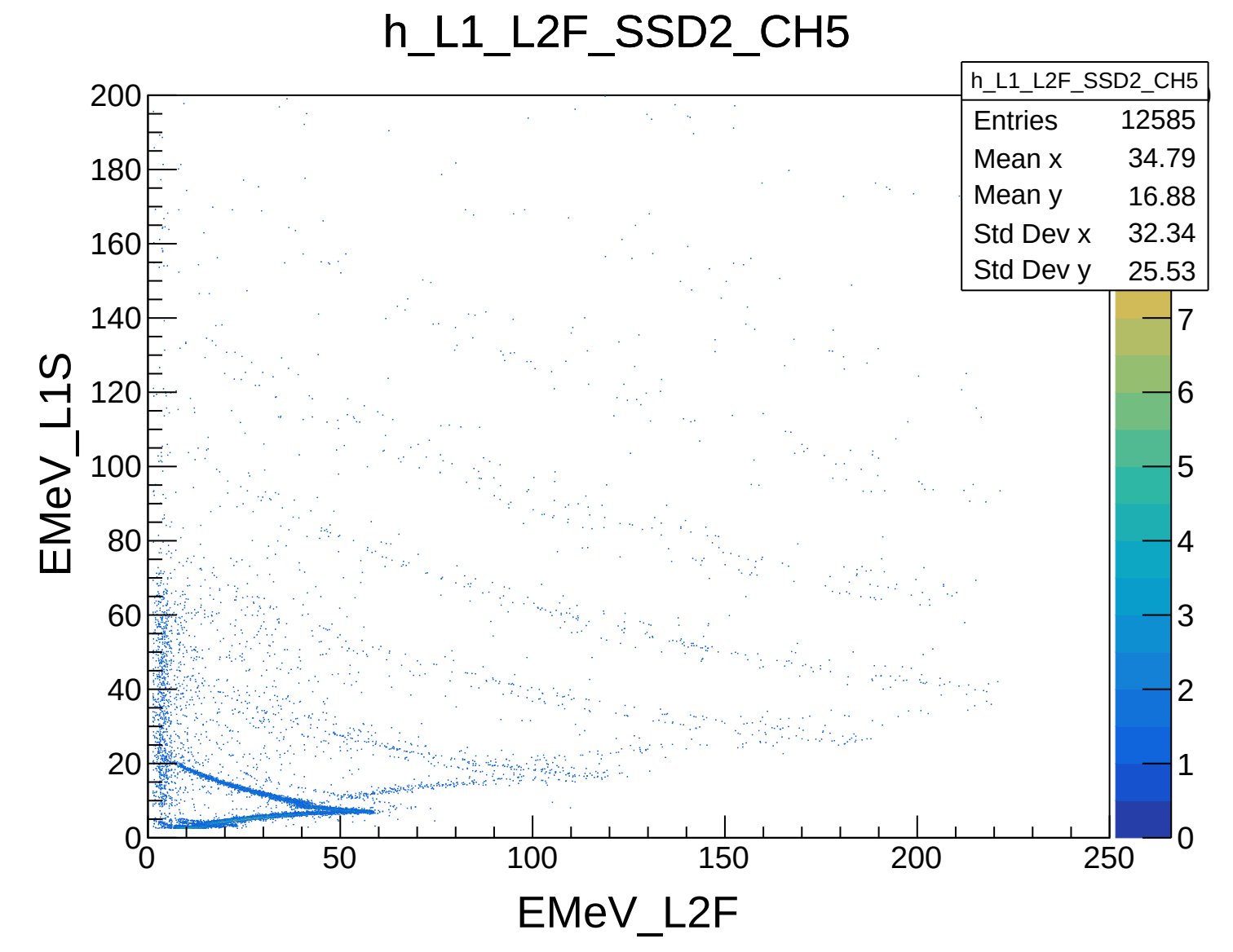

h_L1_L2F_SSD2_CH0
h_L1_L2F_SSD2_CH0
Entries 1833
Mean x 10.88
Mean y 33.4
Std Dev x 12.88
Std Dev y 28.66
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
0.5
1
1.5
2
2.5
3
3.5

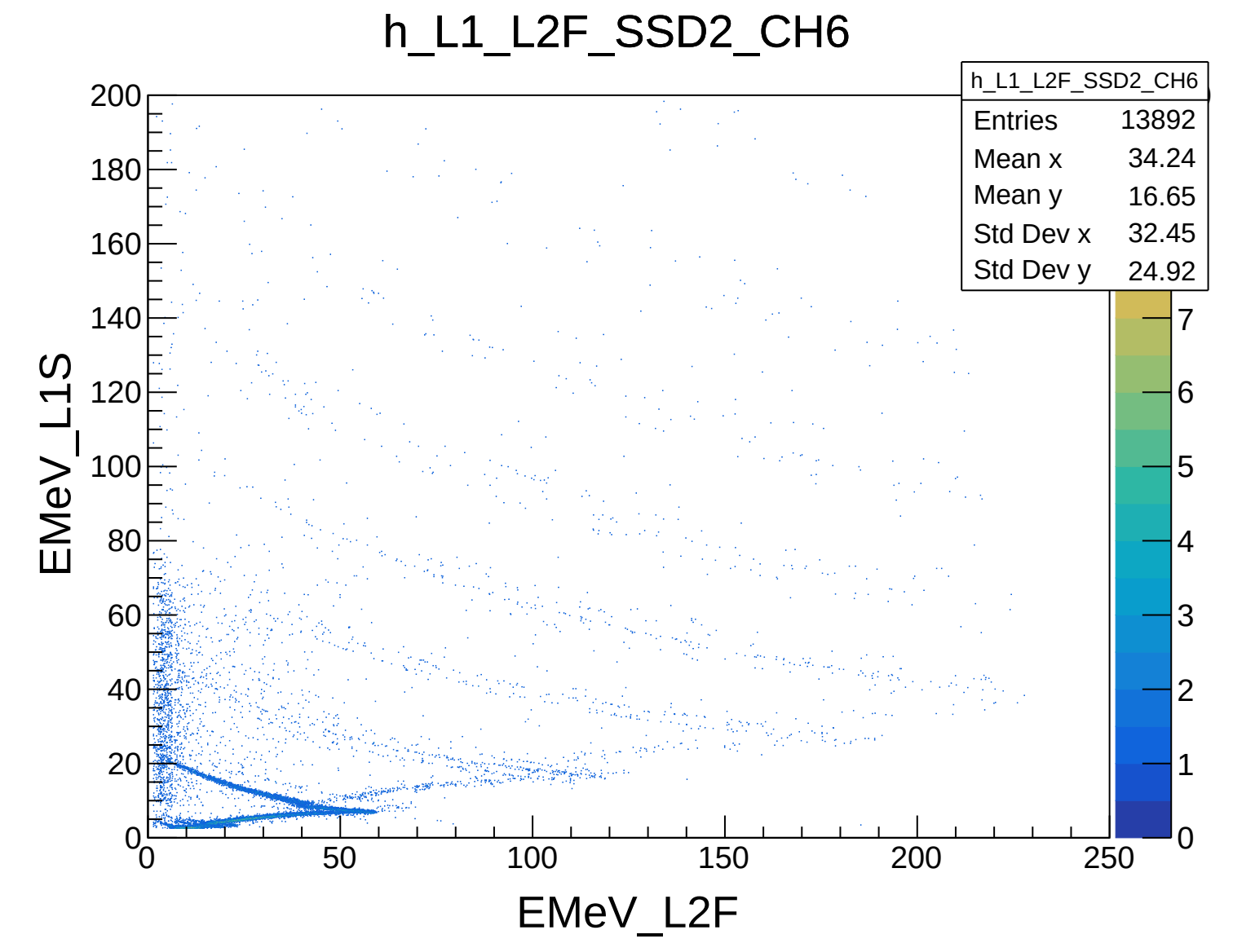

h_L1_L2F_SSD2_CH1
h_L1_L2F_SSD2_CH1
Entries 1695
Mean x 7.887
Mean y 33.84
Std Dev x 8.528
Std Dev y 29.18
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
1
2
3
4
5
6

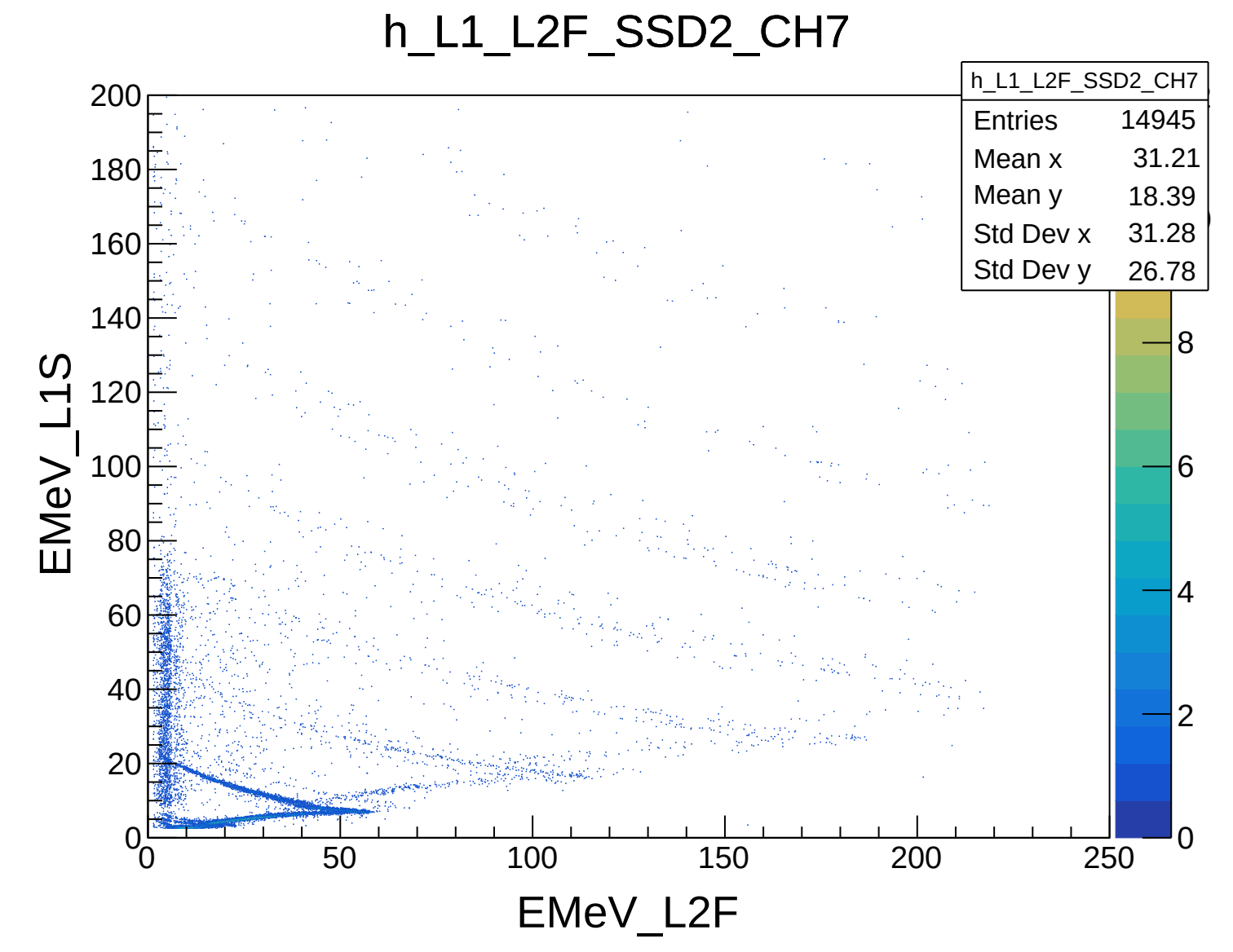

h_L1_L2F_SSD2_CH2
h_L1_L2F_SSD2_CH2
Entries 11865
Mean x 32.67
Mean y 16.62
Std Dev x 30.15
Std Dev y 24.49
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
1
2
3
4
5
6
7

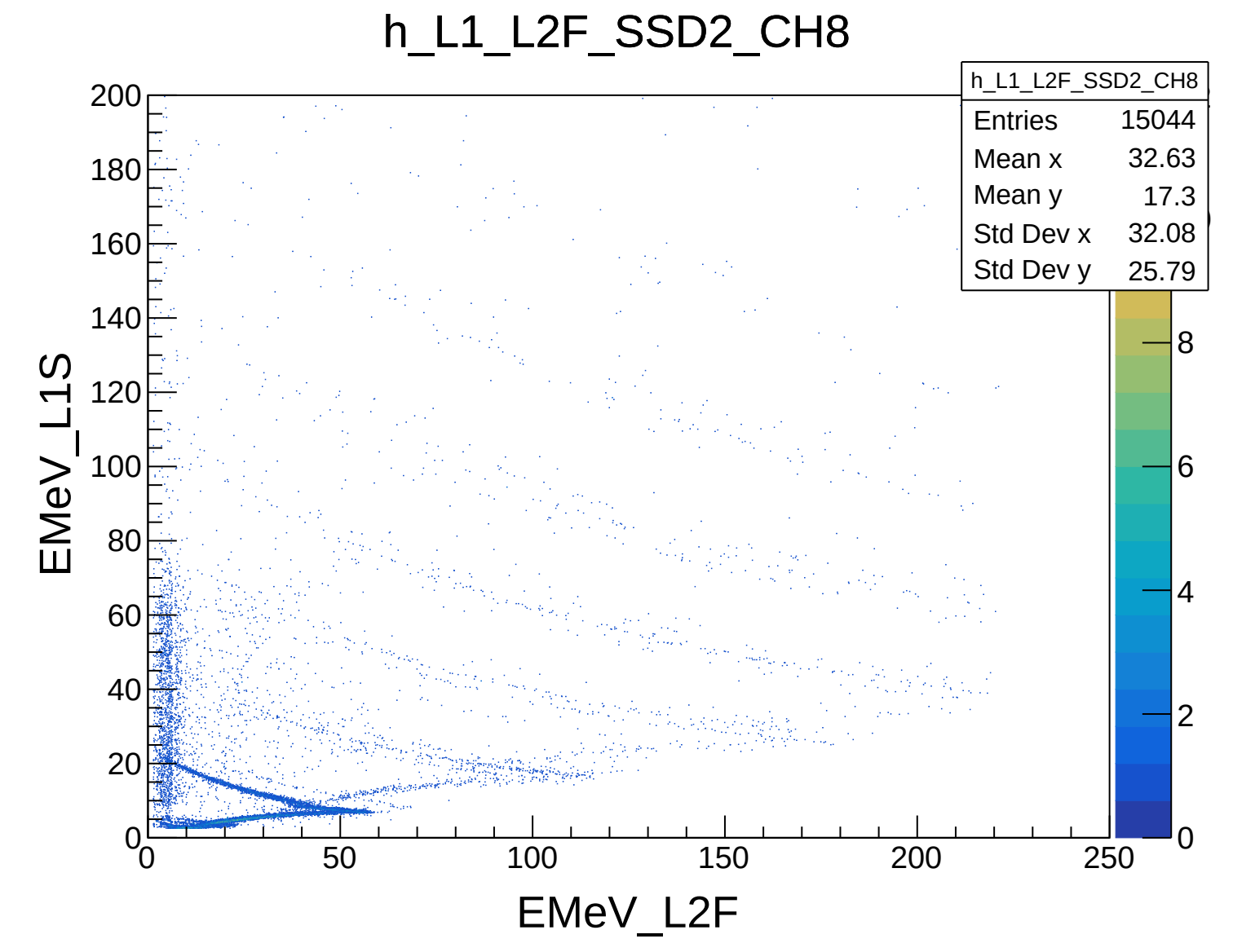

h_L1_L2F_SSD2_CH3
h_L1_L2F_SSD2_CH3
Entries 12519
Mean x 32.96
Mean y 16.96
Std Dev x 31.22
Std Dev y 25.03
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
1
2
3
4
5
6
7

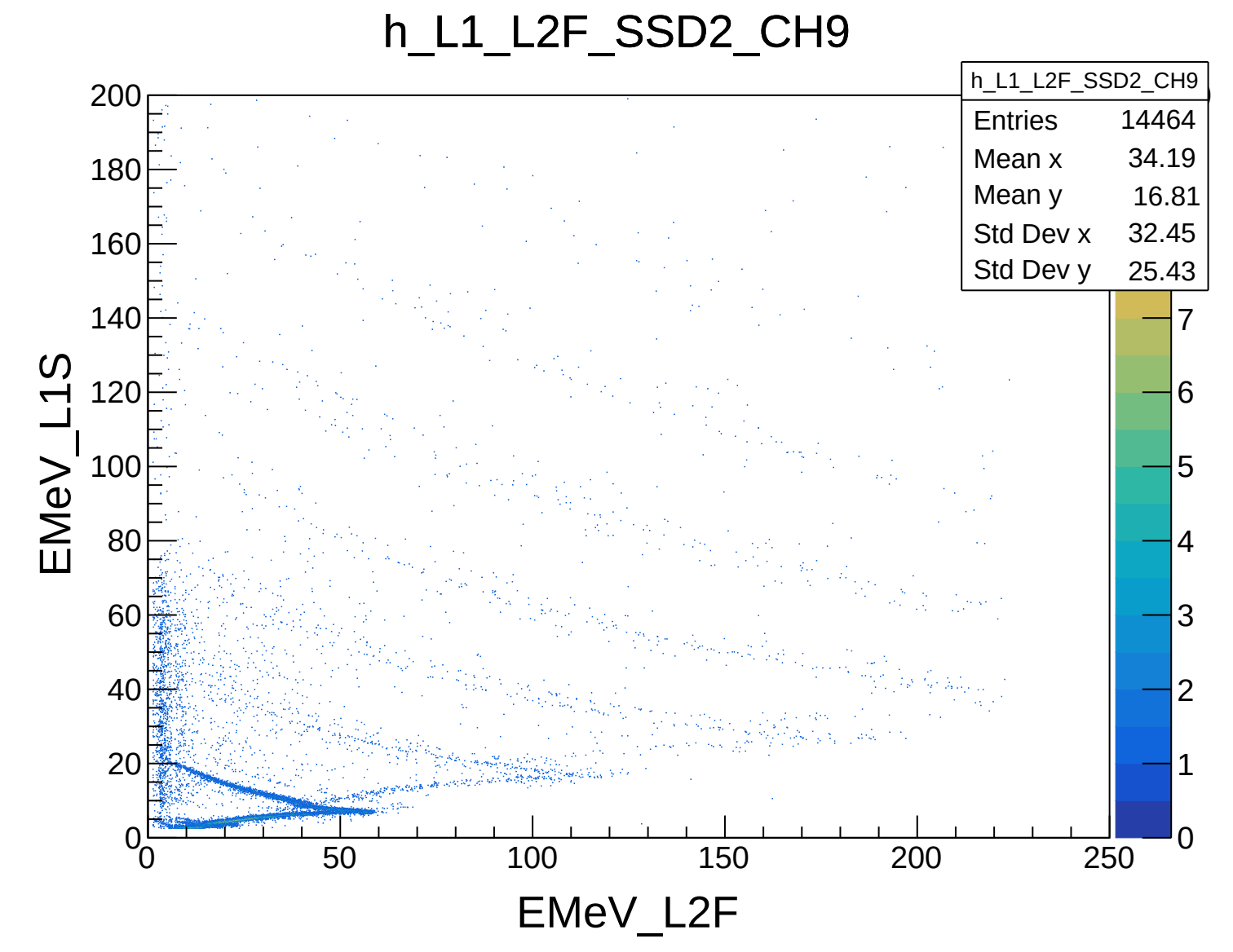

h_L1_L2F_SSD2_CH4
h_L1_L2F_SSD2_CH4
Entries 12360
Mean x 33.51
Mean y 16.76
Std Dev x 30.79
Std Dev y 25.17
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
1
2
3
4
5
6
7

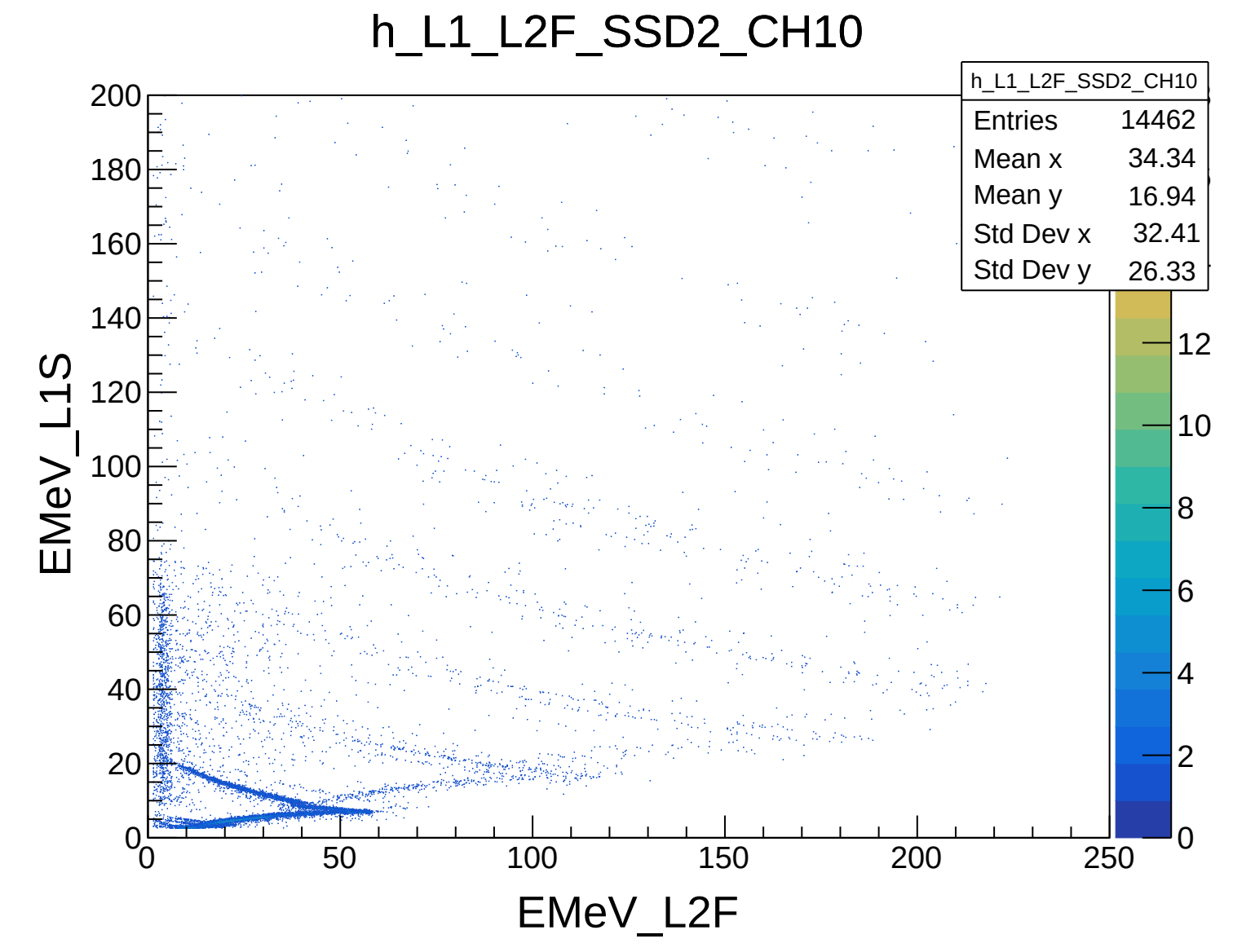

h_L1_L2F_SSD2_CH5
h_L1_L2F_SSD2_CH5
Entries 12585
Mean x 34.79
Mean y 16.88
Std Dev x 32.34
Std Dev y 25.53
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
1
2
3
4
5
6
7

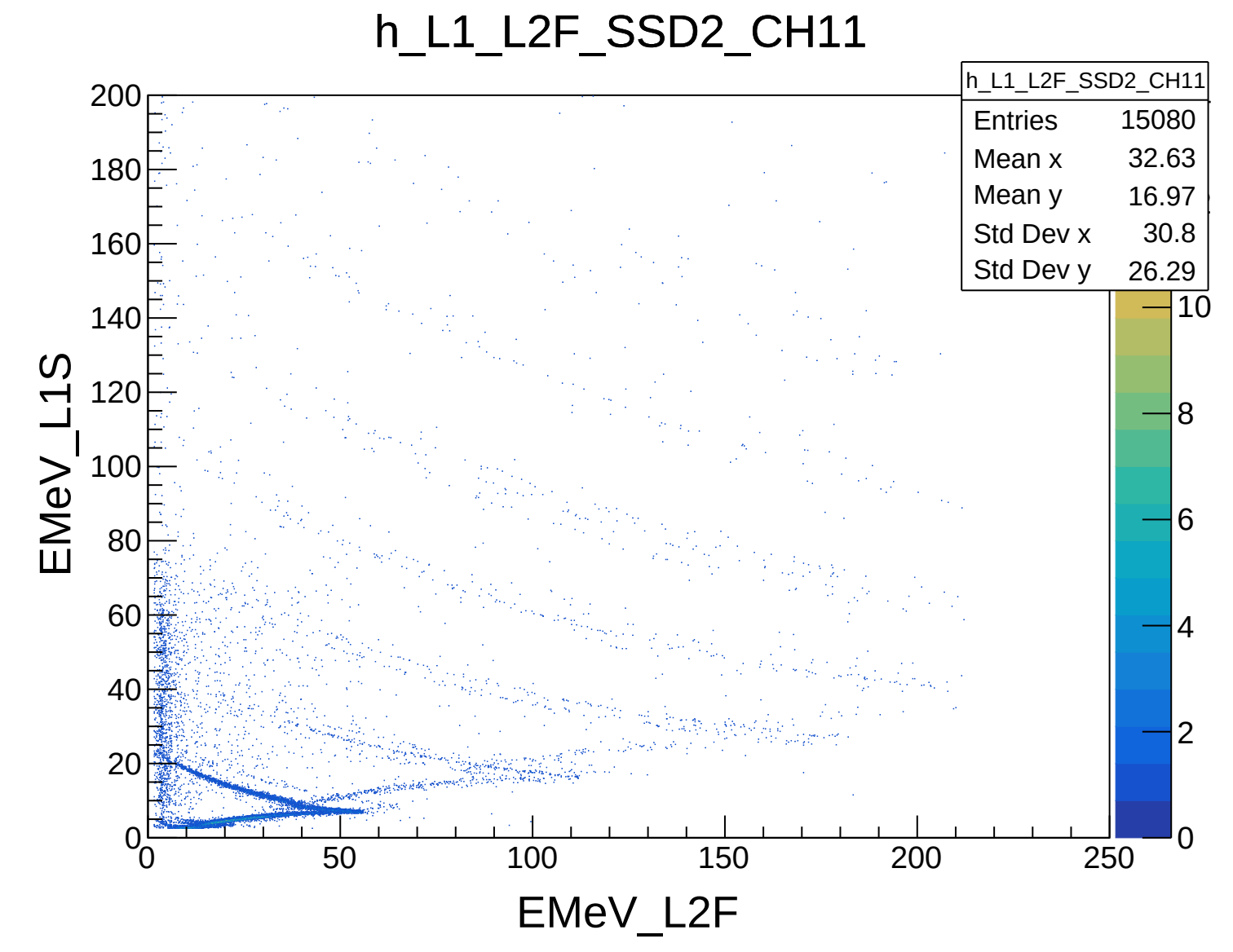

h_L1_L2F_SSD2_CH6
h_L1_L2F_SSD2_CH6
Entries 13892
Mean x 34.24
Mean y 16.65
Std Dev x 32.45
Std Dev y 24.92
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
1
2
3
4
5
6
7

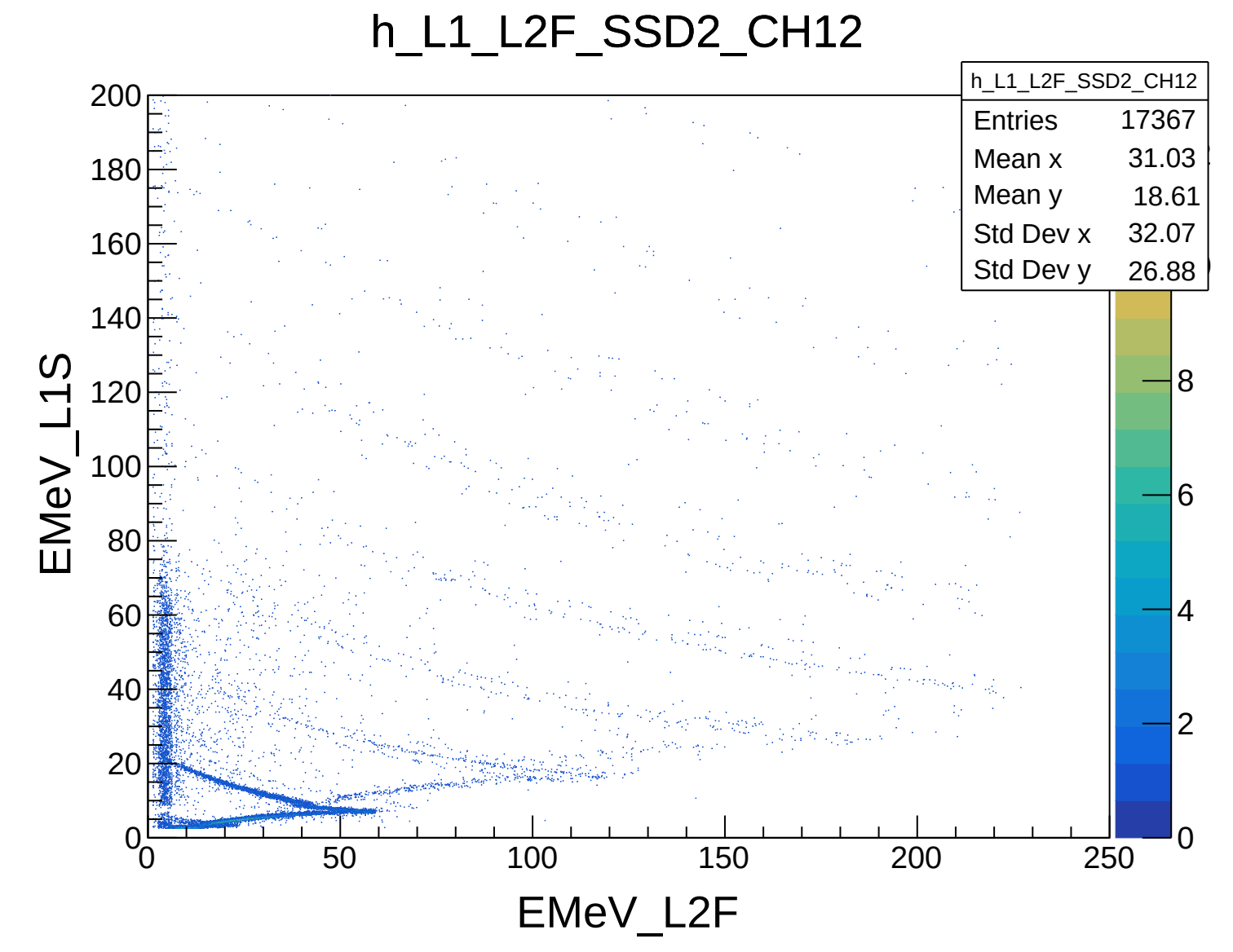

h_L1_L2F_SSD2_CH7
h_L1_L2F_SSD2_CH7
Entries 14945
Mean x 31.21
Mean y 18.39
Std Dev x 31.28
Std Dev y 26.78
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8

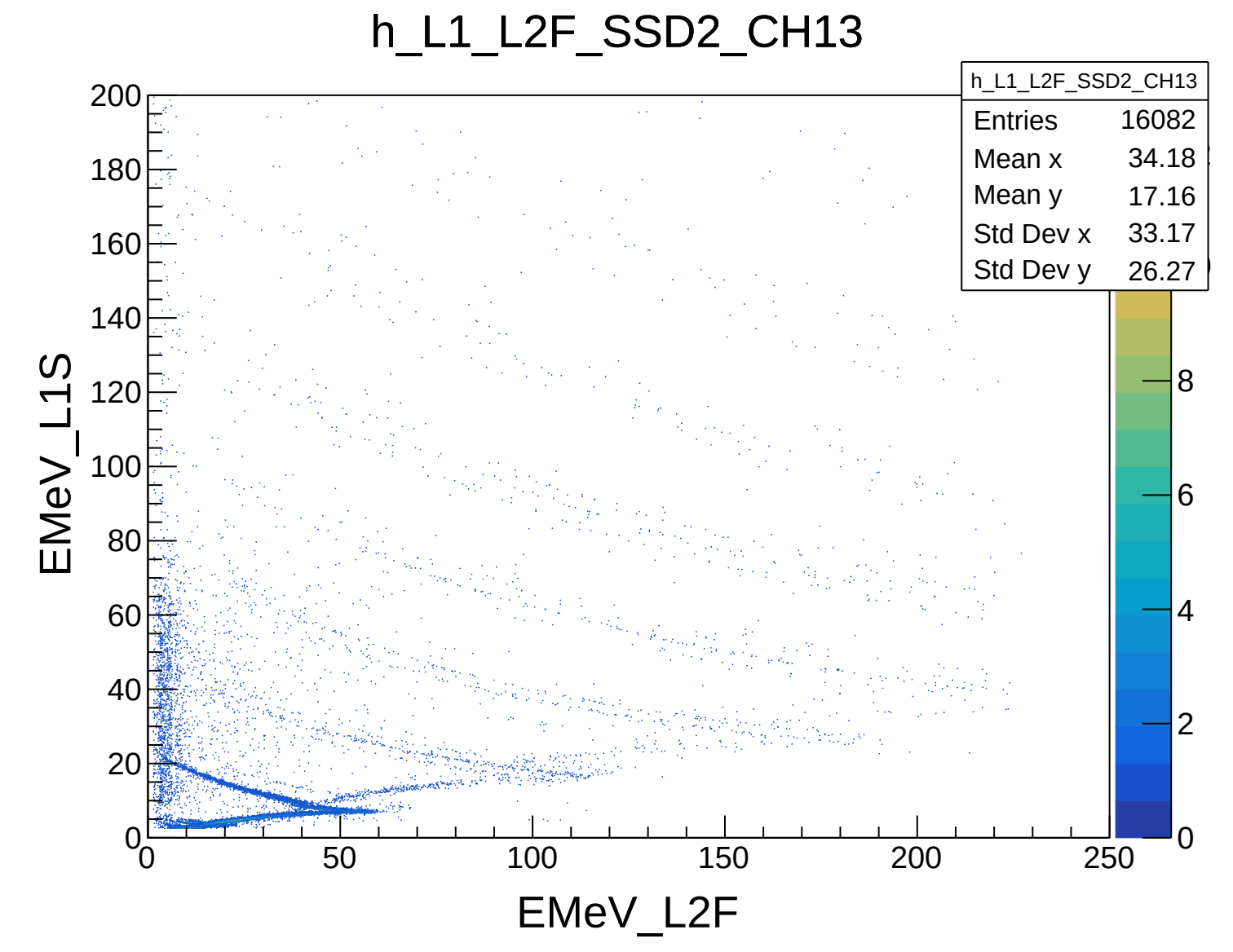

h_L1_L2F_SSD2_CH8
h_L1_L2F_SSD2_CH8
Entries 15044
Mean x 32.63
Mean y 17.3
Std Dev x 32.08
Std Dev y 25.79
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8

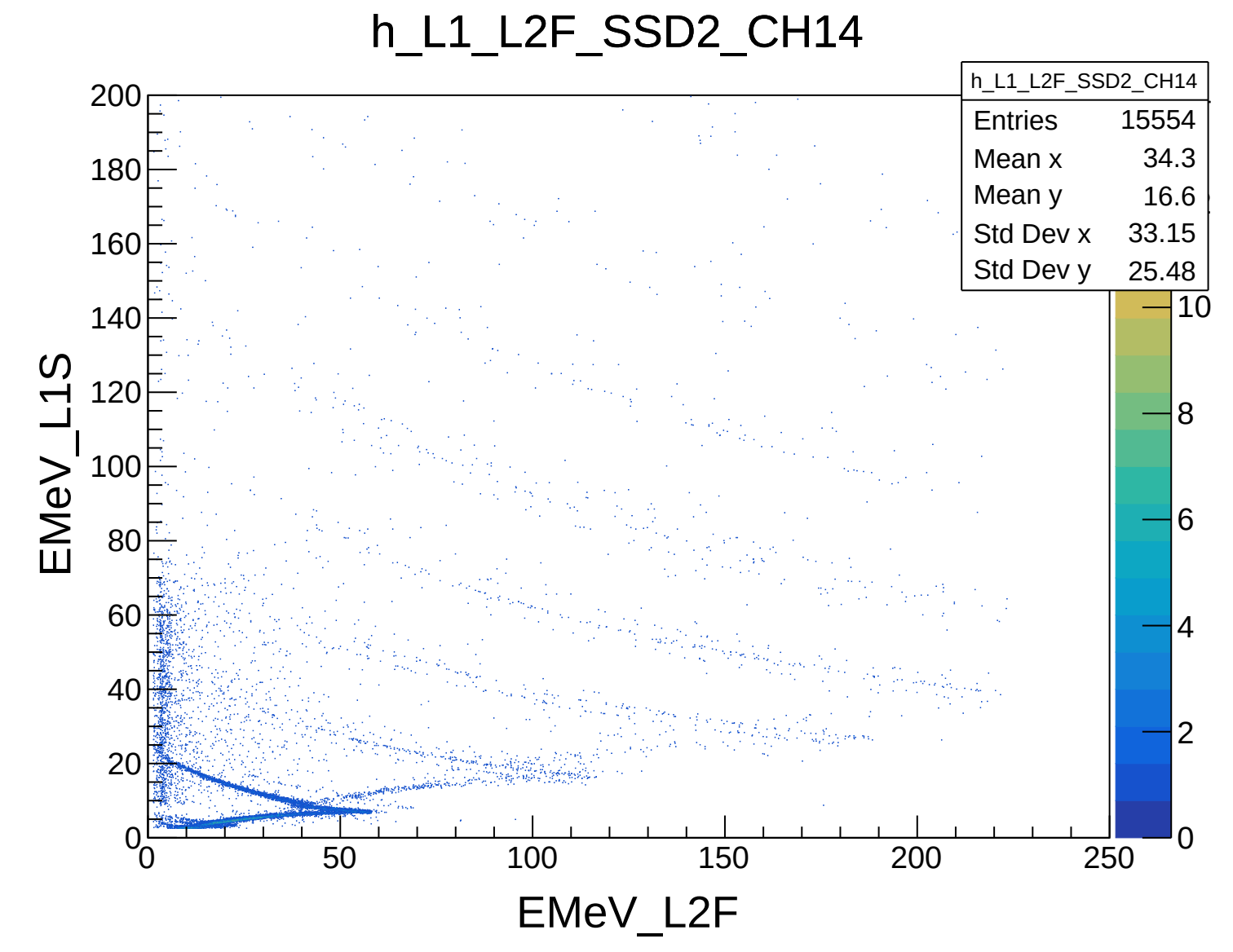

h_L1_L2F_SSD2_CH9
h_L1_L2F_SSD2_CH9
Entries 14464
Mean x 34.19
Mean y 16.81
Std Dev x 32.45
Std Dev y 25.43
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
1
2
3
4
5
6
7

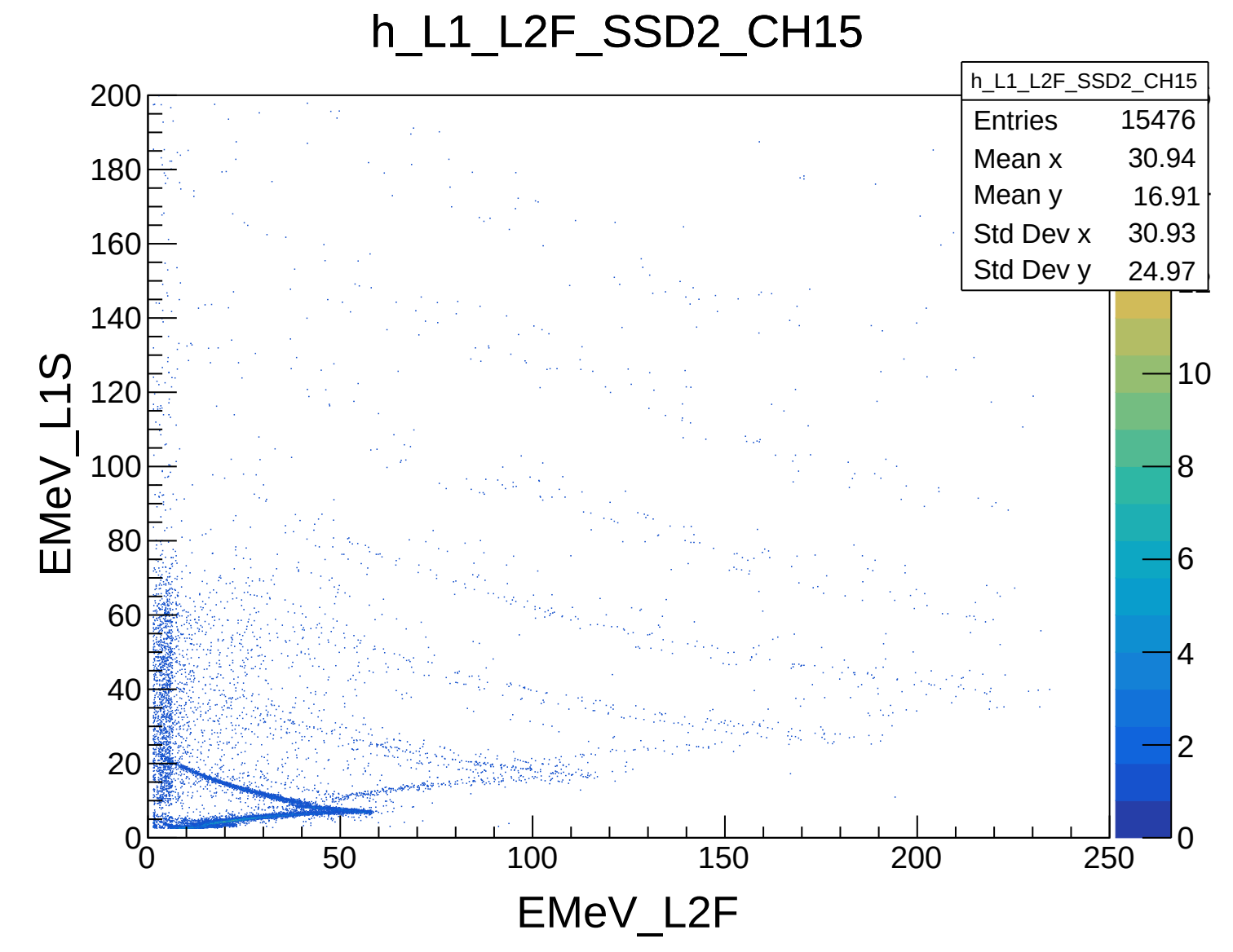

h_L1_L2F_SSD2_CH10
h_L1_L2F_SSD2_CH10
Entries 14462
Mean x 34.34
Mean y 16.94
Std Dev x 32.41
Std Dev y 26.33
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10
12

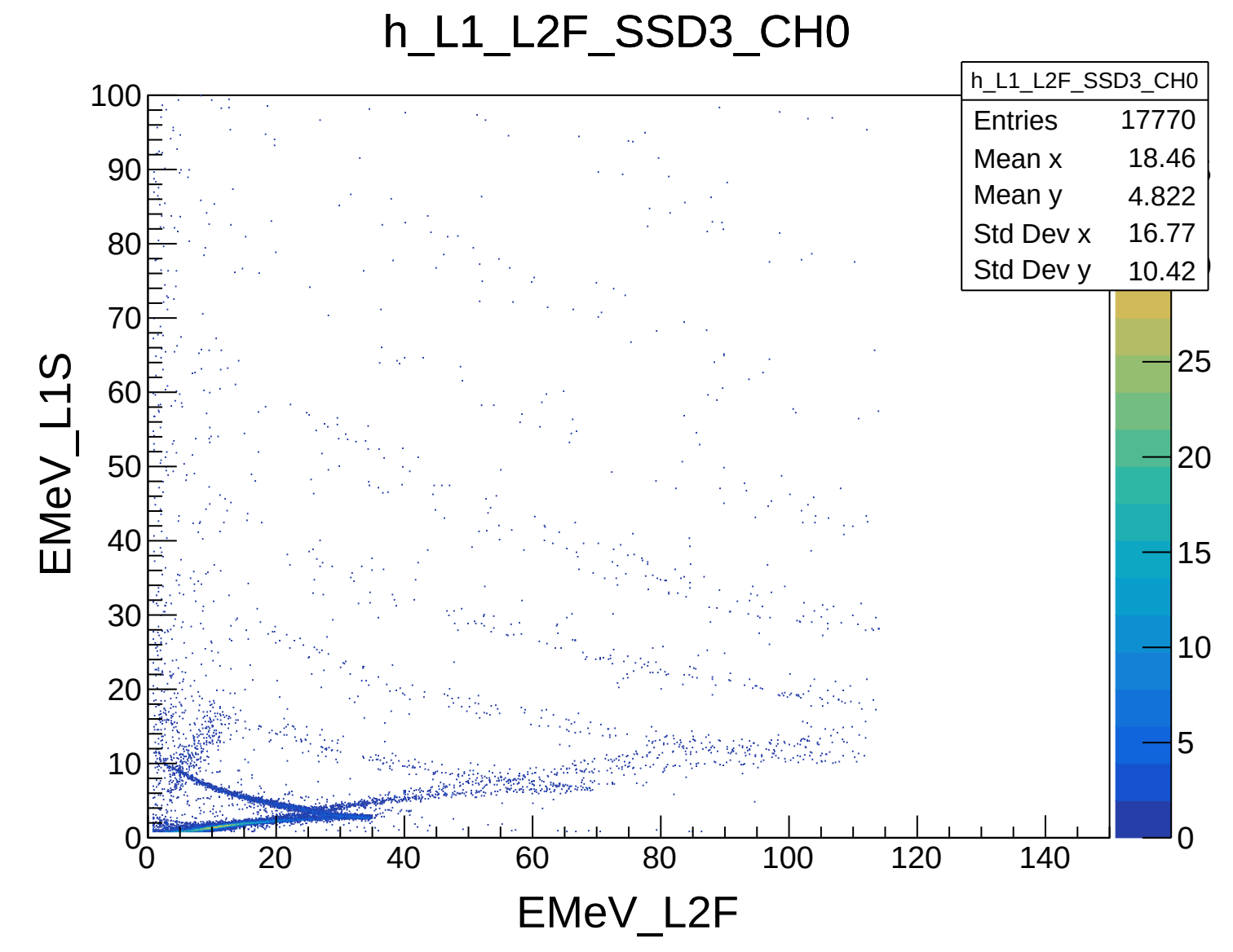

h_L1_L2F_SSD2_CH11
h_L1_L2F_SSD2_CH11
Entries 15080
Mean x 32.63
Mean y 16.97
Std Dev x 30.8
Std Dev y 26.29
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10

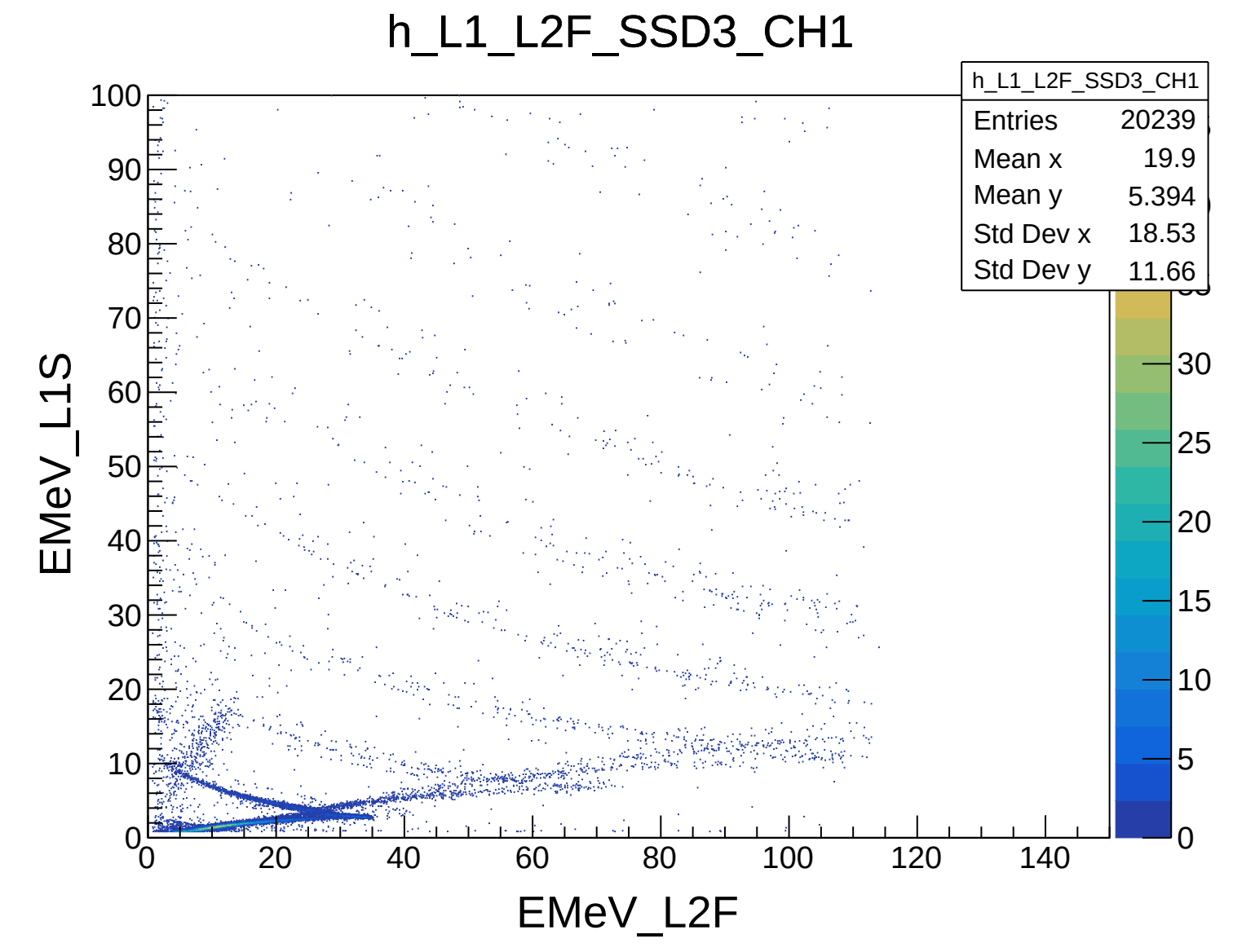

h_L1_L2F_SSD2_CH12
h_L1_L2F_SSD2_CH12
Entries 17367
Mean x 31.03
Mean y 18.61
Std Dev x 32.07
Std Dev y 26.88
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8

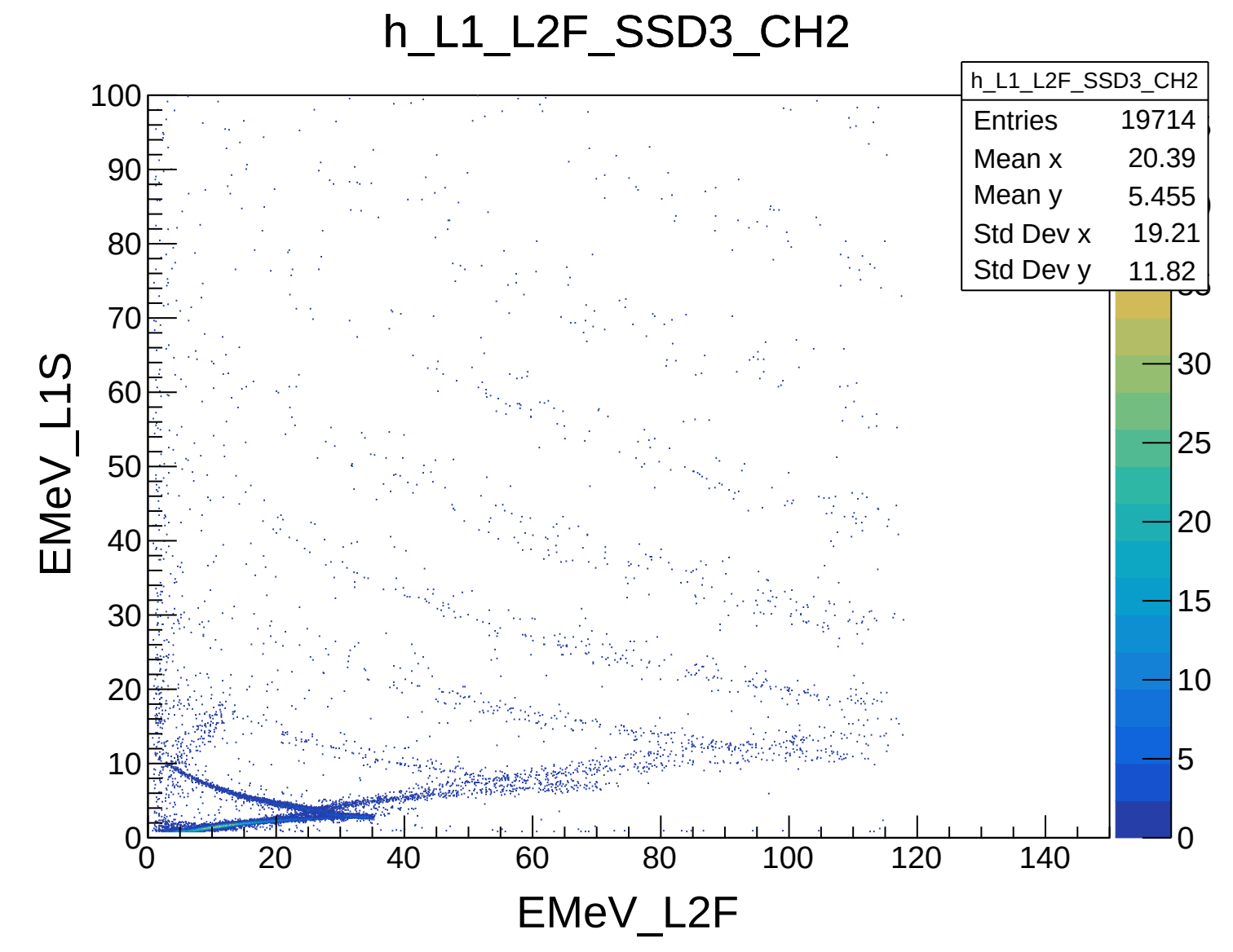

h_L1_L2F_SSD2_CH13
h_L1_L2F_SSD2_CH13
Entries 16082
Mean x 34.18
Mean y 17.16
Std Dev x 33.17
Std Dev y 26.27
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8

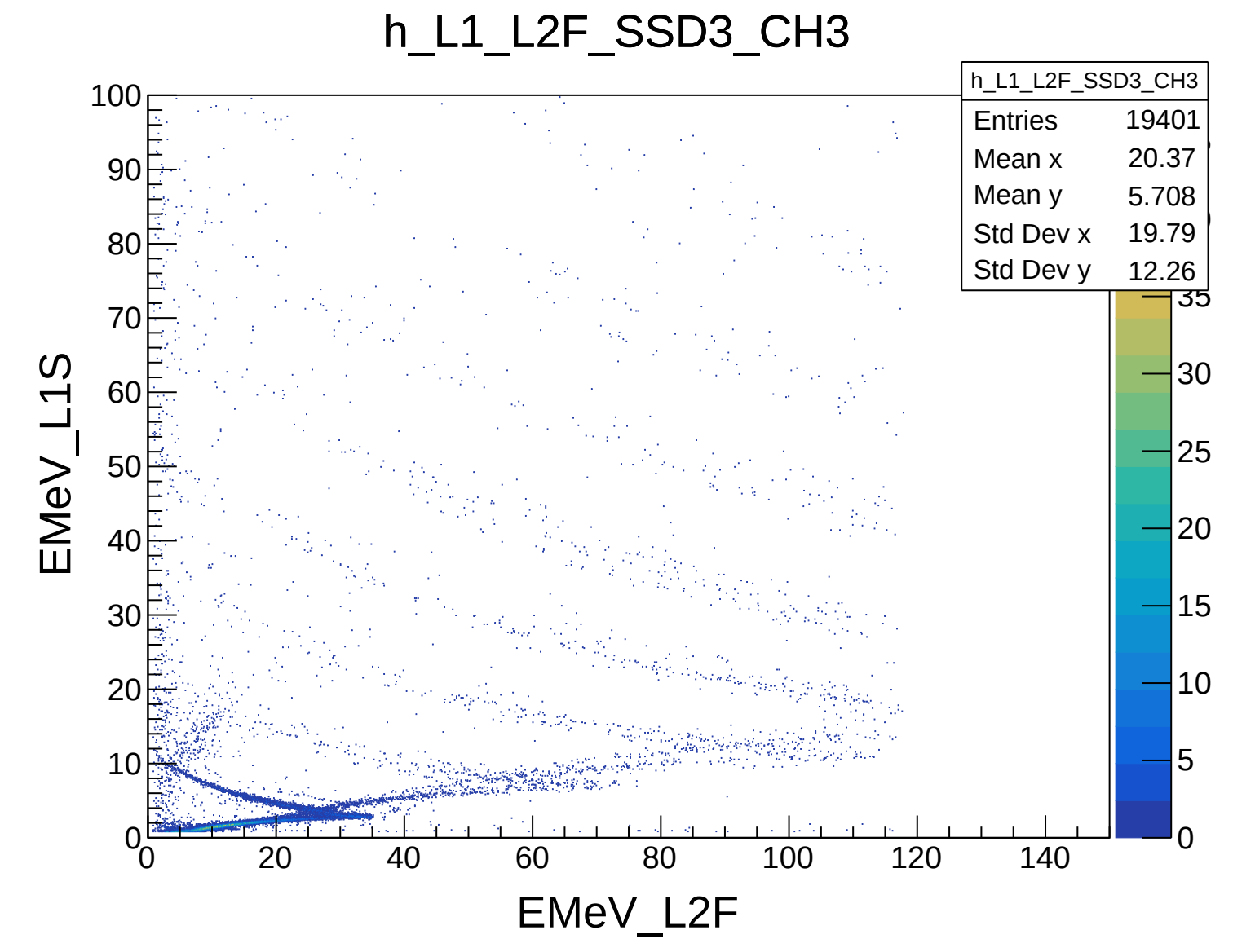

h_L1_L2F_SSD2_CH14
h_L1_L2F_SSD2_CH14
Entries 15554
Mean x 34.3
Mean y 16.6
Std Dev x 33.15
Std Dev y 25.48
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10

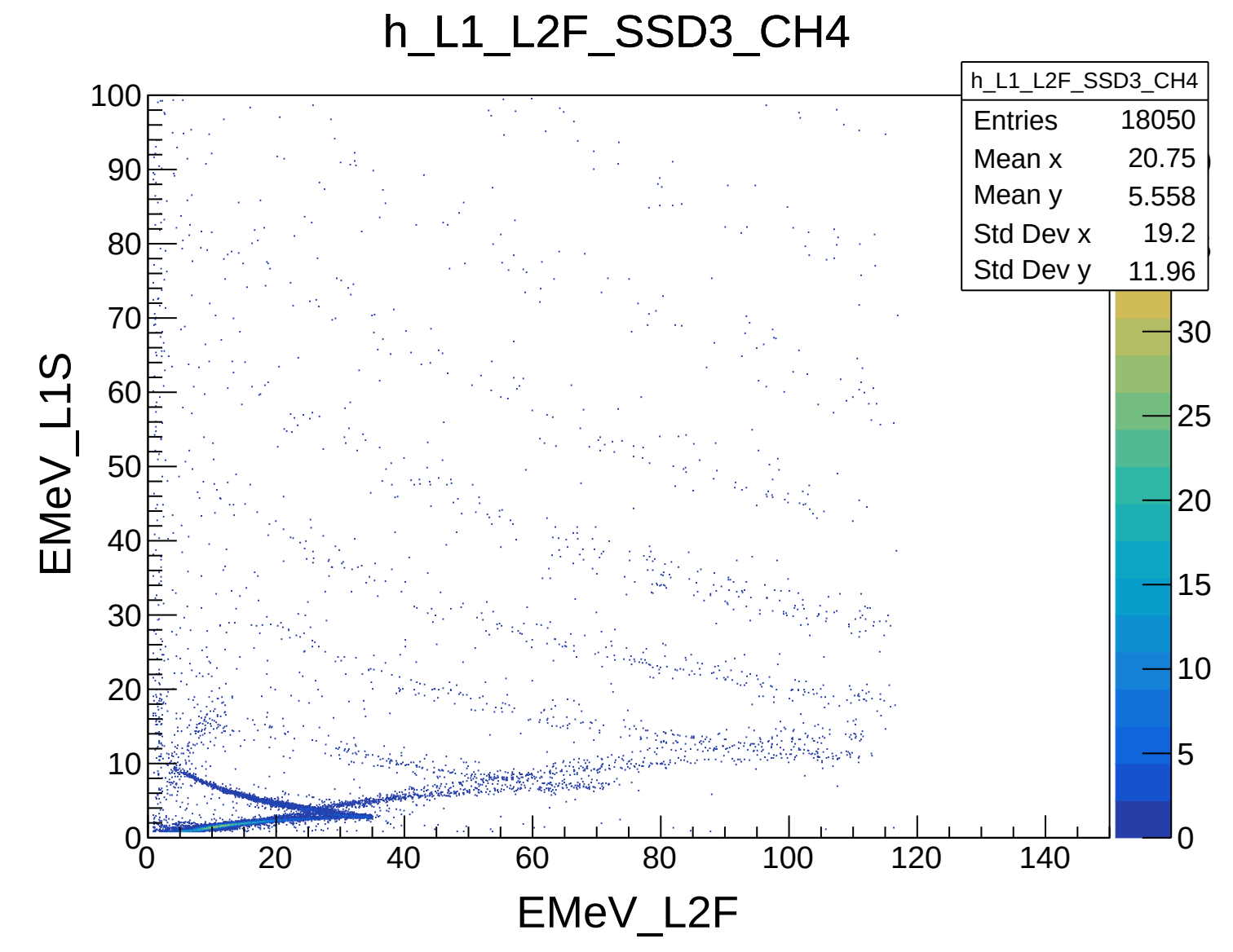

h_L1_L2F_SSD2_CH15
h_L1_L2F_SSD2_CH15
Entries 15476
Mean x 30.94
Mean y 16.91
Std Dev x 30.93
Std Dev y 24.97
EMeV_L1S
EMeV_L2F
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10

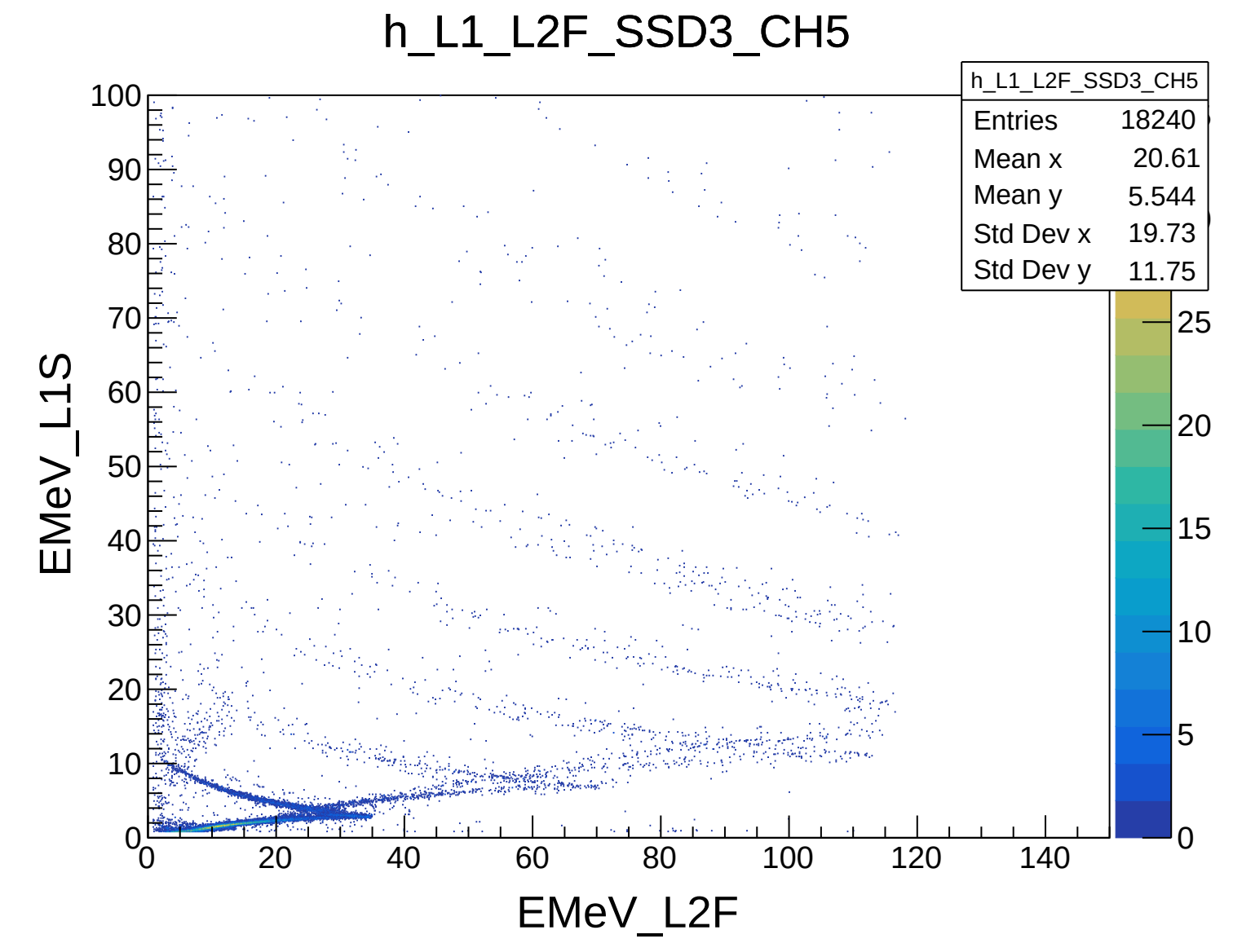

h_L1_L2F_SSD3_CH0
h_L1_L2F_SSD3_CH0
Entries 17770
Mean x 18.46
Mean y 4.822
Std Dev x 16.77
Std Dev y 10.42
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25

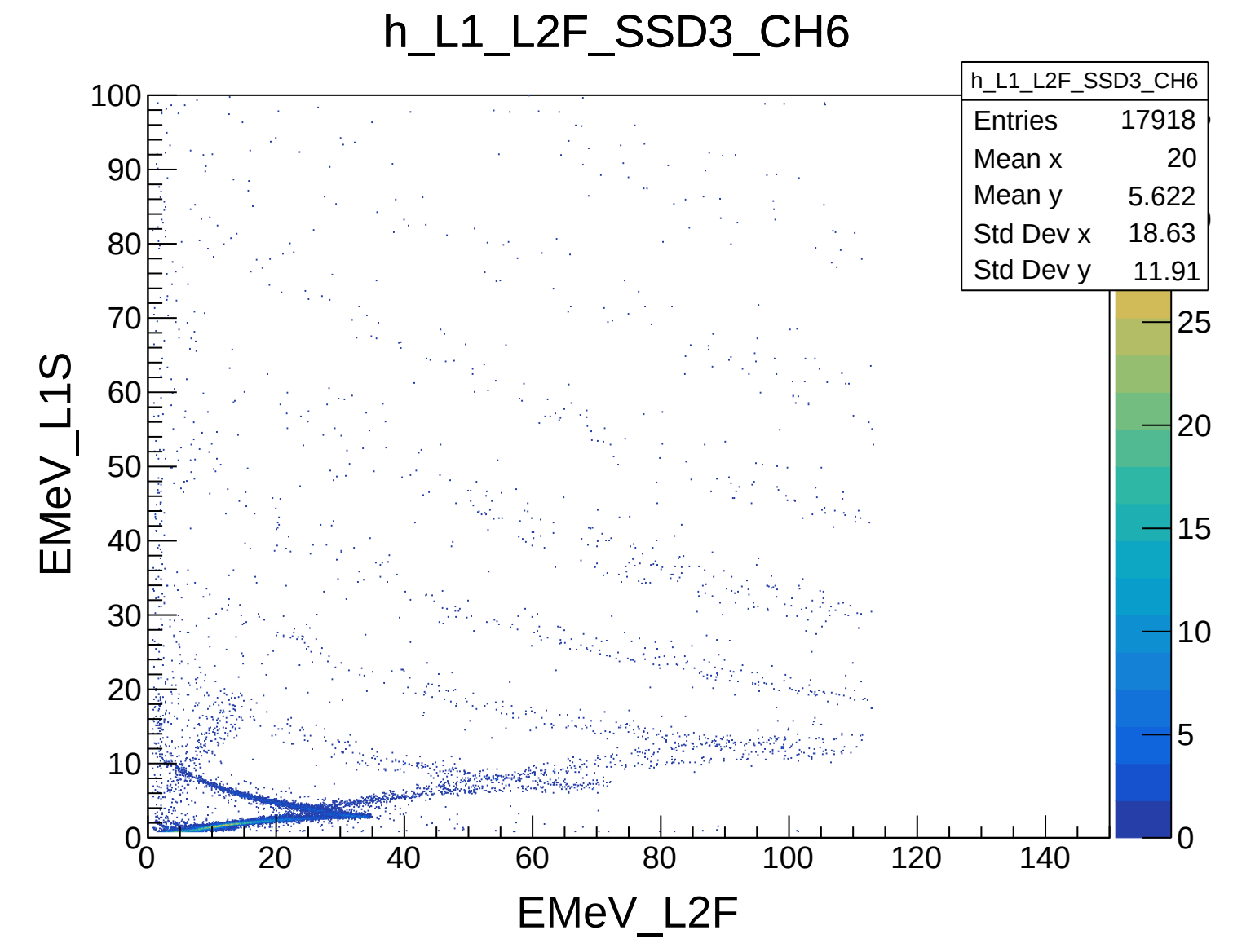

h_L1_L2F_SSD3_CH1
h_L1_L2F_SSD3_CH1
Entries 20239
Mean x 19.9
Mean y 5.394
Std Dev x 18.53
Std Dev y 11.66
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25
30

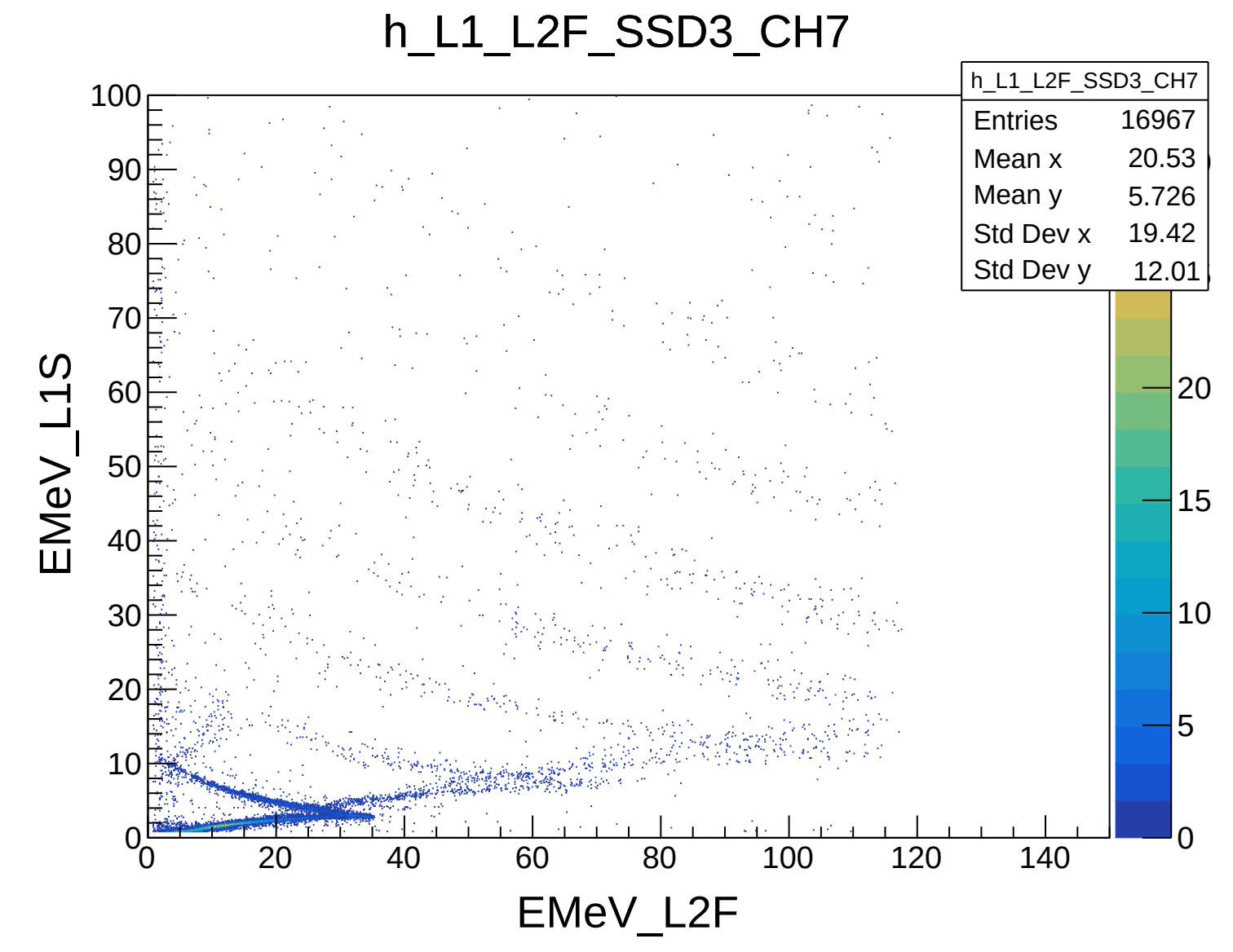

h_L1_L2F_SSD3_CH2
h_L1_L2F_SSD3_CH2
Entries 19714
Mean x 20.39
Mean y 5.455
Std Dev x 19.21
Std Dev y 11.82
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25
30

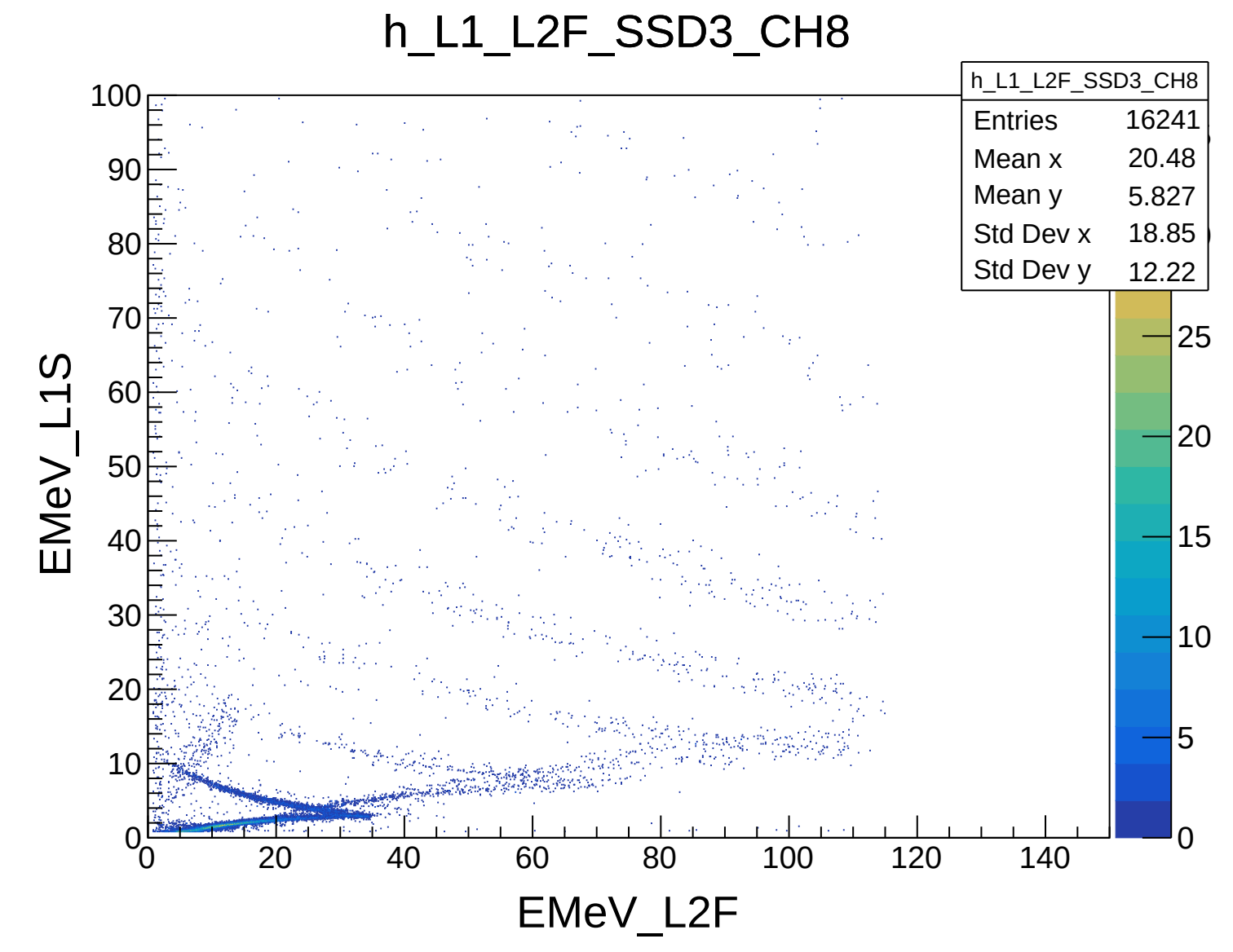

h_L1_L2F_SSD3_CH3
h_L1_L2F_SSD3_CH3
Entries 19401
Mean x 20.37
Mean y 5.708
Std Dev x 19.79
Std Dev y 12.26
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25
30
35

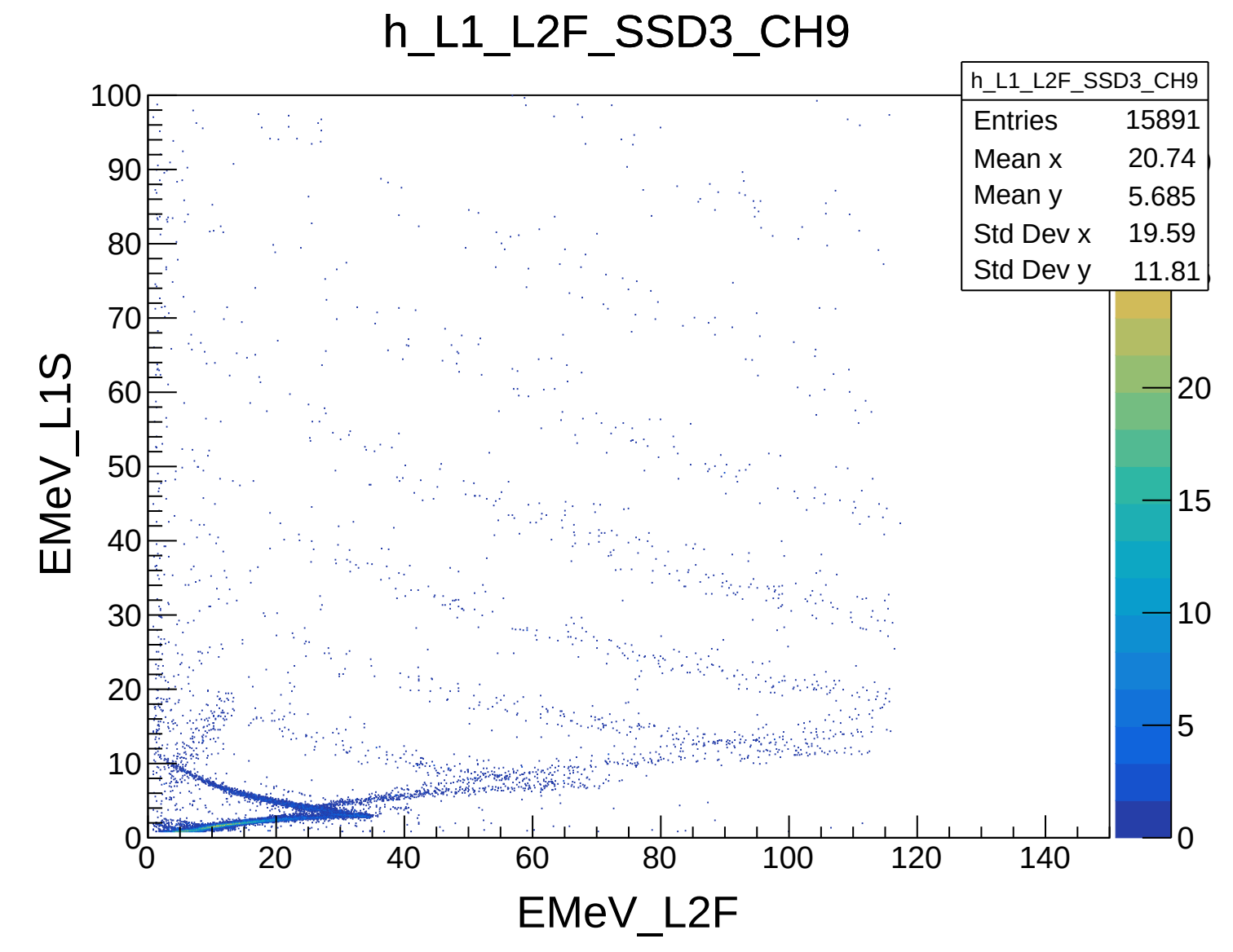

h_L1_L2F_SSD3_CH4
h_L1_L2F_SSD3_CH4
Entries 18050
Mean x 20.75
Mean y 5.558
Std Dev x 19.2
Std Dev y 11.96
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25
30

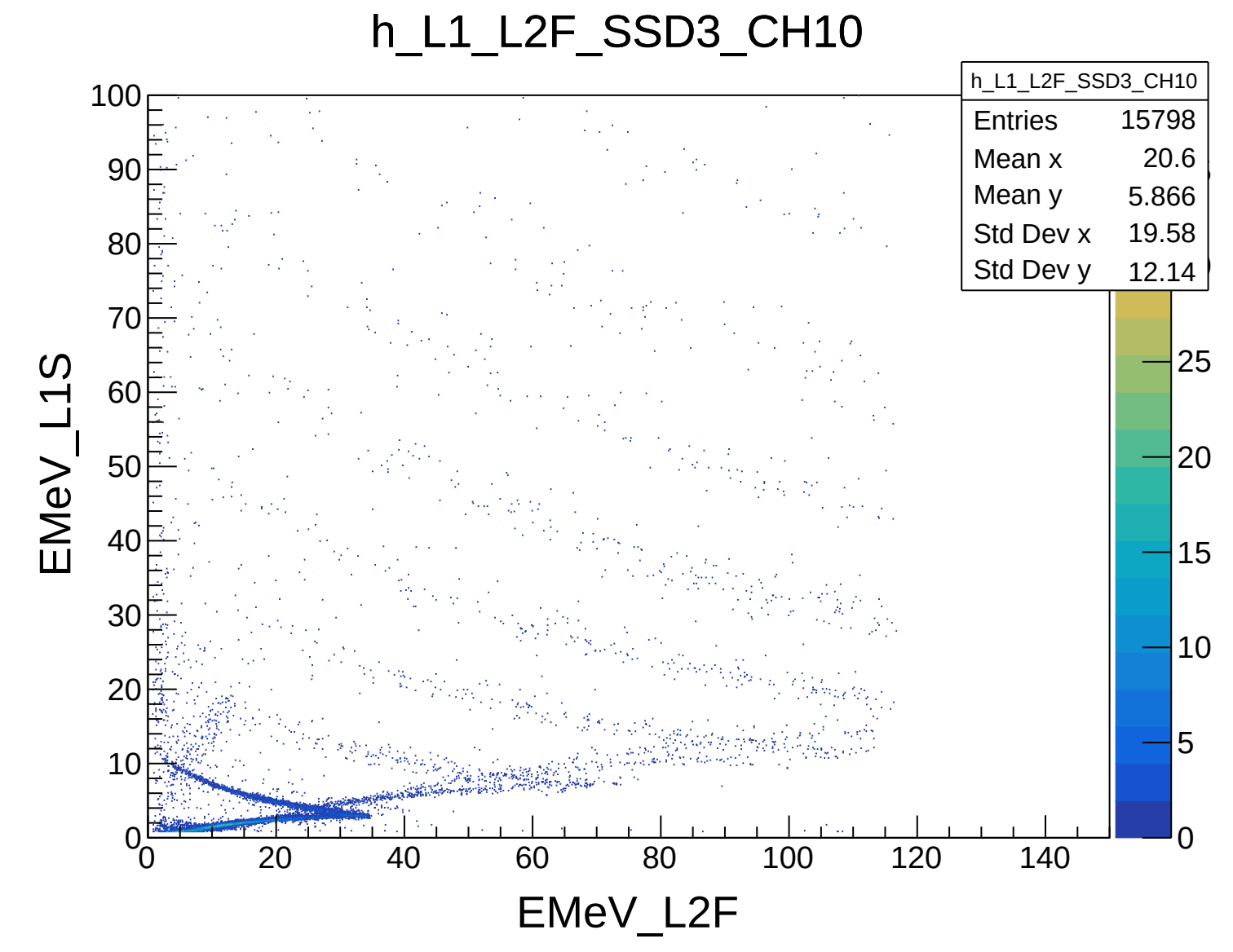

h_L1_L2F_SSD3_CH5
h_L1_L2F_SSD3_CH5
Entries 18240
Mean x 20.61
Mean y 5.544
Std Dev x 19.73
Std Dev y 11.75
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25

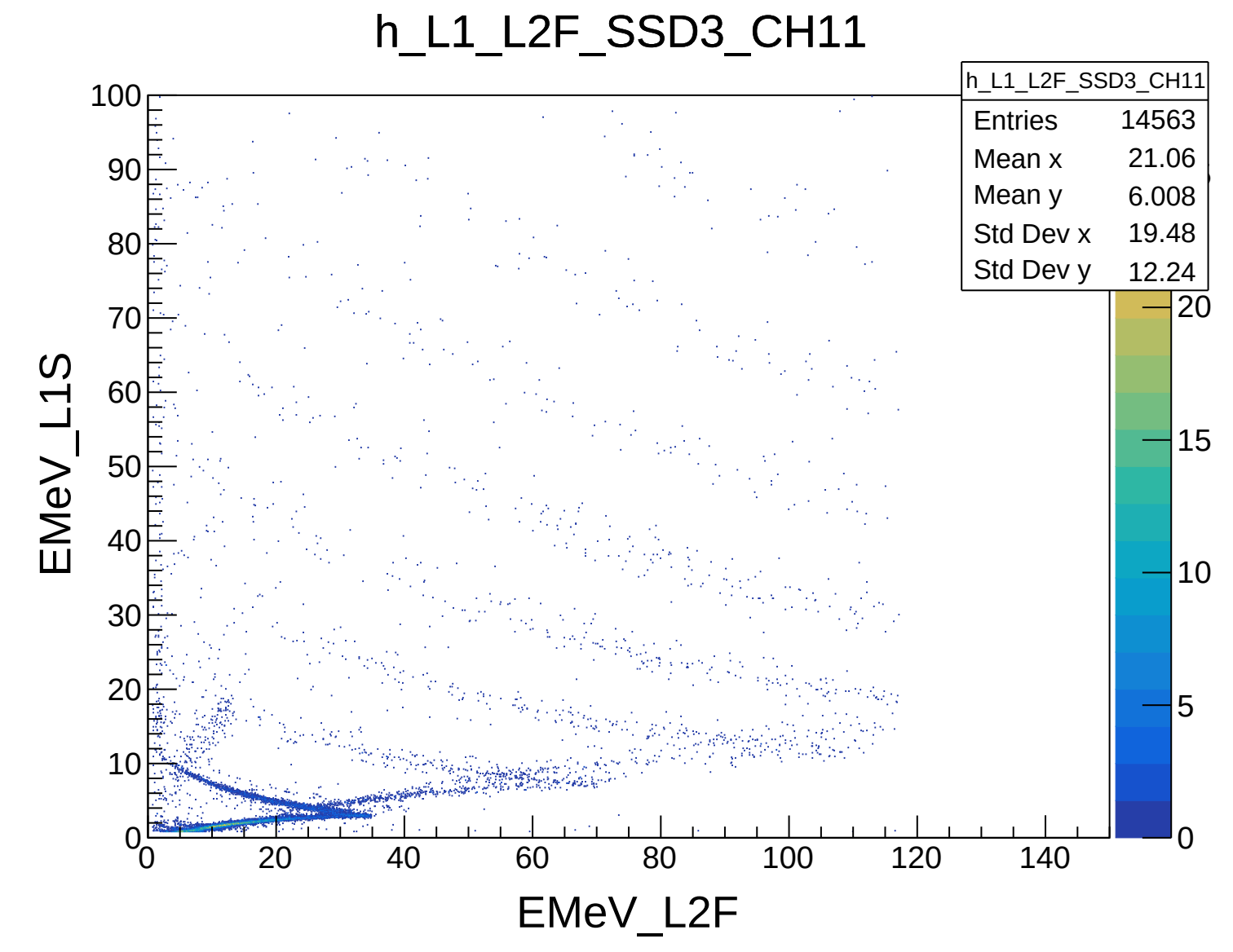

h_L1_L2F_SSD3_CH6
h_L1_L2F_SSD3_CH6
Entries 17918
Mean x 20
Mean y 5.622
Std Dev x 18.63
Std Dev y 11.91
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25

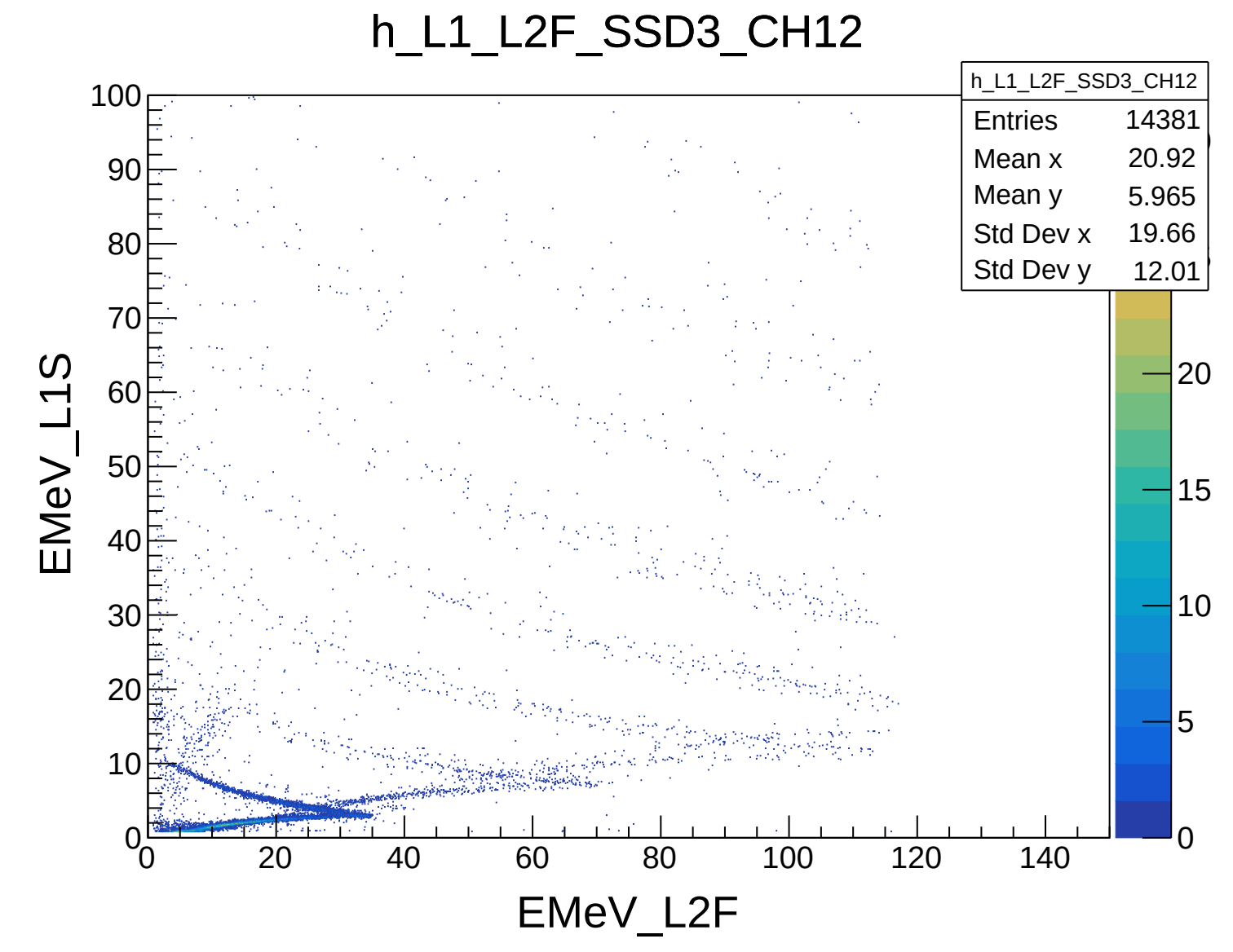

h_L1_L2F_SSD3_CH7
h_L1_L2F_SSD3_CH7
Entries 16967
Mean x 20.53
Mean y 5.726
Std Dev x 19.42
Std Dev y 12.01
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20

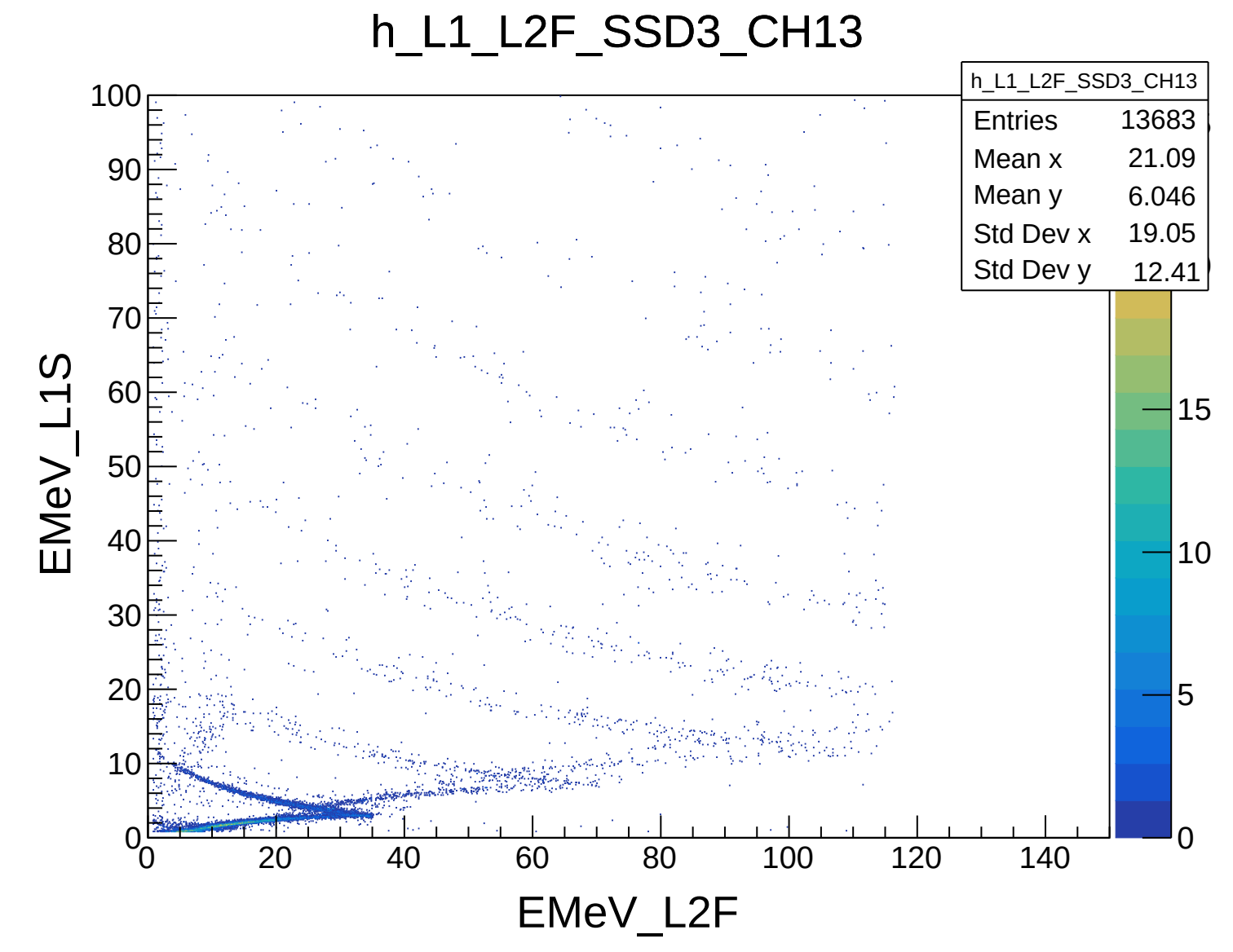

h_L1_L2F_SSD3_CH8
h_L1_L2F_SSD3_CH8
Entries 16241
Mean x 20.48
Mean y 5.827
Std Dev x 18.85
Std Dev y 12.22
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25

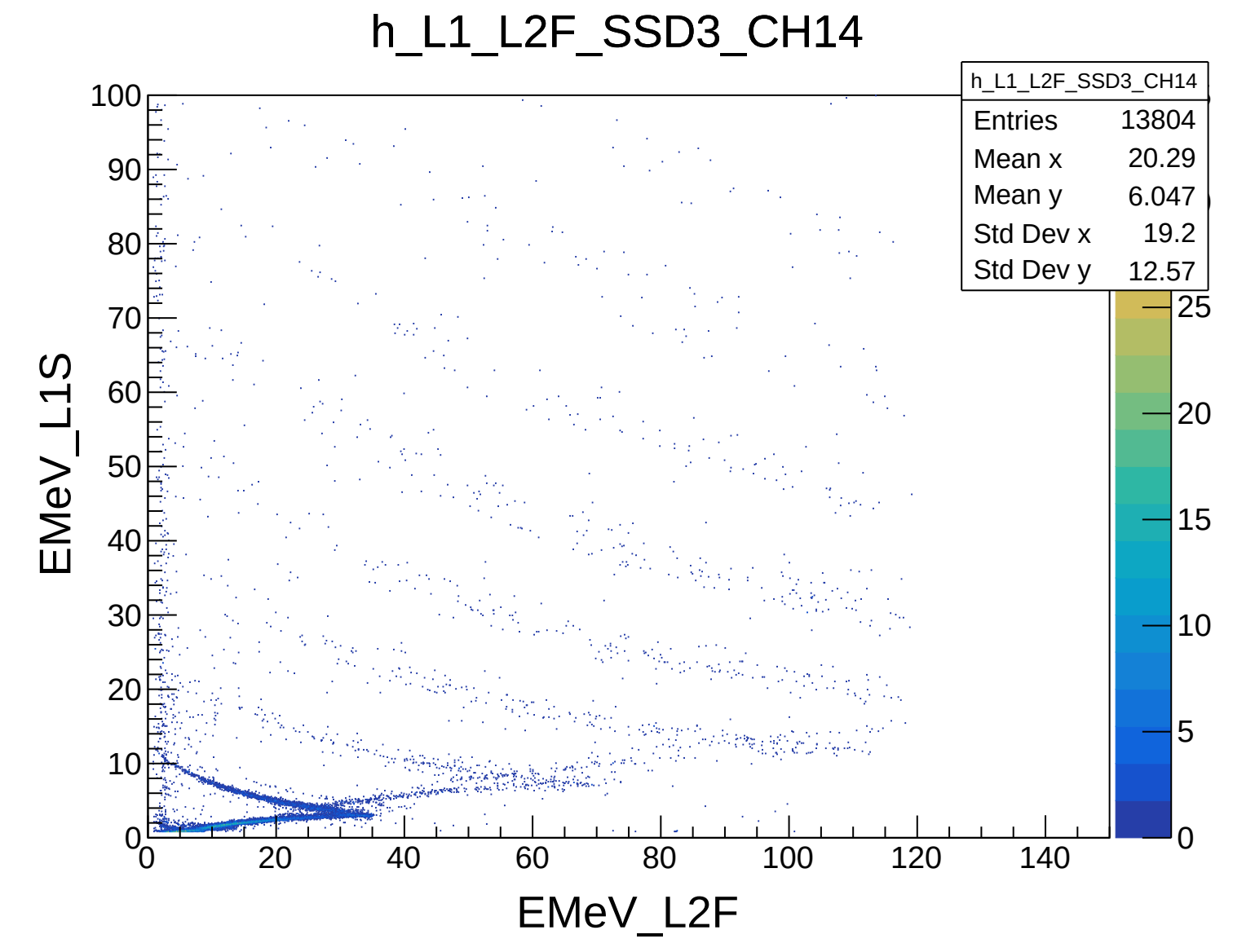

h_L1_L2F_SSD3_CH9
h_L1_L2F_SSD3_CH9
Entries 15891
Mean x 20.74
Mean y 5.685
Std Dev x 19.59
Std Dev y 11.81
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20

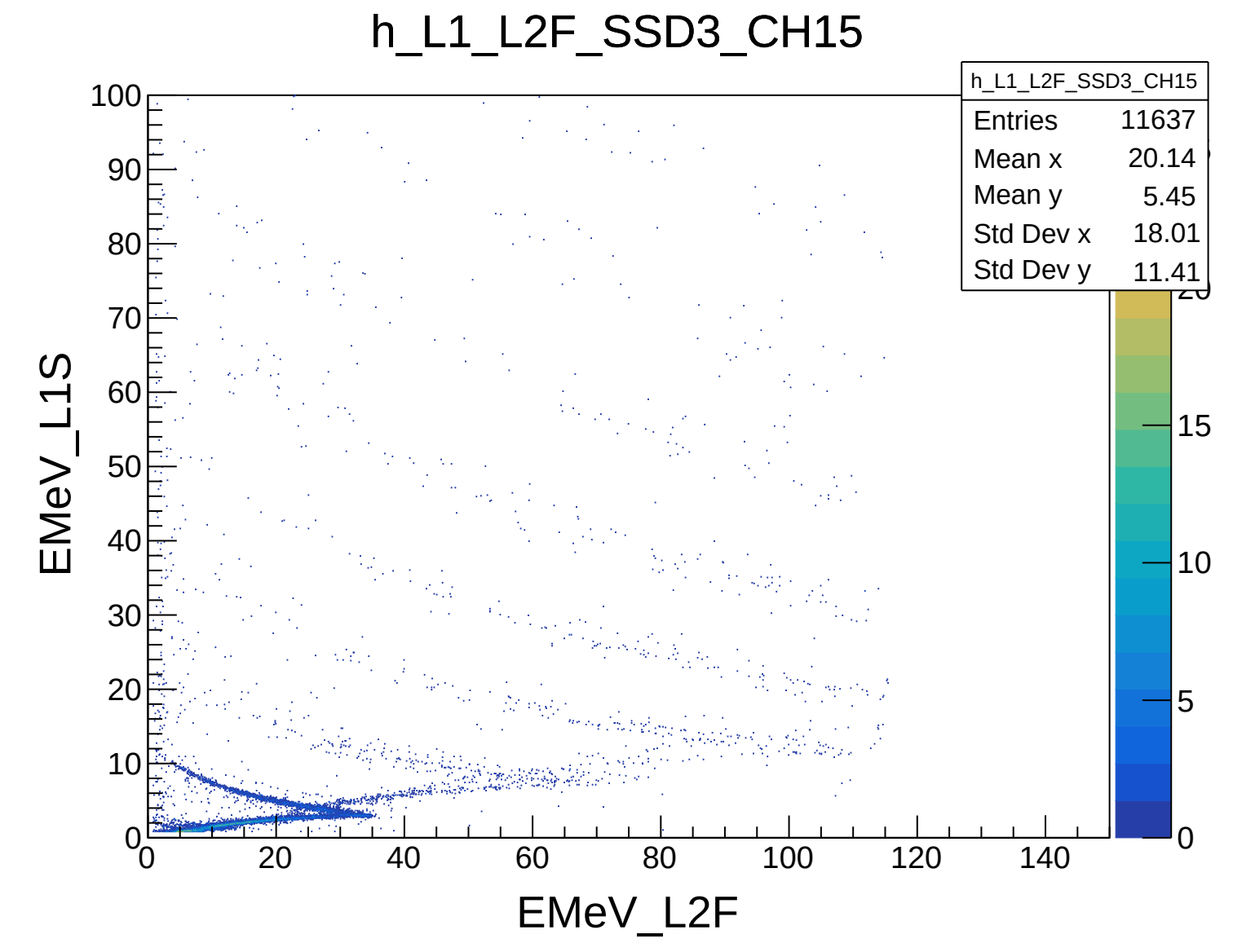

h_L1_L2F_SSD3_CH10
h_L1_L2F_SSD3_CH10
Entries 15798
Mean x 20.6
Mean y 5.866
Std Dev x 19.58
Std Dev y 12.14
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25

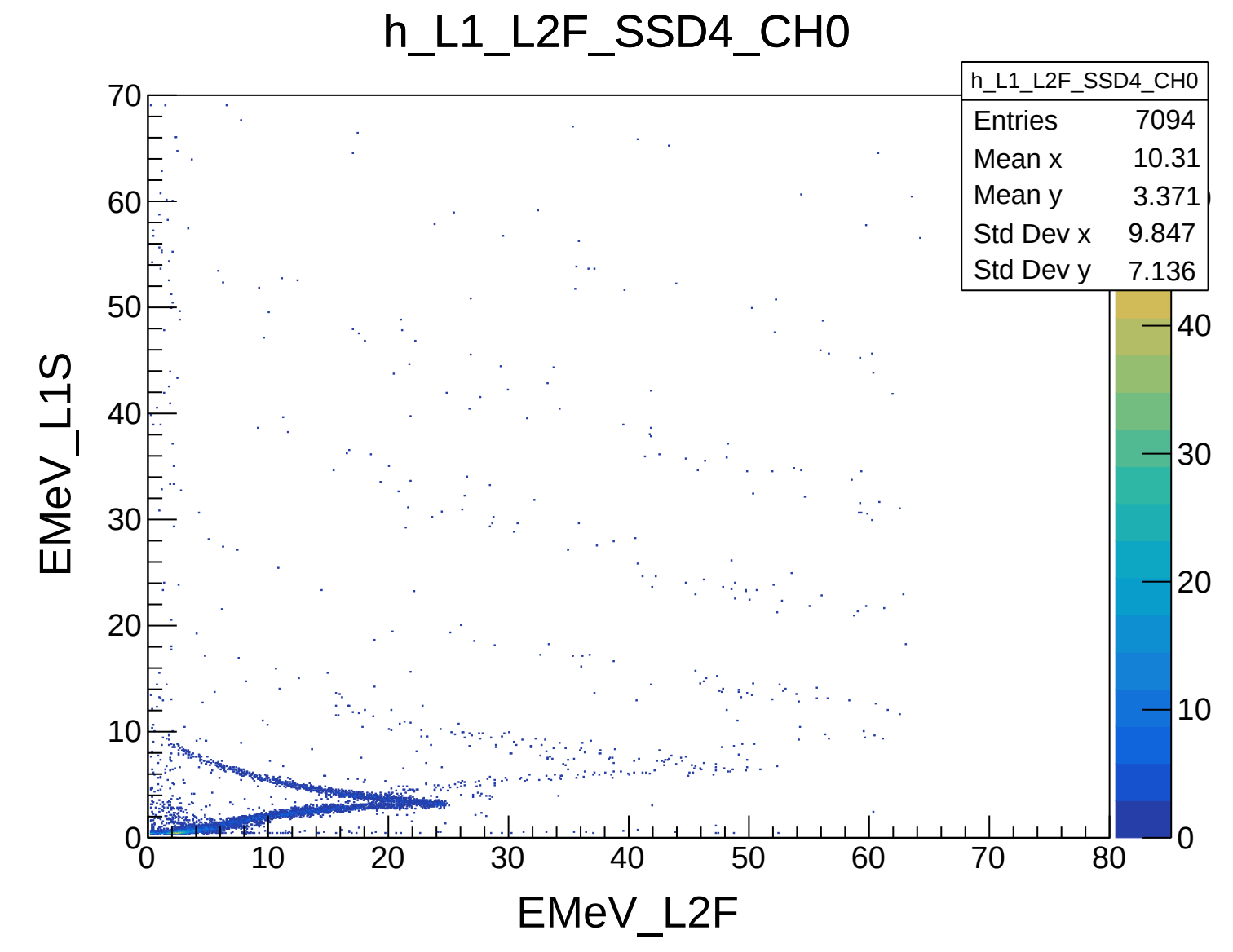

h_L1_L2F_SSD3_CH11
h_L1_L2F_SSD3_CH11
Entries 14563
Mean x 21.06
Mean y 6.008
Std Dev x 19.48
Std Dev y 12.24
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20

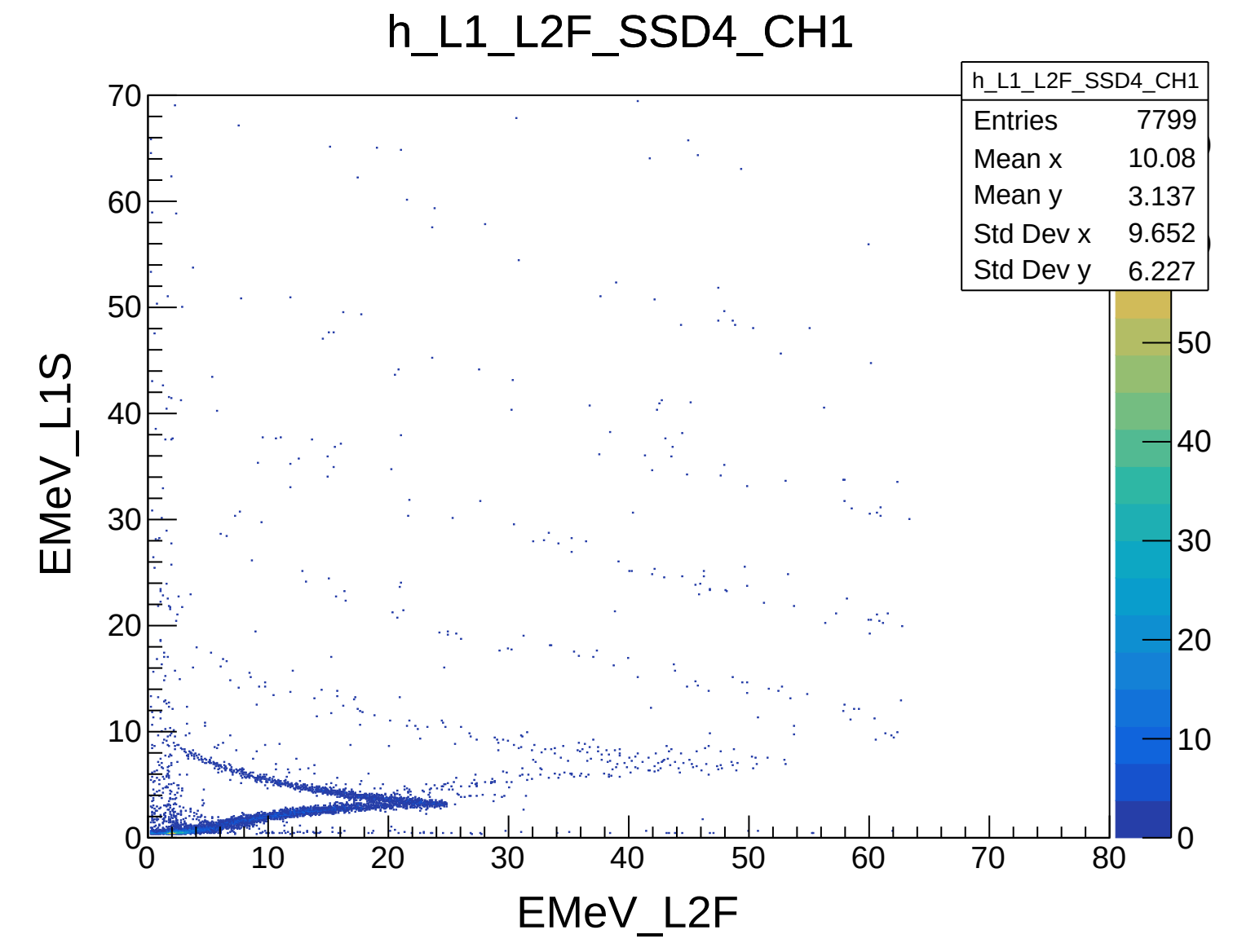

h_L1_L2F_SSD3_CH12
h_L1_L2F_SSD3_CH12
Entries 14381
Mean x 20.92
Mean y 5.965
Std Dev x 19.66
Std Dev y 12.01
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20

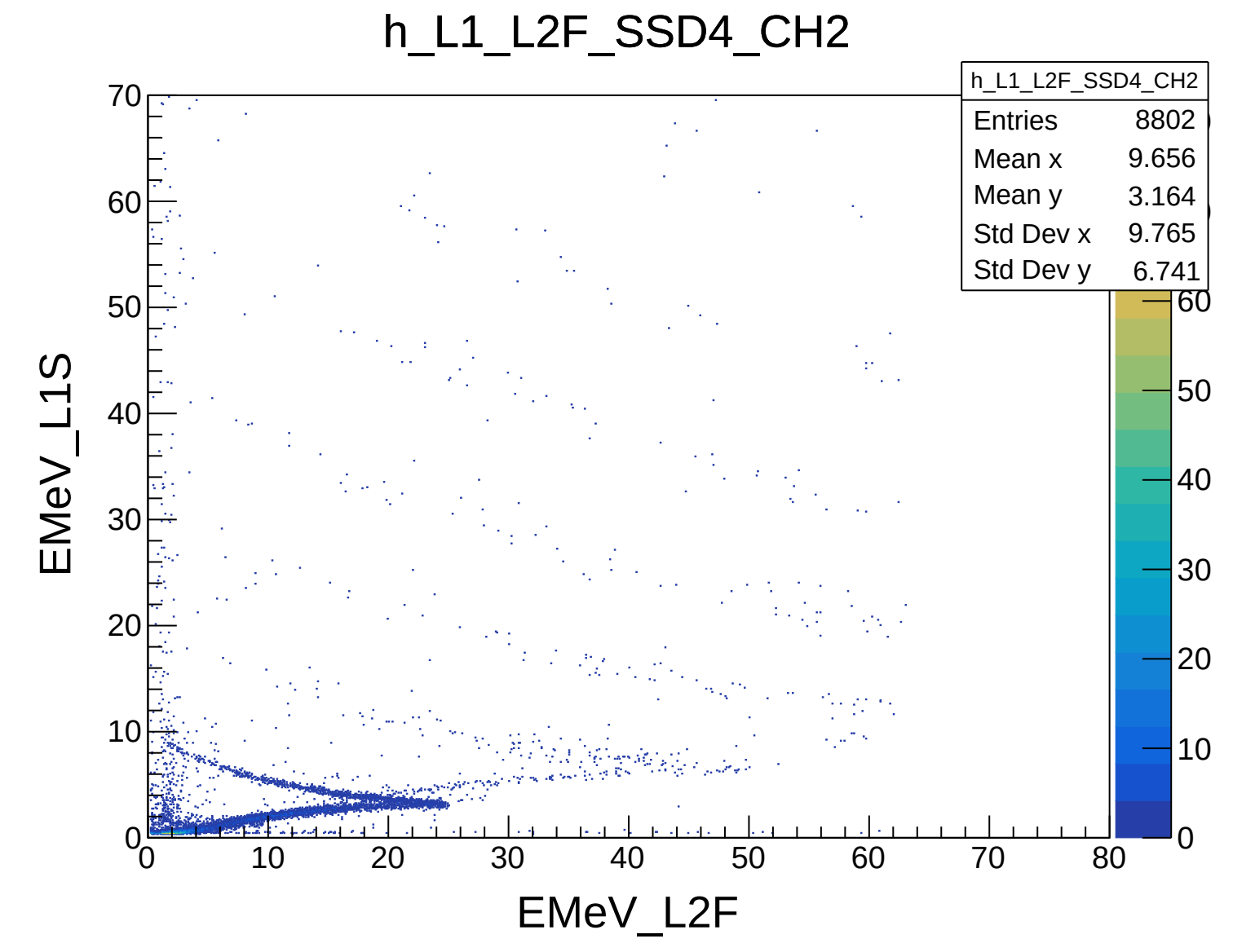

h_L1_L2F_SSD3_CH13
h_L1_L2F_SSD3_CH13
Entries 13683
Mean x 21.09
Mean y 6.046
Std Dev x 19.05
Std Dev y 12.41
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15

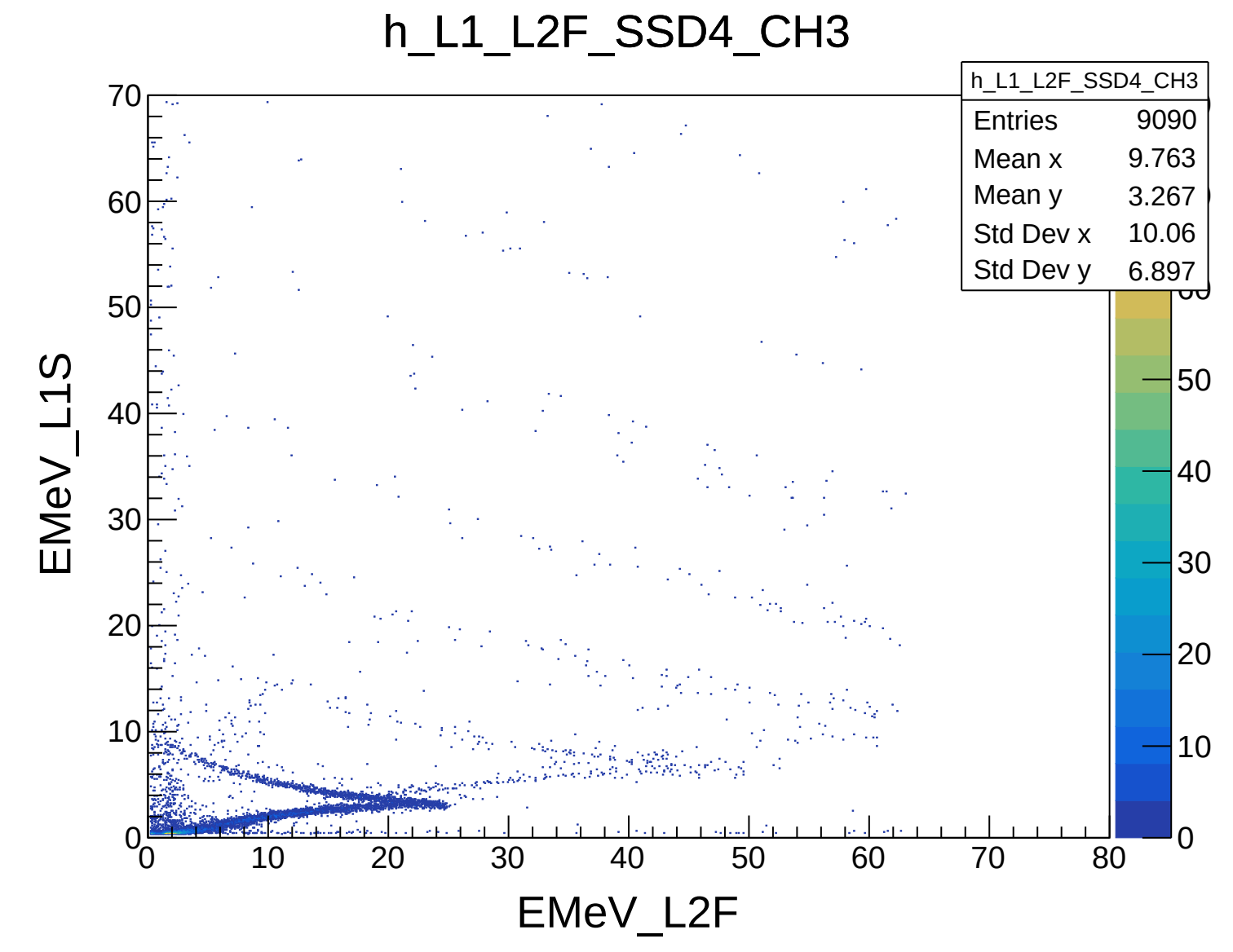

h_L1_L2F_SSD3_CH14
h_L1_L2F_SSD3_CH14
Entries 13804
Mean x 20.29
Mean y 6.047
Std Dev x 19.2
Std Dev y 12.57
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20
25

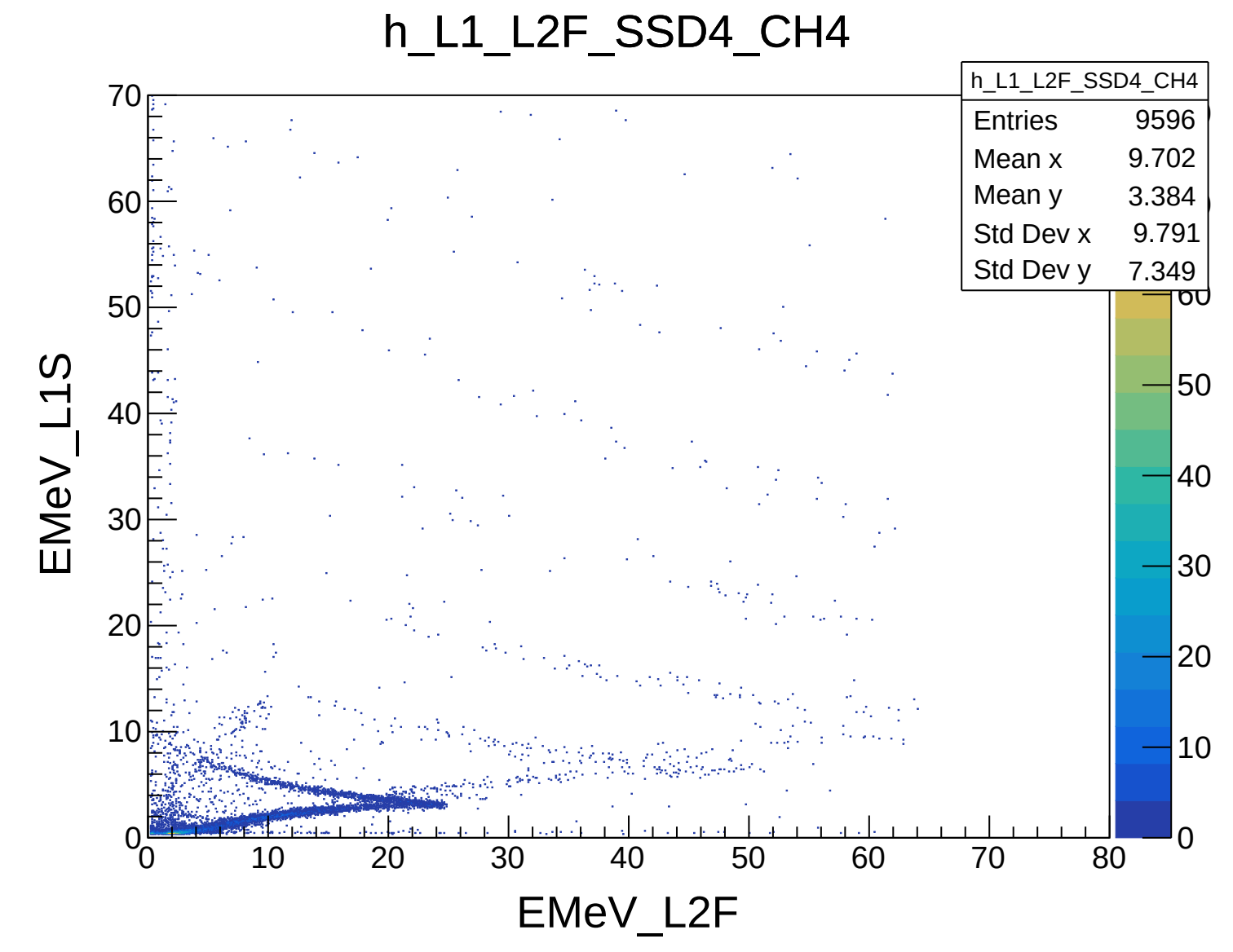

h_L1_L2F_SSD3_CH15
h_L1_L2F_SSD3_CH15
Entries 11637
Mean x 20.14
Mean y 5.45
Std Dev x 18.01
Std Dev y 11.41
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
5
10
15
20

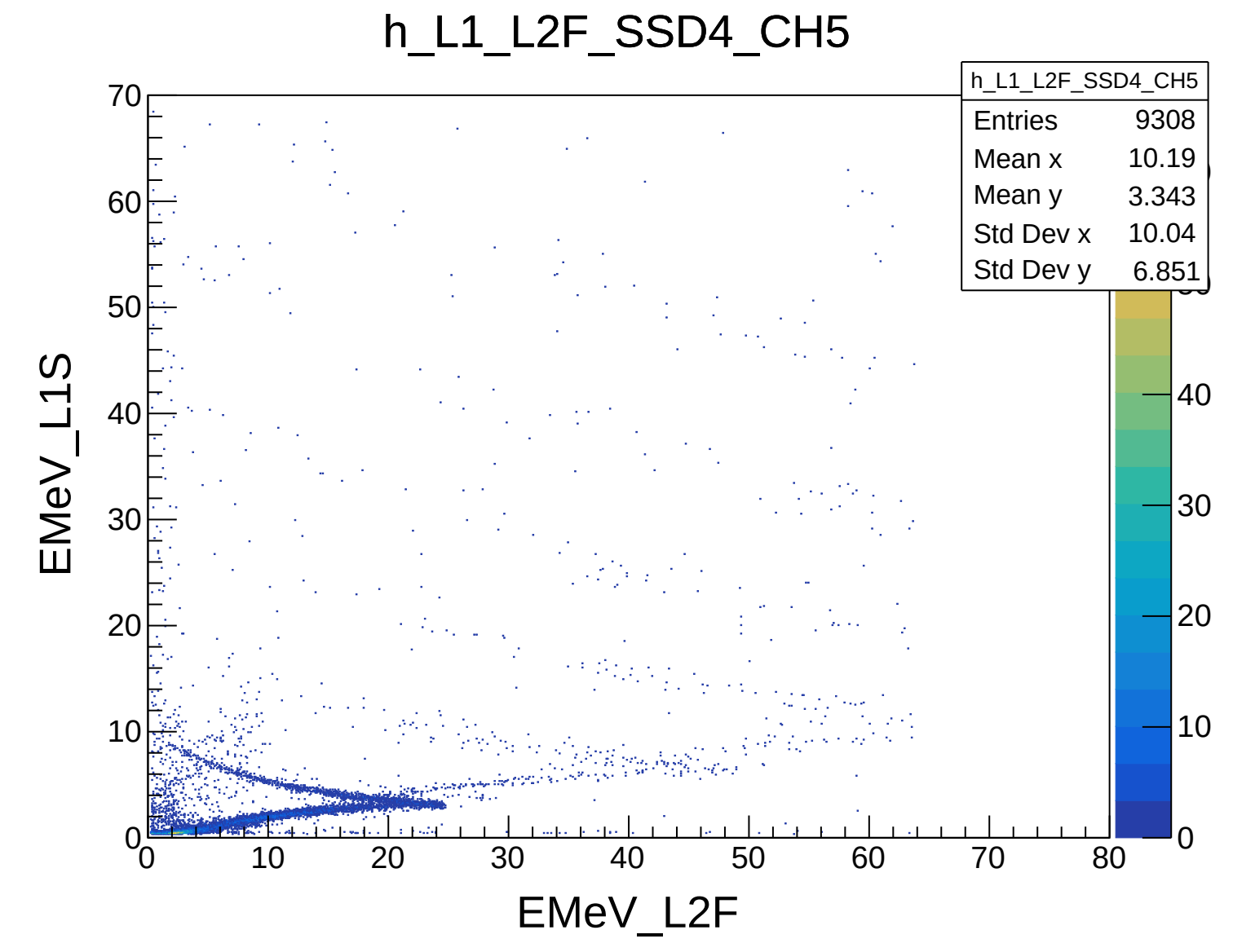

h_L1_L2F_SSD4_CH0
h_L1_L2F_SSD4_CH0
Entries 7094
Mean x 10.31
Mean y 3.371
Std Dev x 9.847
Std Dev y 7.136
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

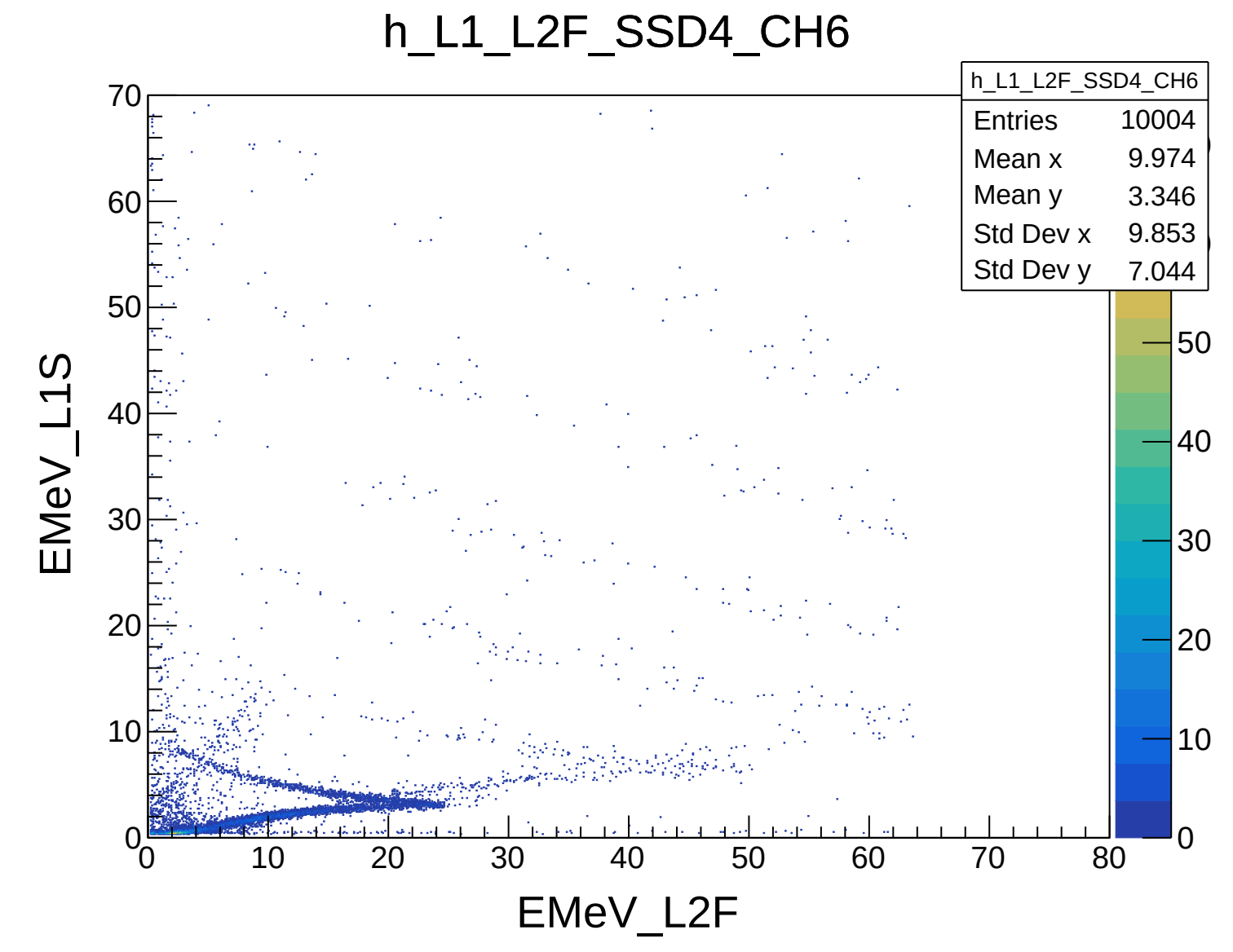

h_L1_L2F_SSD4_CH1
h_L1_L2F_SSD4_CH1
Entries 7799
Mean x 10.08
Mean y 3.137
Std Dev x 9.652
Std Dev y 6.227
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

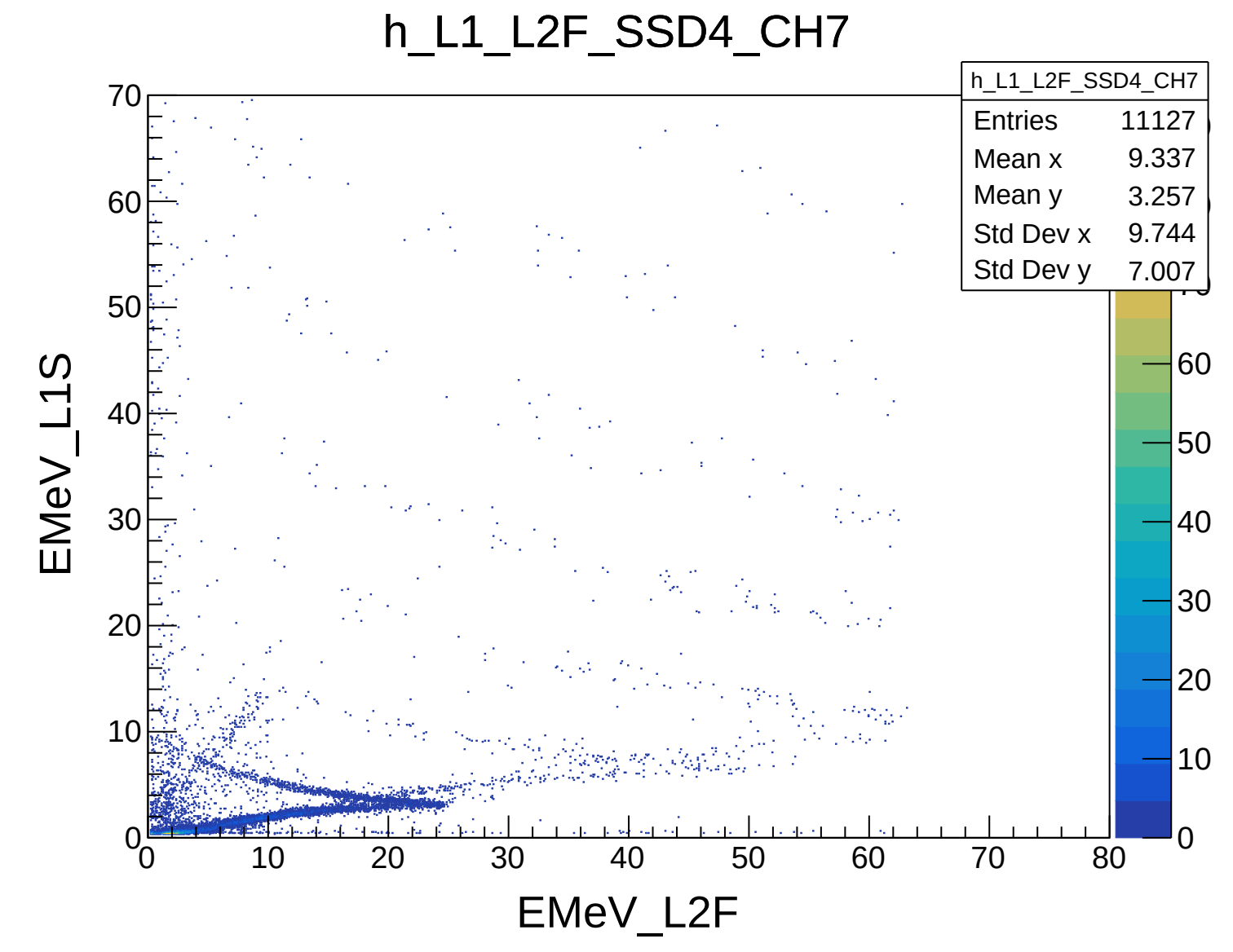

h_L1_L2F_SSD4_CH2
h_L1_L2F_SSD4_CH2
Entries 8802
Mean x 9.656
Mean y 3.164
Std Dev x 9.765
Std Dev y 6.741
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

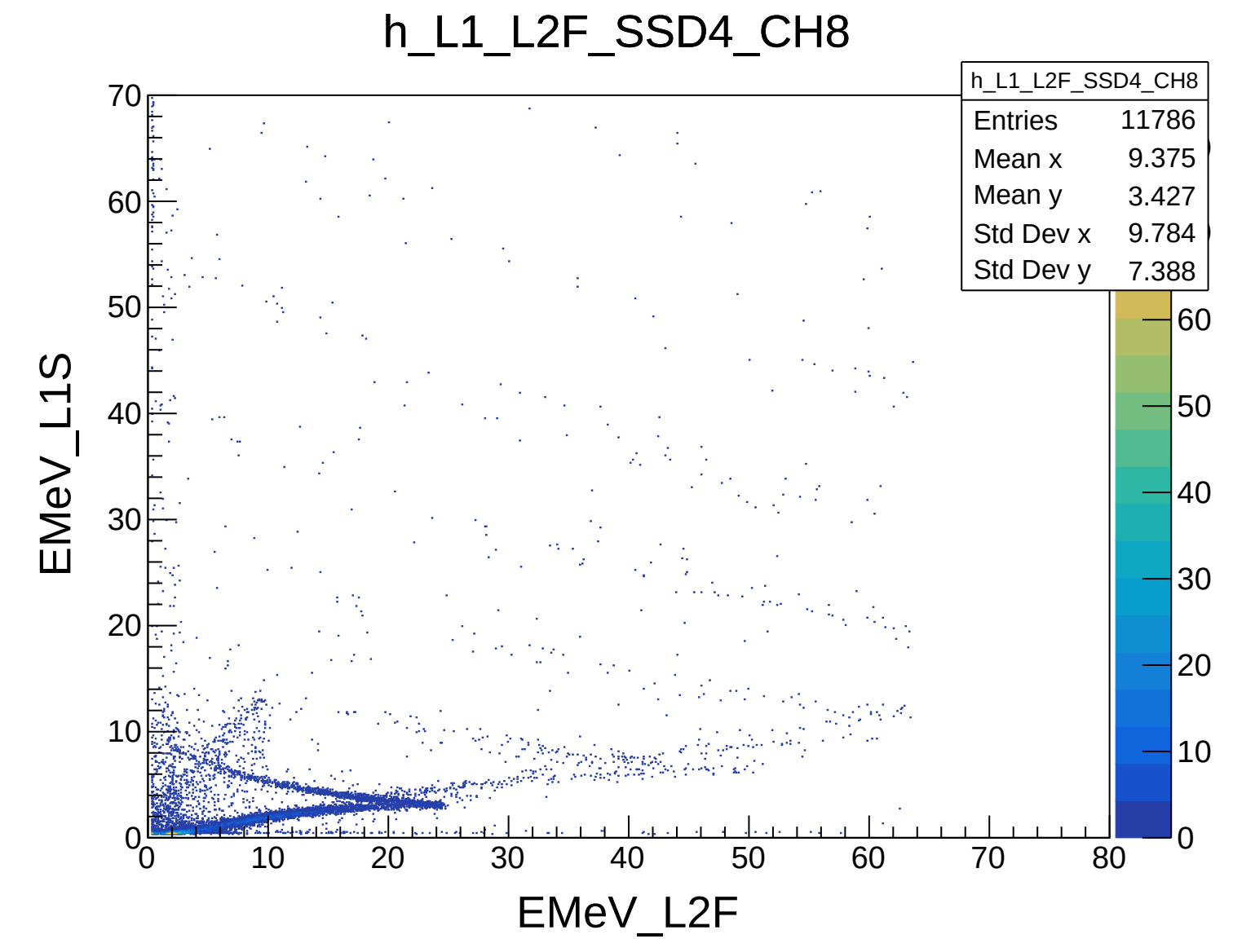

h_L1_L2F_SSD4_CH3
h_L1_L2F_SSD4_CH3
Entries 9090
Mean x 9.763
Mean y 3.267
Std Dev x 10.06
Std Dev y 6.897
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

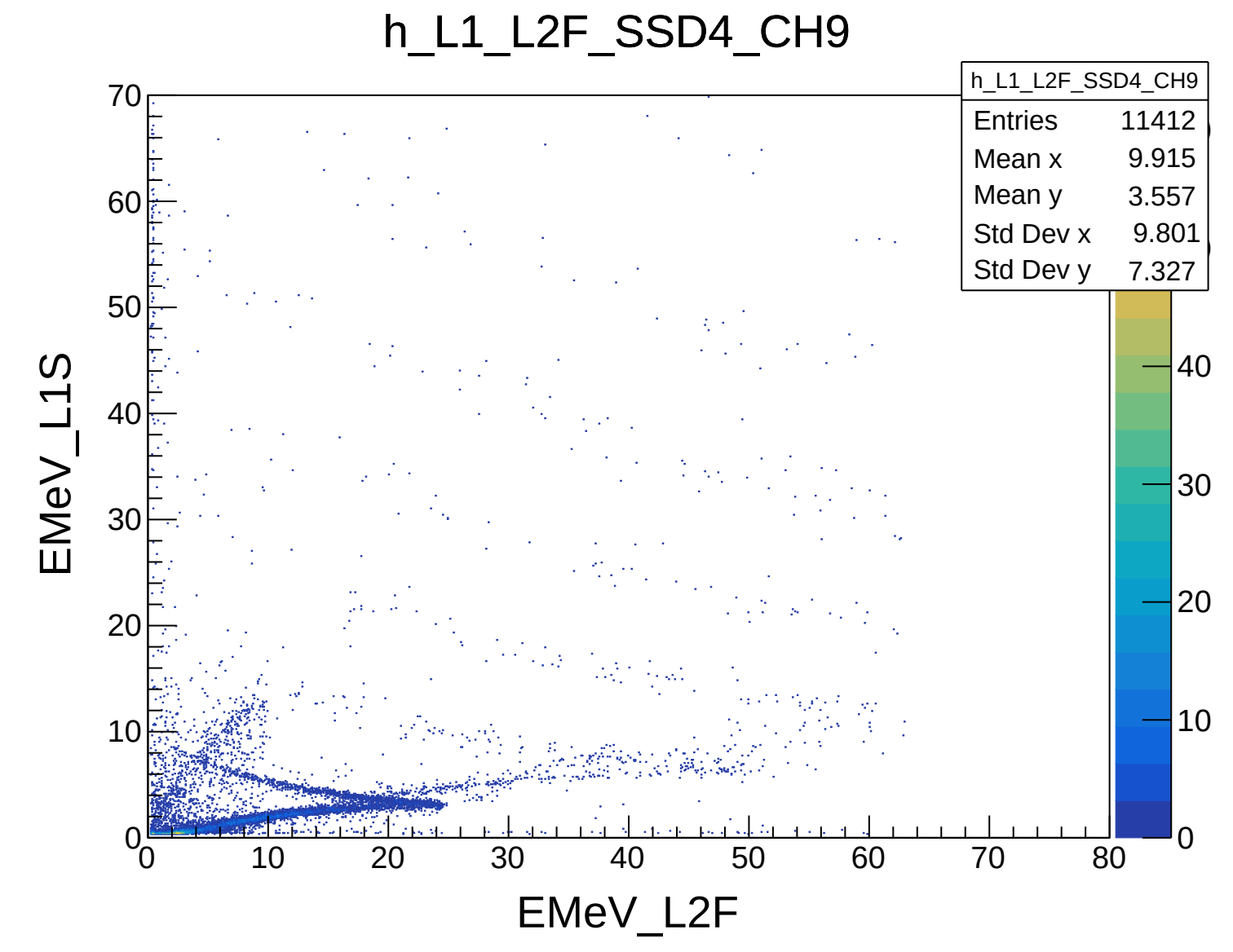

h_L1_L2F_SSD4_CH4
h_L1_L2F_SSD4_CH4
Entries 9596
Mean x 9.702
Mean y 3.384
Std Dev x 9.791
Std Dev y 7.349
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

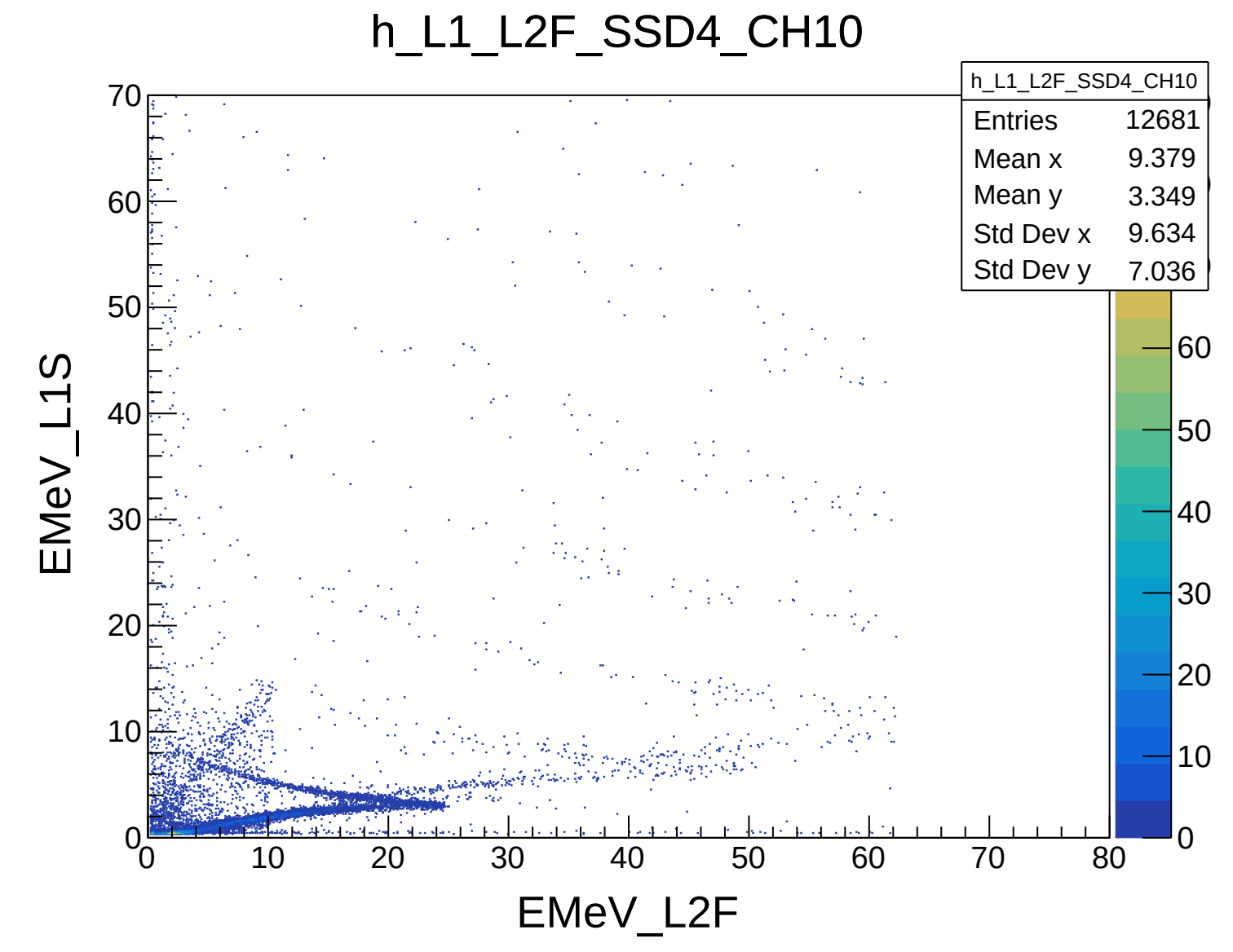

h_L1_L2F_SSD4_CH5
h_L1_L2F_SSD4_CH5
Entries 9308
Mean x 10.19
Mean y 3.343
Std Dev x 10.04
Std Dev y 6.851
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

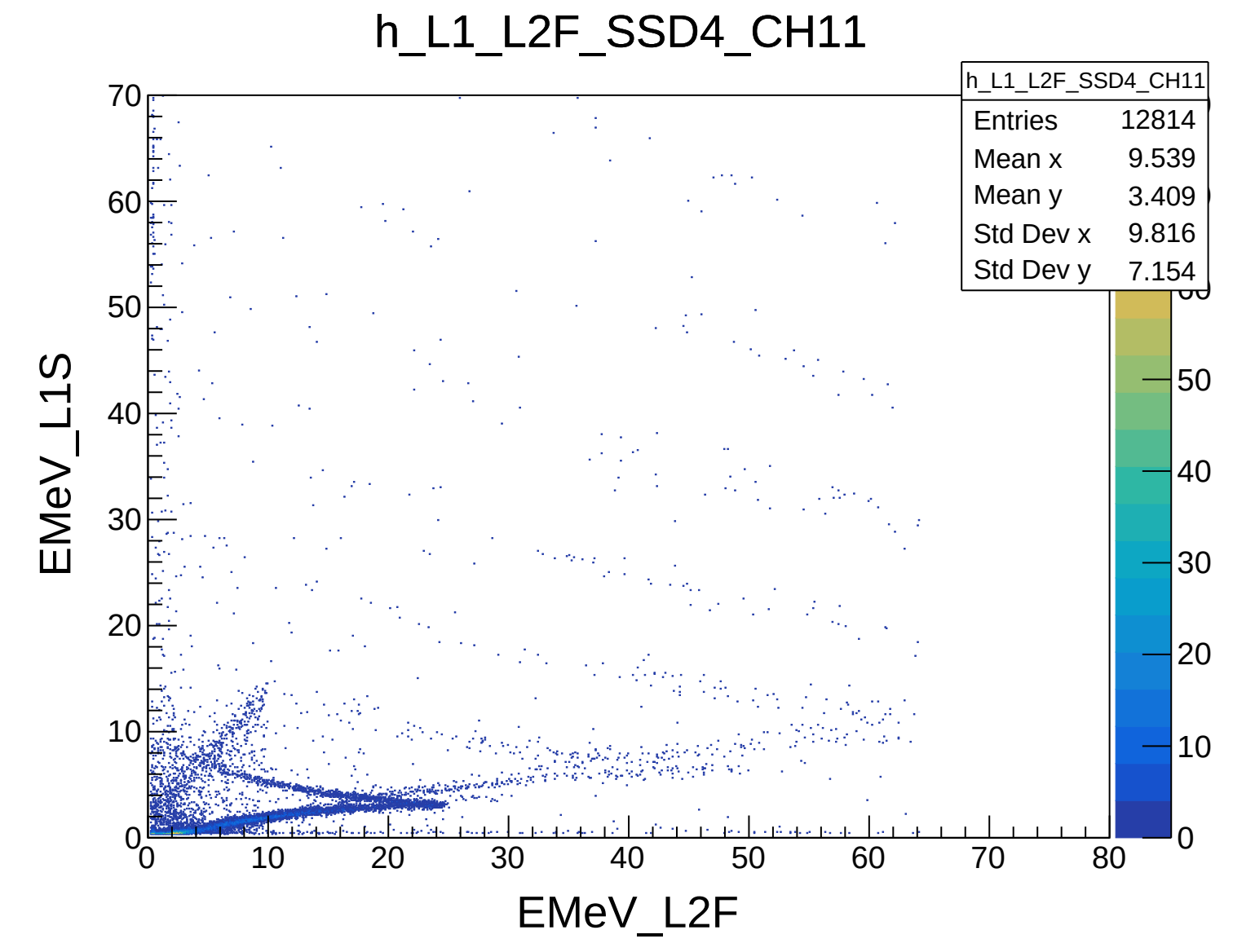

h_L1_L2F_SSD4_CH6
h_L1_L2F_SSD4_CH6
Entries 10004
Mean x 9.974
Mean y 3.346
Std Dev x 9.853
Std Dev y 7.044
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

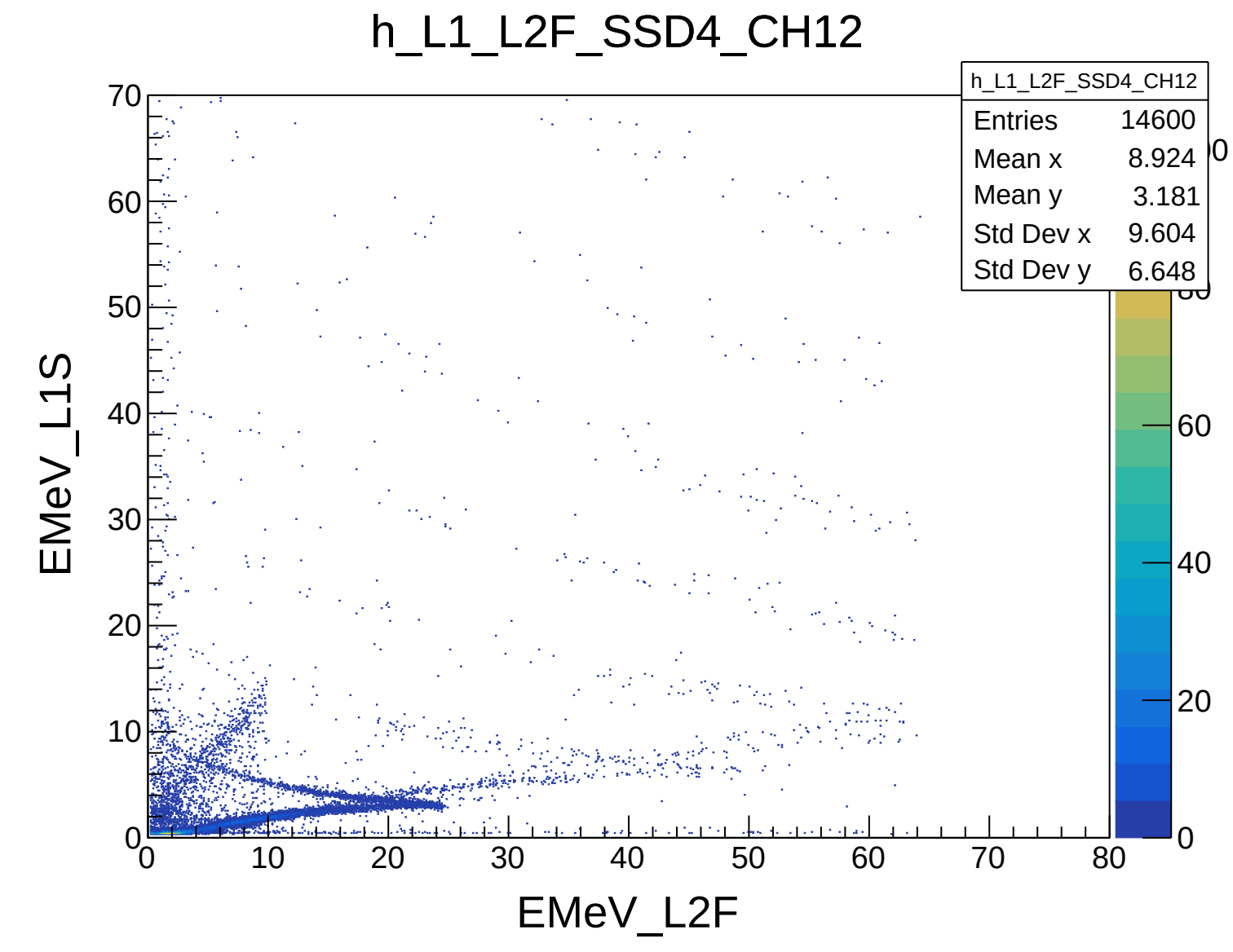

h_L1_L2F_SSD4_CH7
h_L1_L2F_SSD4_CH7
Entries 11127
Mean x 9.337
Mean y 3.257
Std Dev x 9.744
Std Dev y 7.007
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

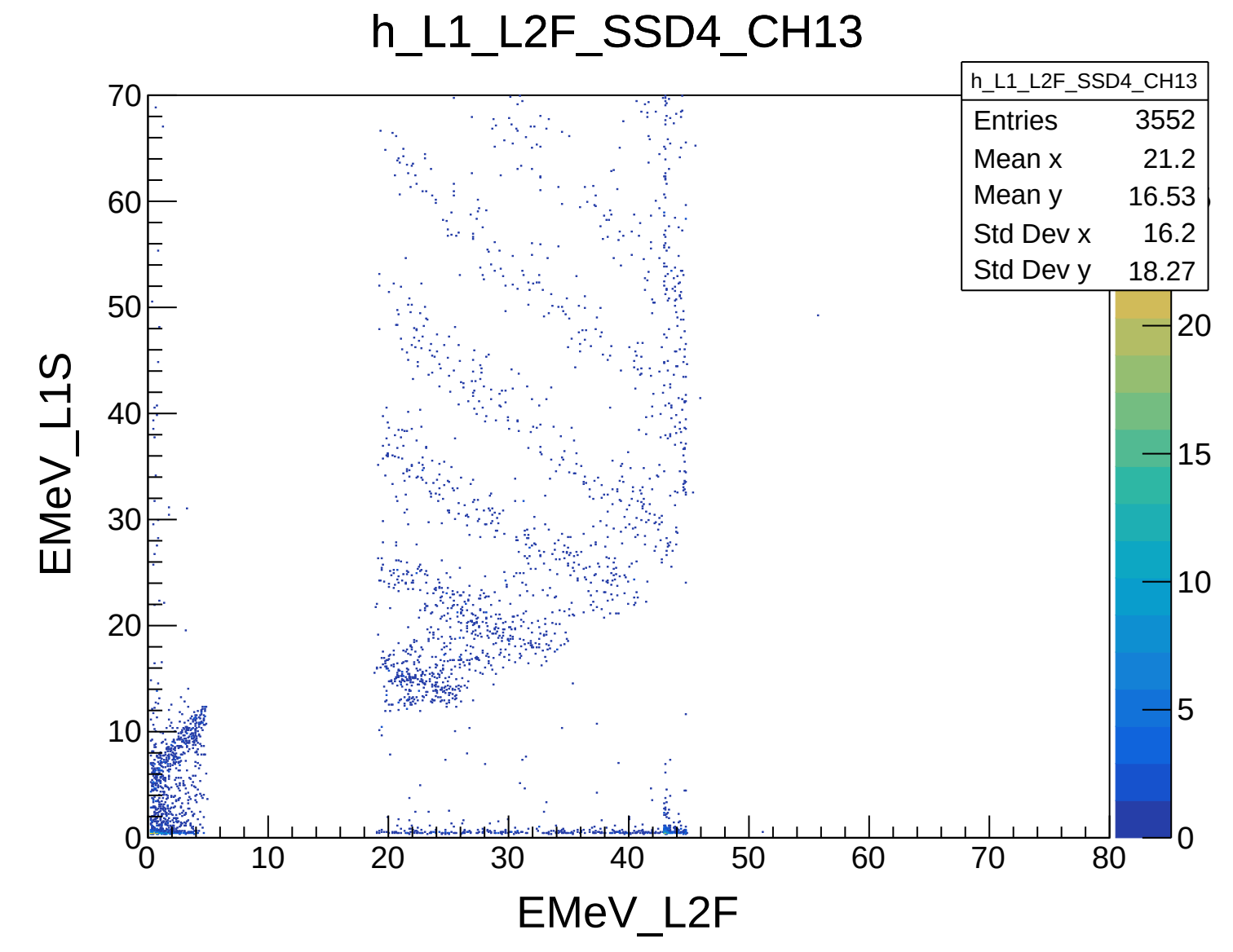

h_L1_L2F_SSD4_CH8
h_L1_L2F_SSD4_CH8
Entries 11786
Mean x 9.375
Mean y 3.427
Std Dev x 9.784
Std Dev y 7.388
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

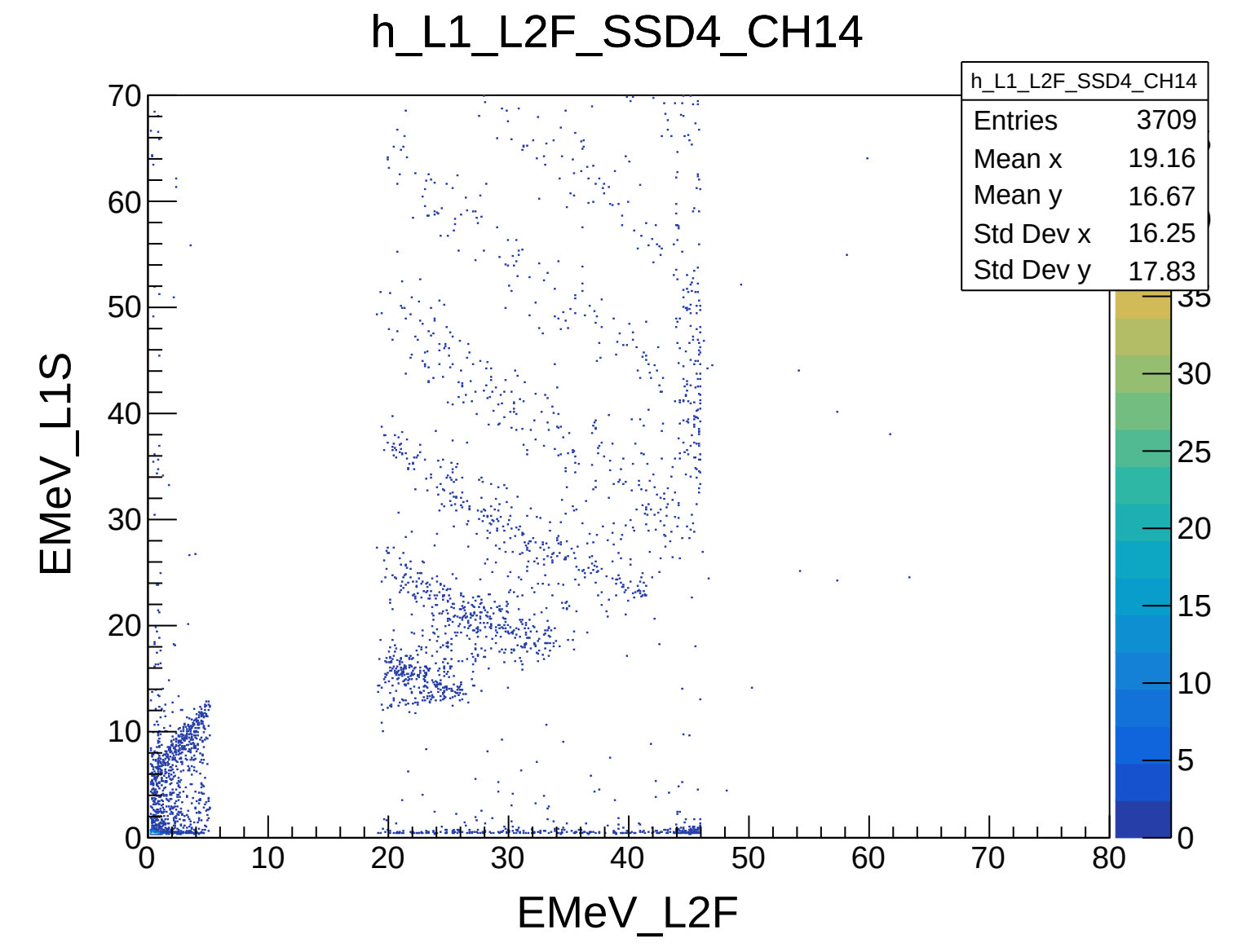

h_L1_L2F_SSD4_CH9
h_L1_L2F_SSD4_CH9
Entries 11412
Mean x 9.915
Mean y 3.557
Std Dev x 9.801
Std Dev y 7.327
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80

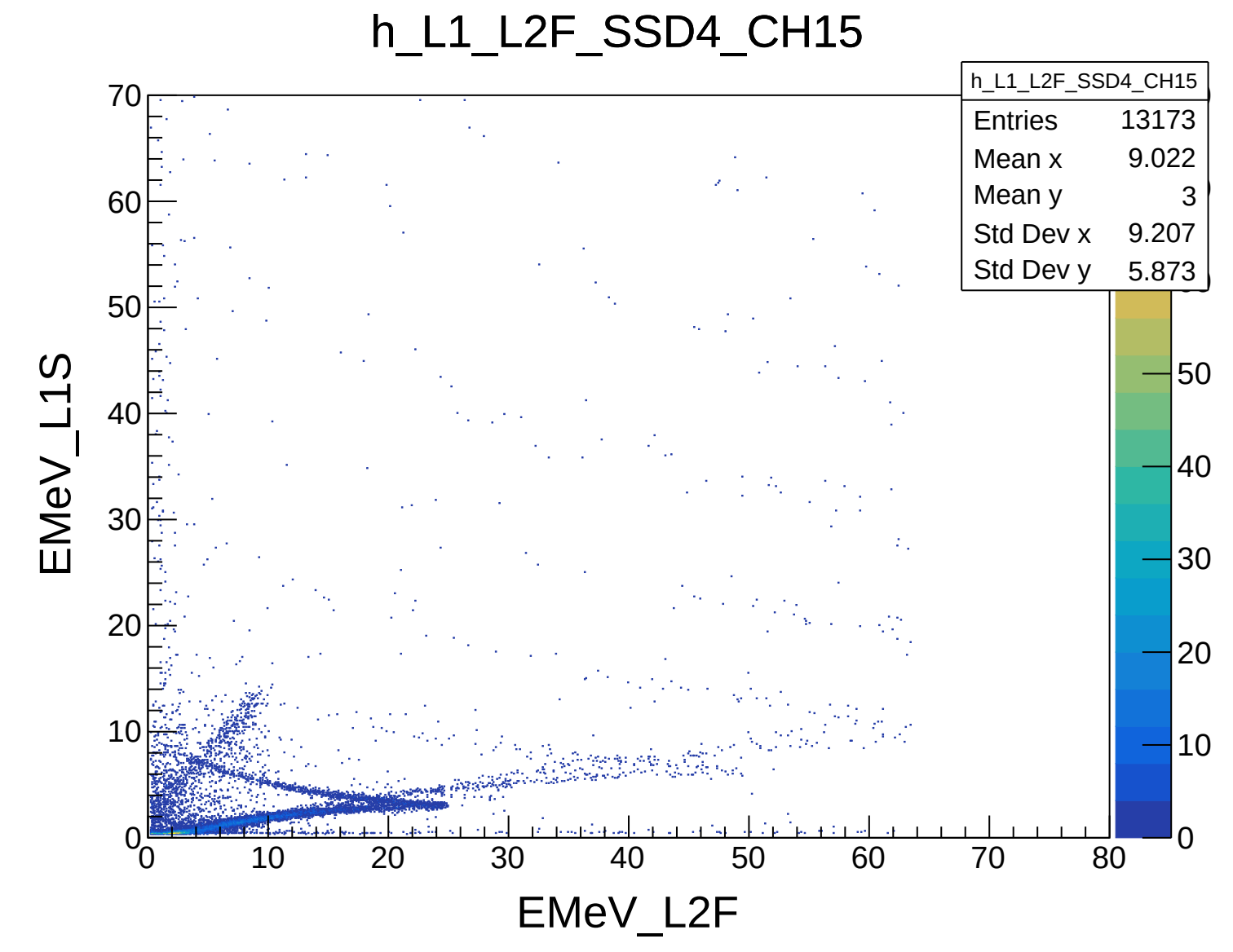

h_L1_L2F_SSD4_CH10
h_L1_L2F_SSD4_CH10
Entries 12681
Mean x 9.379
Mean y 3.349
Std Dev x 9.634
Std Dev y 7.036
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80


h_L1_L2F_SSD4_CH11
h_L1_L2F_SSD4_CH11
Entries 12814
Mean x 9.539
Mean y 3.409
Std Dev x 9.816
Std Dev y 7.154
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80


h_L1_L2F_SSD4_CH12
h_L1_L2F_SSD4_CH12
Entries 14600
Mean x 8.924
Mean y 3.181
Std Dev x 9.604
Std Dev y 6.648
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80


h_L1_L2F_SSD4_CH13
h_L1_L2F_SSD4_CH13
Entries 3552
Mean x 21.2
Mean y 16.53
Std Dev x 16.2
Std Dev y 18.27
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
5
15


h_L1_L2F_SSD4_CH14
h_L1_L2F_SSD4_CH14
Entries 3709
Mean x 19.16
Mean y 16.67
Std Dev x 16.25
Std Dev y 17.83
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80
5
35


h_L1_L2F_SSD4_CH15
h_L1_L2F_SSD4_CH15
Entries 13173
Mean x 9.022
Mean y 3
Std Dev x 9.207
Std Dev y 5.873
EMeV_L1S
EMeV_L2F
0
10
20
30
40
50
60
70
80