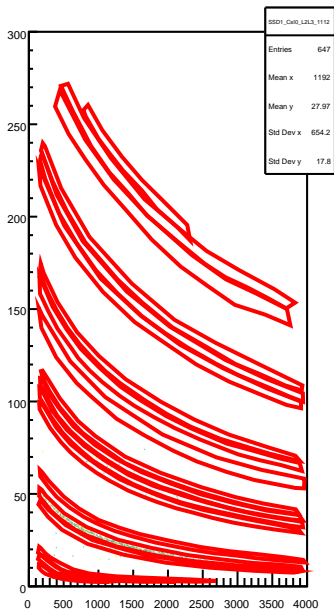
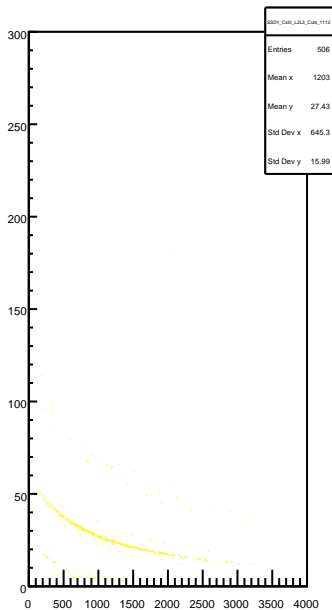


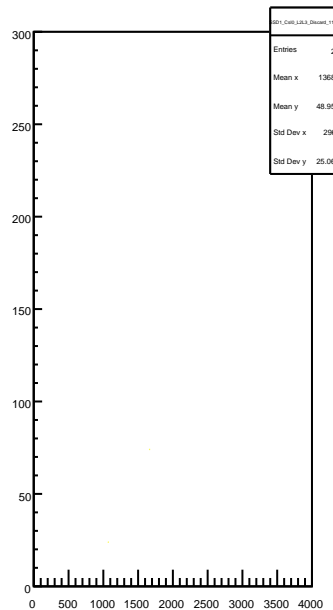
SSD1_CsI0_L2L3_1112



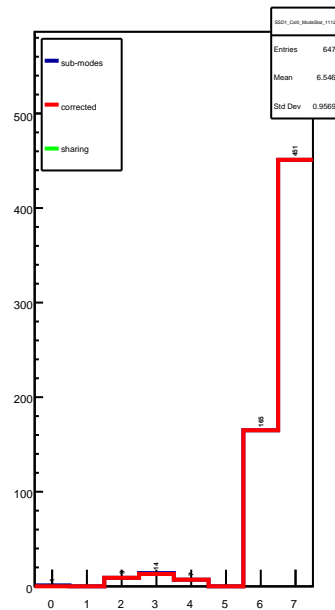
SSD1_CsI0_L2L3_Cuts_1112



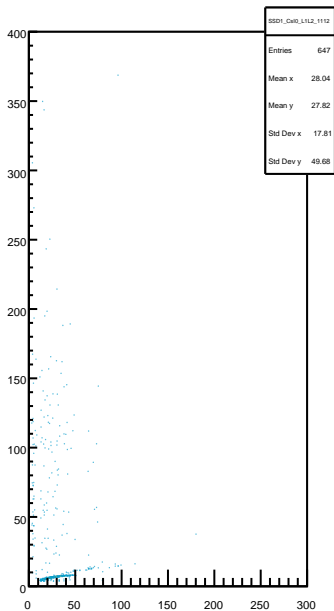
SSD1_CsI0_L2L3_Discard_1112



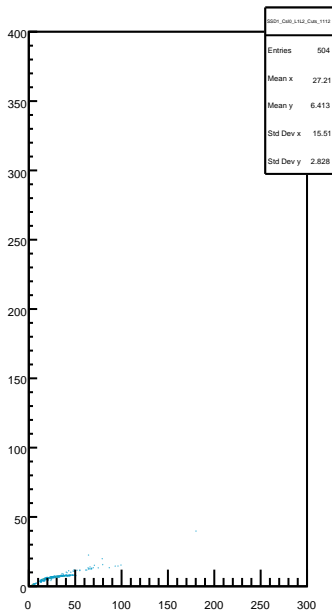
SSD1_CsI0_ModeStat_1112



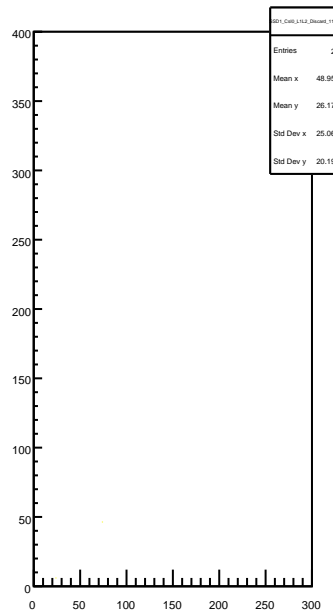
SSD1_CsI0_L1L2_1112



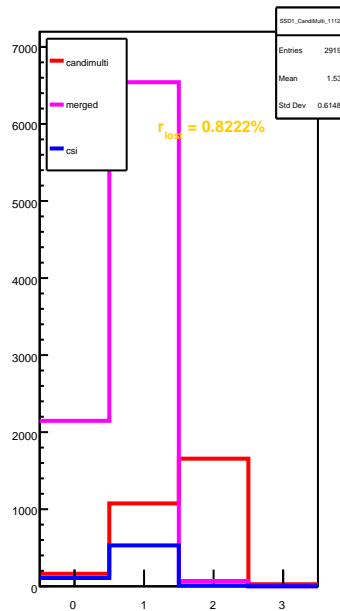
SSD1_CsI0_L1L2_Cuts_1112



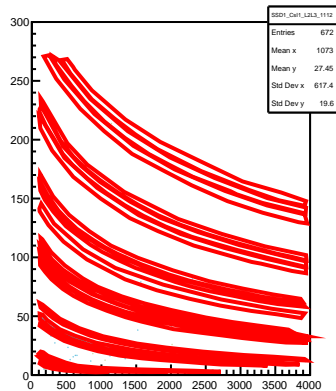
SSD1_CsI0_L1L2_Discard_1112



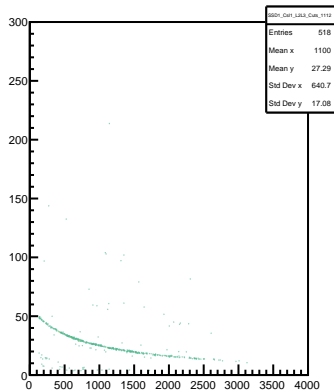
SSD1_CandiMulti_1112



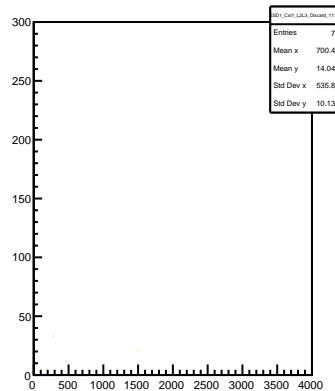
SSD1_Cs1_L2L3_1112



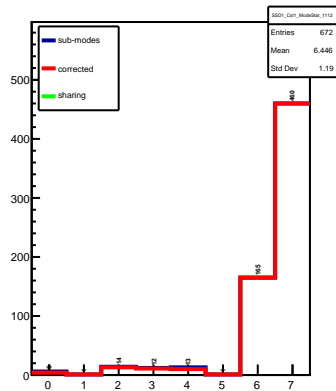
SSD1_Cs1_L2L3_Cuts_1112



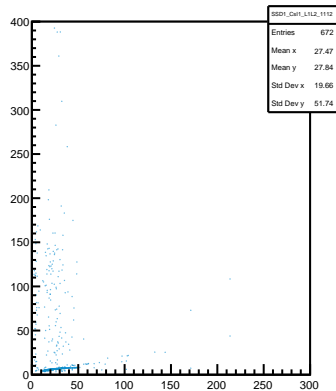
SSD1_Cs1_L2L3_Discard_1112



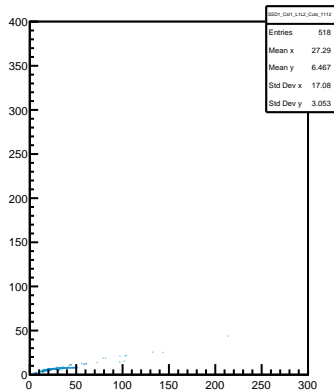
SSD1_Cs1_ModeStat_1112



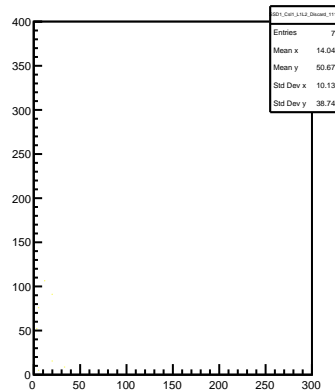
SSD1_Cs1_L1L2_1112



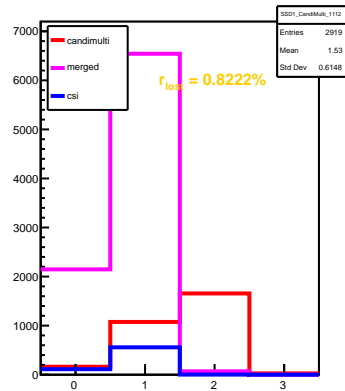
SSD1_Cs1_L1L2_Cuts_1112



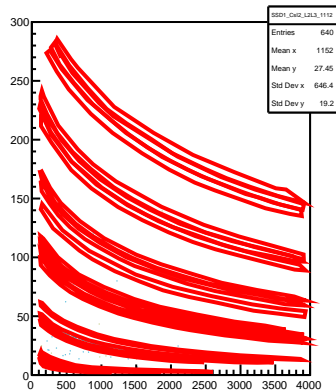
SSD1_Cs1_L1L2_Discard_1112



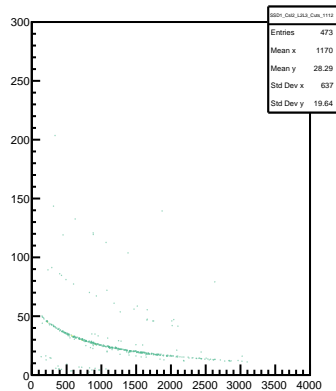
SSD1_CandiMulti_1112



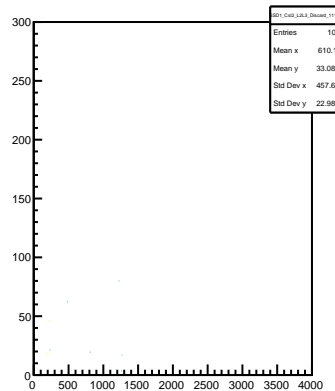
SSD1_CsI2_L2L3_1112



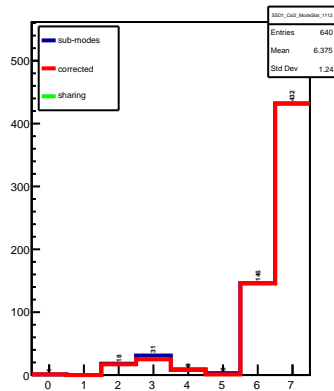
SSD1_CsI2_L2L3_Cuts_1112



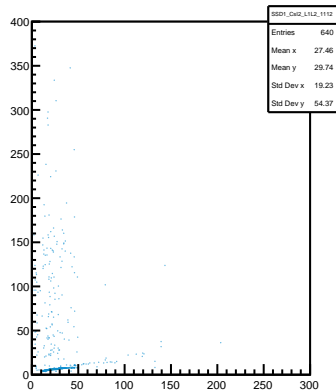
SSD1_CsI2_L2L3_Discard_1112



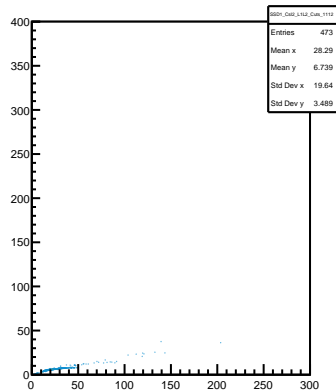
SSD1_CsI2_ModeStat_1112



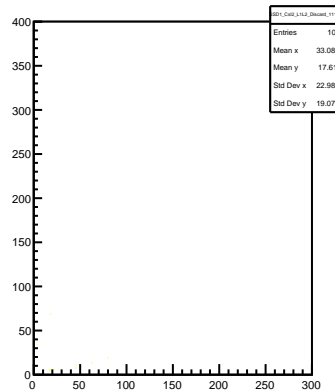
SSD1_CsI2_L1L2_1112



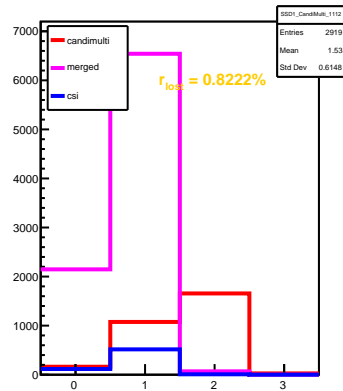
SSD1_CsI2_L1L2_Cuts_1112



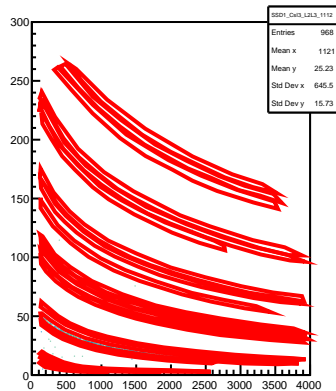
SSD1_CsI2_L1L2_Discard_1112



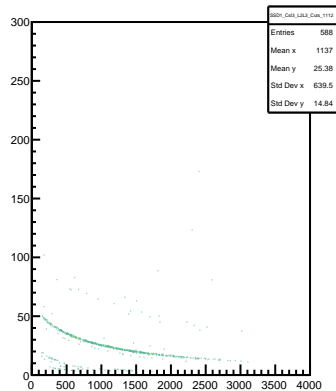
SSD1_CandiMulti_1112



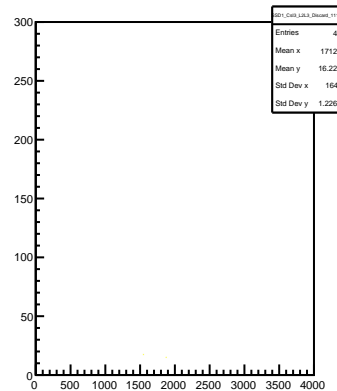
SSD1_Csl3_L2L3_1112



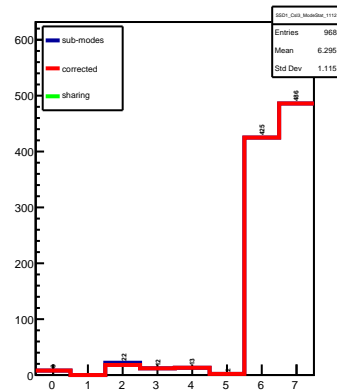
SSD1_Csl3_L2L3_Cuts_1112



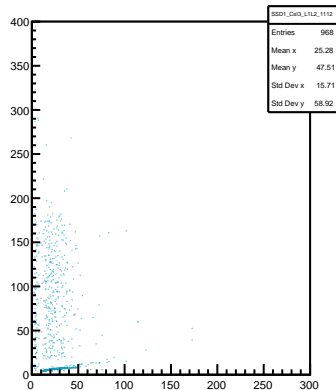
SSD1_Csl3_L2L3_Discard_1112



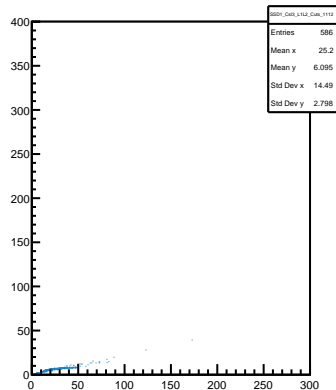
SSD1_Csl3_ModeStat_1112



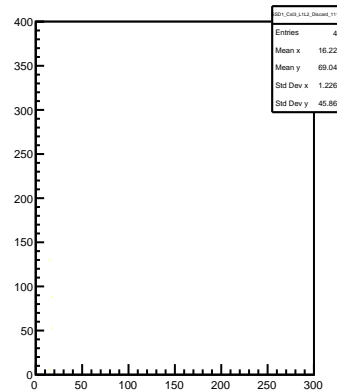
SSD1_Csl3_L1L2_1112



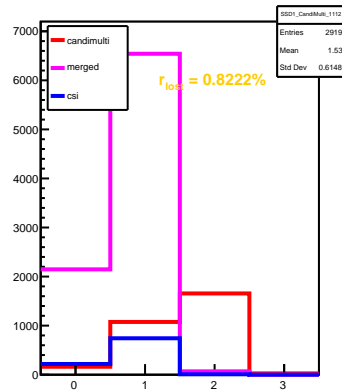
SSD1_Csl3_L1L2_Cuts_1112



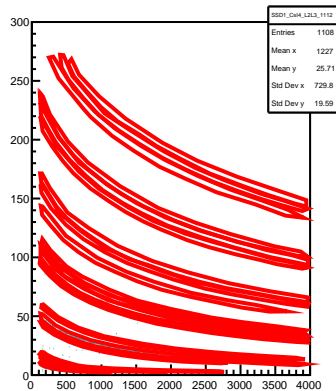
SSD1_Csl3_L1L2_Discard_1112



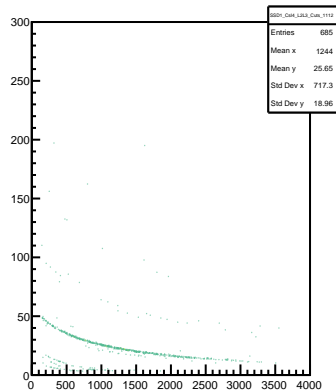
SSD1_CandiMulti_1112



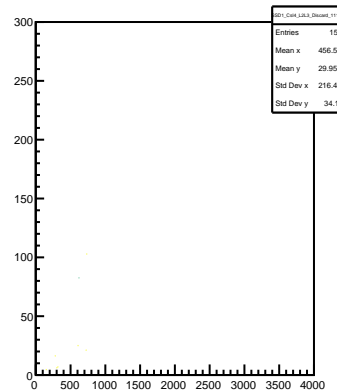
SSD1_Csl4_L2L3_1112



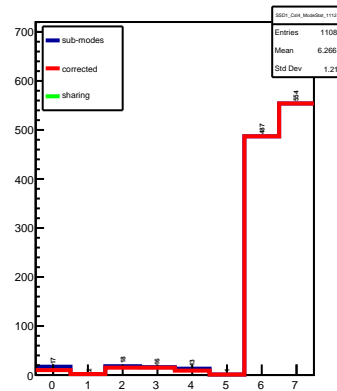
SSD1_Csl4_L2L3_Cuts_1112



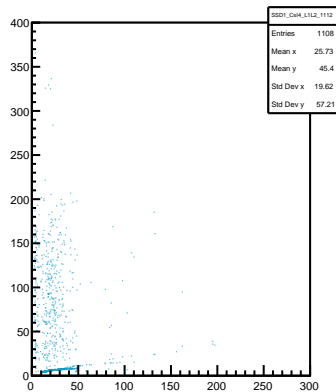
SSD1_Csl4_L2L3_Discard_1112



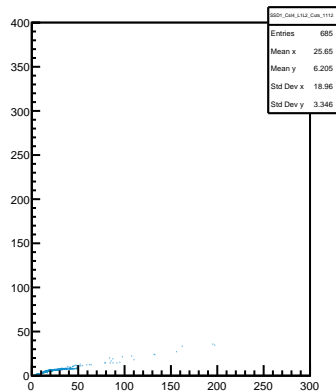
SSD1_Csl4_ModeStat_1112



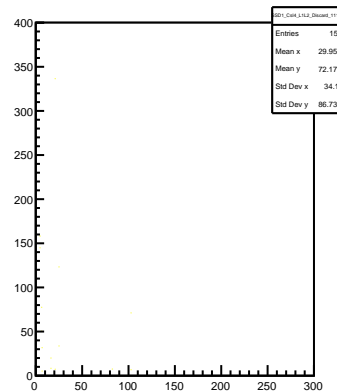
SSD1_Csl4_L1L2_1112



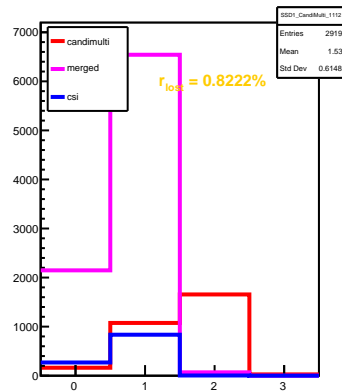
SSD1_Csl4_L1L2_Cuts_1112



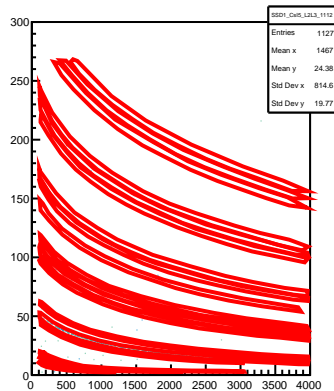
SSD1_Csl4_L1L2_Discard_1112



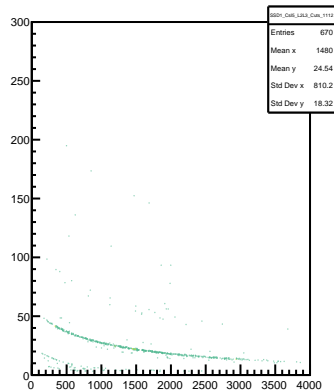
SSD1_CandiMulti_1112



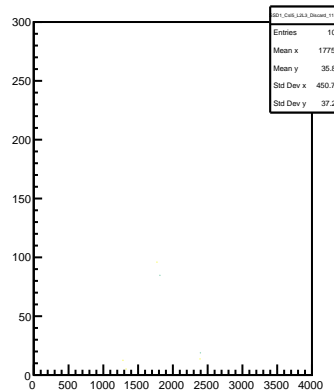
SSD1_Csl5_L2L3_1112



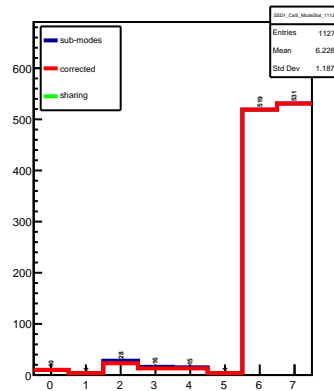
SSD1_Csl5_L2L3_Cuts_1112



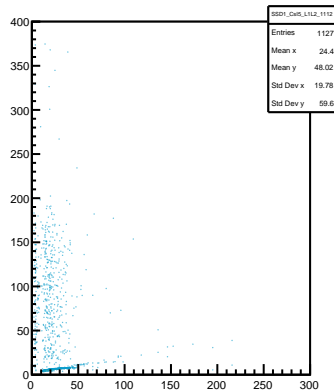
SSD1_Csl5_L2L3_Discard_1112



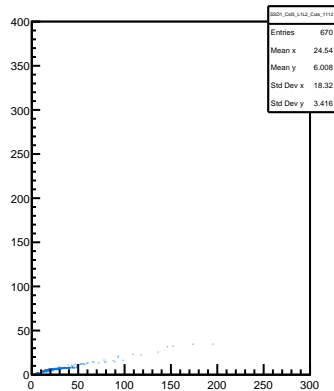
SSD1_Csl5_ModeStat_1112



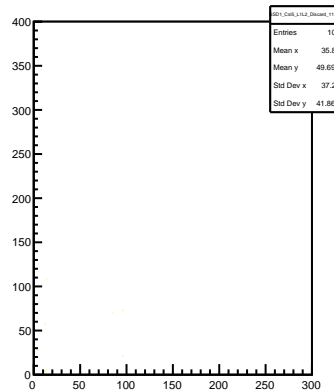
SSD1_Csl5_L1L2_1112



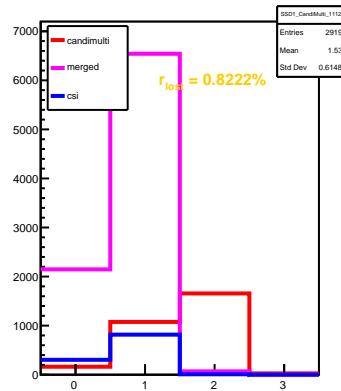
SSD1_Csl5_L1L2_Cuts_1112



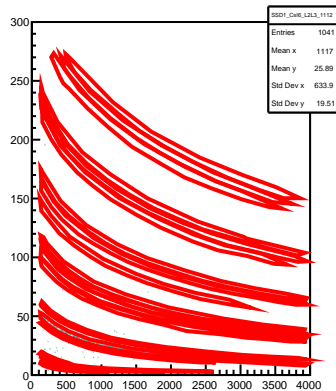
SSD1_Csl5_L1L2_Discard_1112



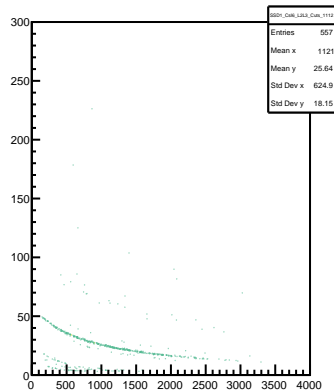
SSD1_CandiMulti_1112



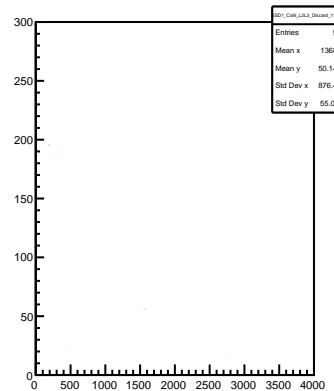
SSD1_Csl6_L2L3_1112



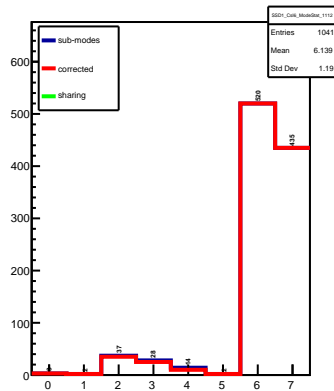
SSD1_Csl6_L2L3_Cuts_1112



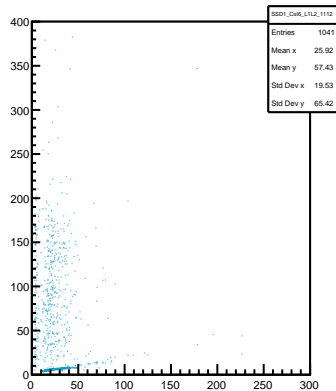
SSD1_Csl6_L2L3_Discard_1112



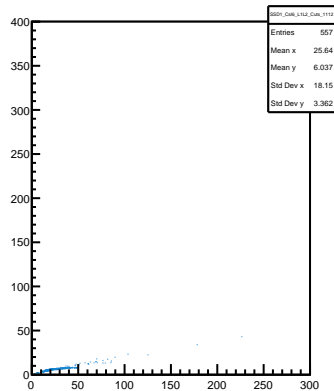
SSD1_Csl6_ModeStat_1112



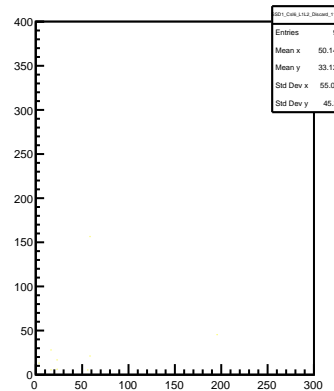
SSD1_Csl6_L1L2_1112



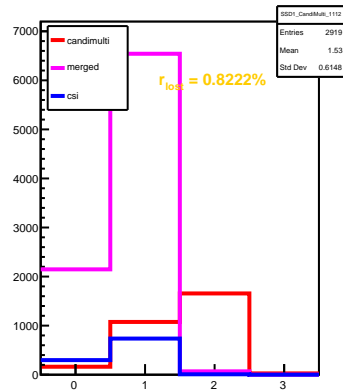
SSD1_Csl6_L1L2_Cuts_1112



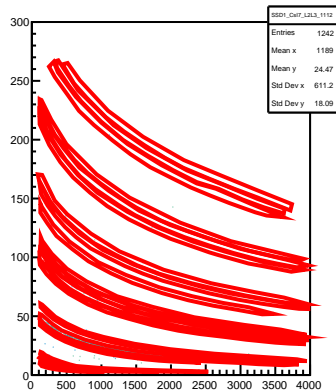
SSD1_Csl6_L1L2_Discard_1112



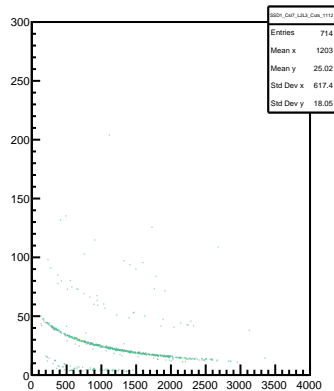
SSD1_CandiMulti_1112



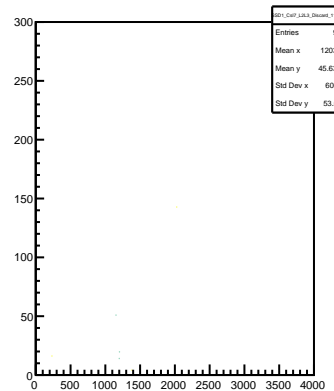
SSD1_Csl7_L2L3_1112



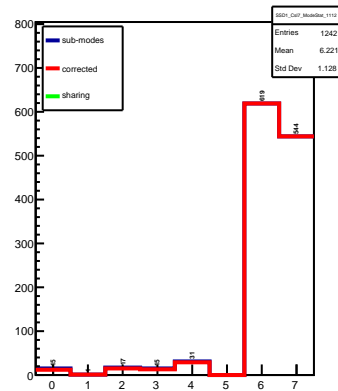
SSD1_Csl7_L2L3_Cuts_1112



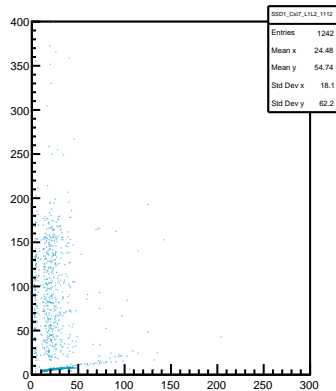
SSD1_Csl7_L2L3_Discard_1112



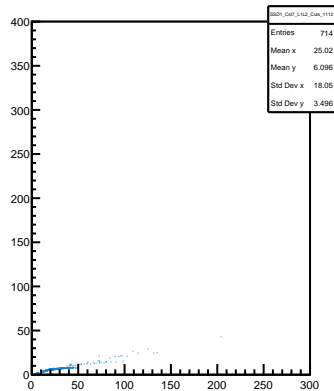
SSD1_Csl7_ModeStat_1112



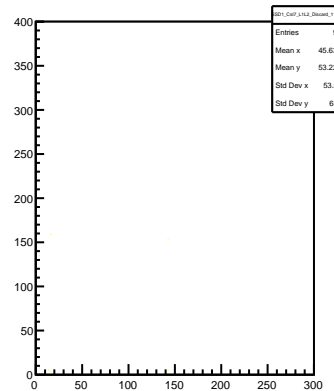
SSD1_Csl7_L1L2_1112



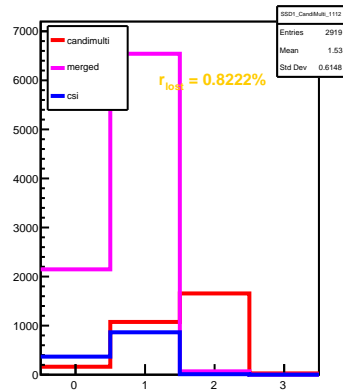
SSD1_Csl7_L1L2_Cuts_1112



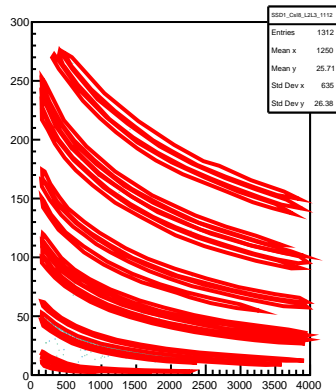
SSD1_Csl7_L1L2_Discard_1112



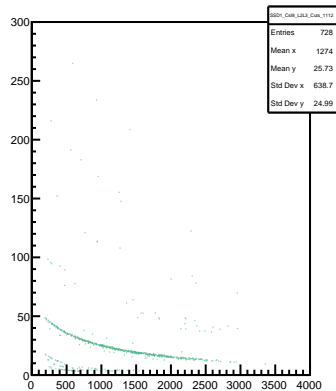
SSD1_CandiMulti_1112



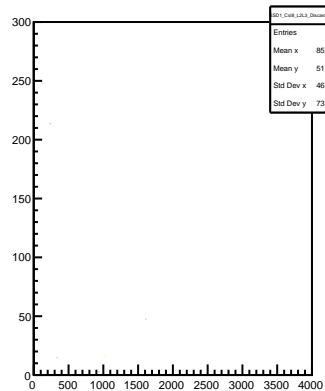
SSD1_Csl8_L2L3_1112



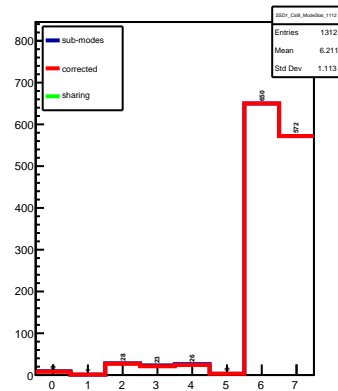
SSD1_Csl8_L2L3_Cuts_1112



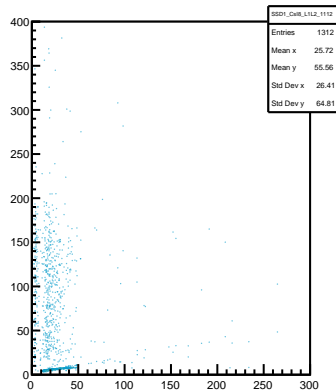
SSD1_Csl8_L2L3_Discard_1112



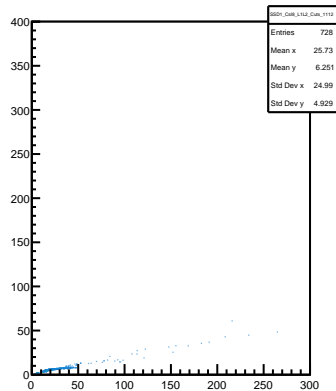
SSD1_Csl8_ModeStat_1112



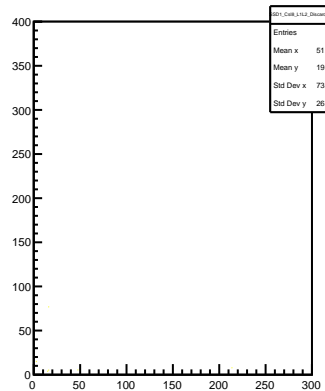
SSD1_Csl8_L1L2_1112



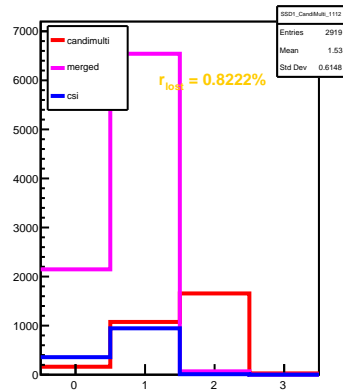
SSD1_Csl8_L1L2_Cuts_1112



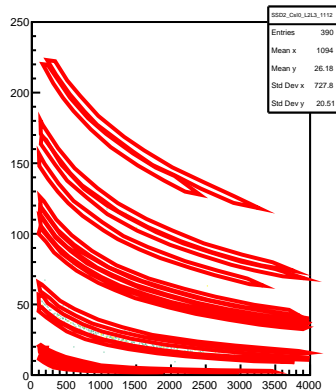
SSD1_Csl8_L1L2_Discard_1112



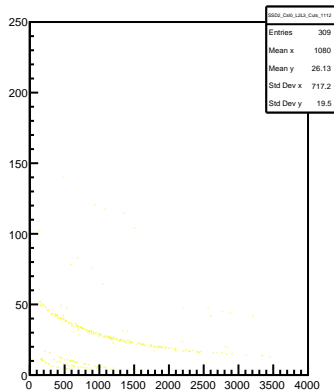
SSD1_CandiMulti_1112



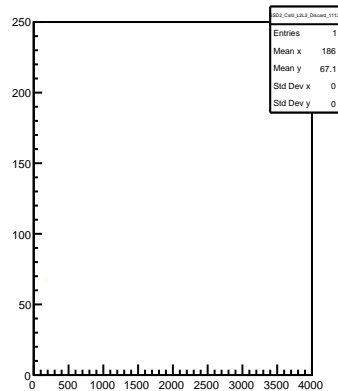
SSD2_Csl0_L2L3_1112



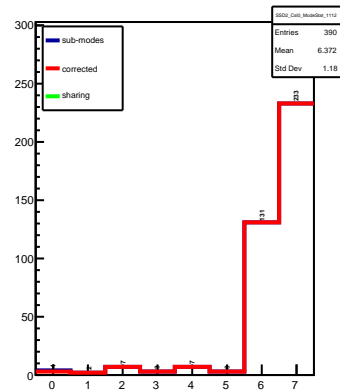
SSD2_Csl0_L2L3_Cuts_1112



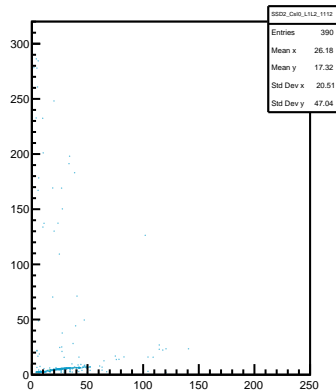
SSD2_Csl0_L2L3_Discard_1112



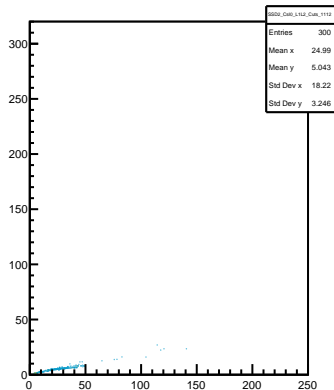
SSD2_Csl0_ModeStat_1112



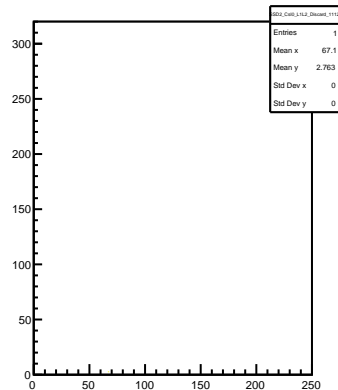
SSD2_Csl0_L1L2_1112



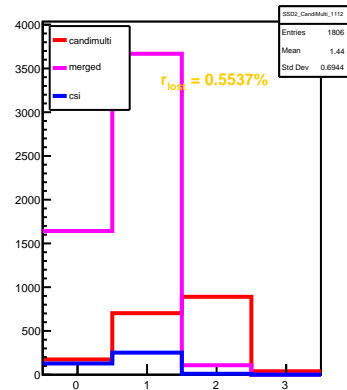
SSD2_Csl0_L1L2_Cuts_1112



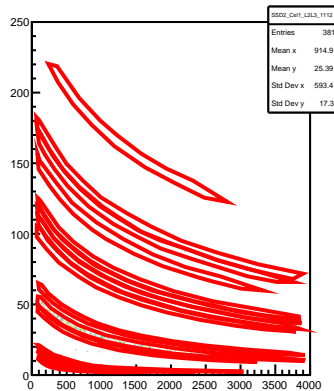
SSD2_Csl0_L1L2_Discard_1112



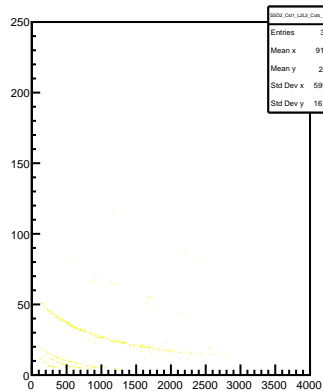
SSD2_CandiMulti_1112



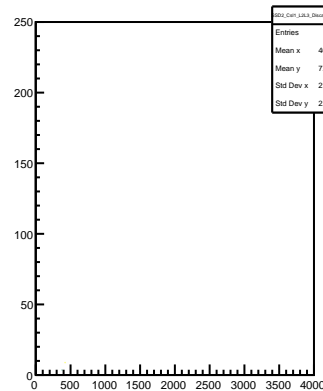
SSD2_Csl1_L2L3_1112



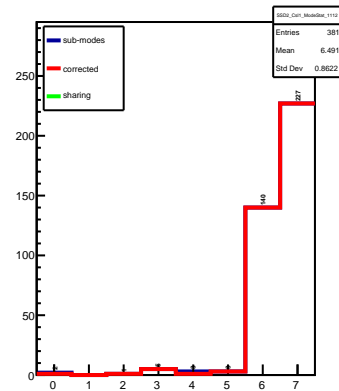
SSD2_Csl1_L2L3_Cuts_1112



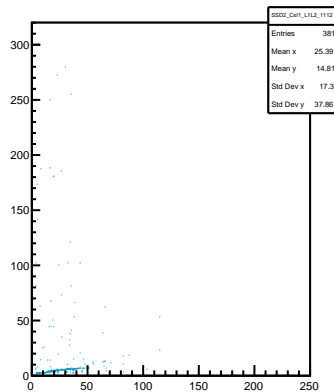
SSD2_Csl1_L2L3_Discard_1112



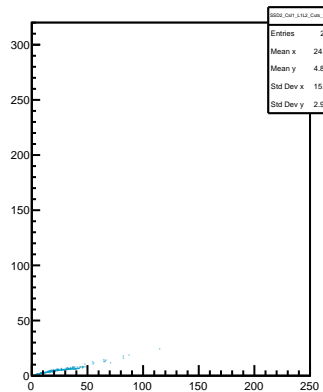
SSD2_Csl1_ModeStat_1112



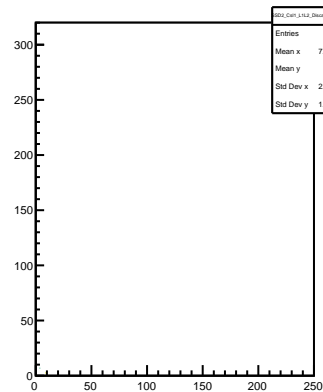
SSD2_Csl1_L1L2_1112



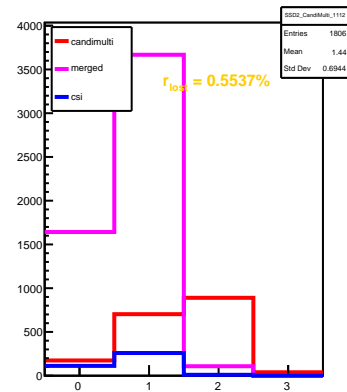
SSD2_Csl1_L1L2_Cuts_1112



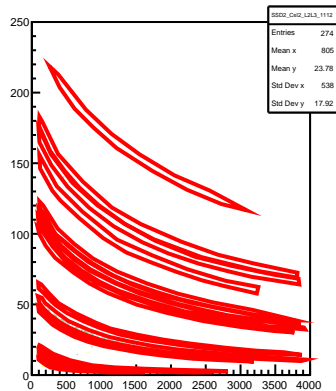
SSD2_Csl1_L1L2_Discard_1112



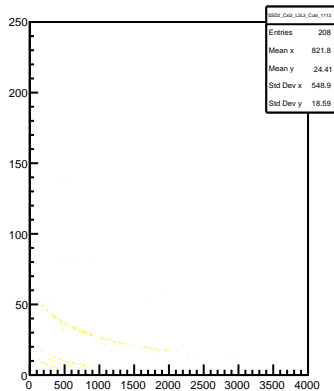
SSD2_CandiMulti_1112



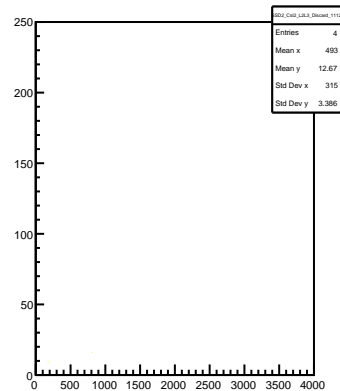
SSD2_CsI2_L2L3_1112



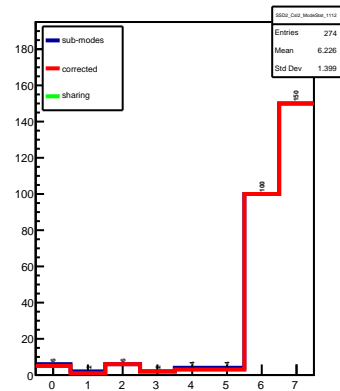
SSD2_CsI2_L2L3_Cuts_1112



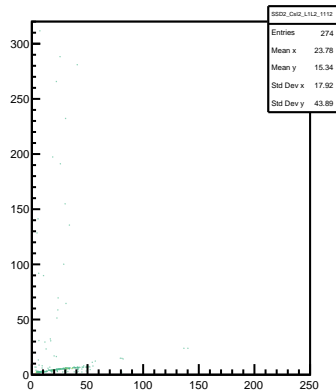
SSD2_CsI2_L2L3_Discard_1112



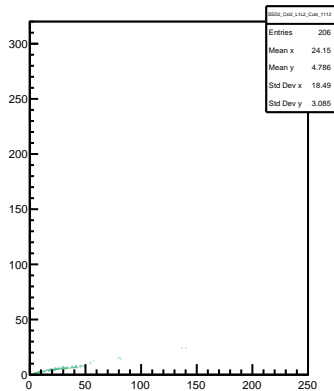
SSD2_CsI2_ModeStat_1112



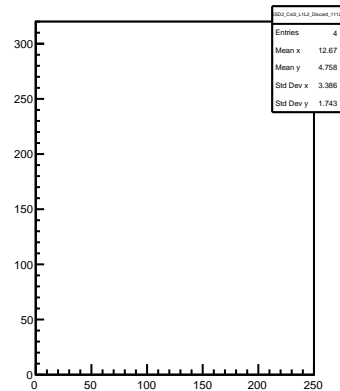
SSD2_CsI2_L1L2_1112



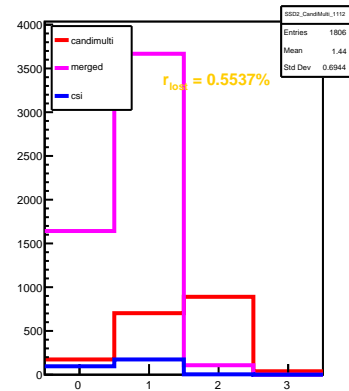
SSD2_CsI2_L1L2_Cuts_1112



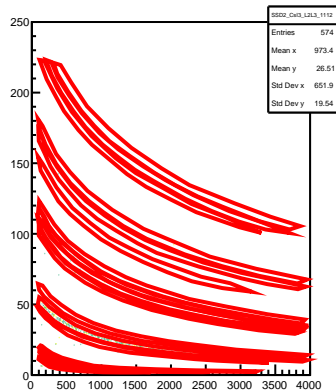
SSD2_CsI2_L1L2_Discard_1112



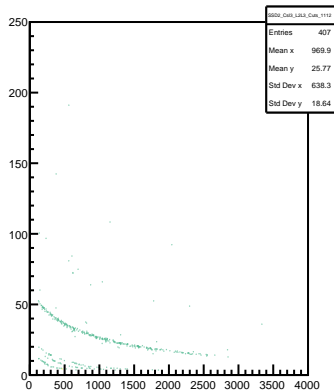
SSD2_CandiMulti_1112



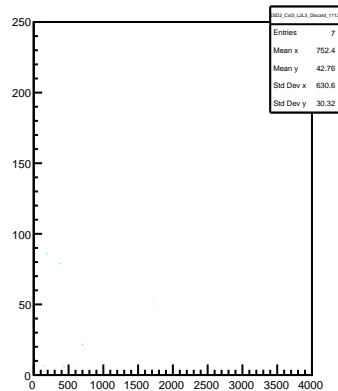
SSD2_Csl3_L2L3_1112



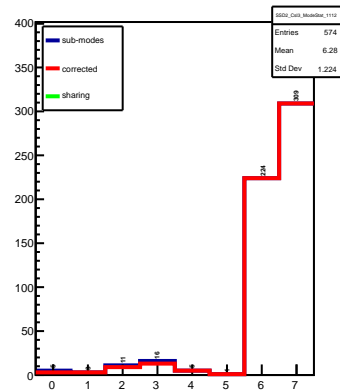
SSD2_Csl3_L2L3_Cuts_1112



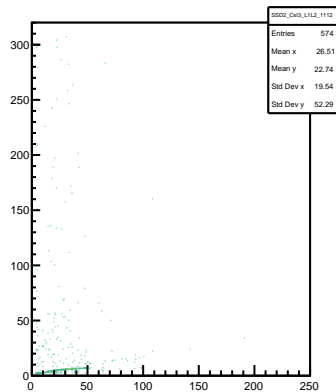
SSD2_Csl3_L2L3_Discard_1112



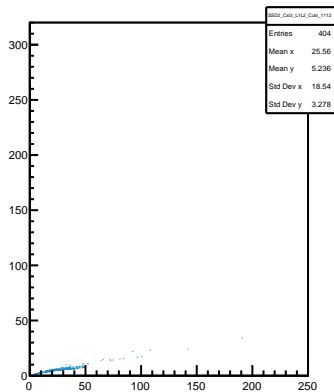
SSD2_Csl3_ModeStat_1112



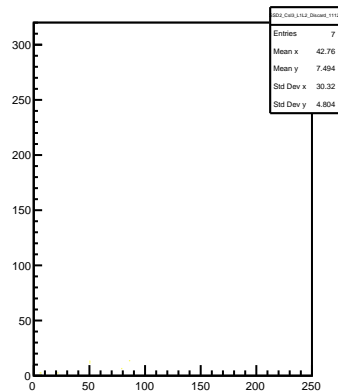
SSD2_Csl3_L1L2_1112



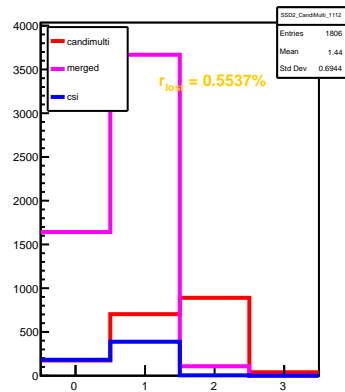
SSD2_Csl3_L1L2_Cuts_1112



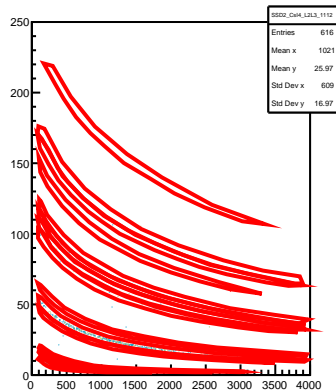
SSD2_Csl3_L1L2_Discard_1112



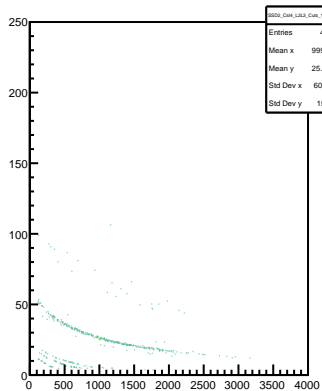
SSD2_CandiMulti_1112



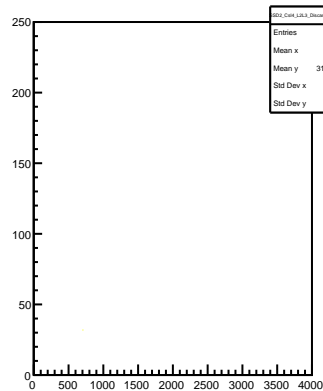
SSD2_Csl4_L2L3_1112



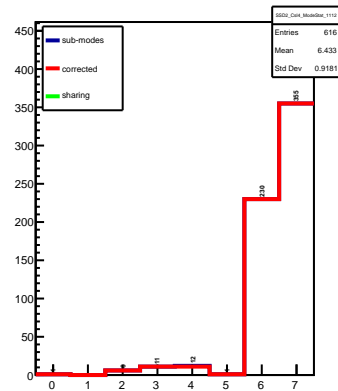
SSD2_Csl4_L2L3_Cuts_1112



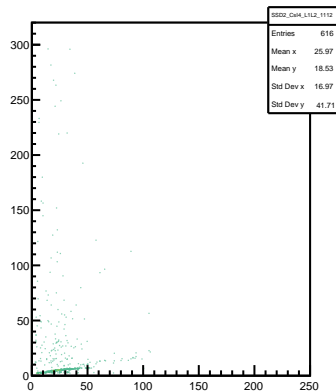
SSD2_Csl4_L2L3_Discard_1112



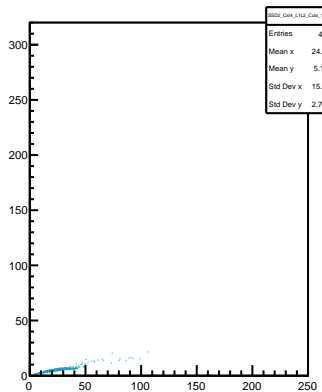
SSD2_Csl4_ModeStat_1112



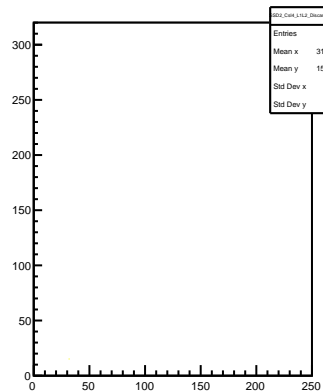
SSD2_Csl4_L1L2_1112



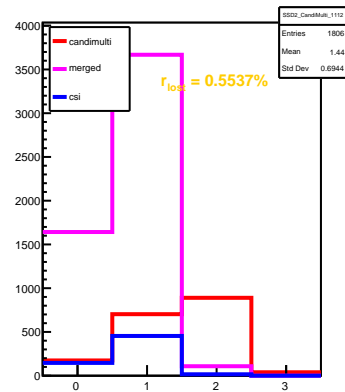
SSD2_Csl4_L1L2_Cuts_1112



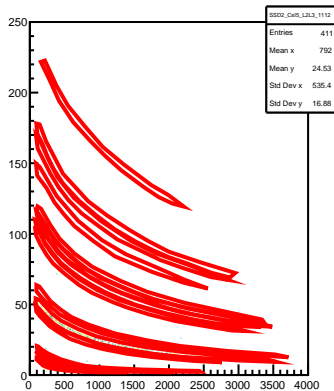
SSD2_Csl4_L1L2_Discard_1112



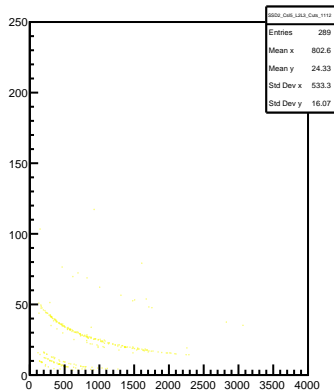
SSD2_CandiMulti_1112



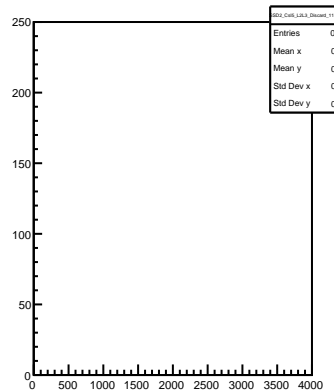
SSD2_Csl5_L2L3_1112



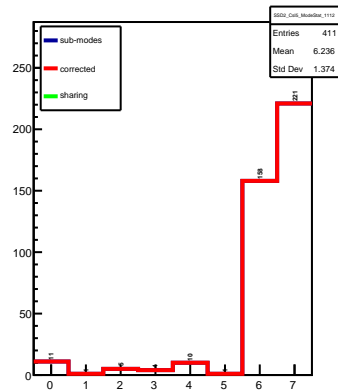
SSD2_Csl5_L2L3_Cuts_1112



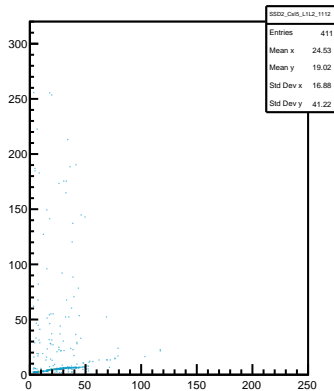
SSD2_Csl5_L2L3_Discard_1112



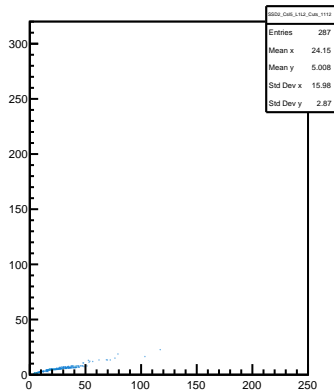
SSD2_Csl5_ModeStat_1112



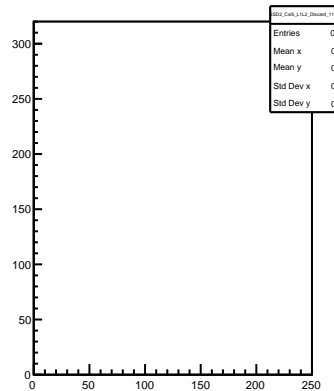
SSD2_Csl5_L1L2_1112



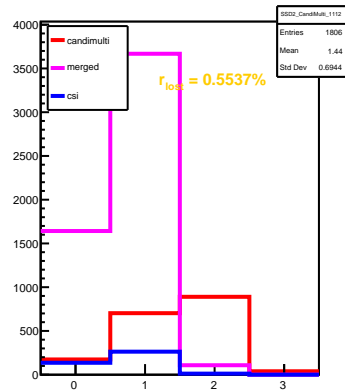
SSD2_Csl5_L1L2_Cuts_1112



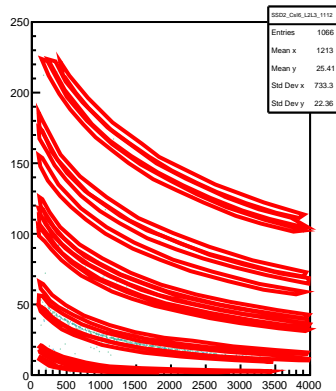
SSD2_Csl5_L1L2_Discard_1112



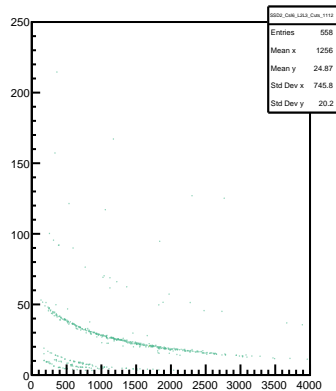
SSD2_CandiMulti_1112



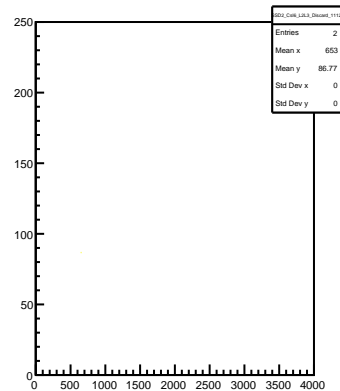
SSD2_Csl6_L2L3_1112



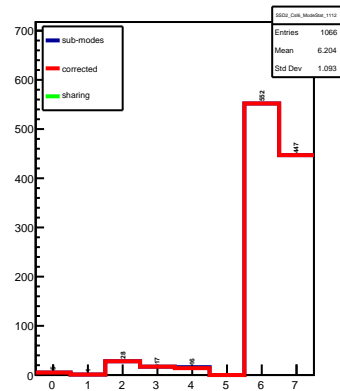
SSD2_Csl6_L2L3_Cuts_1112



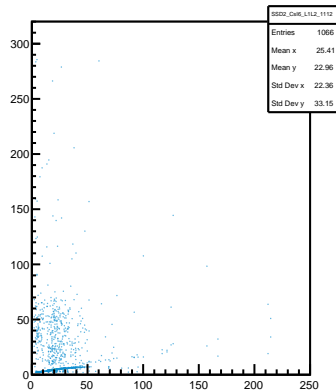
SSD2_Csl6_L2L3_Discard_1112



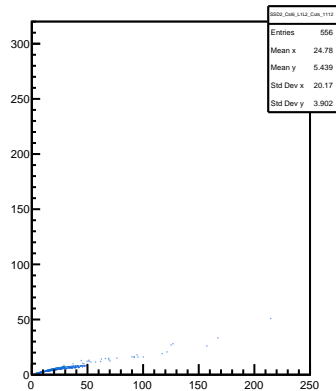
SSD2_Csl6_ModeStat_1112



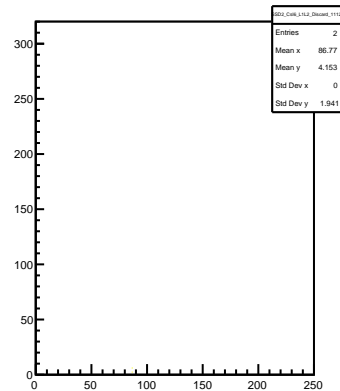
SSD2_Csl6_L1L2_1112



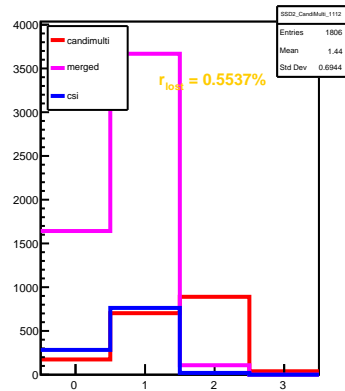
SSD2_Csl6_L1L2_Cuts_1112



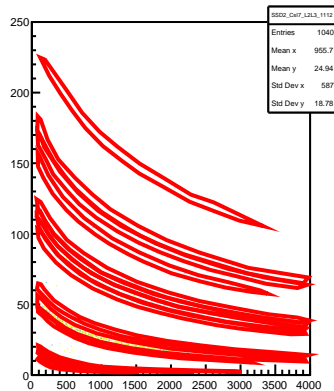
SSD2_Csl6_L1L2_Discard_1112



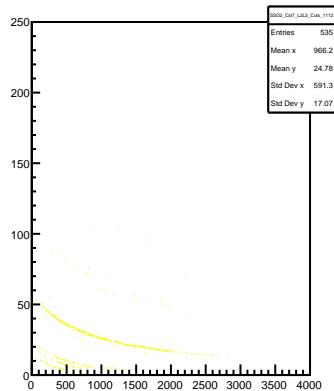
SSD2_CandiMulti_1112



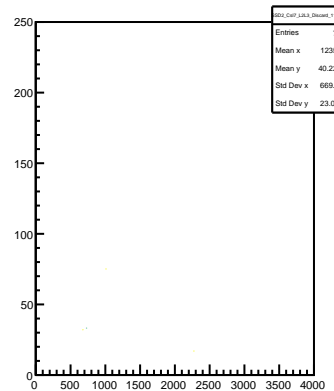
SSD2_CsI7_L2L3_1112



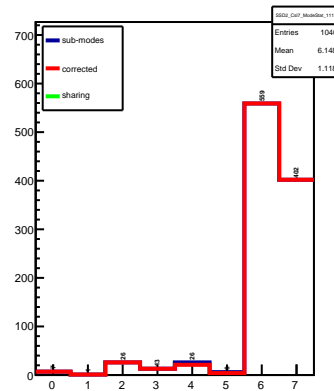
SSD2_CsI7_L2L3_Cuts_1112



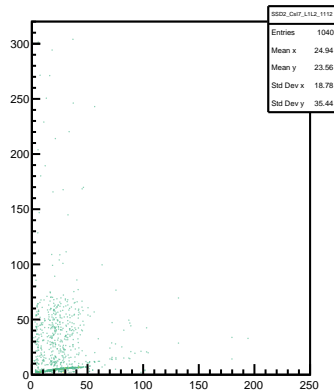
SSD2_CsI7_L2L3_Discard_1112



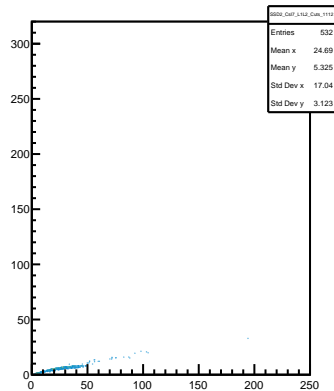
SSD2_CsI7_ModeStat_1112



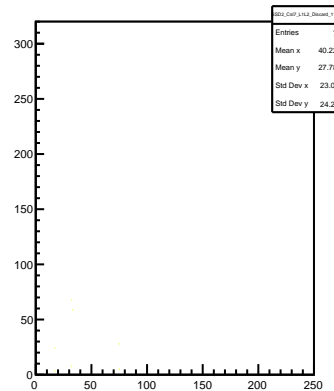
SSD2_CsI7_L1L2_1112



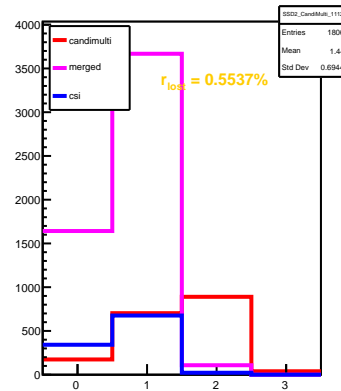
SSD2_CsI7_L1L2_Cuts_1112



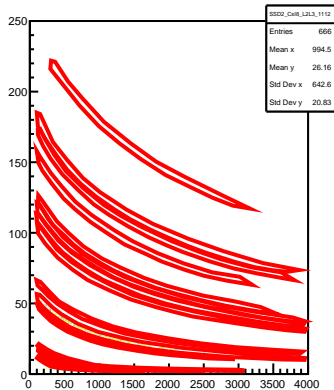
SSD2_CsI7_L1L2_Discard_1112



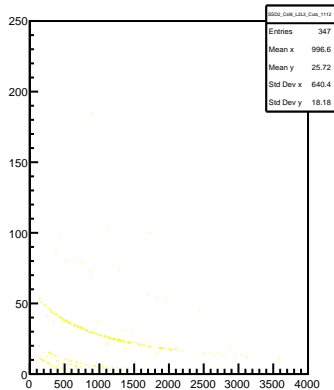
SSD2_CandiMulti_1112



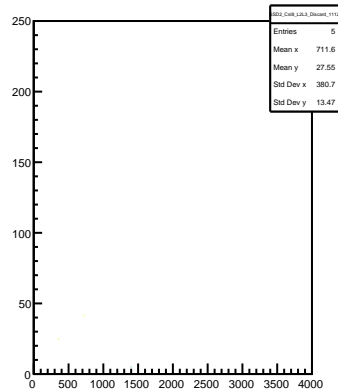
SSD2_Csl8_L2L3_1112



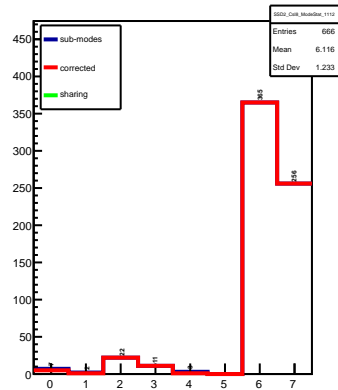
SSD2_Csl8_L2L3_Cuts_1112



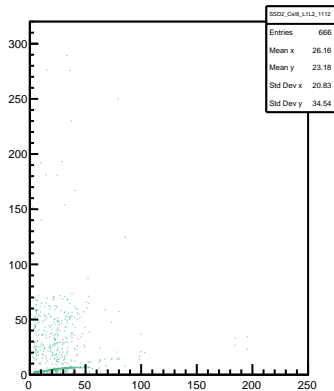
SSD2_Csl8_L2L3_Discard_1112



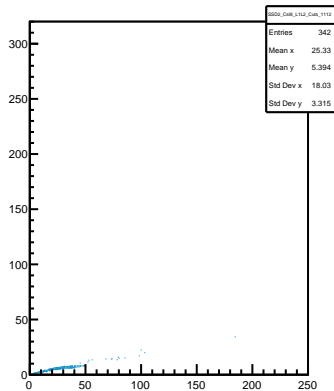
SSD2_Csl8_ModeStat_1112



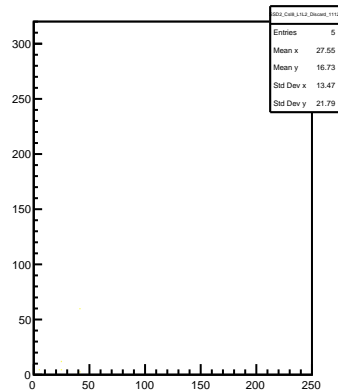
SSD2_Csl8_L1L2_1112



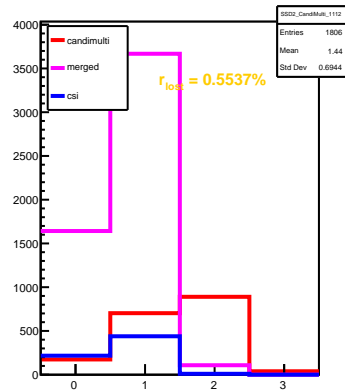
SSD2_Csl8_L1L2_Cuts_1112



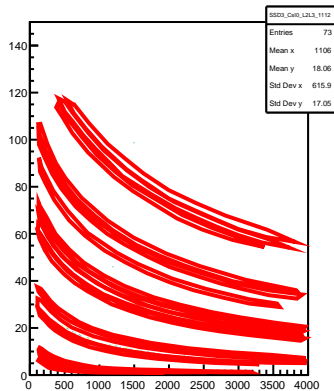
SSD2_Csl8_L1L2_Discard_1112



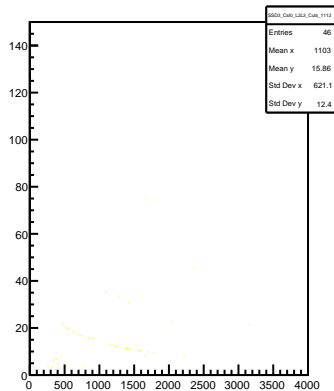
SSD2_CandiMulti_1112



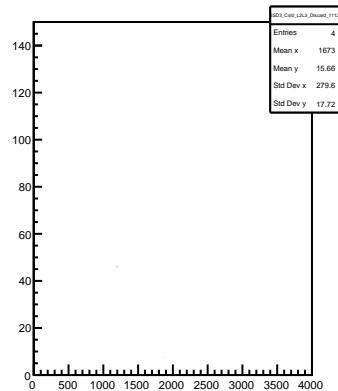
SSD3_Csl0_L2L3_1112



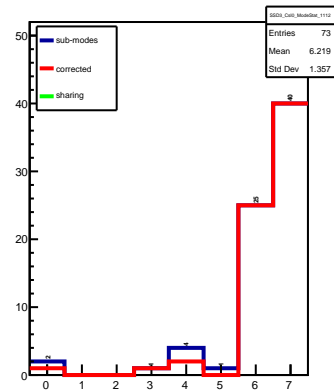
SSD3_Csl0_L2L3_Cuts_1112



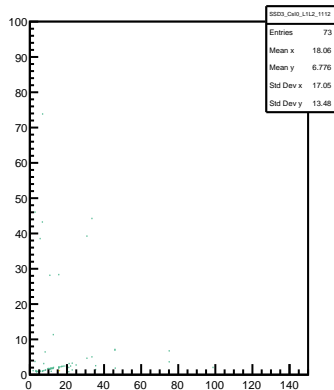
SSD3_Csl0_L2L3_Discard_1112



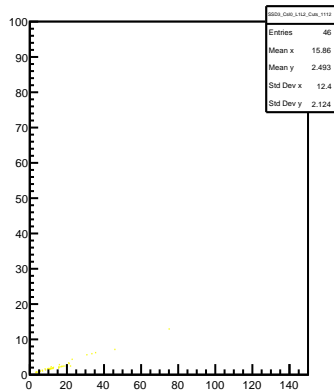
SSD3_Csl0_ModeStat_1112



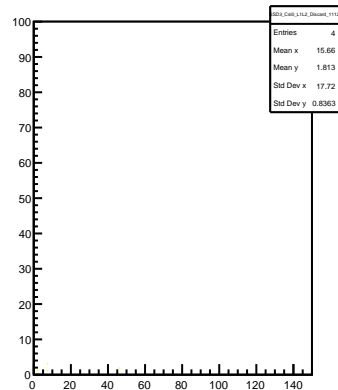
SSD3_Csl0_L1L2_1112



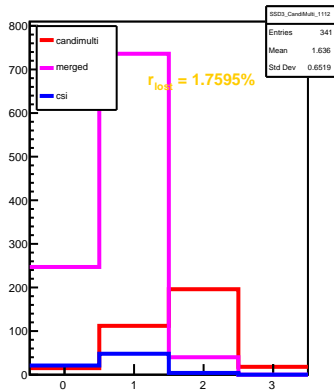
SSD3_Csl0_L1L2_Cuts_1112



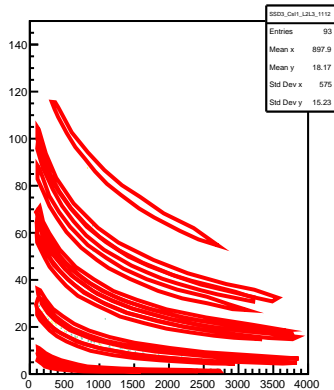
SSD3_Csl0_L1L2_Discard_1112



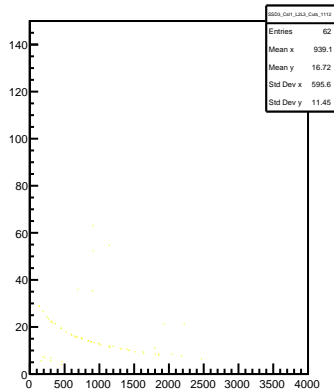
SSD3_CandiMulti_1112



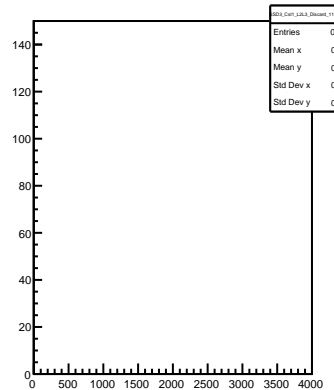
SSD3_Csl1_L2L3_1112



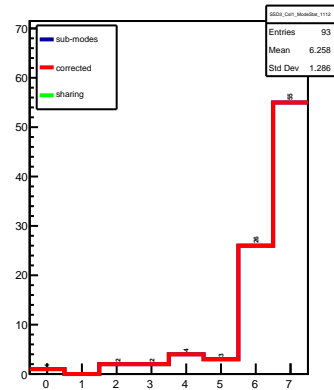
SSD3_Csl1_L2L3_Cuts_1112



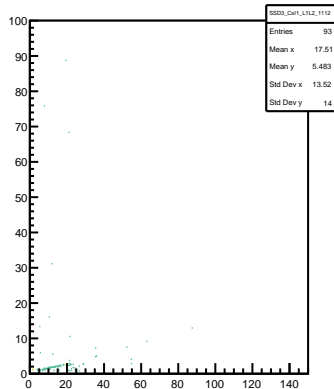
SSD3_Csl1_L2L3_Discard_1112



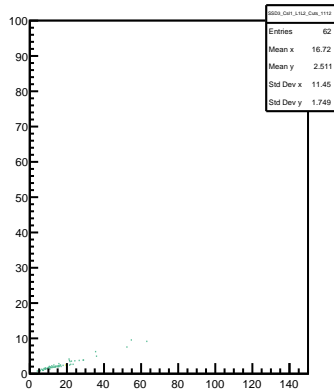
SSD3_Csl1_ModeStat_1112



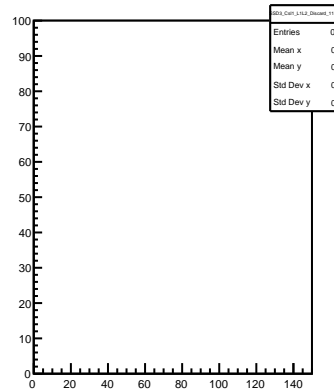
SSD3_Csl1_L1L2_1112



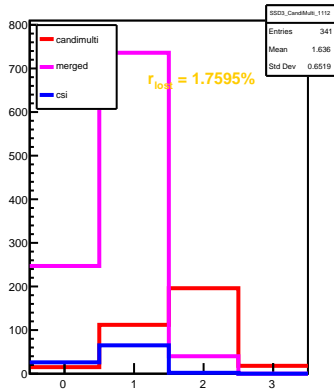
SSD3_Csl1_L1L2_Cuts_1112



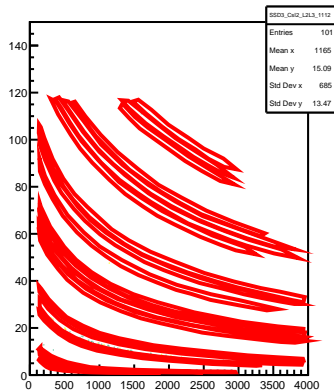
SSD3_Csl1_L1L2_Discard_1112



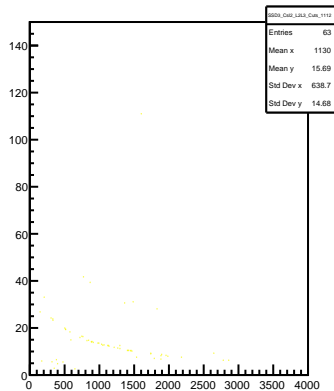
SSD3_CandiMulti_1112



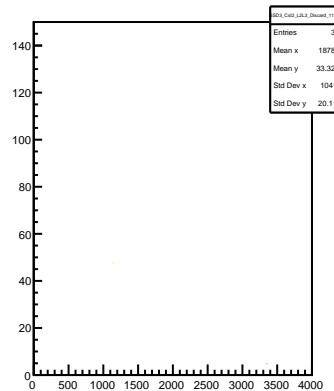
SSD3_Csl2_L2L3_1112



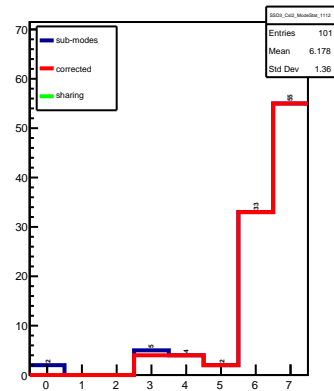
SSD3_Csl2_L2L3_Cuts_1112



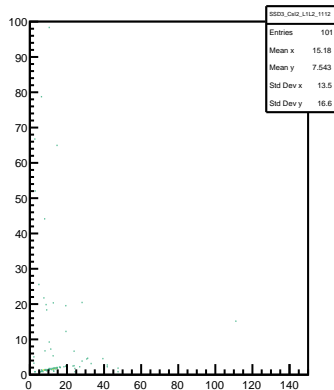
SSD3_Csl2_L2L3_Discard_1112



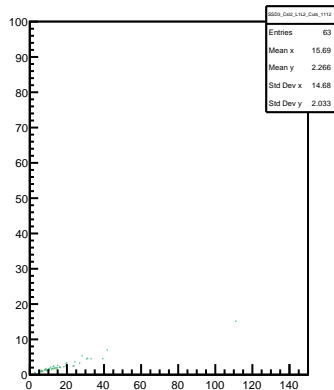
SSD3_Csl2_ModeStat_1112



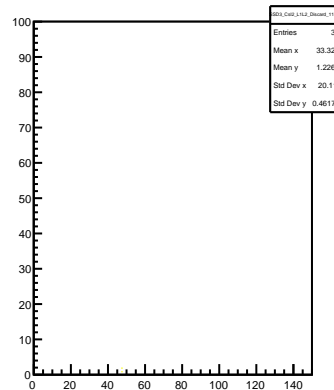
SSD3_Csl2_L1L2_1112



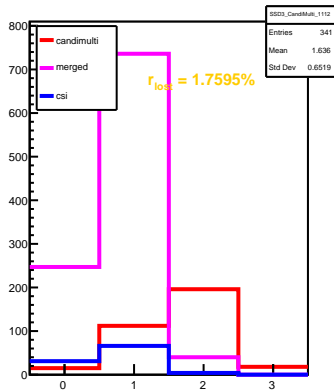
SSD3_Csl2_L1L2_Cuts_1112



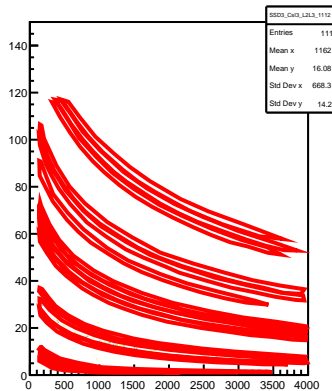
SSD3_Csl2_L1L2_Discard_1112



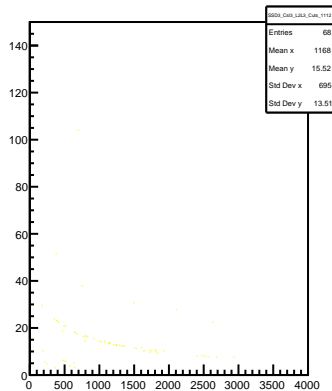
SSD3_CandiMulti_1112



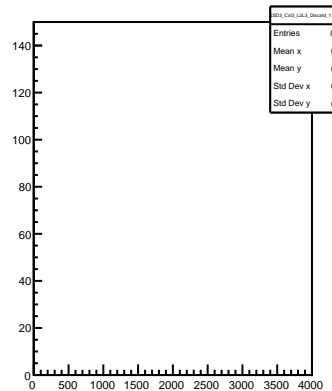
SSD3_Csl3_L2L3_1112



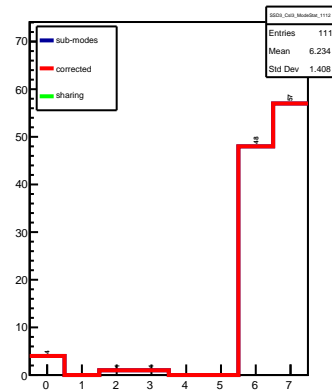
SSD3_Csl3_L2L3_Cuts_1112



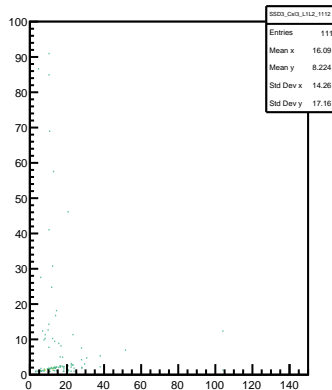
SSD3_Csl3_L2L3_Discard_1112



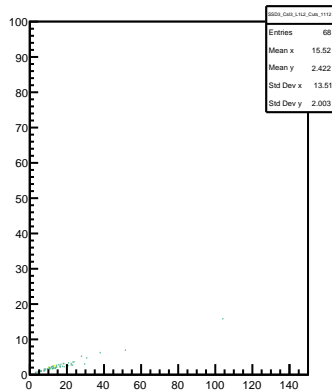
SSD3_Csl3_ModeStat_1112



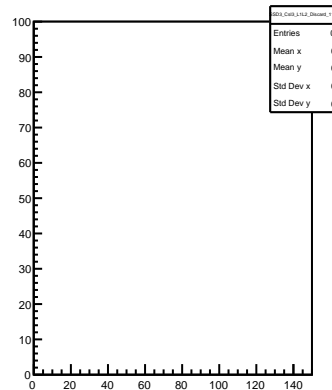
SSD3_Csl3_L1L2_1112



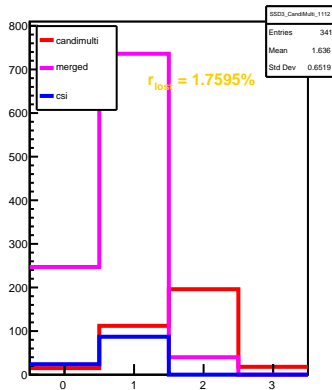
SSD3_Csl3_L1L2_Cuts_1112



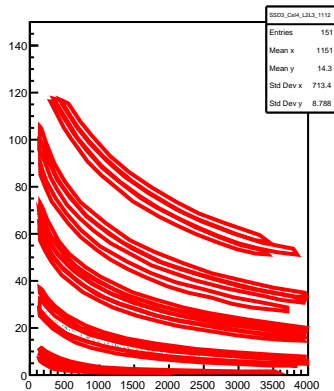
SSD3_Csl3_L1L2_Discard_1112



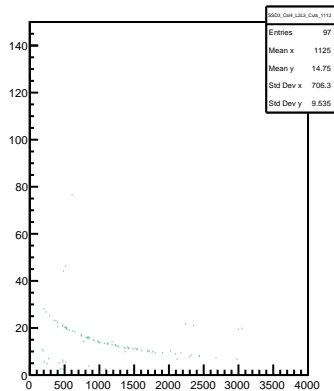
SSD3_CandiMulti_1112



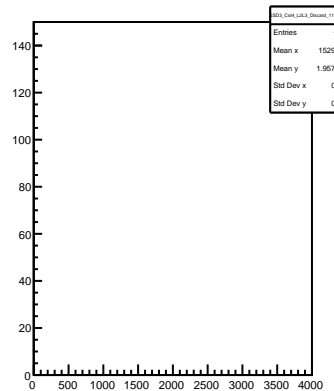
SSD3_Csl4_L2L3_1112



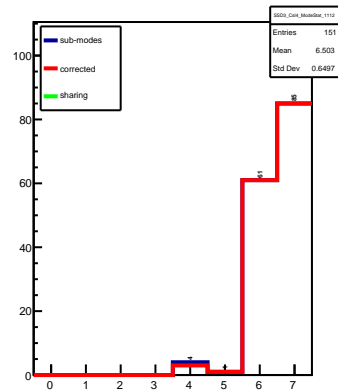
SSD3_Csl4_L2L3_Cuts_1112



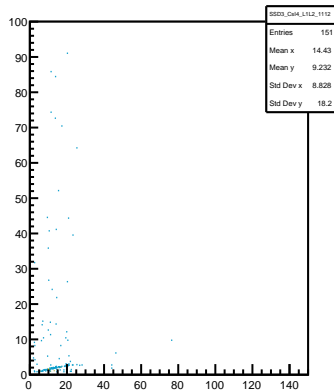
SSD3_Csl4_L2L3_Discard_1112



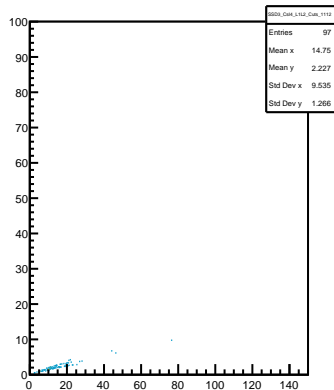
SSD3_Csl4_ModeStat_1112



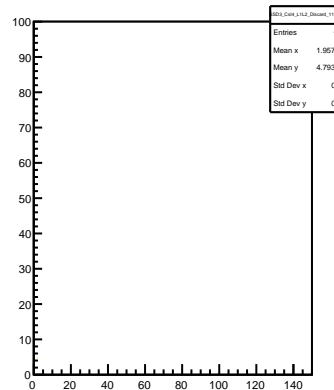
SSD3_Csl4_L1L2_1112



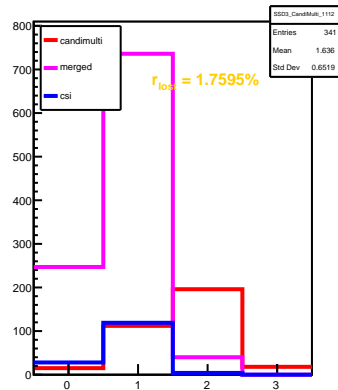
SSD3_Csl4_L1L2_Cuts_1112



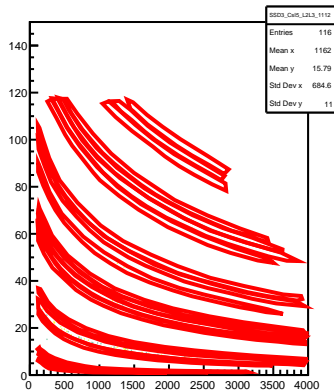
SSD3_Csl4_L1L2_Discard_1112



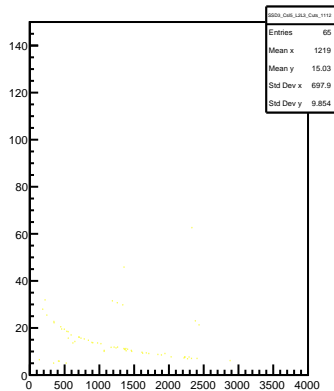
SSD3_CandiMulti_1112



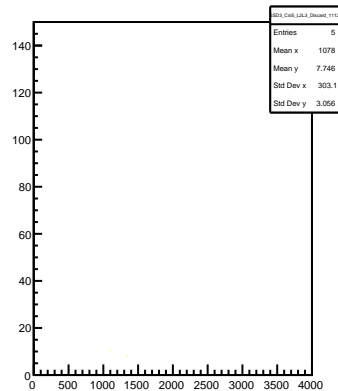
SSD3_Csl5_L2L3_1112



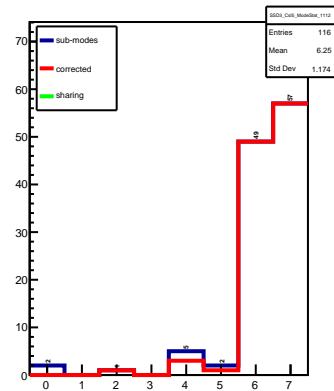
SSD3_Csl5_L2L3_Cuts_1112



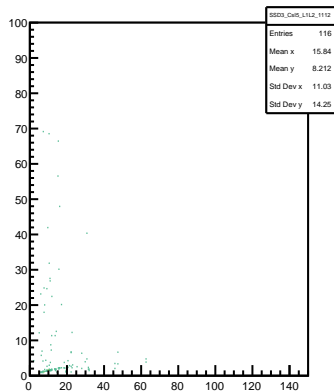
SSD3_Csl5_L2L3_Discard_1112



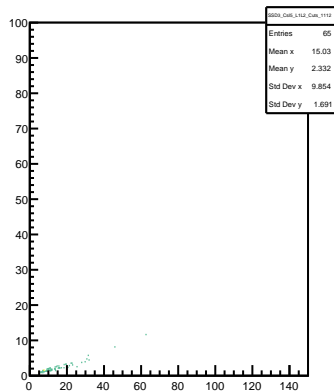
SSD3_Csl5_ModeStat_1112



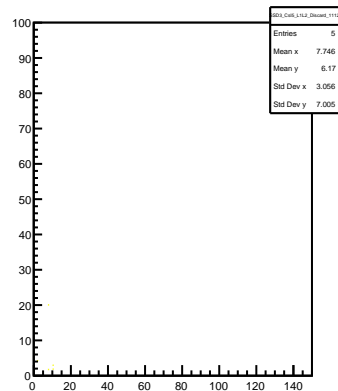
SSD3_Csl5_L1L2_1112



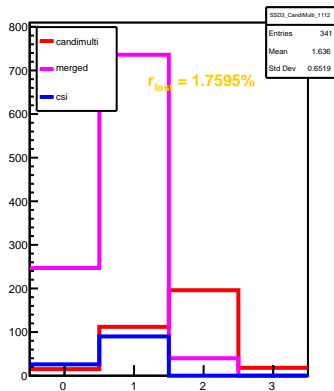
SSD3_Csl5_L1L2_Cuts_1112



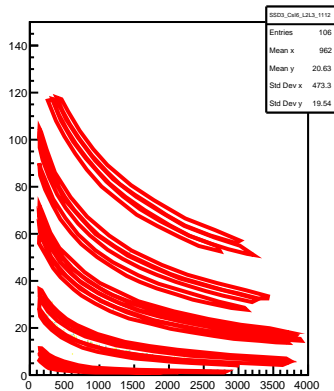
SSD3_Csl5_L1L2_Discard_1112



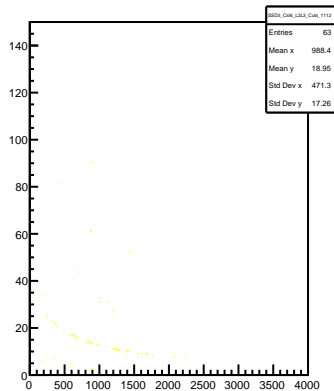
SSD3_CandiMulti_1112



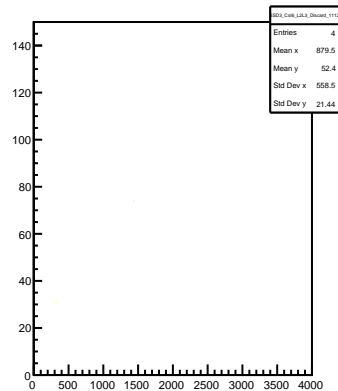
SSD3_Csl6_L2L3_1112



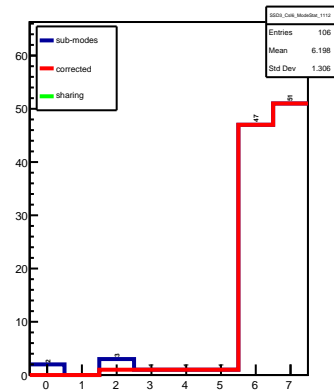
SSD3_Csl6_L2L3_Cuts_1112



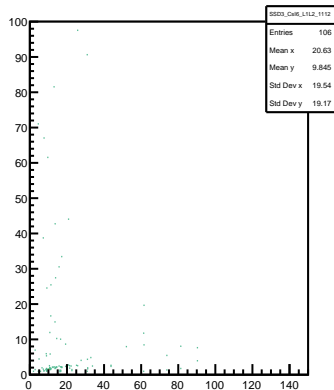
SSD3_Csl6_L2L3_Discard_1112



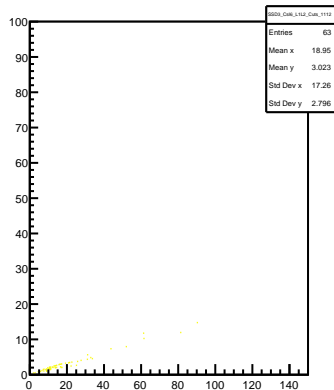
SSD3_Csl6_ModeStat_1112



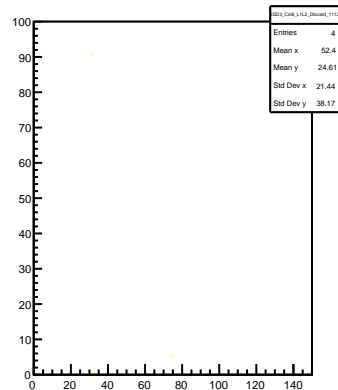
SSD3_Csl6_L1L2_1112



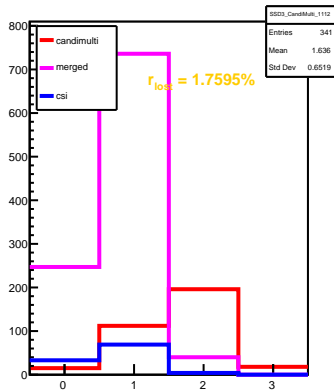
SSD3_Csl6_L1L2_Cuts_1112



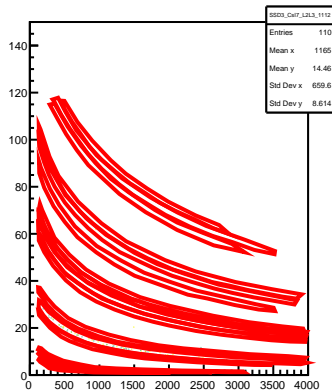
SSD3_Csl6_L1L2_Discard_1112



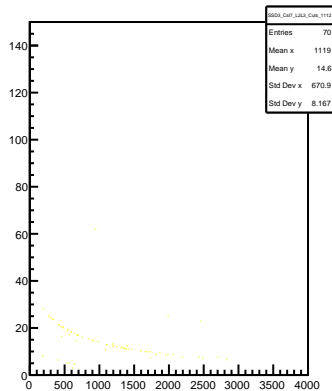
SSD3_CandiMulti_1112



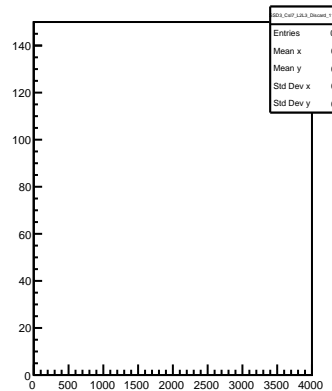
SSD3_Csl7_L2L3_1112



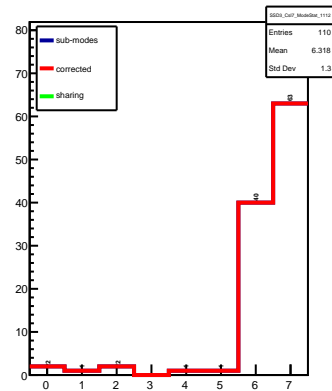
SSD3_Csl7_L2L3_Cuts_1112



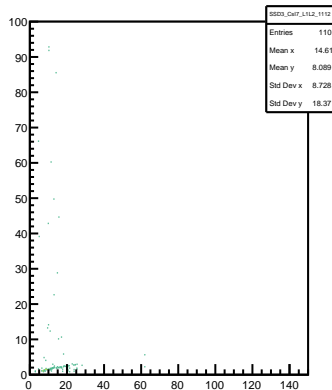
SSD3_Csl7_L2L3_Discard_1112



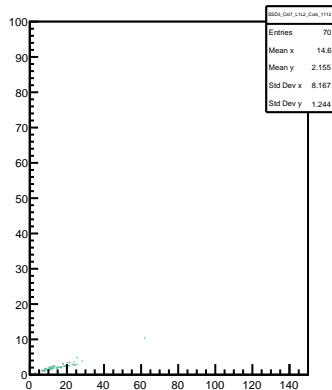
SSD3_Csl7_ModeStat_1112



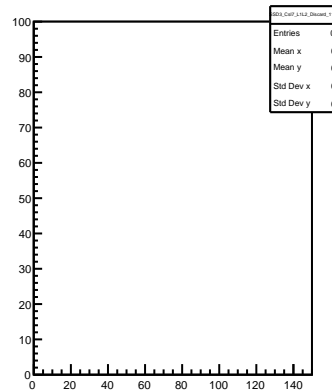
SSD3_Csl7_L1L2_1112



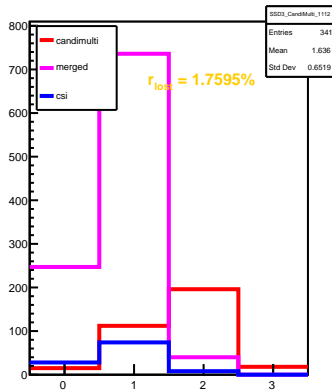
SSD3_Csl7_L1L2_Cuts_1112



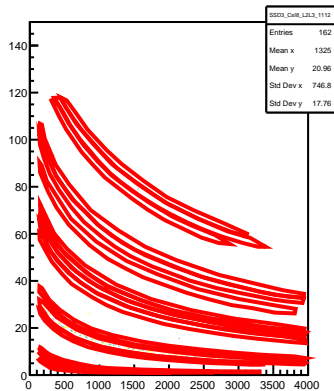
SSD3_Csl7_L1L2_Discard_1112



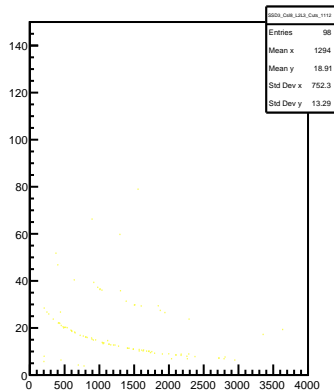
SSD3_CandiMulti_1112



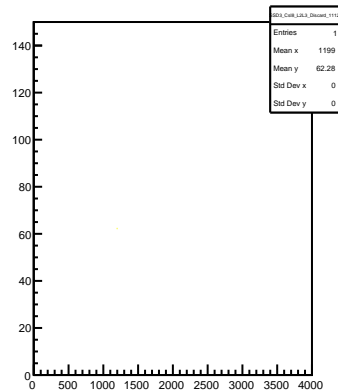
SSD3_Csl8_L2L3_1112



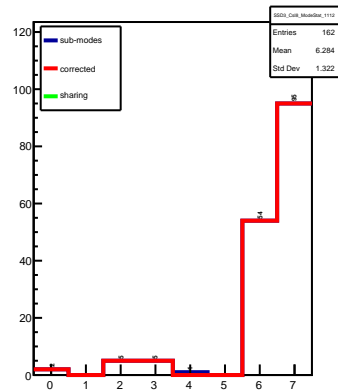
SSD3_Csl8_L2L3_Cuts_1112



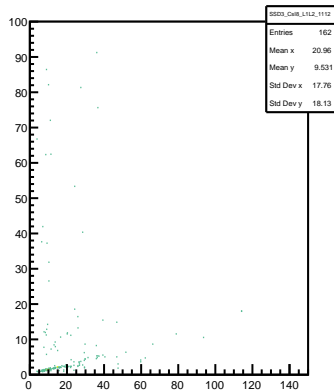
SSD3_Csl8_L2L3_Discard_1112



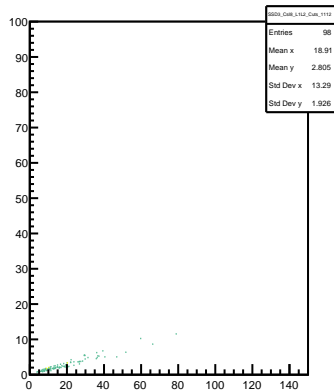
SSD3_Csl8_ModeStat_1112



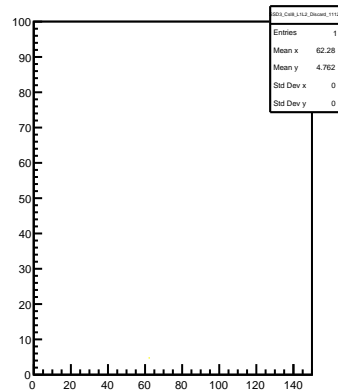
SSD3_Csl8_L1L2_1112



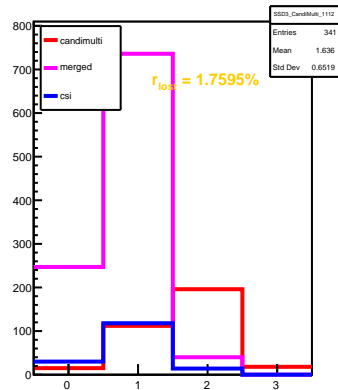
SSD3_Csl8_L1L2_Cuts_1112



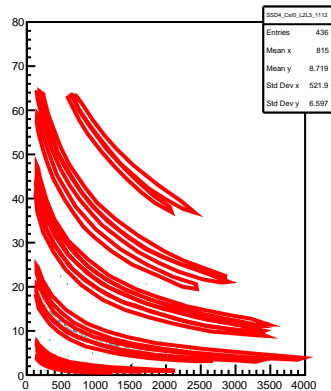
SSD3_Csl8_L1L2_Discard_1112



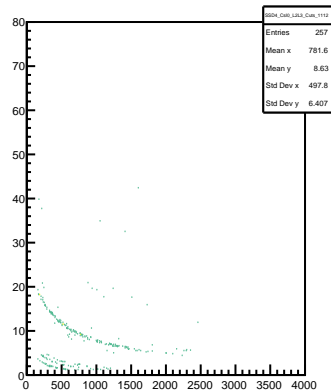
SSD3_CandiMulti_1112



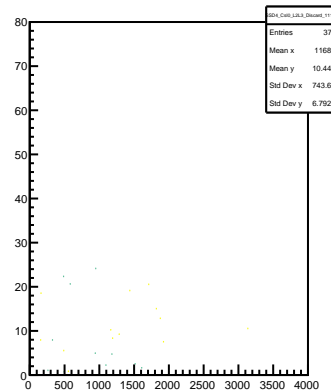
SSD4_Csl0_L2L3_1112



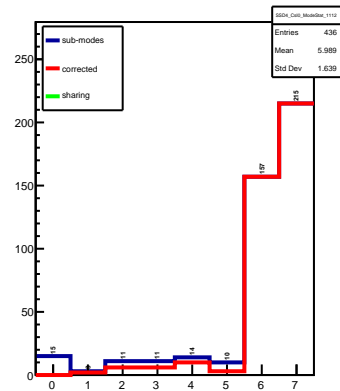
SSD4_Csl0_L2L3_Cuts_1112



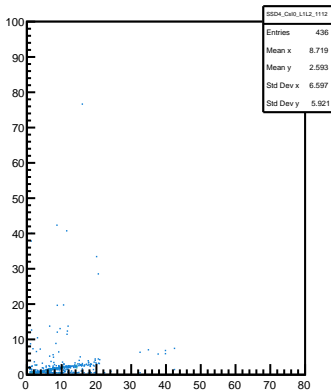
SSD4_Csl0_L2L3_Discard_1112



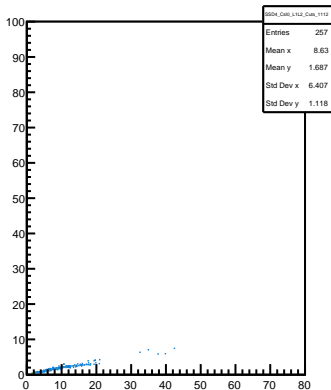
SSD4_Csl0_ModeStat_1112



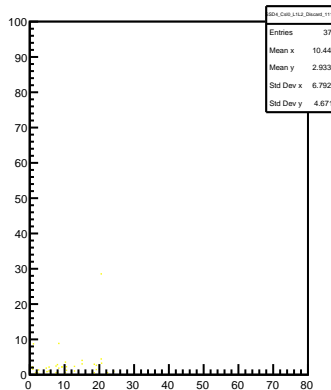
SSD4_Csl0_L1L2_1112



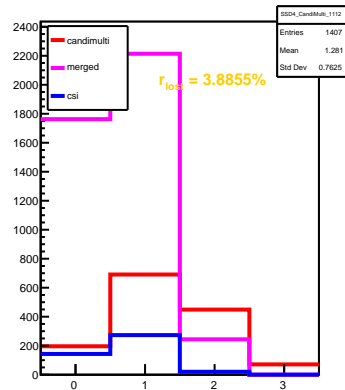
SSD4_Csl0_L1L2_Cuts_1112



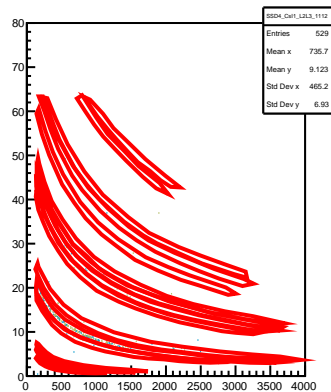
SSD4_Csl0_L1L2_Discard_1112



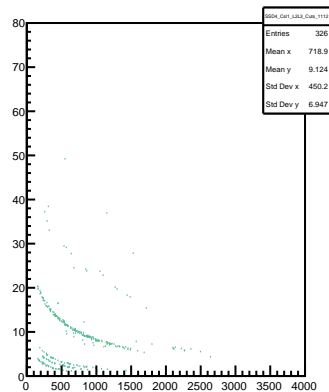
SSD4_CandiMulti_1112



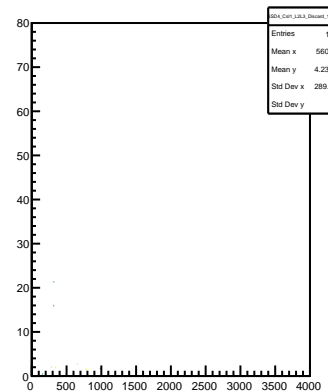
SSD4_Csl1_L2L3_1112



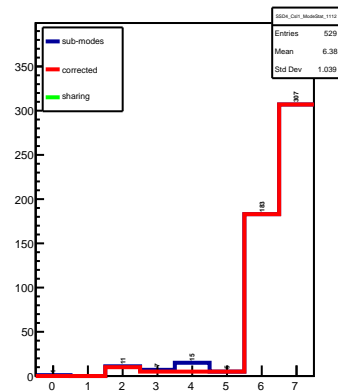
SSD4_Csl1_L2L3_Cuts_1112



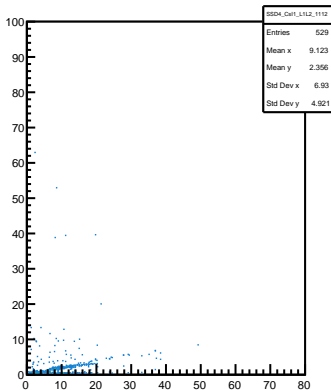
SSD4_Csl1_L2L3_Discard_1112



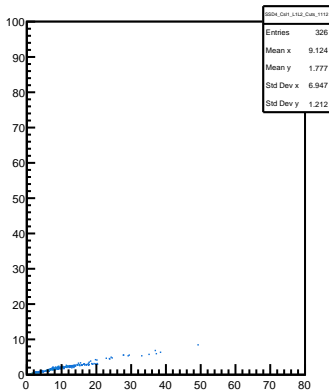
SSD4_Csl1_ModeStat_1112



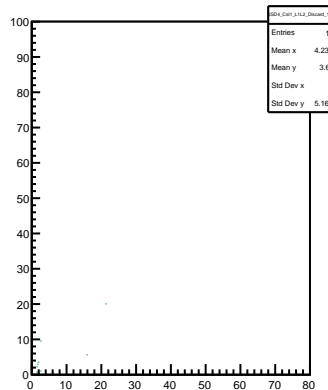
SSD4_Csl1_L1L2_1112



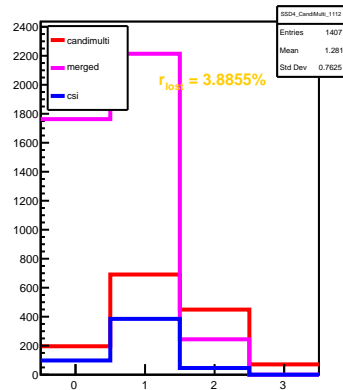
SSD4_Csl1_L1L2_Cuts_1112



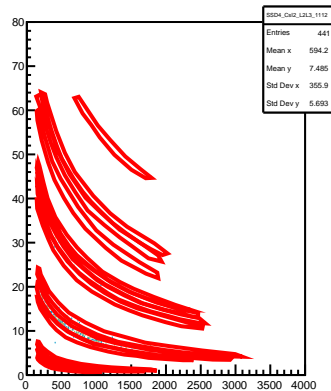
SSD4_Csl1_L1L2_Discard_1112



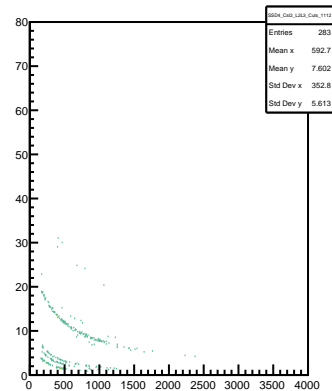
SSD4_CandiMulti_1112



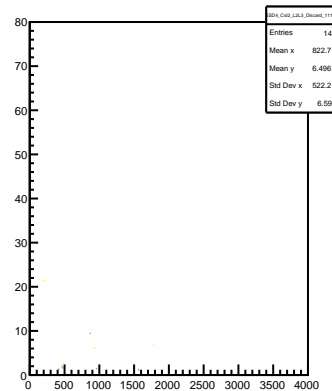
SSD4_Csi2_L2L3_1112



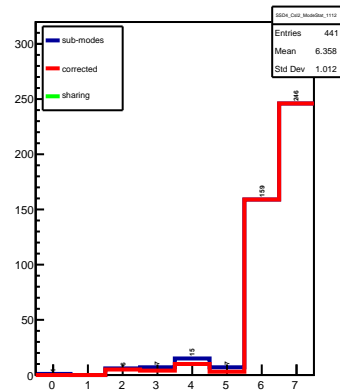
SSD4_Csi2_L2L3_Cuts_1112



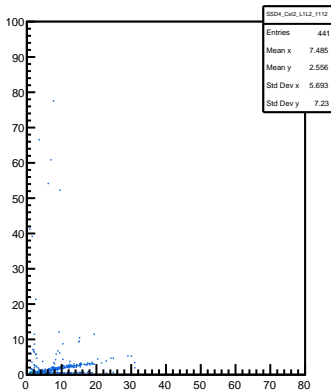
SSD4_Csi2_L2L3_Discard_1112



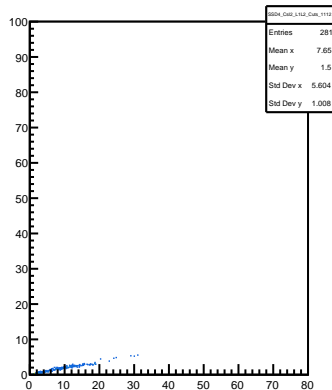
SSD4_Csi2_ModeStat_1112



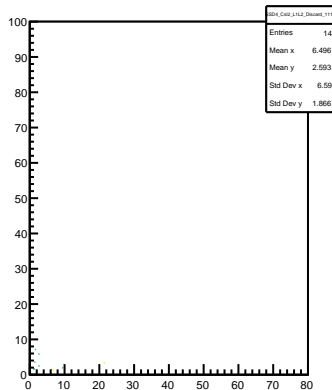
SSD4_Csi2_L1L2_1112



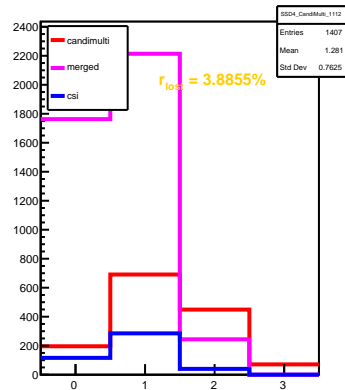
SSD4_Csi2_L1L2_Cuts_1112



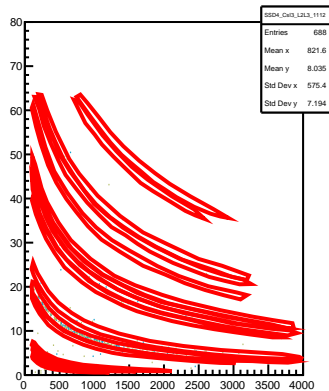
SSD4_Csi2_L1L2_Discard_1112



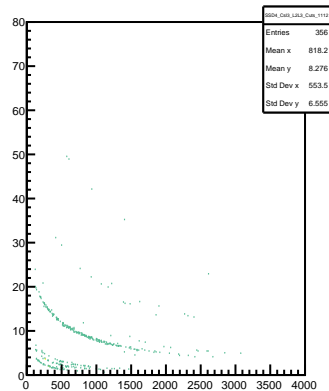
SSD4_CandiMulti_1112



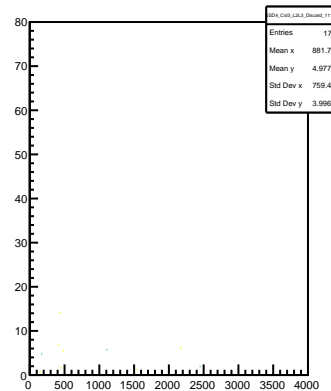
SSD4_Csl3_L2L3_1112



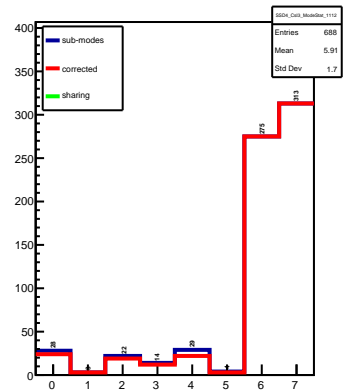
SSD4_Csl3_L2L3_Cuts_1112



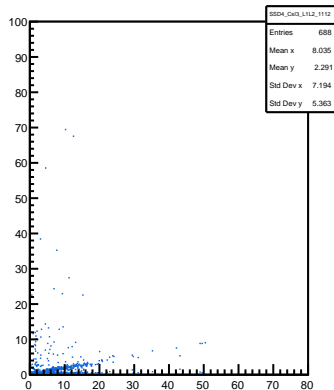
SSD4_Csl3_L2L3_Discard_1112



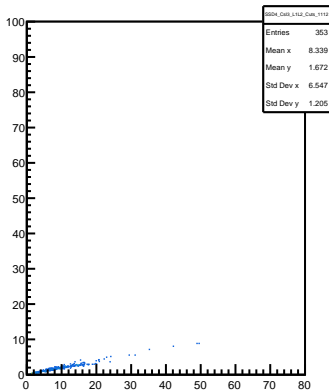
SSD4_Csl3_ModeStat_1112



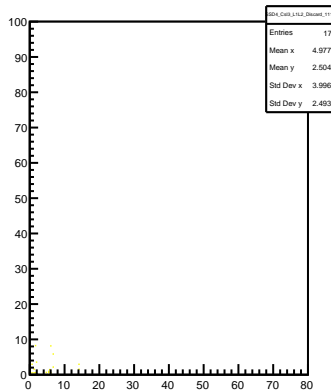
SSD4_Csl3_L1L2_1112



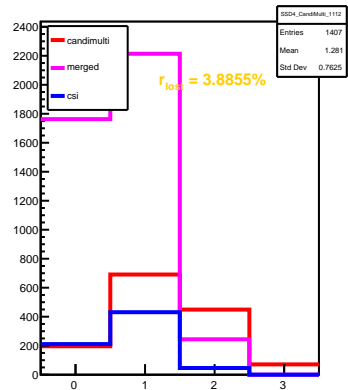
SSD4_Csl3_L1L2_Cuts_1112



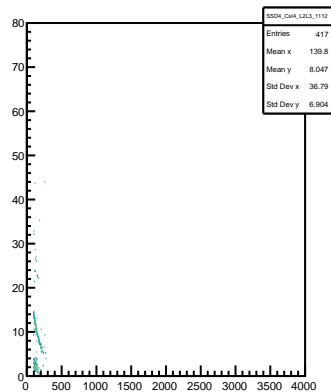
SSD4_Csl3_L1L2_Discard_1112



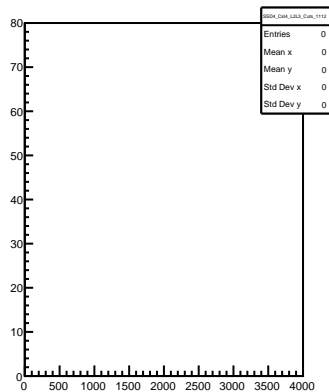
SSD4_CandiMulti_1112



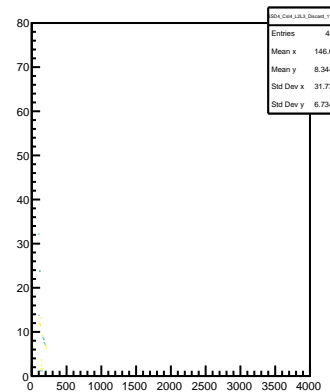
SSD4_Csl4_L2L3_1112



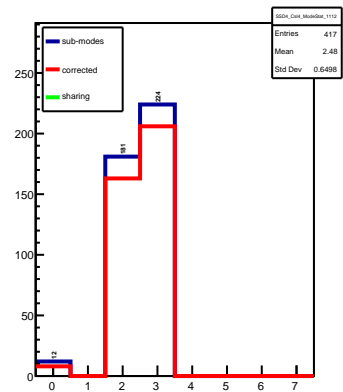
SSD4_Csl4_L2L3_Cuts_1112



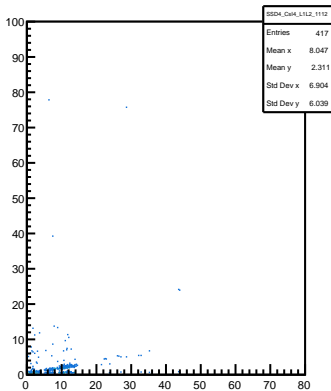
SSD4_Csl4_L2L3_Discard_1112



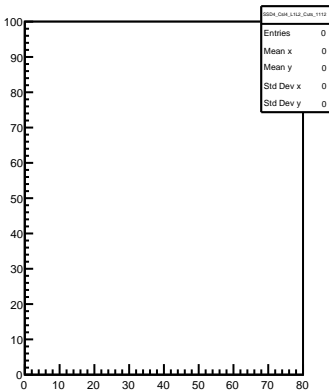
SSD4_Csl4_ModeStat_1112



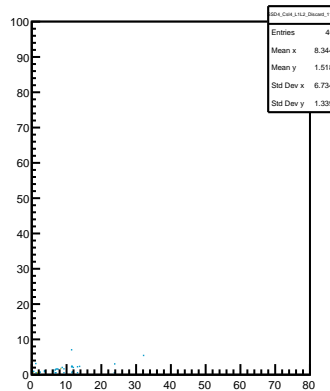
SSD4_Csl4_L1L2_1112



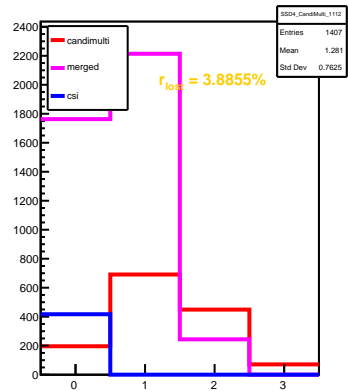
SSD4_Csl4_L1L2_Cuts_1112



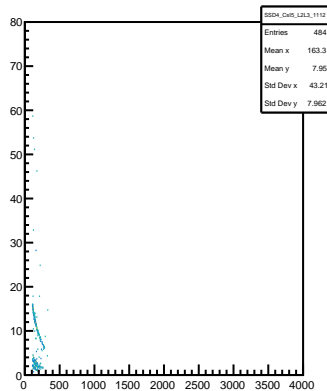
SSD4_Csl4_L1L2_Discard_1112



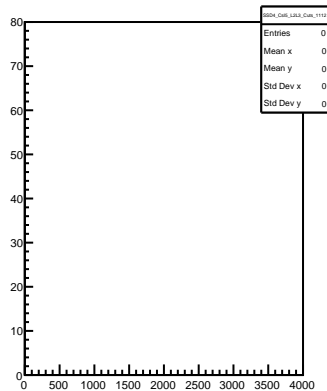
SSD4_CandiMulti_1112



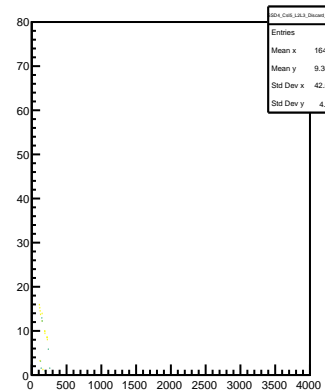
SSD4_Csl5_L2L3_1112



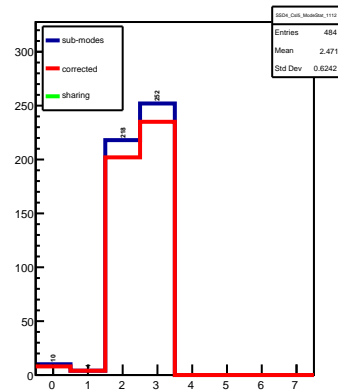
SSD4_Csl5_L2L3_Cuts_1112



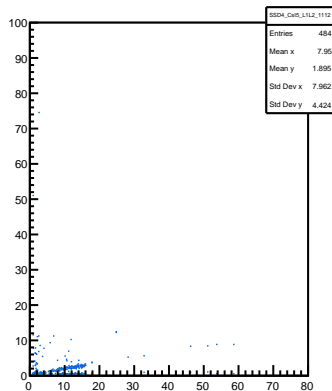
SSD4_Csl5_L2L3_Discard_1112



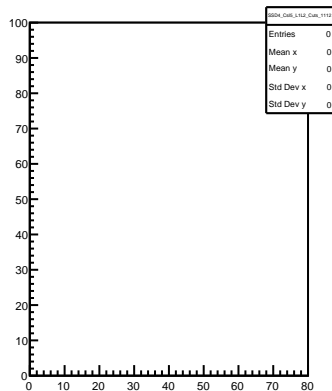
SSD4_Csl5_ModeStat_1112



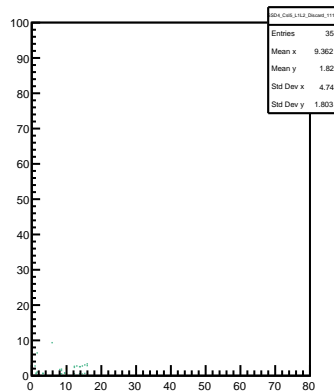
SSD4_Csl5_L1L2_1112



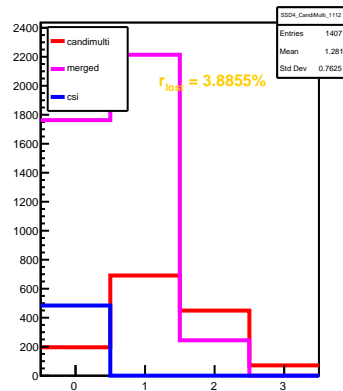
SSD4_Csl5_L1L2_Cuts_1112



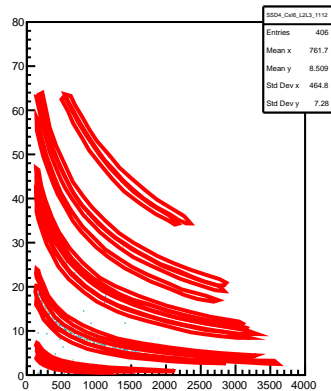
SSD4_Csl5_L1L2_Discard_1112



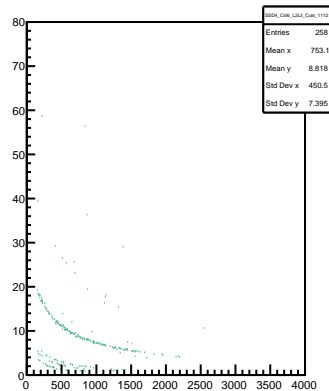
SSD4_CandiMulti_1112



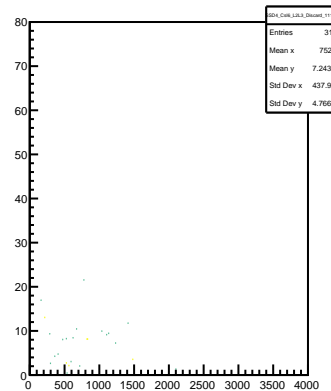
SSD4_Csl6_L2L3_1112



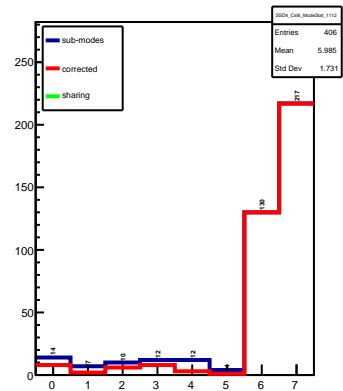
SSD4_Csl6_L2L3_Cuts_1112



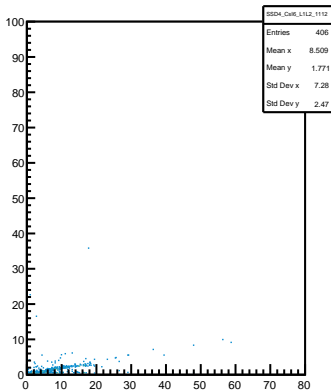
SSD4_Csl6_L2L3_Discard_1112



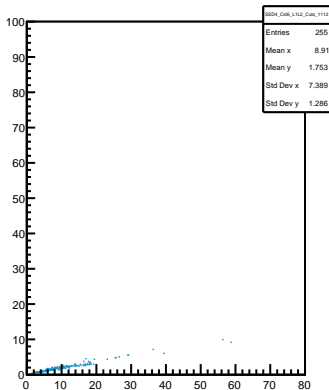
SSD4_Csl6_ModeStat_1112



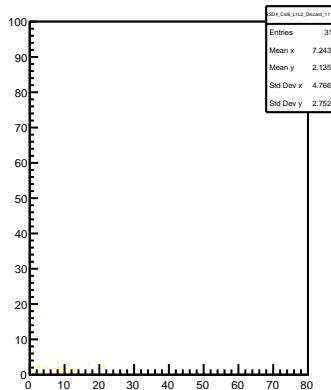
SSD4_Csl6_L1L2_1112



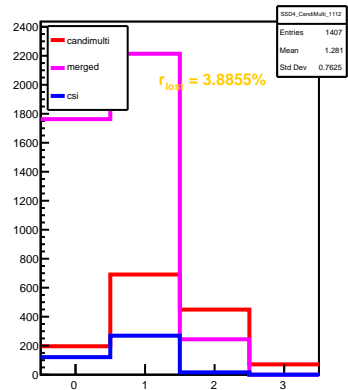
SSD4_Csl6_L1L2_Cuts_1112



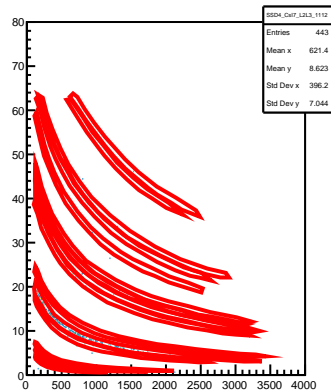
SSD4_Csl6_L1L2_Discard_1112



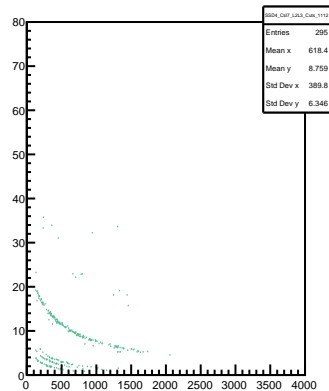
SSD4_CandiMulti_1112



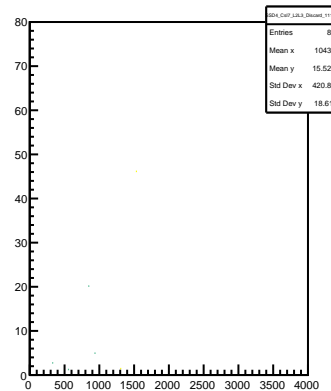
SSD4_Csl7_L2L3_1112



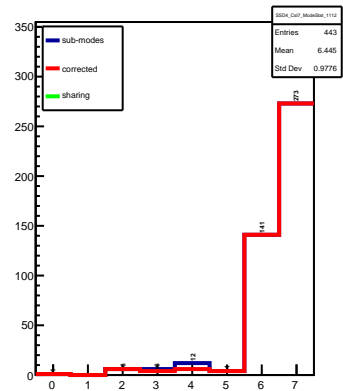
SSD4_Csl7_L2L3_Cuts_1112



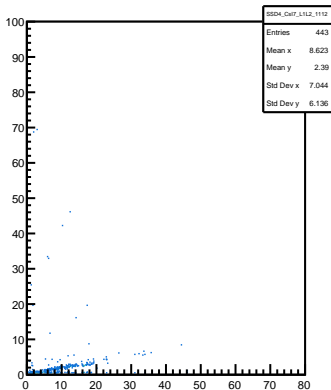
SSD4_Csl7_L2L3_Discard_1112



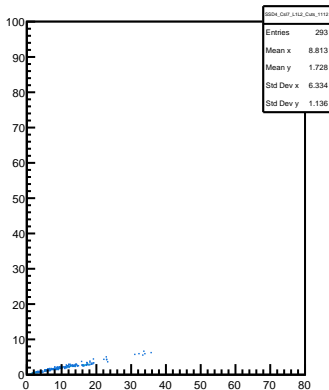
SSD4_Csl7_ModeStat_1112



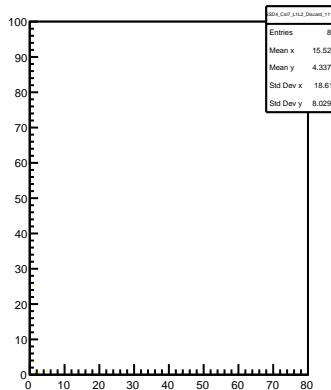
SSD4_Csl7_L1L2_1112



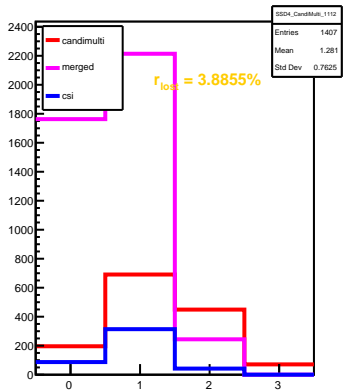
SSD4_Csl7_L1L2_Cuts_1112



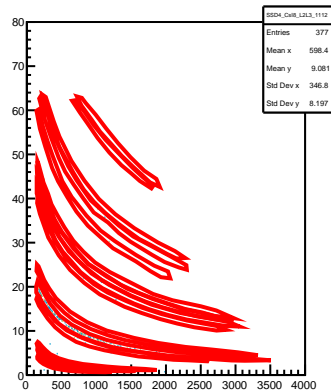
SSD4_Csl7_L1L2_Discard_1112



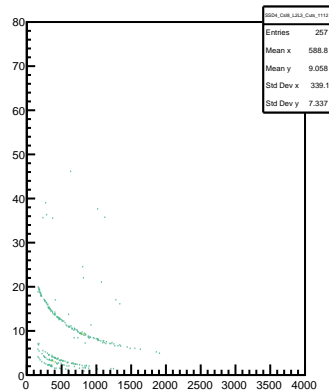
SSD4_CandiMulti_1112



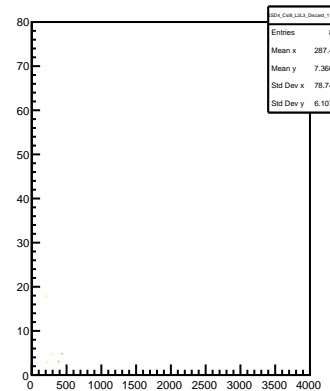
SSD4_Csl8_L2L3_1112



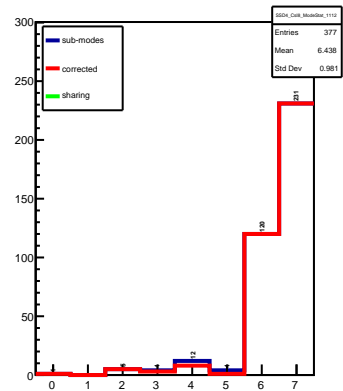
SSD4_Csl8_L2L3_Cuts_1112



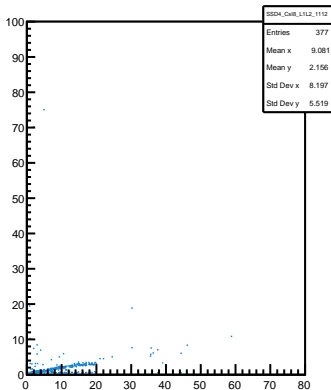
SSD4_Csl8_L2L3_Discard_1112



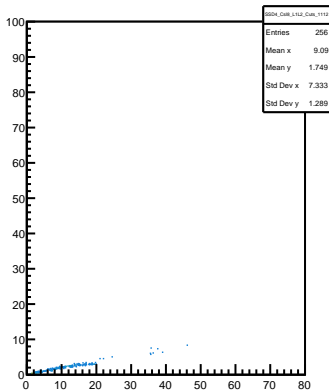
SSD4_Csl8_ModeStat_1112



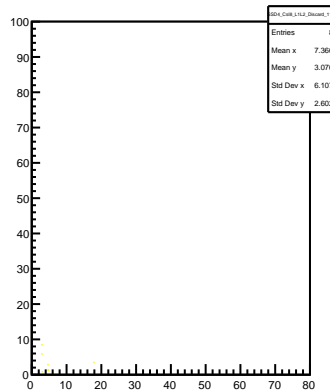
SSD4_Csl8_L1L2_1112



SSD4_Csl8_L1L2_Cuts_1112



SSD4_Csl8_L1L2_Discard_1112



SSD4_CandiMulti_1112

