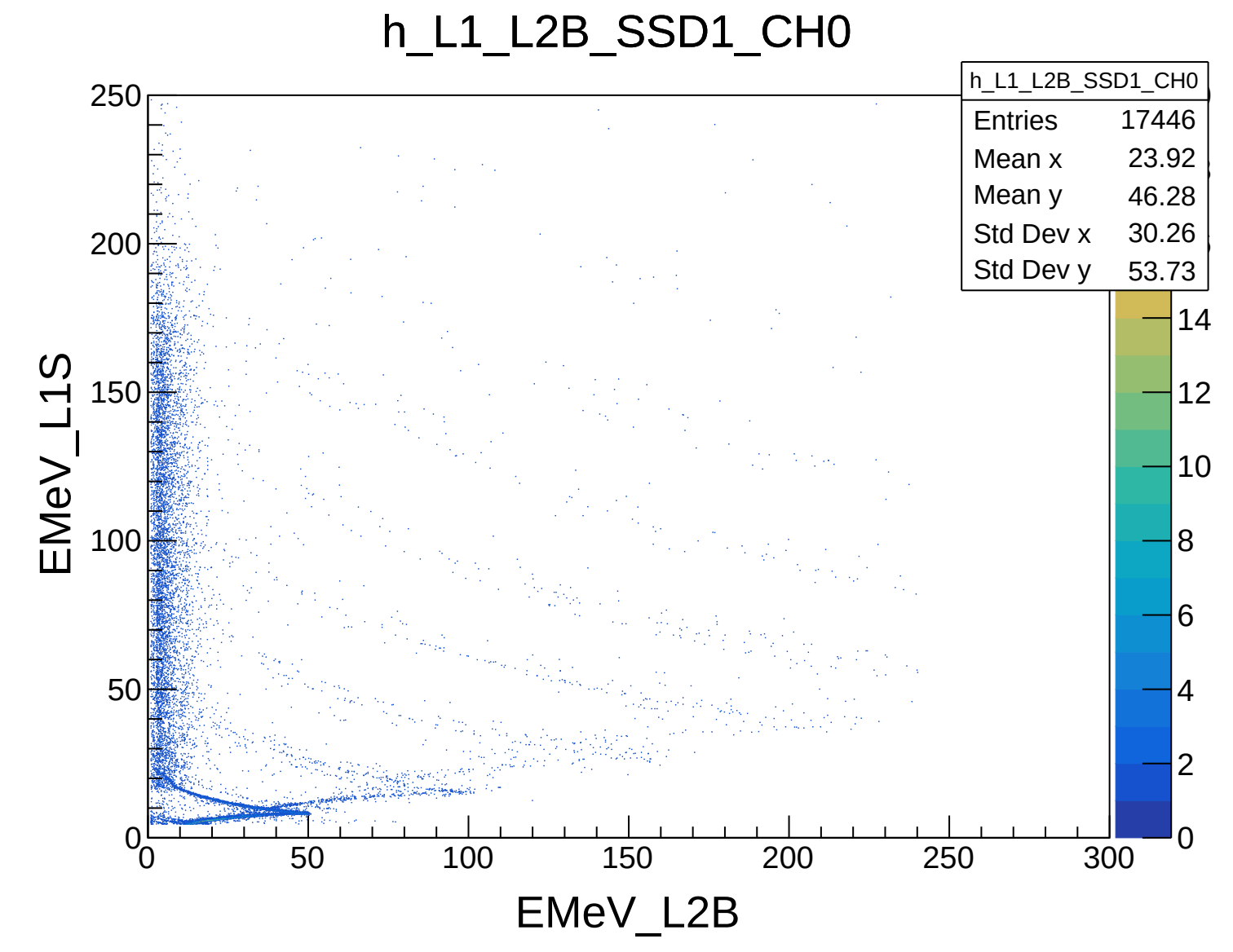
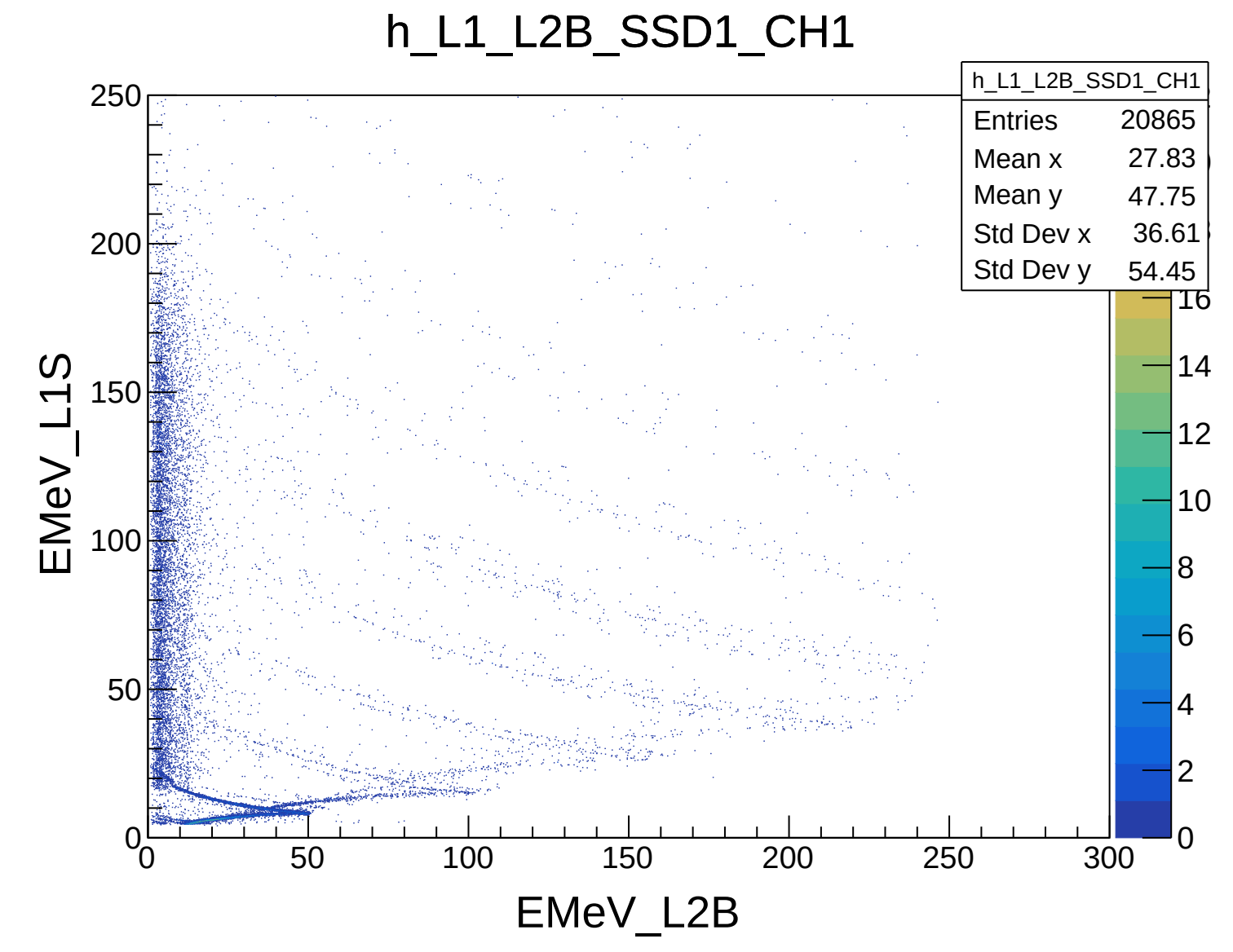
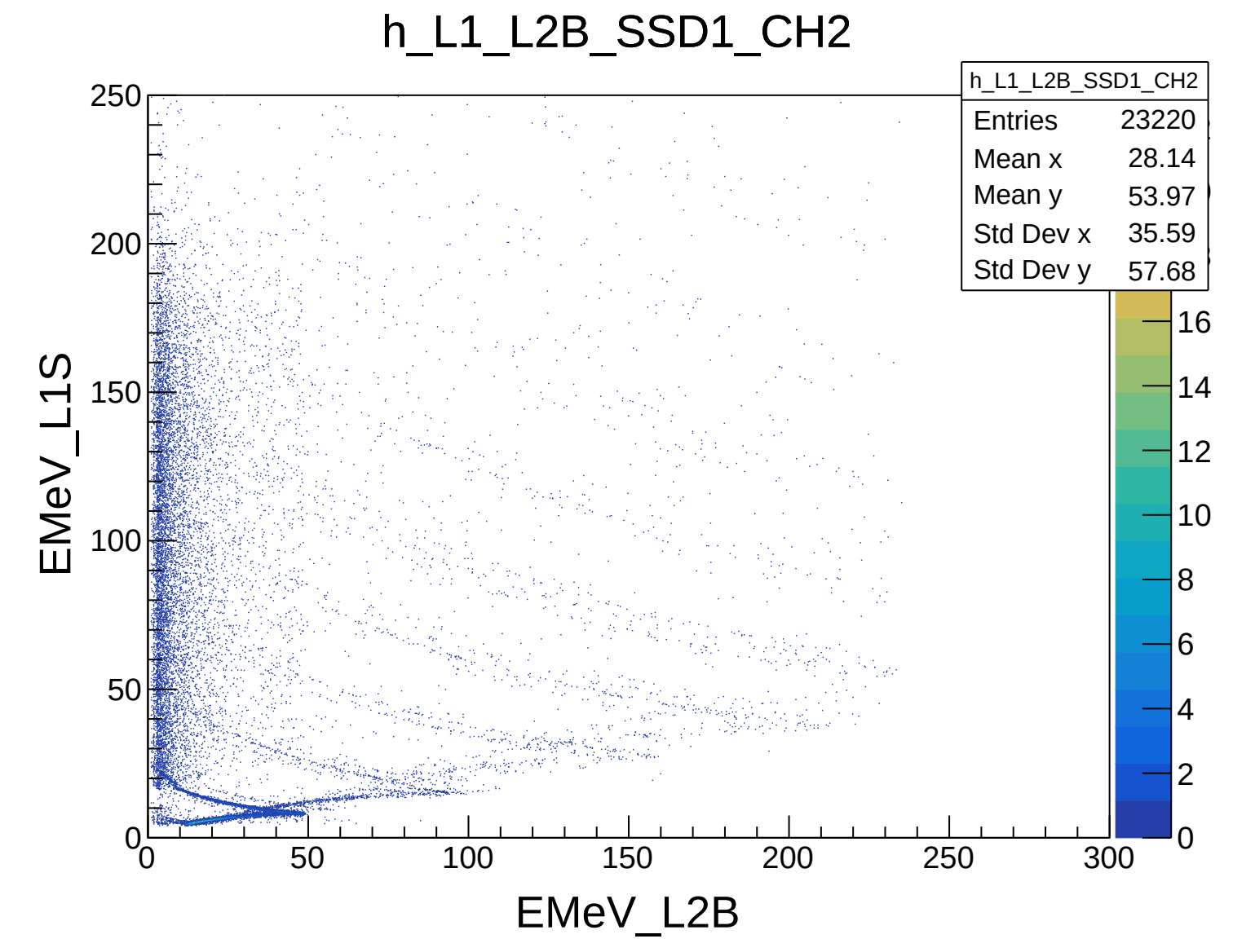
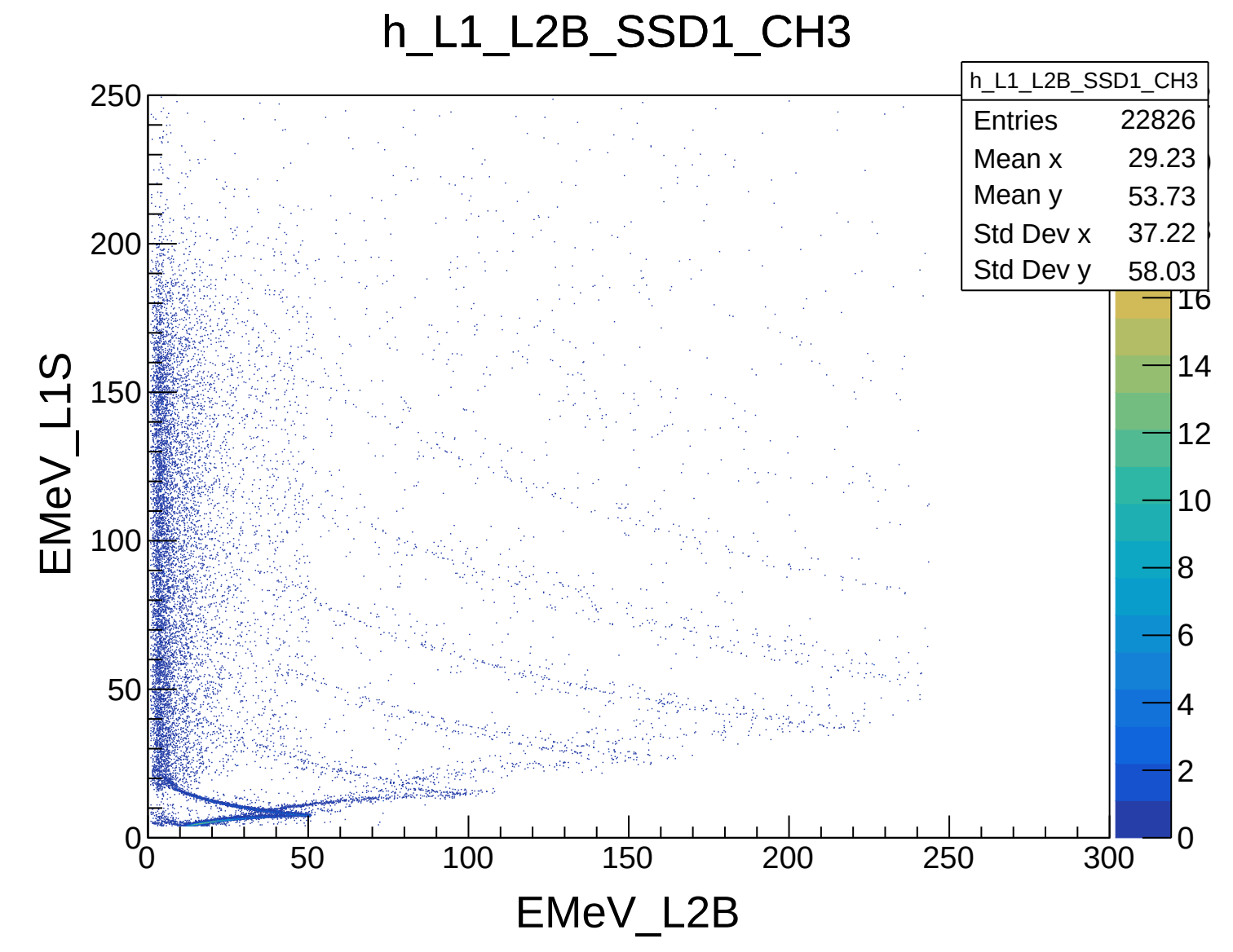
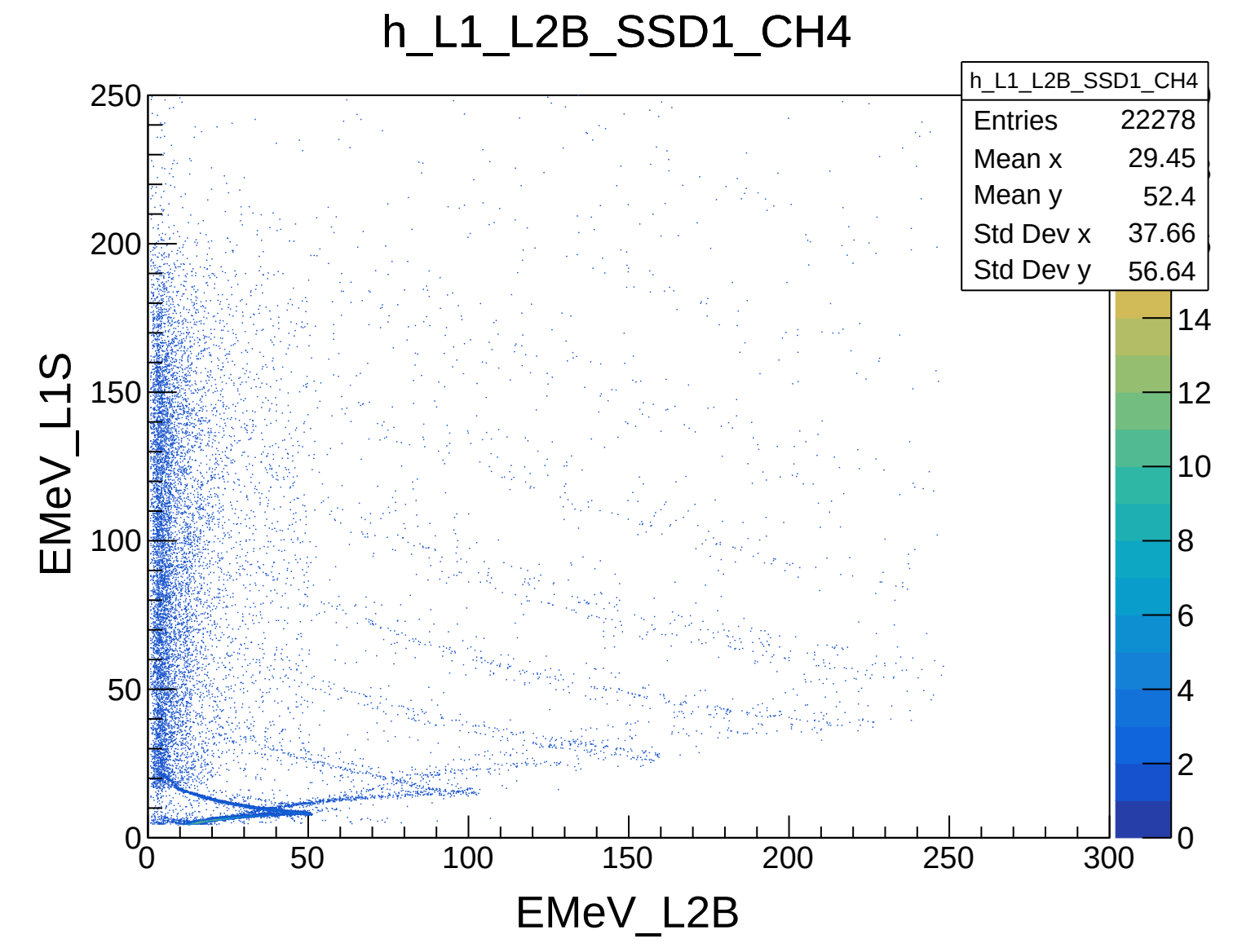
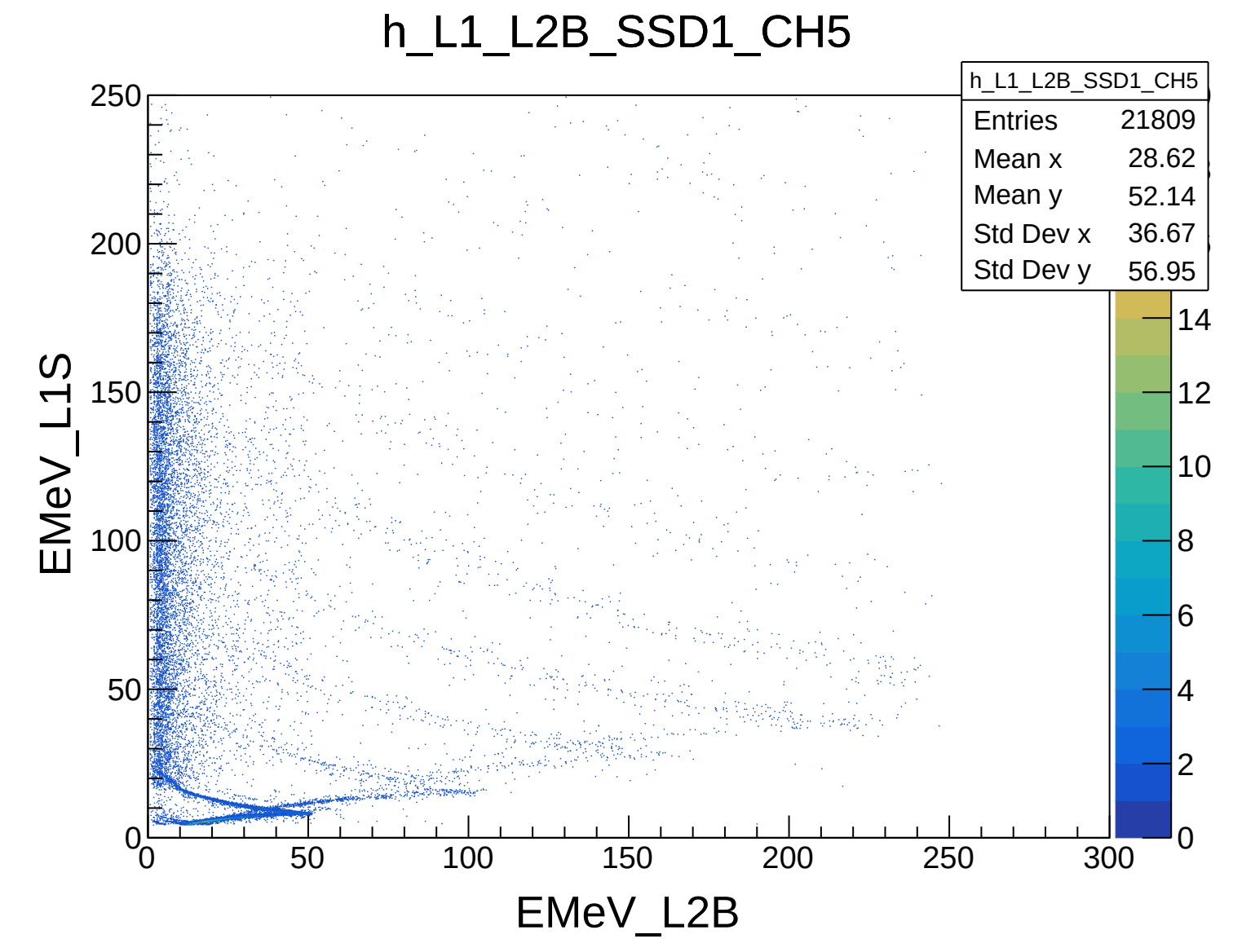

h_L1_L2B_SSD1_CH0
h_L1_L2B_SSD1_CH0
Entries 17446
Mean x 23.92
Mean y 46.28
Std Dev x 30.26
Std Dev y 53.73
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10
12
14

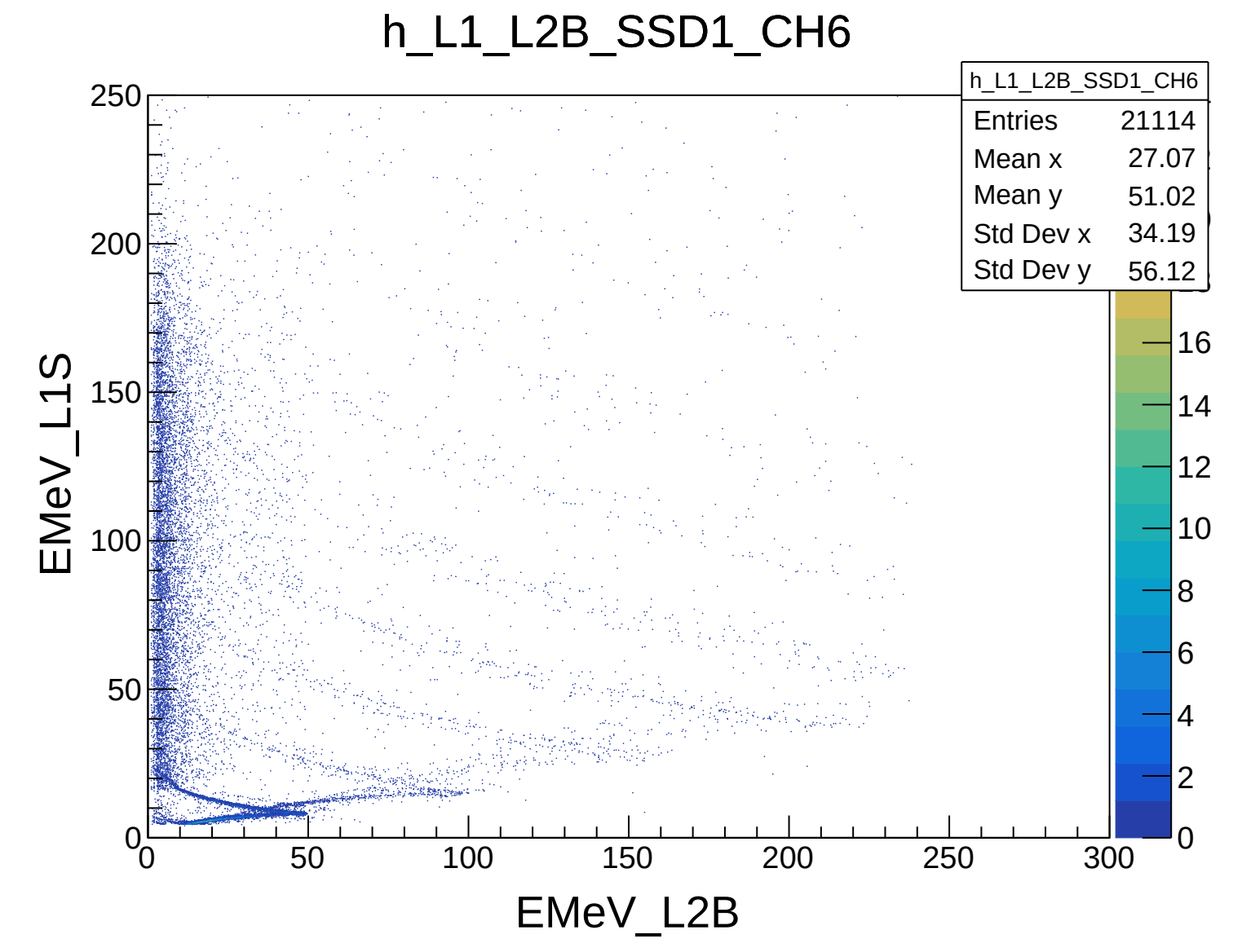

h_L1_L2B_SSD1_CH1
h_L1_L2B_SSD1_CH1
Entries 20865
Mean x 27.83
Mean y 47.75
Std Dev x 36.61
Std Dev y 54.45
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
2
4
6
8
10
12
14
16

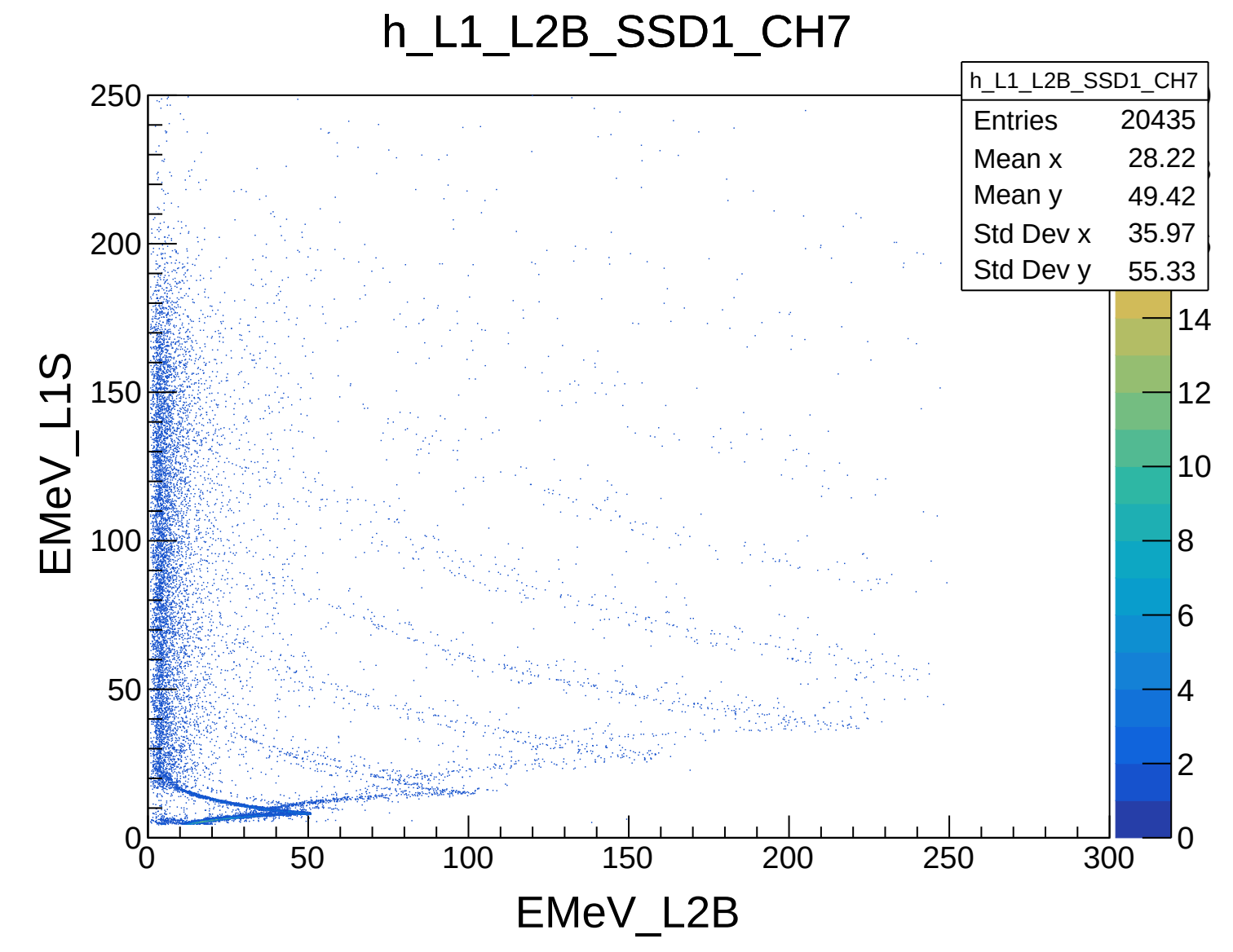

h_L1_L2B_SSD1_CH2
h_L1_L2B_SSD1_CH2
Entries 23220
Mean x 28.14
Mean y 53.97
Std Dev x 35.59
Std Dev y 57.68
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10
12
14
16

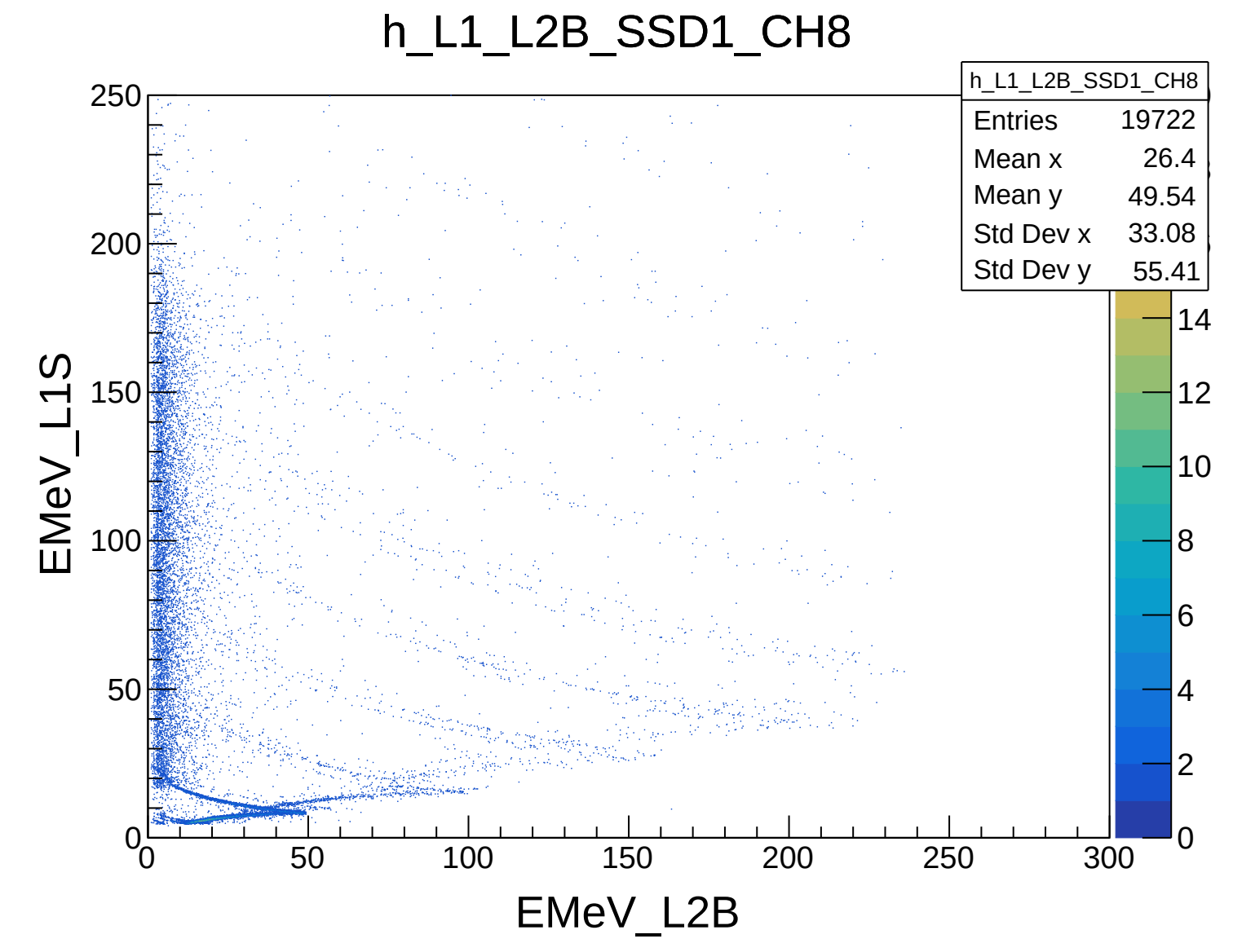

h_L1_L2B_SSD1_CH3
h_L1_L2B_SSD1_CH3
Entries 22826
Mean x 29.23
Mean y 53.73
Std Dev x 37.22
Std Dev y 58.03
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10
12
14
16

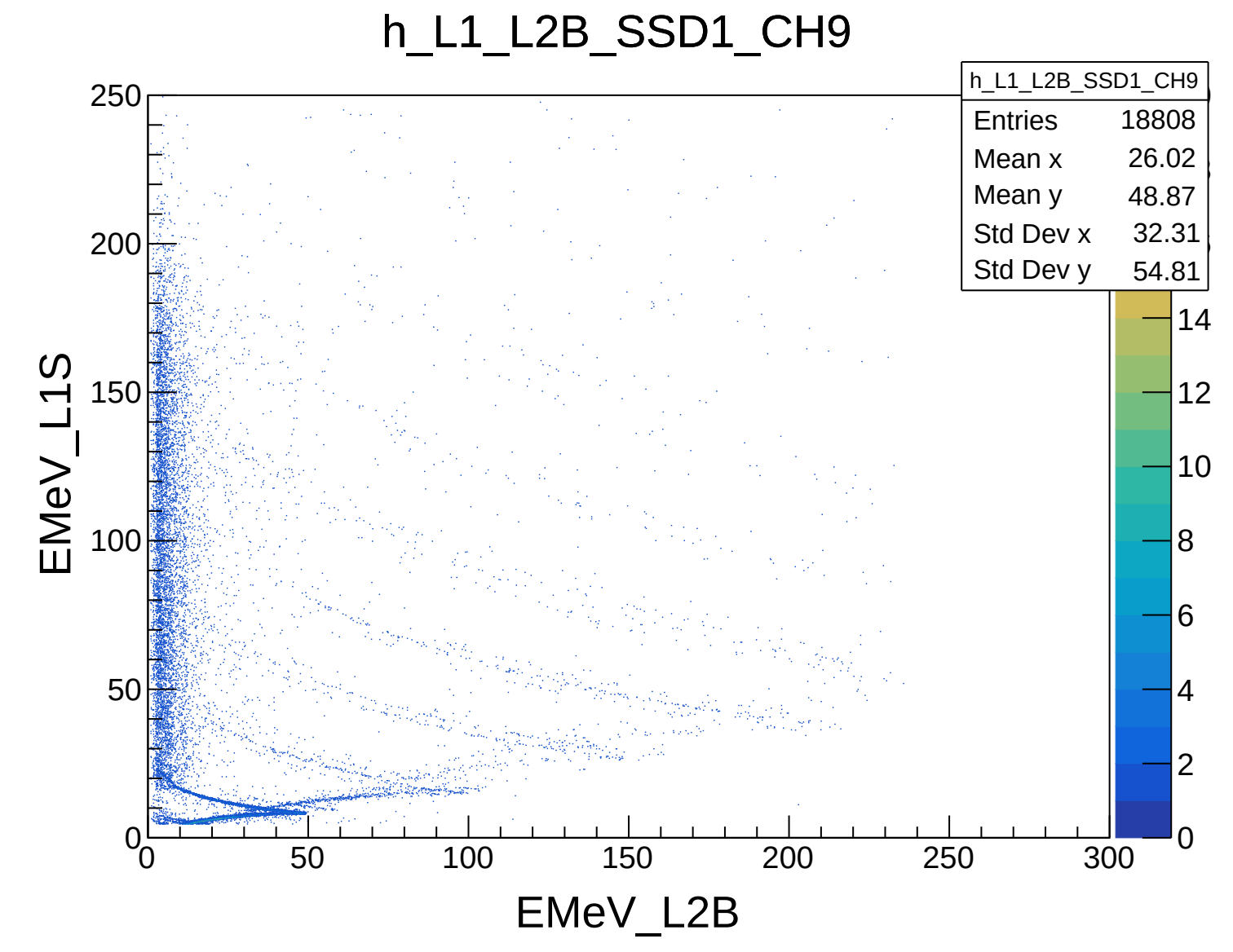

h_L1_L2B_SSD1_CH4
h_L1_L2B_SSD1_CH4
Entries 22278
Mean x 29.45
Mean y 52.4
Std Dev x 37.66
Std Dev y 56.64
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10
12
14

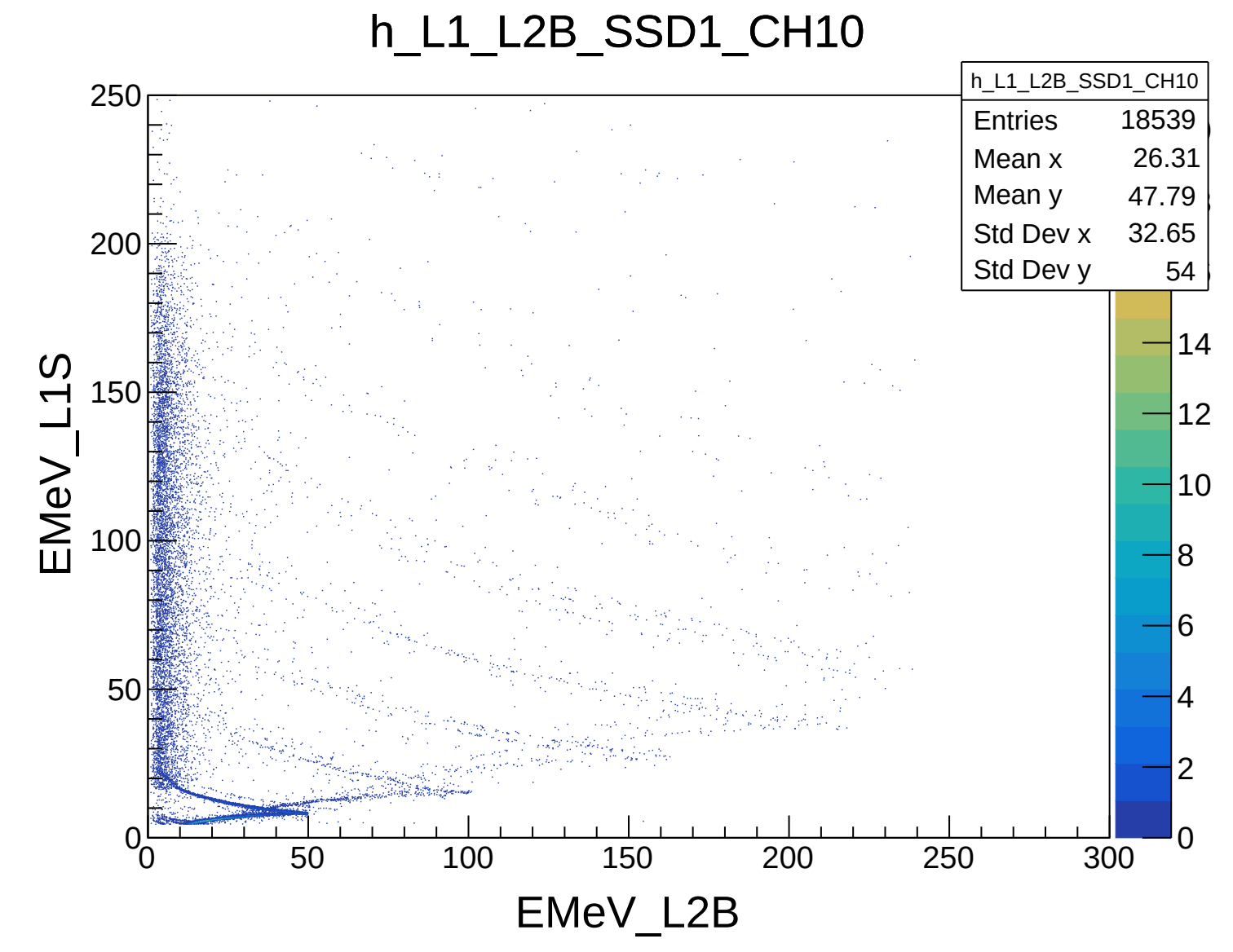

h_L1_L2B_SSD1_CH5
h_L1_L2B_SSD1_CH5
Entries 21809
Mean x 28.62
Mean y 52.14
Std Dev x 36.67
Std Dev y 56.95
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10
12
14

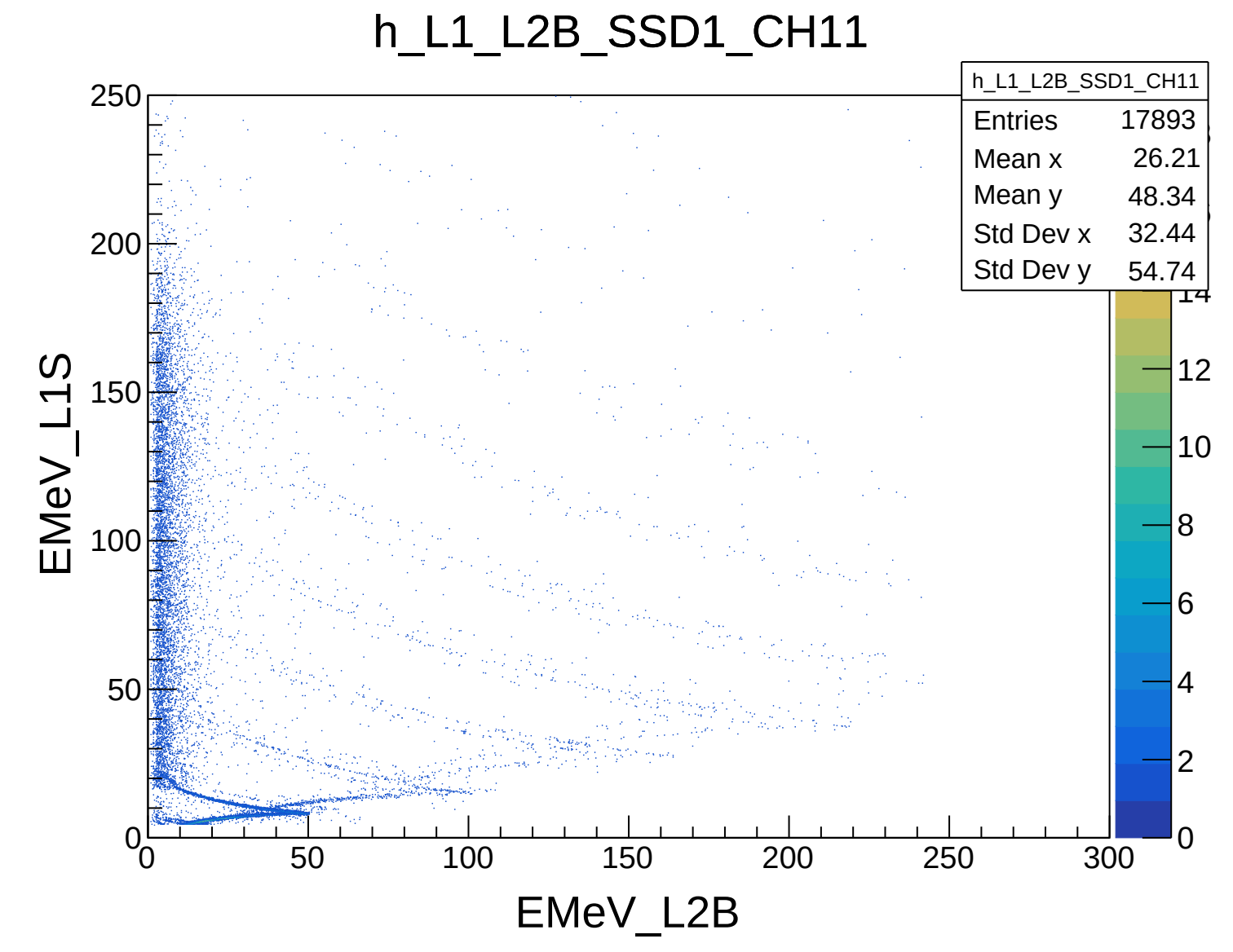

h_L1_L2B_SSD1_CH6
h_L1_L2B_SSD1_CH6
Entries 21114
Mean x 27.07
Mean y 51.02
Std Dev x 34.19
Std Dev y 56.12
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10
12
14
16

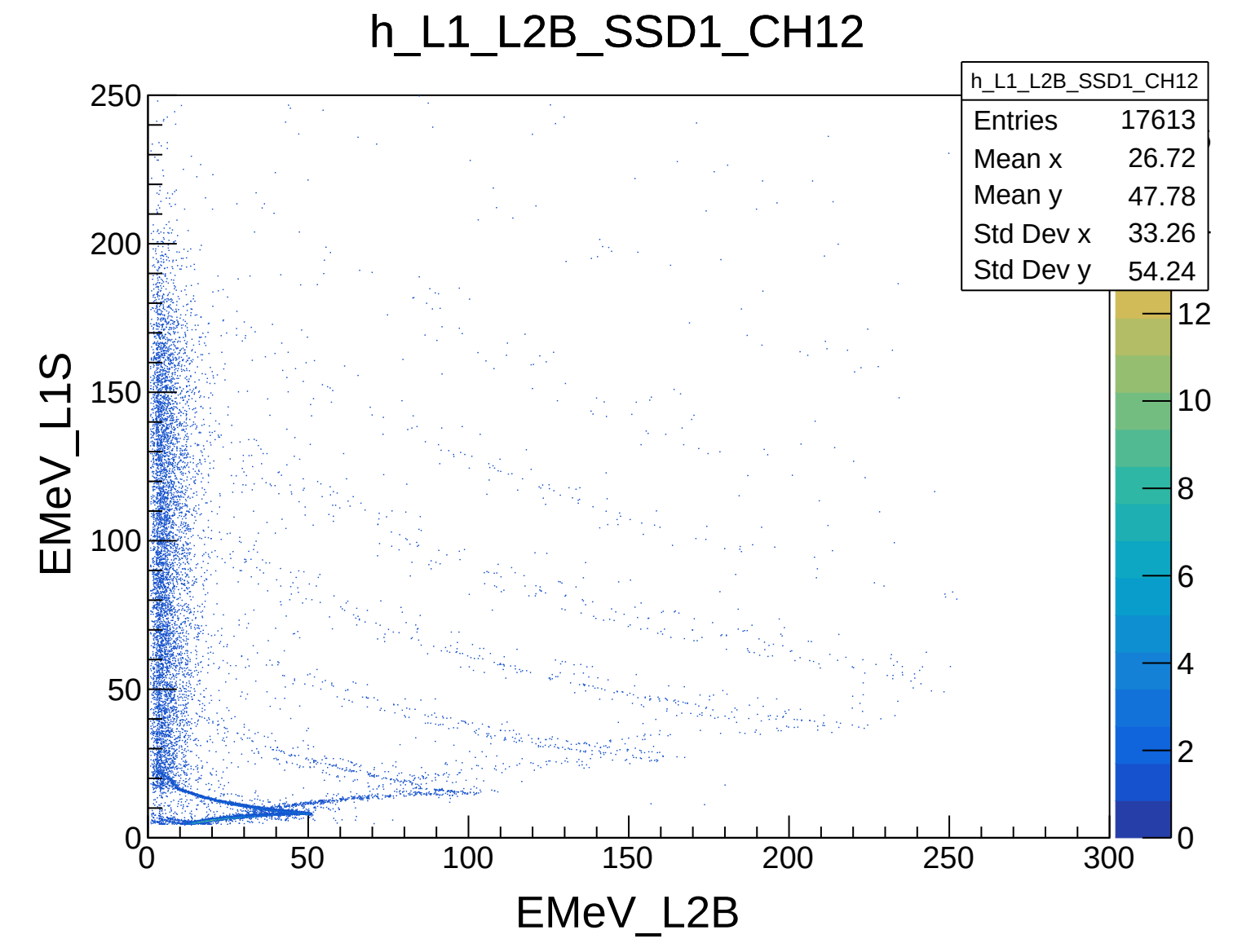

h_L1_L2B_SSD1_CH7
h_L1_L2B_SSD1_CH7
Entries 20435
Mean x 28.22
Mean y 49.42
Std Dev x 35.97
Std Dev y 55.33
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
2
4
6
8
10
12
14

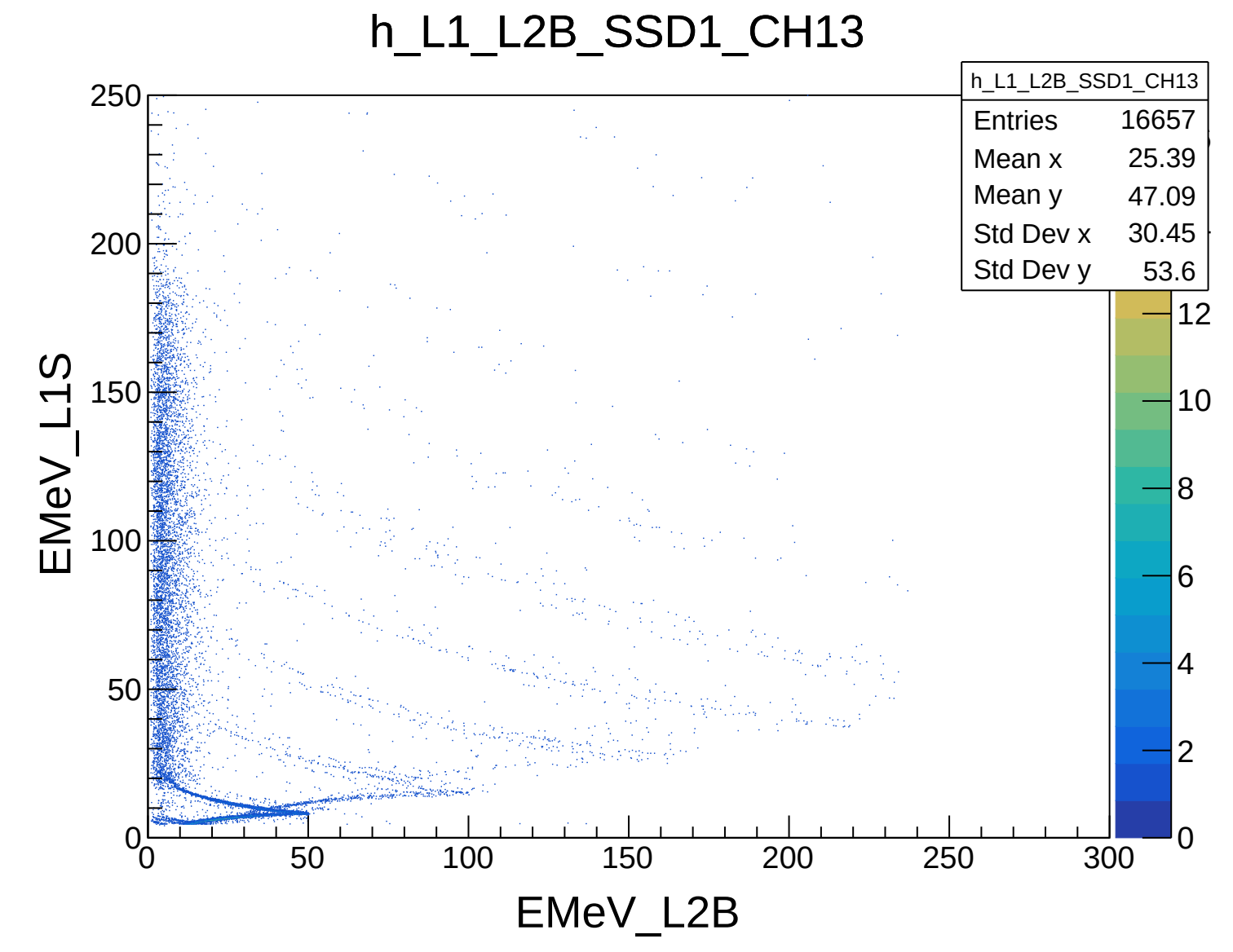

h_L1_L2B_SSD1_CH8
h_L1_L2B_SSD1_CH8
Entries 19722
Mean x 26.4
Mean y 49.54
Std Dev x 33.08
Std Dev y 55.41
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10
12
14

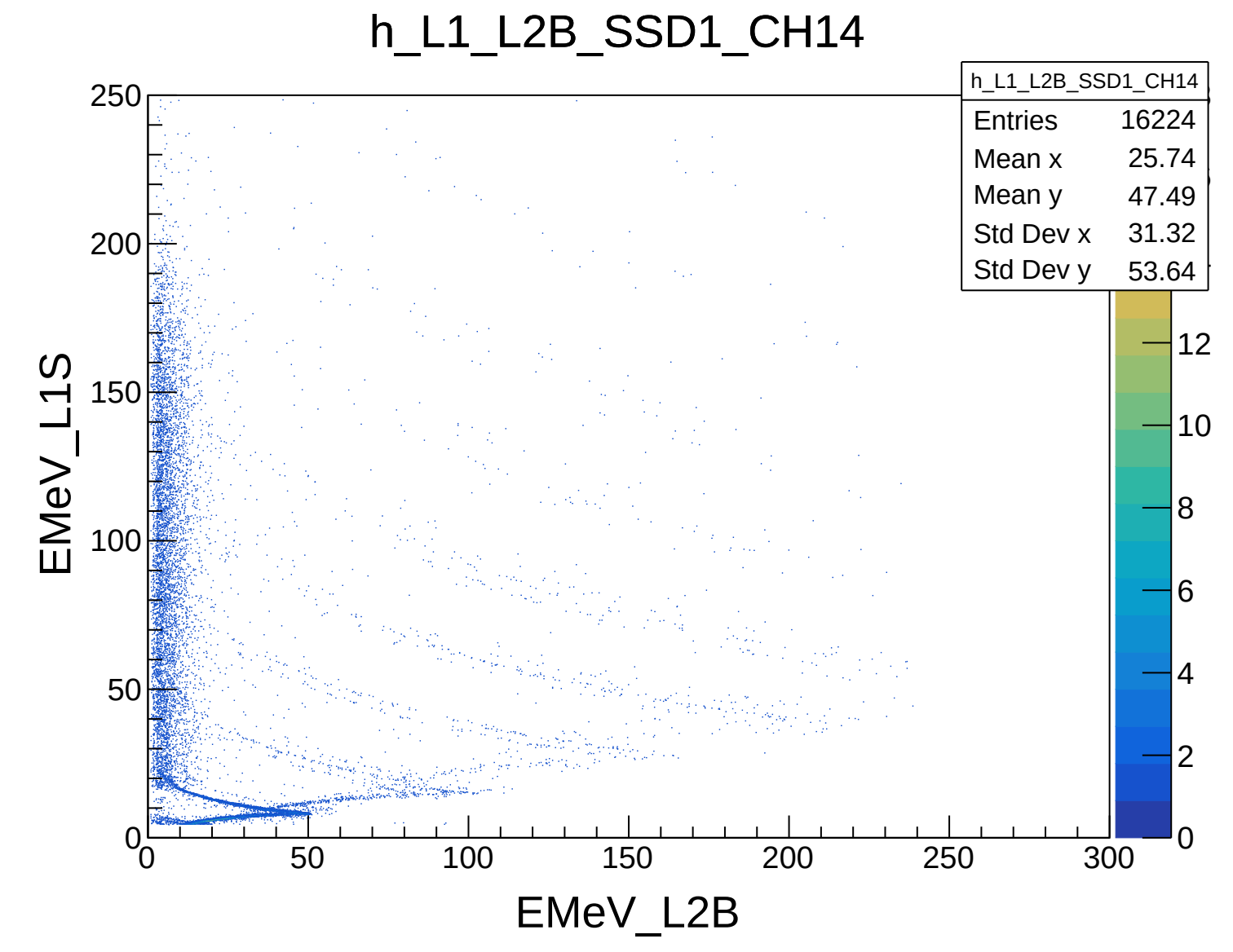

h_L1_L2B_SSD1_CH9
h_L1_L2B_SSD1_CH9
Entries 18808
Mean x 26.02
Mean y 48.87
Std Dev x 32.31
Std Dev y 54.81
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10
12
14

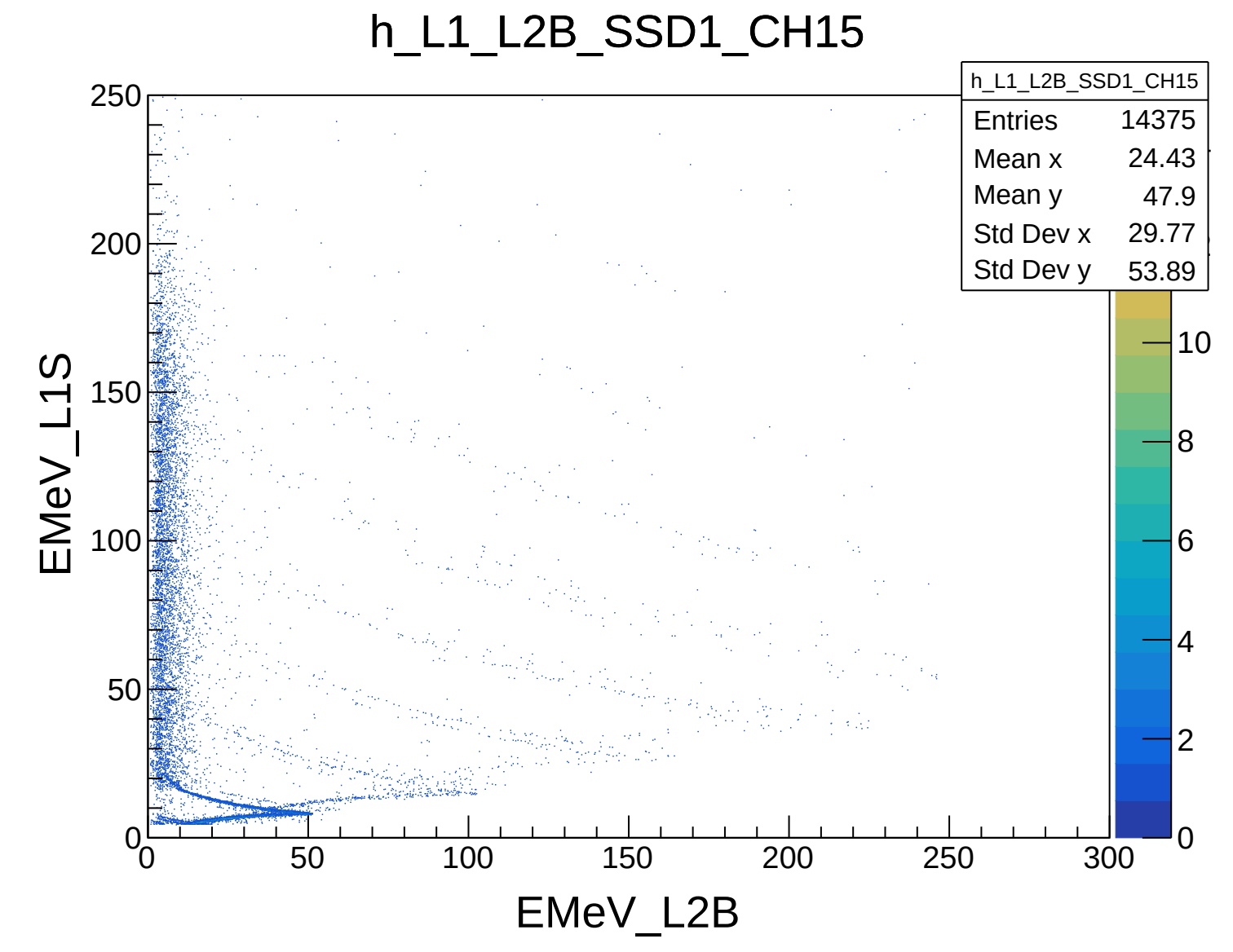

h_L1_L2B_SSD1_CH10
h_L1_L2B_SSD1_CH10
Entries 18539
Mean x 26.31
Mean y 47.79
Std Dev x 32.65
Std Dev y 54
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
2
4
6
8
10
12
14

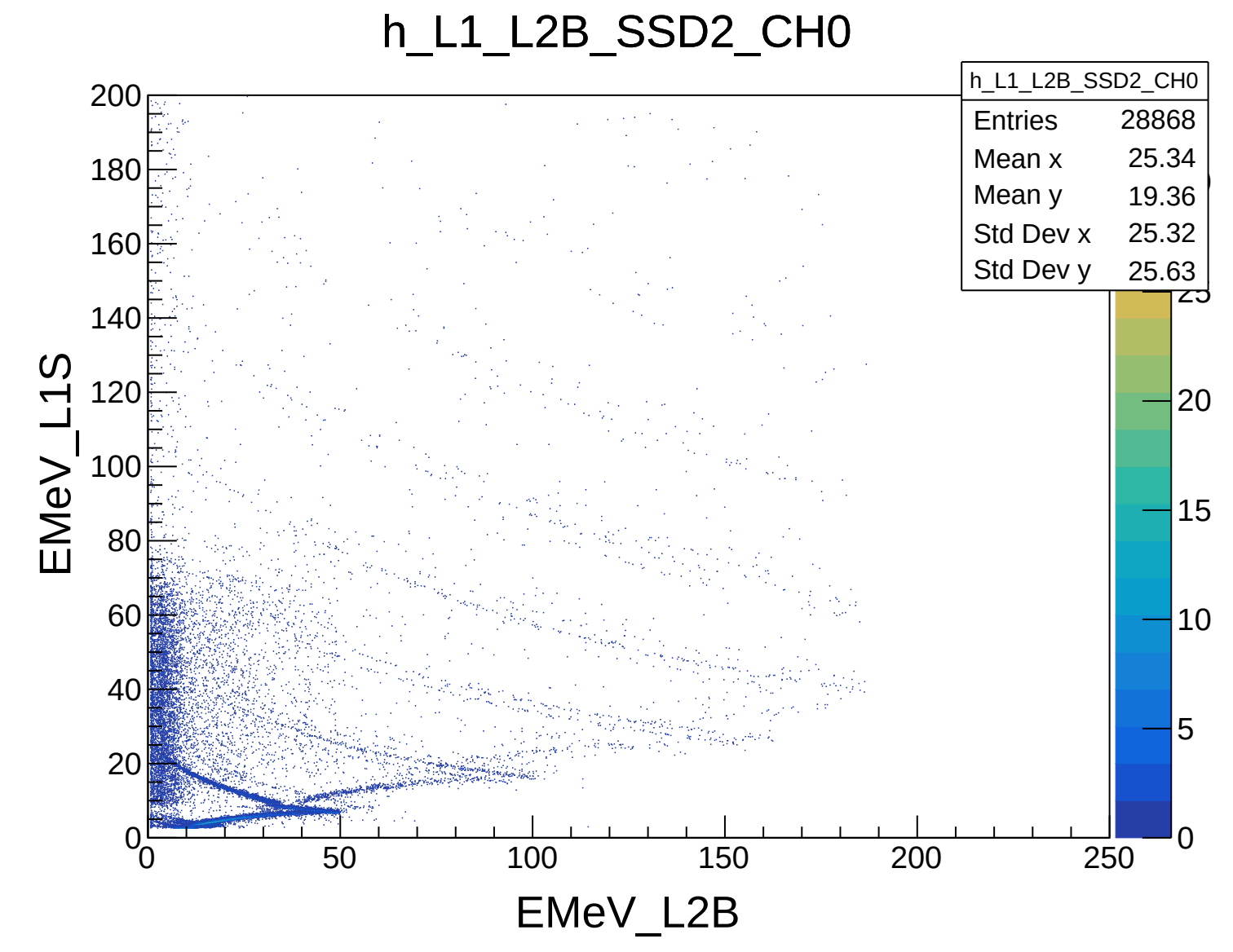

h_L1_L2B_SSD1_CH11
h_L1_L2B_SSD1_CH11
Entries 17893
Mean x 26.21
Mean y 48.34
Std Dev x 32.44
Std Dev y 54.74
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10
12
14

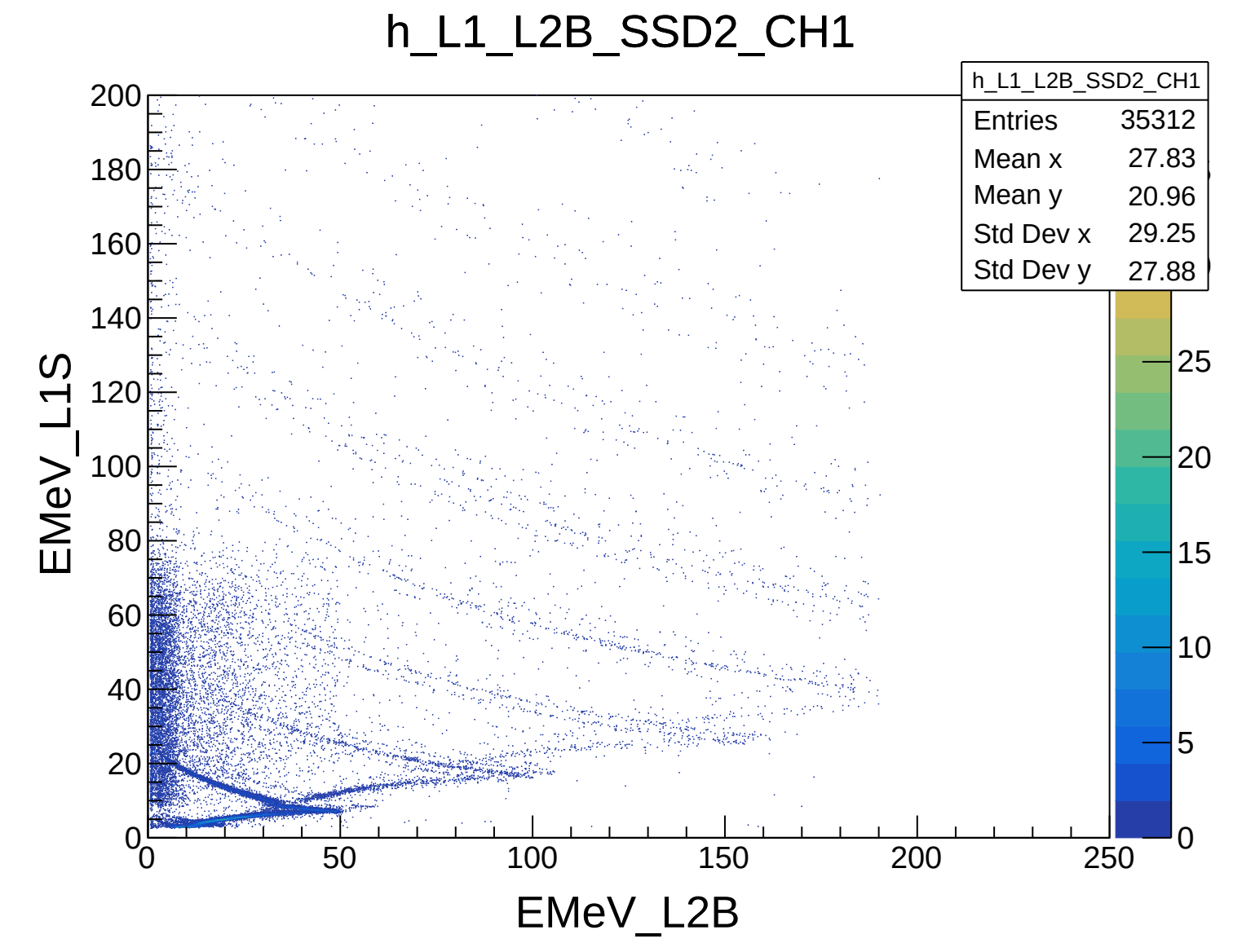

h_L1_L2B_SSD1_CH12
h_L1_L2B_SSD1_CH12
Entries 17613
Mean x 26.72
Mean y 47.78
Std Dev x 33.26
Std Dev y 54.24
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10
12

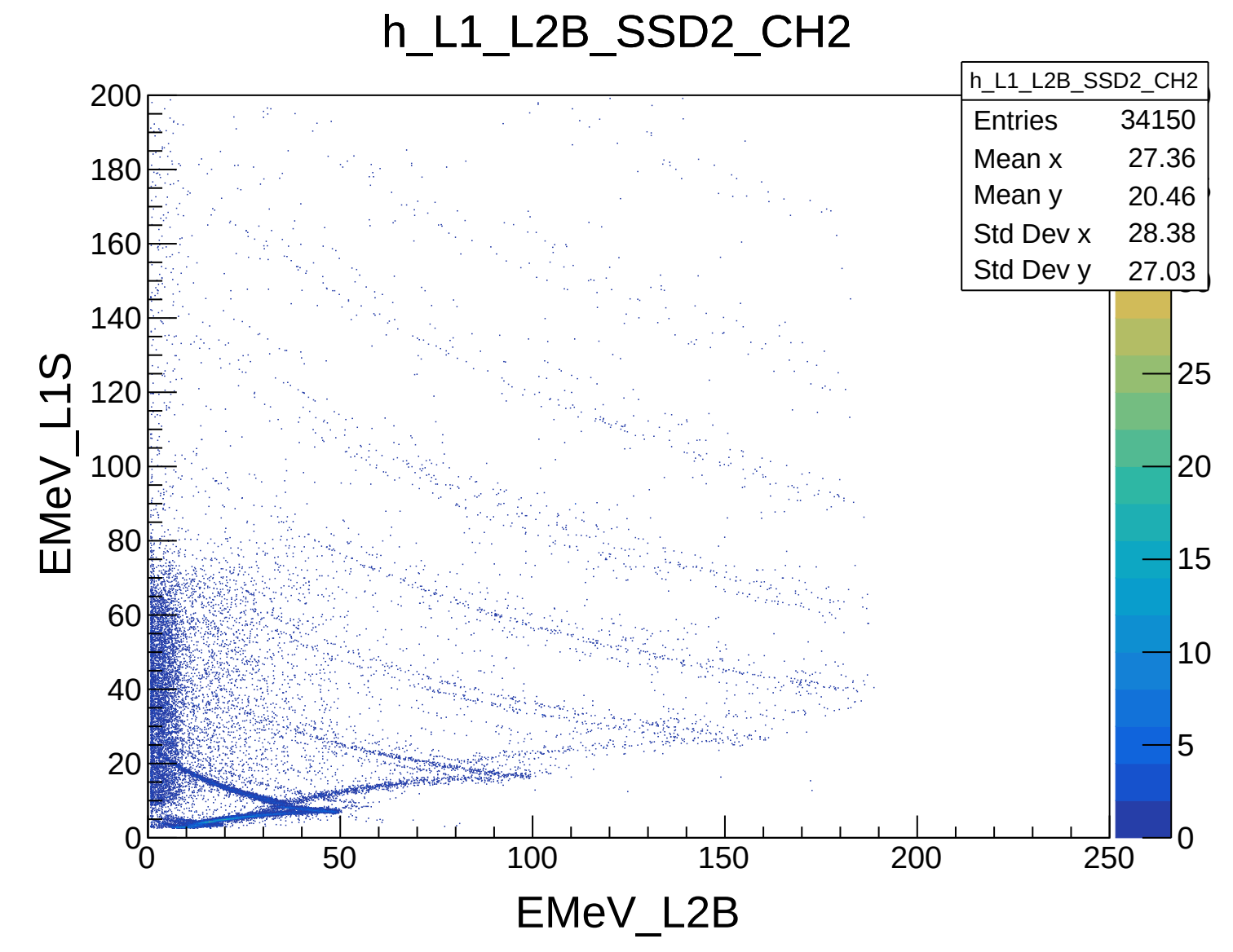

h_L1_L2B_SSD1_CH13
h_L1_L2B_SSD1_CH13
Entries 16657
Mean x 25.39
Mean y 47.09
Std Dev x 30.45
Std Dev y 53.6
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10
12

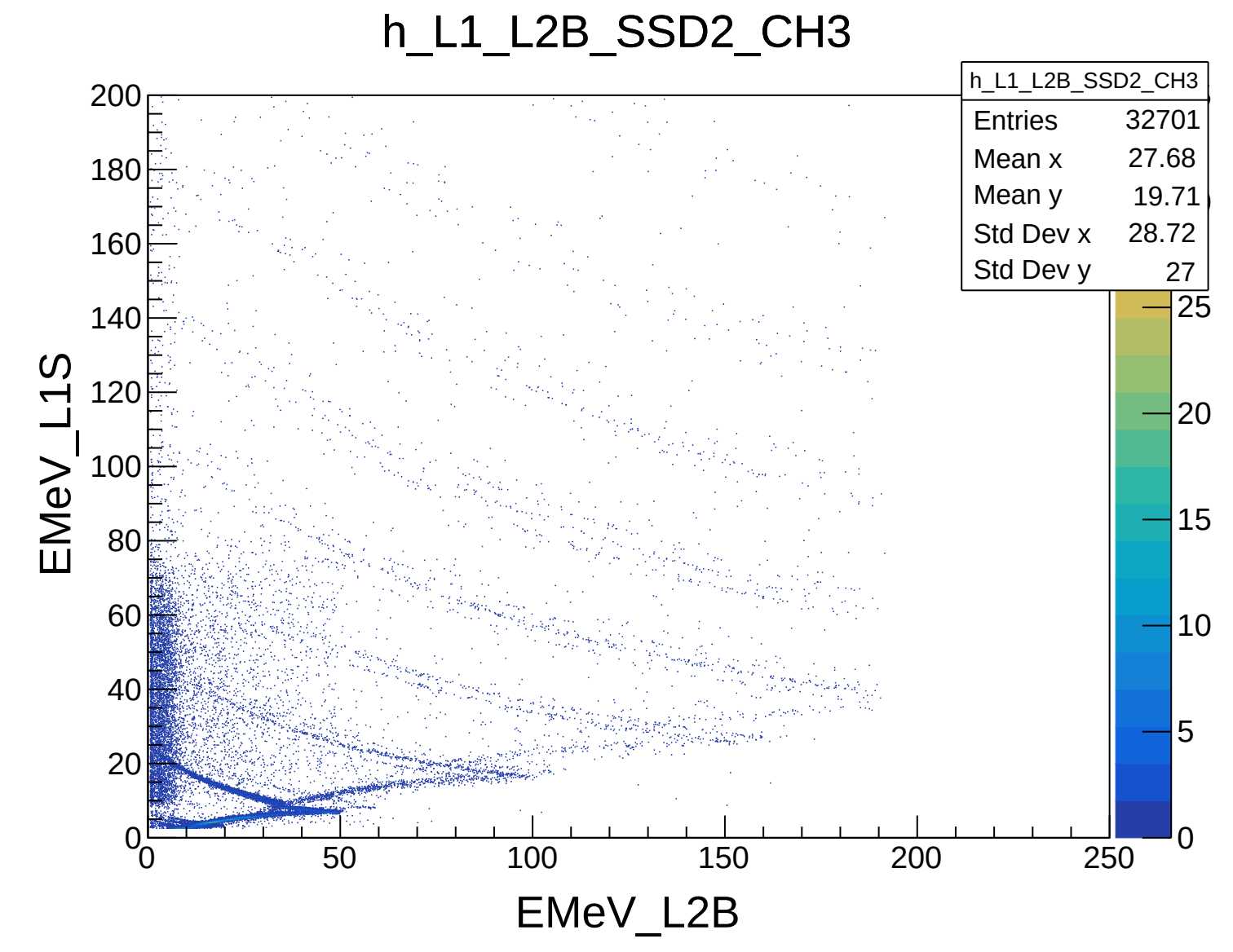

h_L1_L2B_SSD1_CH14
h_L1_L2B_SSD1_CH14
Entries 16224
Mean x 25.74
Mean y 47.49
Std Dev x 31.32
Std Dev y 53.64
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10
12

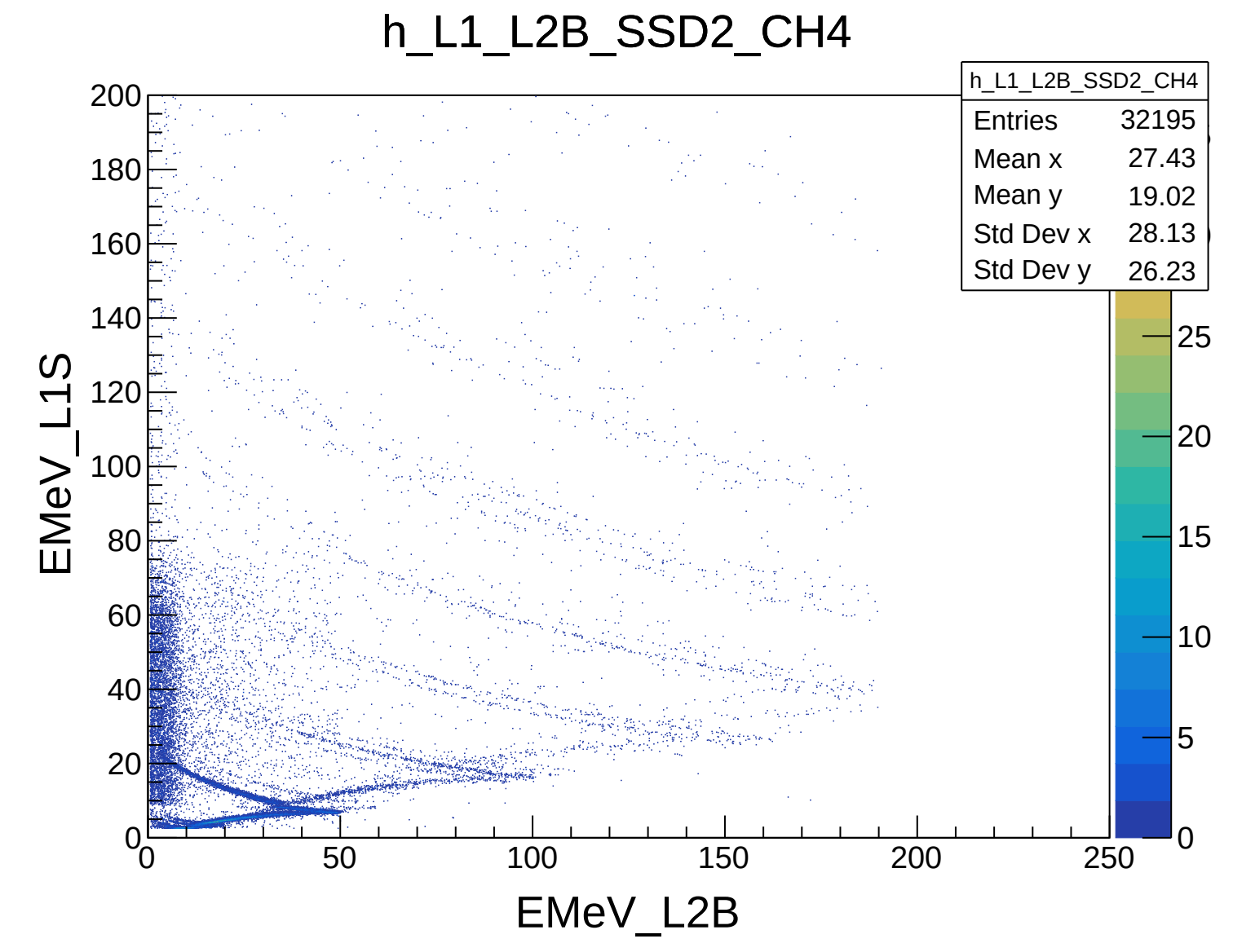

h_L1_L2B_SSD1_CH15
h_L1_L2B_SSD1_CH15
Entries 14375
Mean x 24.43
Mean y 47.9
Std Dev x 29.77
Std Dev y 53.89
EMeV_L1S
EMeV_L2B
0
50
100
150
200
250
300
0
2
4
6
8
10

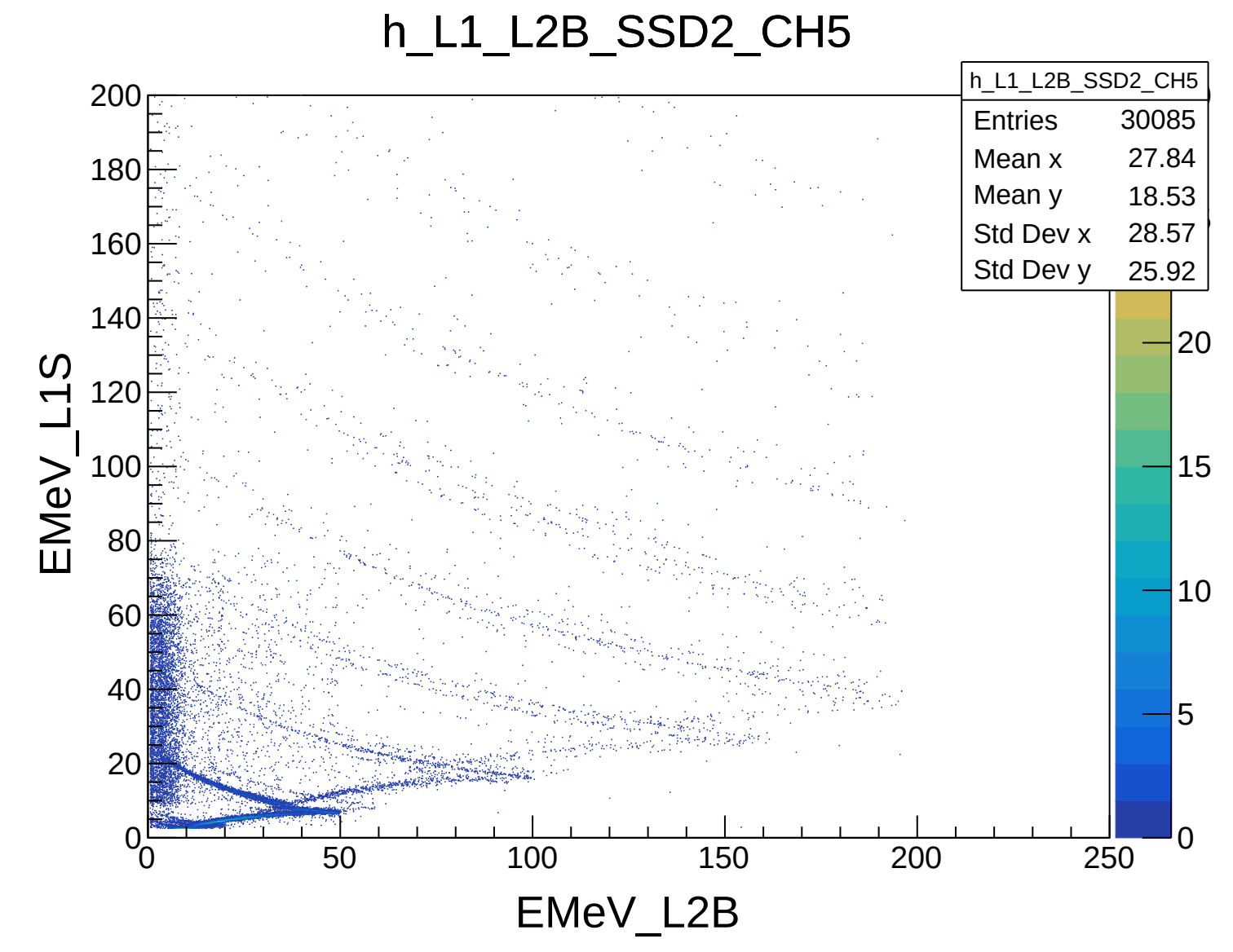

h_L1_L2B_SSD2_CH0
h_L1_L2B_SSD2_CH0
Entries 28868
Mean x 25.34
Mean y 19.36
Std Dev x 25.32
Std Dev y 25.63
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
5
10
15
20

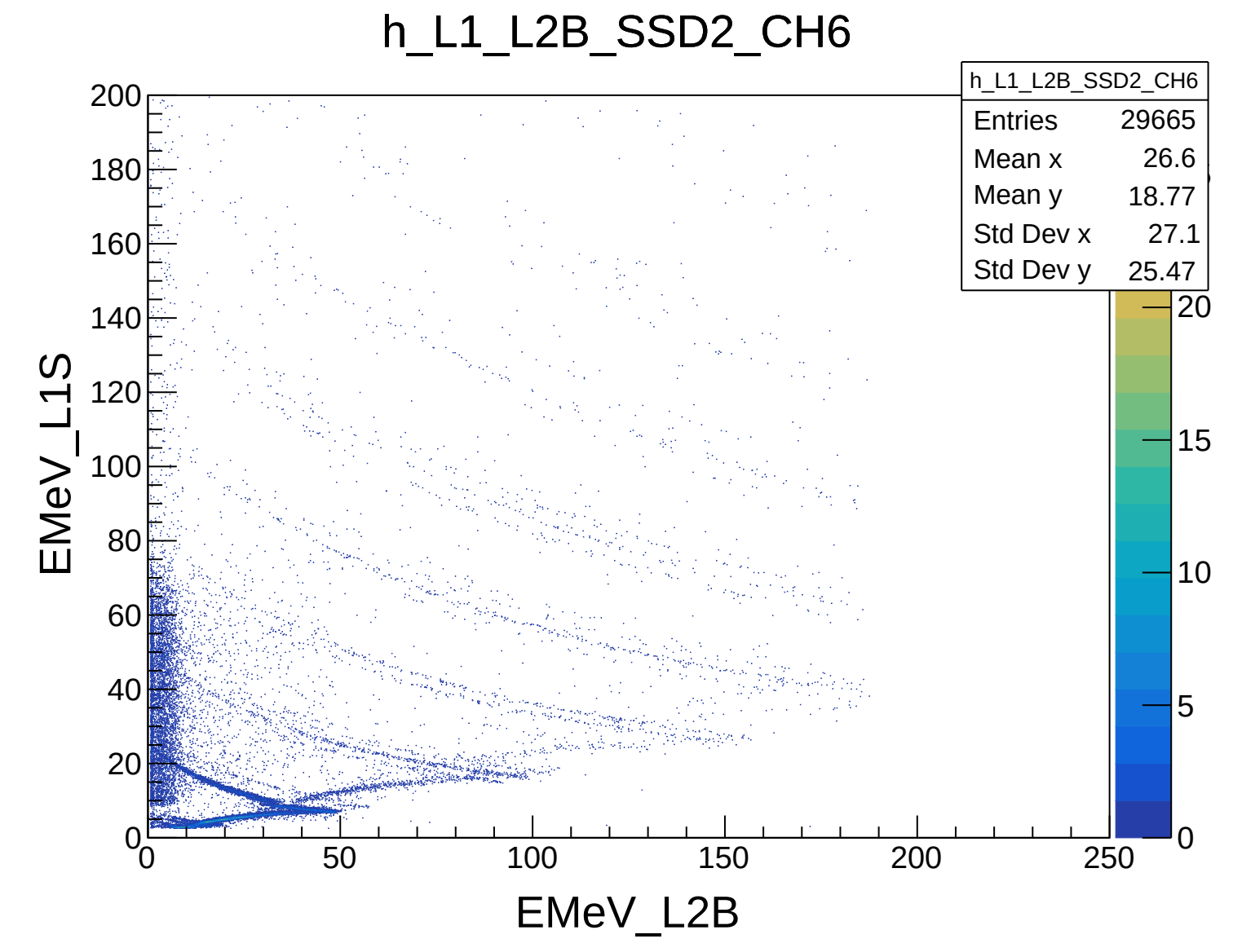

h_L1_L2B_SSD2_CH1
h_L1_L2B_SSD2_CH1
Entries 35312
Mean x 27.83
Mean y 20.96
Std Dev x 29.25
Std Dev y 27.88
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
5
10
15
20
25

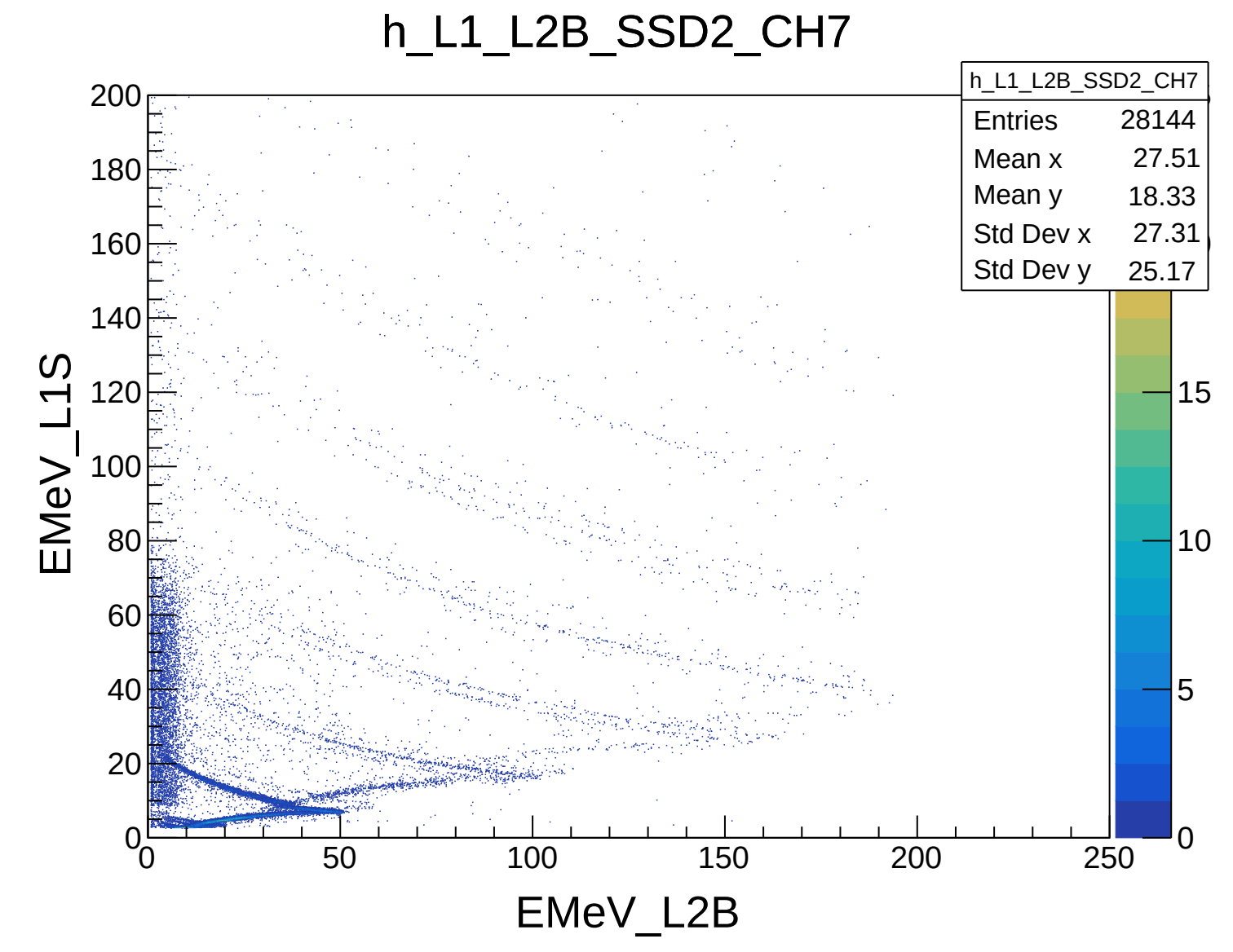

h_L1_L2B_SSD2_CH2
h_L1_L2B_SSD2_CH2
Entries 34150
Mean x 27.36
Mean y 20.46
Std Dev x 28.38
Std Dev y 27.03
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
5
10
15
20
25

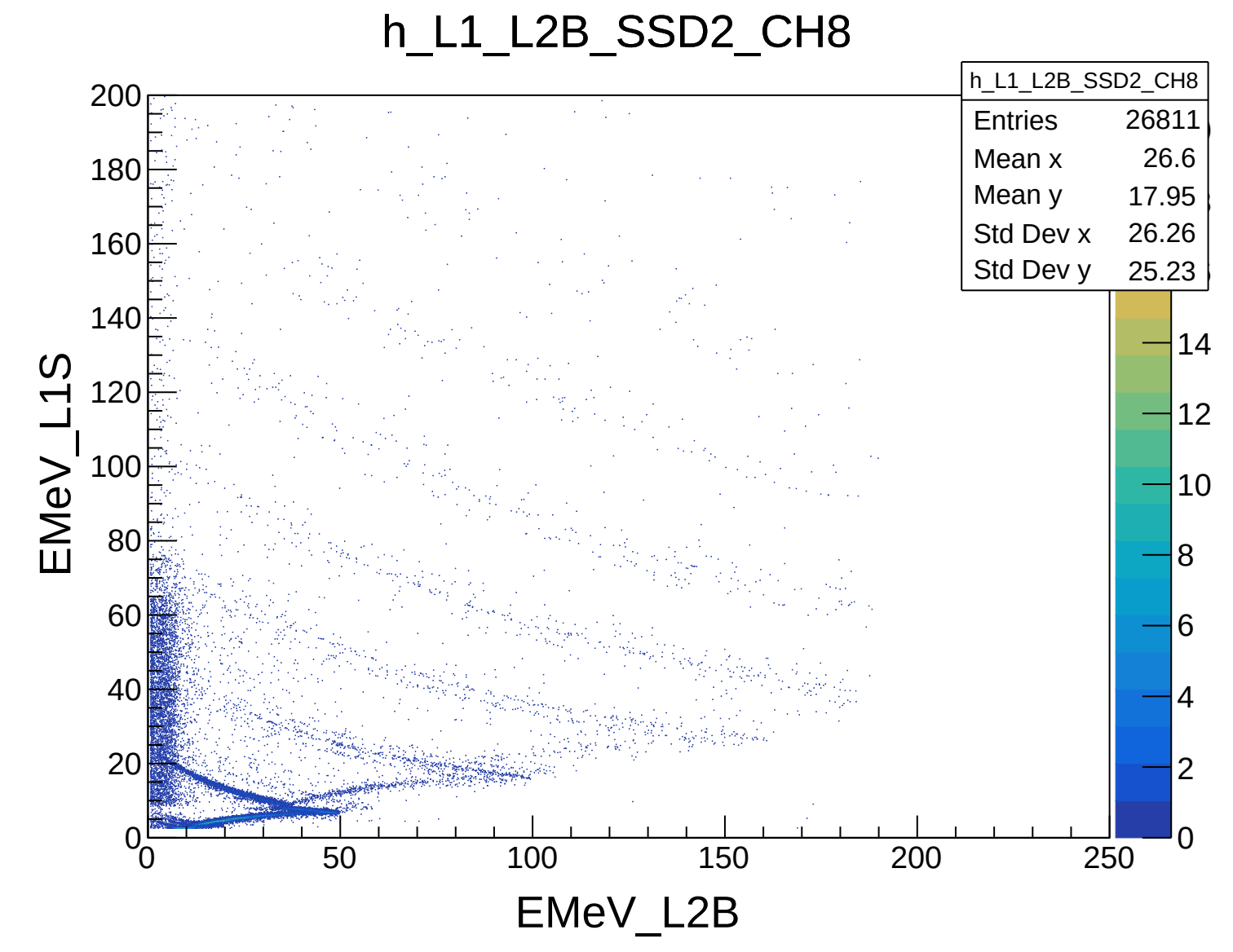

h_L1_L2B_SSD2_CH3
h_L1_L2B_SSD2_CH3
Entries 32701
Mean x 27.68
Mean y 19.71
Std Dev x 28.72
Std Dev y 27
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
5
10
15
20
25

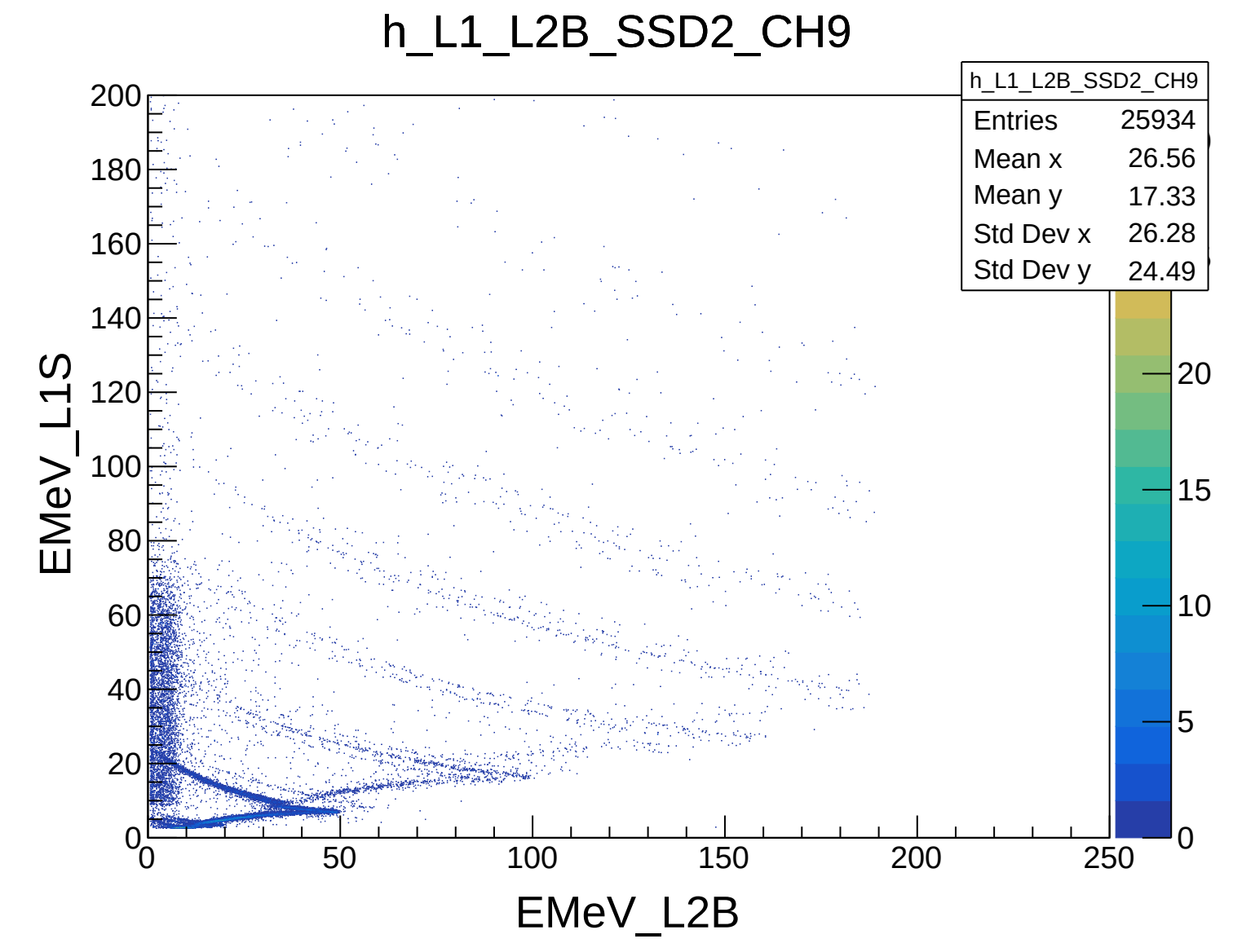

h_L1_L2B_SSD2_CH4
h_L1_L2B_SSD2_CH4
Entries 32195
Mean x 27.43
Mean y 19.02
Std Dev x 28.13
Std Dev y 26.23
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
5
10
15
20
25

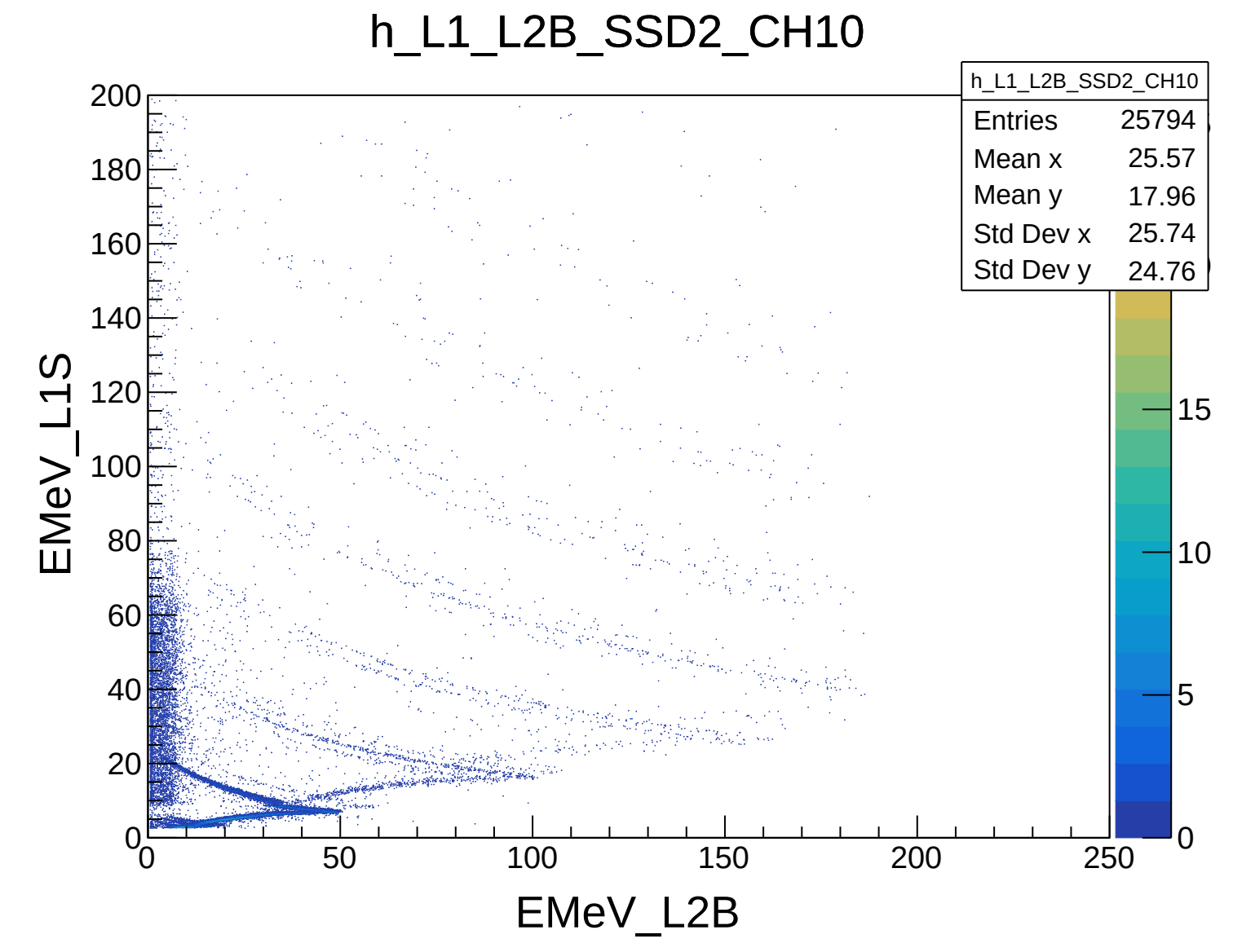

h_L1_L2B_SSD2_CH5
h_L1_L2B_SSD2_CH5
Entries 30085
Mean x 27.84
Mean y 18.53
Std Dev x 28.57
Std Dev y 25.92
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
5
10
15
20

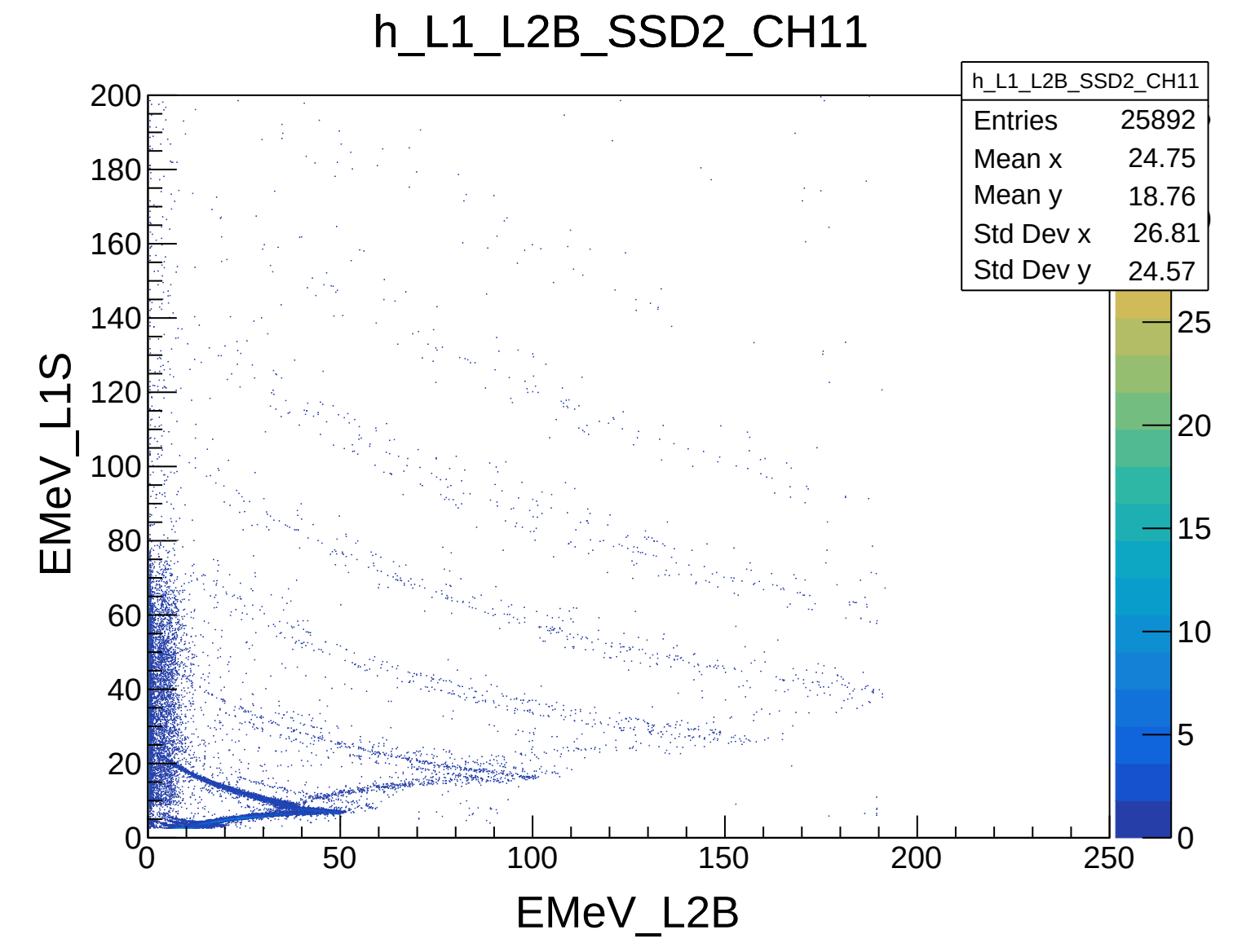

h_L1_L2B_SSD2_CH6
h_L1_L2B_SSD2_CH6
Entries 29665
Mean x 26.6
Mean y 18.77
Std Dev x 27.1
Std Dev y 25.47
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
5
10
15
20

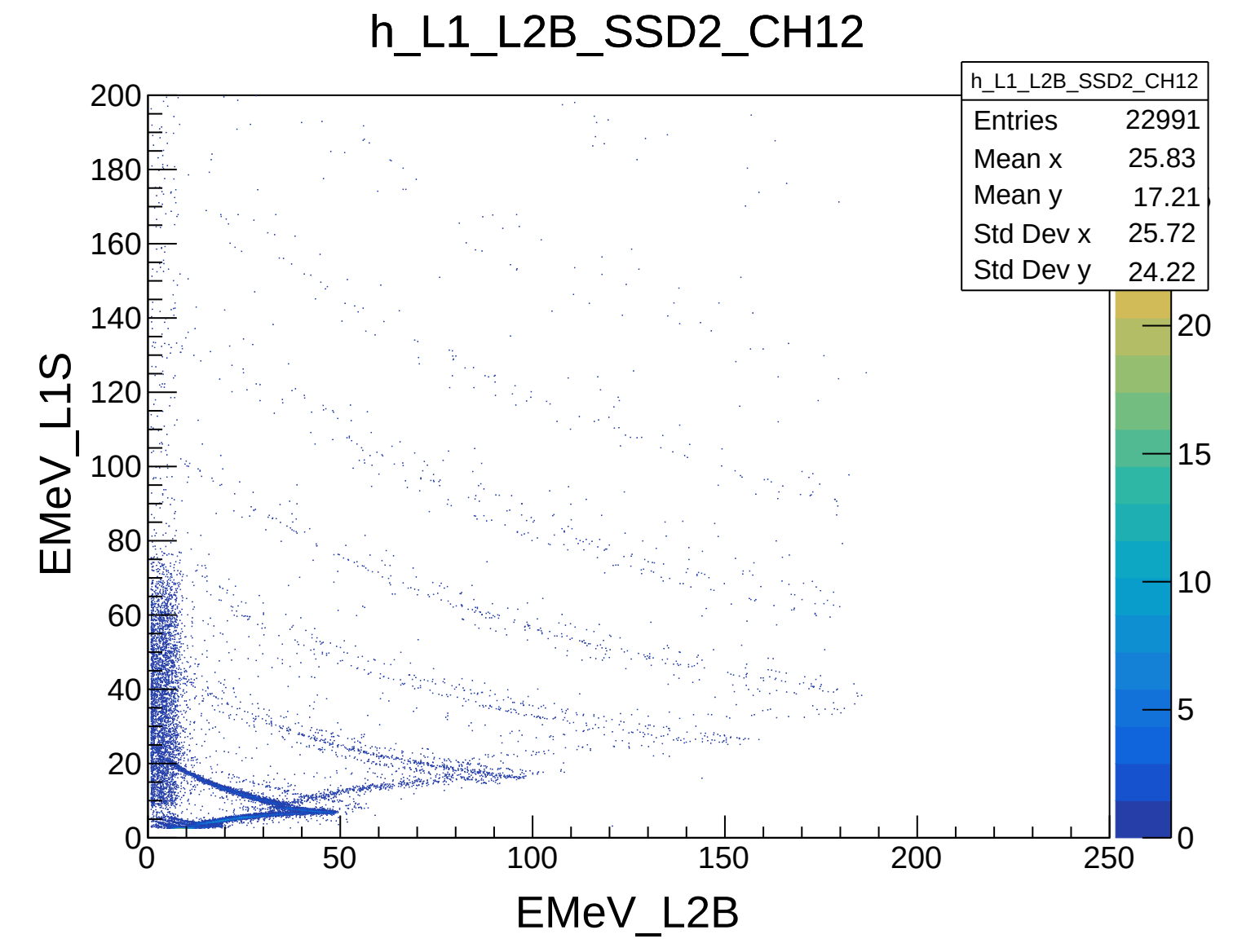

h_L1_L2B_SSD2_CH7
h_L1_L2B_SSD2_CH7
Entries 28144
Mean x 27.51
Mean y 18.33
Std Dev x 27.31
Std Dev y 25.17
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
5
10
15

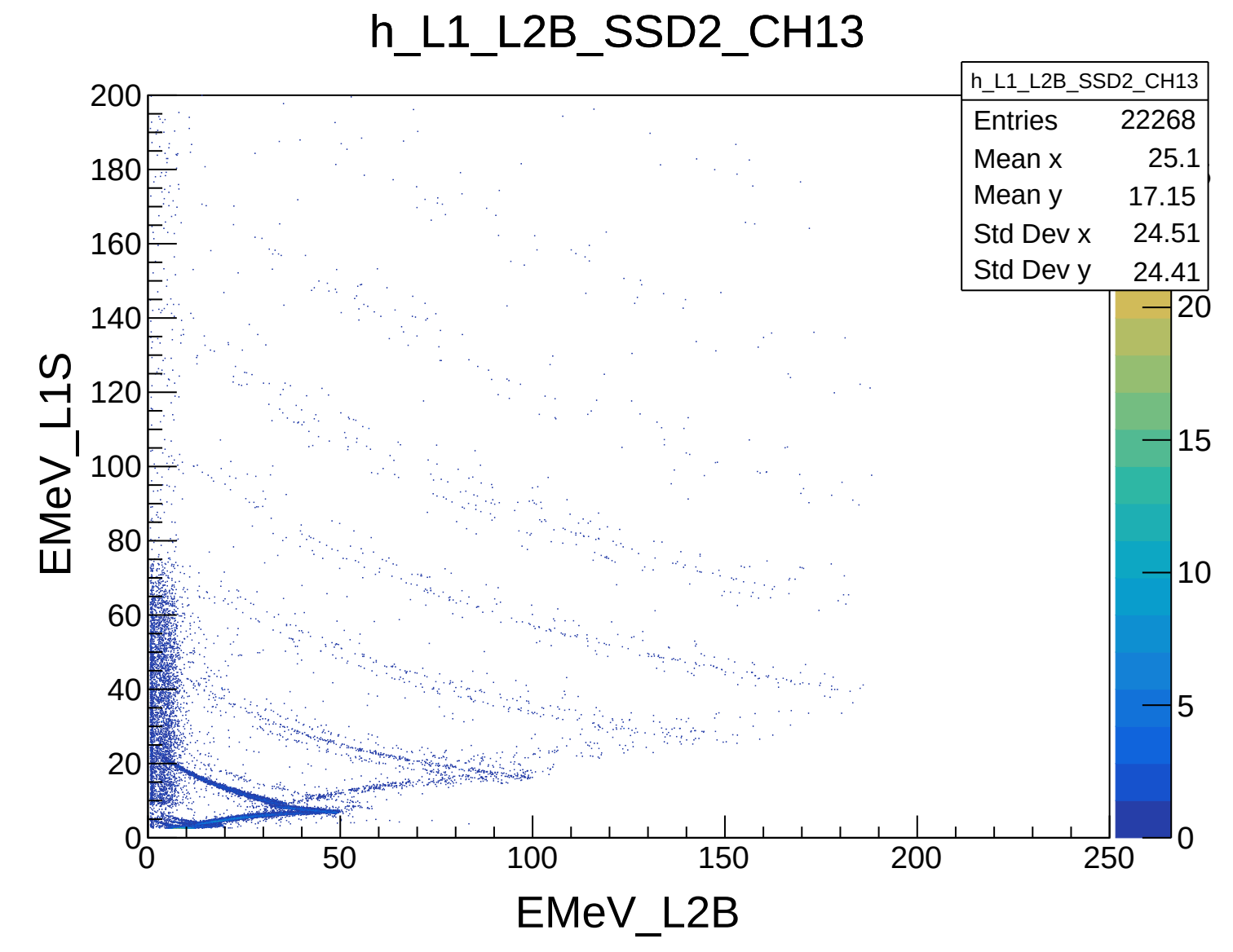

h_L1_L2B_SSD2_CH8
h_L1_L2B_SSD2_CH8
Entries 26811
Mean x 26.6
Mean y 17.95
Std Dev x 26.26
Std Dev y 25.23
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10
12
14

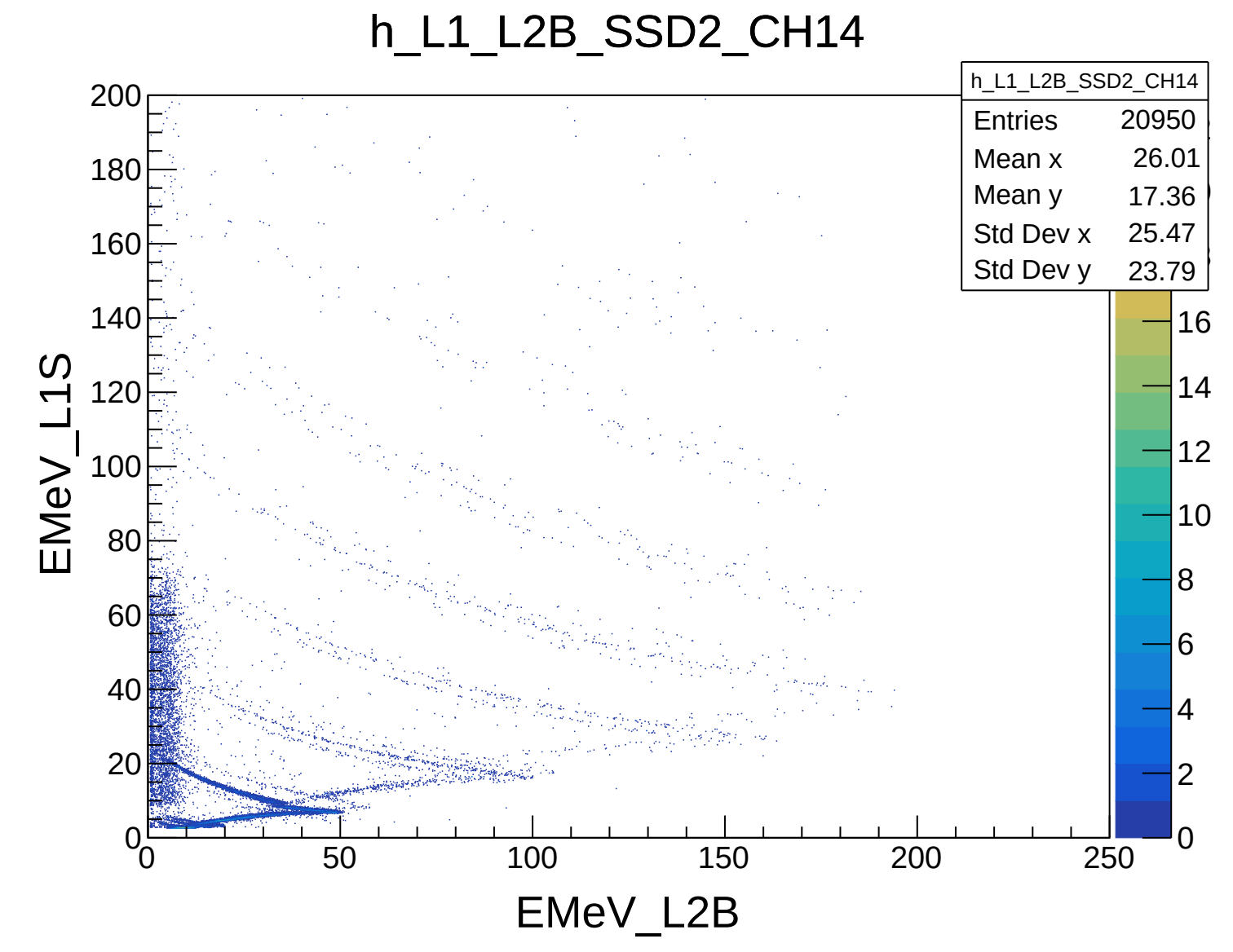

h_L1_L2B_SSD2_CH9
h_L1_L2B_SSD2_CH9
Entries 25934
Mean x 26.56
Mean y 17.33
Std Dev x 26.28
Std Dev y 24.49
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
5
10
15
20

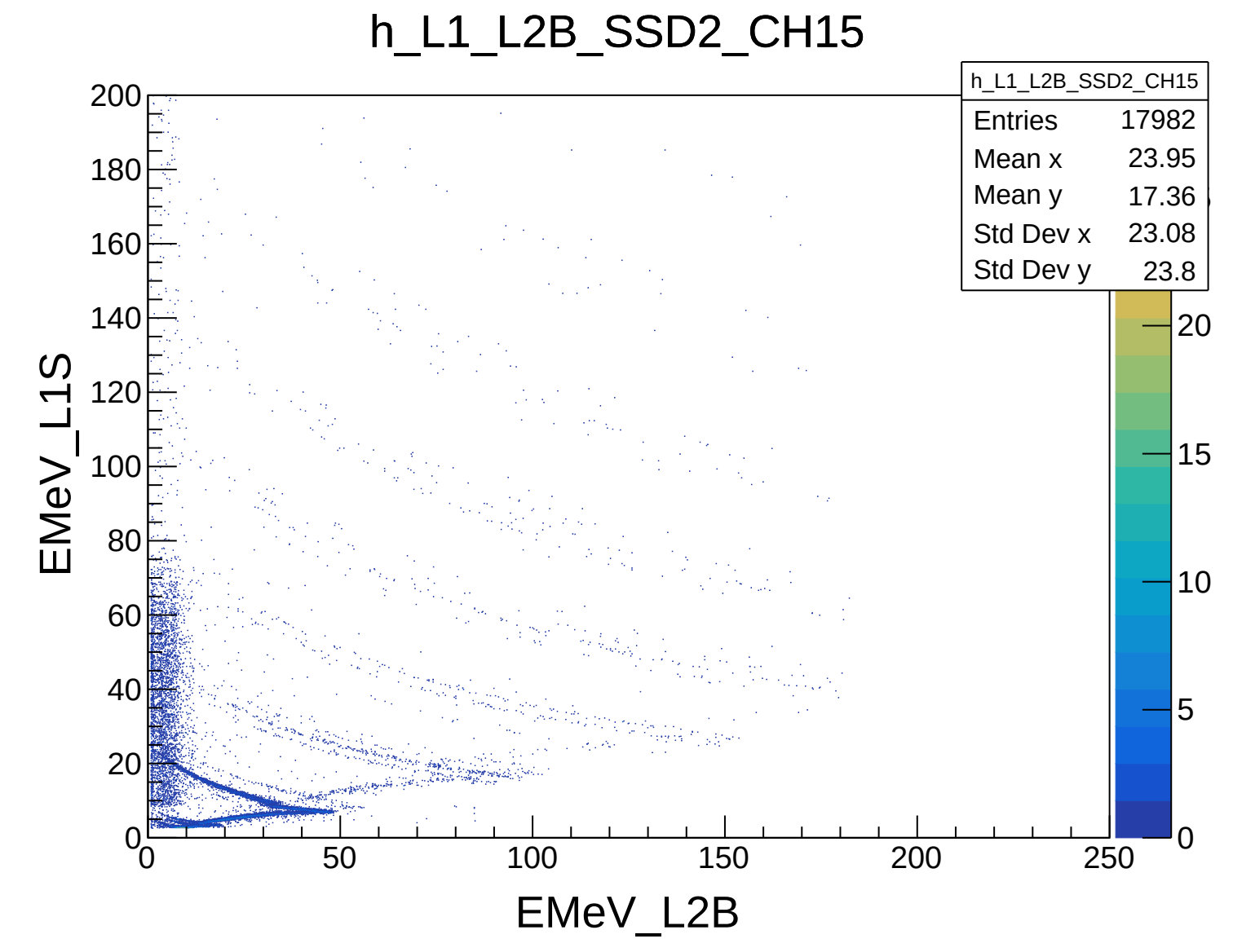

h_L1_L2B_SSD2_CH10
h_L1_L2B_SSD2_CH10
Entries 25794
Mean x 25.57
Mean y 17.96
Std Dev x 25.74
Std Dev y 24.76
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
5
10
15

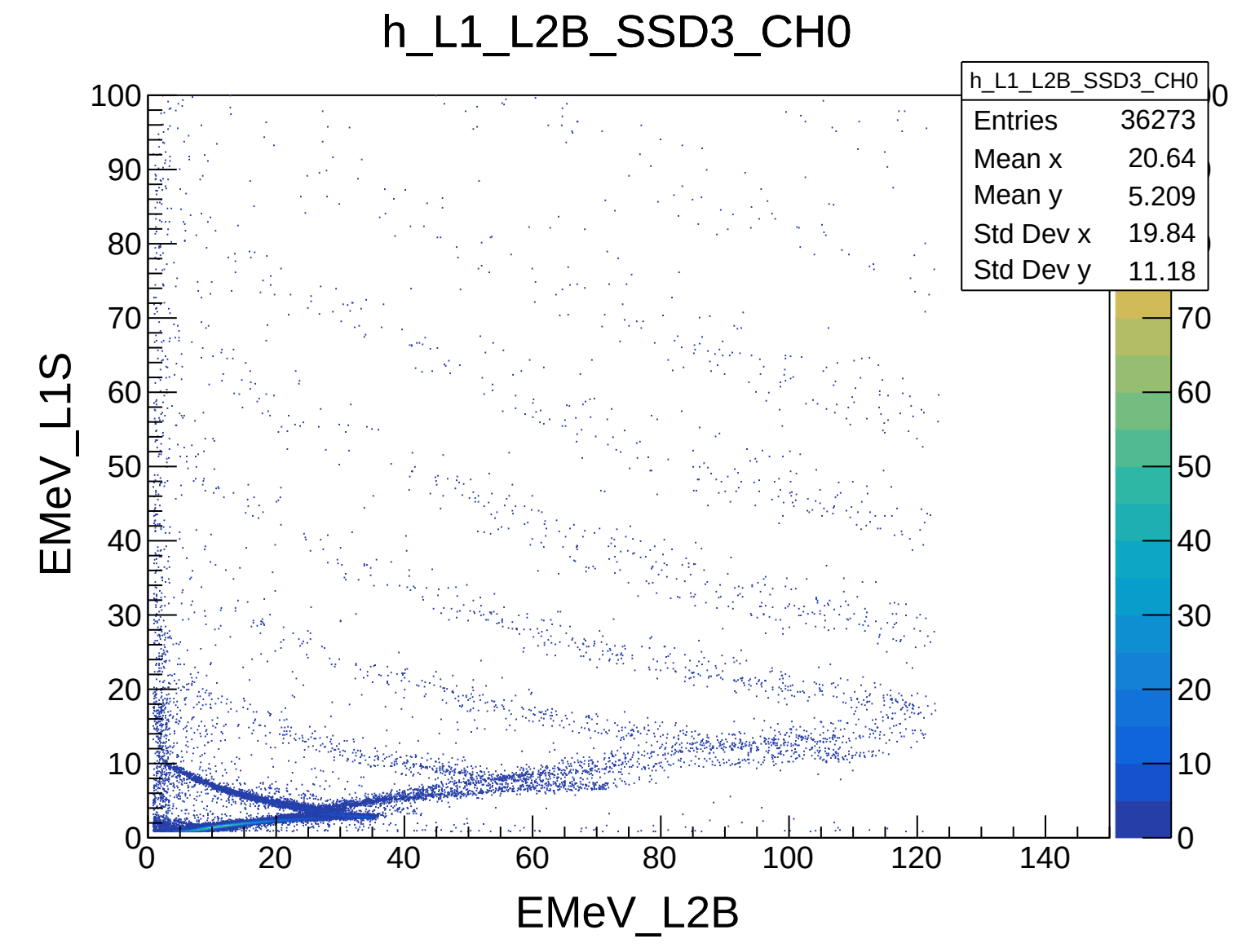

h_L1_L2B_SSD2_CH11
h_L1_L2B_SSD2_CH11
Entries 25892
Mean x 24.75
Mean y 18.76
Std Dev x 26.81
Std Dev y 24.57
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
5
10
15
20
25

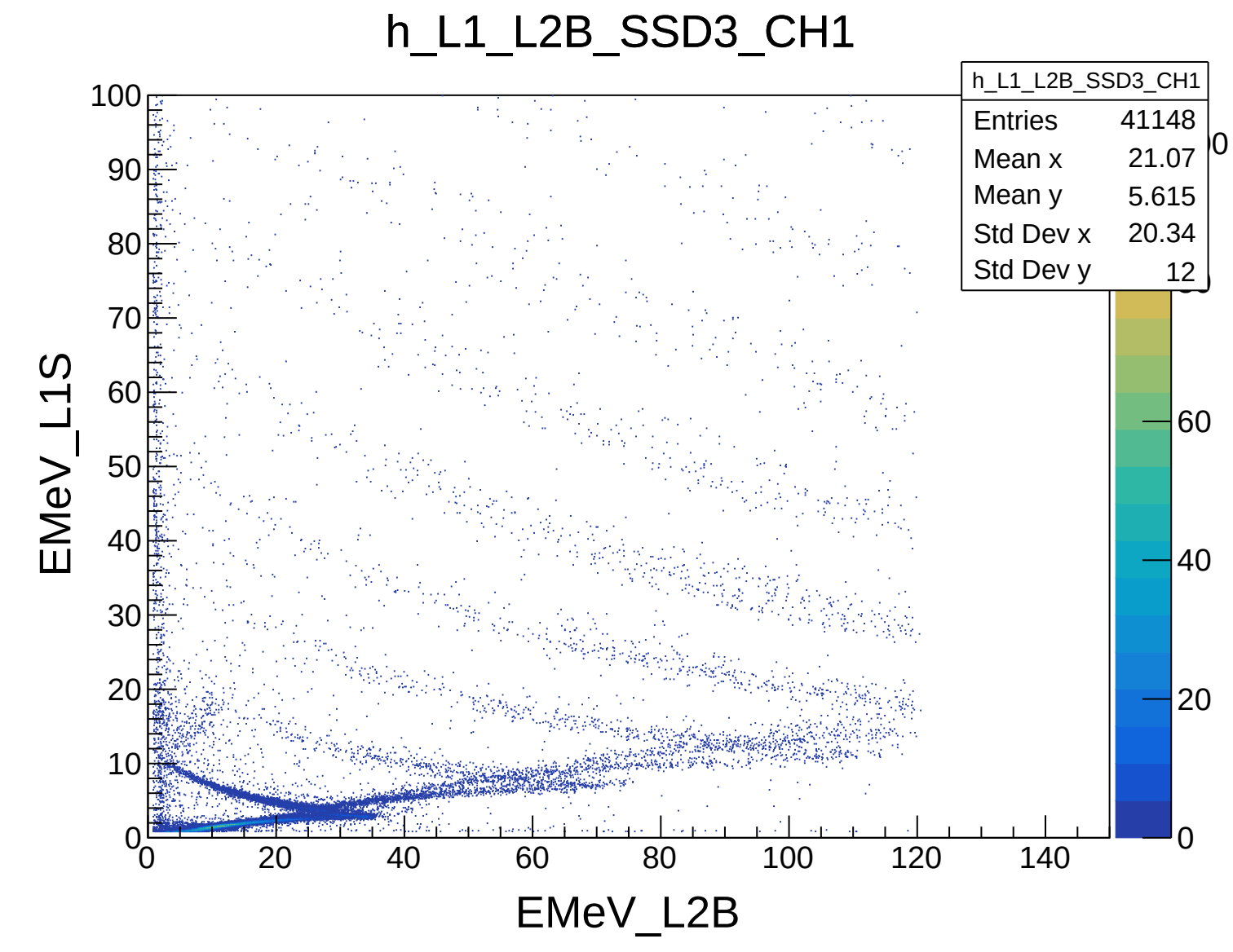

h_L1_L2B_SSD2_CH12
h_L1_L2B_SSD2_CH12
Entries 22991
Mean x 25.83
Mean y 17.21
Std Dev x 25.72
Std Dev y 24.22
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
5
10
15
20

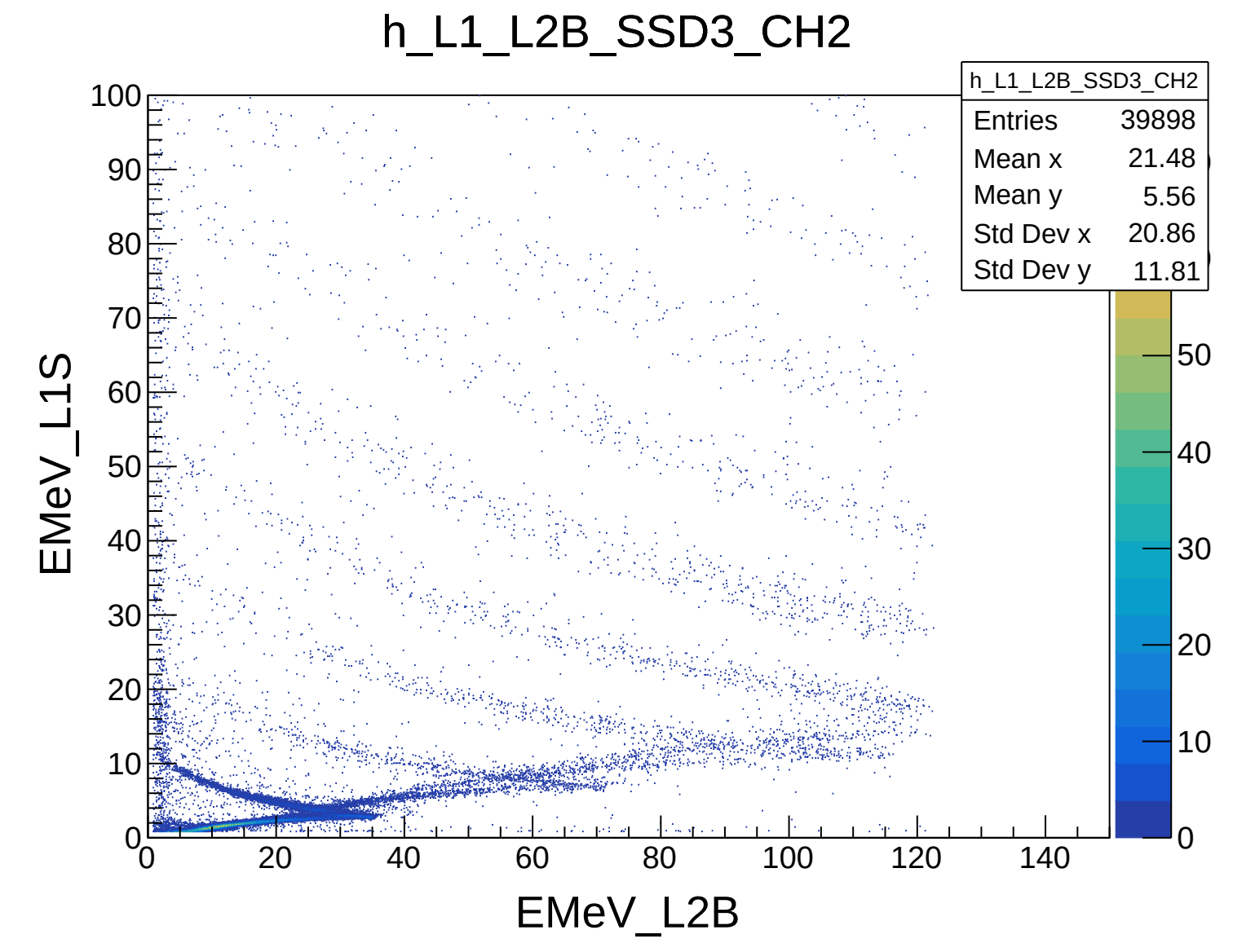

h_L1_L2B_SSD2_CH13
h_L1_L2B_SSD2_CH13
Entries 22268
Mean x 25.1
Mean y 17.15
Std Dev x 24.51
Std Dev y 24.41
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
5
10
15
20

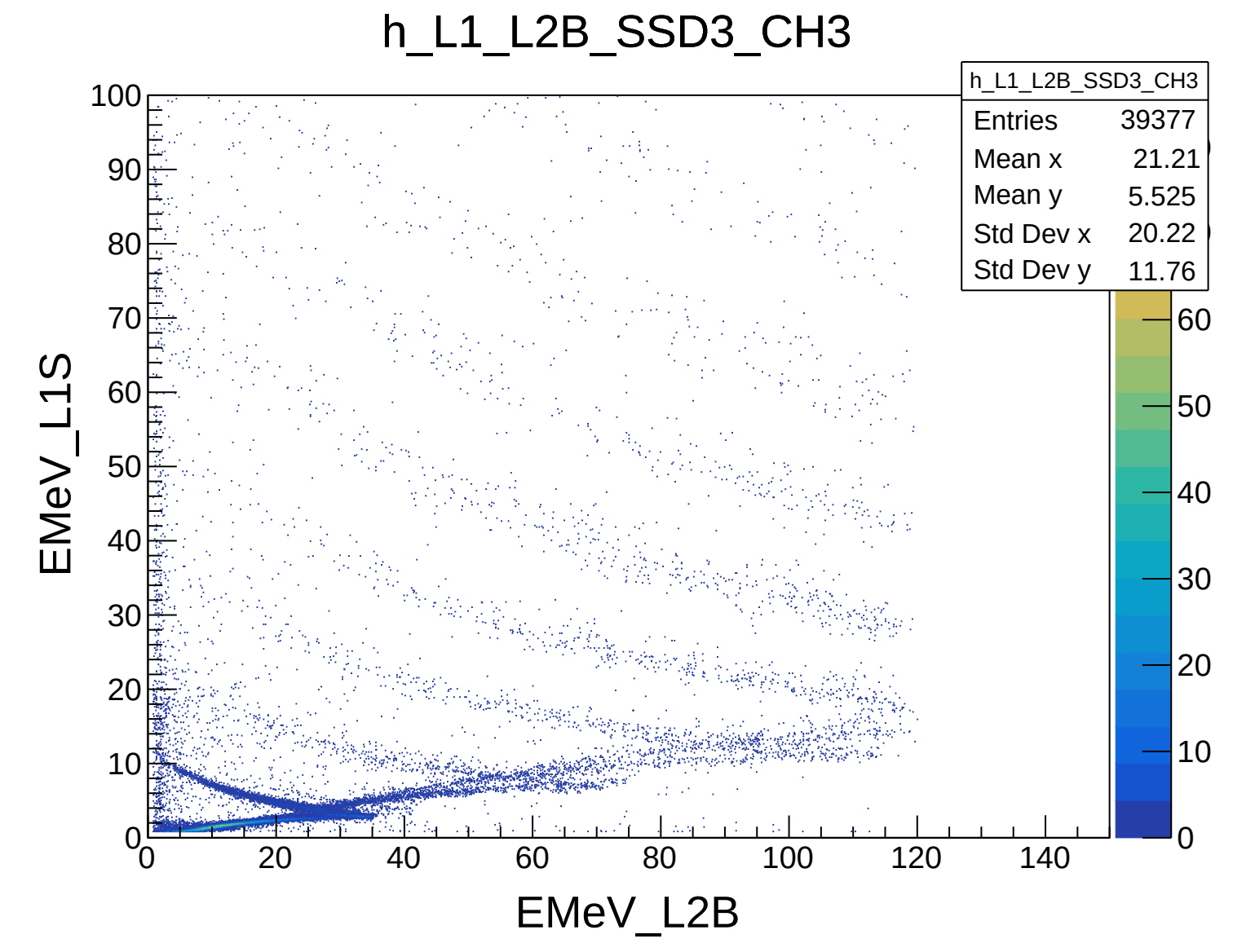

h_L1_L2B_SSD2_CH14
h_L1_L2B_SSD2_CH14
Entries 20950
Mean x 26.01
Mean y 17.36
Std Dev x 25.47
Std Dev y 23.79
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
2
4
6
8
10
12
14
16

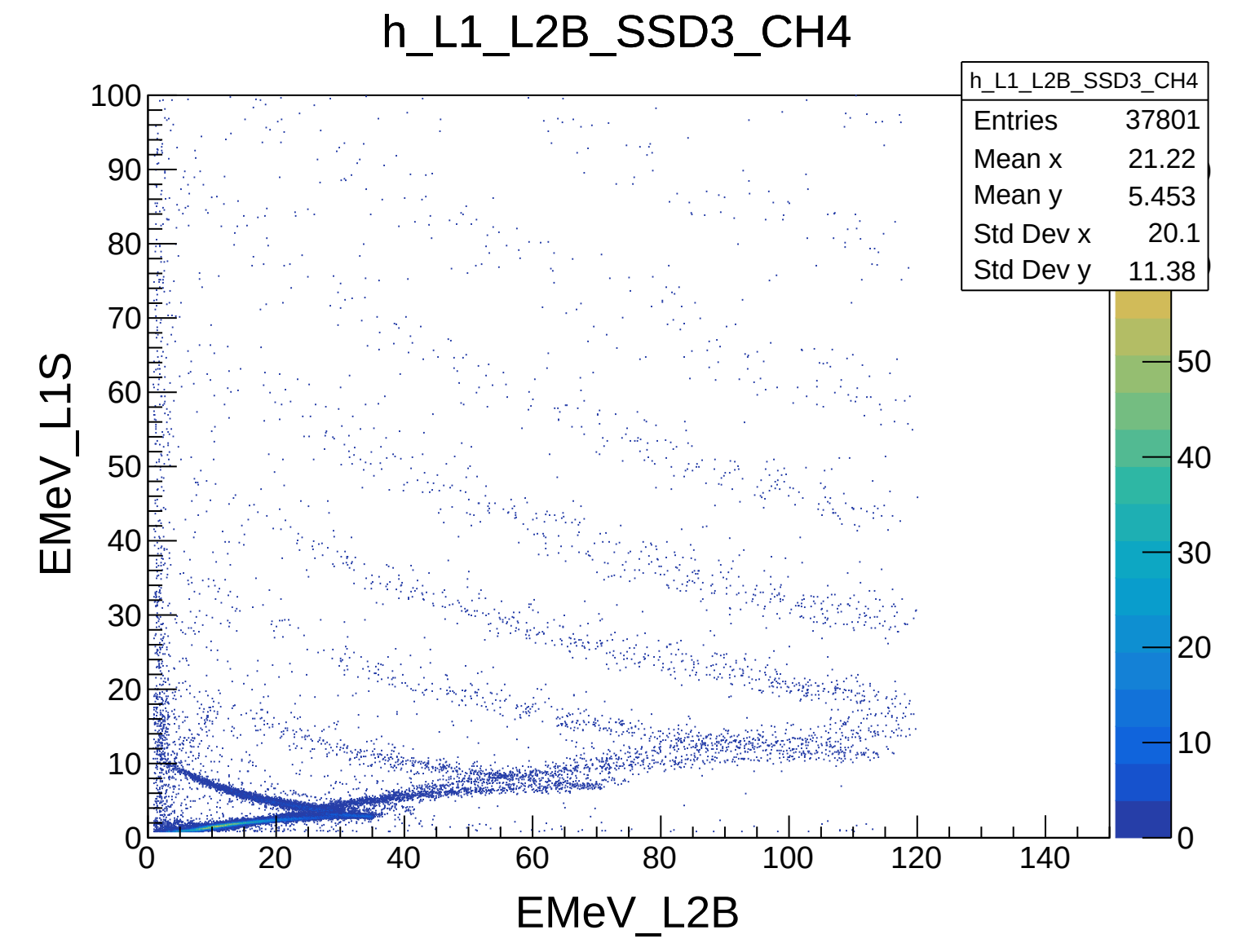

h_L1_L2B_SSD2_CH15
h_L1_L2B_SSD2_CH15
Entries 17982
Mean x 23.95
Mean y 17.36
Std Dev x 23.08
Std Dev y 23.8
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
160
180
200
0
50
100
150
200
250
0
5
10
15
20

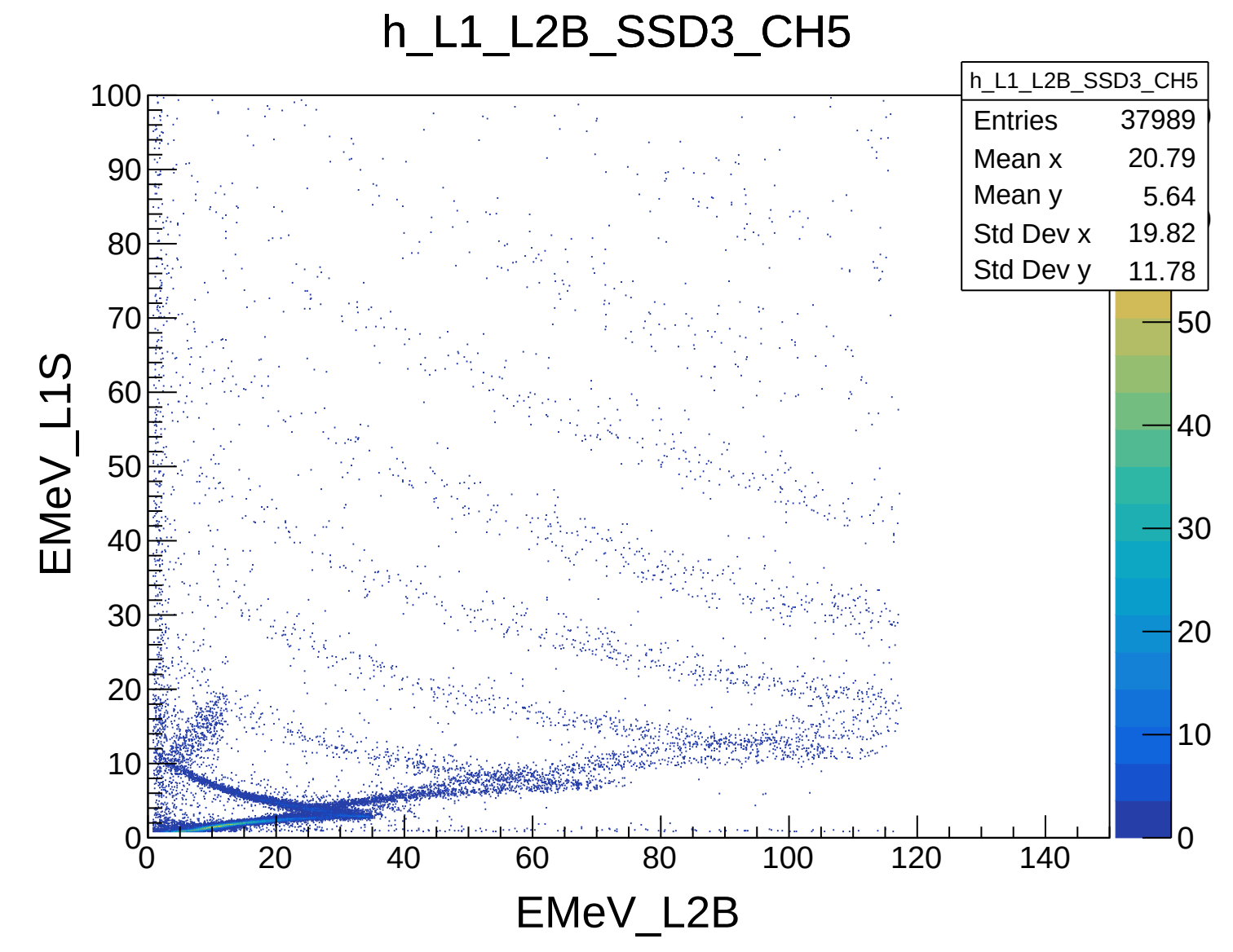

h_L1_L2B_SSD3_CH0
h_L1_L2B_SSD3_CH0
Entries 36273
Mean x 20.64
Mean y 5.209
Std Dev x 19.84
Std Dev y 11.18
EMeV_L1S
EMeV_L2B
0
20
40
60
80
100
120
140
10
30
50
70
90

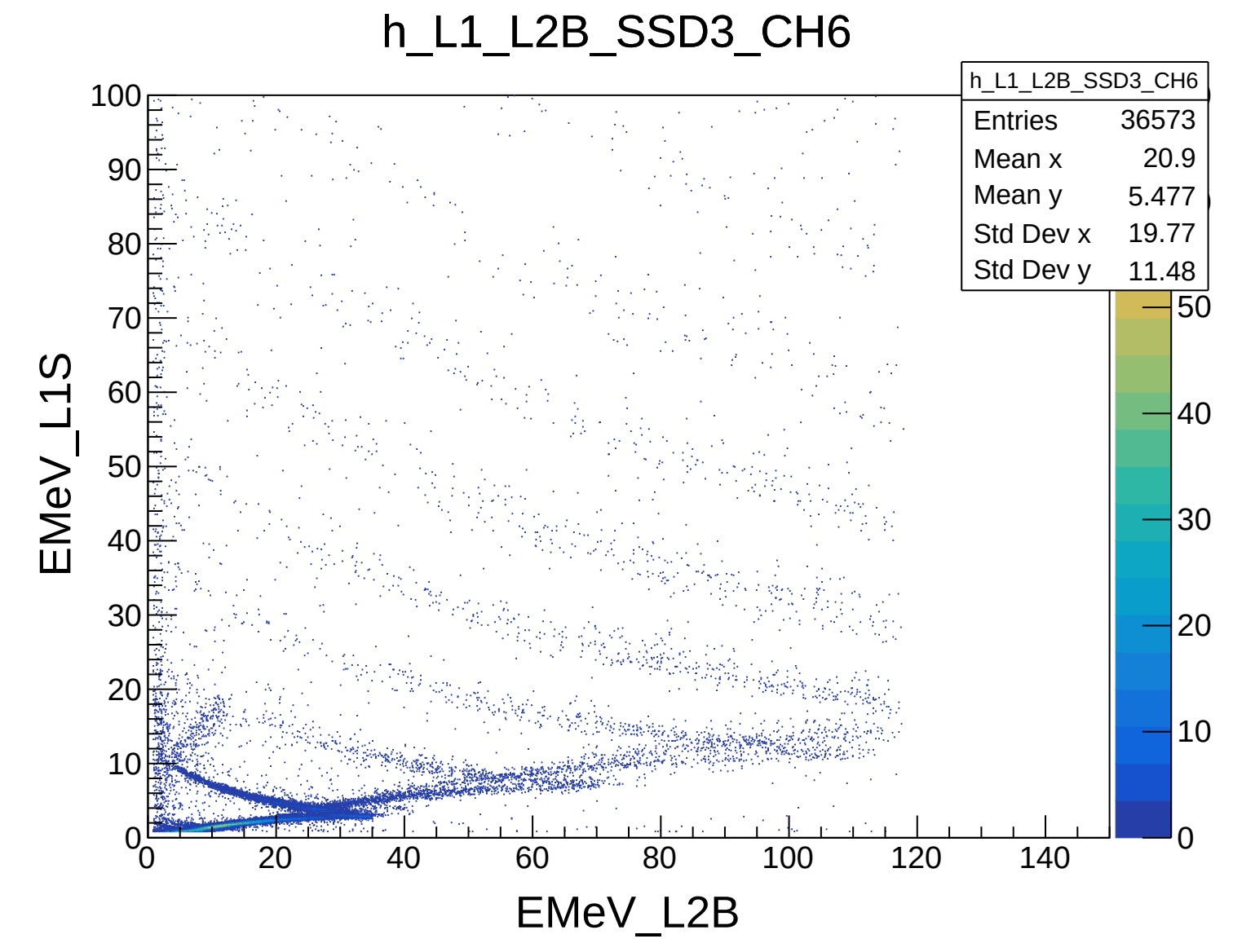

h_L1_L2B_SSD3_CH1
h_L1_L2B_SSD3_CH1
Entries 41148
Mean x 21.07
Mean y 5.615
Std Dev x 20.34
Std Dev y 12
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
20
40
60

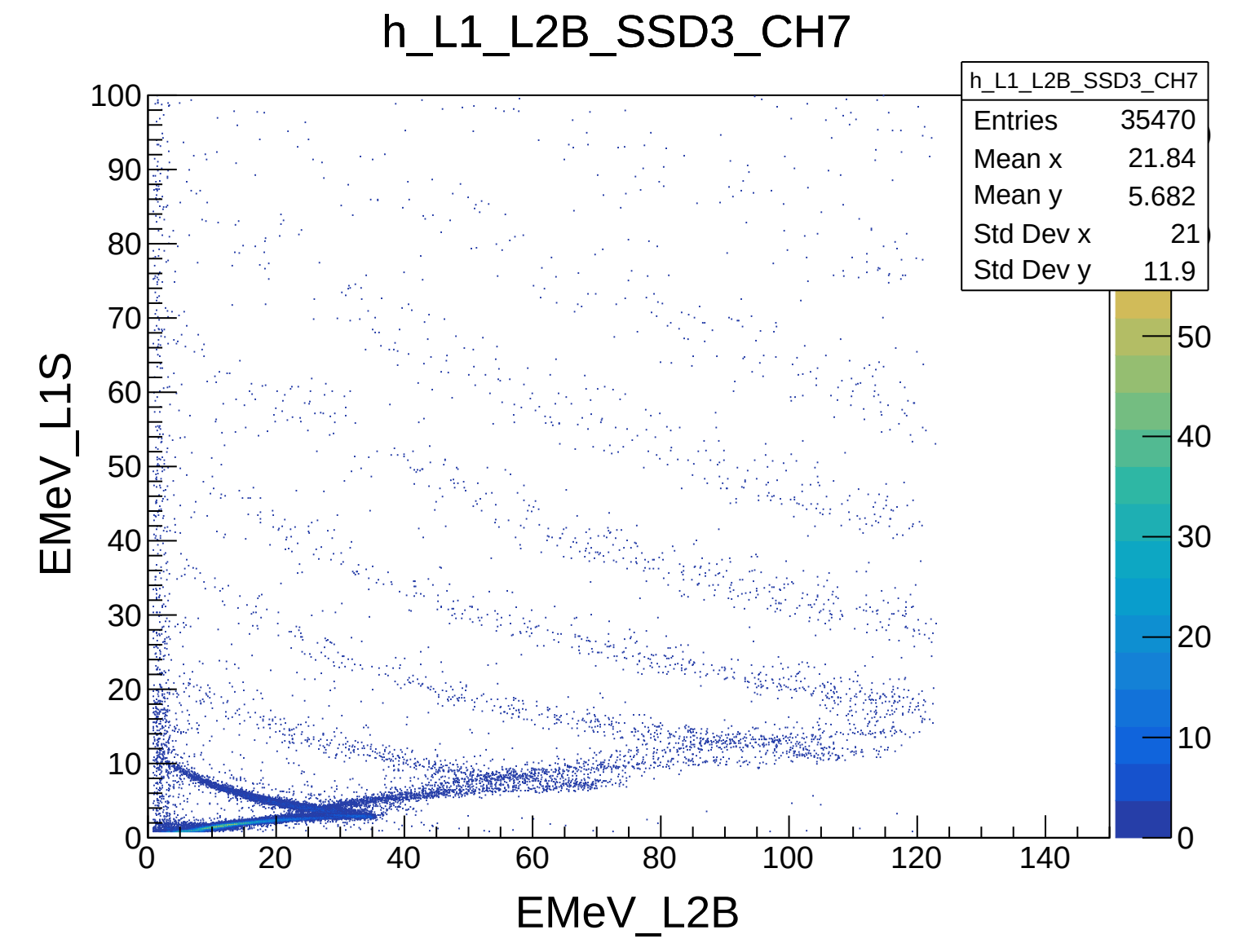

h_L1_L2B_SSD3_CH2
h_L1_L2B_SSD3_CH2
Entries 39898
Mean x 21.48
Mean y 5.56
Std Dev x 20.86
Std Dev y 11.81
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30
40
50

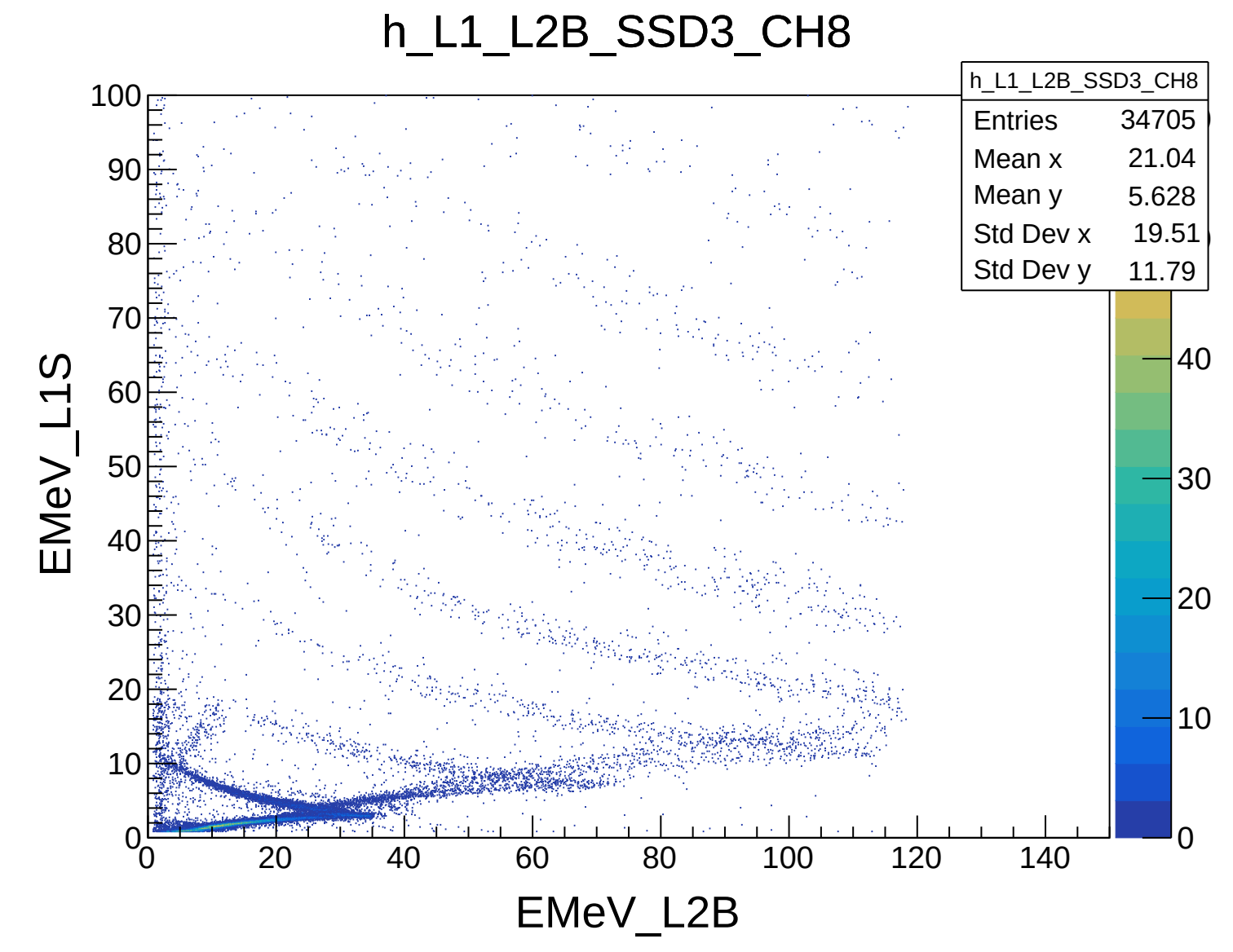

h_L1_L2B_SSD3_CH3
h_L1_L2B_SSD3_CH3
Entries 39377
Mean x 21.21
Mean y 5.525
Std Dev x 20.22
Std Dev y 11.76
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30
40
50
60

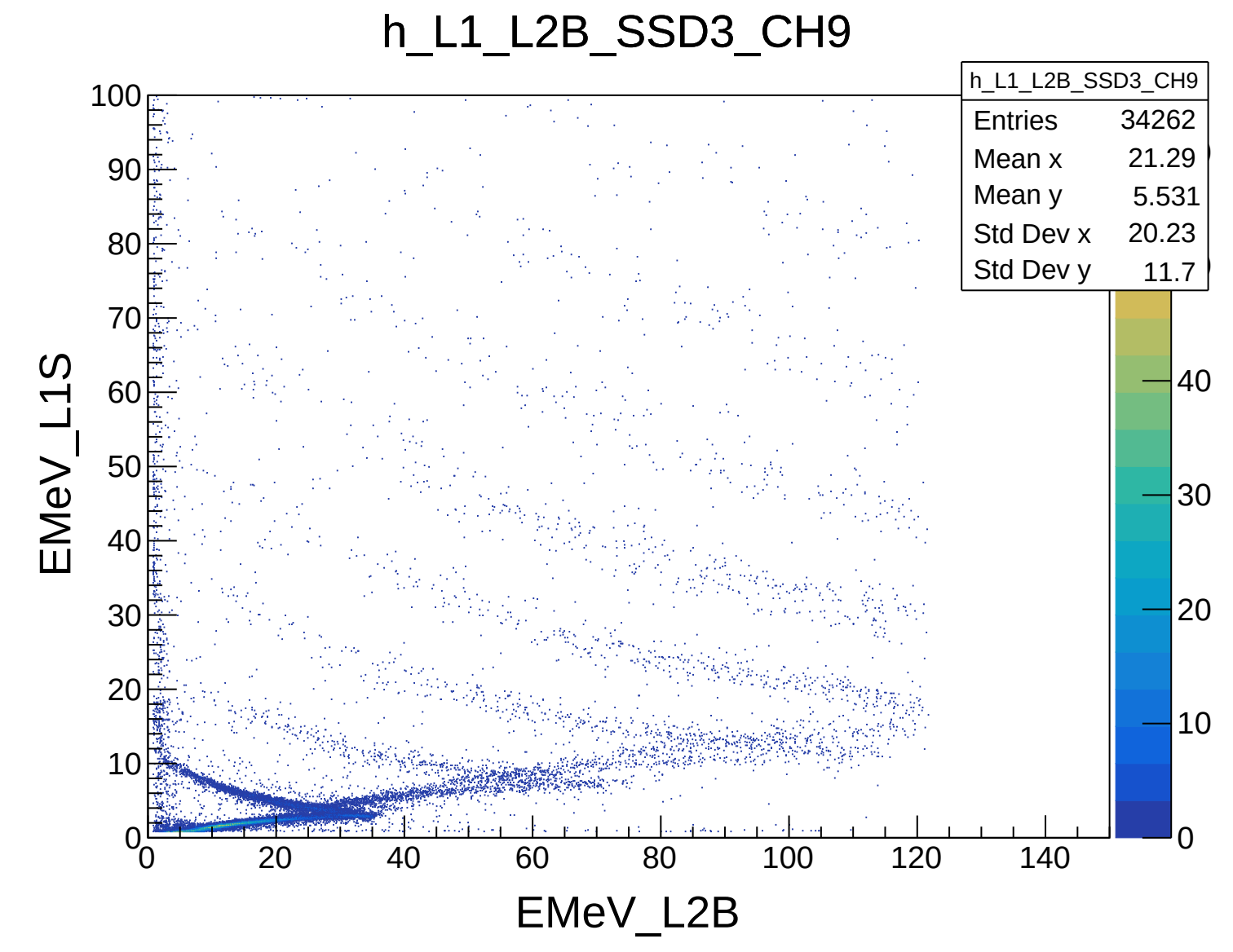

h_L1_L2B_SSD3_CH4
h_L1_L2B_SSD3_CH4
Entries 37801
Mean x 21.22
Mean y 5.453
Std Dev x 20.1
Std Dev y 11.38
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30
40
50

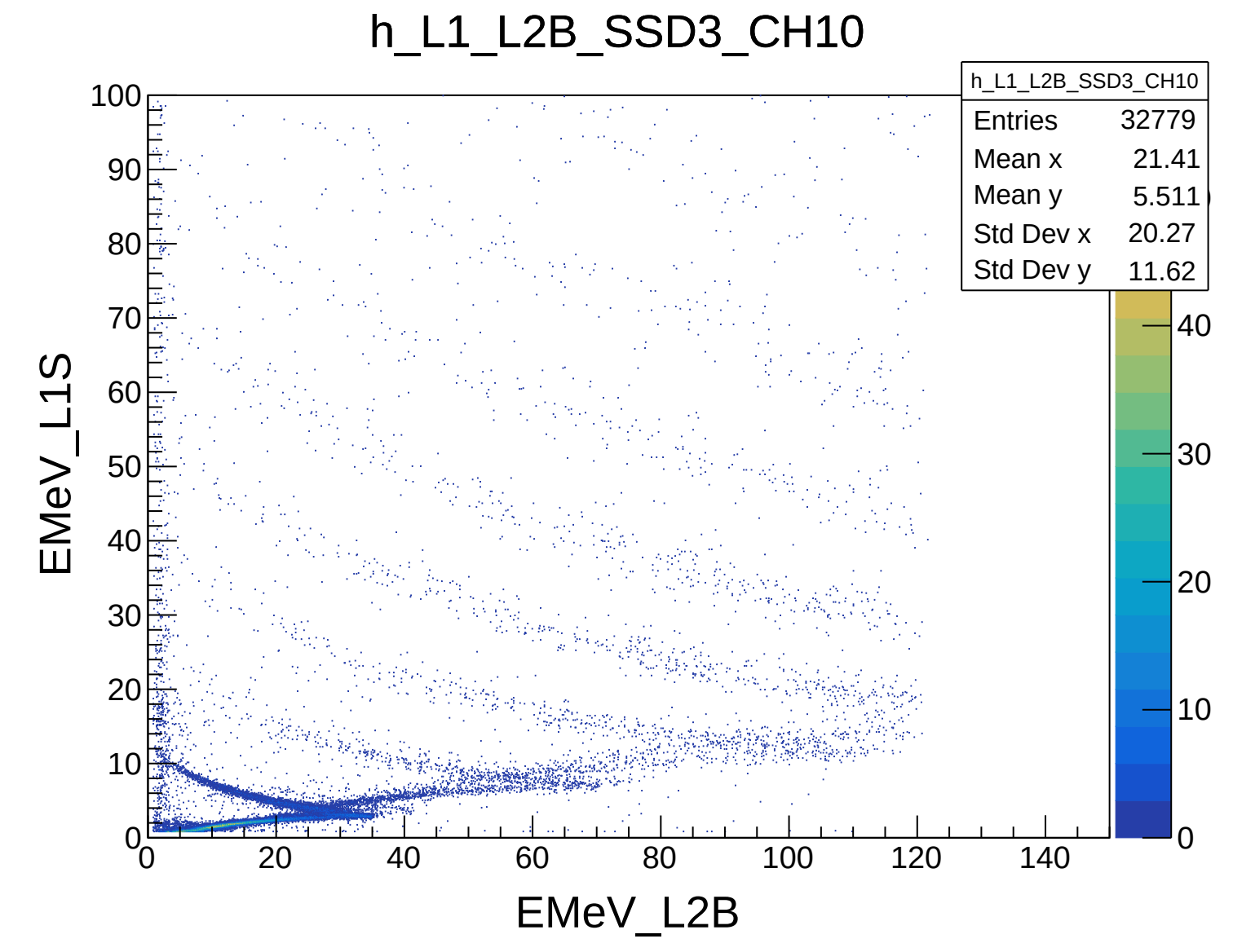

h_L1_L2B_SSD3_CH5
h_L1_L2B_SSD3_CH5
Entries 37989
Mean x 20.79
Mean y 5.64
Std Dev x 19.82
Std Dev y 11.78
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30
40
50

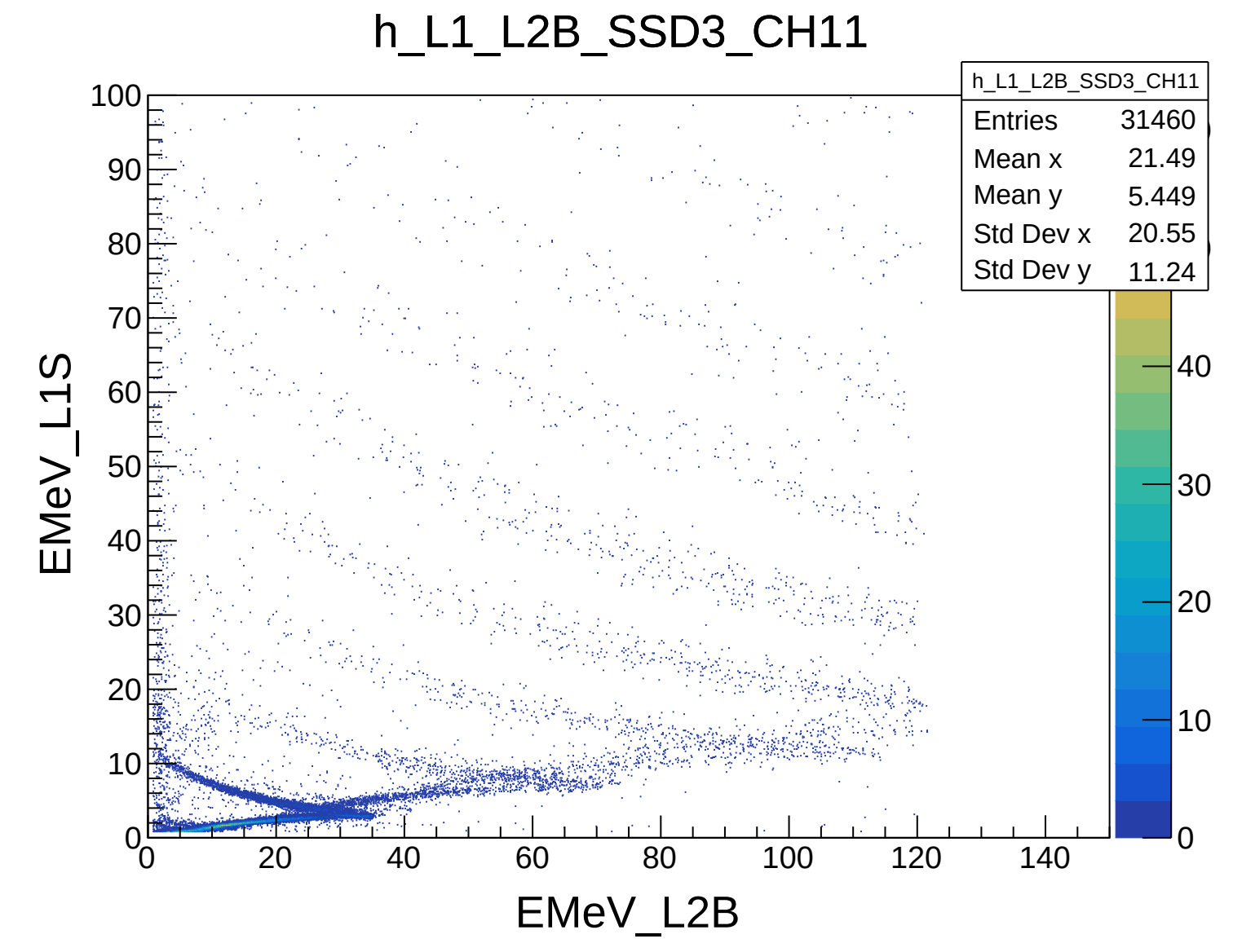

h_L1_L2B_SSD3_CH6
h_L1_L2B_SSD3_CH6
Entries 36573
Mean x 20.9
Mean y 5.477
Std Dev x 19.77
Std Dev y 11.48
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30
40
50

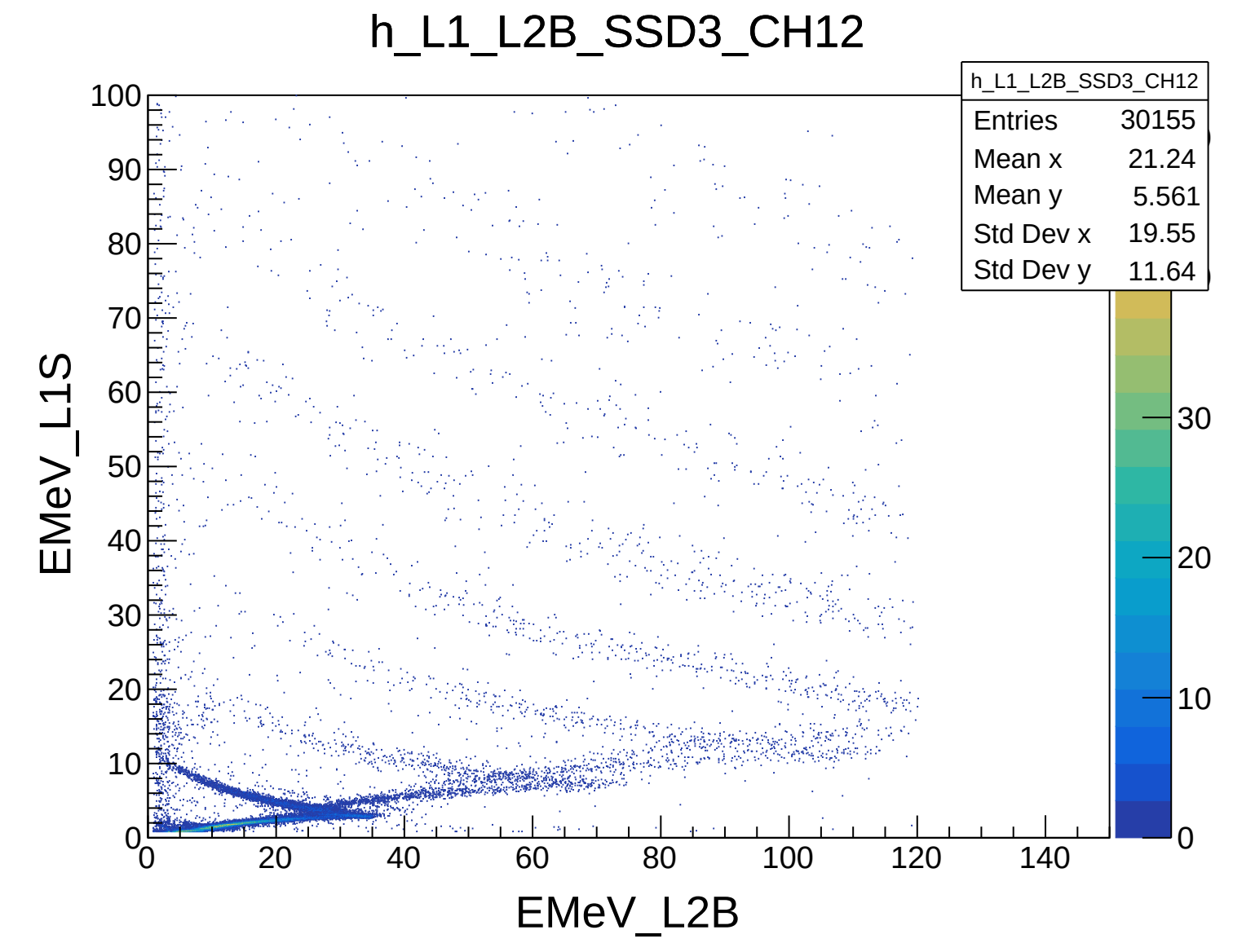

h_L1_L2B_SSD3_CH7
h_L1_L2B_SSD3_CH7
Entries 35470
Mean x 21.84
Mean y 5.682
Std Dev x 21
Std Dev y 11.9
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30
40
50

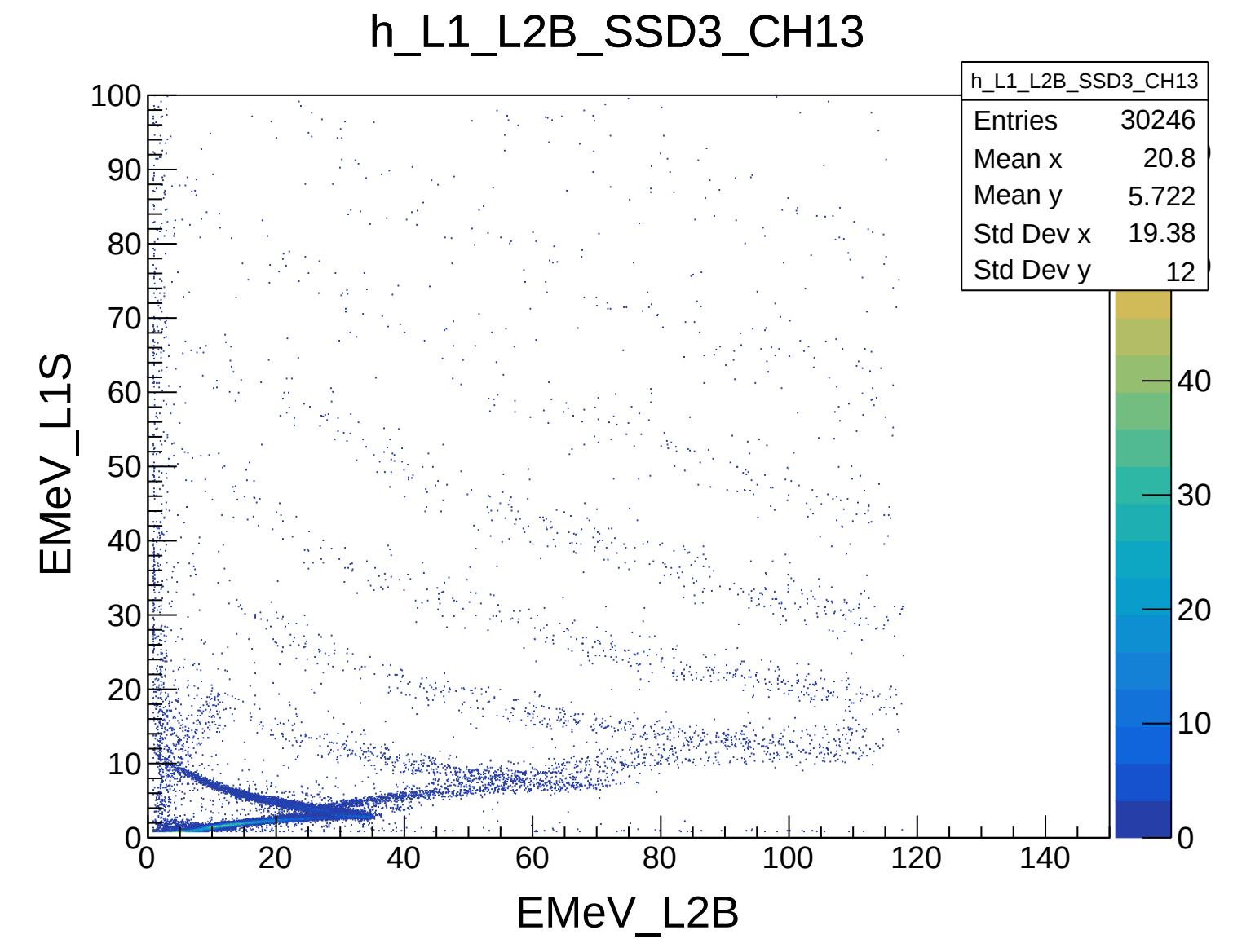

h_L1_L2B_SSD3_CH8
h_L1_L2B_SSD3_CH8
Entries 34705
Mean x 21.04
Mean y 5.628
Std Dev x 19.51
Std Dev y 11.79
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30
40

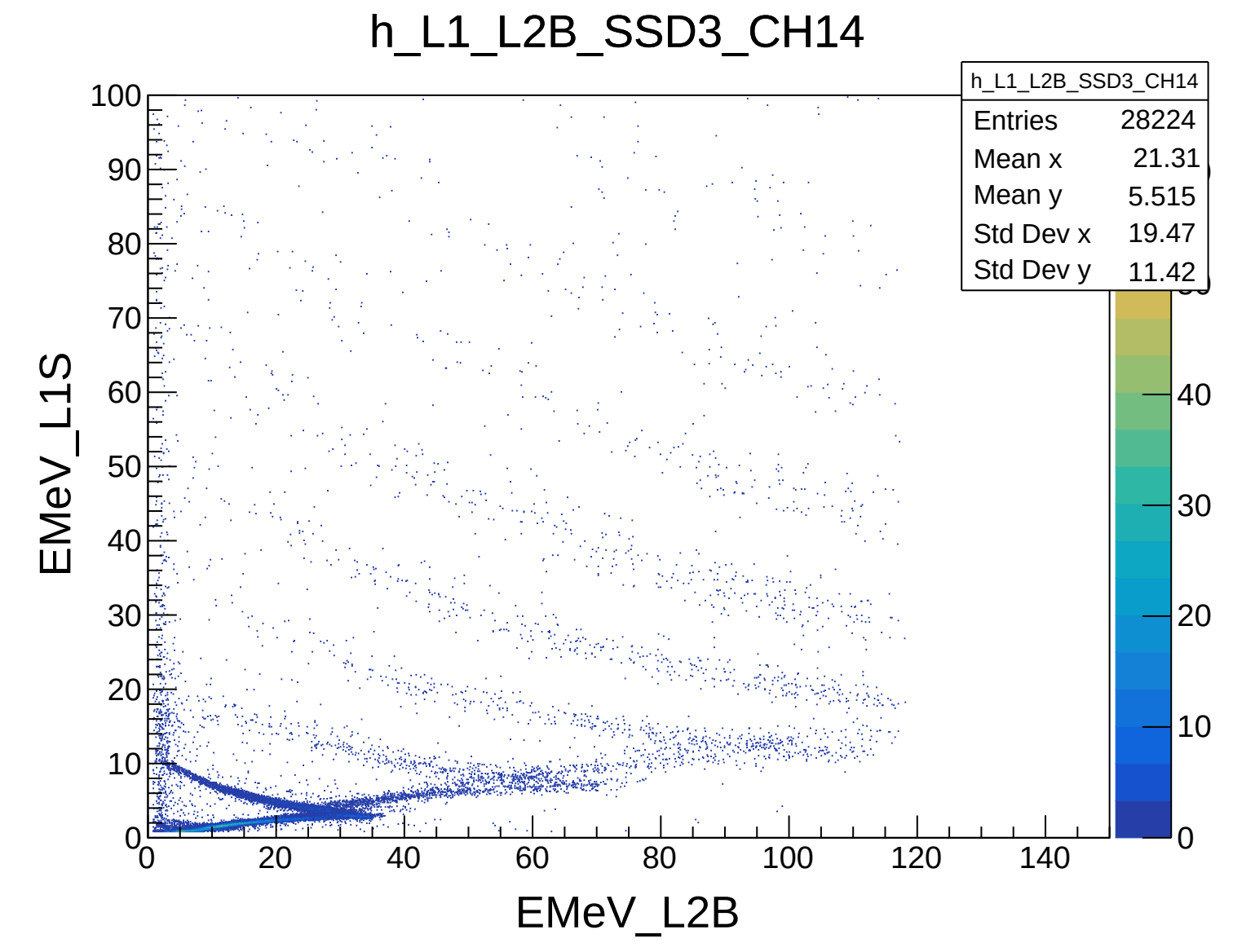

h_L1_L2B_SSD3_CH9
h_L1_L2B_SSD3_CH9
Entries 34262
Mean x 21.29
Mean y 5.531
Std Dev x 20.23
Std Dev y 11.7
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30
40

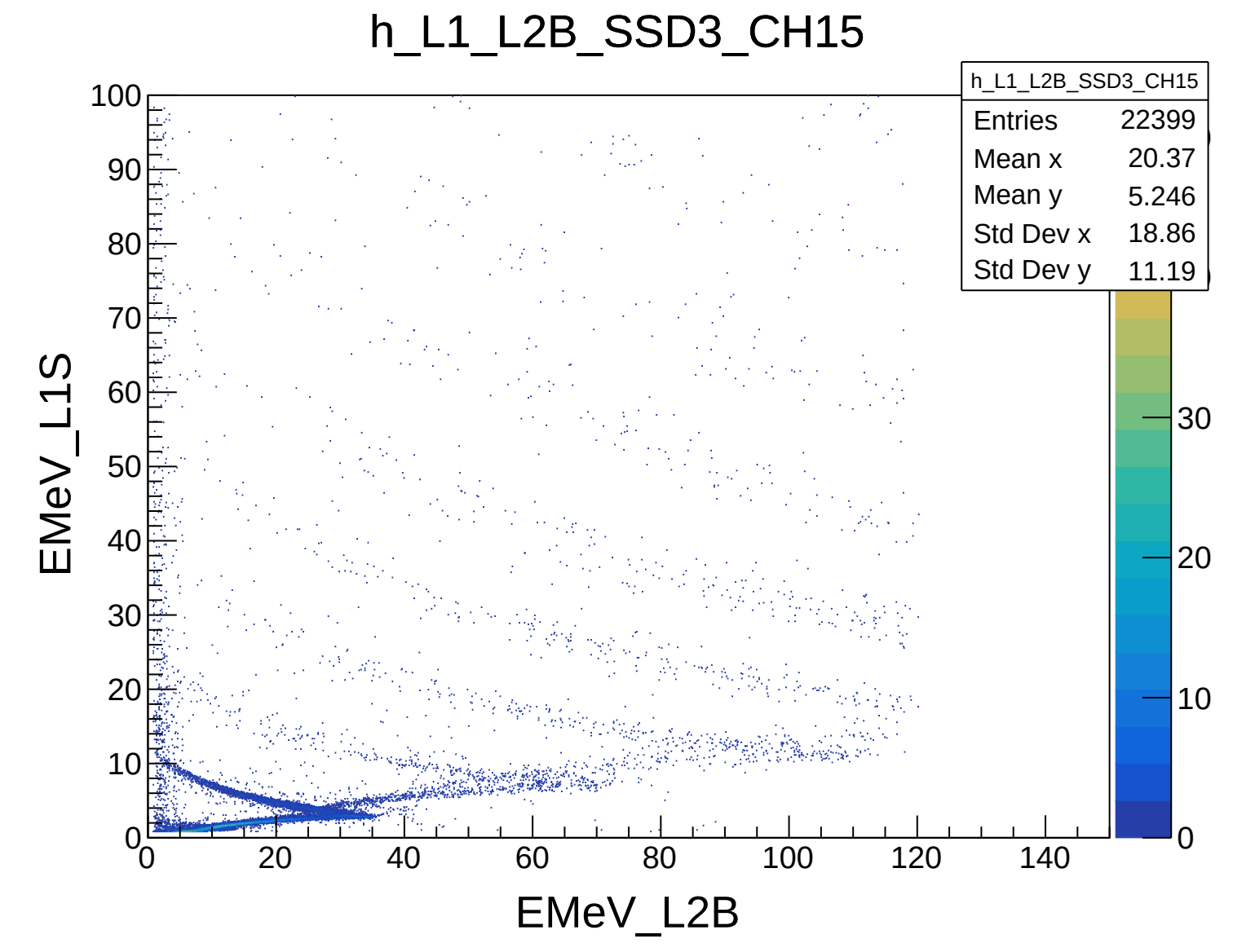

h_L1_L2B_SSD3_CH10
h_L1_L2B_SSD3_CH10
Entries 32779
Mean x 21.41
Mean y 5.511
Std Dev x 20.27
Std Dev y 11.62
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30
40

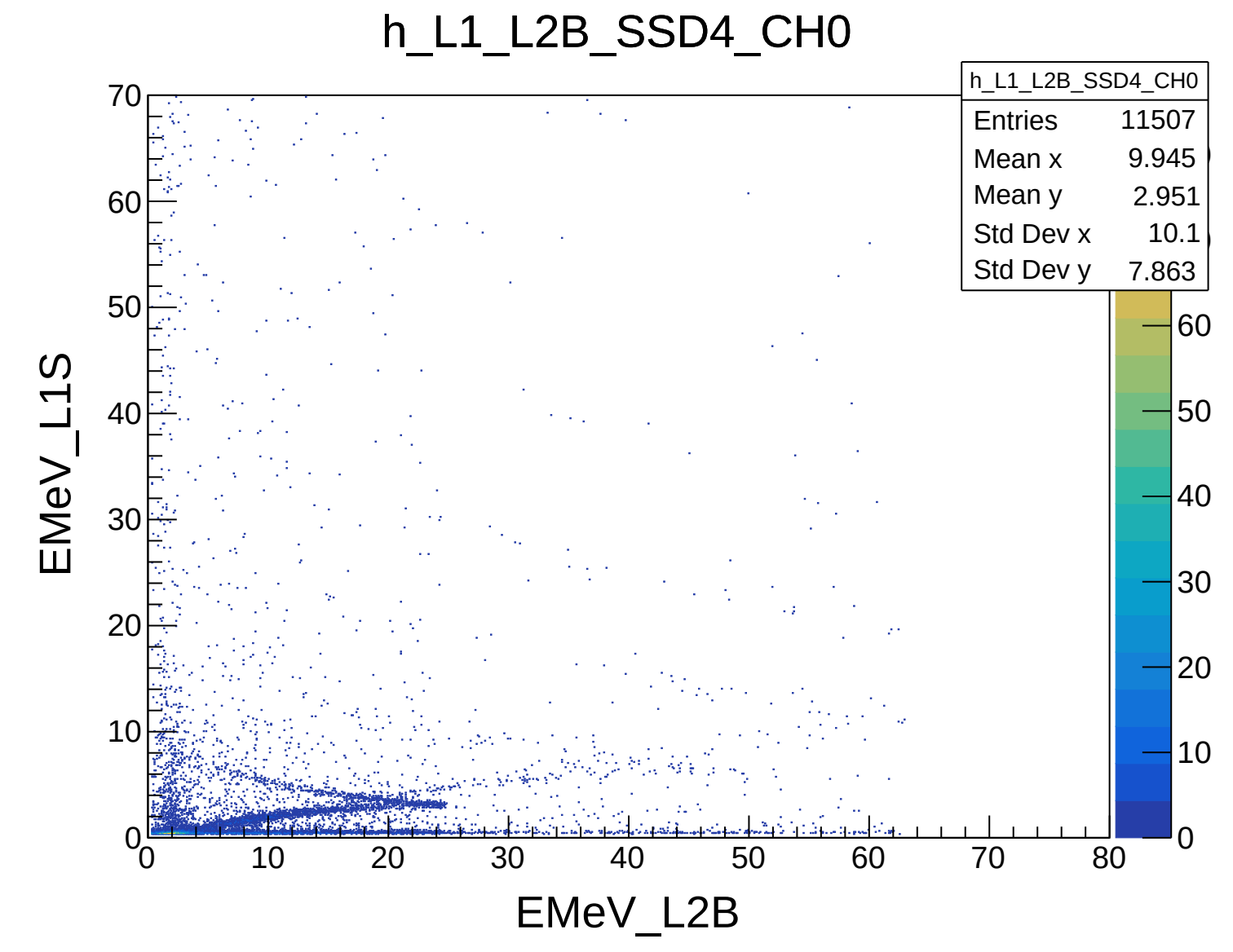

h_L1_L2B_SSD3_CH11
h_L1_L2B_SSD3_CH11
Entries 31460
Mean x 21.49
Mean y 5.449
Std Dev x 20.55
Std Dev y 11.24
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30
40

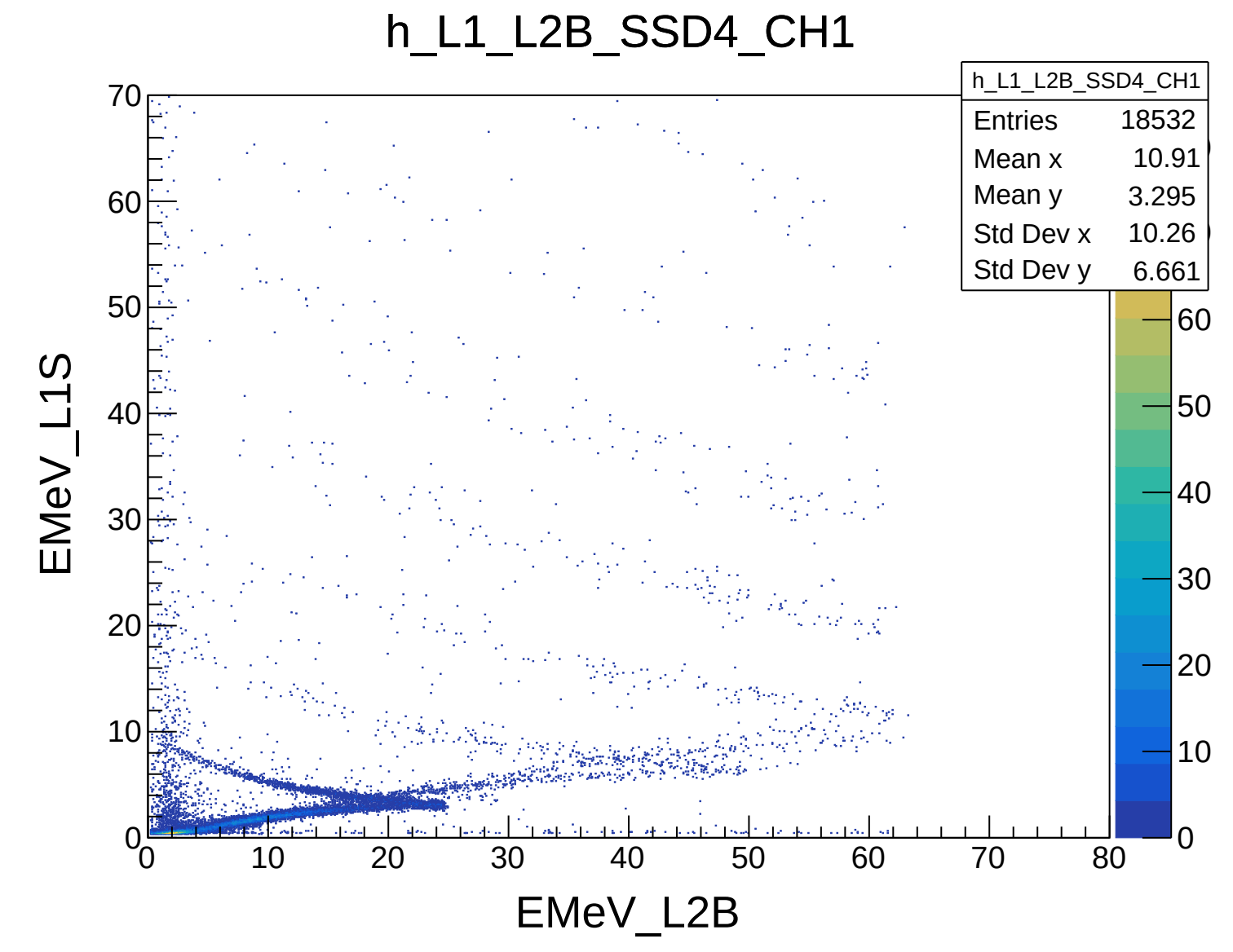

h_L1_L2B_SSD3_CH12
h_L1_L2B_SSD3_CH12
Entries 30155
Mean x 21.24
Mean y 5.561
Std Dev x 19.55
Std Dev y 11.64
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30

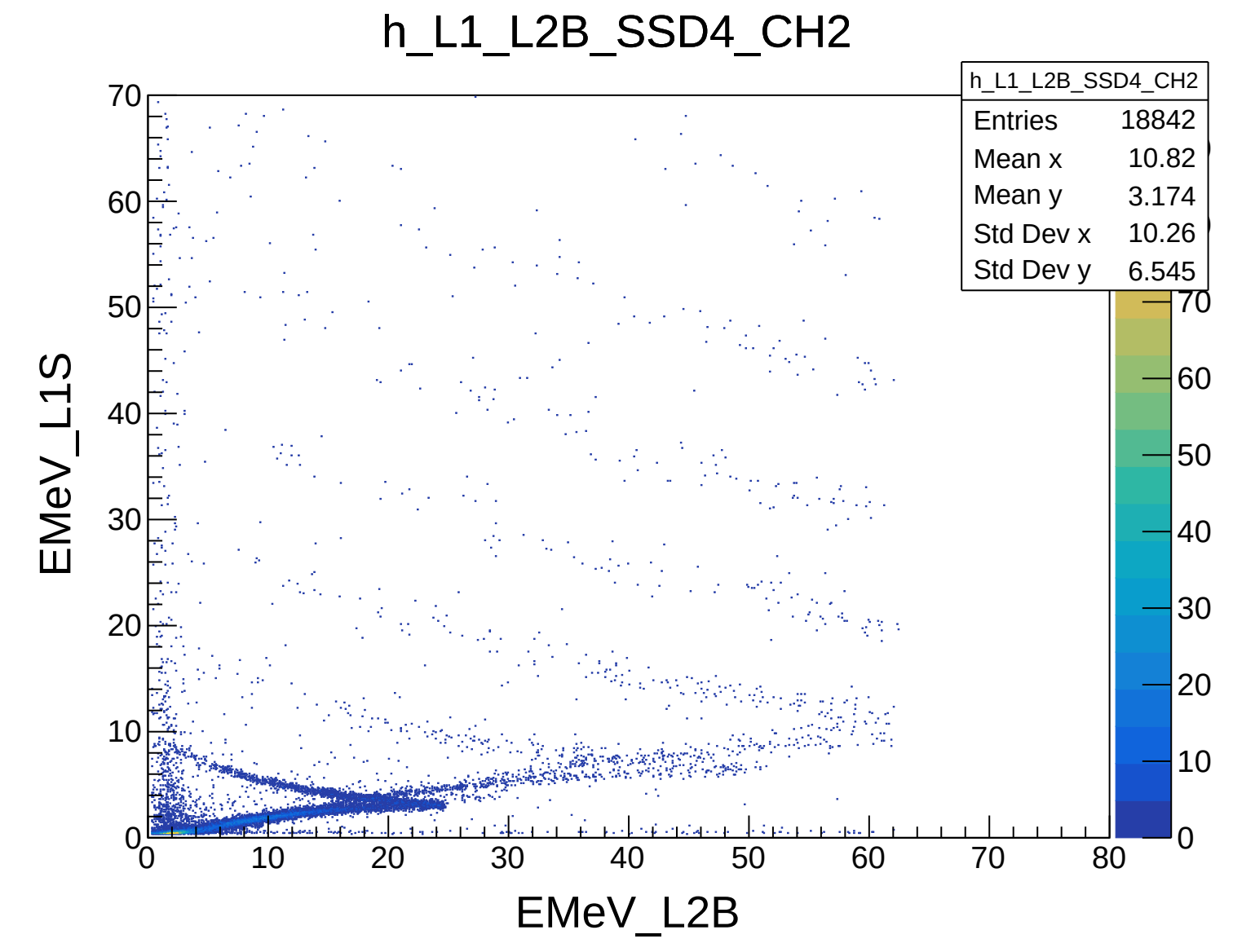

h_L1_L2B_SSD3_CH13
h_L1_L2B_SSD3_CH13
Entries 30246
Mean x 20.8
Mean y 5.722
Std Dev x 19.38
Std Dev y 12
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30
40

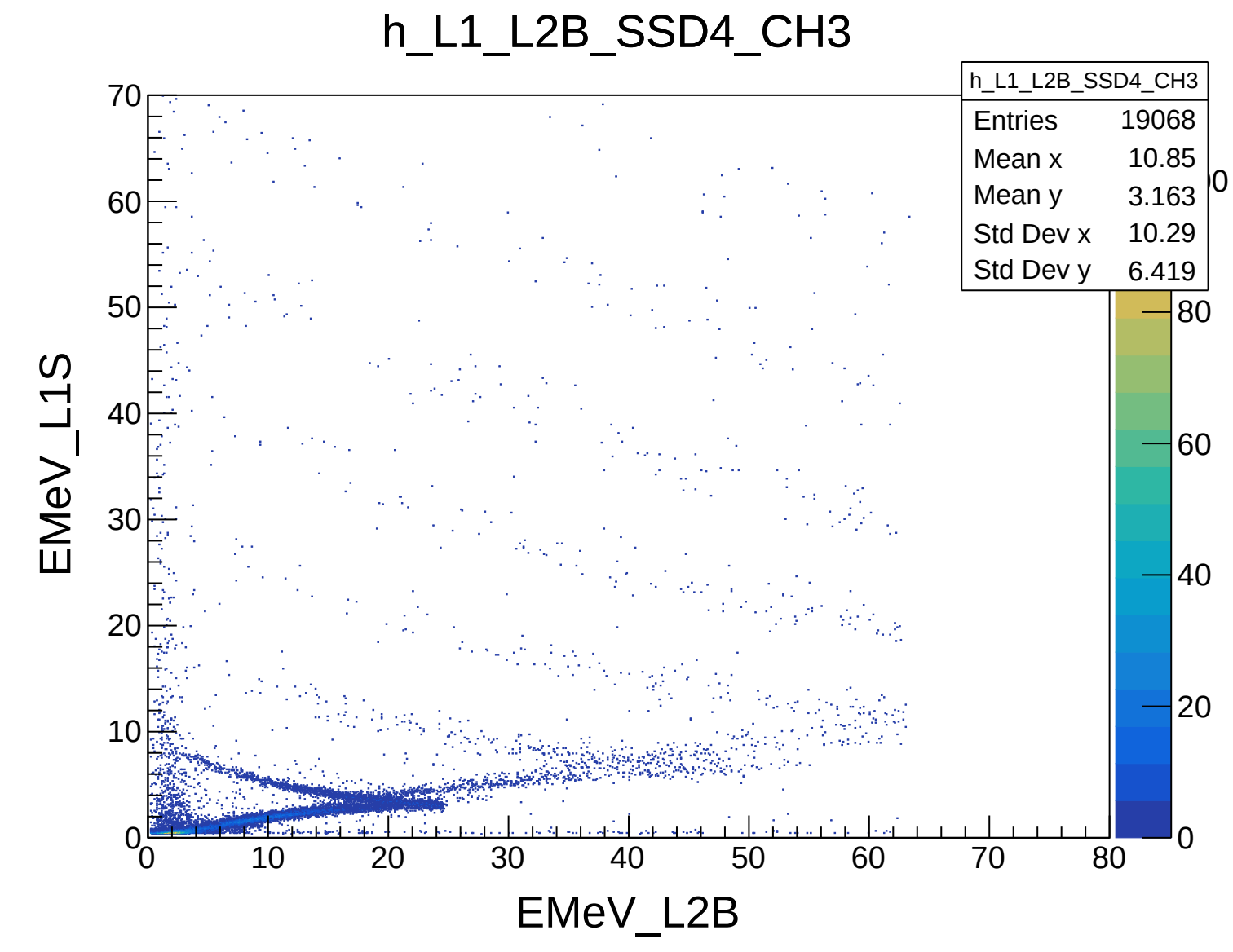

h_L1_L2B_SSD3_CH14
h_L1_L2B_SSD3_CH14
Entries 28224
Mean x 21.31
Mean y 5.515
Std Dev x 19.47
Std Dev y 11.42
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30
40

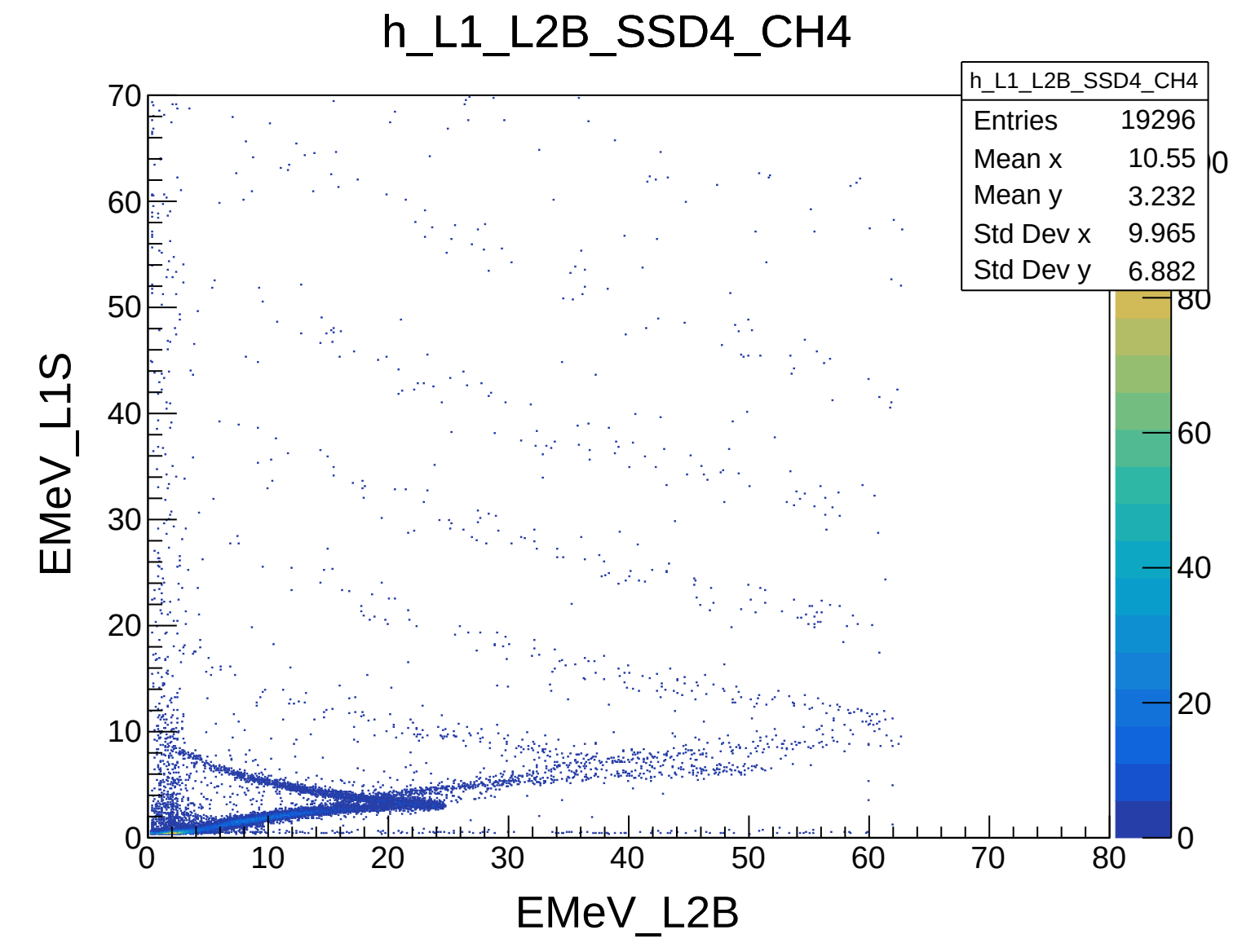

h_L1_L2B_SSD3_CH15
h_L1_L2B_SSD3_CH15
Entries 22399
Mean x 20.37
Mean y 5.246
Std Dev x 18.86
Std Dev y 11.19
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
90
100
0
20
40
60
80
100
120
140
0
10
20
30

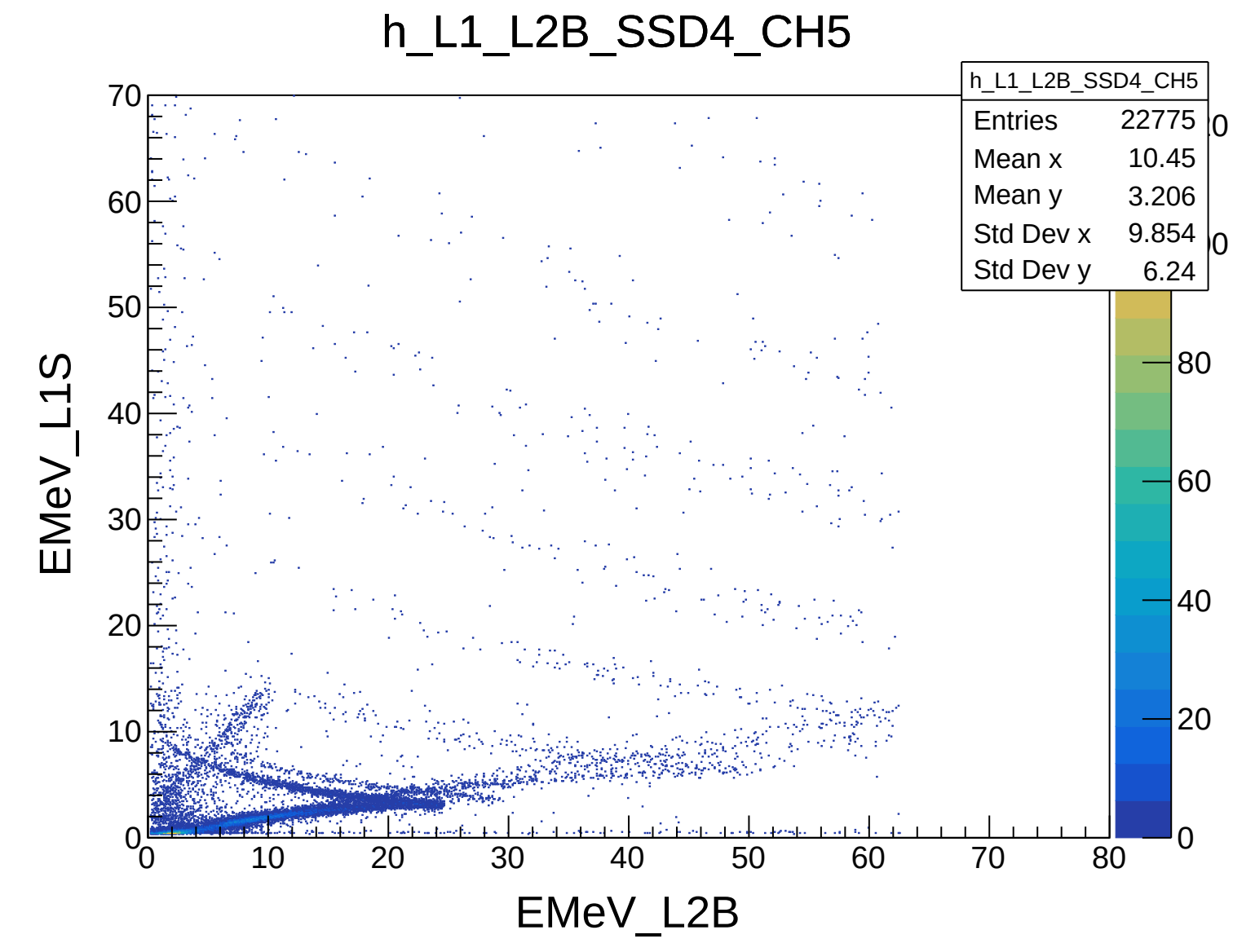

h_L1_L2B_SSD4_CH0
h_L1_L2B_SSD4_CH0
Entries 11507
Mean x 9.945
Mean y 2.951
Std Dev x 10.1
Std Dev y 7.863
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

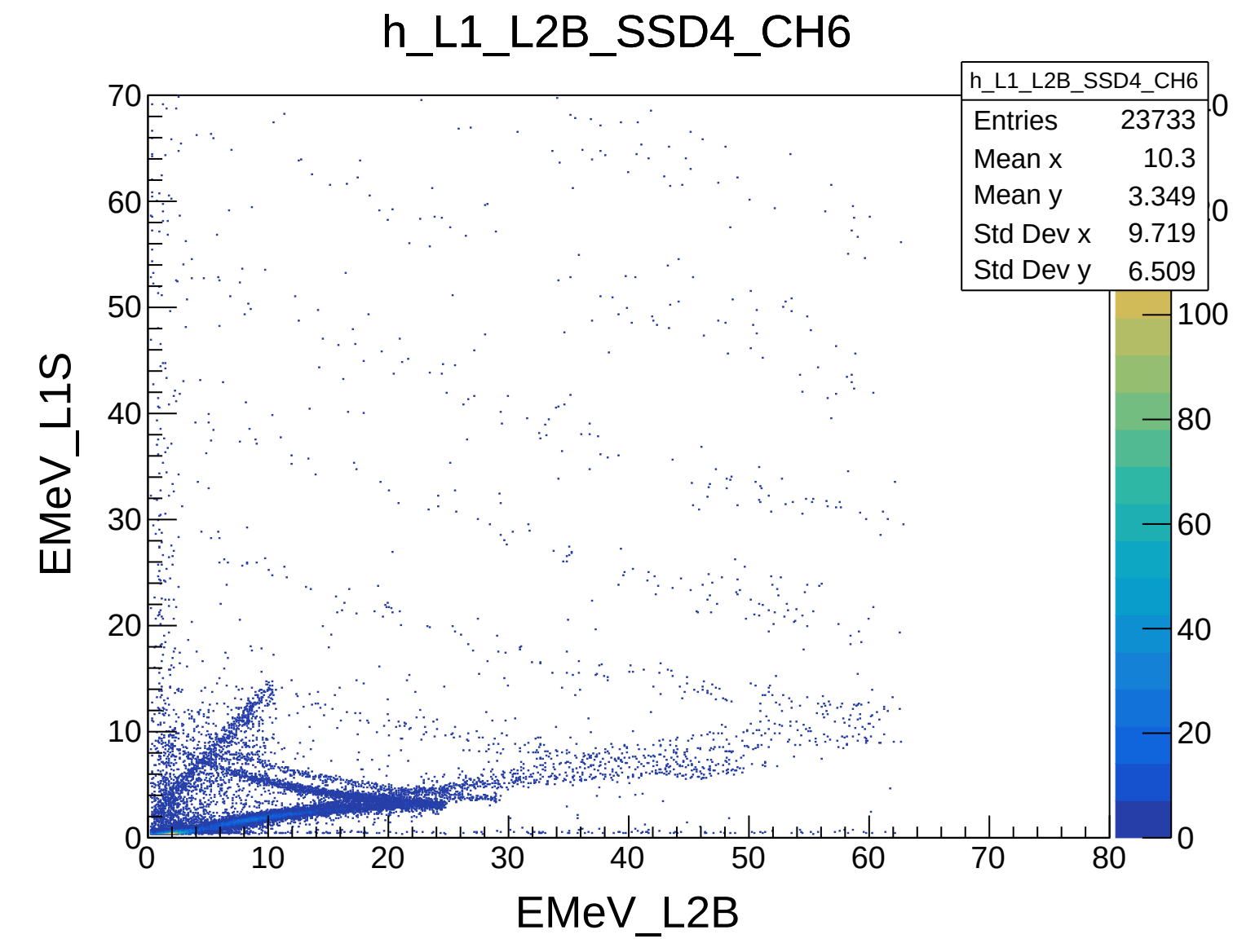

h_L1_L2B_SSD4_CH1
h_L1_L2B_SSD4_CH1
Entries 18532
Mean x 10.91
Mean y 3.295
Std Dev x 10.26
Std Dev y 6.661
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

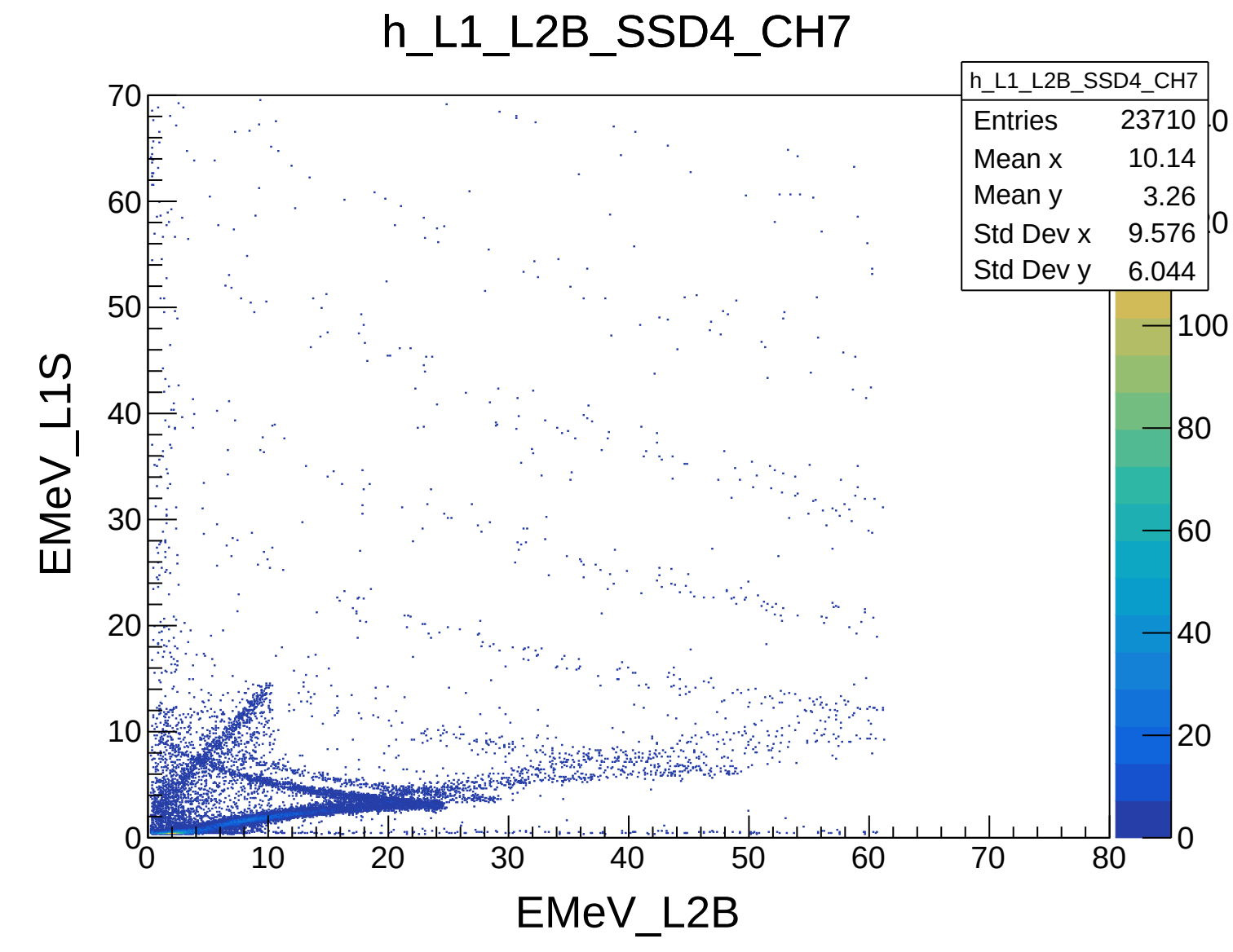

h_L1_L2B_SSD4_CH2
h_L1_L2B_SSD4_CH2
Entries 18842
Mean x 10.82
Mean y 3.174
Std Dev x 10.26
Std Dev y 6.545
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

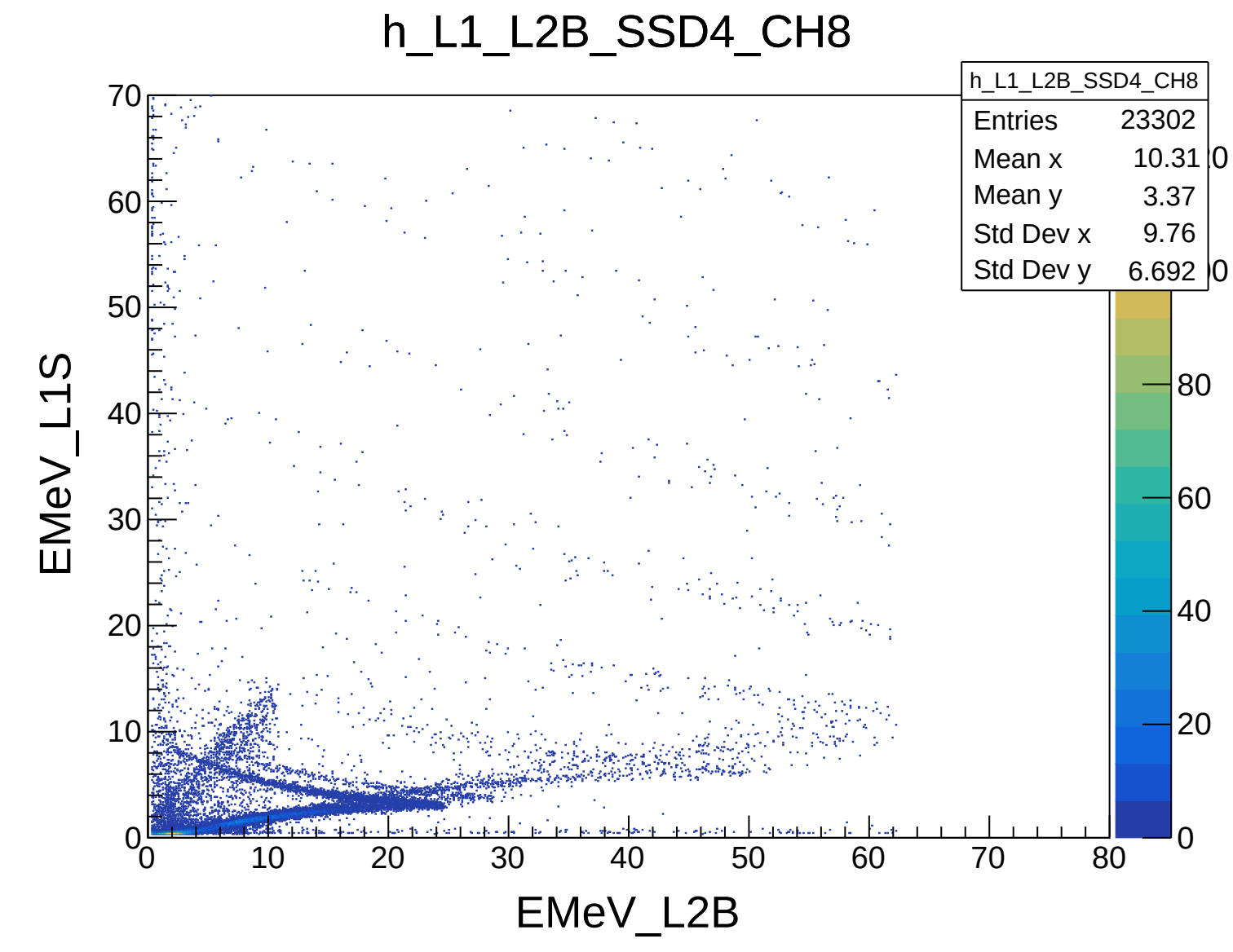

h_L1_L2B_SSD4_CH3
h_L1_L2B_SSD4_CH3
Entries 19068
Mean x 10.85
Mean y 3.163
Std Dev x 10.29
Std Dev y 6.419
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

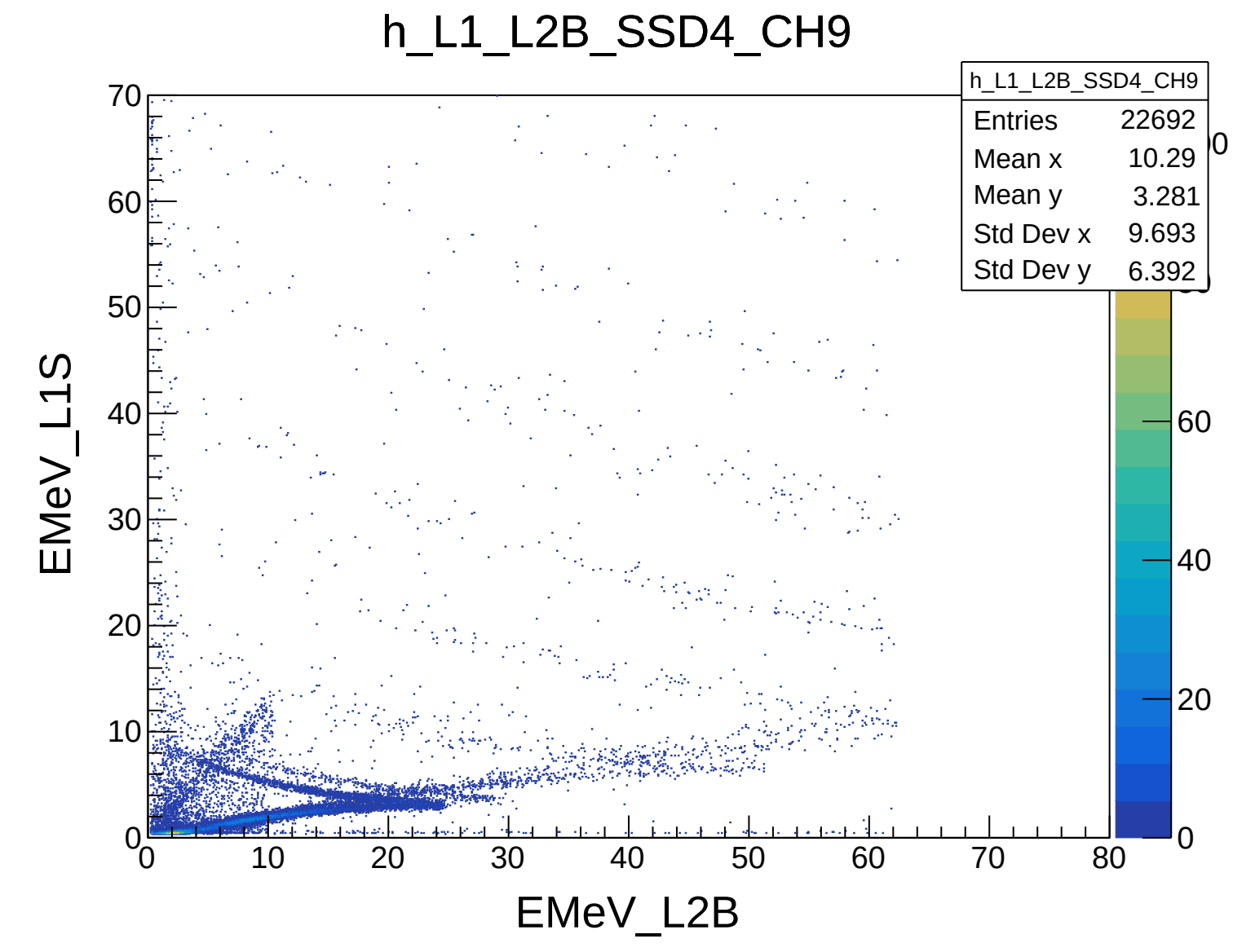

h_L1_L2B_SSD4_CH4
h_L1_L2B_SSD4_CH4
Entries 19296
Mean x 10.55
Mean y 3.232
Std Dev x 9.965
Std Dev y 6.882
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

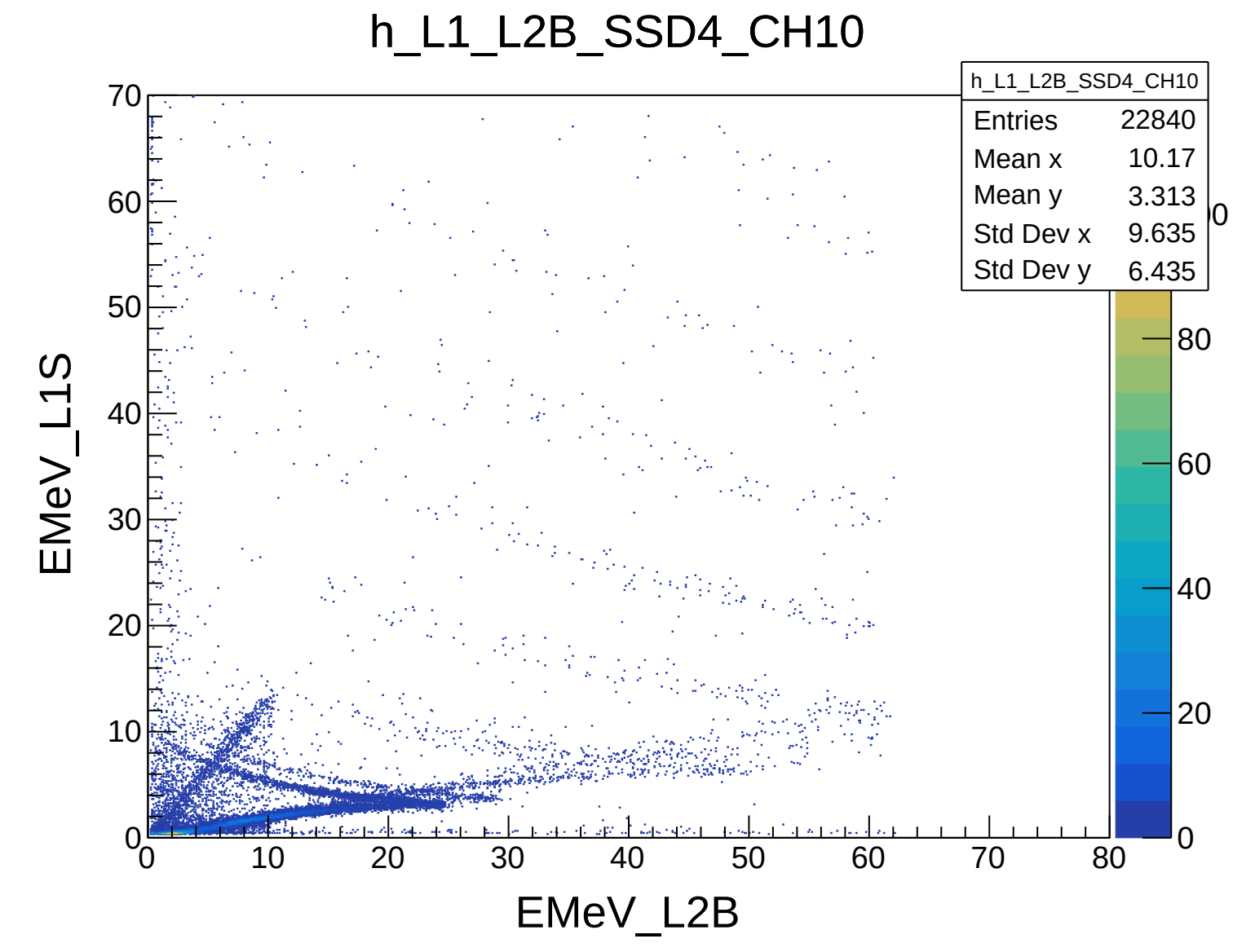

h_L1_L2B_SSD4_CH5
h_L1_L2B_SSD4_CH5
Entries 22775
Mean x 10.45
Mean y 3.206
Std Dev x 9.854
Std Dev y 6.24
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

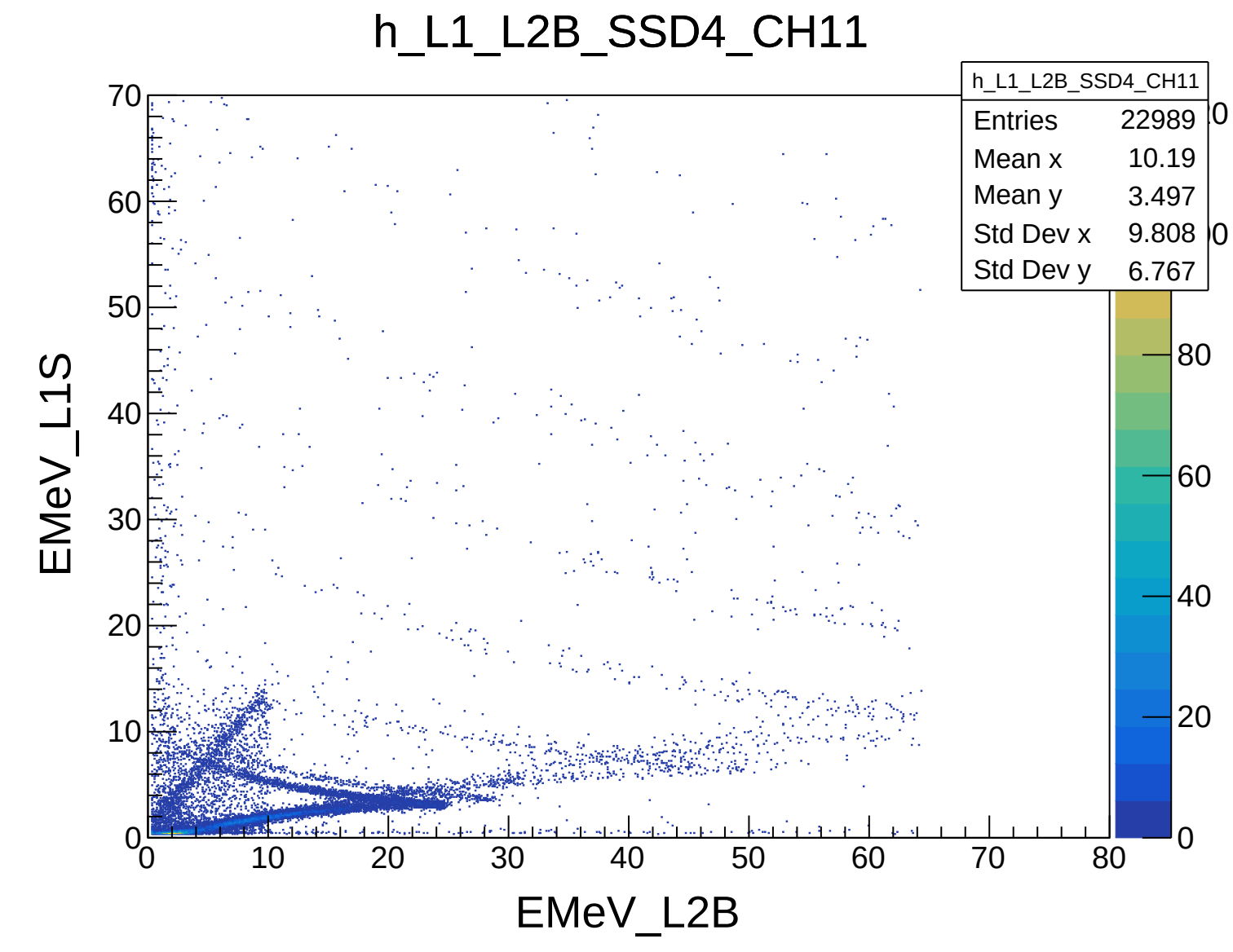

h_L1_L2B_SSD4_CH6
h_L1_L2B_SSD4_CH6
Entries 23733
Mean x 10.3
Mean y 3.349
Std Dev x 9.719
Std Dev y 6.509
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
100

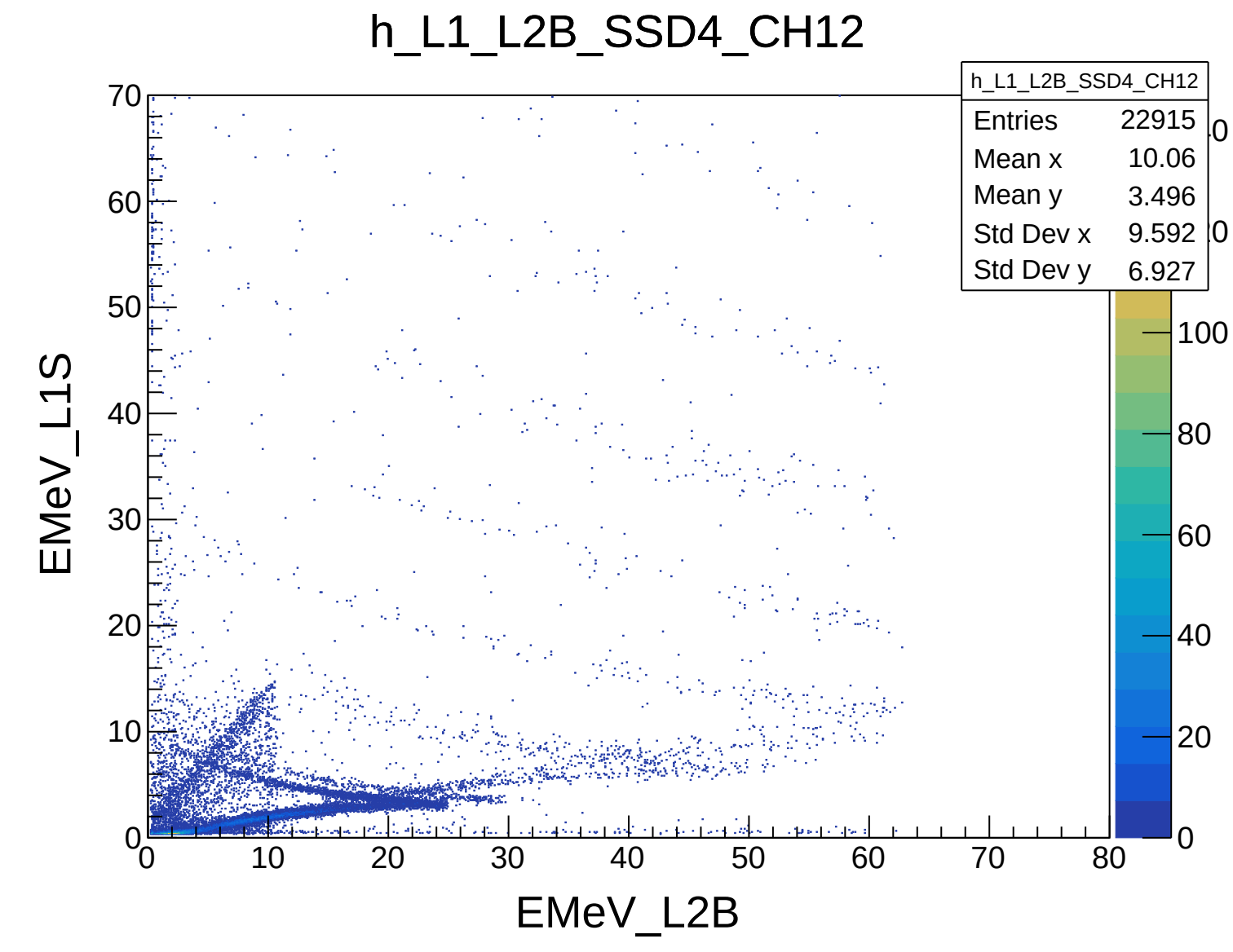

h_L1_L2B_SSD4_CH7
h_L1_L2B_SSD4_CH7
Entries 23710
Mean x 10.14
Mean y 3.26
Std Dev x 9.576
Std Dev y 6.044
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
100

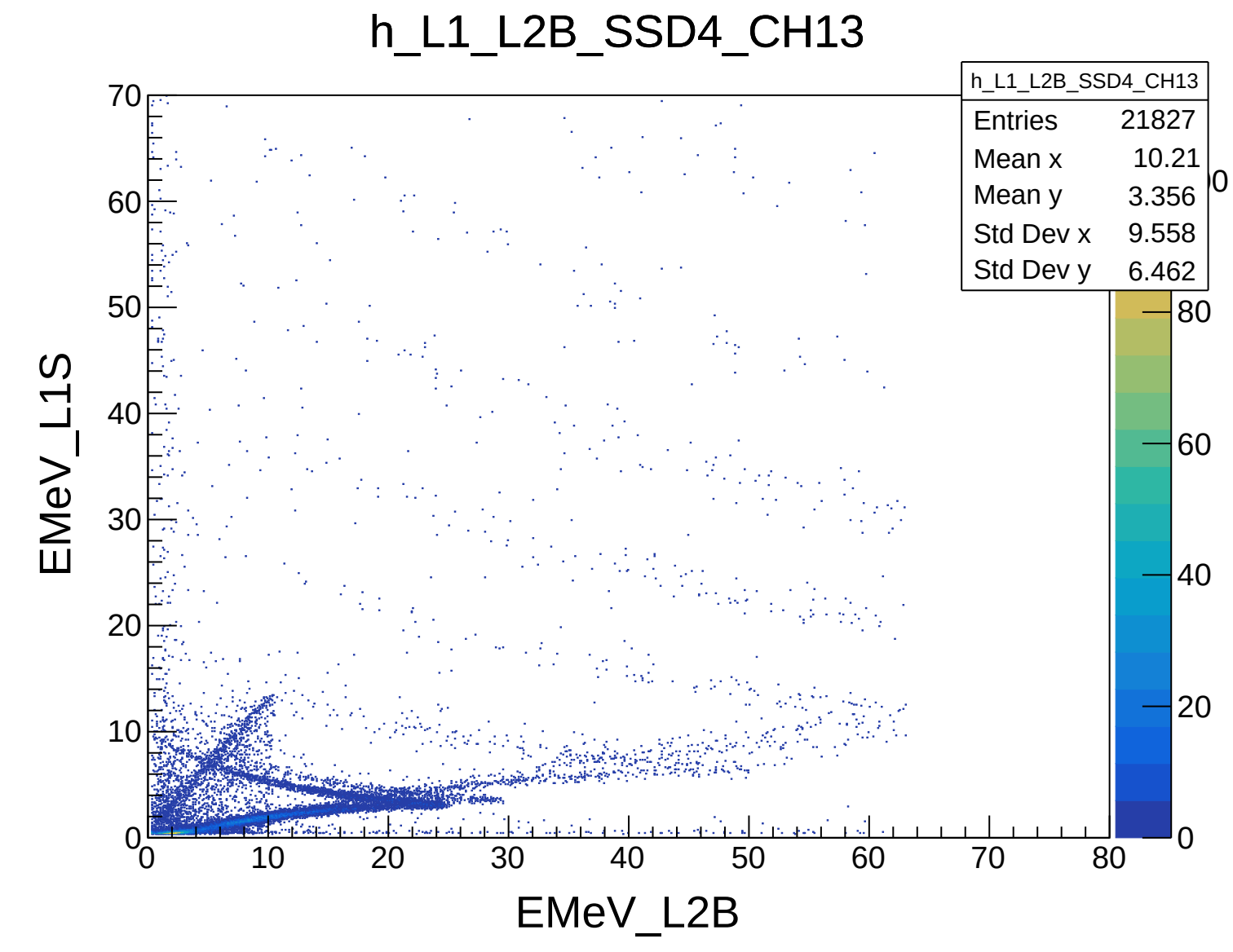

h_L1_L2B_SSD4_CH8
h_L1_L2B_SSD4_CH8
Entries 23302
Mean x 10.31
Mean y 3.37
Std Dev x 9.76
Std Dev y 6.692
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

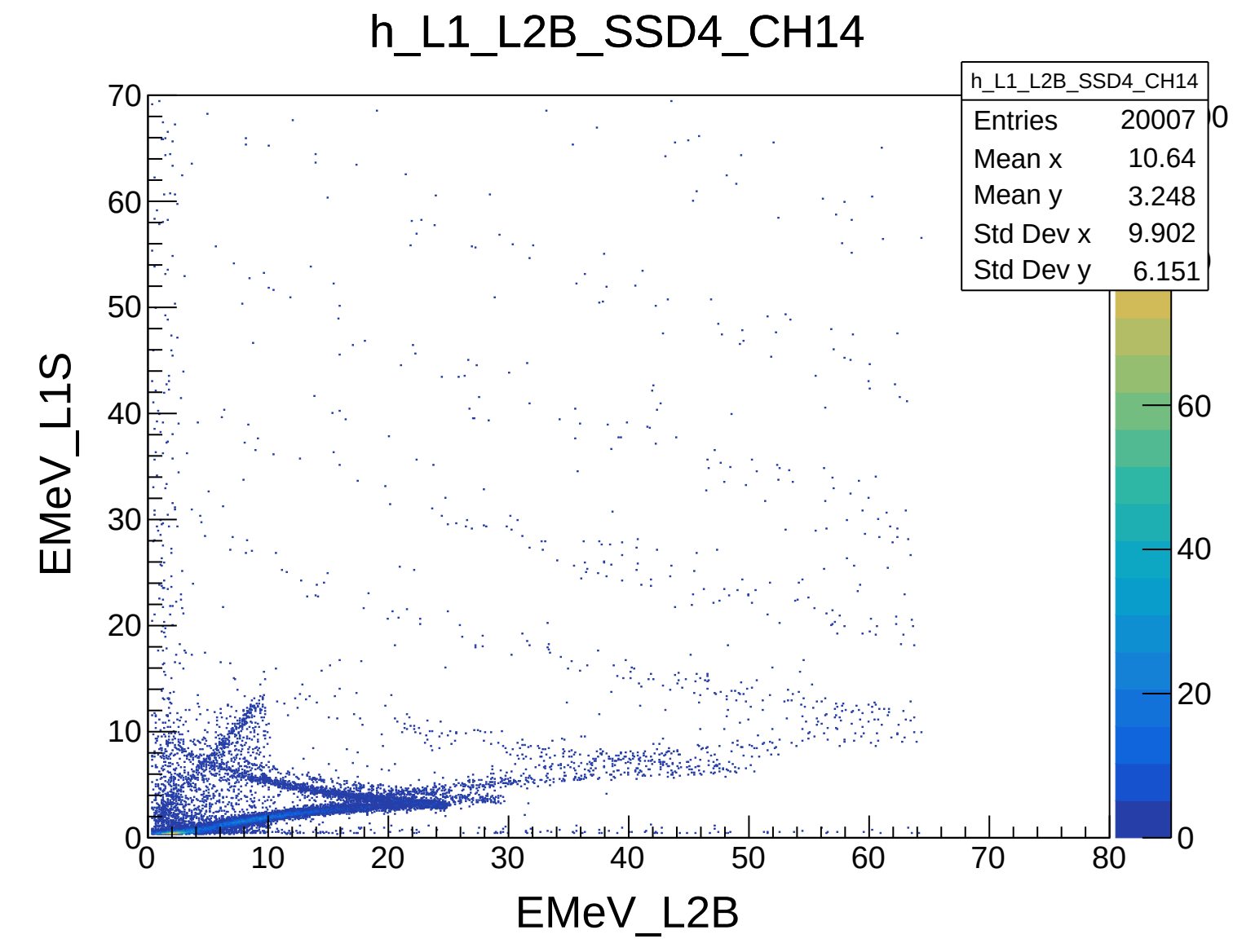

h_L1_L2B_SSD4_CH9
h_L1_L2B_SSD4_CH9
Entries 22692
Mean x 10.29
Mean y 3.281
Std Dev x 9.693
Std Dev y 6.392
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80

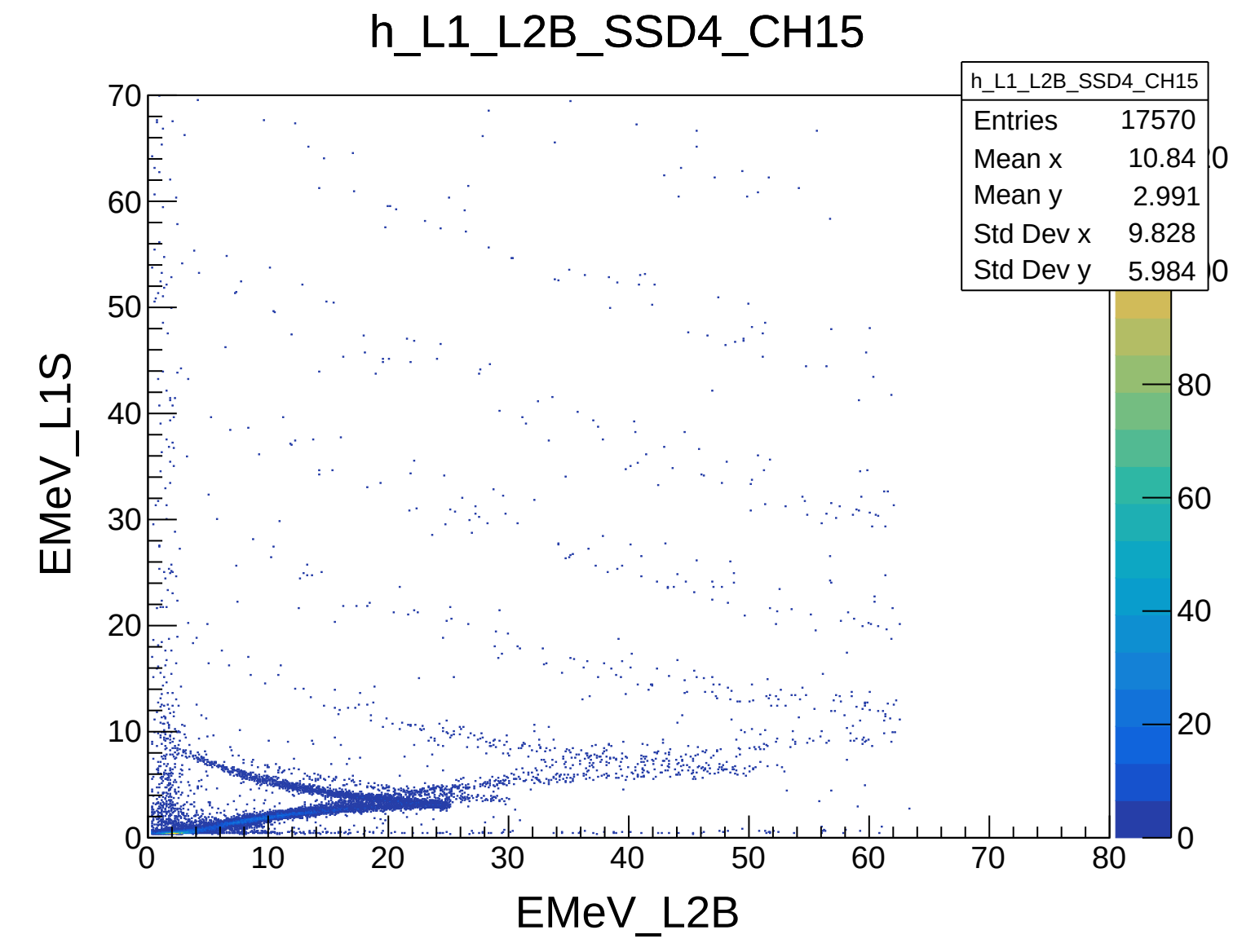

h_L1_L2B_SSD4_CH10
h_L1_L2B_SSD4_CH10
Entries 22840
Mean x 10.17
Mean y 3.313
Std Dev x 9.635
Std Dev y 6.435
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80


h_L1_L2B_SSD4_CH11
h_L1_L2B_SSD4_CH11
Entries 22989
Mean x 10.19
Mean y 3.497
Std Dev x 9.808
Std Dev y 6.767
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80


h_L1_L2B_SSD4_CH12
h_L1_L2B_SSD4_CH12
Entries 22915
Mean x 10.06
Mean y 3.496
Std Dev x 9.592
Std Dev y 6.927
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
100


h_L1_L2B_SSD4_CH13
h_L1_L2B_SSD4_CH13
Entries 21827
Mean x 10.21
Mean y 3.356
Std Dev x 9.558
Std Dev y 6.462
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80


h_L1_L2B_SSD4_CH14
h_L1_L2B_SSD4_CH14
Entries 20007
Mean x 10.64
Mean y 3.248
Std Dev x 9.902
Std Dev y 6.151
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80


h_L1_L2B_SSD4_CH15
h_L1_L2B_SSD4_CH15
Entries 17570
Mean x 10.84
Mean y 2.991
Std Dev x 9.828
Std Dev y 5.984
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80