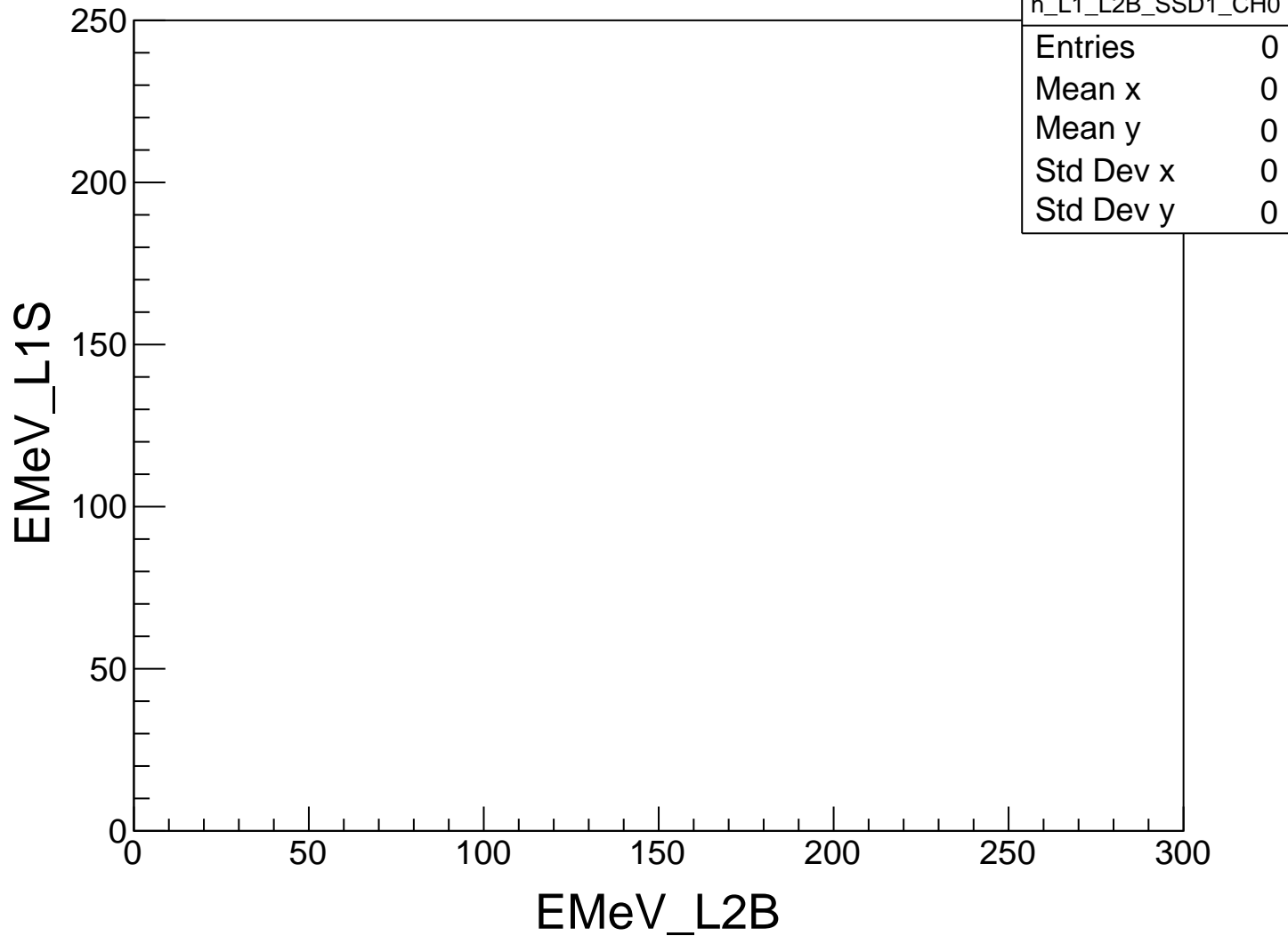
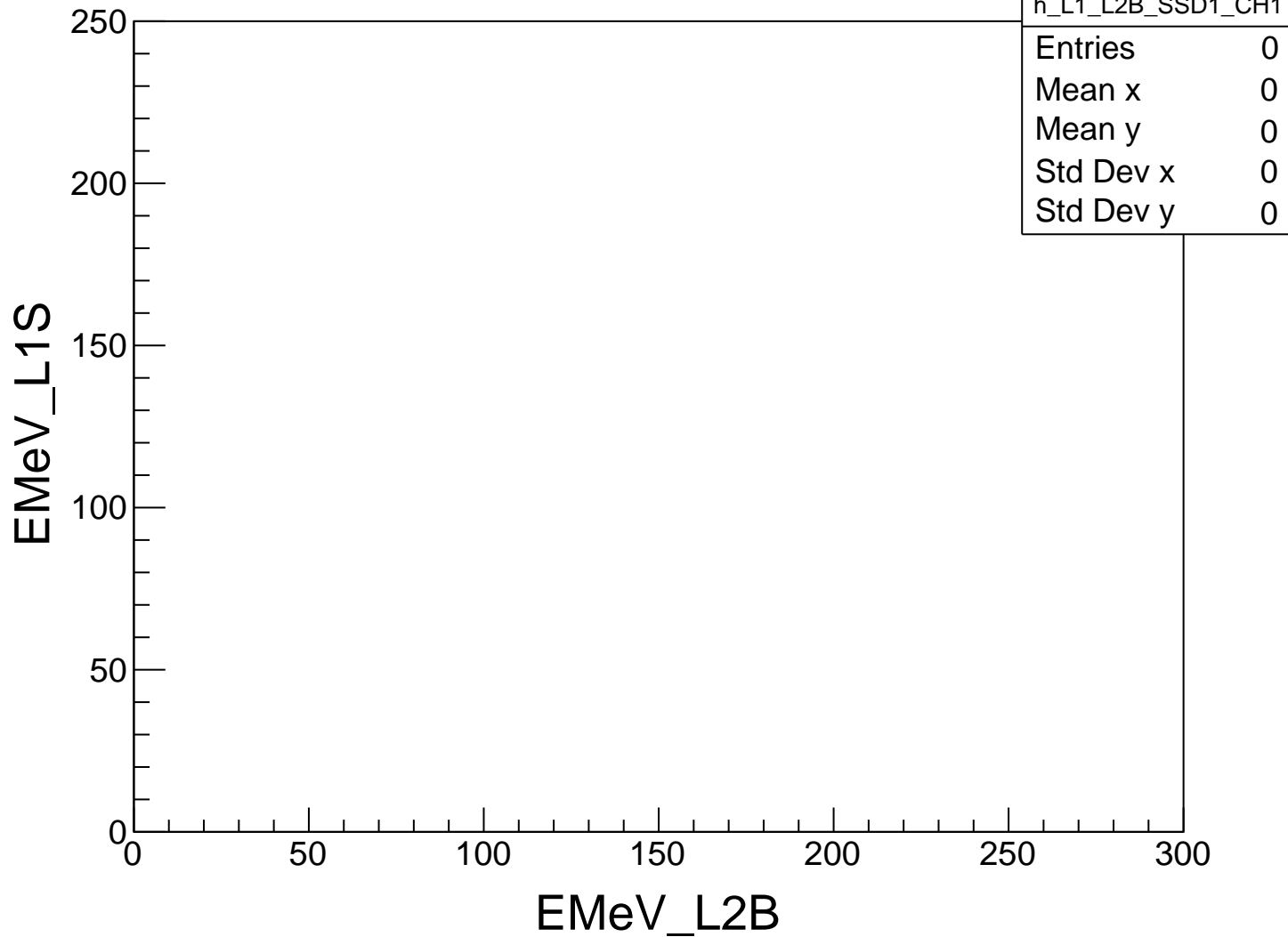


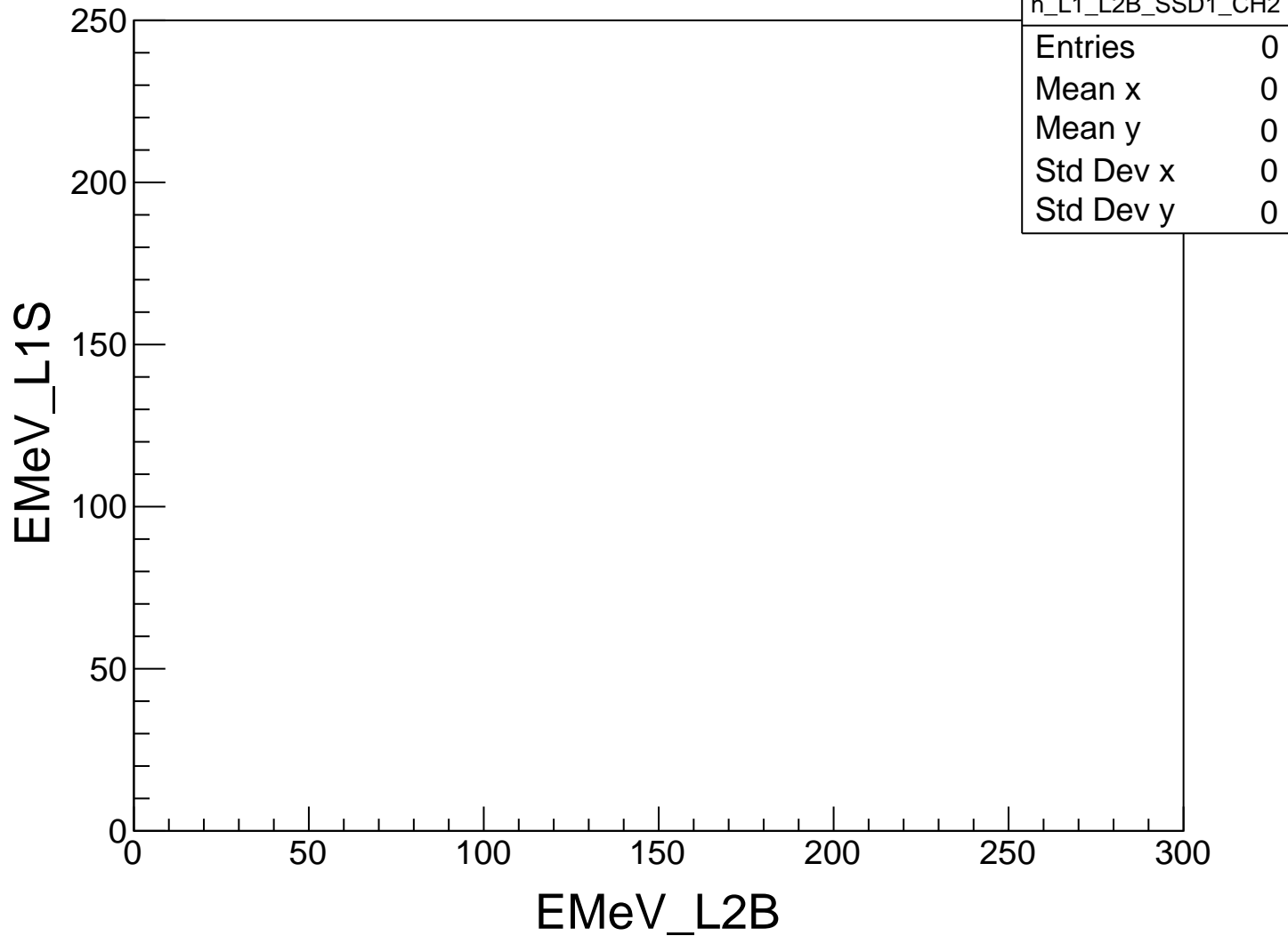
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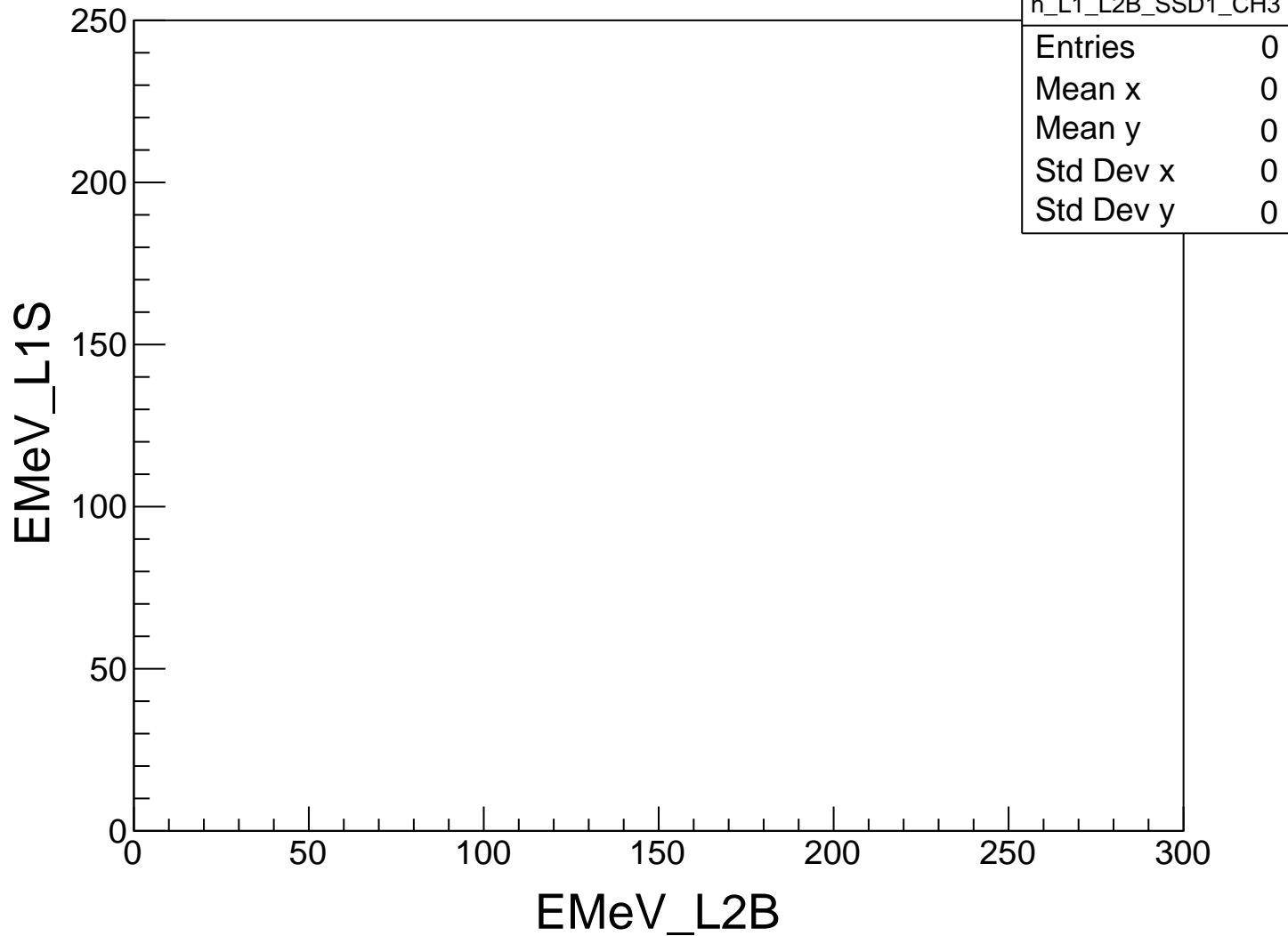
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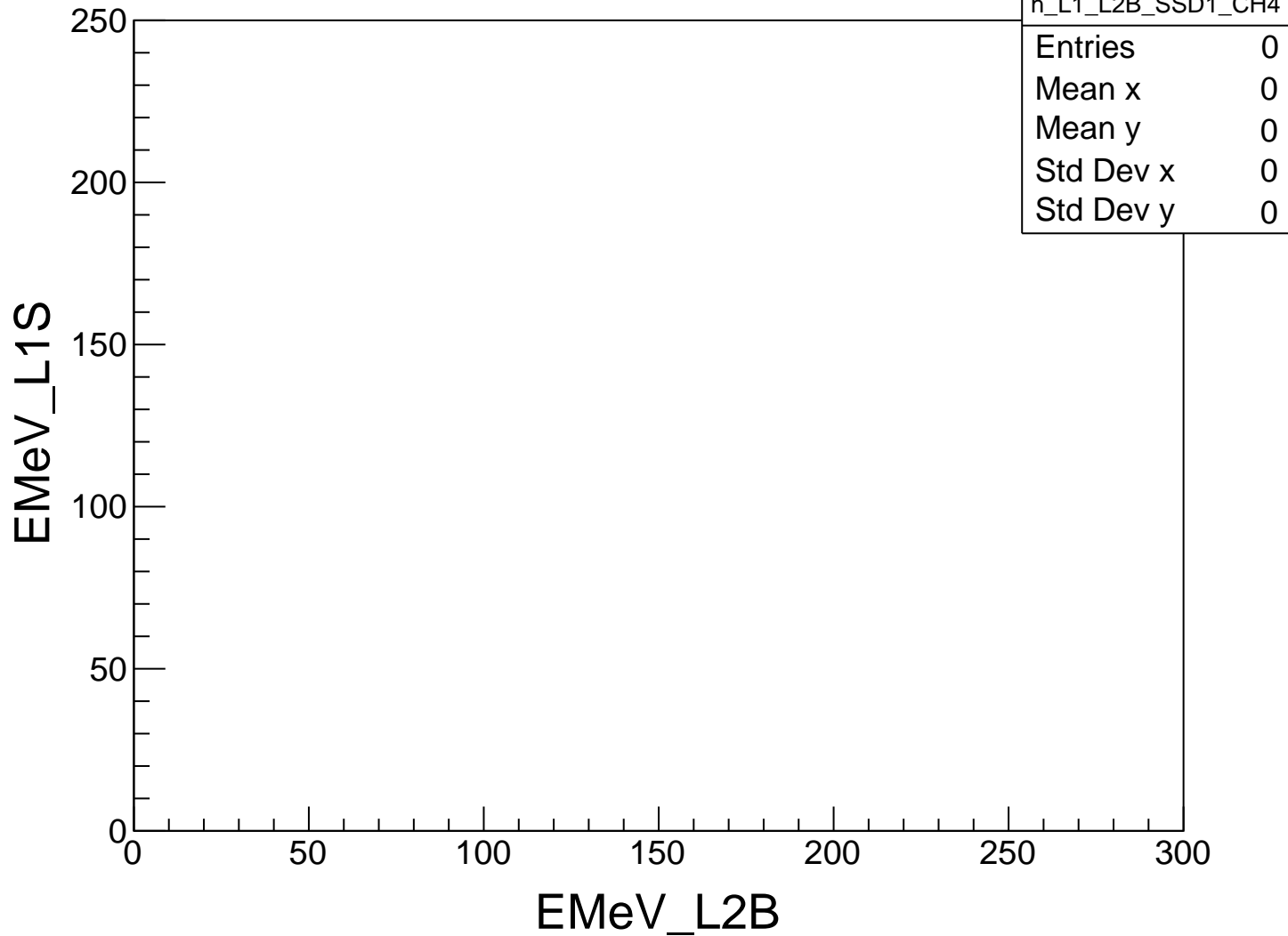
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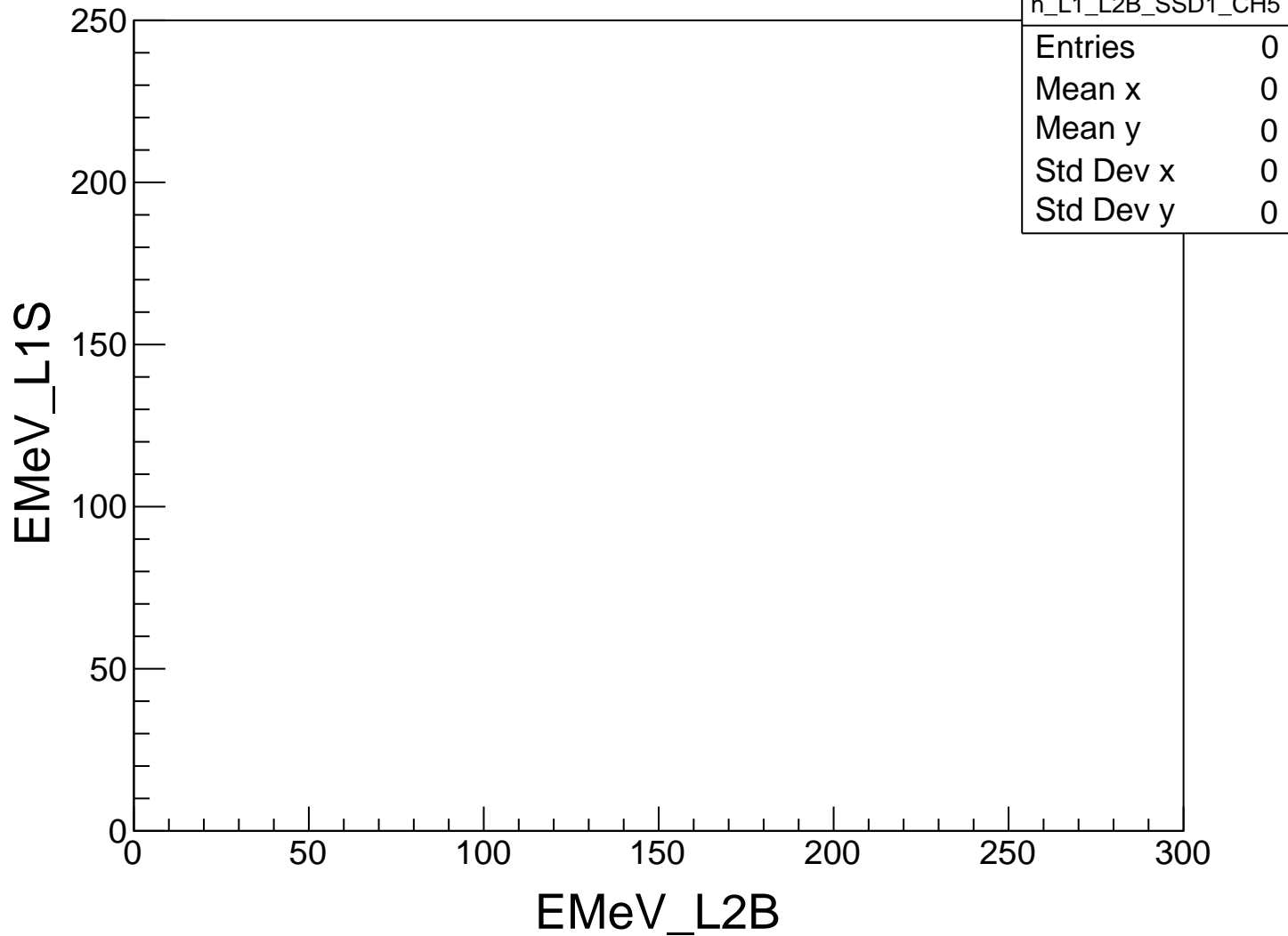
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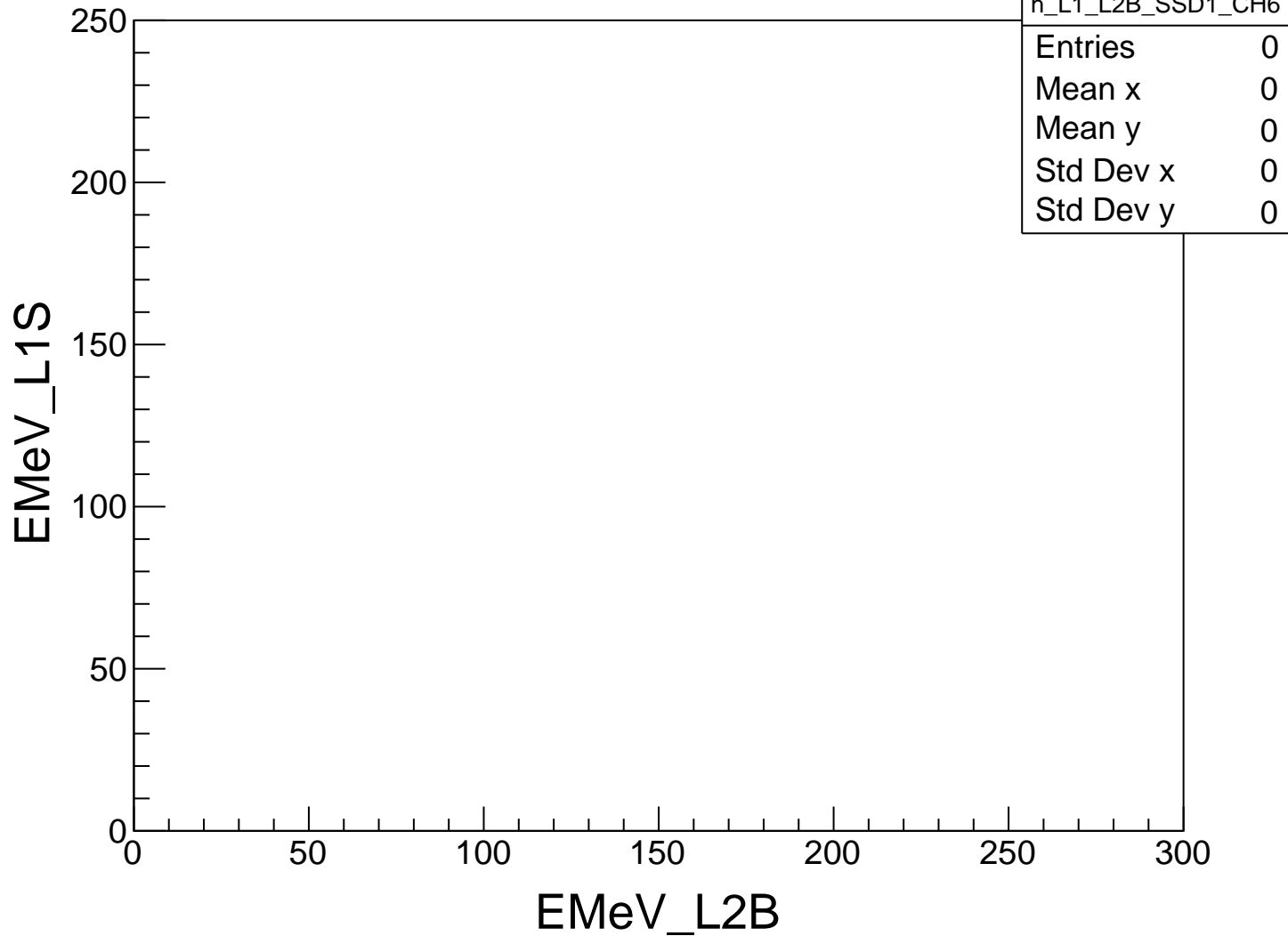
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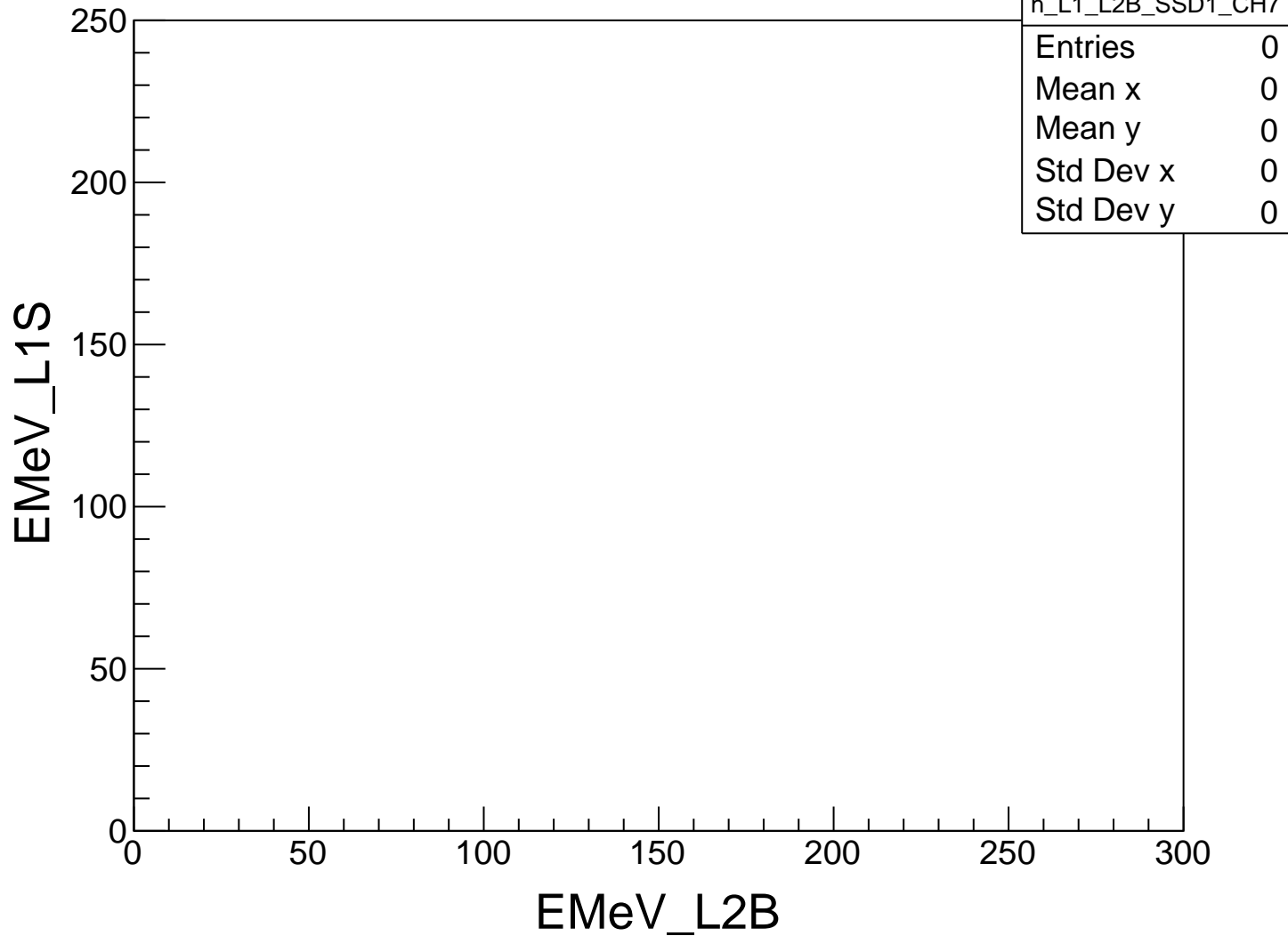
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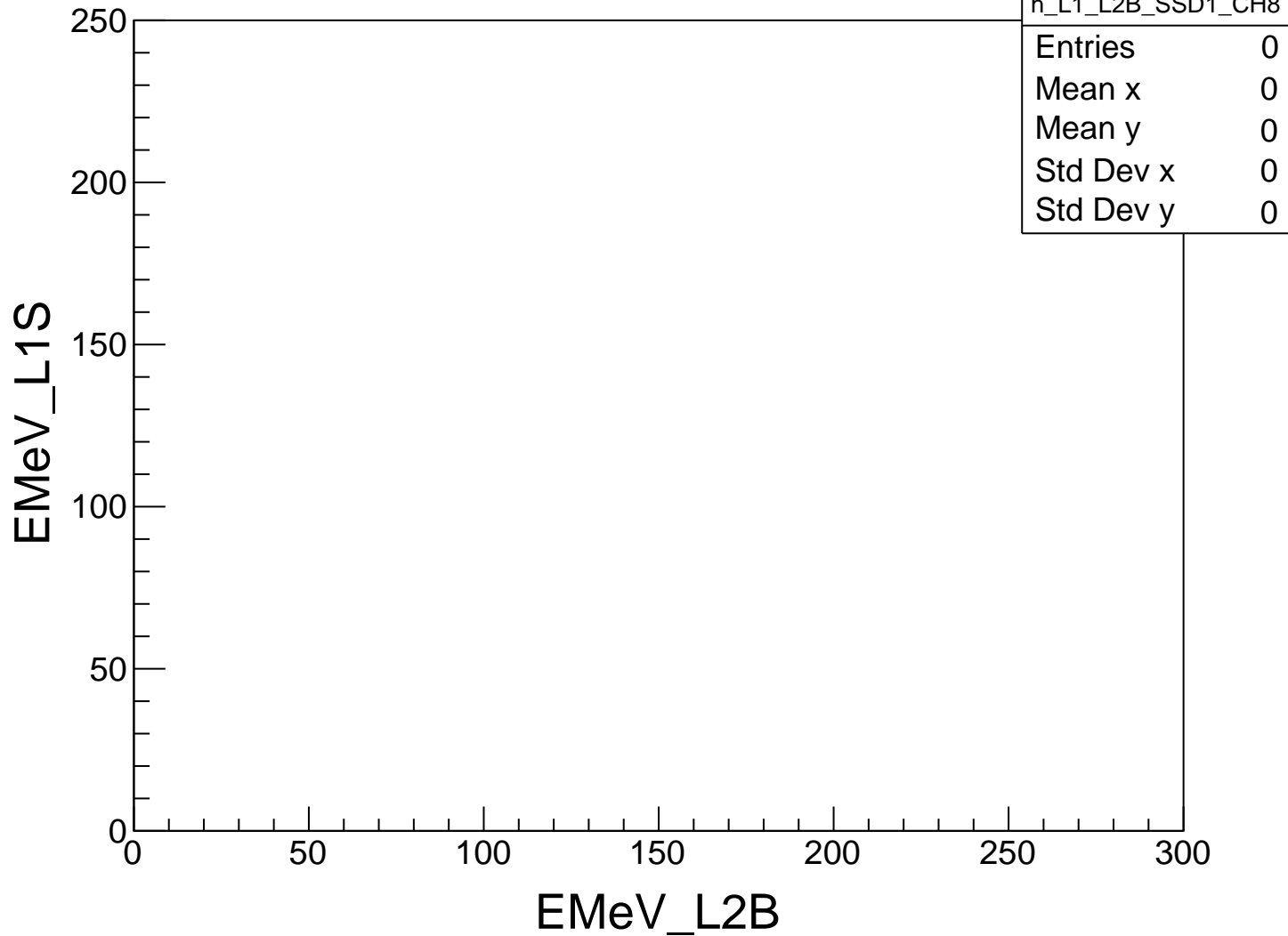
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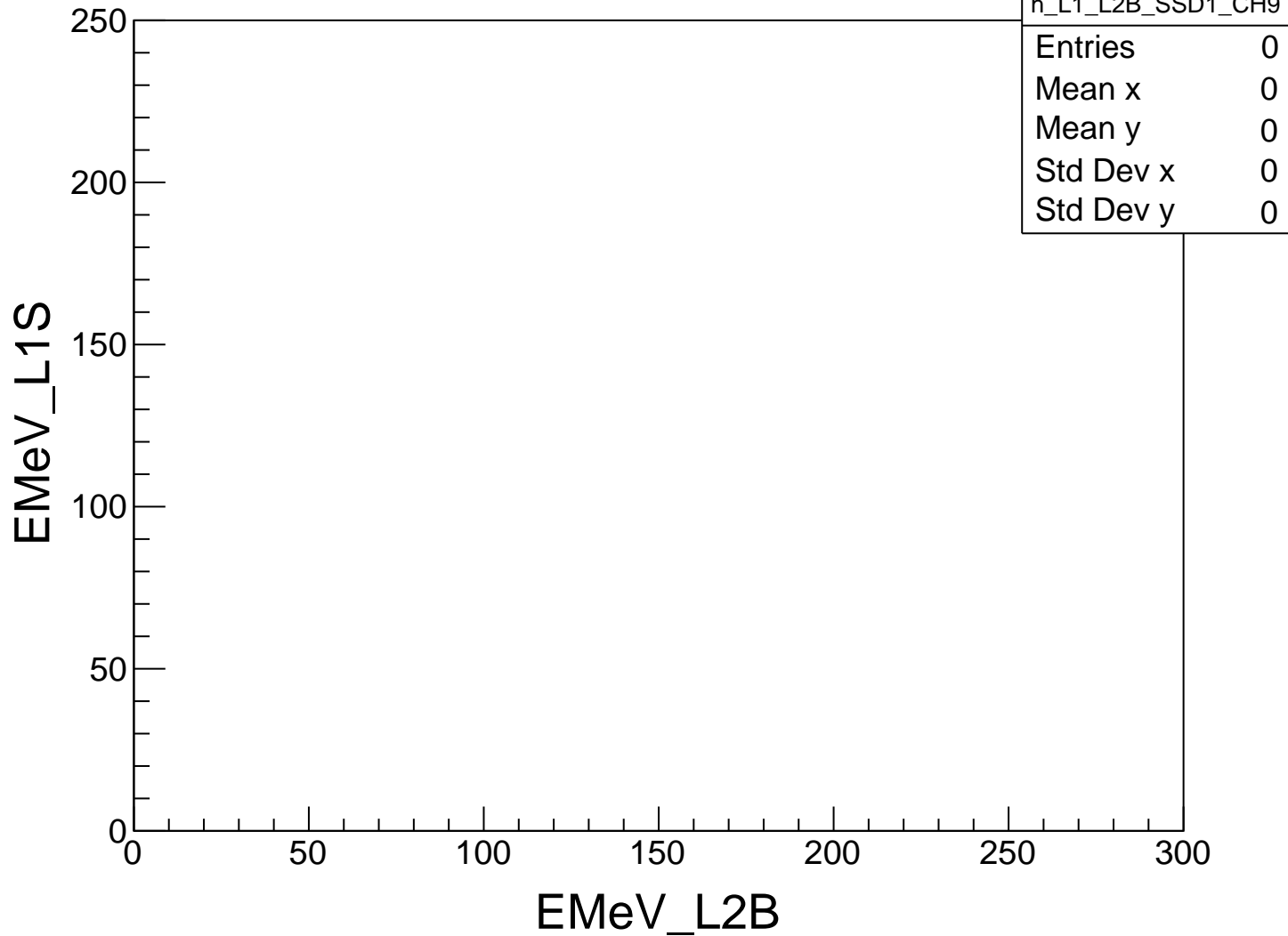
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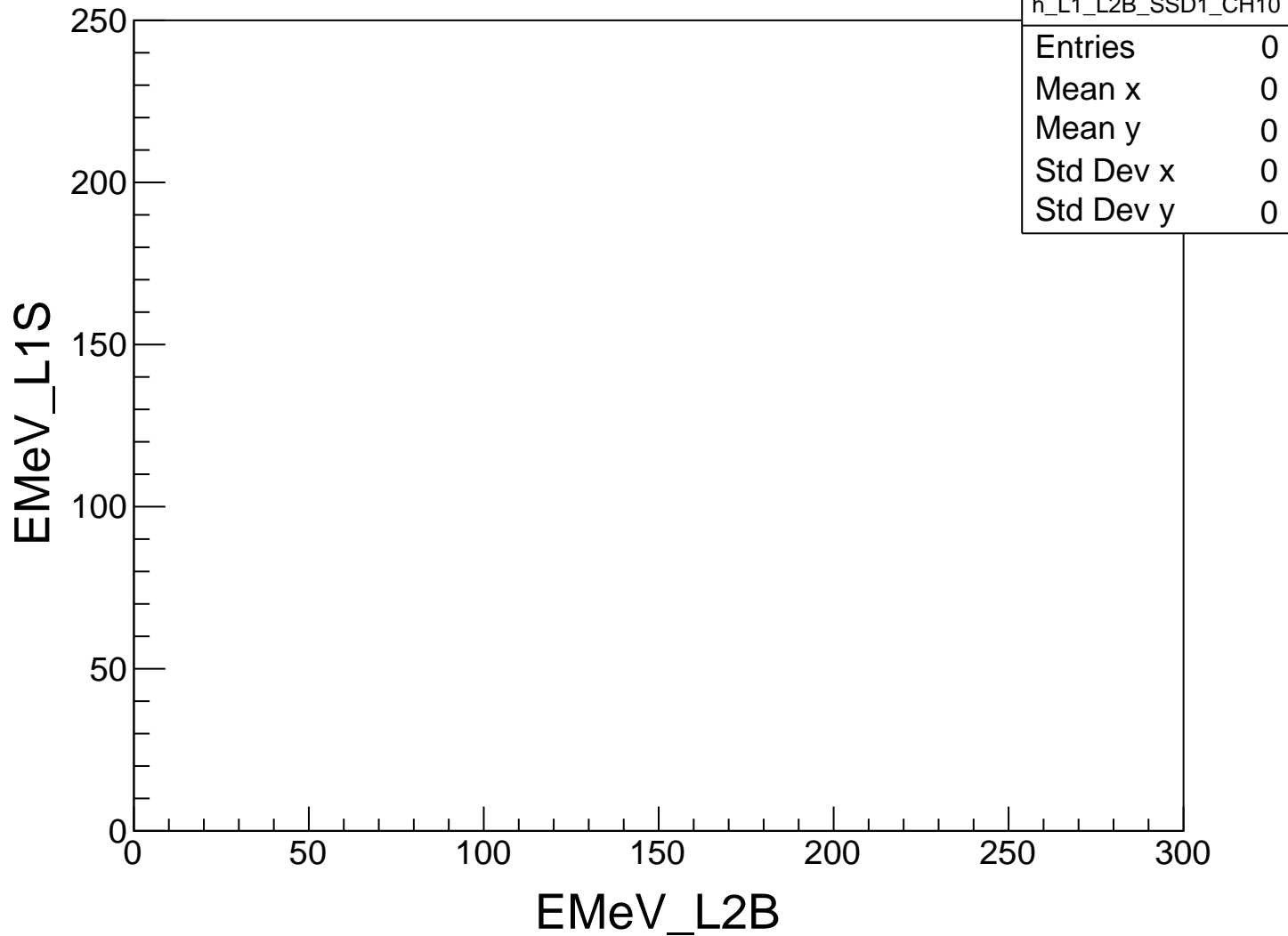
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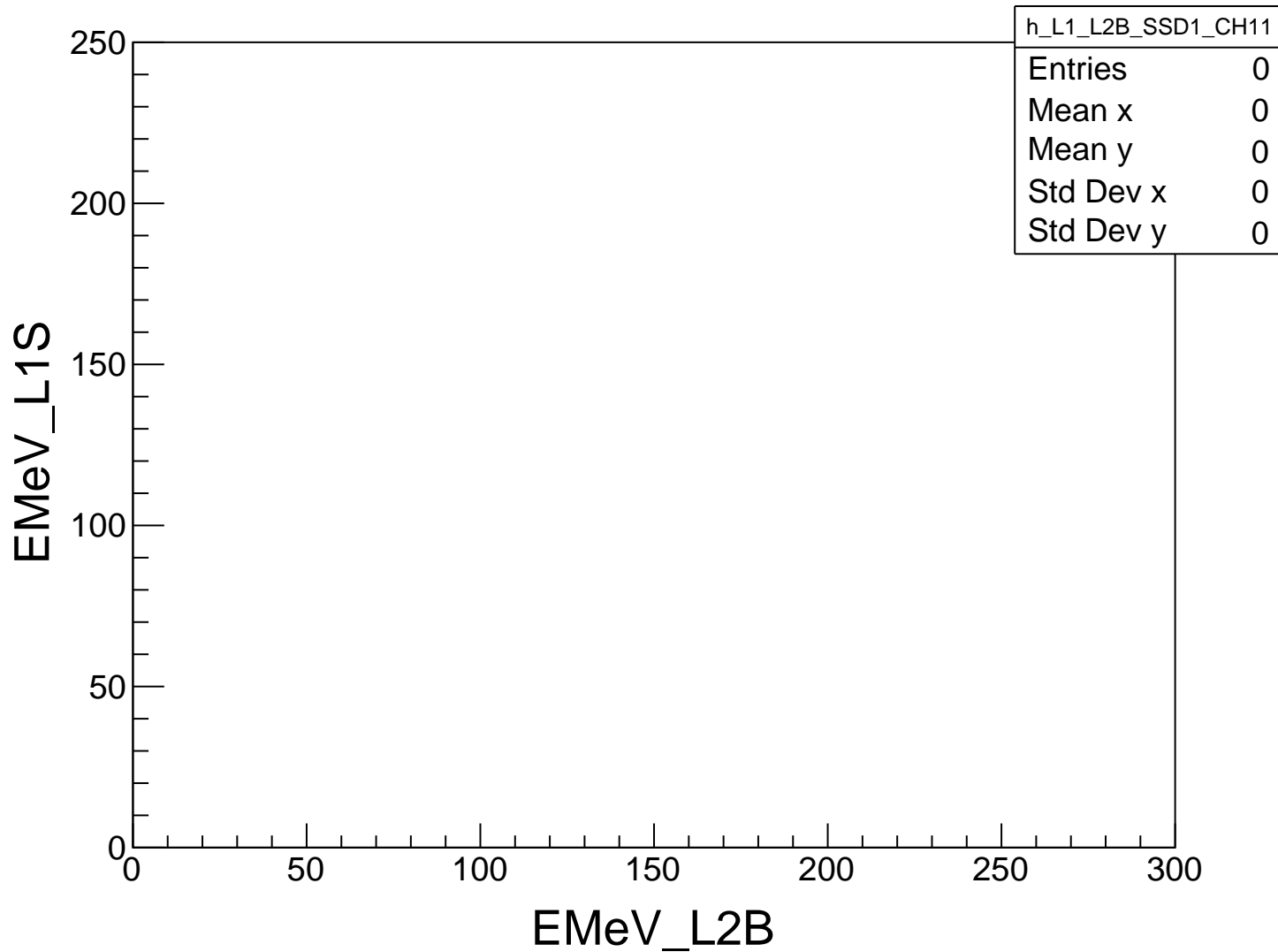
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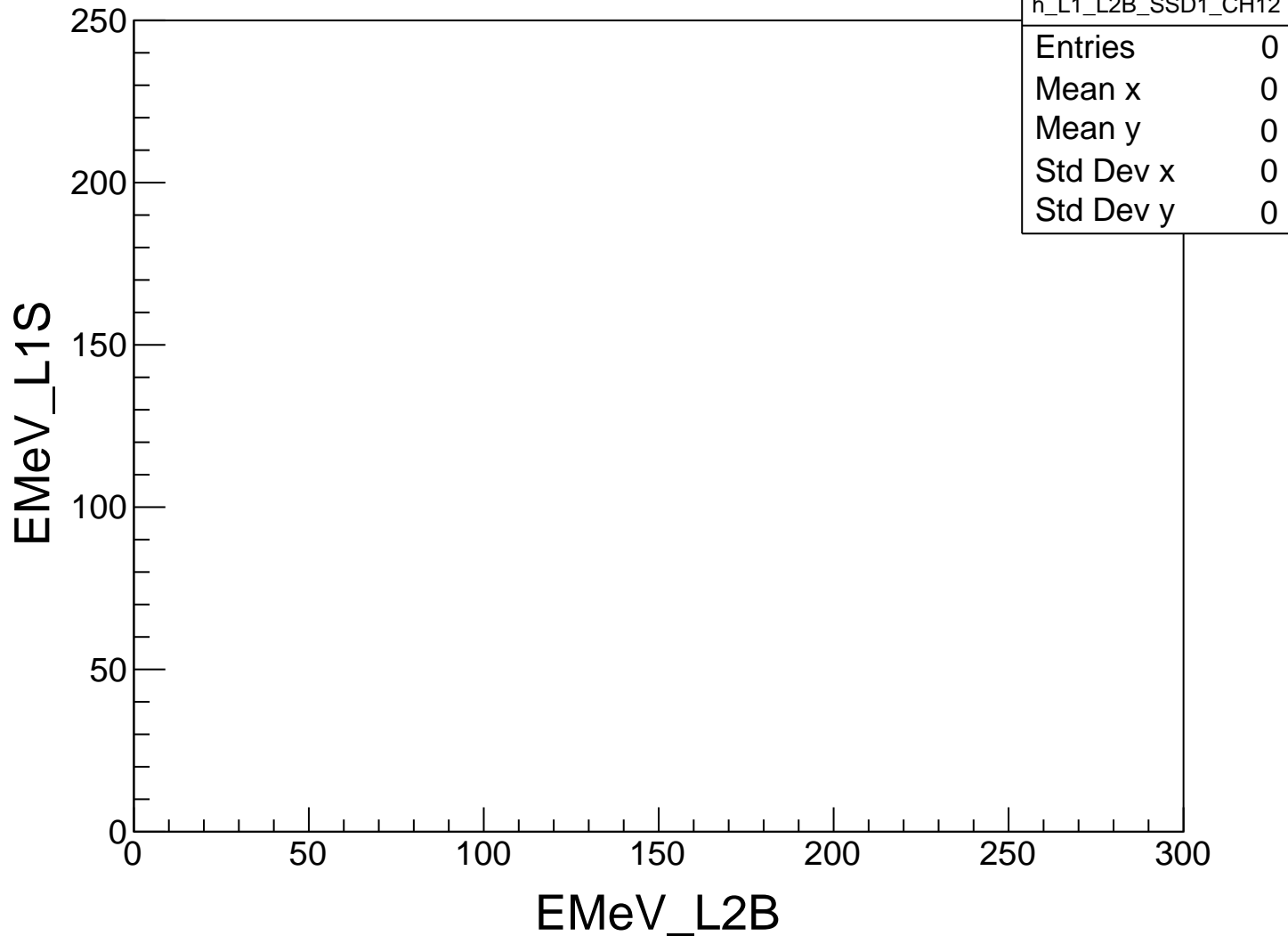
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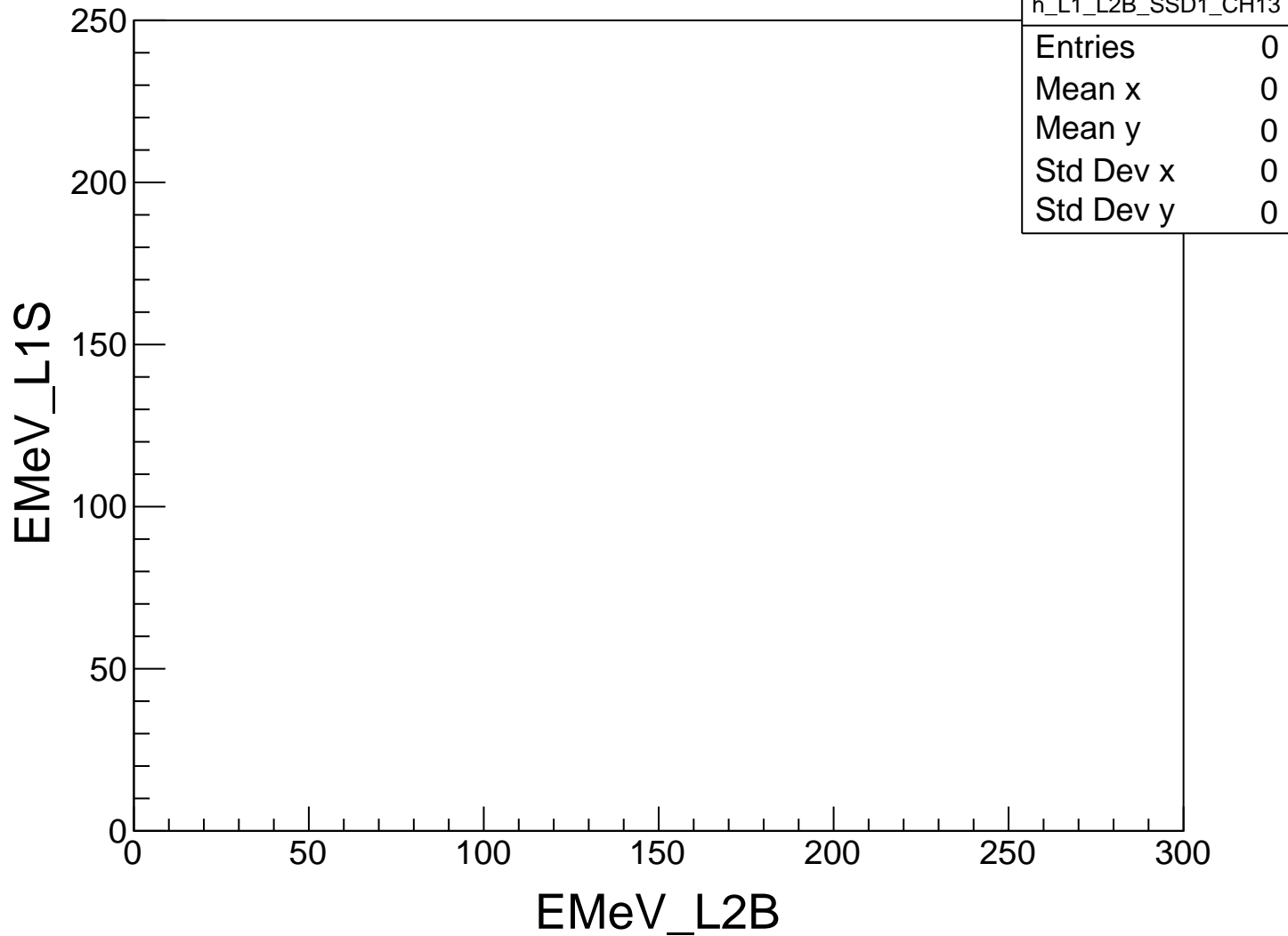
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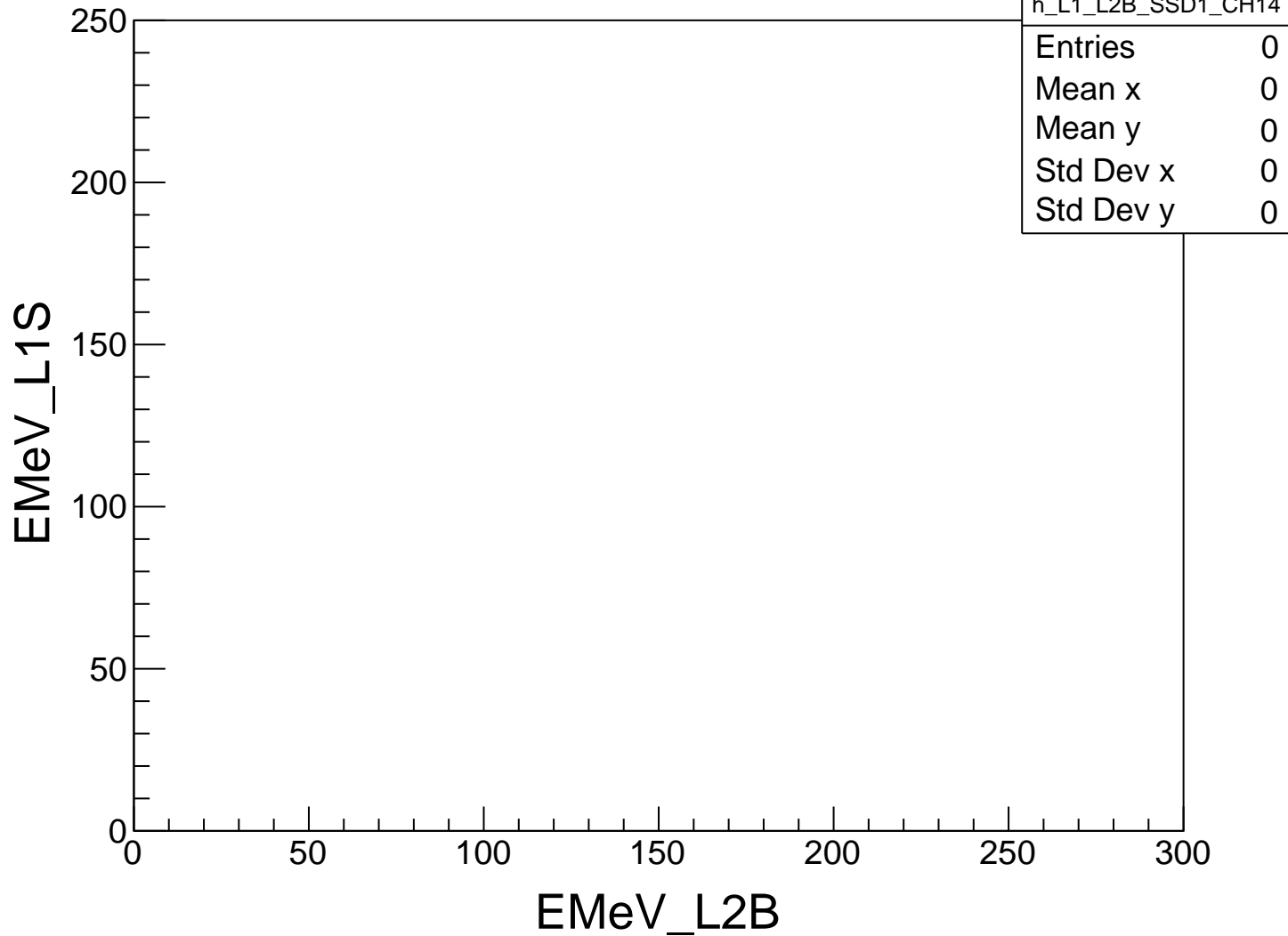
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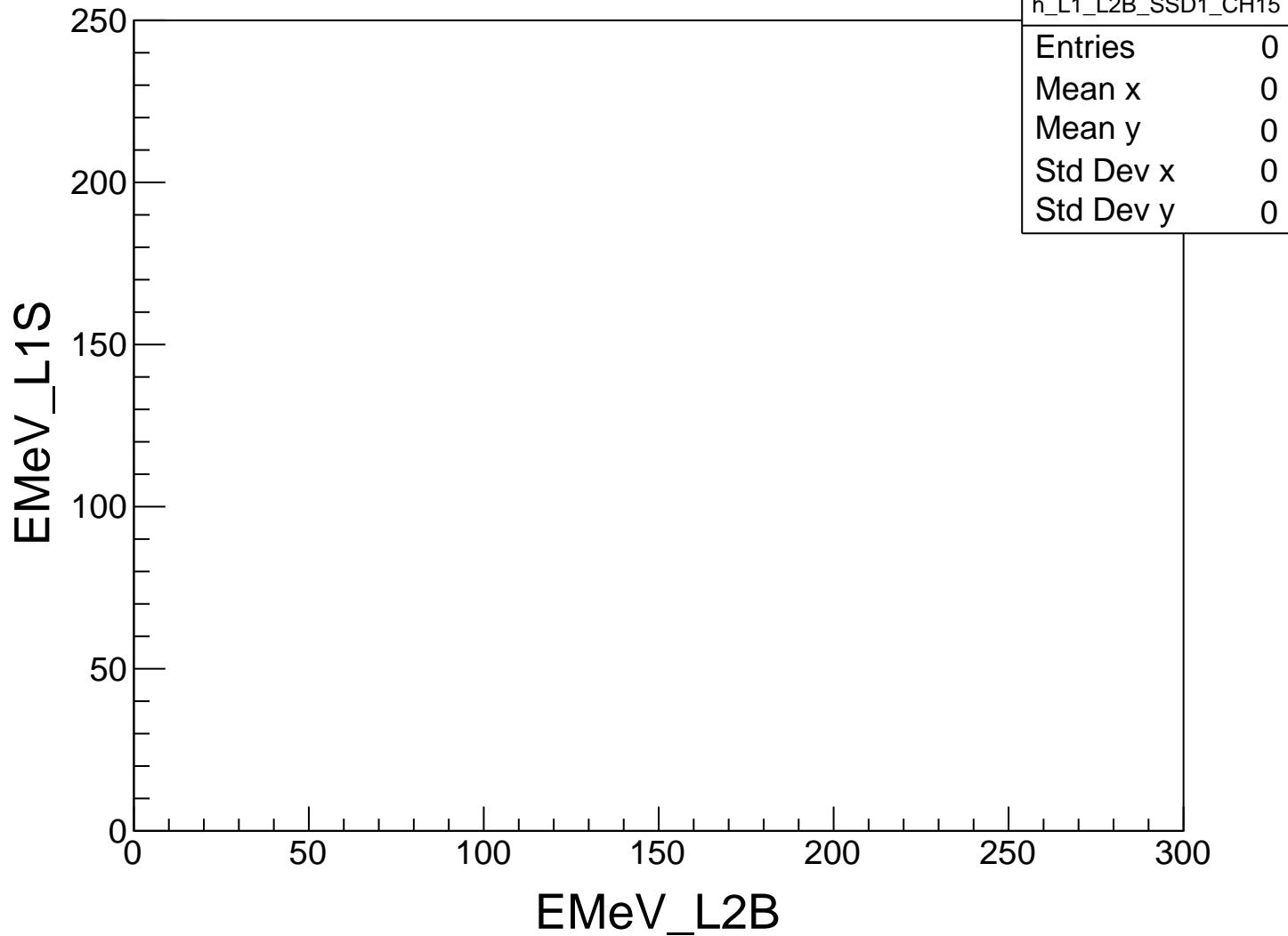
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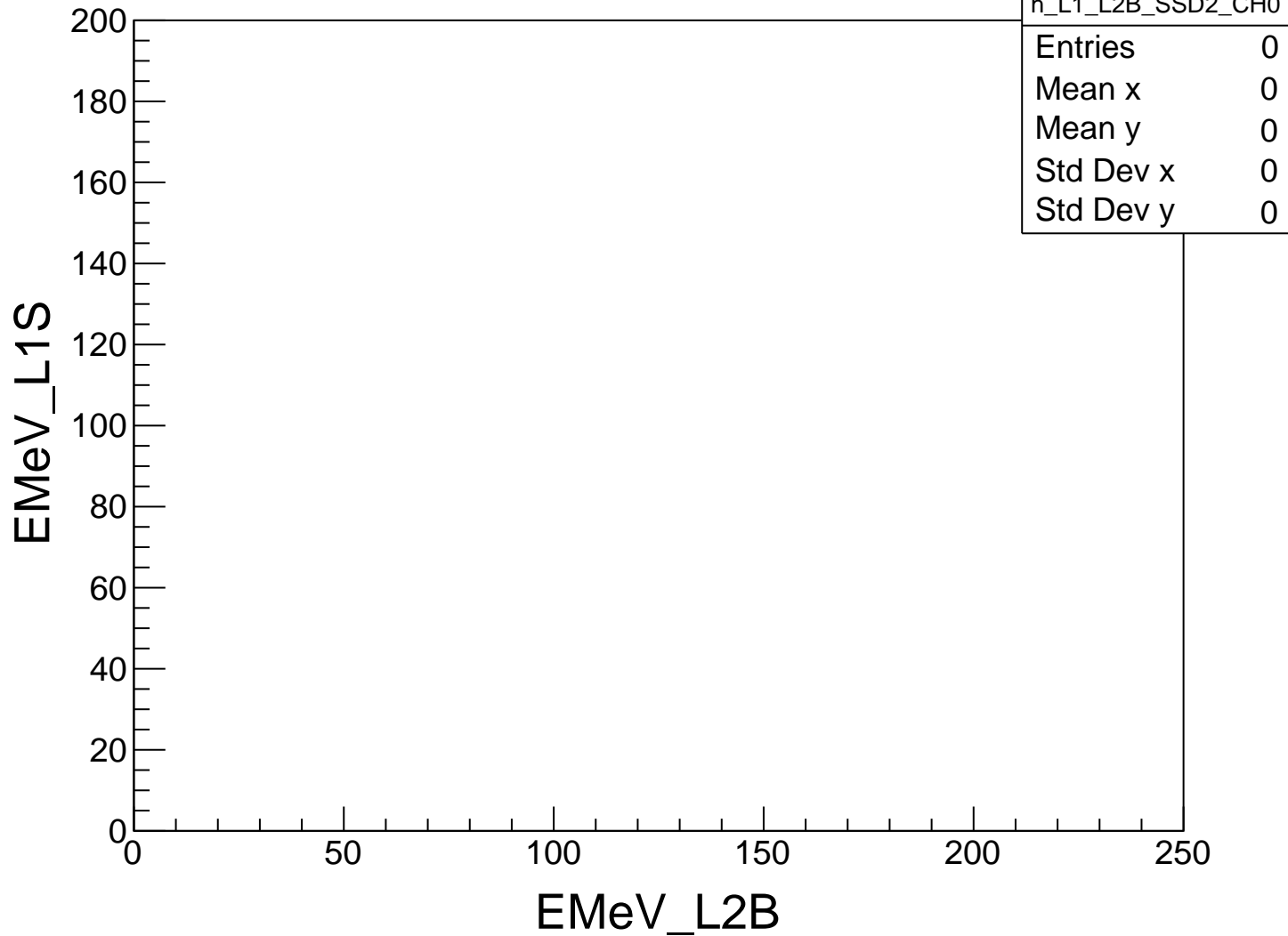
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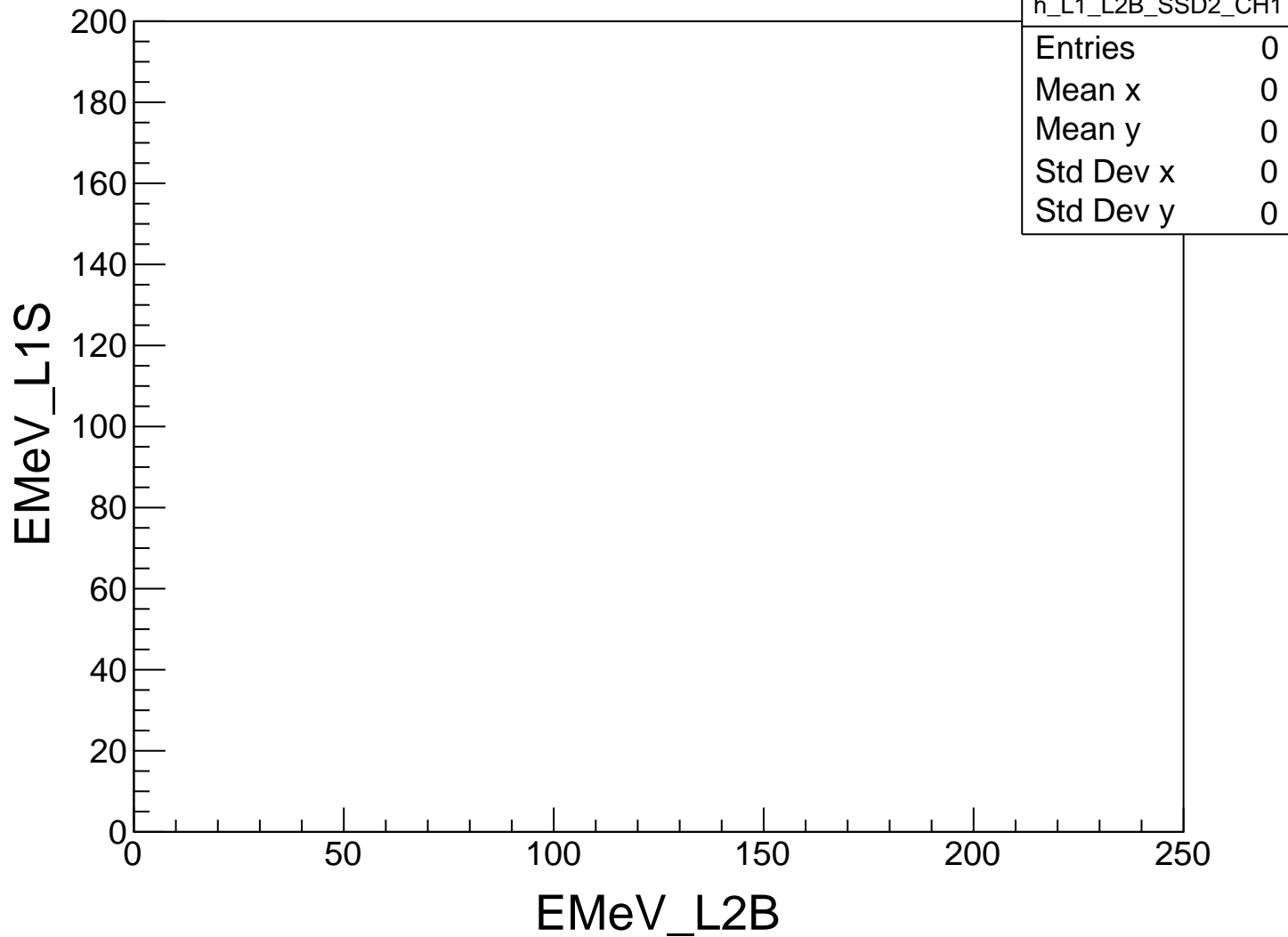
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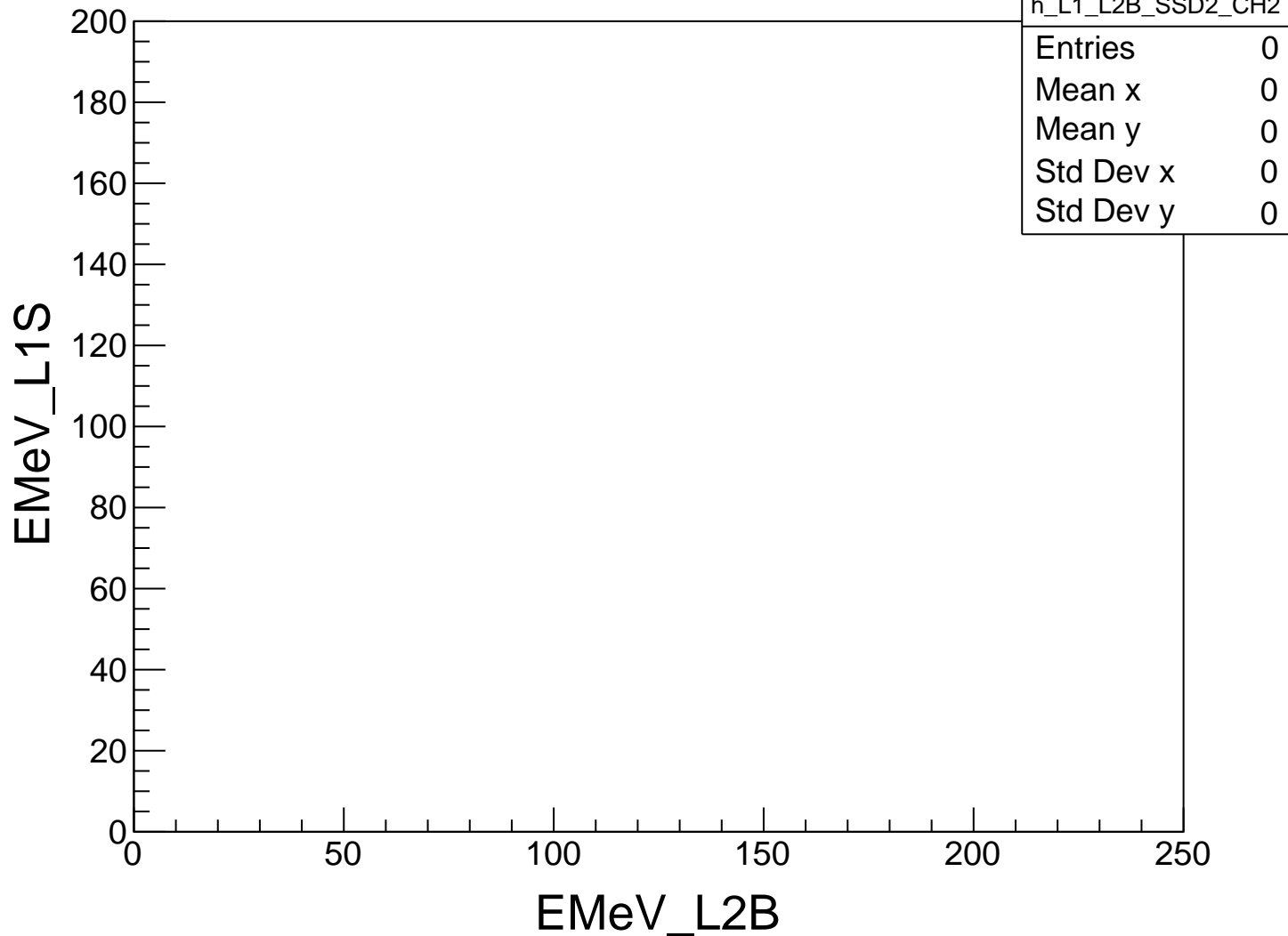
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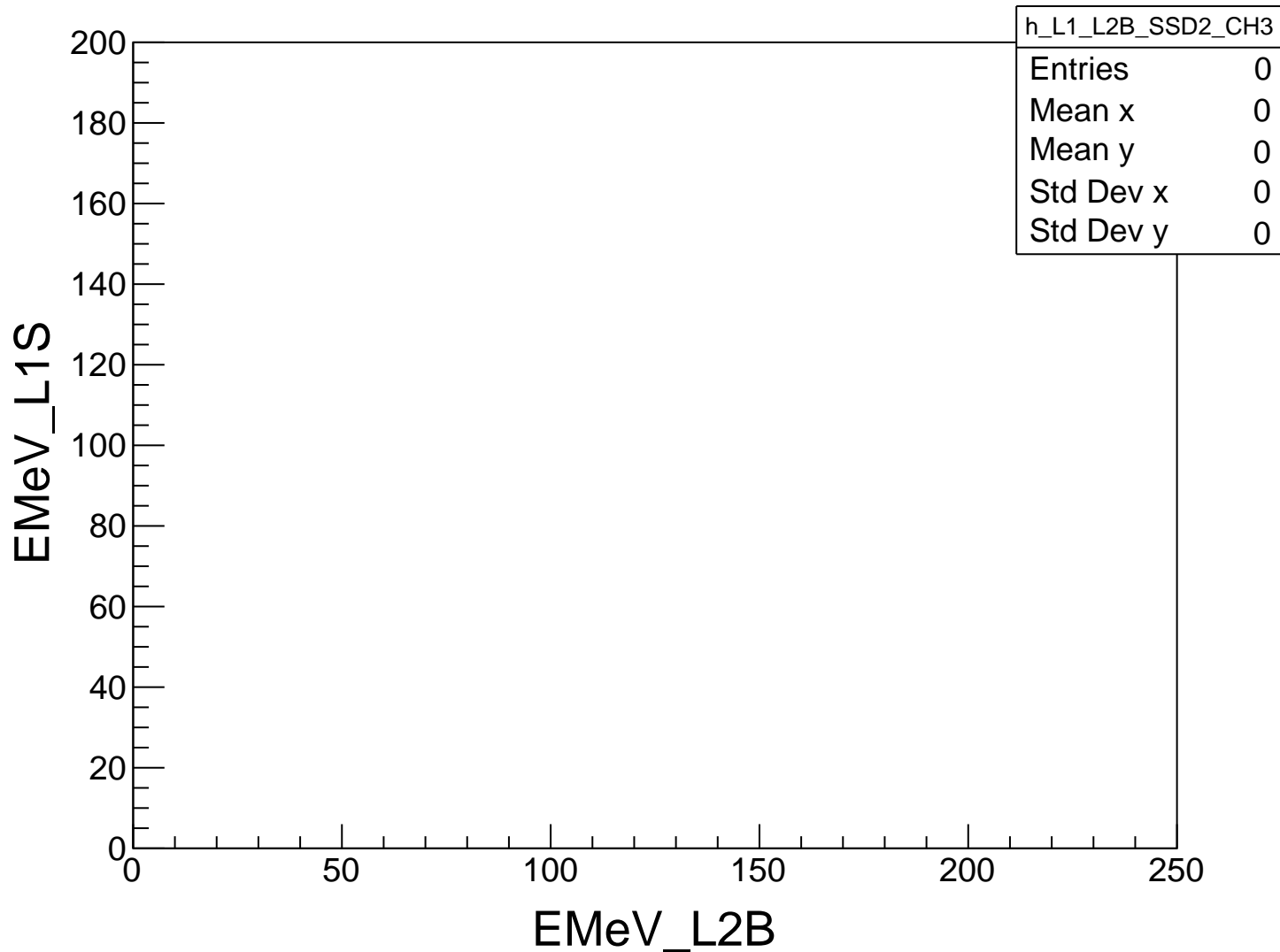
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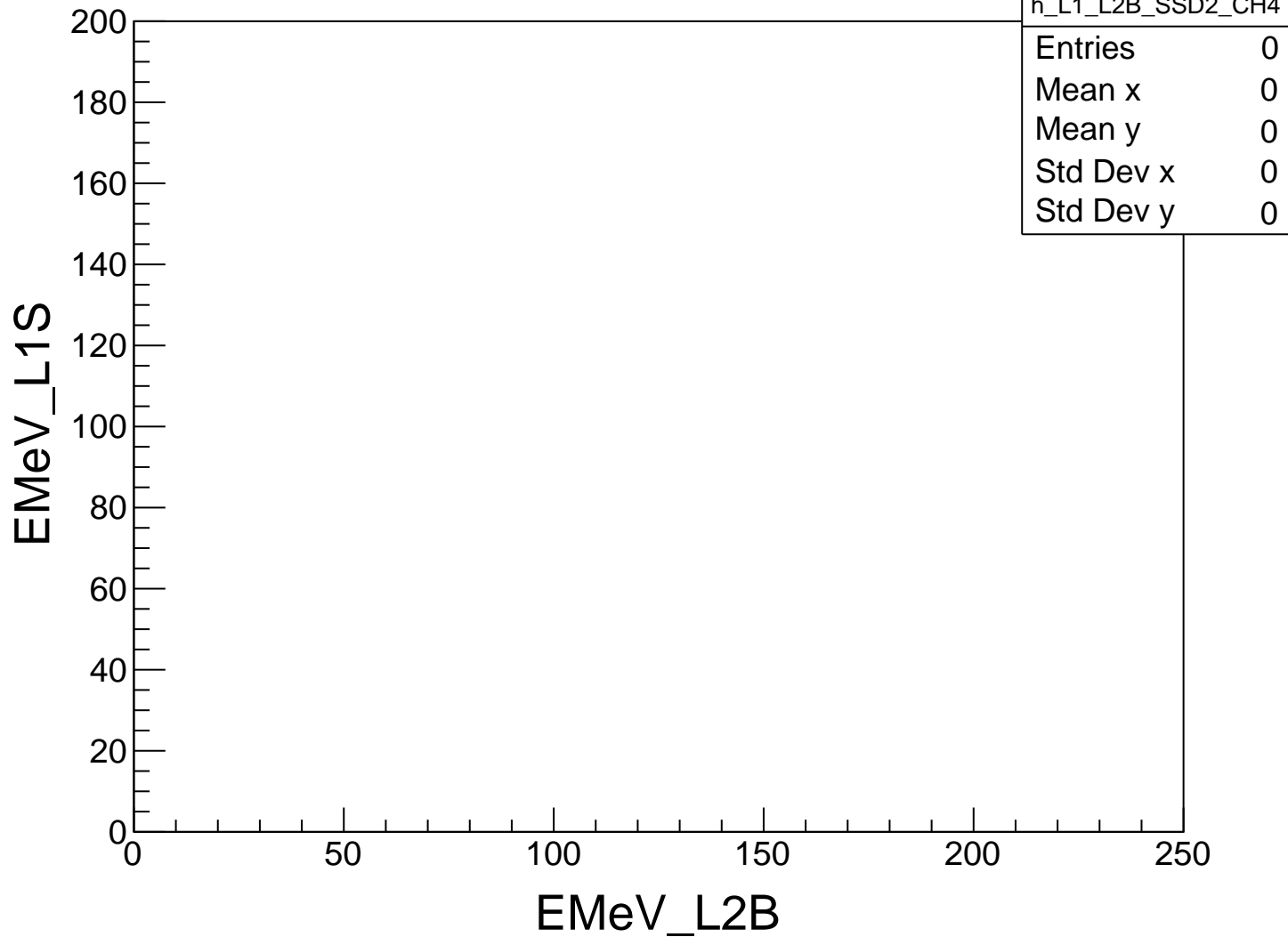
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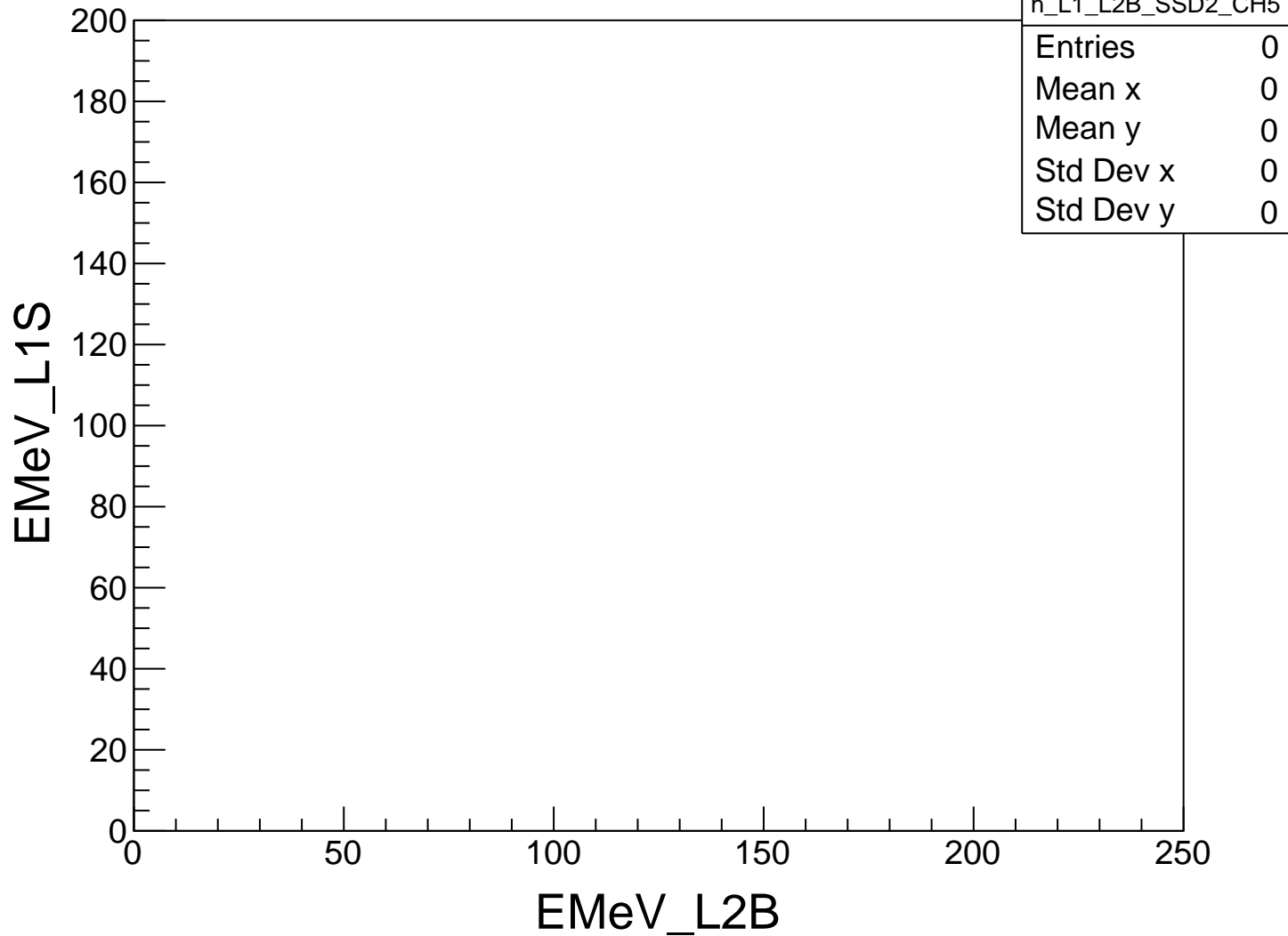
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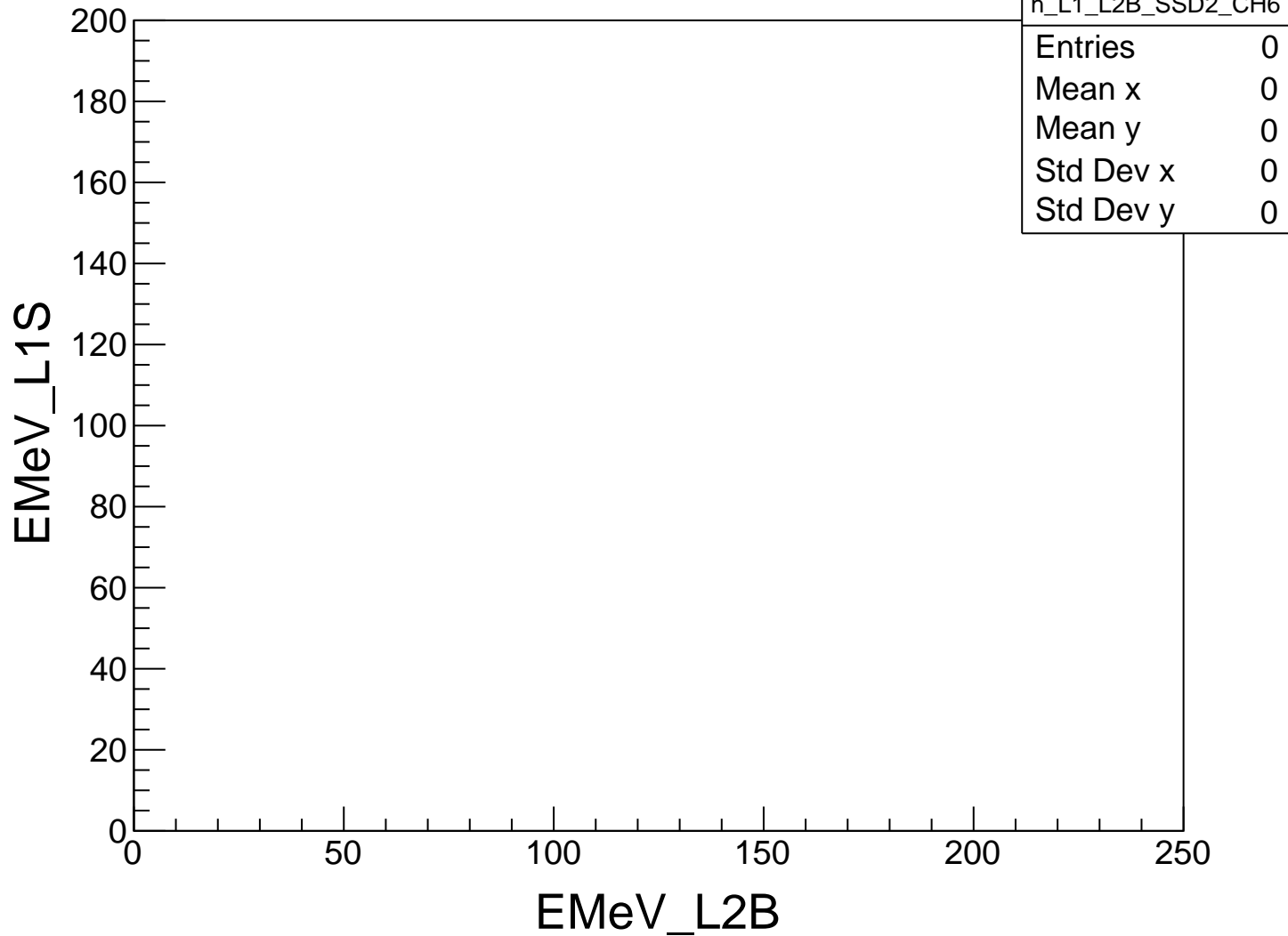
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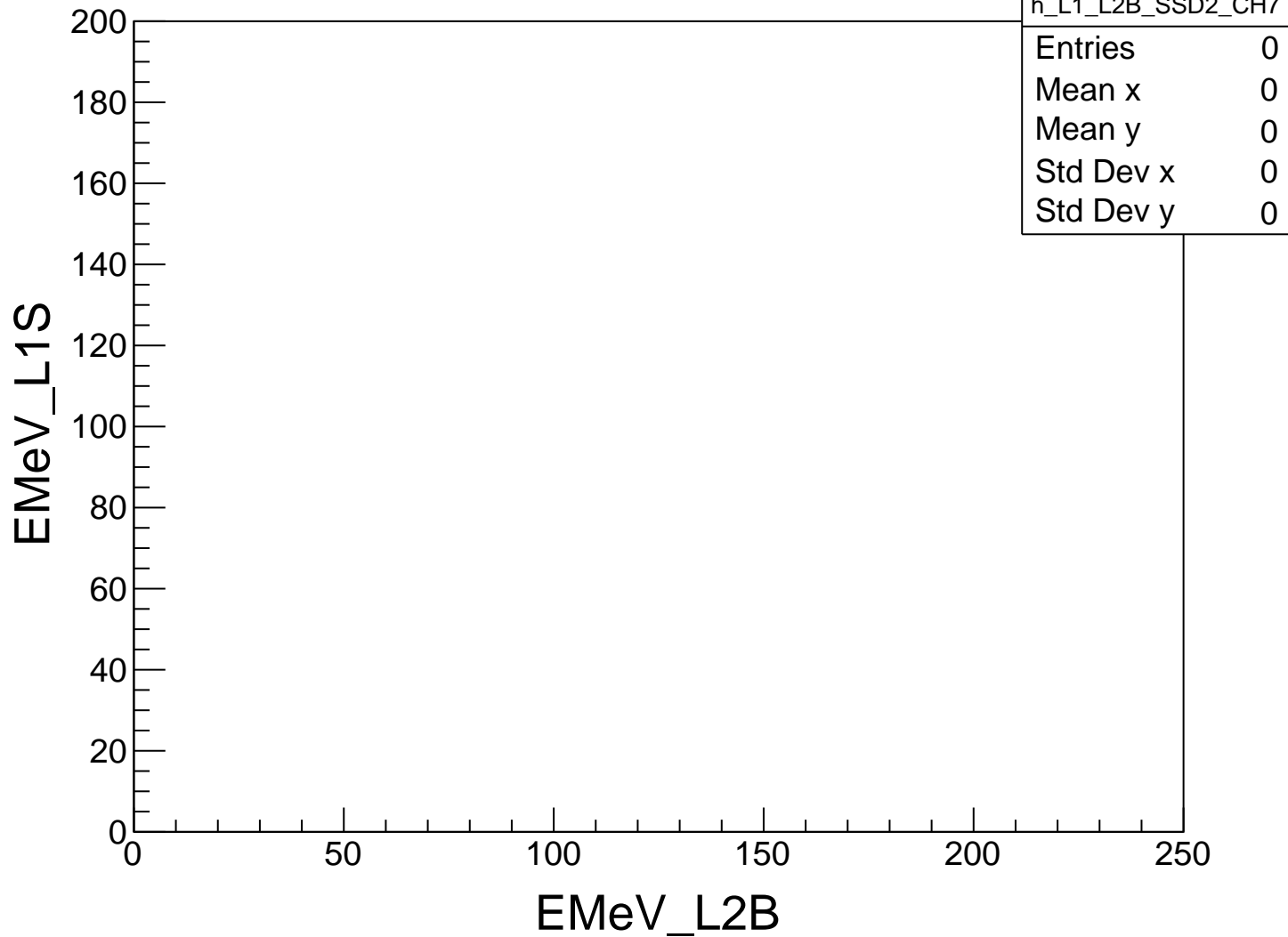
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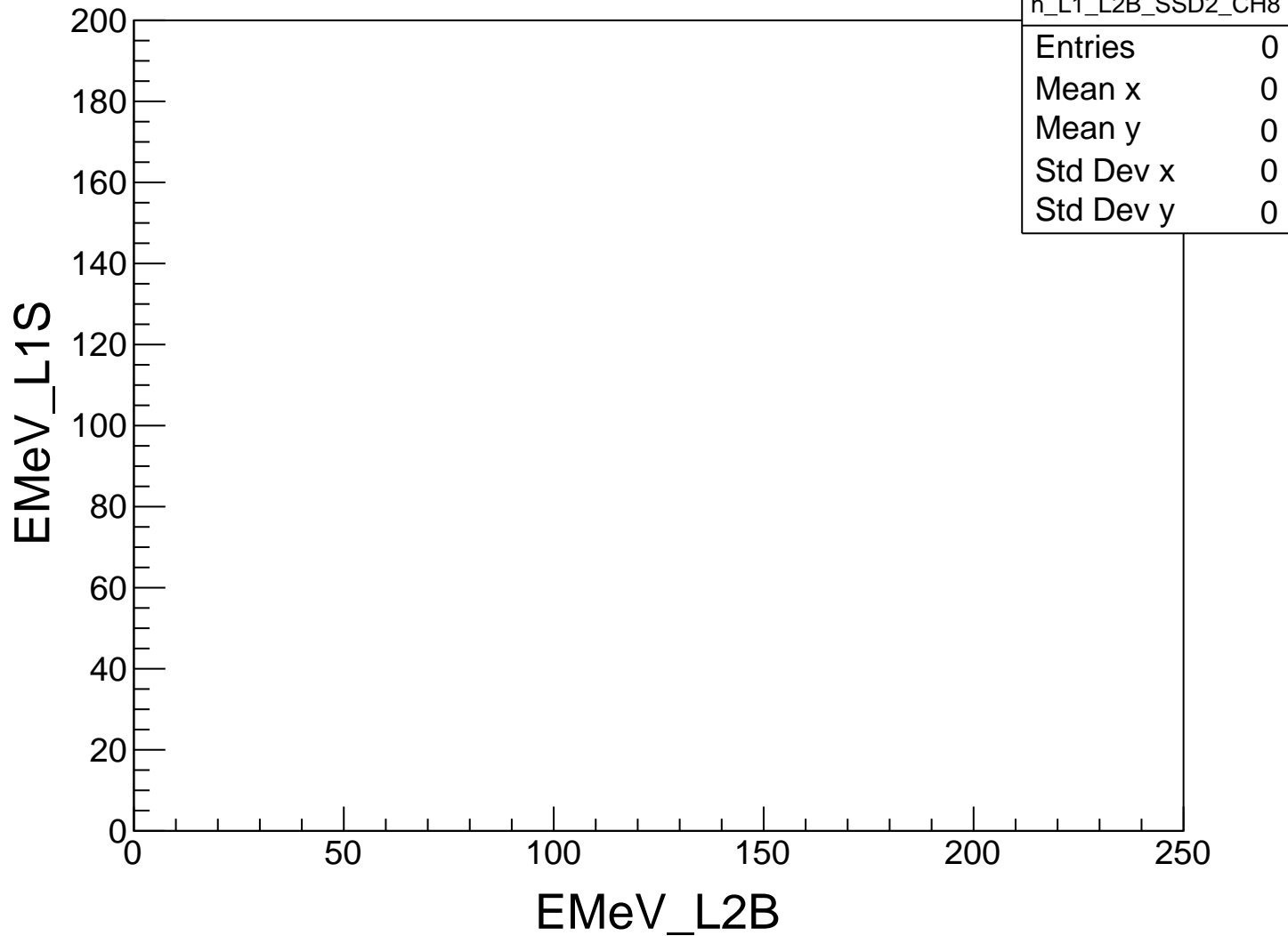
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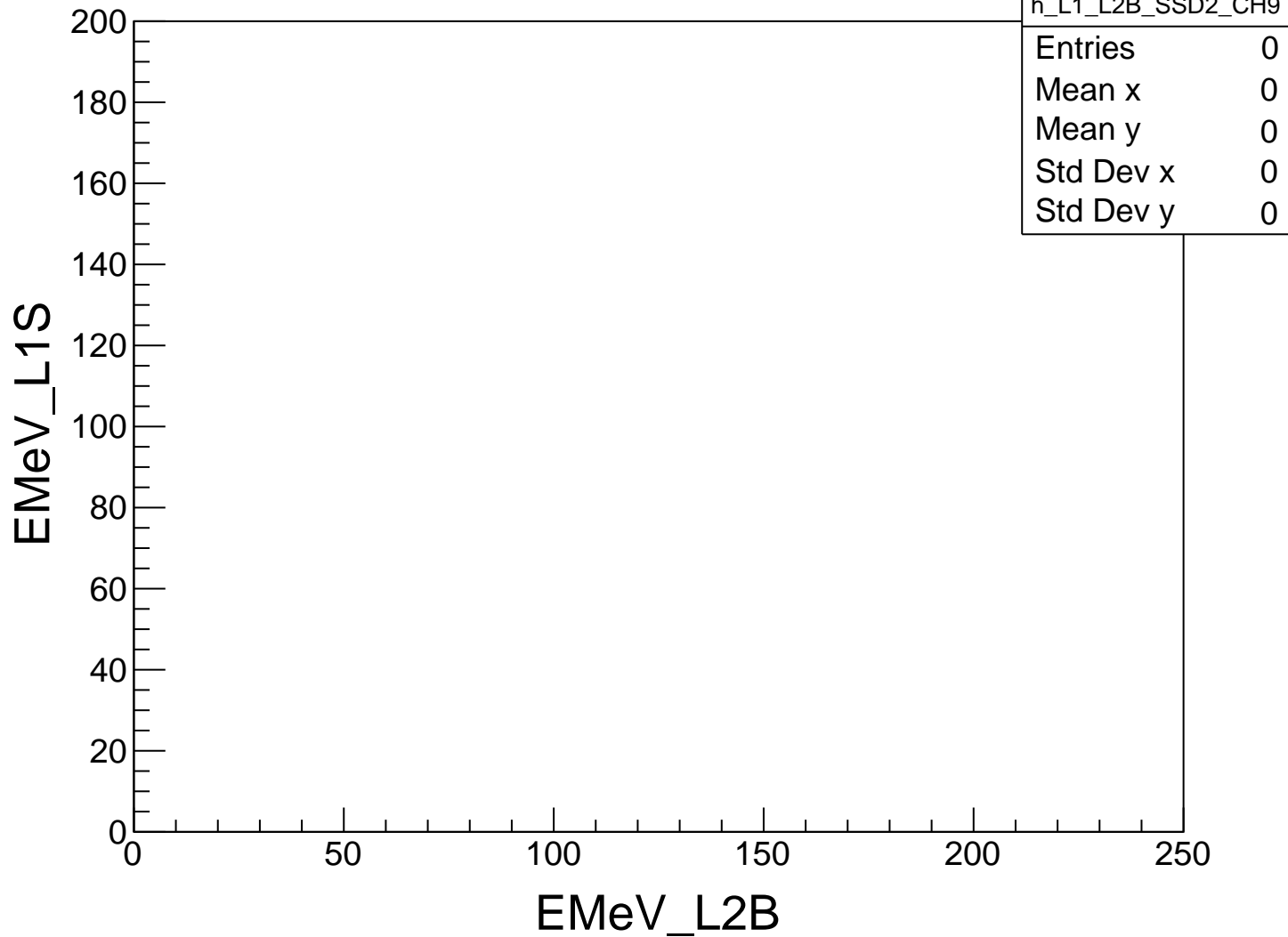
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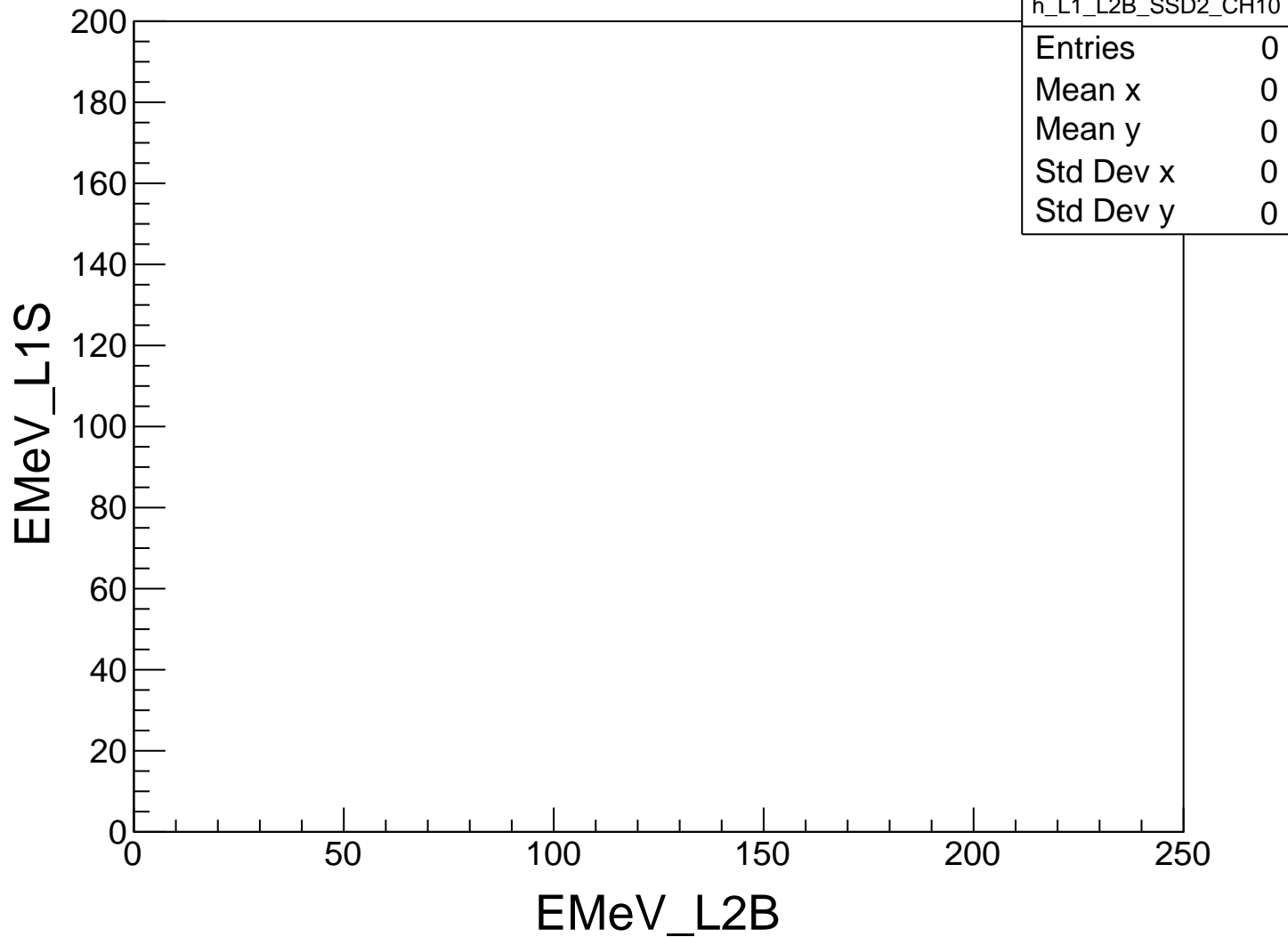
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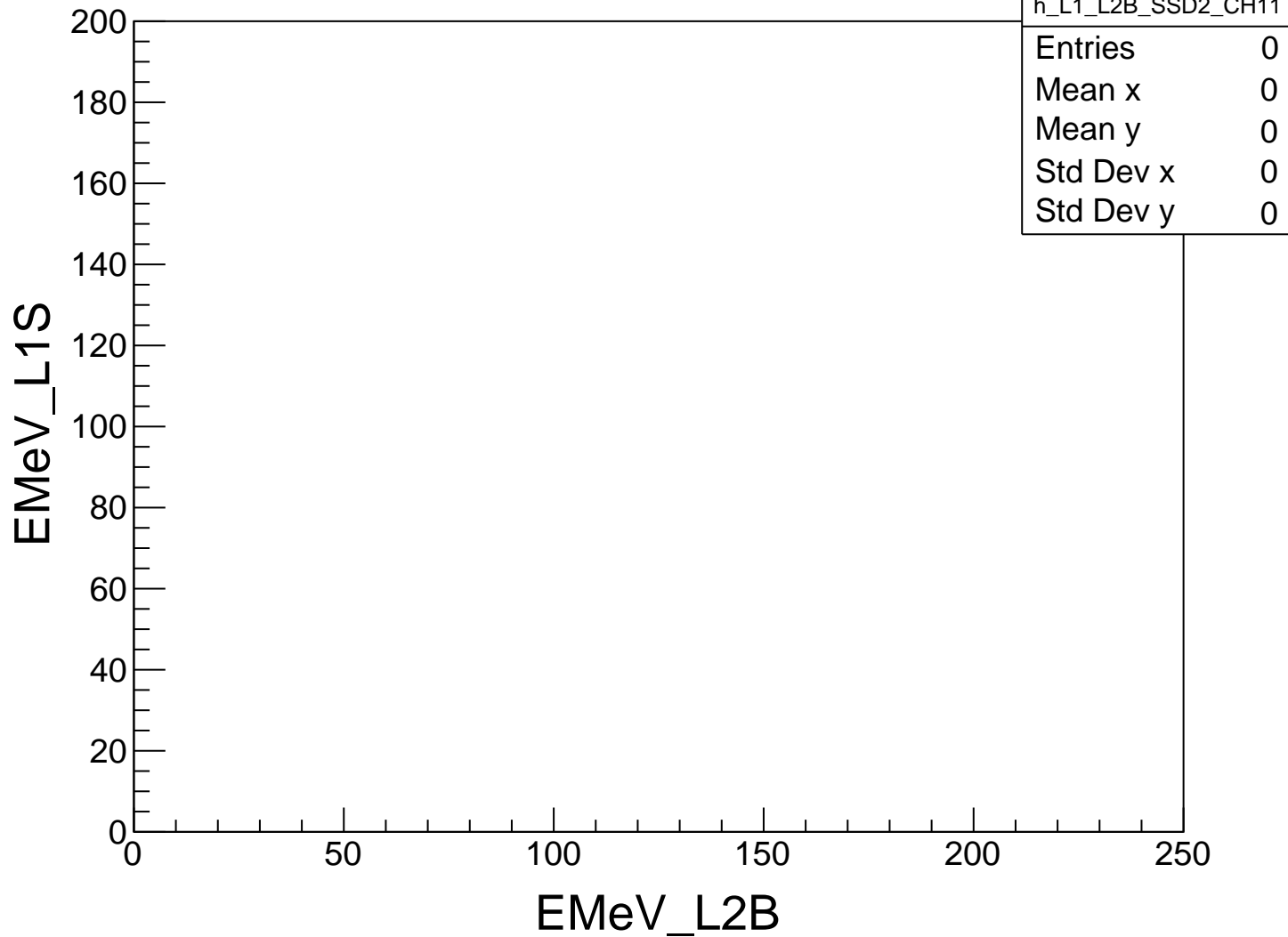
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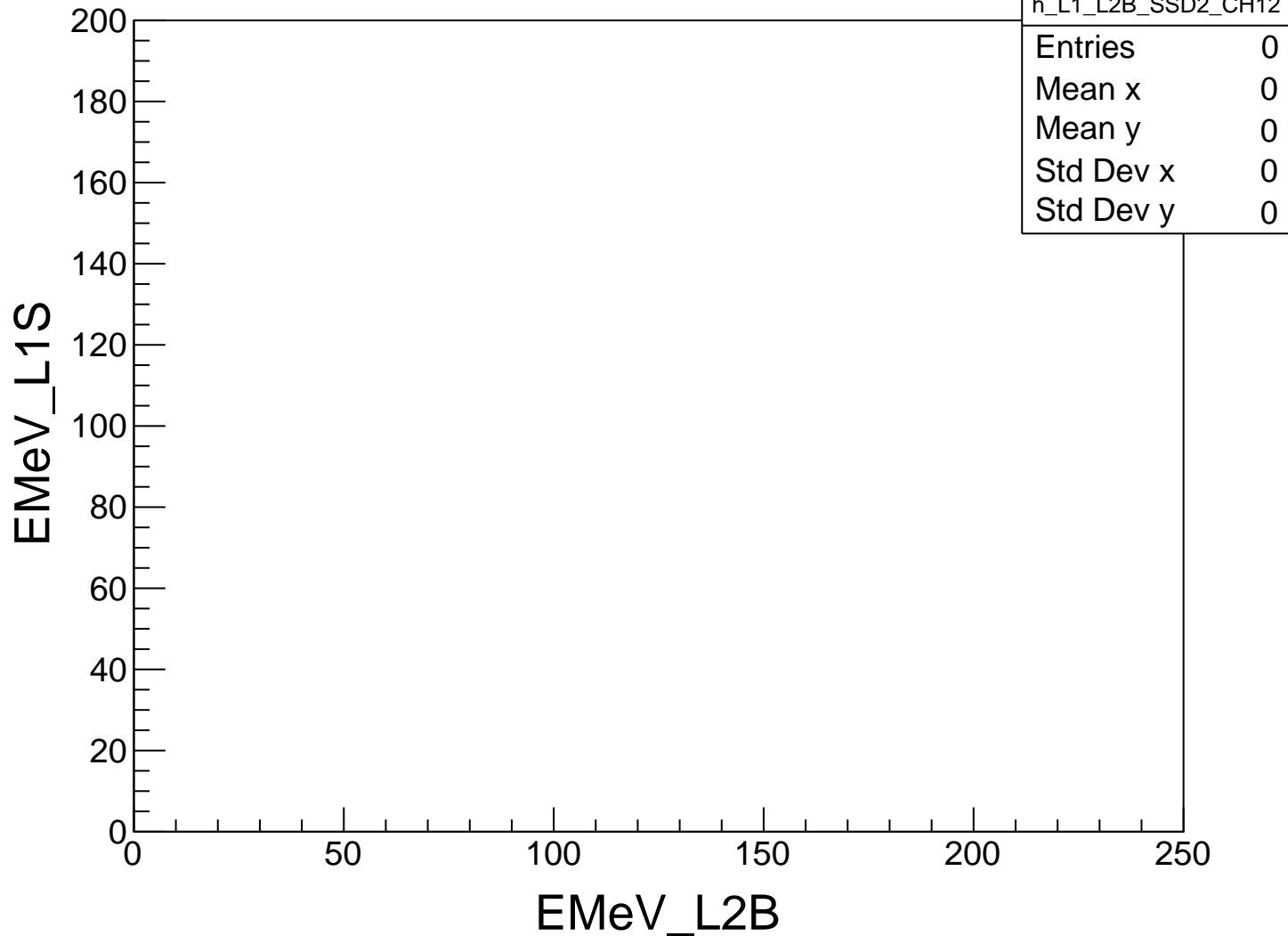
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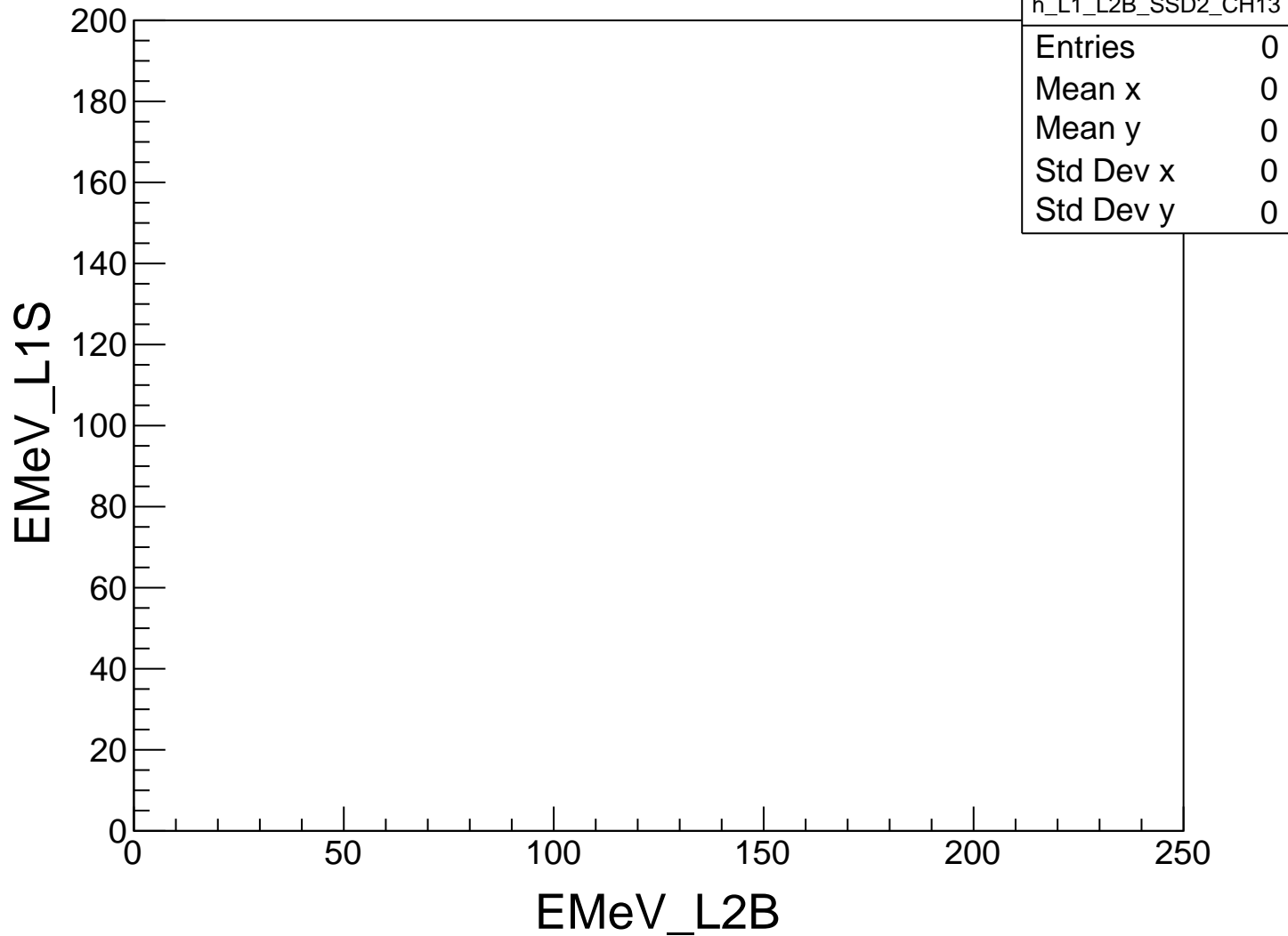
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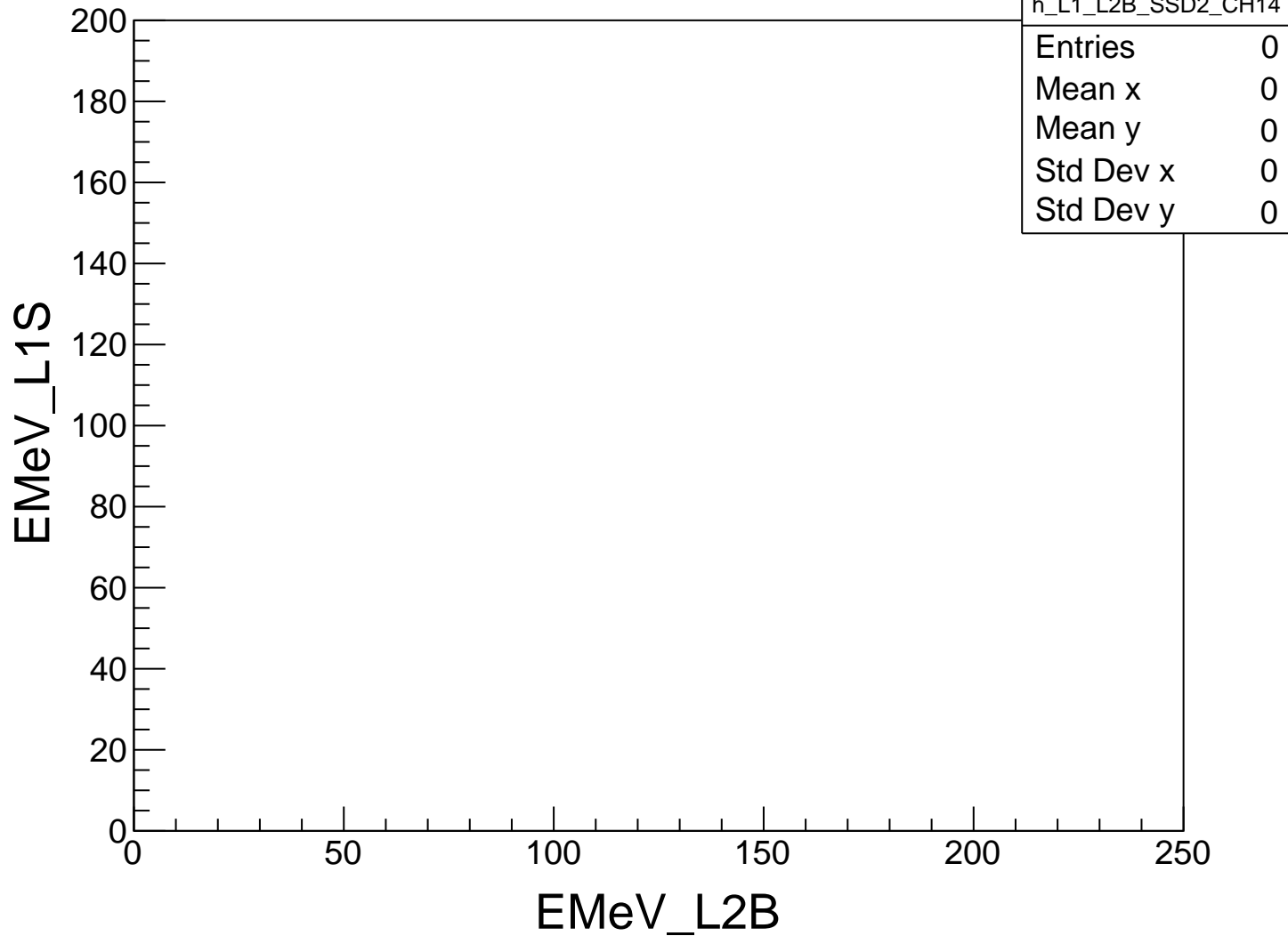
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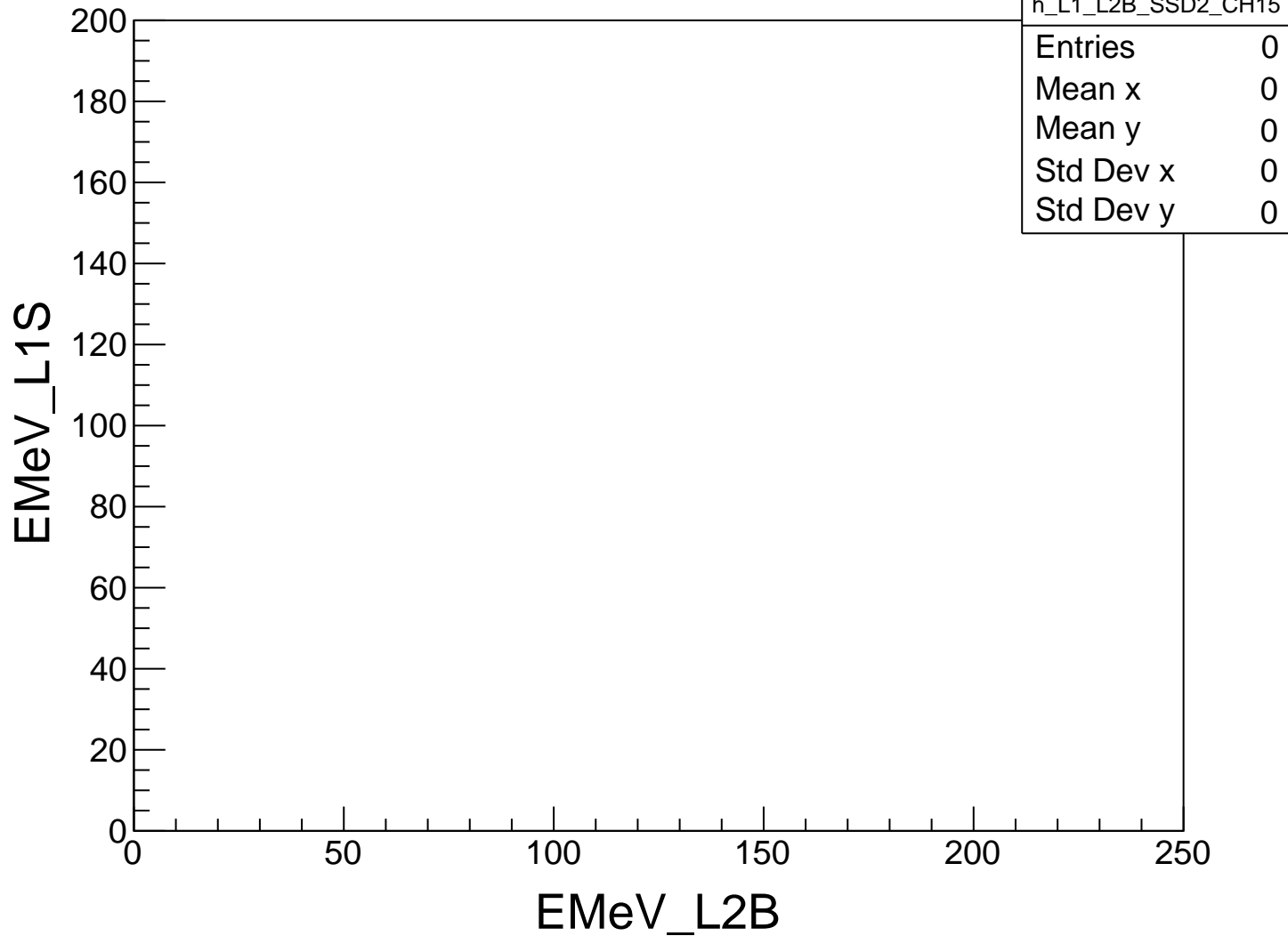
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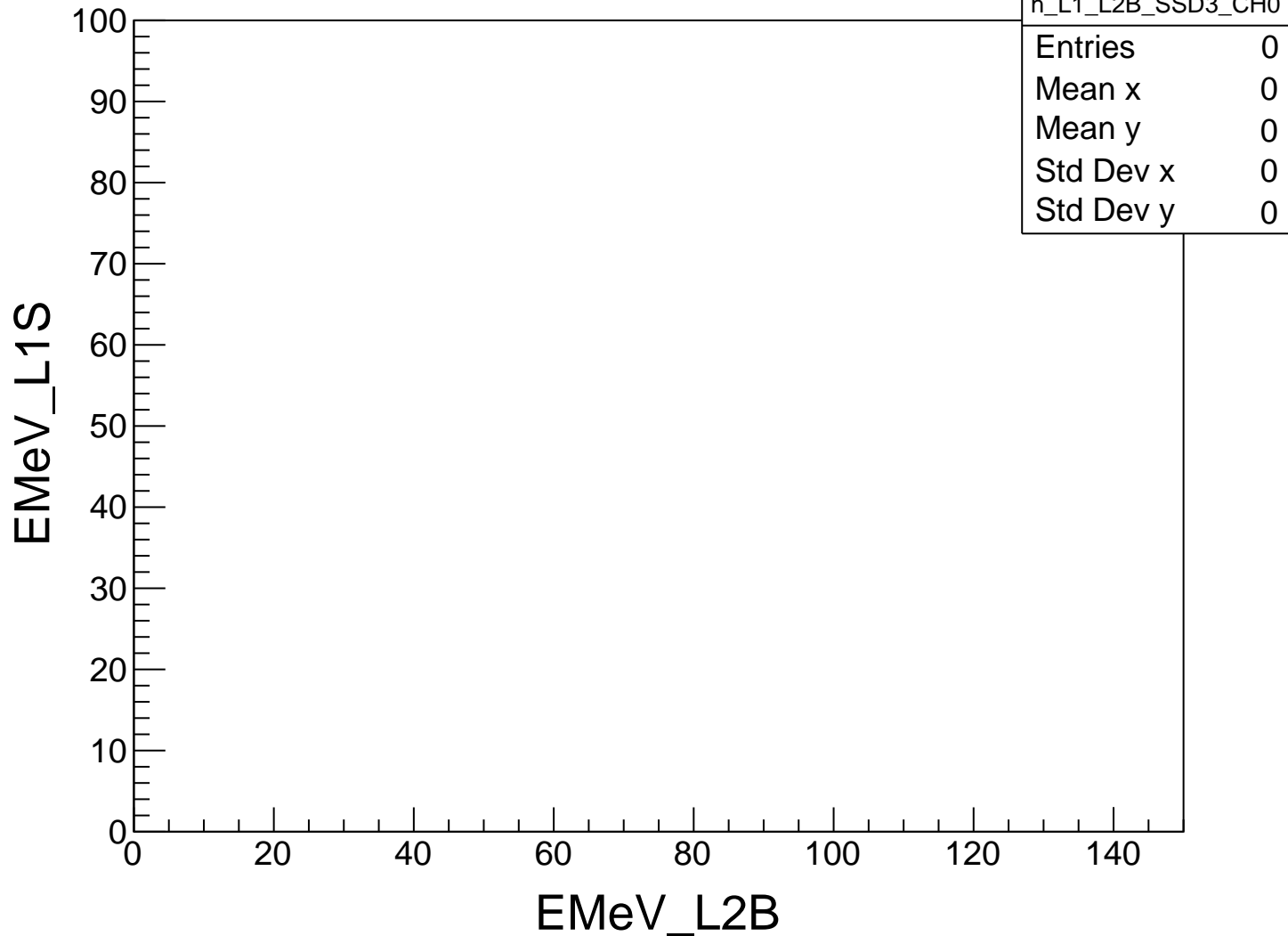
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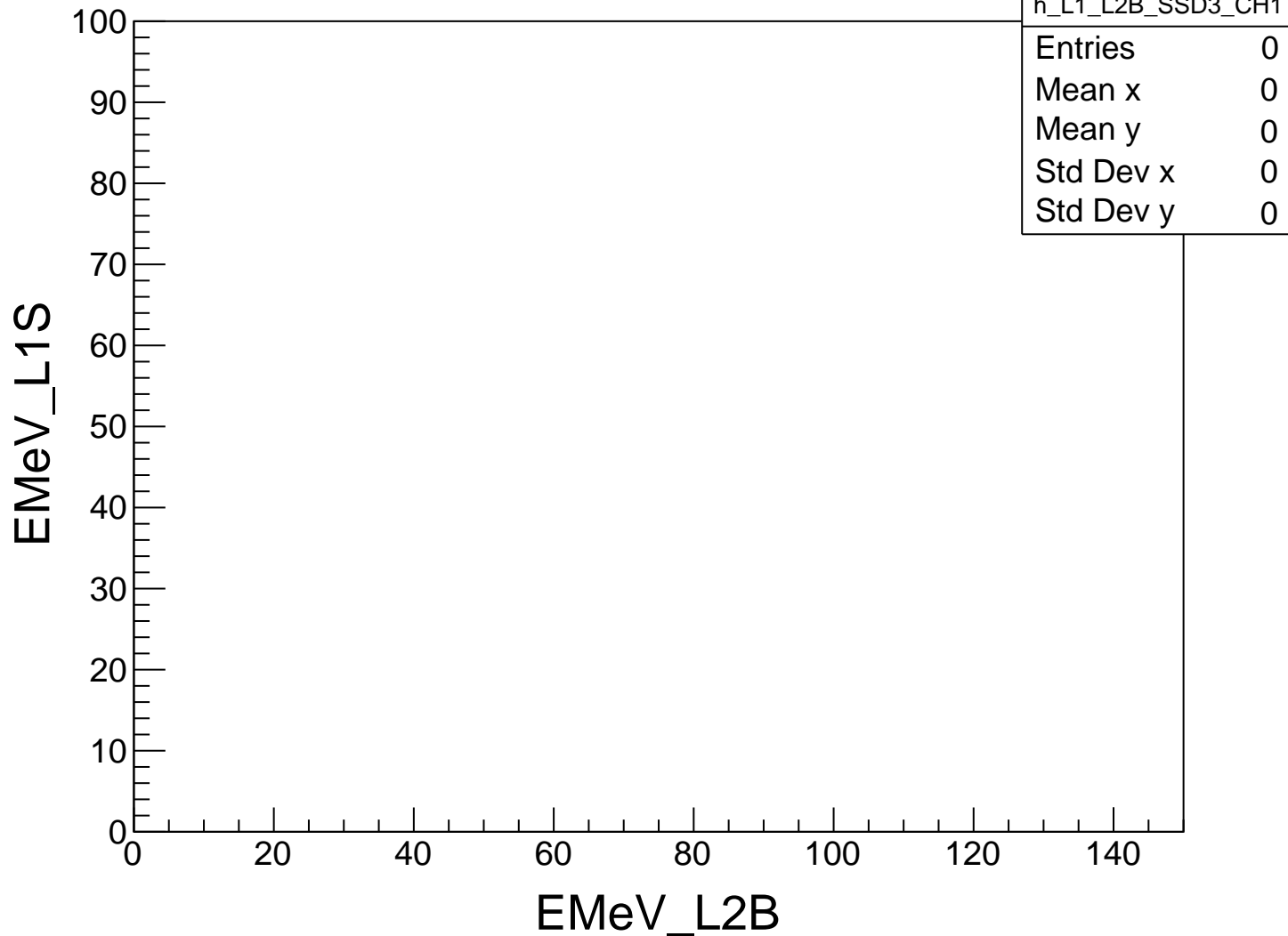
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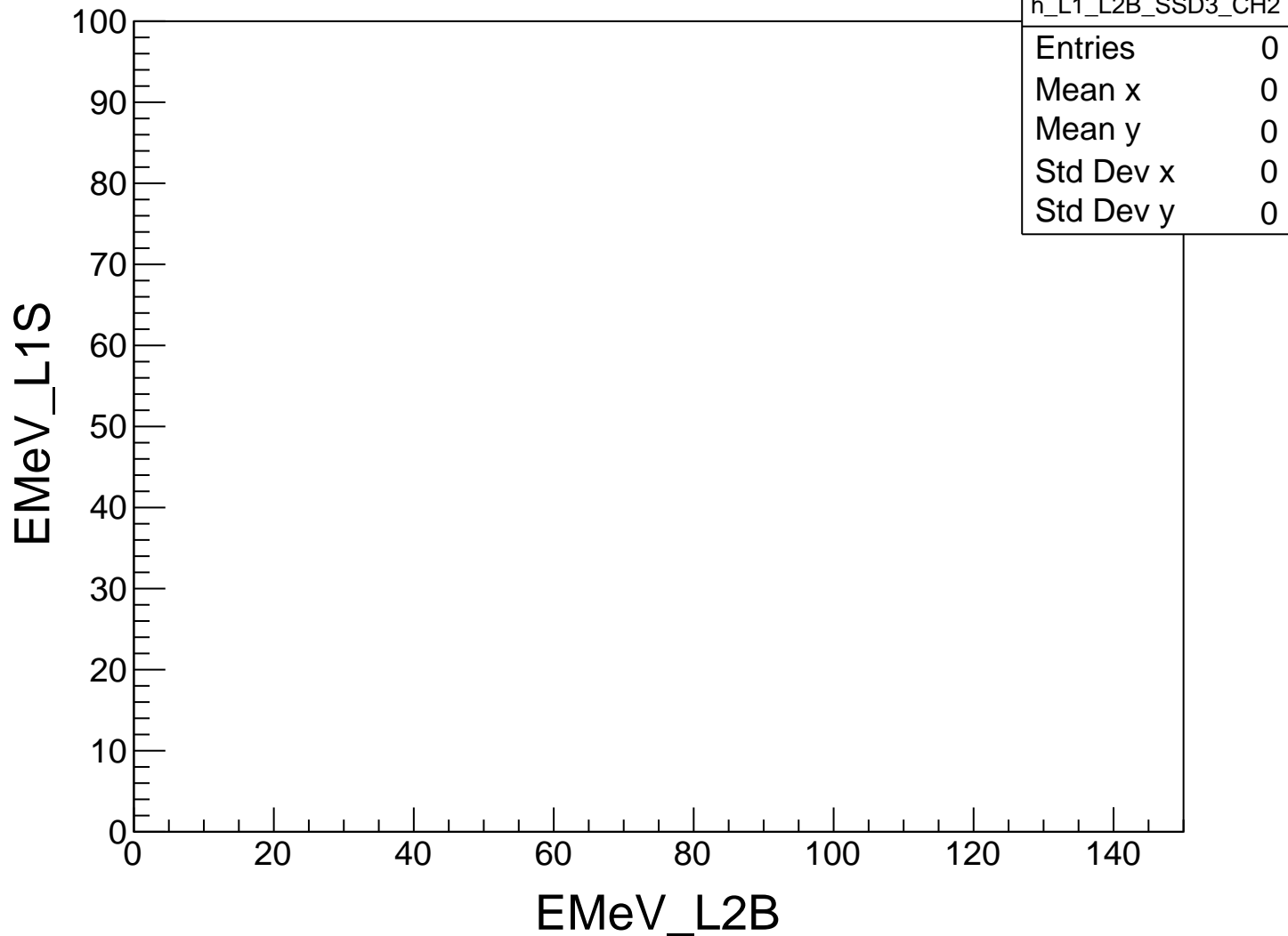
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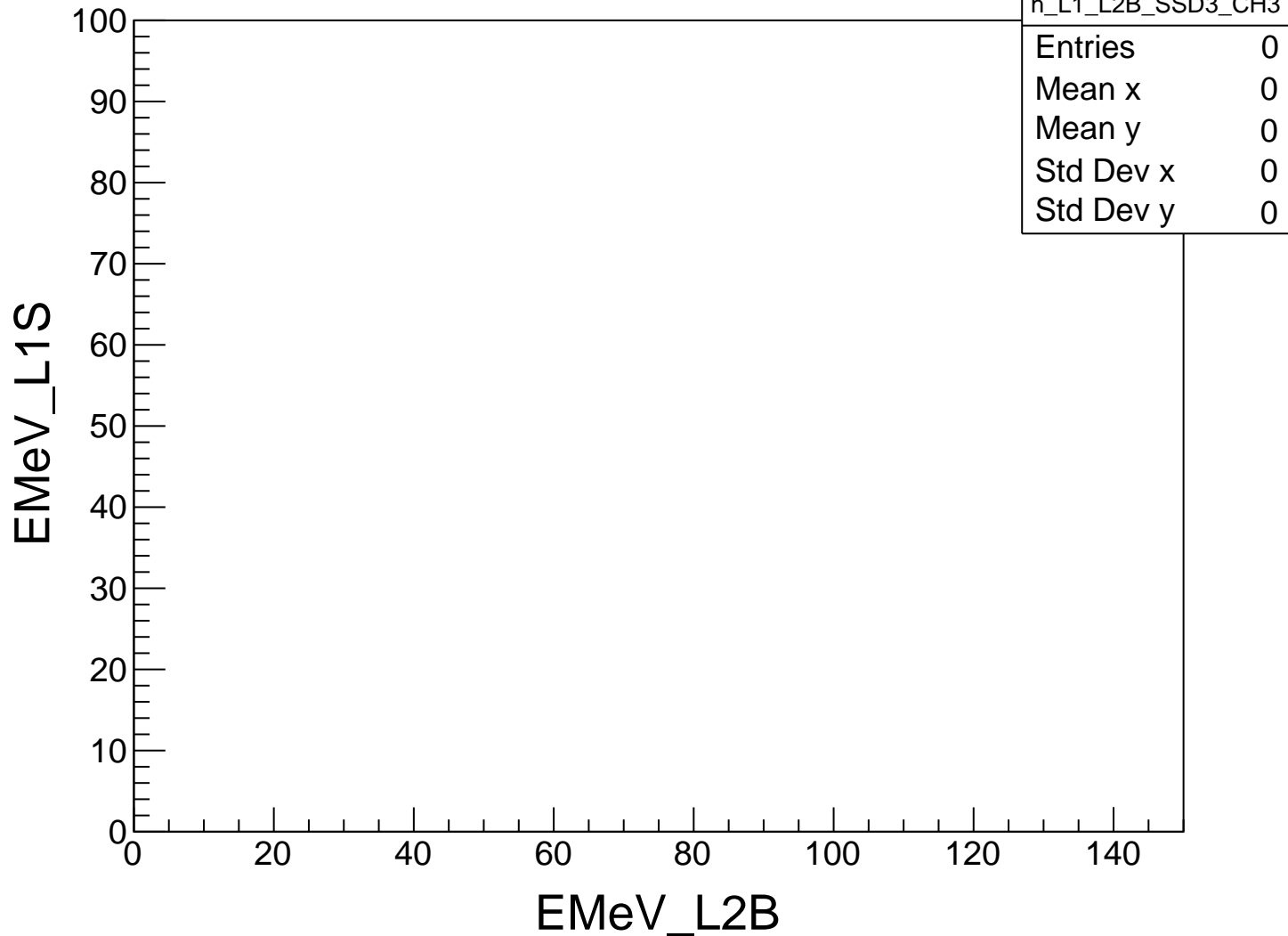
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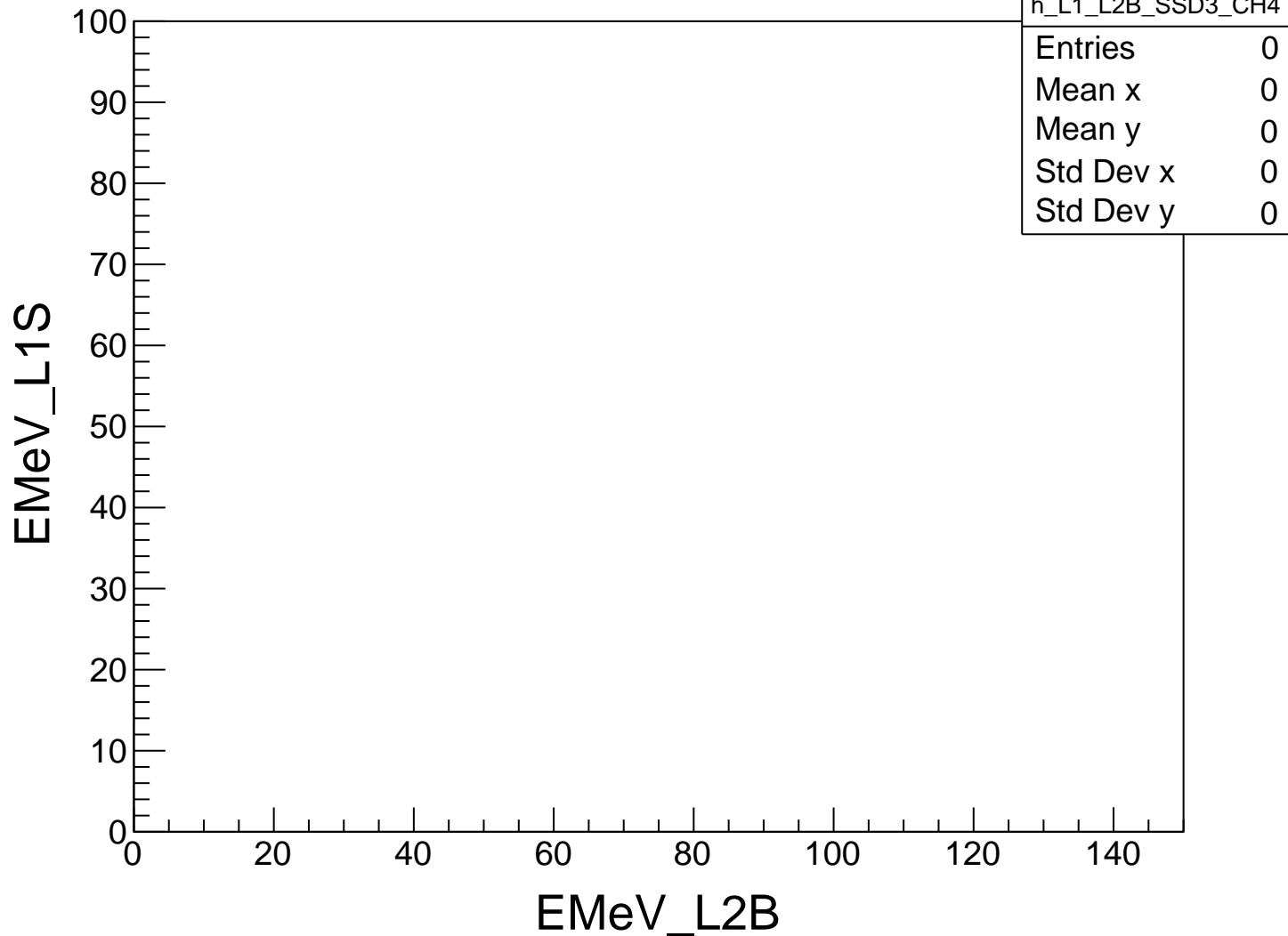
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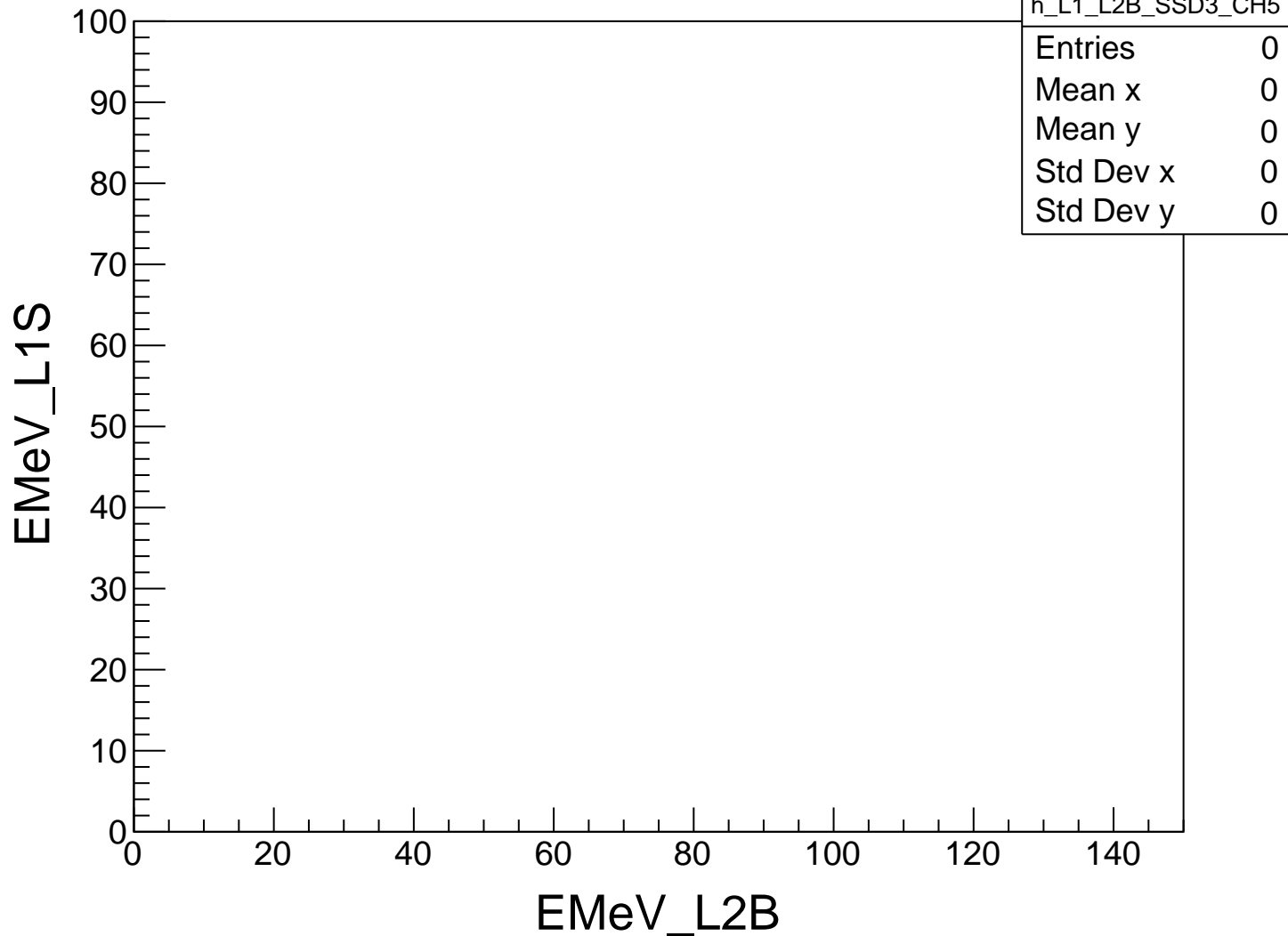
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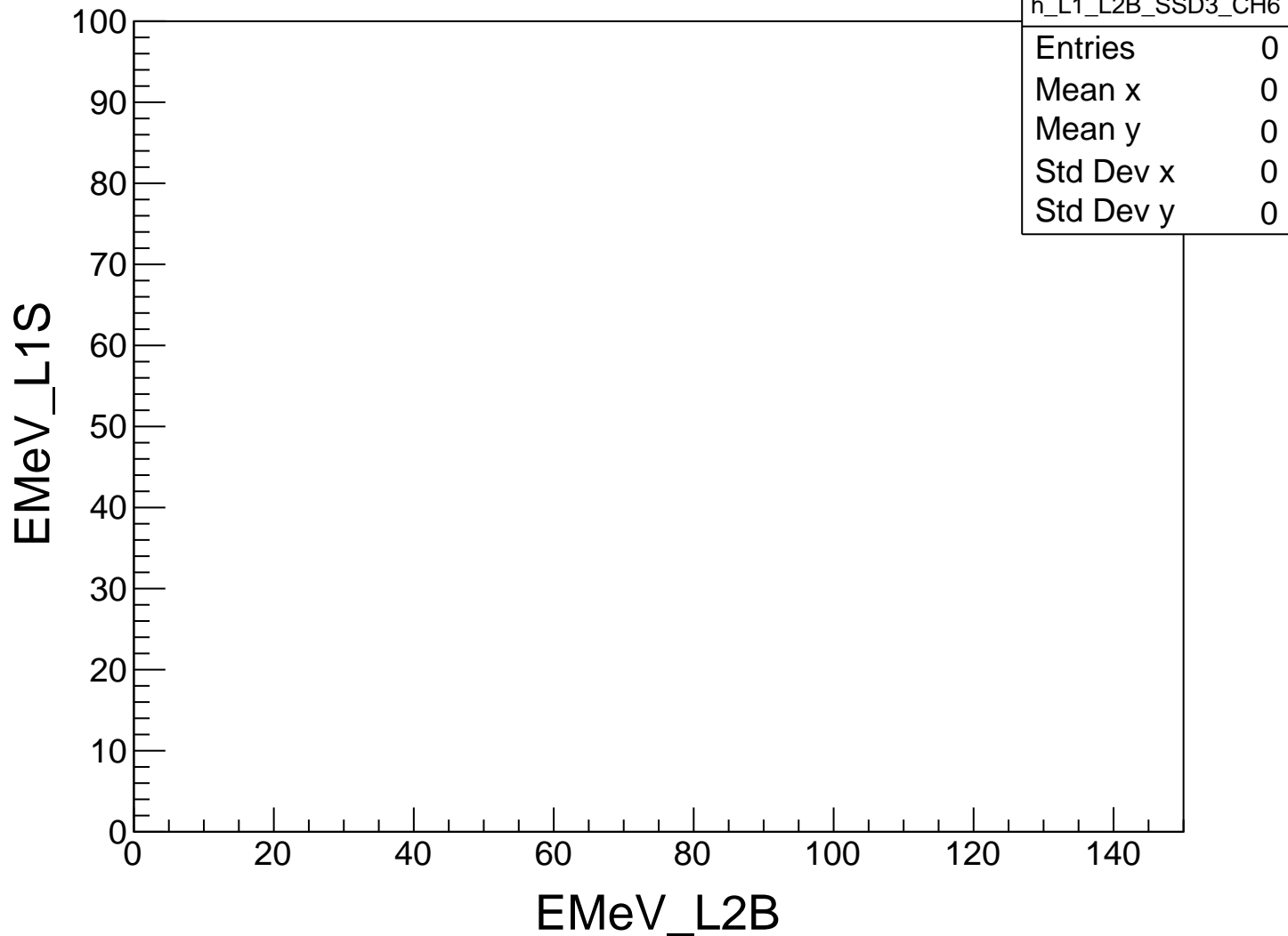
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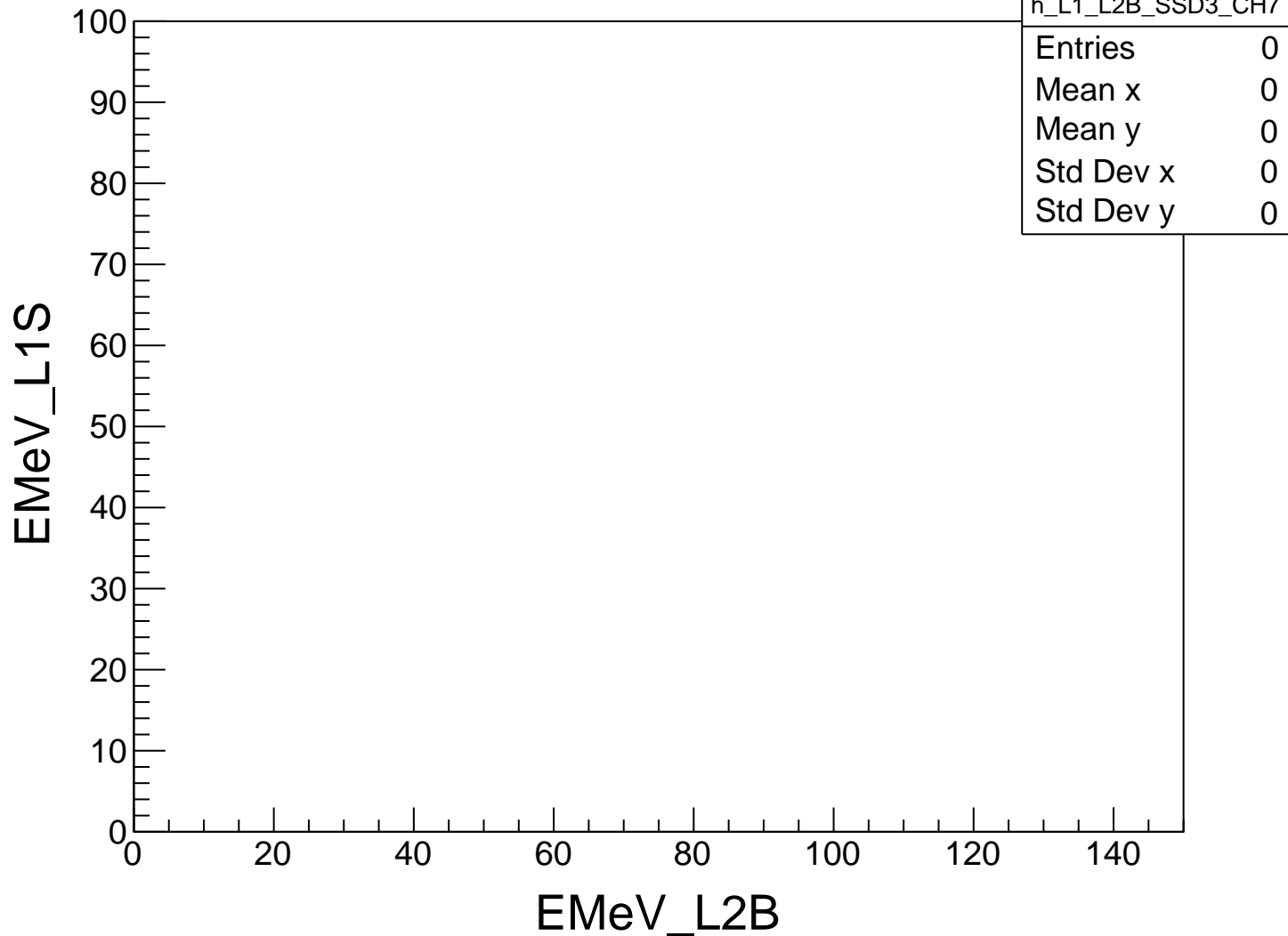
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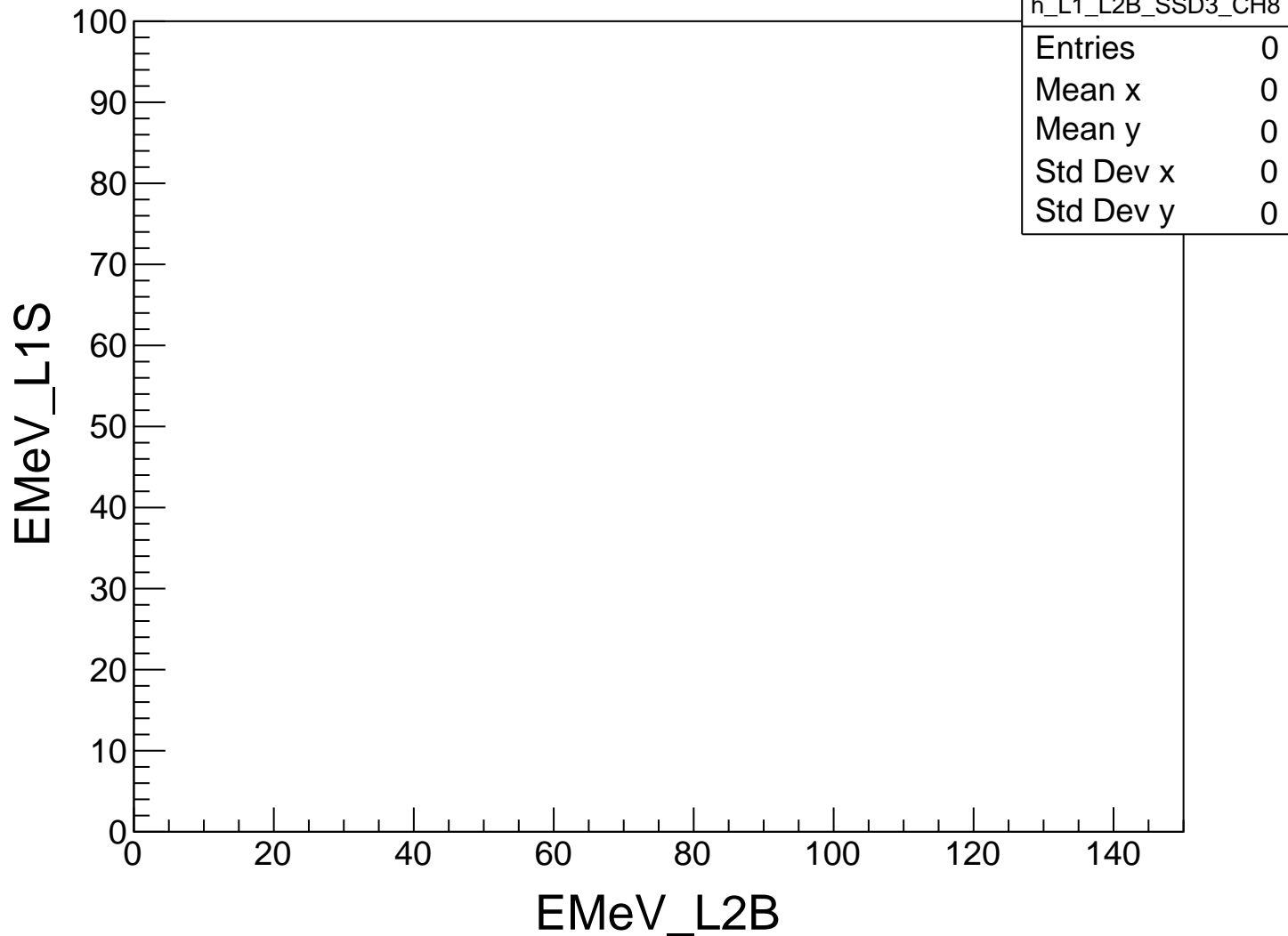
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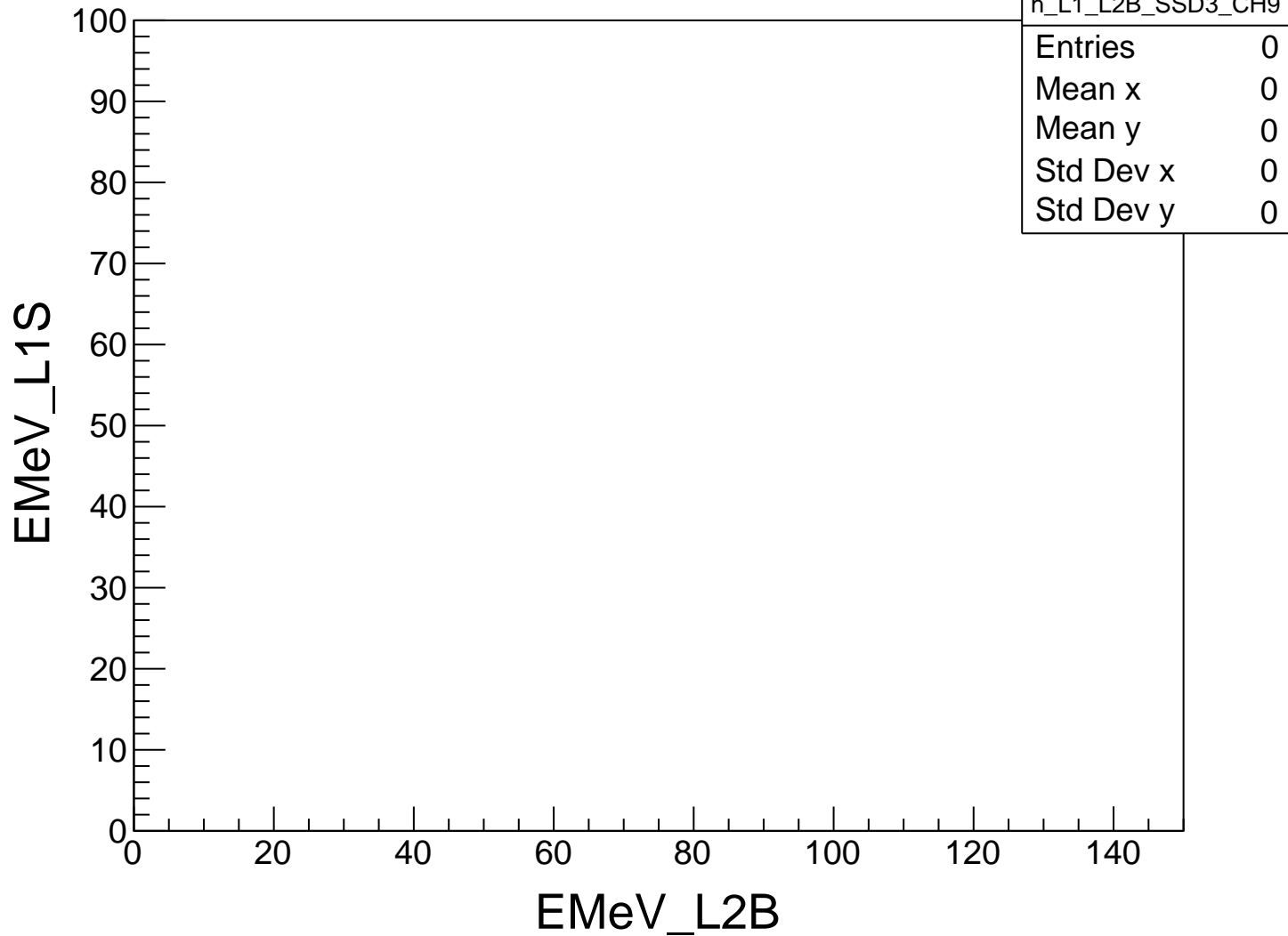
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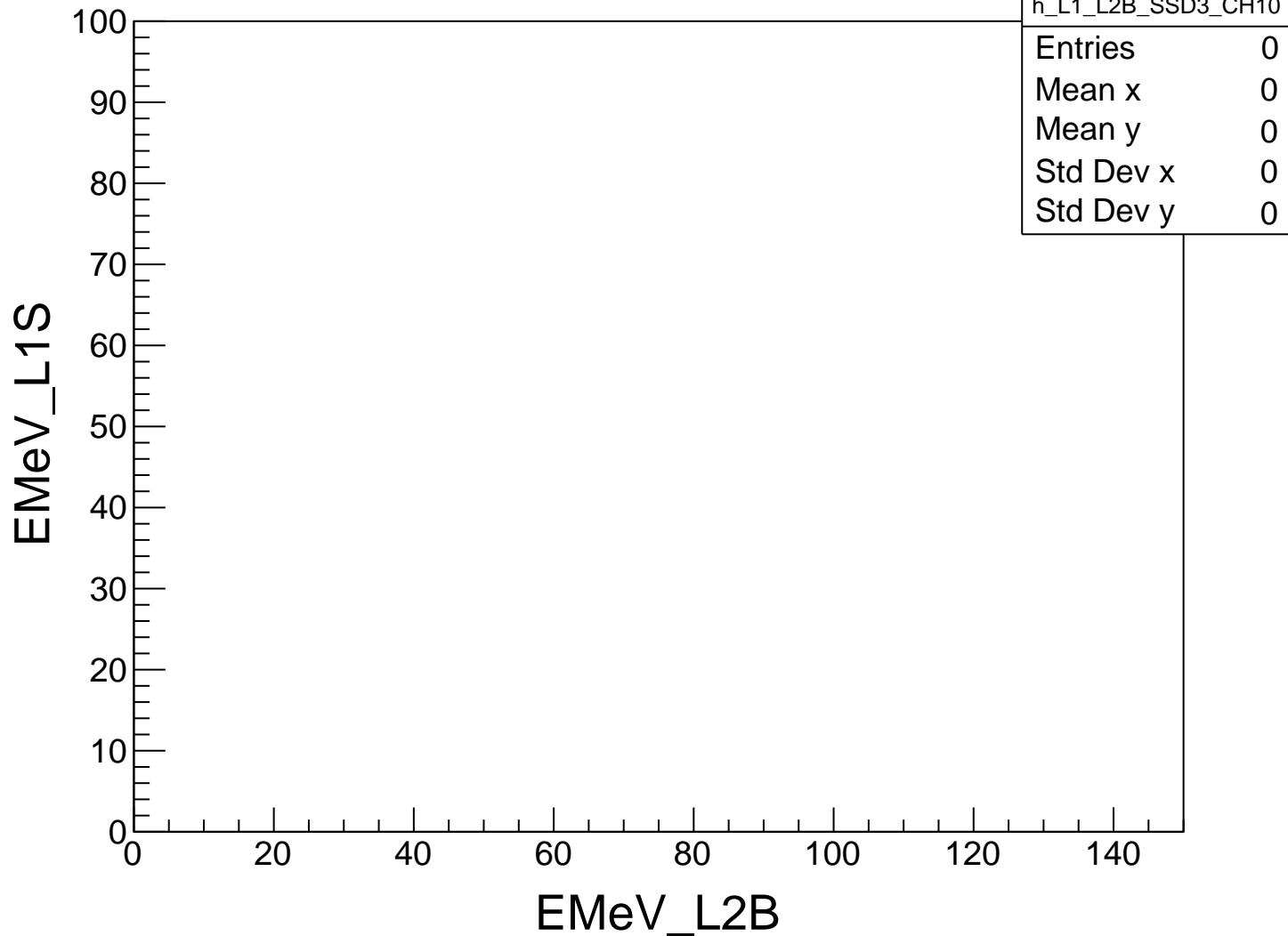
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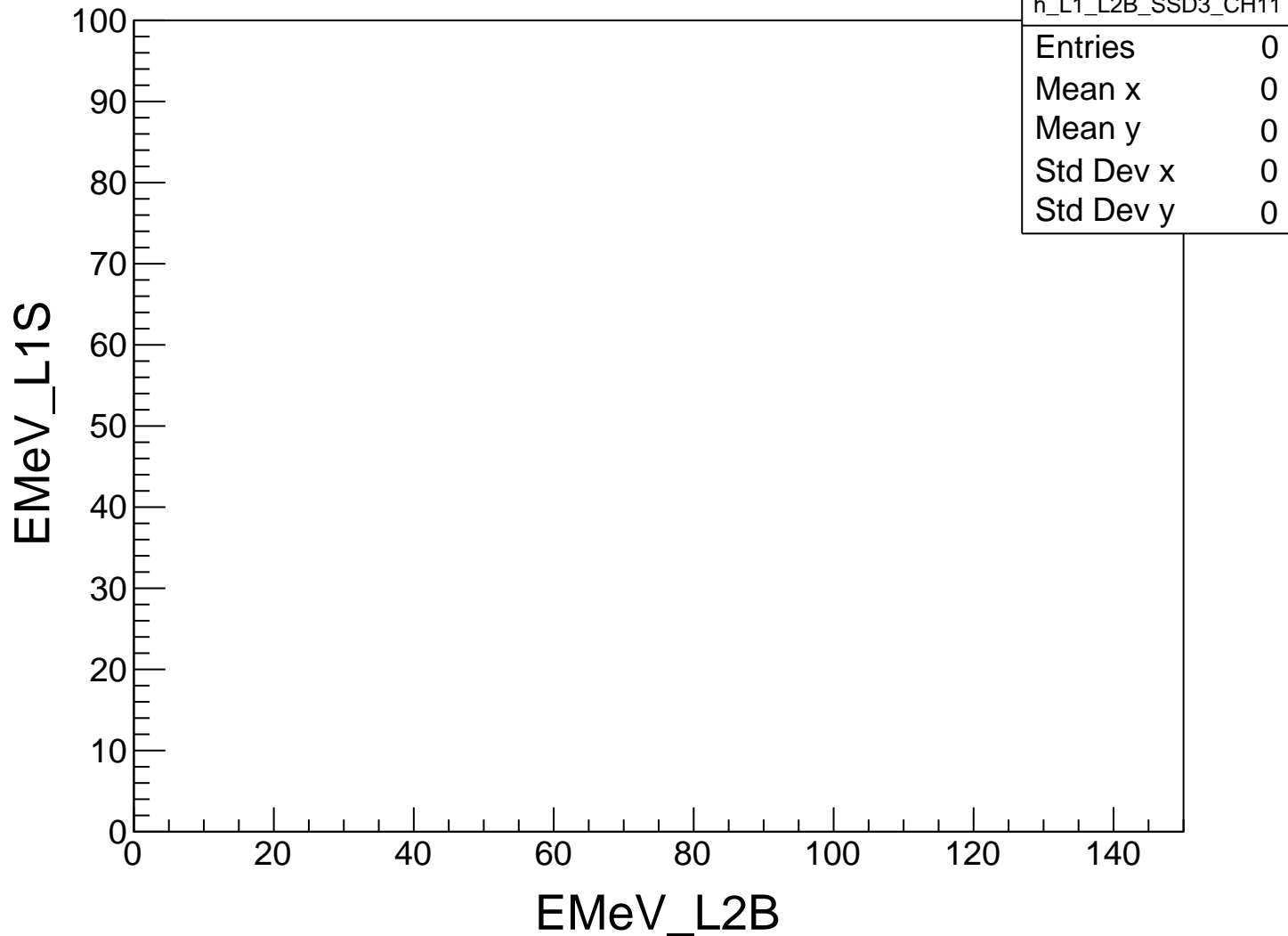
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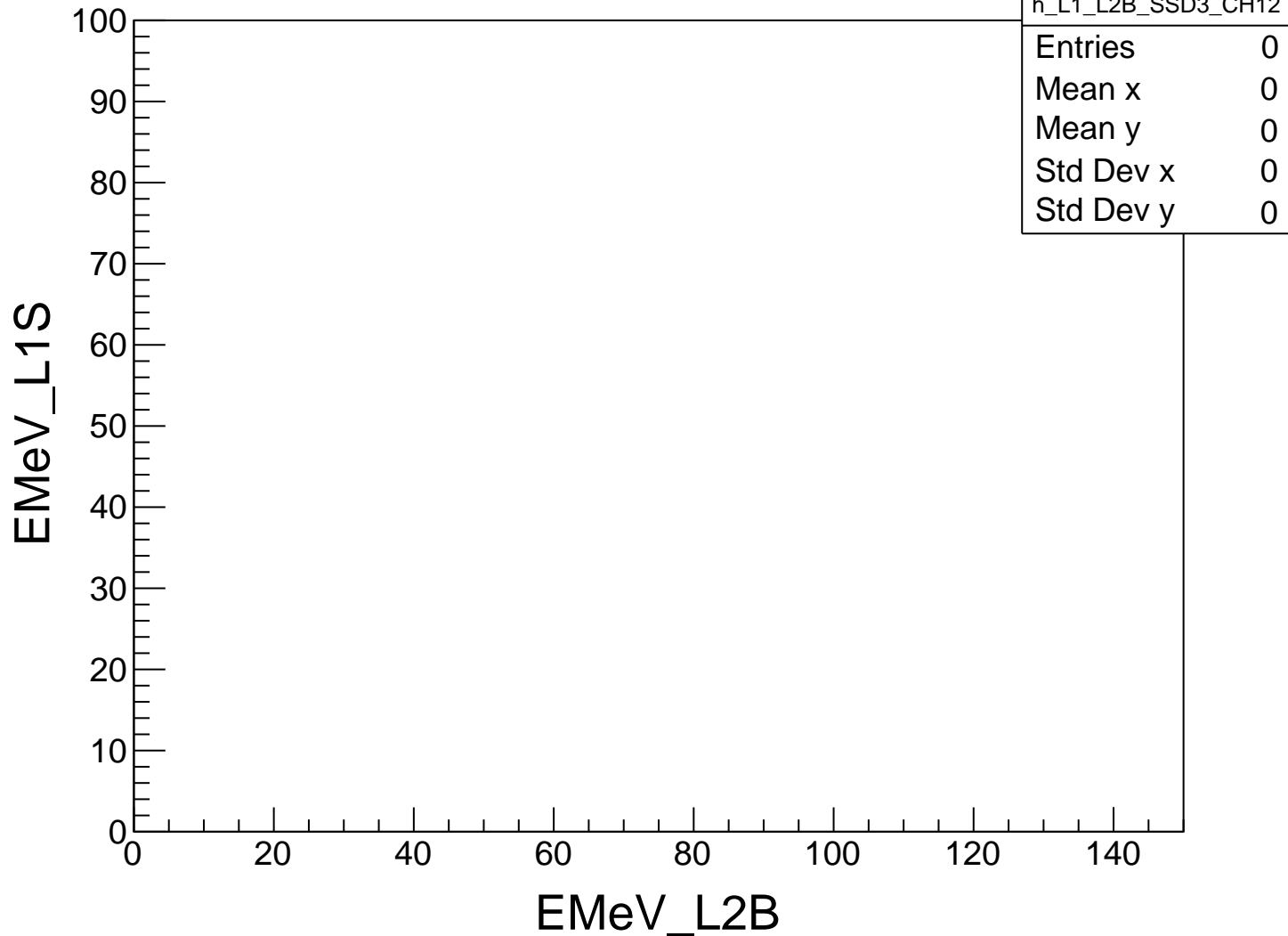
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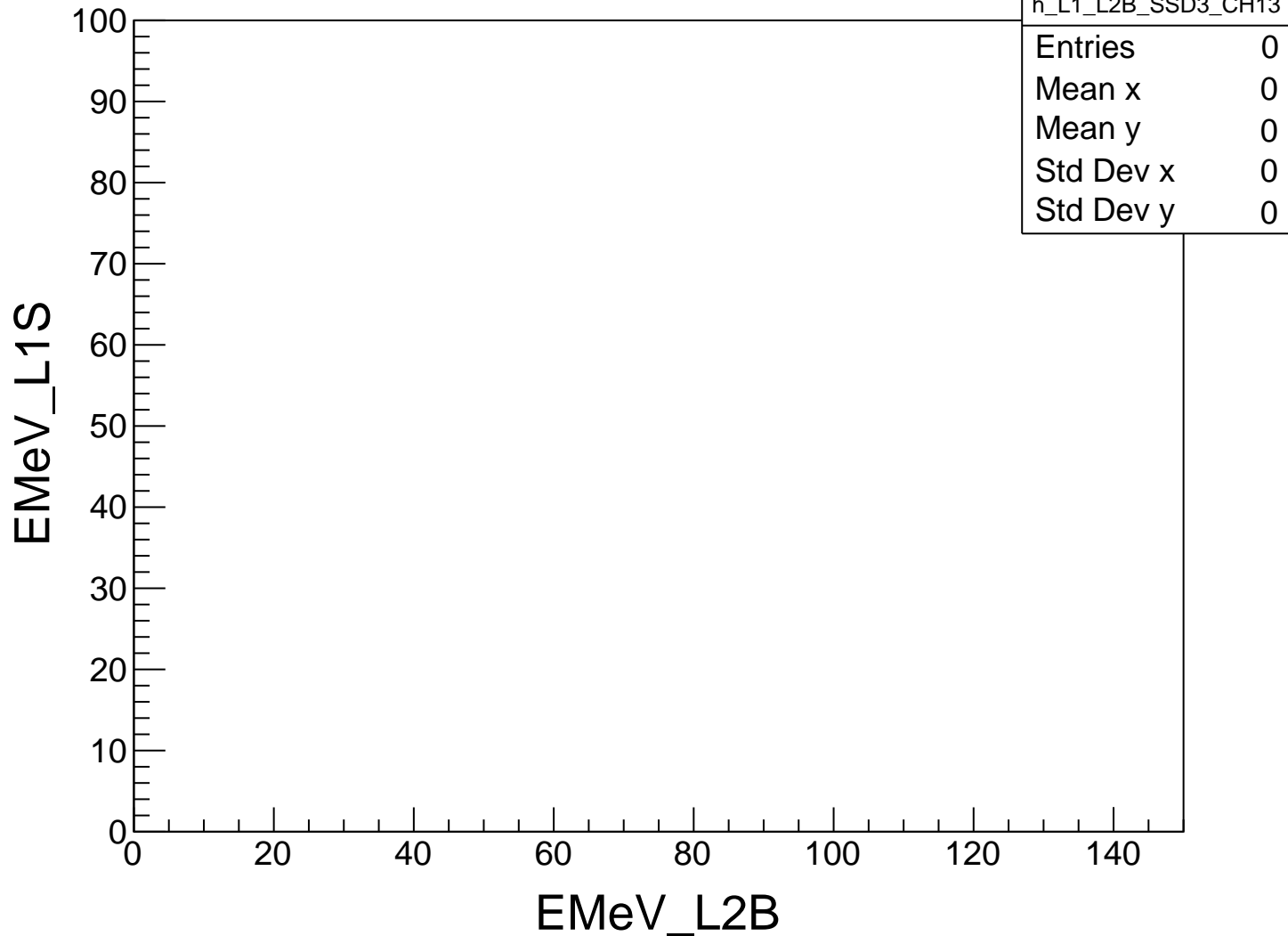
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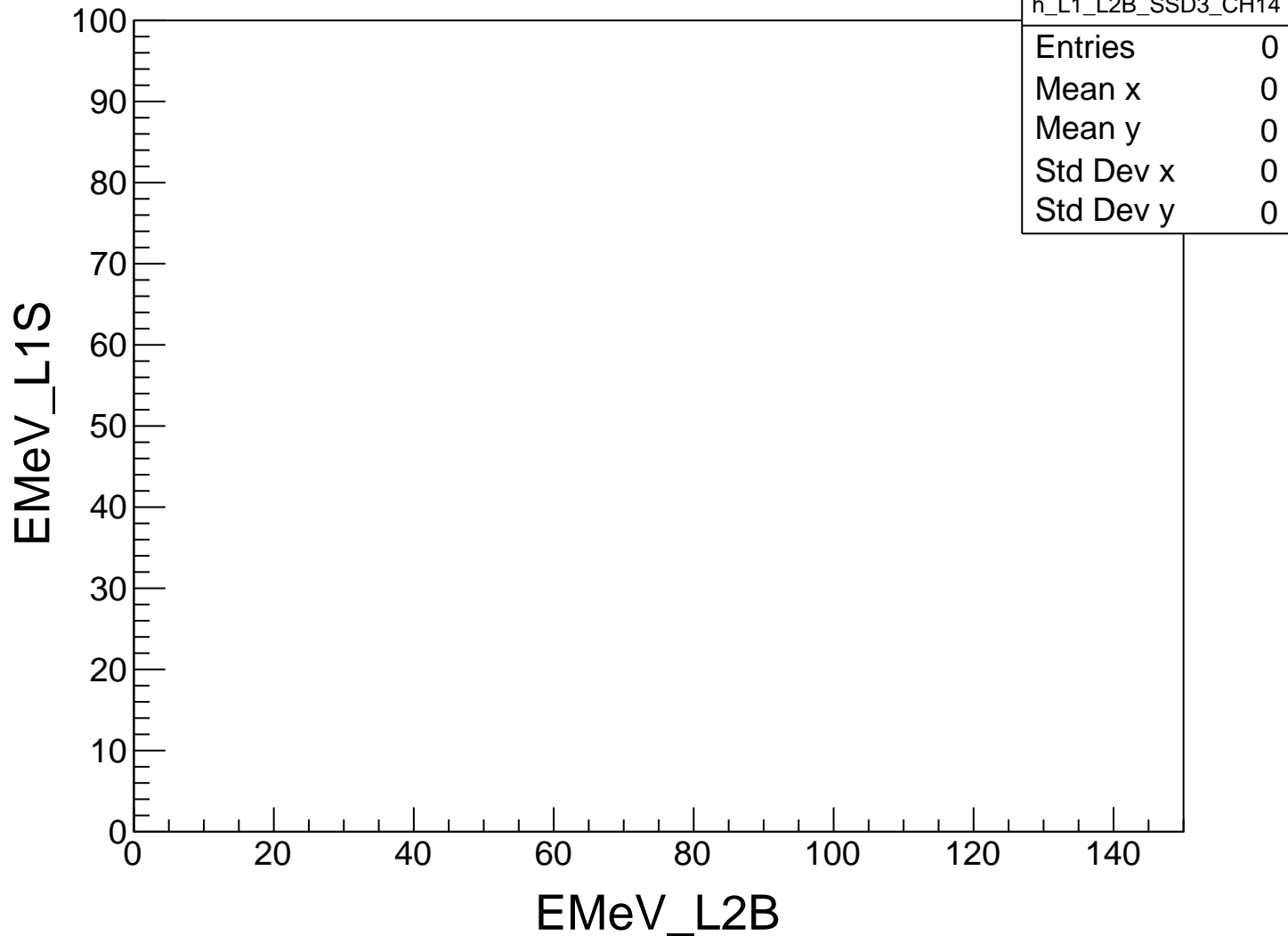
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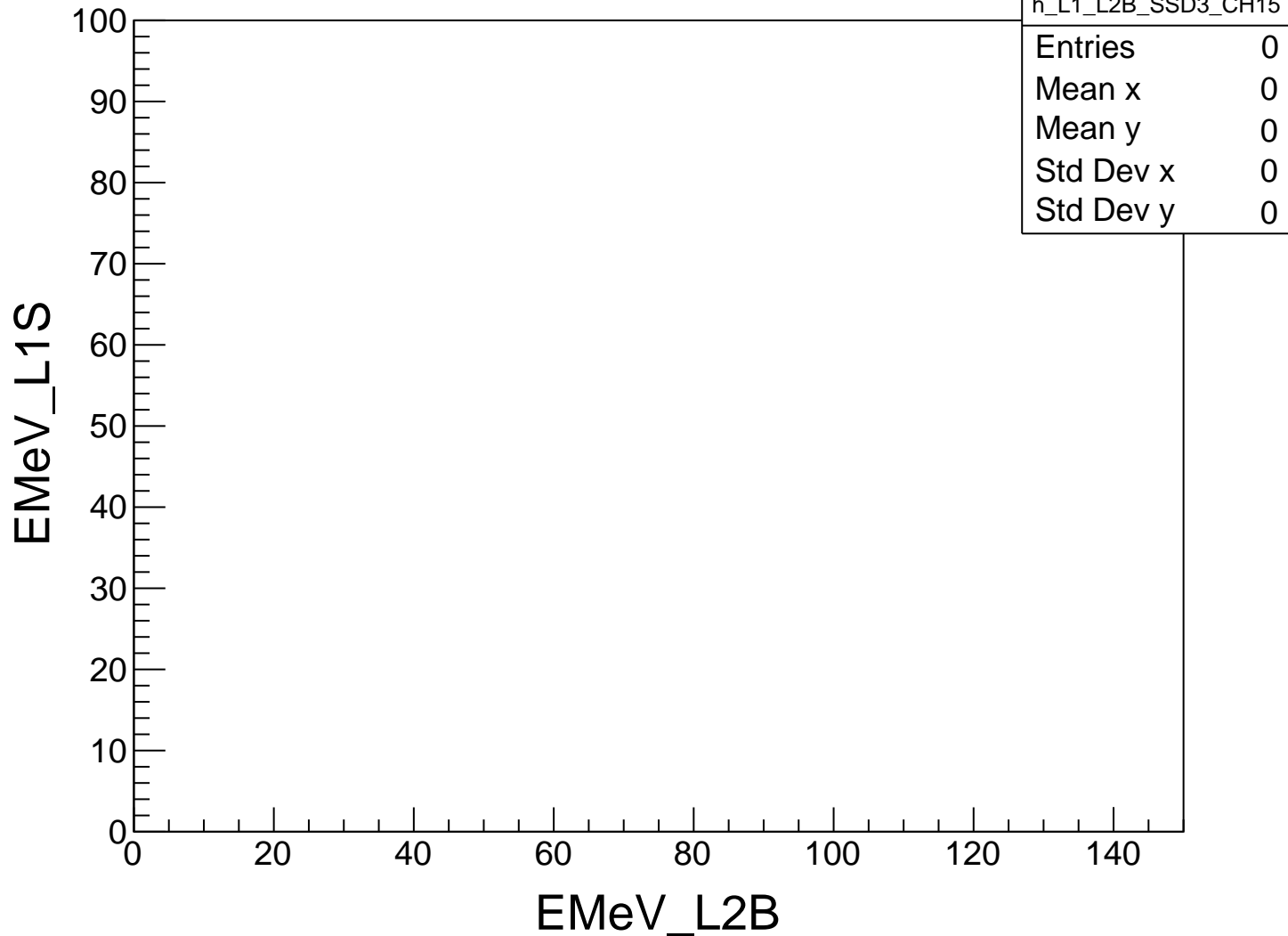
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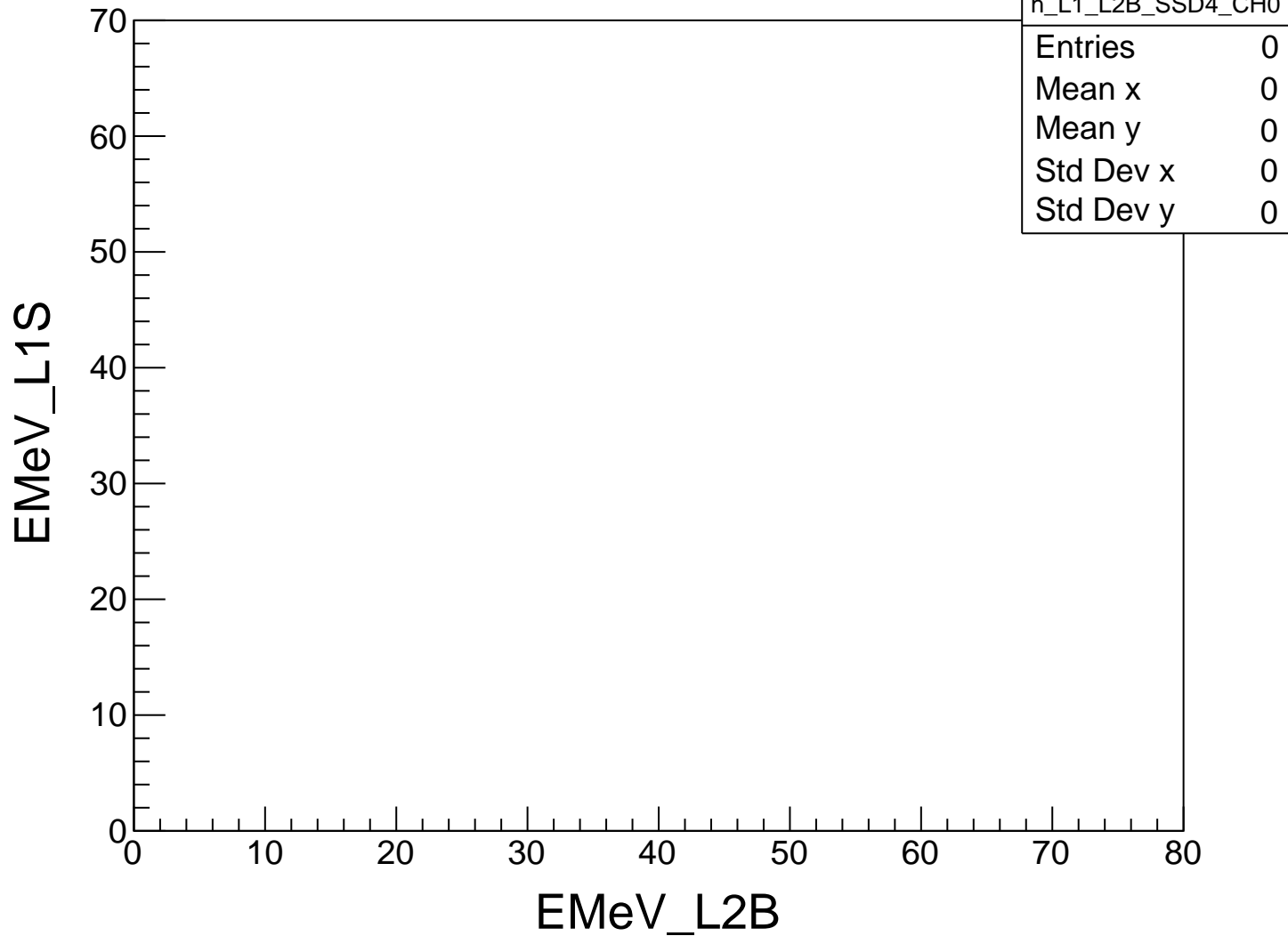
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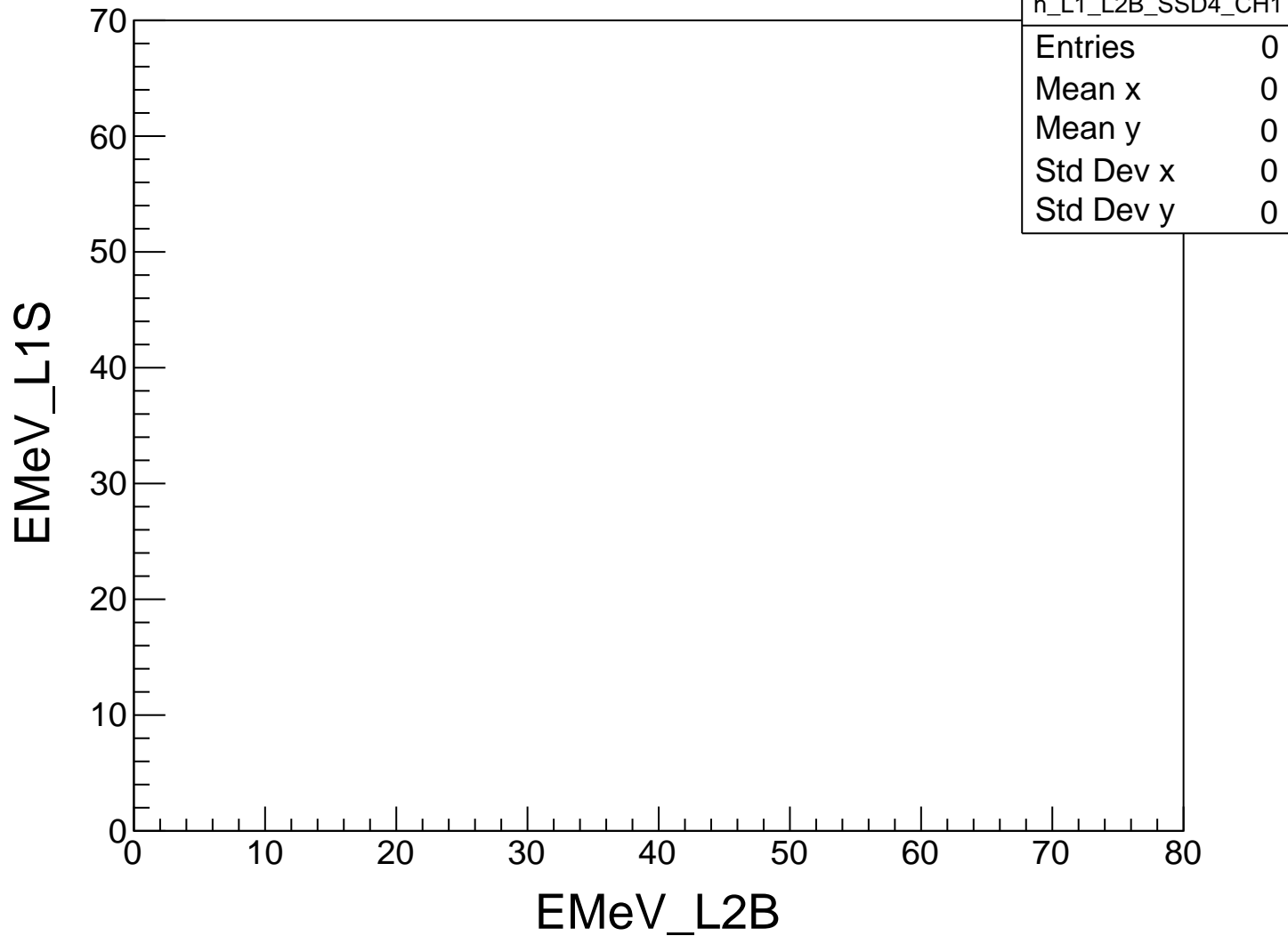
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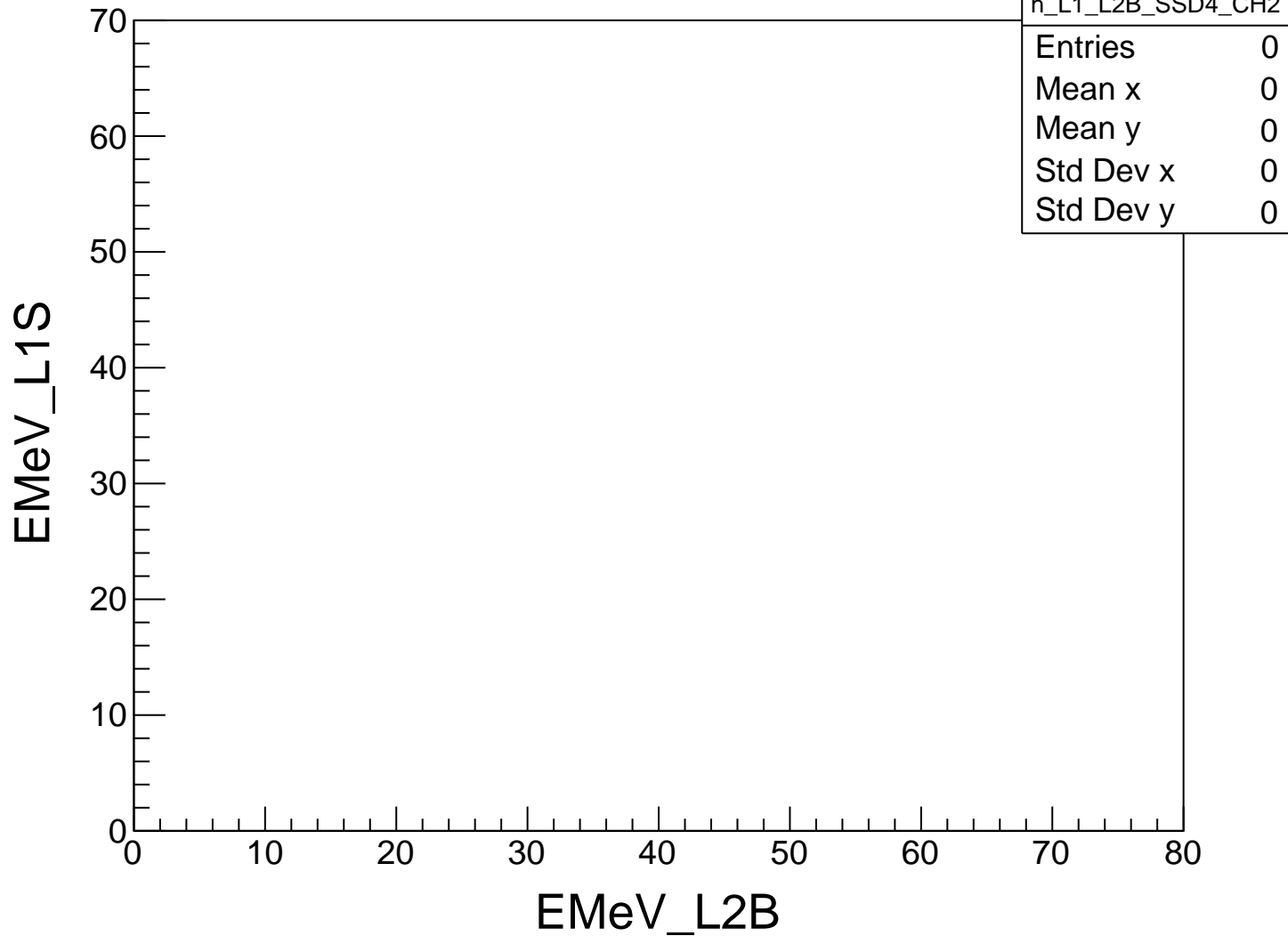
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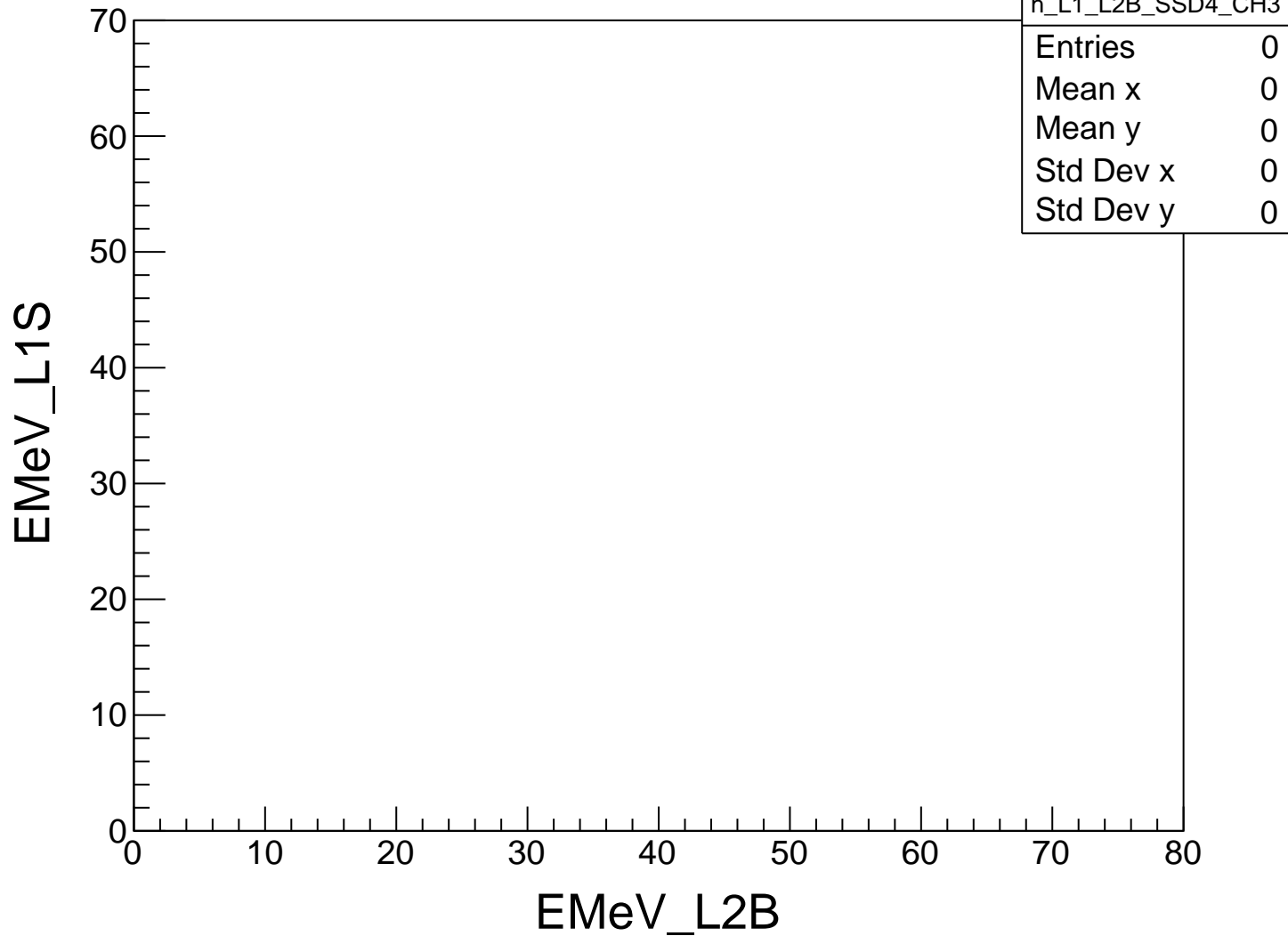
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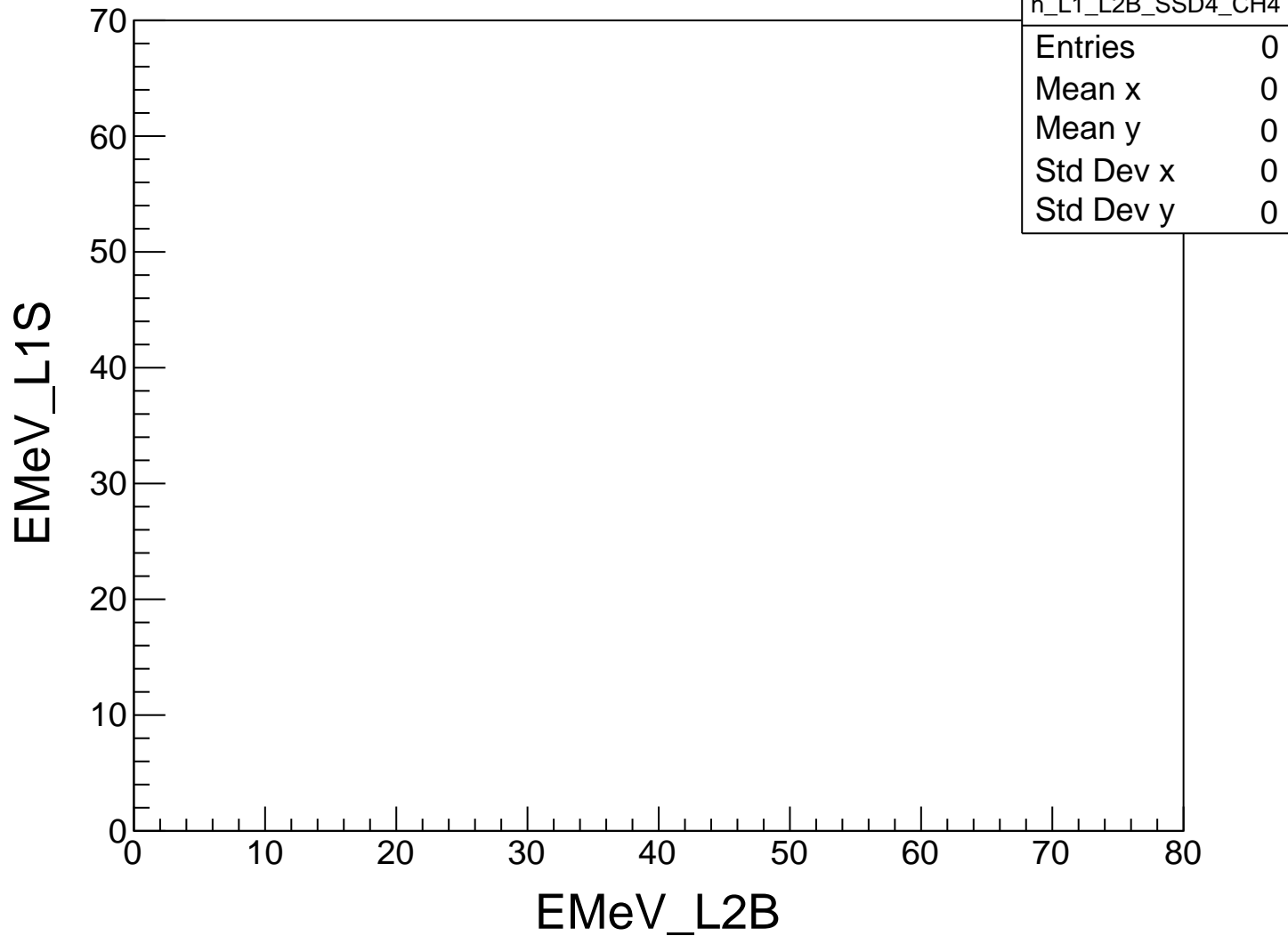
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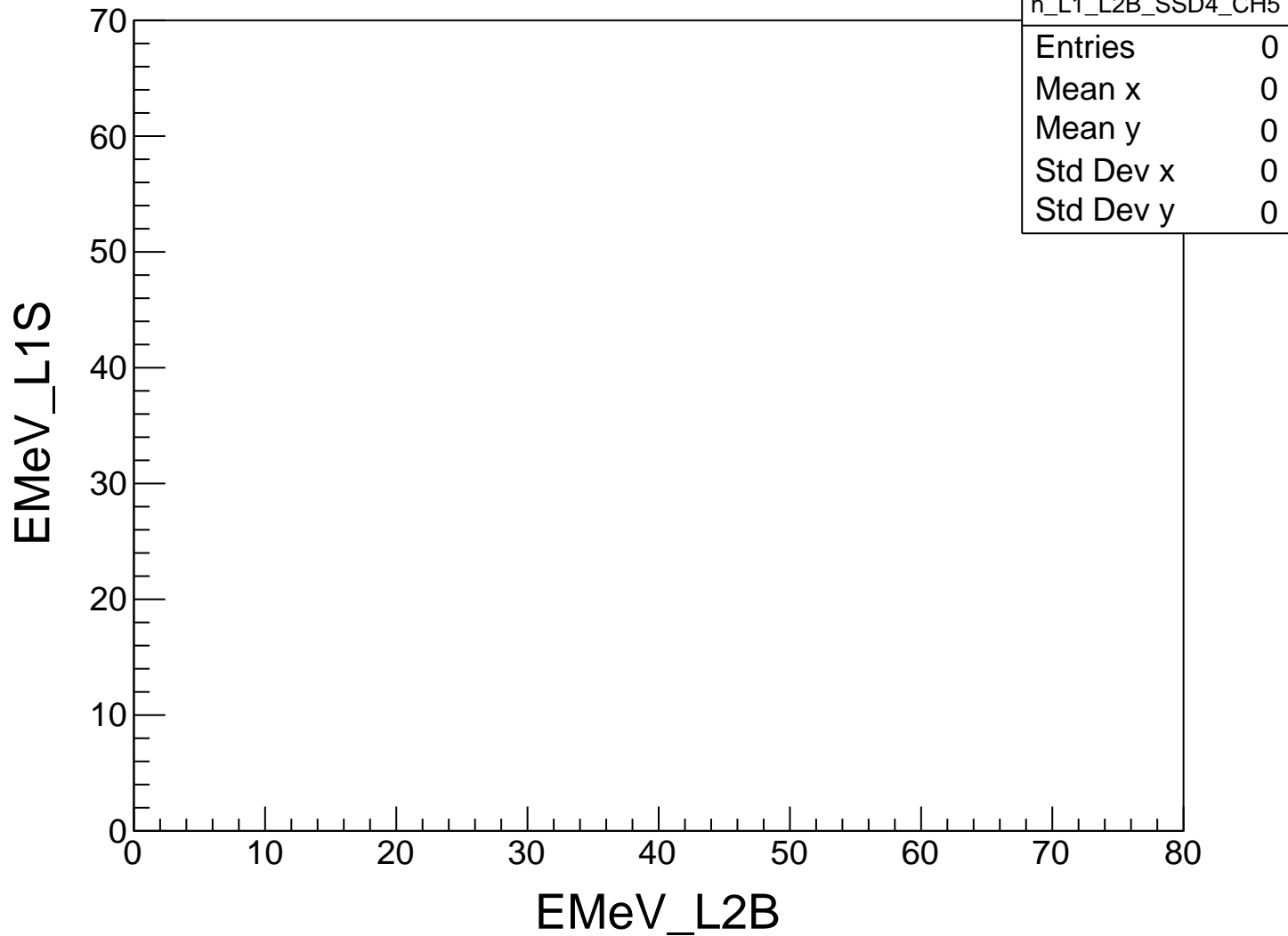
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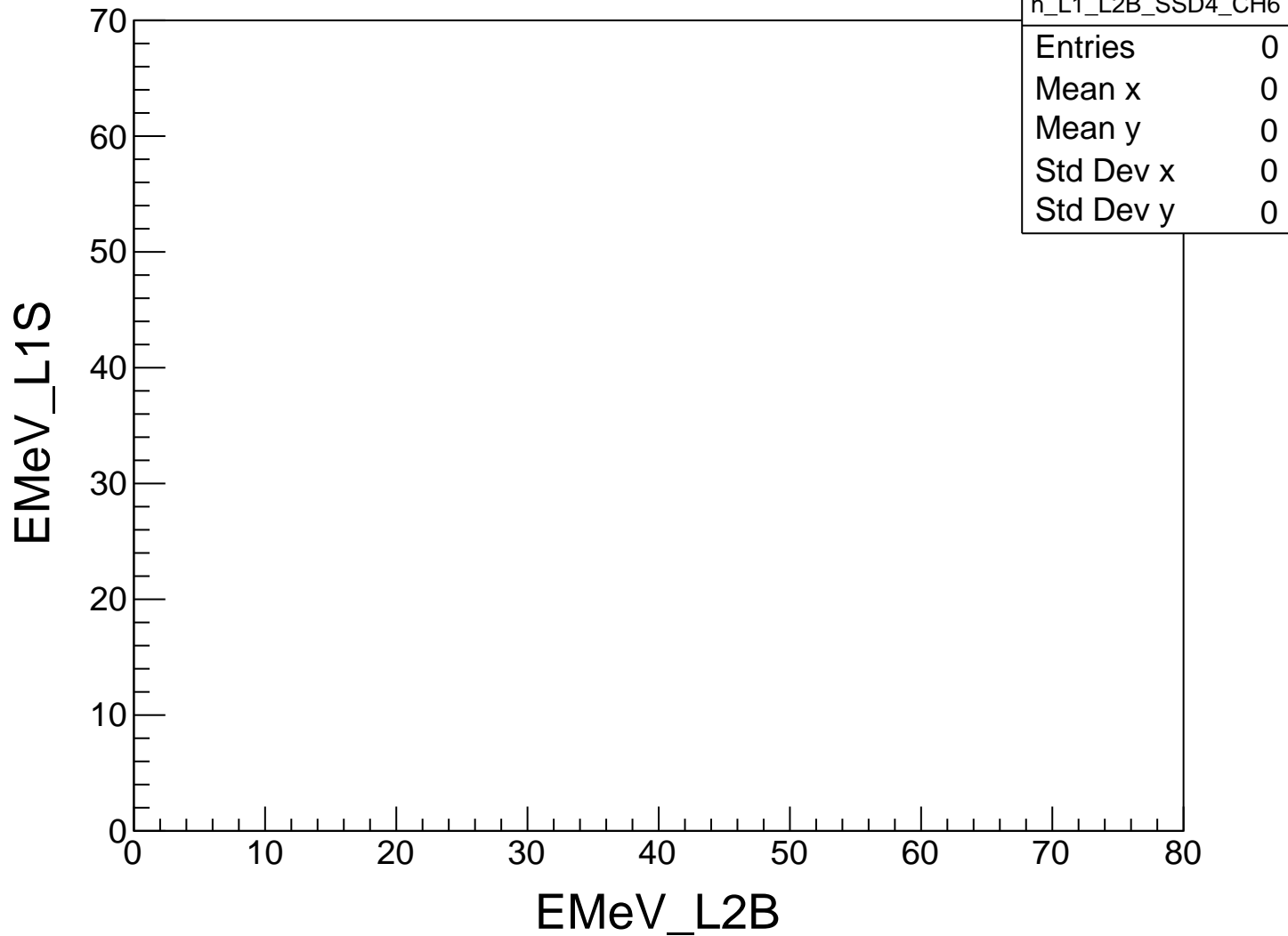
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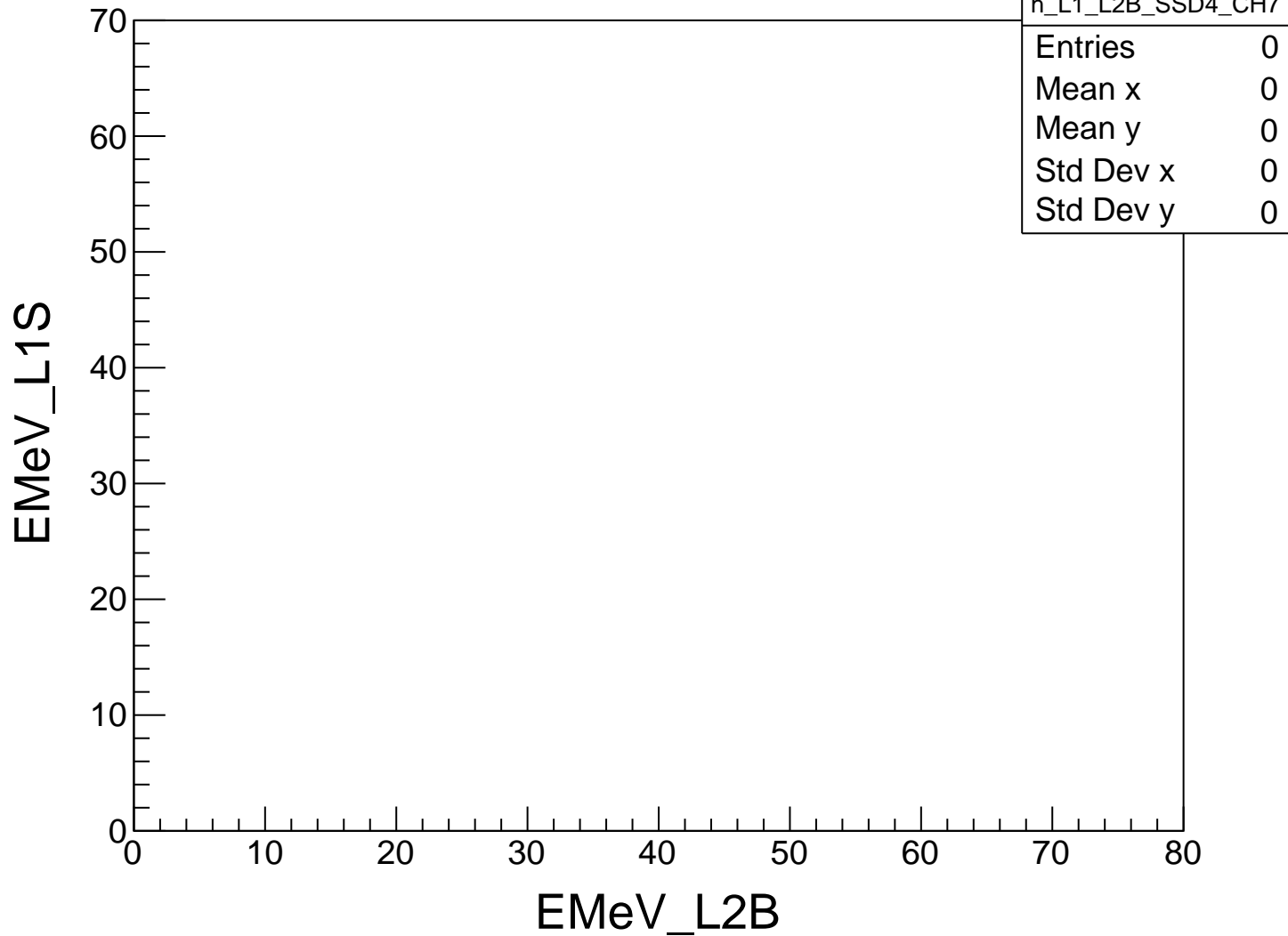
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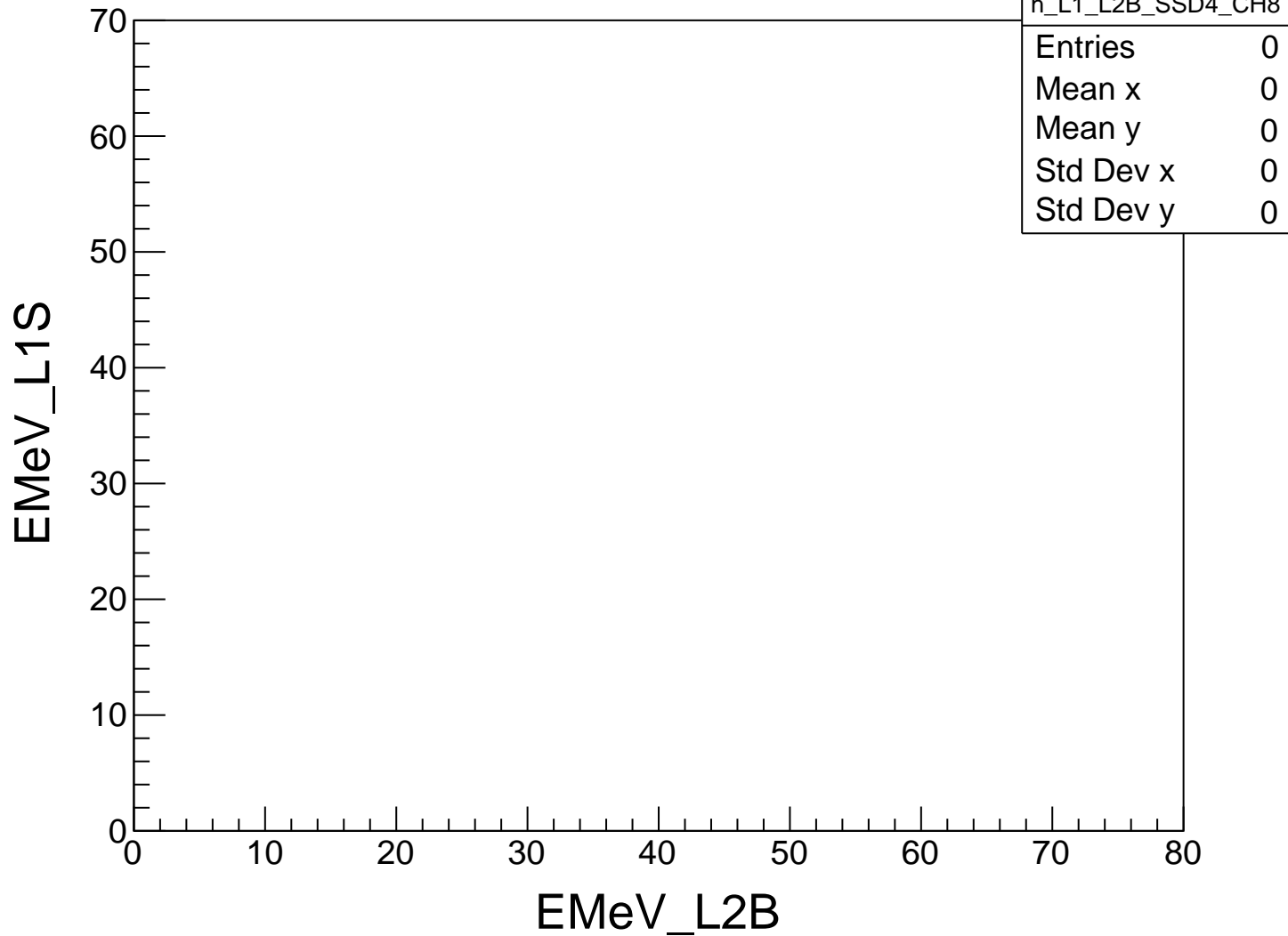
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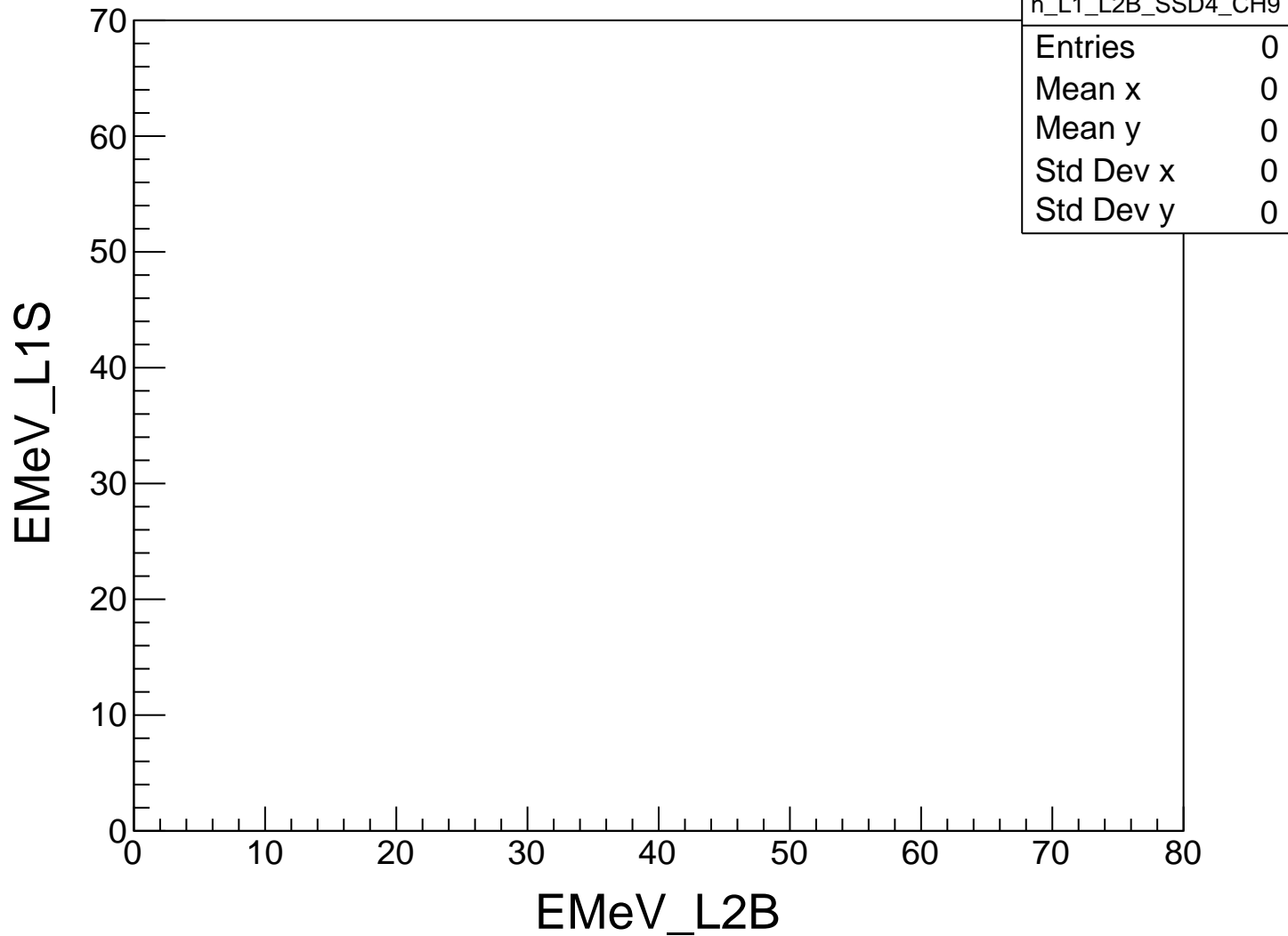
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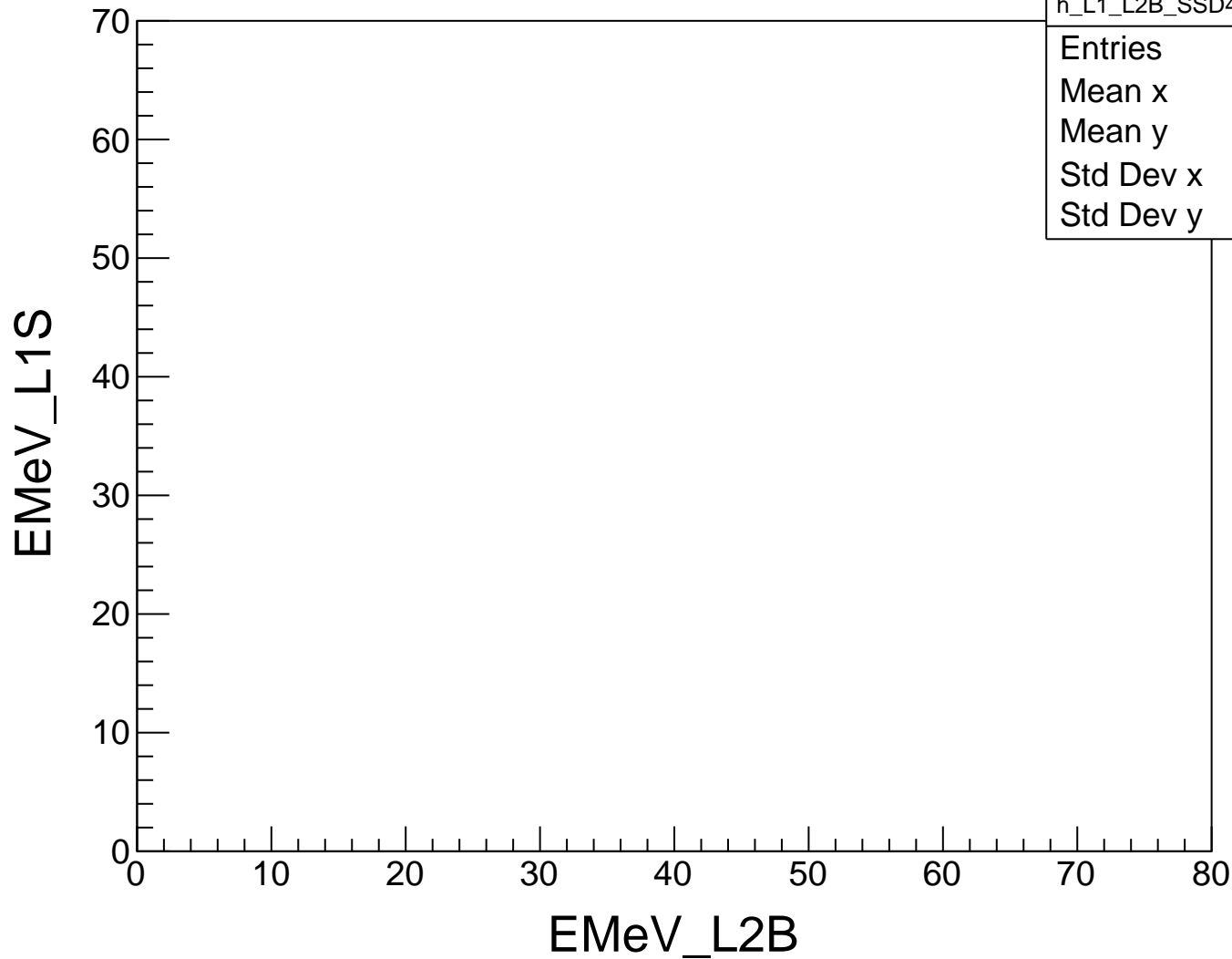
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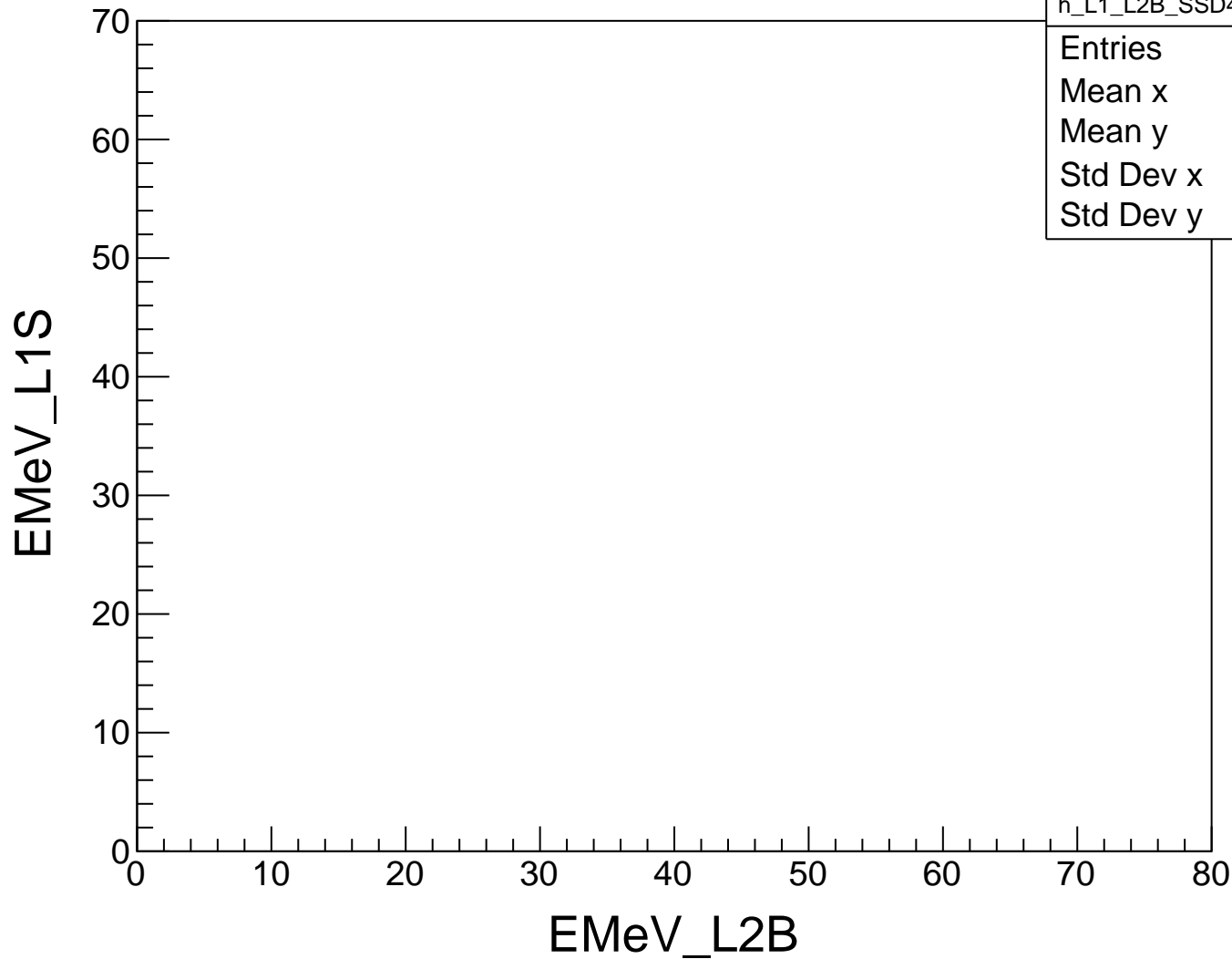
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h_L1_L2B_SSD4_CH10

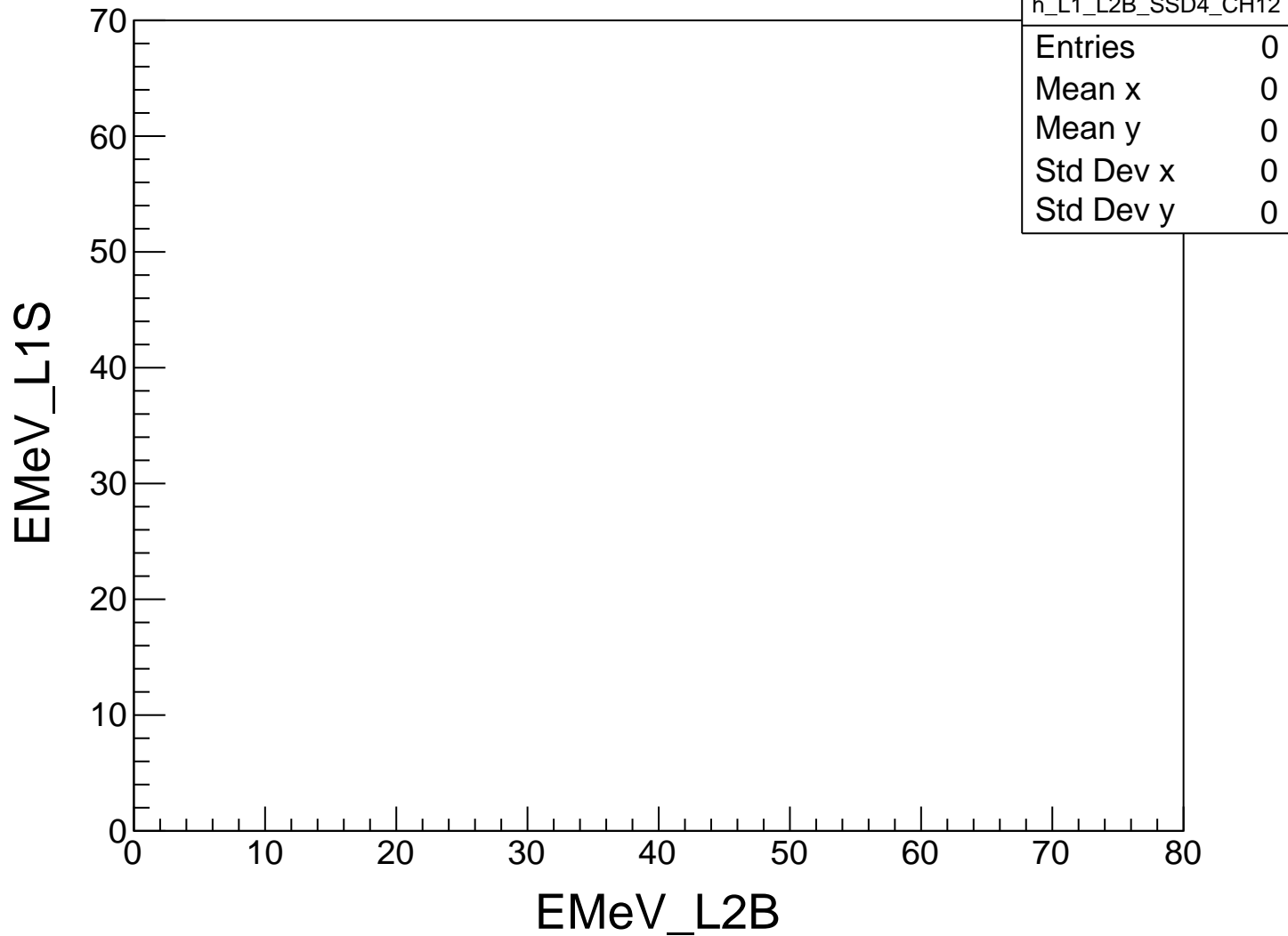


h_L1_L2B_SSD4_CH11

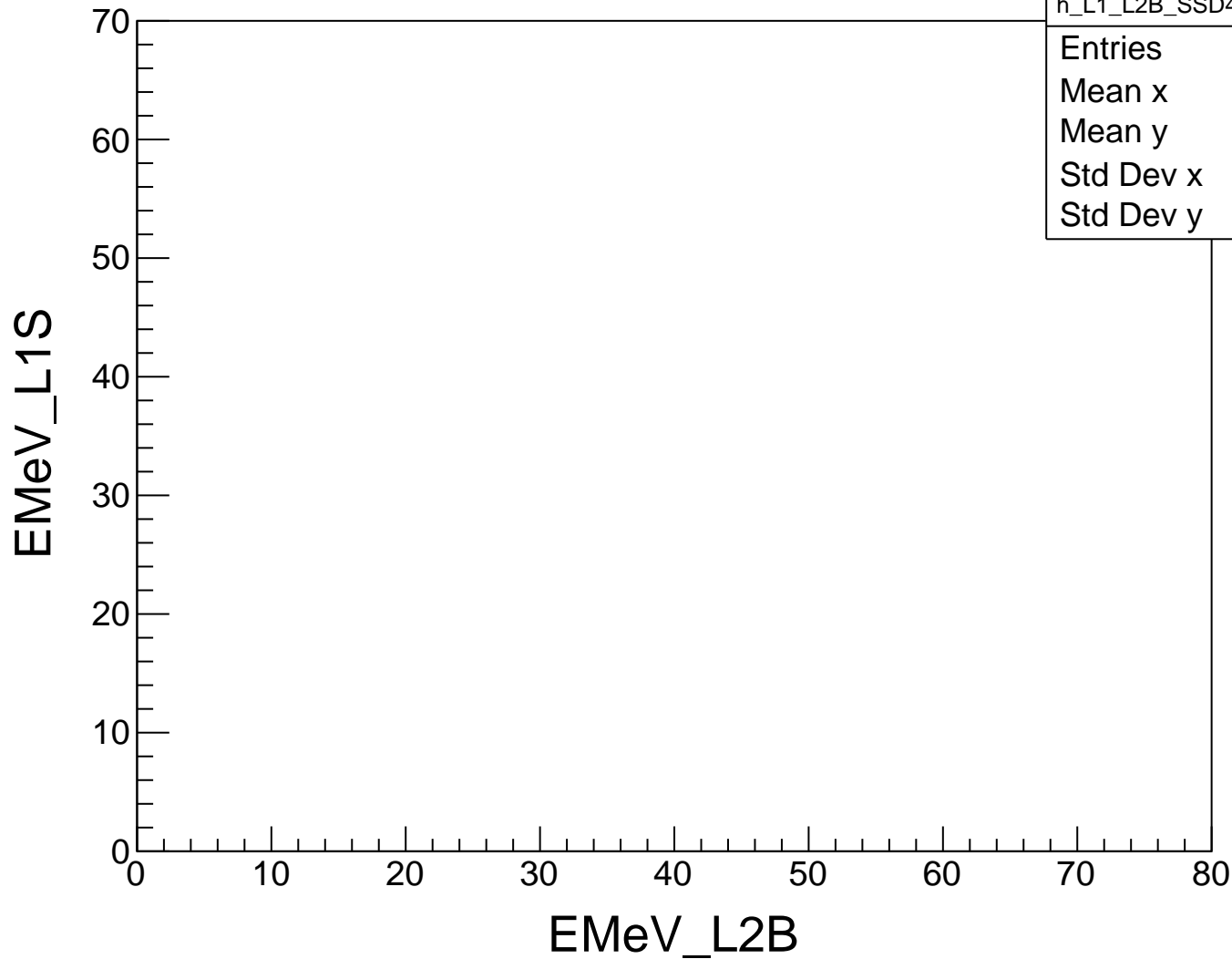


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Mean y	0
Std Dev x	0
Std Dev y	0

h_L1_L2B_SSD4_CH12

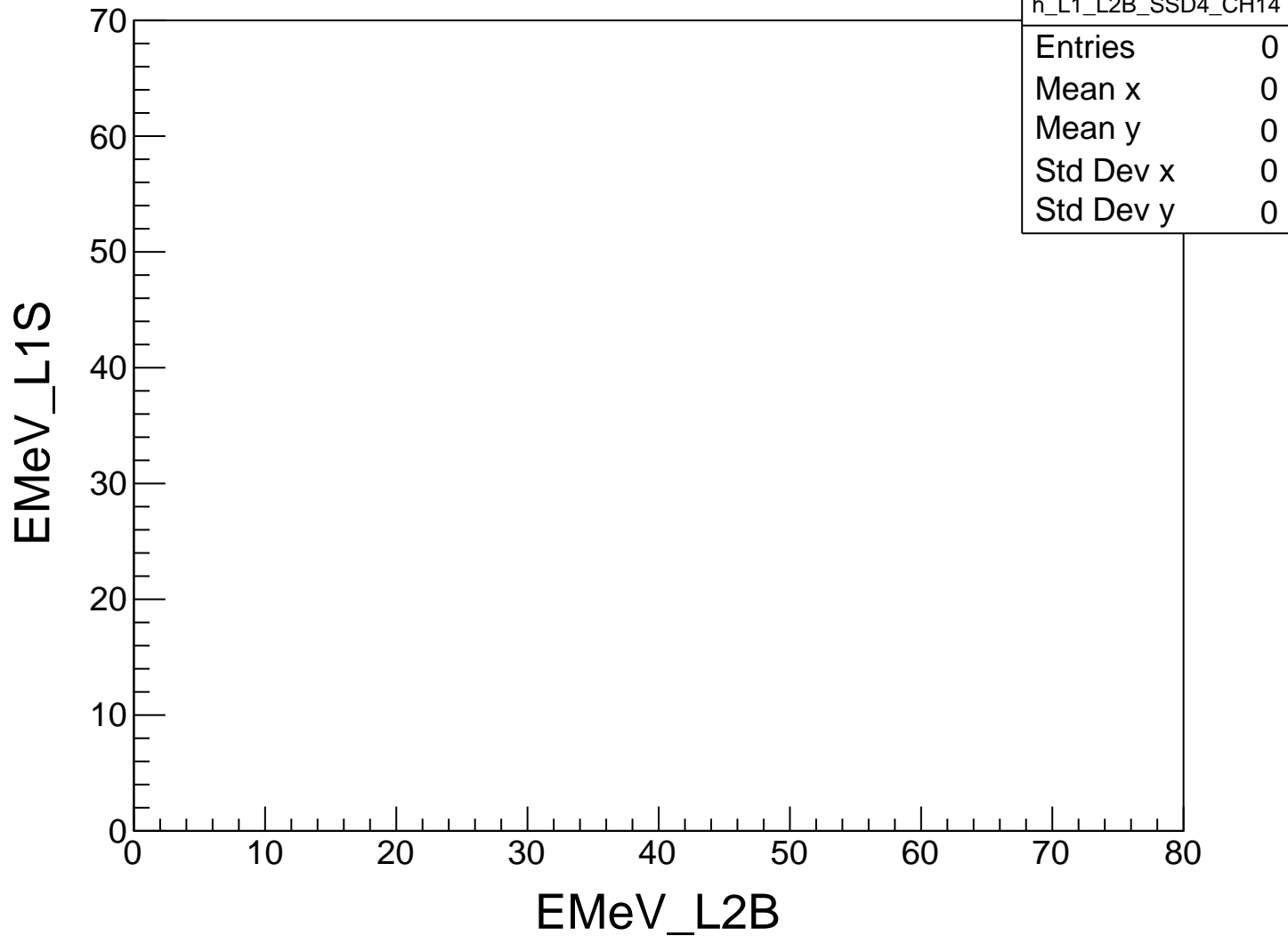


h_L1_L2B_SSD4_CH13

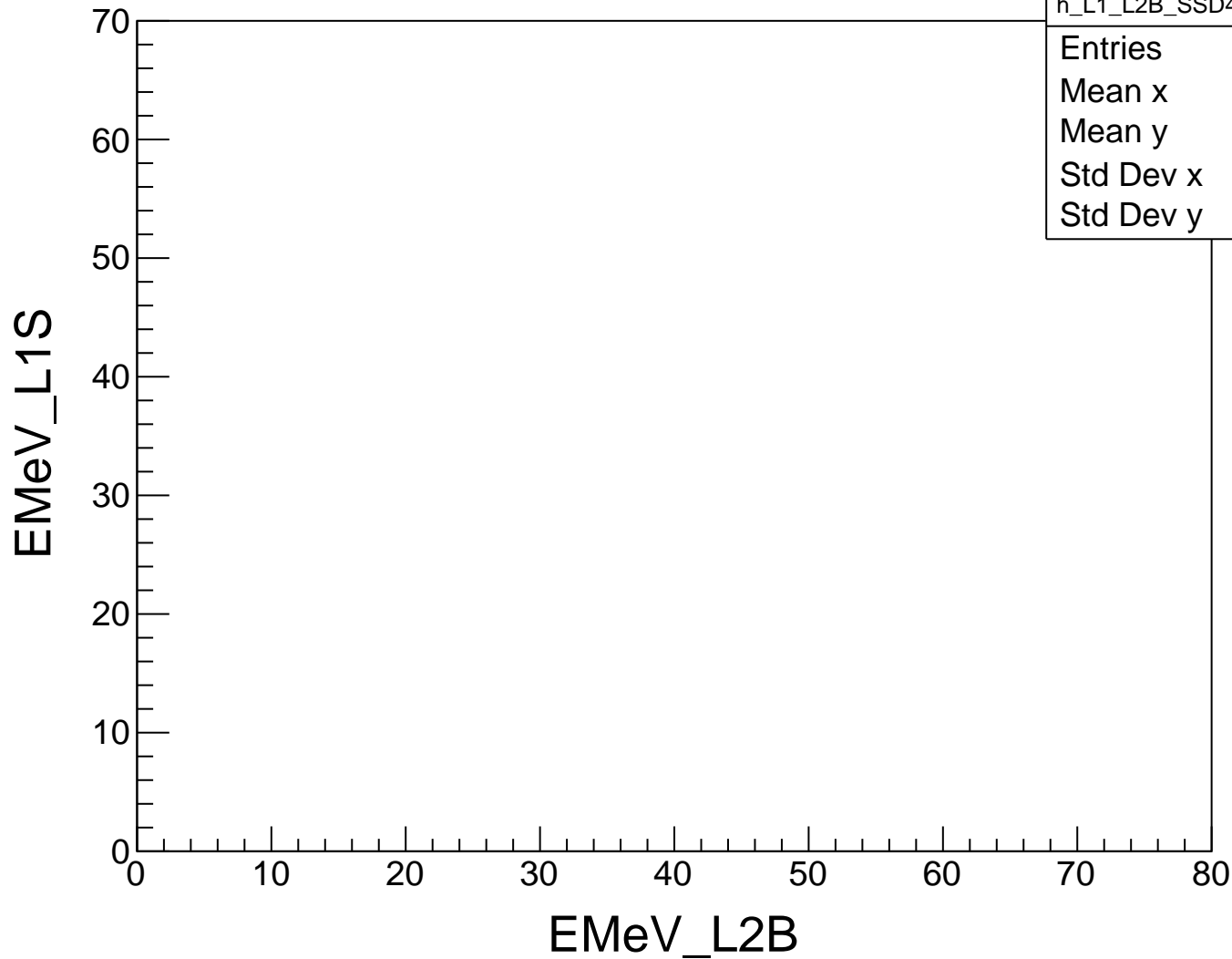


h_L1_L2B_SSD4_CH13	
Entries	0
Mean x	0
Mean y	0
Std Dev x	0
Std Dev y	0

h_L1_L2B_SSD4_CH14



h_L1_L2B_SSD4_CH15



h_L1_L2B_SSD4_CH15	
Entries	0
Mean x	0
Mean y	0
Std Dev x	0
Std Dev y	0