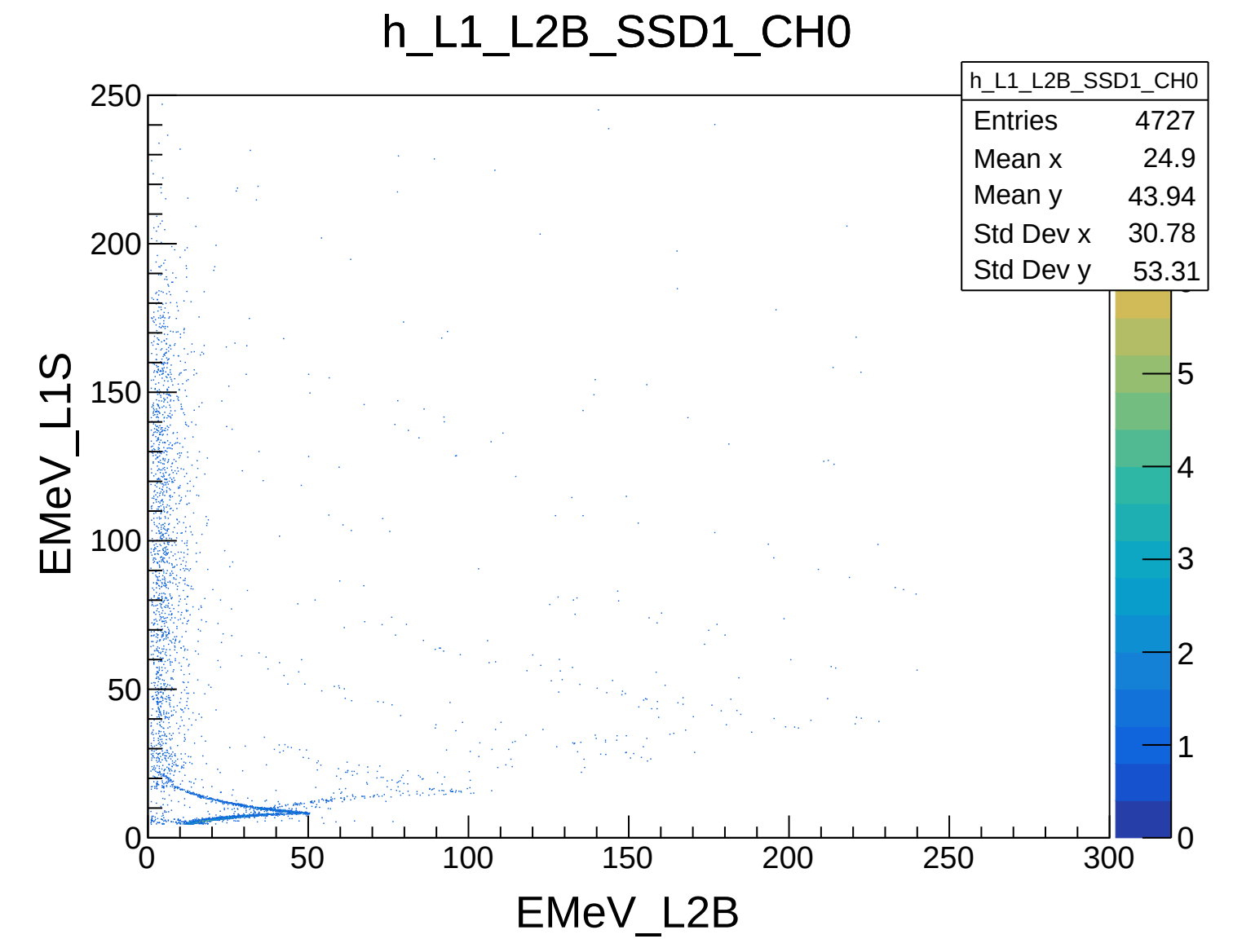
h_L1_L2B_SSD1_CH0
h_L1_L2B_SSD1_CH0
Entries 4727
Mean x 24.9
Mean y 43.94
Std Dev x 30.78
Std Dev y 53.31
EMeV_L1S
EMeV_L2B
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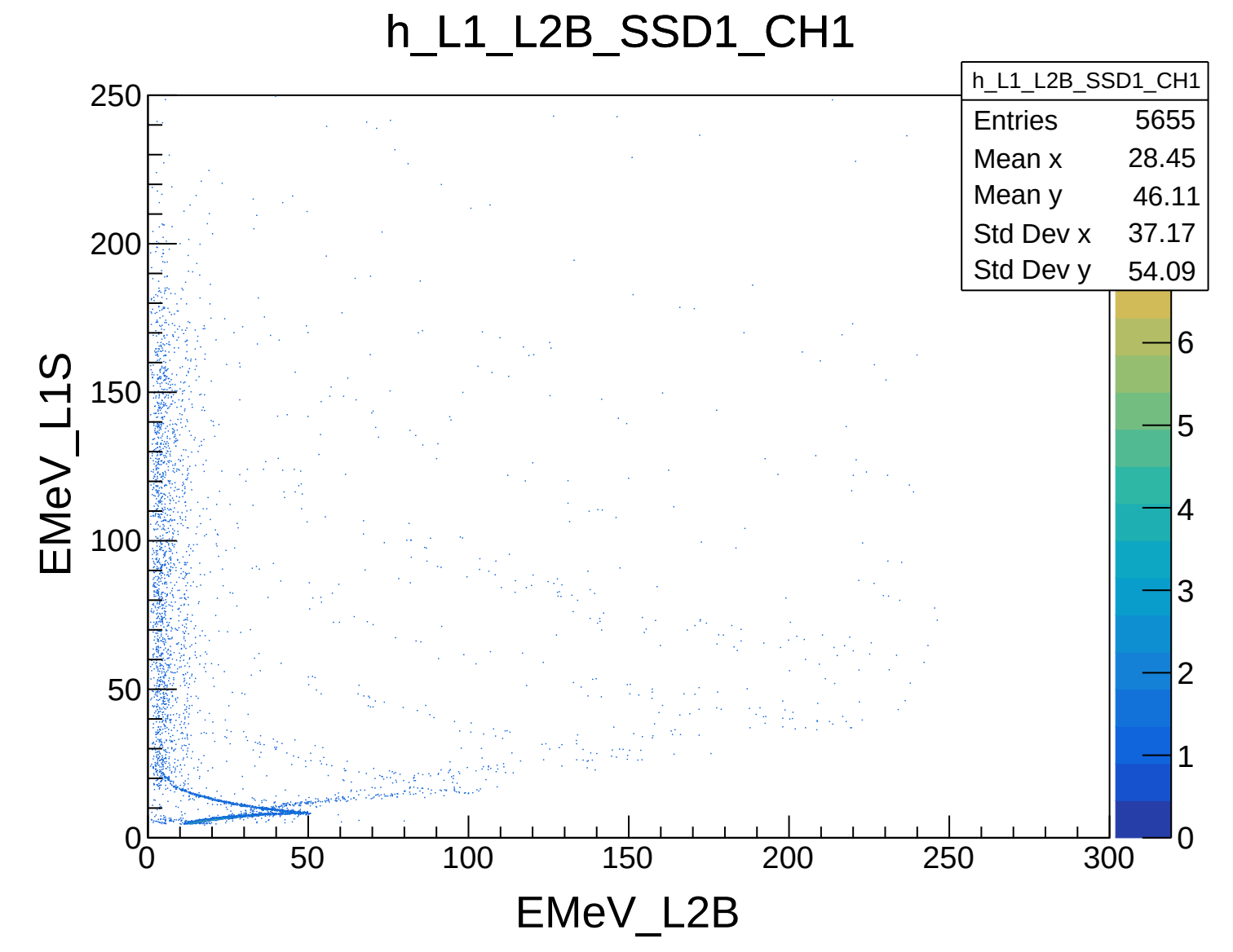
h_L1_L2B_SSD1_CH1
h_L1_L2B_SSD1_CH1
Entries 5655
Mean x 28.45
Mean y 46.11
Std Dev x 37.17
Std Dev y 54.09
EMeV_L1S
EMeV_L2B
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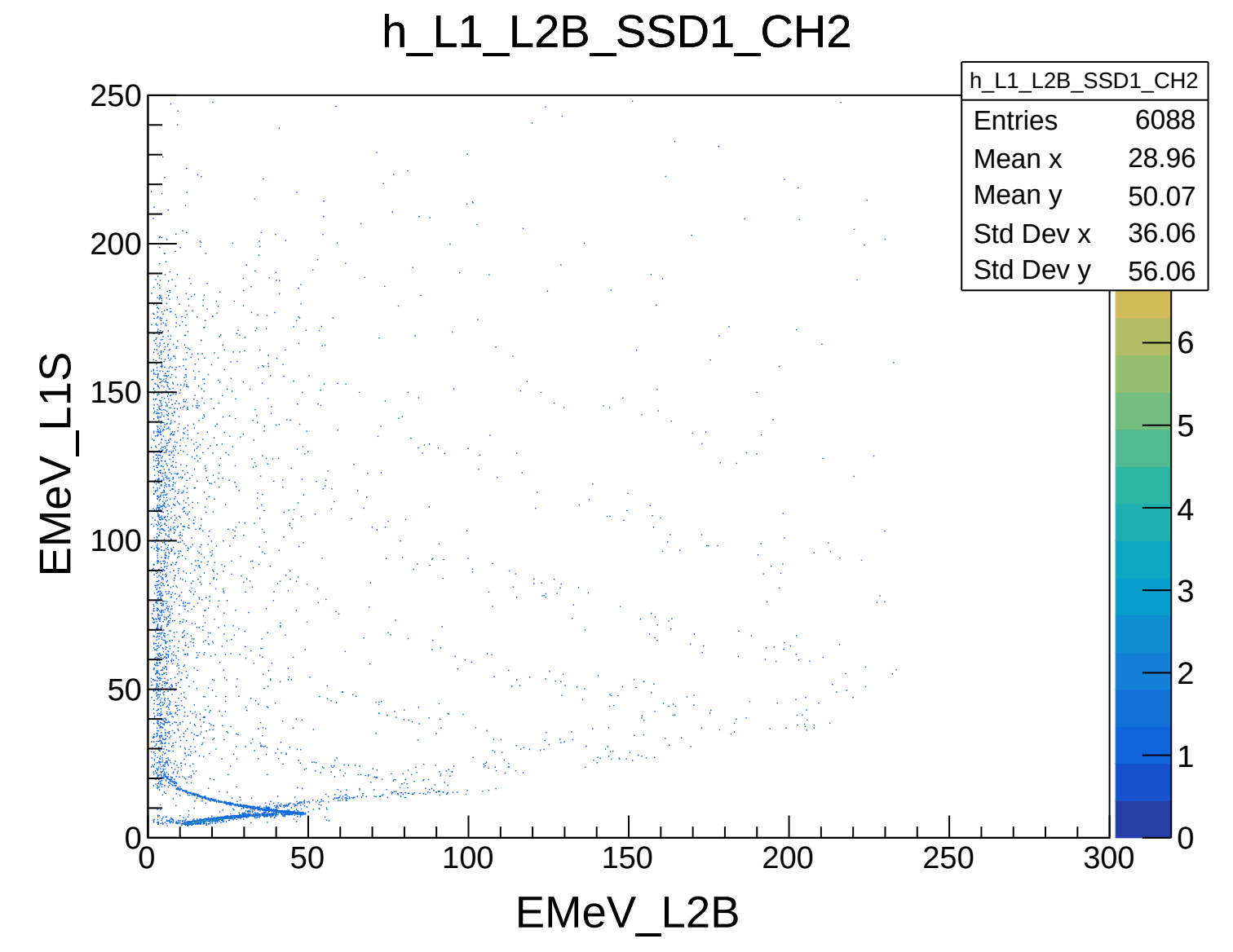
h_L1_L2B_SSD1_CH2
h_L1_L2B_SSD1_CH2
Entries 6088
Mean x 28.96
Mean y 50.07
Std Dev x 36.06
Std Dev y 56.06
EMeV_L1S
EMeV_L2B
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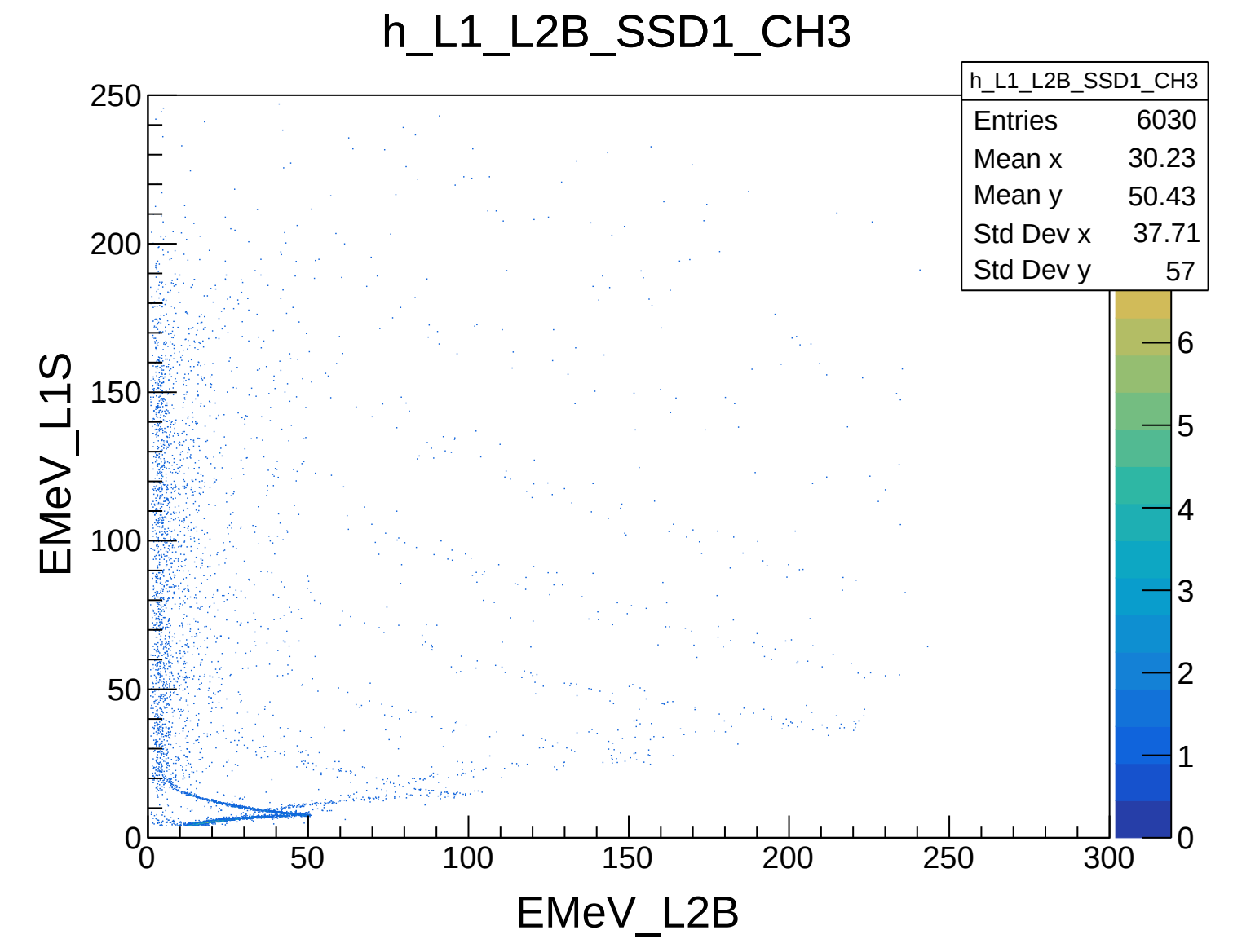
h_L1_L2B_SSD1_CH3
h_L1_L2B_SSD1_CH3
Entries 6030
Mean x 30.23
Mean y 50.43
Std Dev x 37.71
Std Dev y 57
EMeV_L1S
EMeV_L2B
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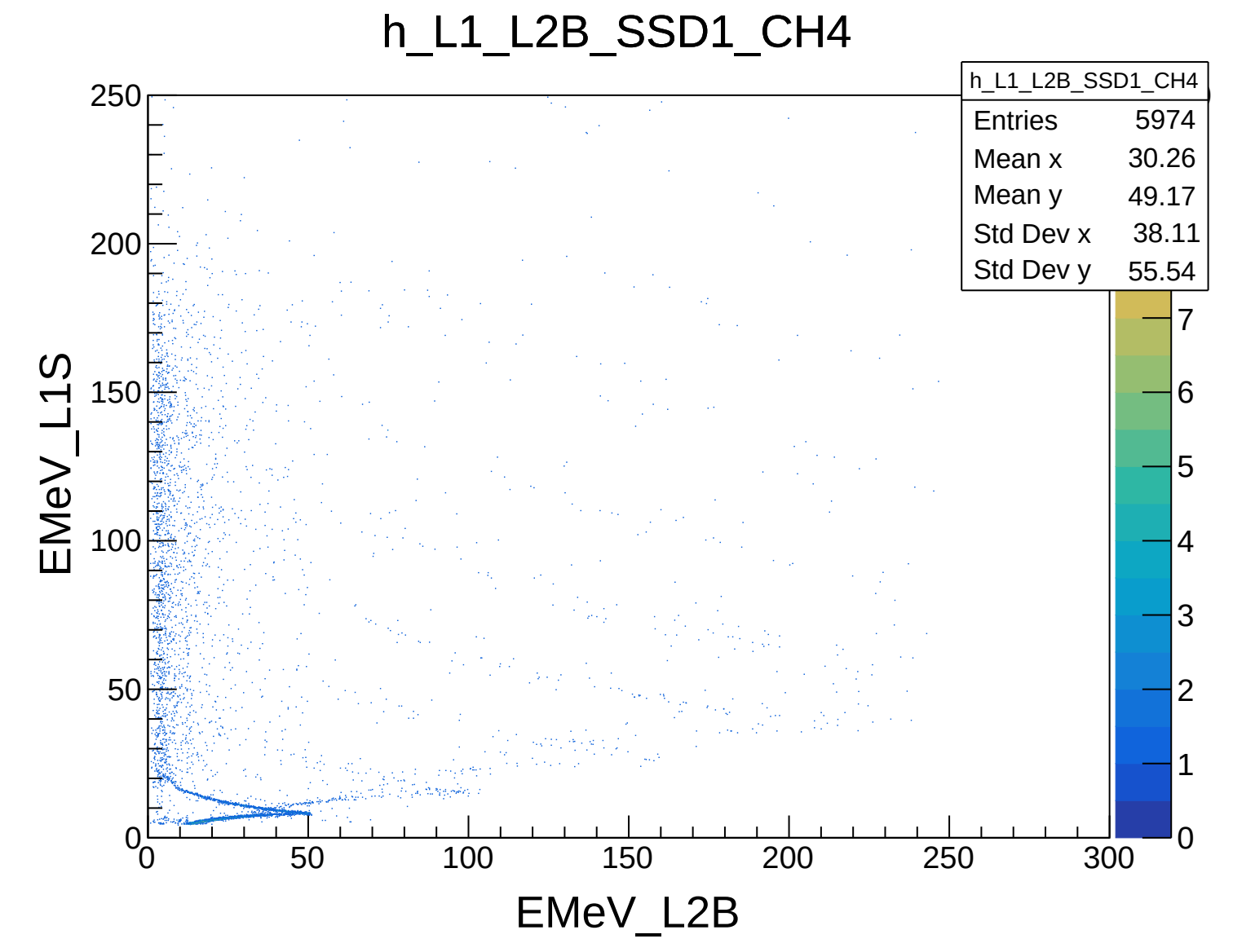
h_L1_L2B_SSD1_CH4
h_L1_L2B_SSD1_CH4
Entries 5974
Mean x 30.26
Mean y 49.17
Std Dev x 38.11
Std Dev y 55.54
EMeV_L1S
EMeV_L2B
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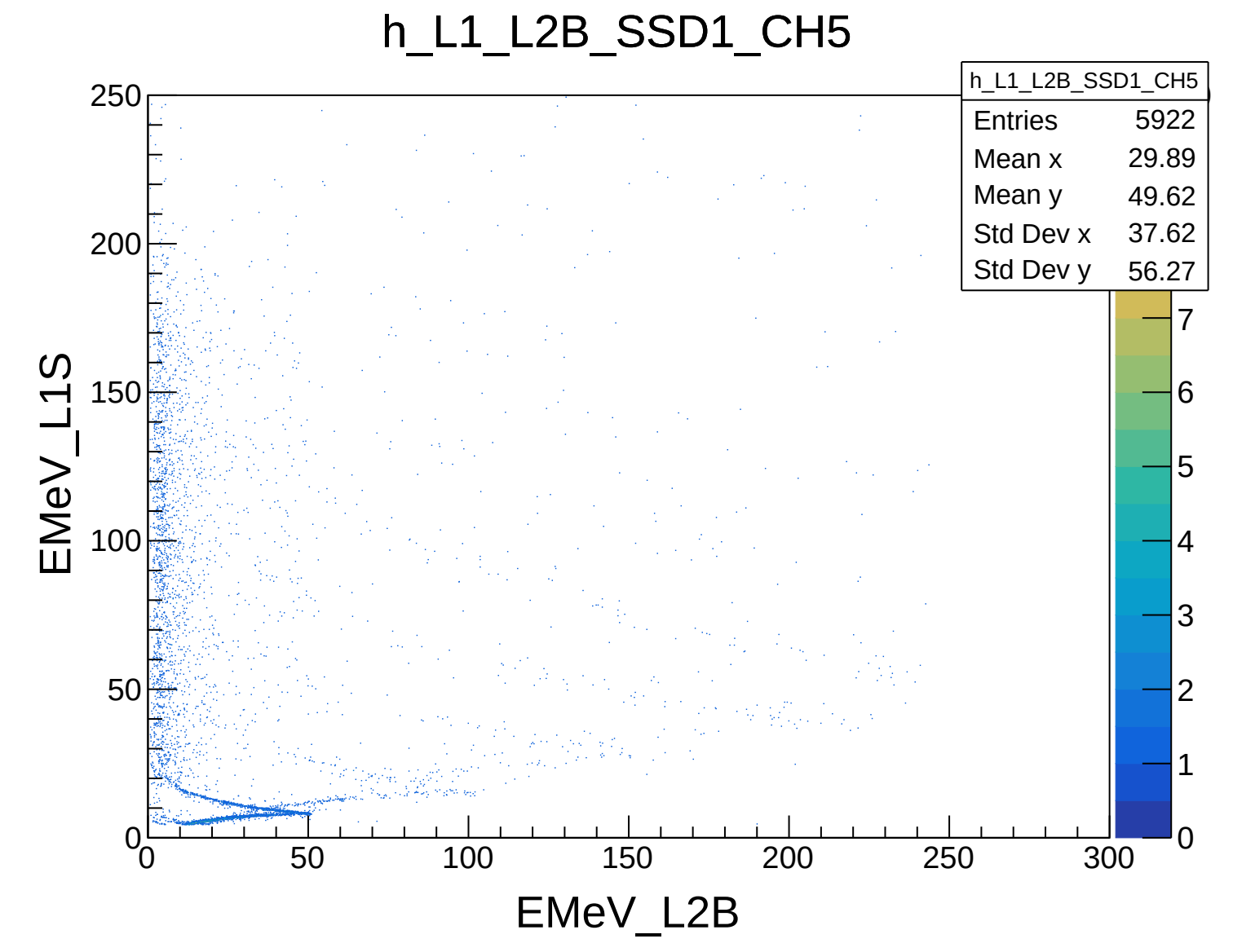
h_L1_L2B_SSD1_CH5
h_L1_L2B_SSD1_CH5
Entries 5922
Mean x 29.89
Mean y 49.62
Std Dev x 37.62
Std Dev y 56.27
EMeV_L1S
EMeV_L2B
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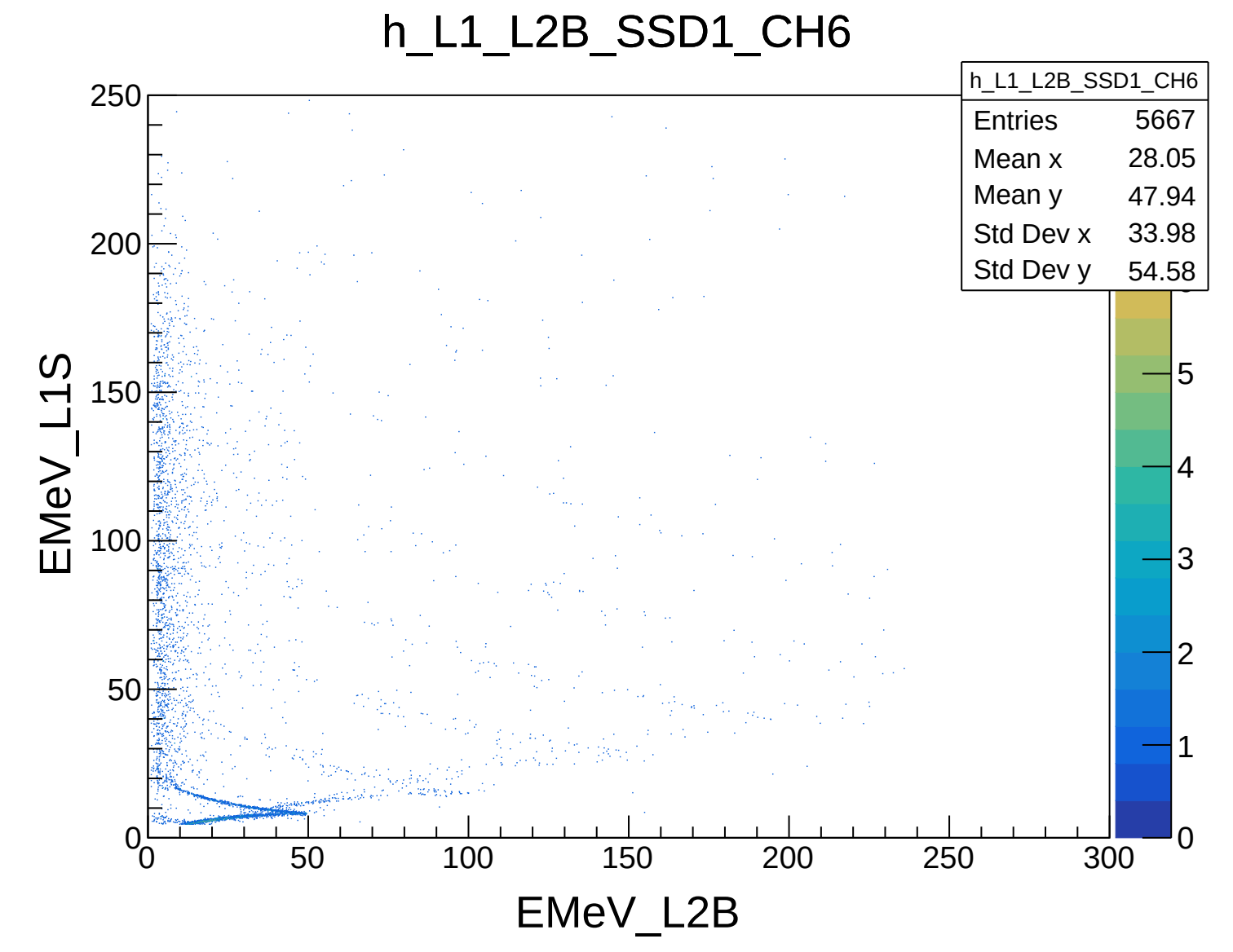
h_L1_L2B_SSD1_CH6
h_L1_L2B_SSD1_CH6
Entries 5667
Mean x 28.05
Mean y 47.94
Std Dev x 33.98
Std Dev y 54.58
EMeV_L1S
EMeV_L2B
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2
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4
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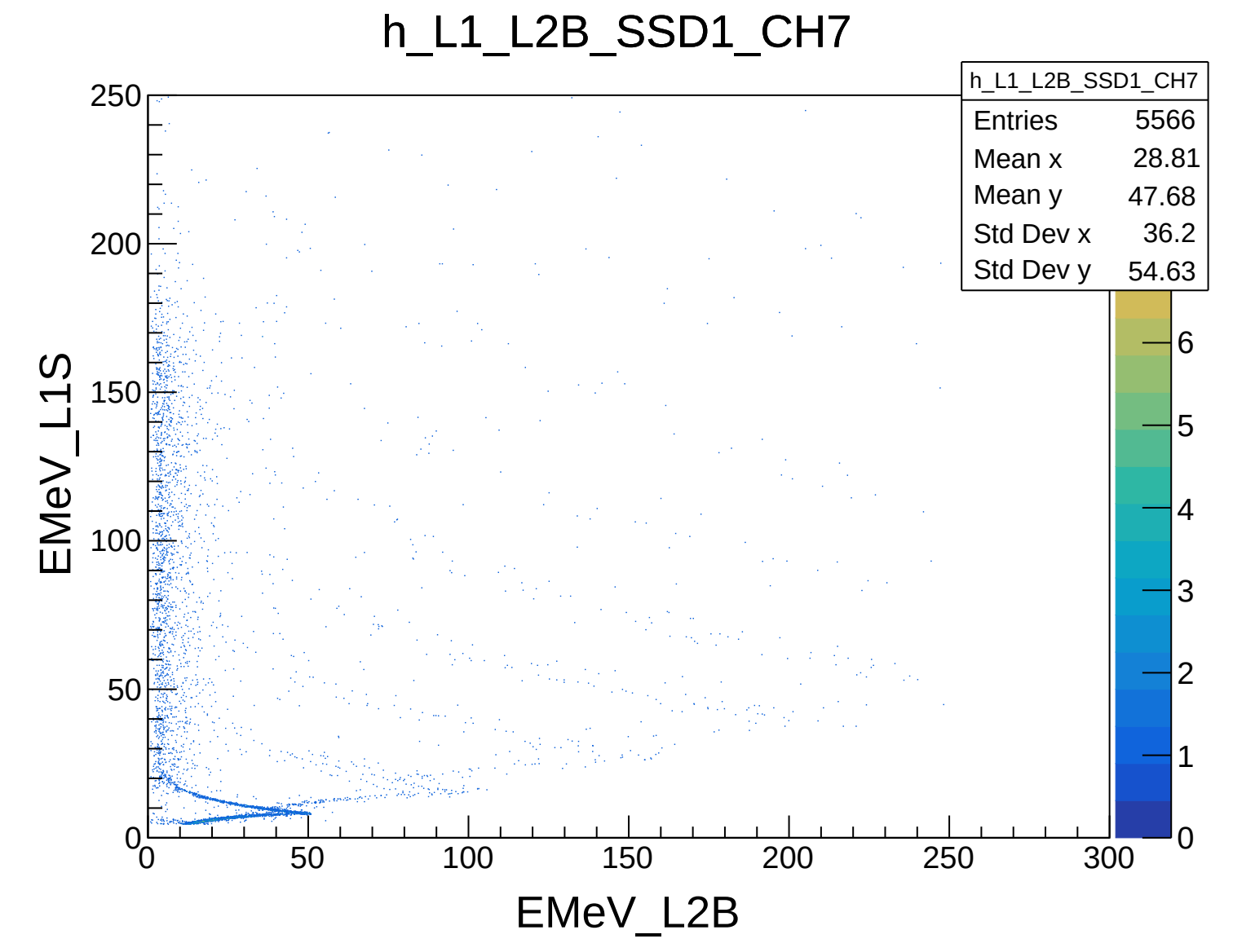
h_L1_L2B_SSD1_CH7
h_L1_L2B_SSD1_CH7
Entries 5566
Mean x 28.81
Mean y 47.68
Std Dev x 36.2
Std Dev y 54.63
EMeV_L1S
EMeV_L2B
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250
300
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3
4
5
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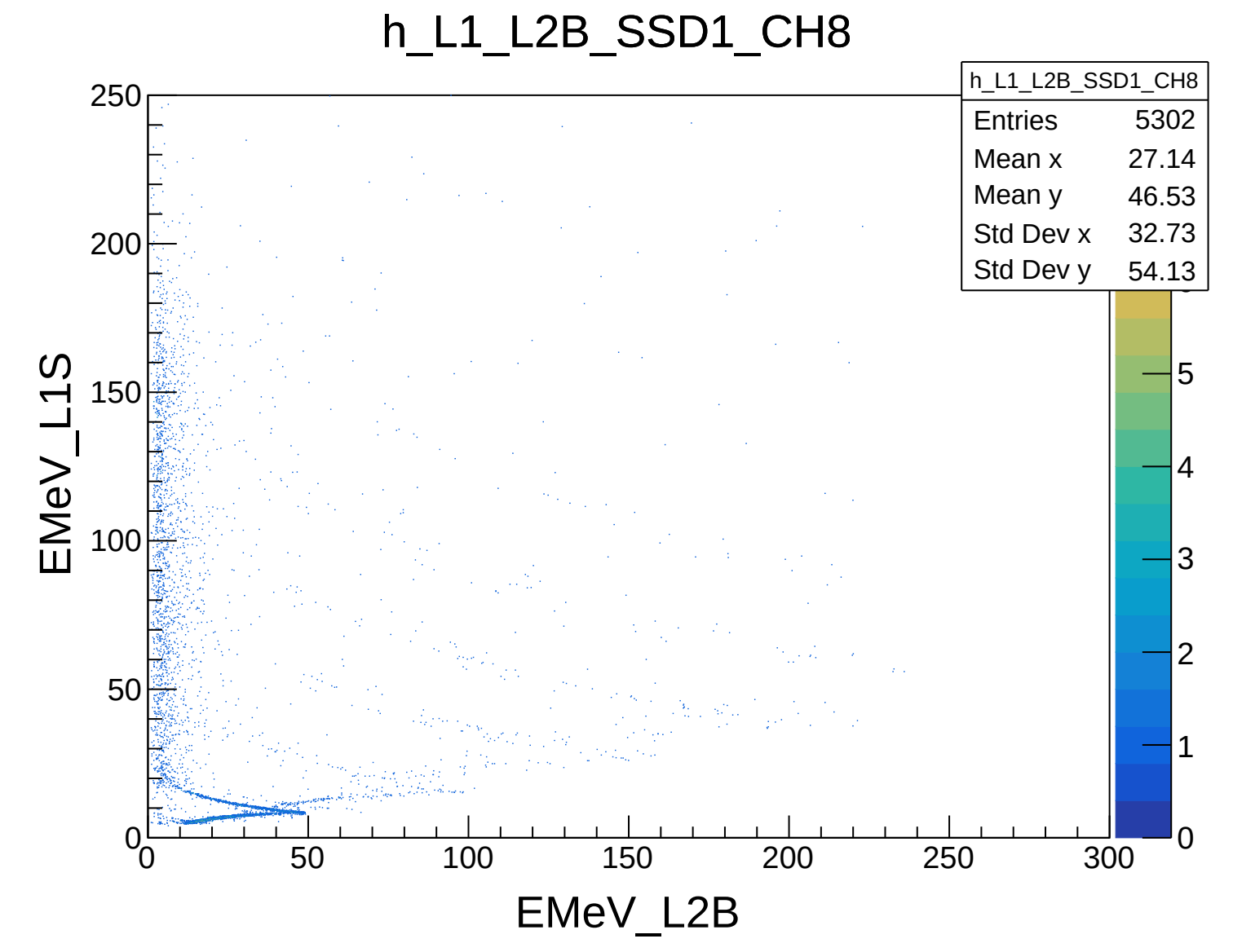
h_L1_L2B_SSD1_CH8
h_L1_L2B_SSD1_CH8
Entries 5302
Mean x 27.14
Mean y 46.53
Std Dev x 32.73
Std Dev y 54.13
EMeV_L1S
EMeV_L2B
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300
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2
3
4
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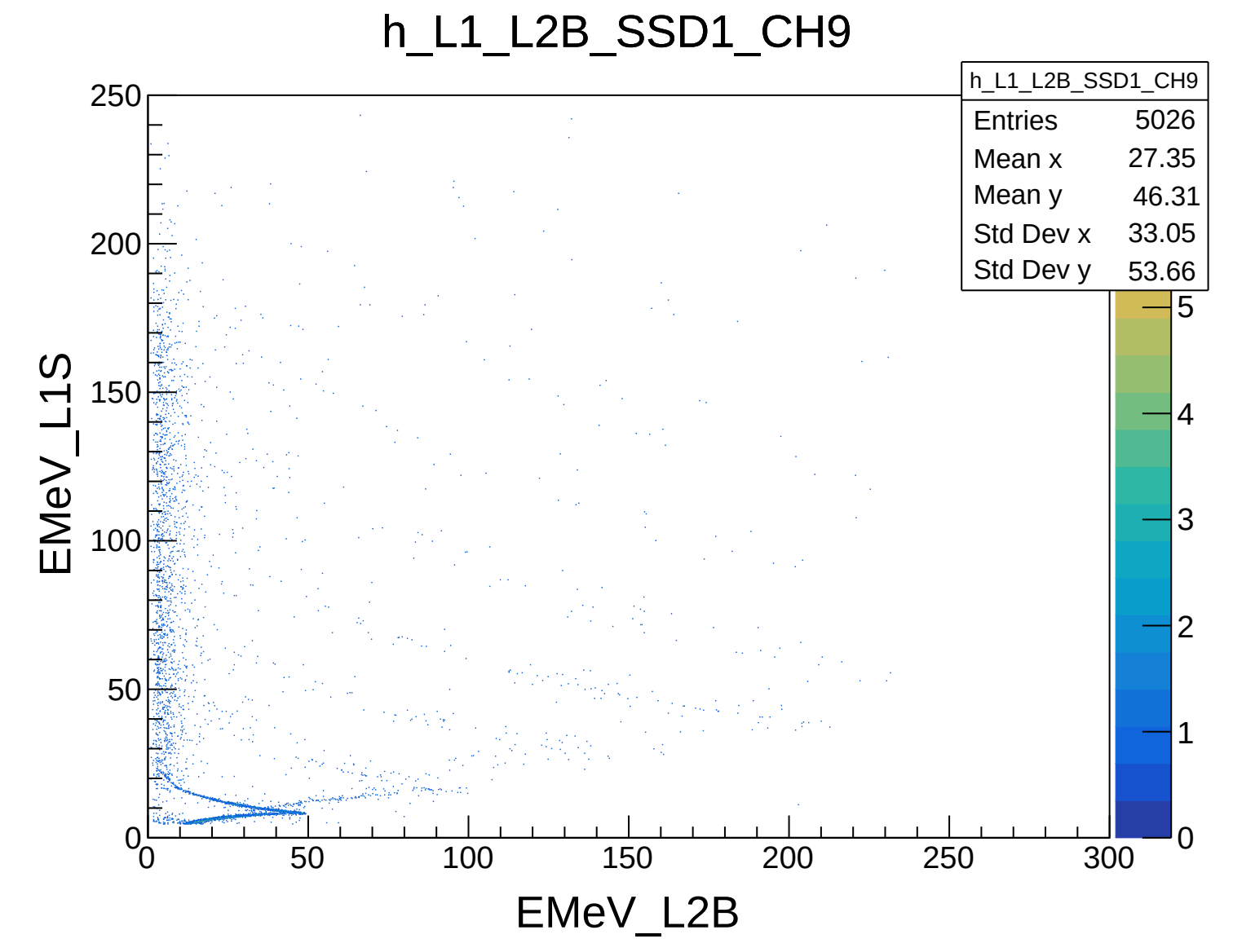
h_L1_L2B_SSD1_CH9
h_L1_L2B_SSD1_CH9
Entries 5026
Mean x 27.35
Mean y 46.31
Std Dev x 33.05
Std Dev y 53.66
EMeV_L1S
EMeV_L2B
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300
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2
3
4
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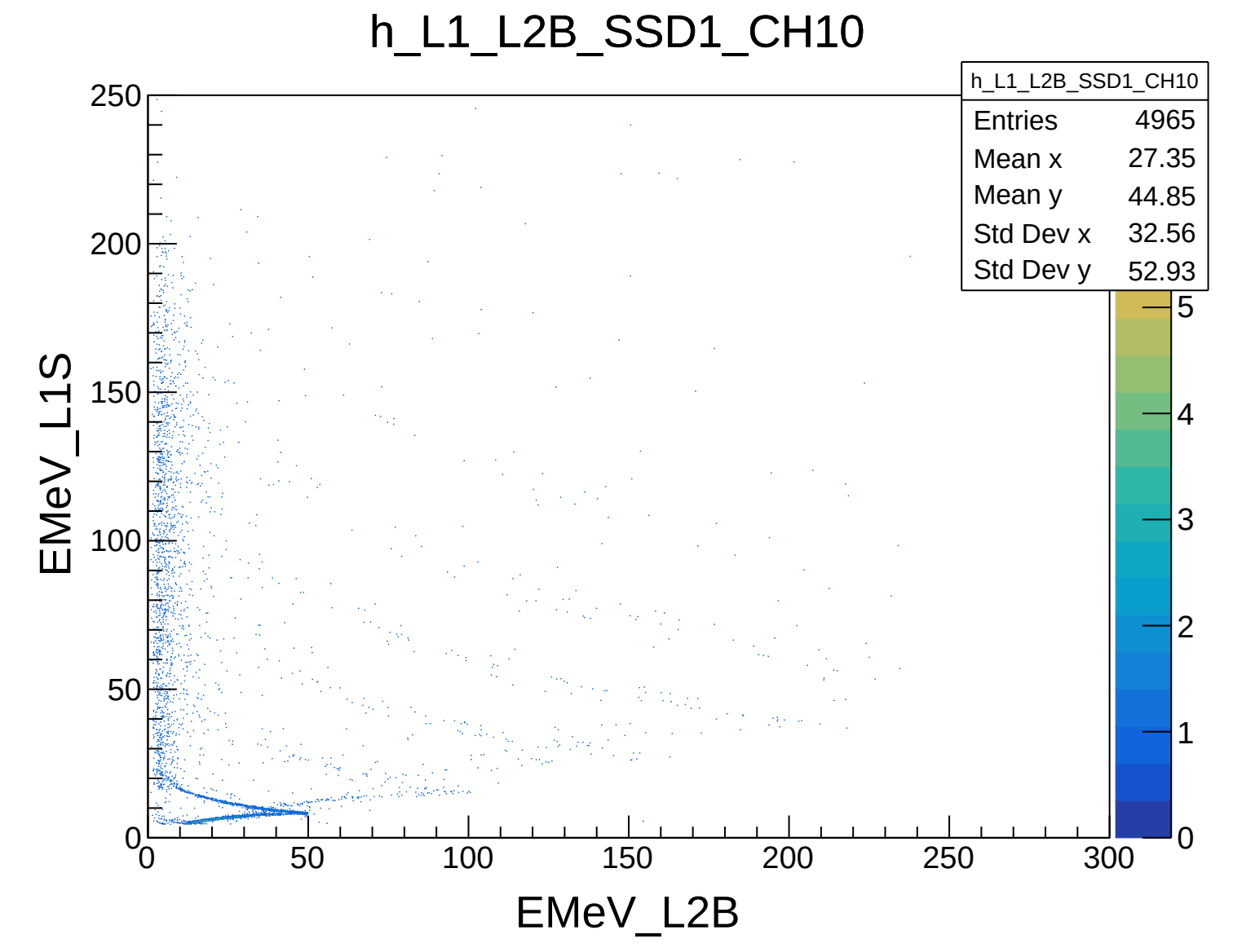
h_L1_L2B_SSD1_CH10
h_L1_L2B_SSD1_CH10
Entries 4965
Mean x 27.35
Mean y 44.85
Std Dev x 32.56
Std Dev y 52.93
EMeV_L1S
EMeV_L2B
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200
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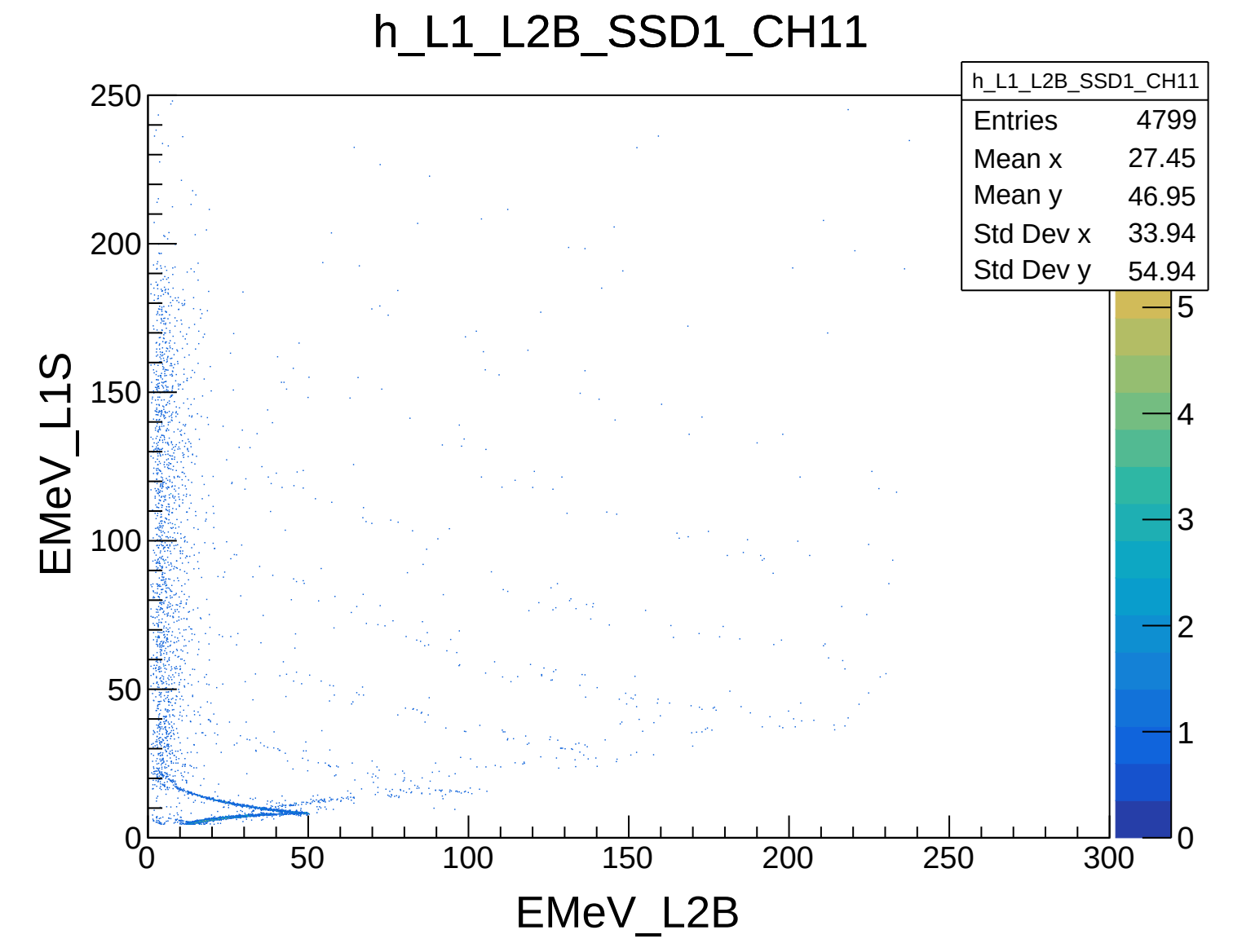
3
4
5


h_L1_L2B_SSD1_CH11
h_L1_L2B_SSD1_CH11
Entries 4799
Mean x 27.45
Mean y 46.95
Std Dev x 33.94
Std Dev y 54.94
EMeV_L1S
EMeV_L2B
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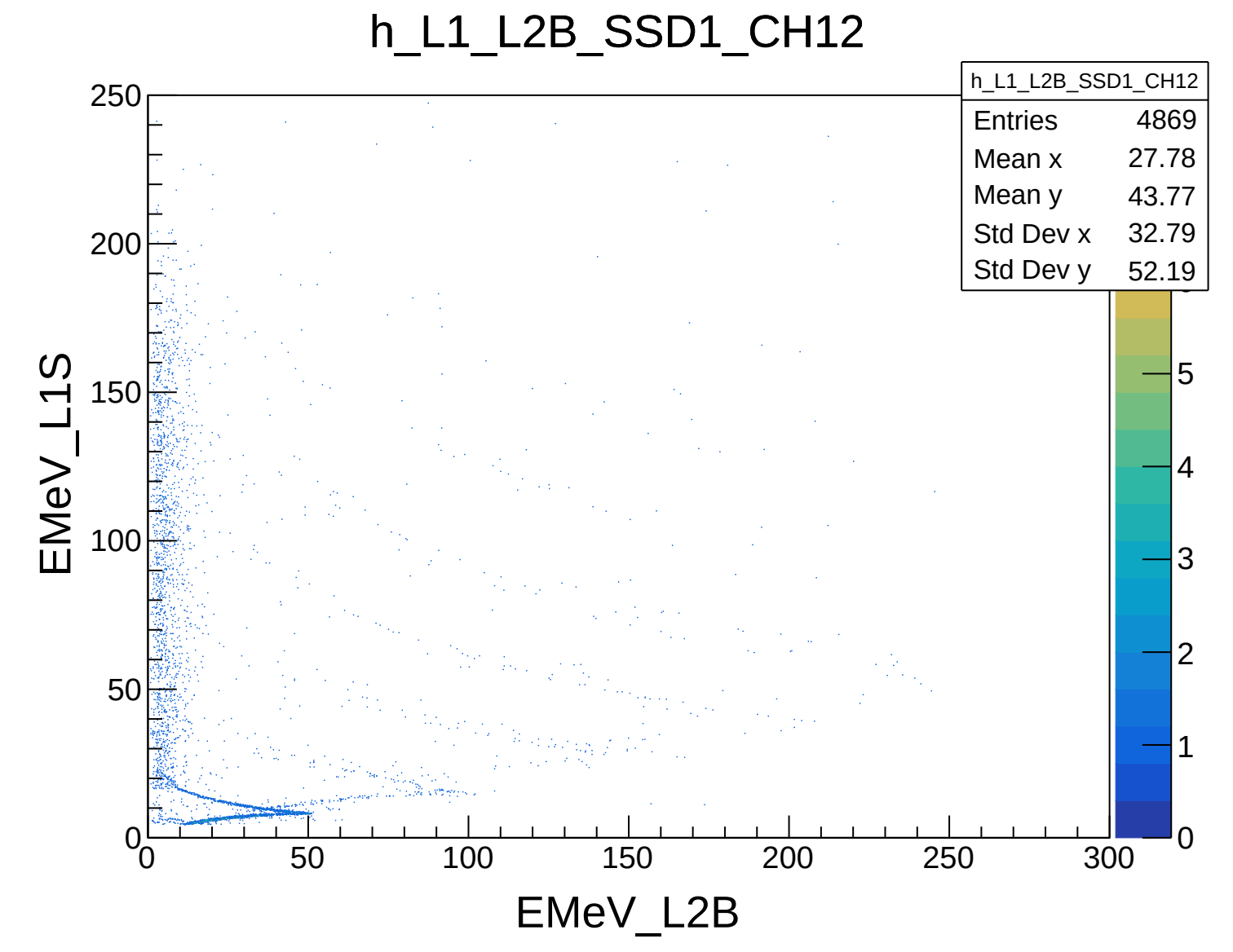
h_L1_L2B_SSD1_CH12
h_L1_L2B_SSD1_CH12
Entries 4869
Mean x 27.78
Mean y 43.77
Std Dev x 32.79
Std Dev y 52.19
EMeV_L1S
EMeV_L2B
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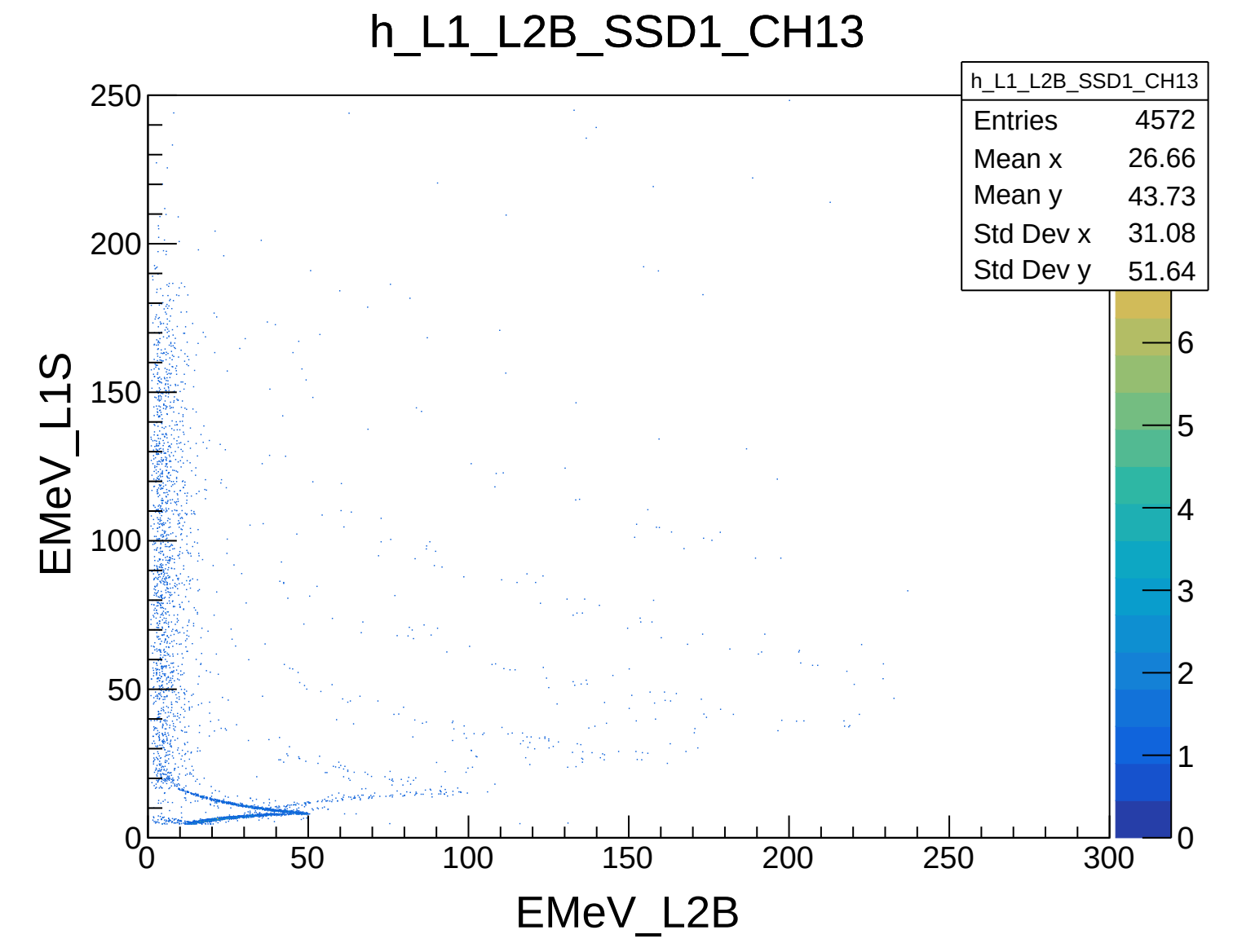
h_L1_L2B_SSD1_CH13
h_L1_L2B_SSD1_CH13
Entries 4572
Mean x 26.66
Mean y 43.73
Std Dev x 31.08
Std Dev y 51.64
EMeV_L1S
EMeV_L2B
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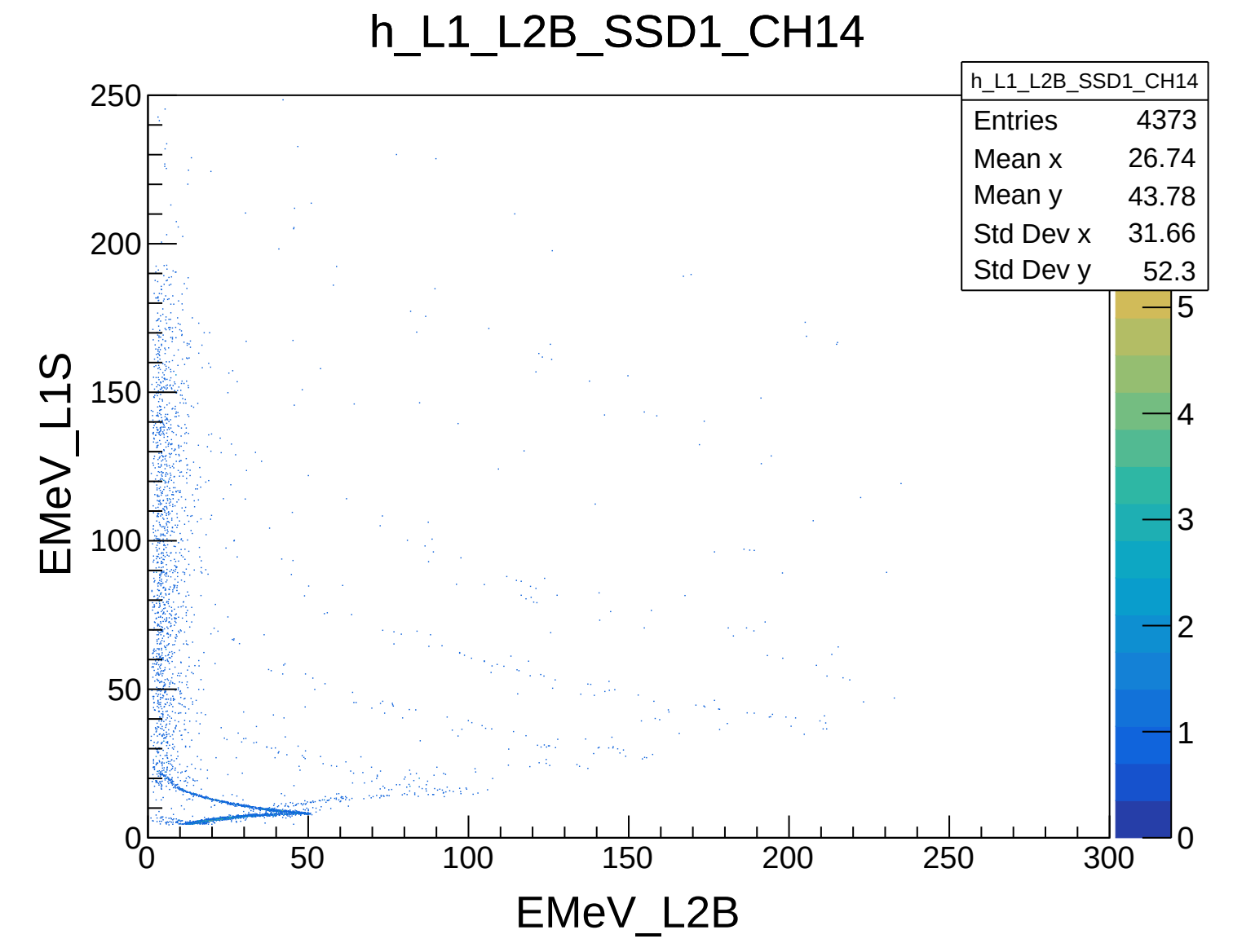
h_L1_L2B_SSD1_CH14
h_L1_L2B_SSD1_CH14
Entries 4373
Mean x 26.74
Mean y 43.78
Std Dev x 31.66
Std Dev y 52.3
EMeV_L1S
EMeV_L2B
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4
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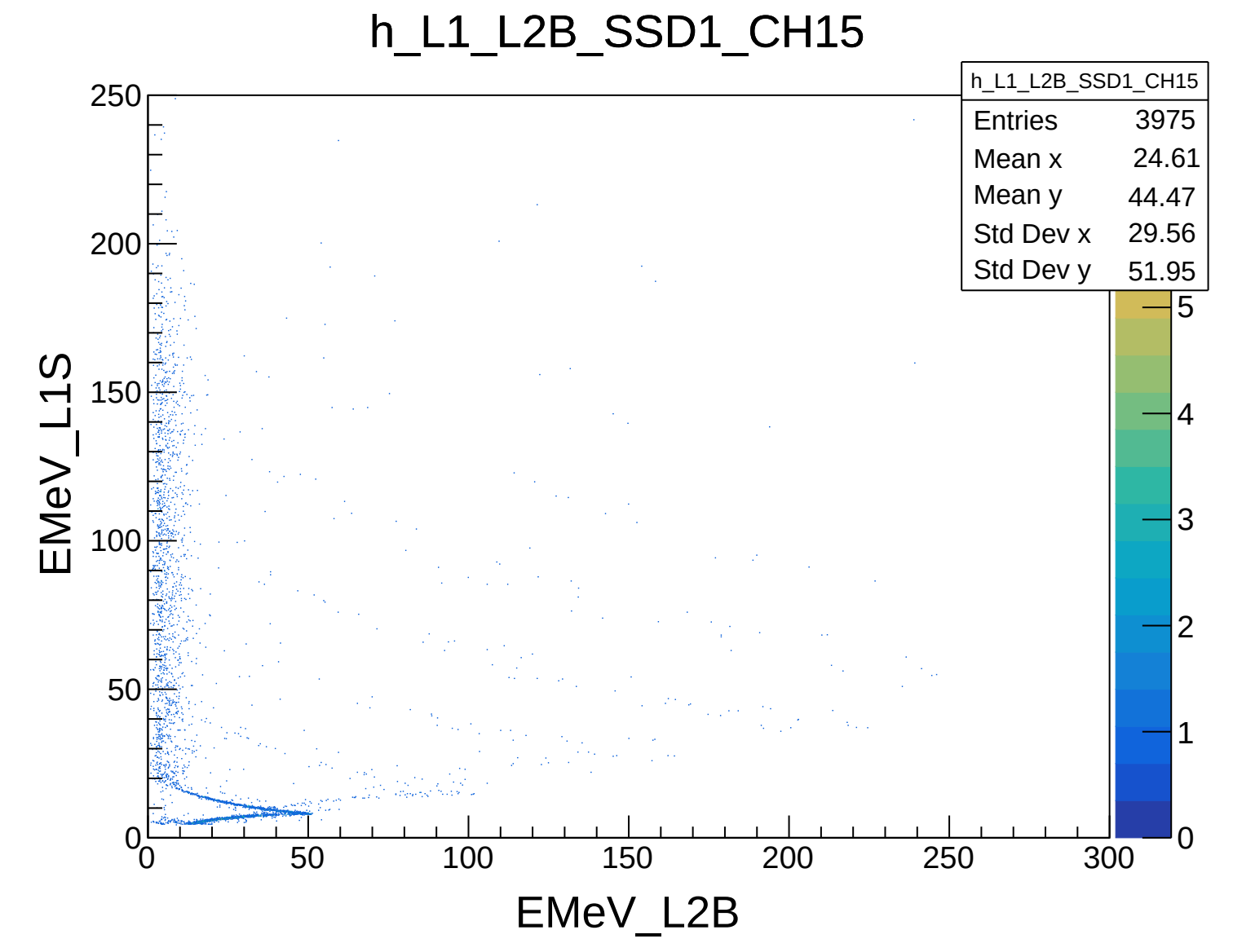
h_L1_L2B_SSD1_CH15
h_L1_L2B_SSD1_CH15
Entries 3975
Mean x 24.61
Mean y 44.47
Std Dev x 29.56
Std Dev y 51.95
EMeV_L1S
EMeV_L2B
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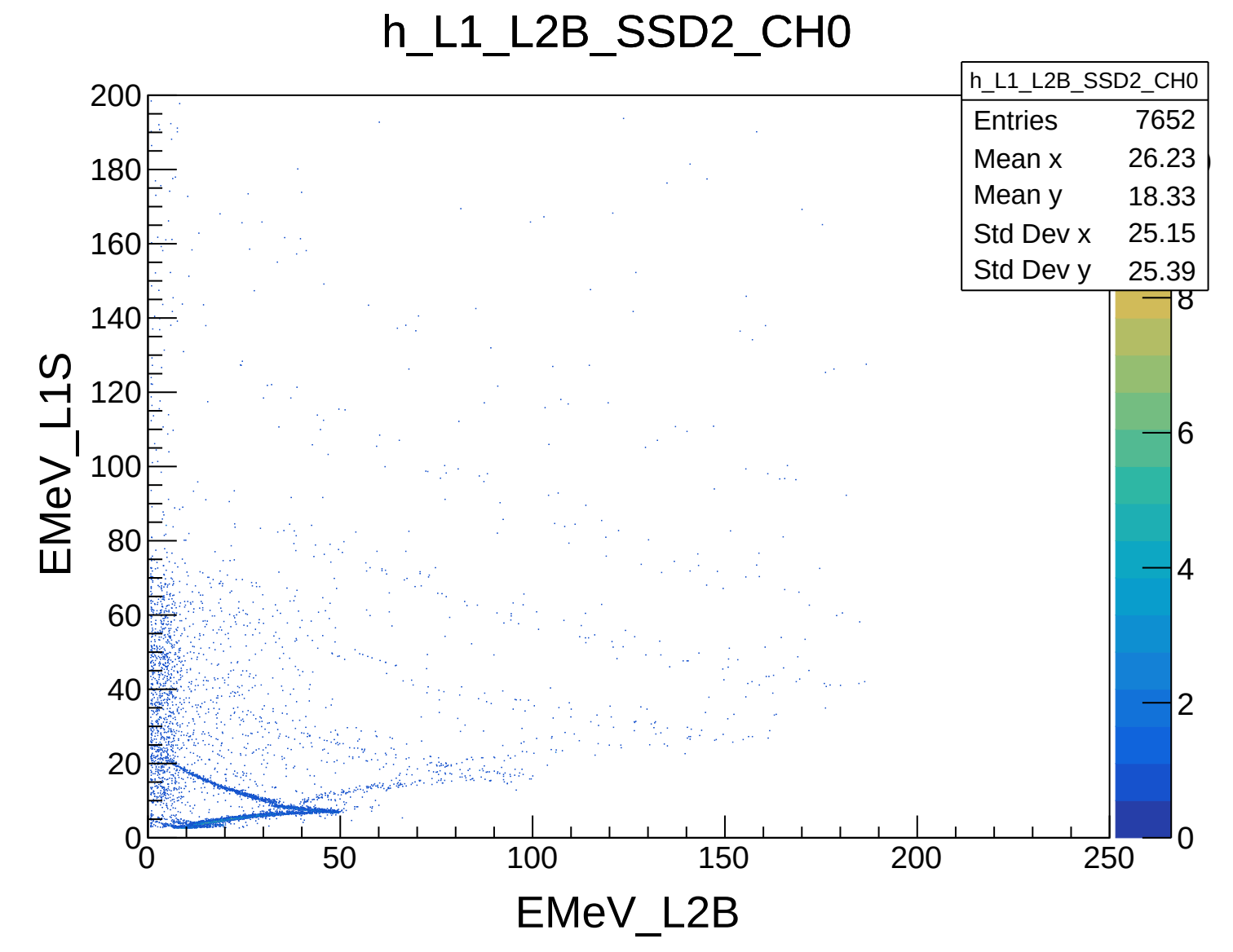
h_L1_L2B_SSD2_CH0
h_L1_L2B_SSD2_CH0
Entries 7652
Mean x 26.23
Mean y 18.33
Std Dev x 25.15
Std Dev y 25.39
EMeV_L1S
EMeV_L2B
0
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6
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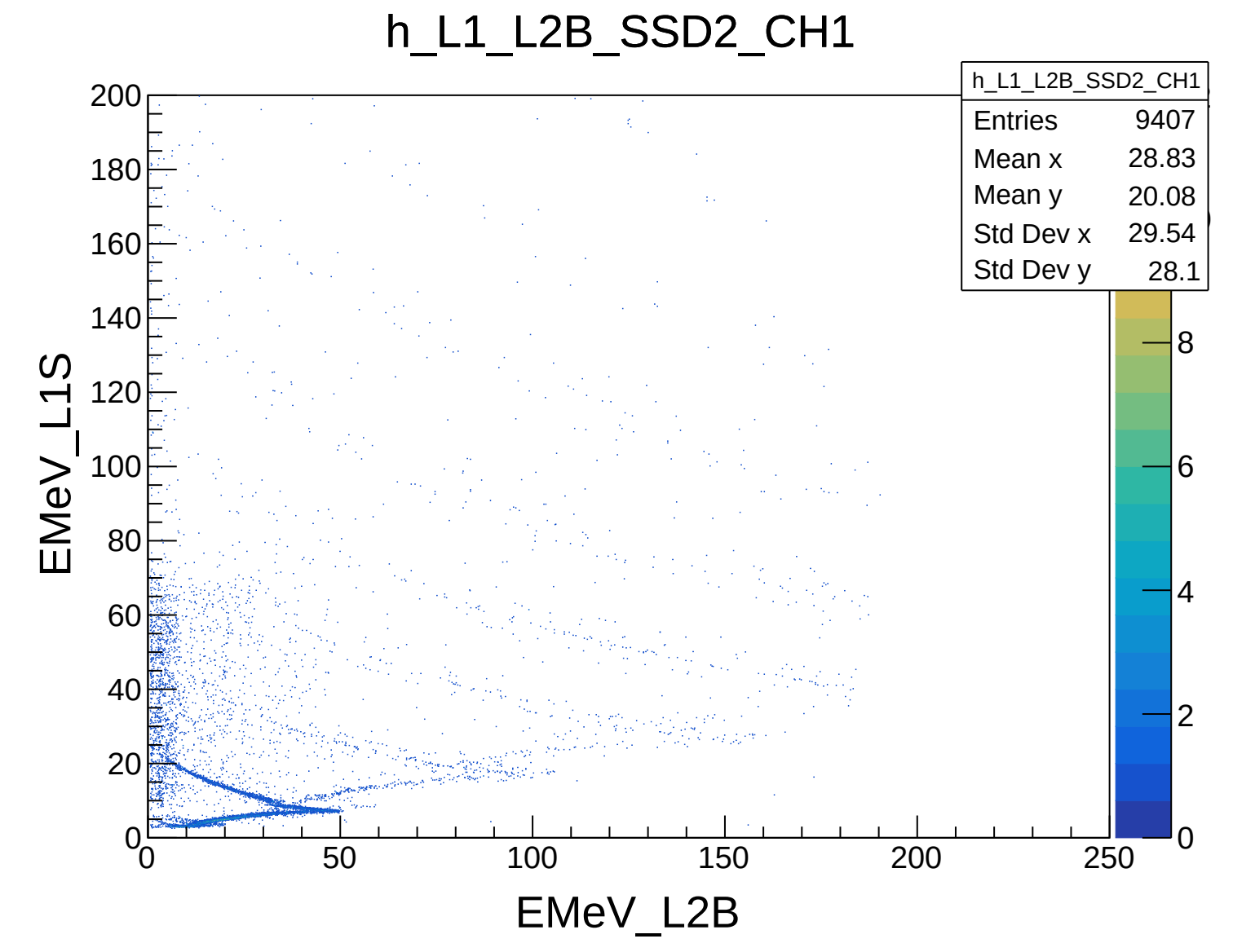
h_L1_L2B_SSD2_CH1
h_L1_L2B_SSD2_CH1
Entries 9407
Mean x 28.83
Mean y 20.08
Std Dev x 29.54
Std Dev y 28.1
EMeV_L1S
EMeV_L2B
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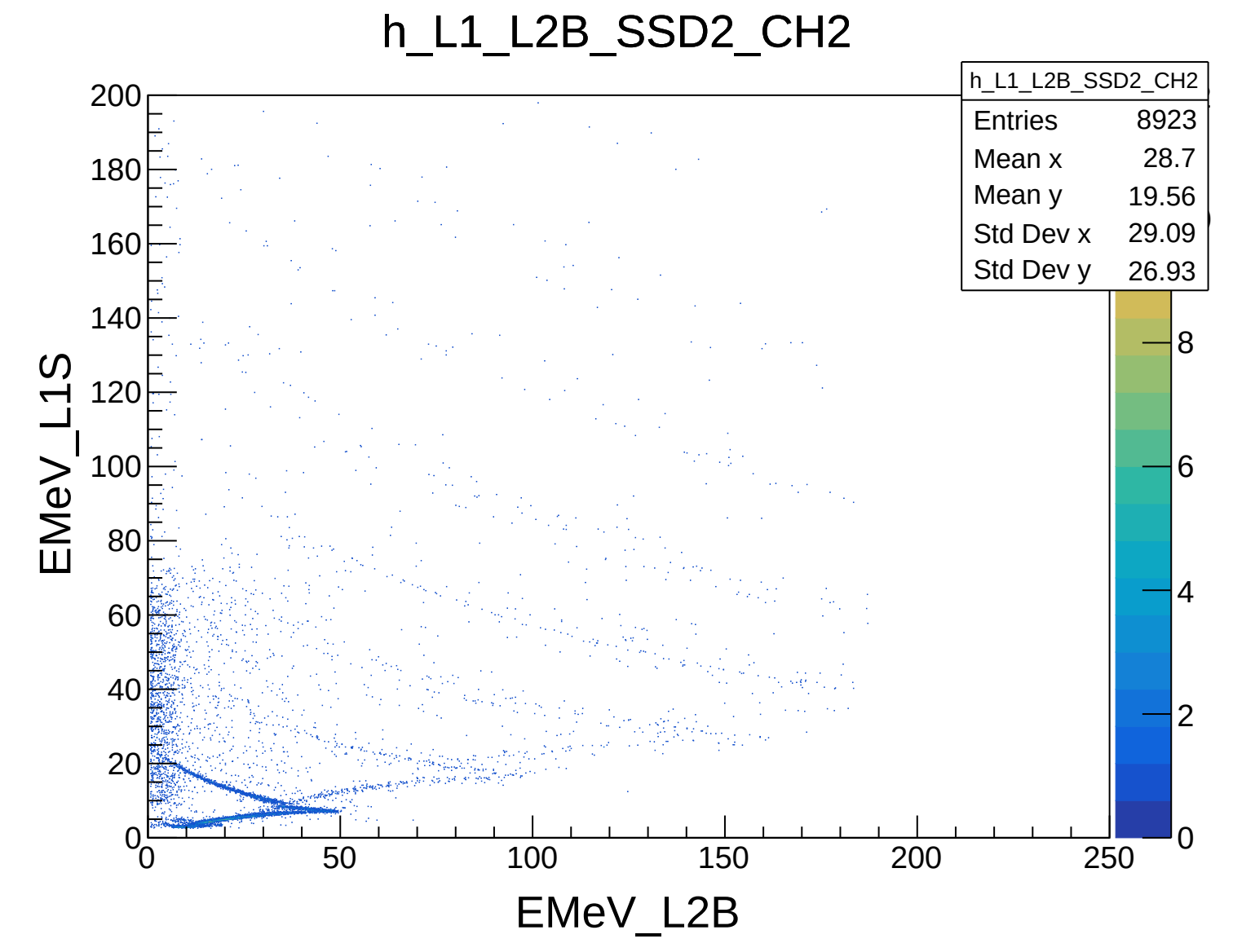
h_L1_L2B_SSD2_CH2
h_L1_L2B_SSD2_CH2
Entries 8923
Mean x 28.7
Mean y 19.56
Std Dev x 29.09
Std Dev y 26.93
EMeV_L1S
EMeV_L2B
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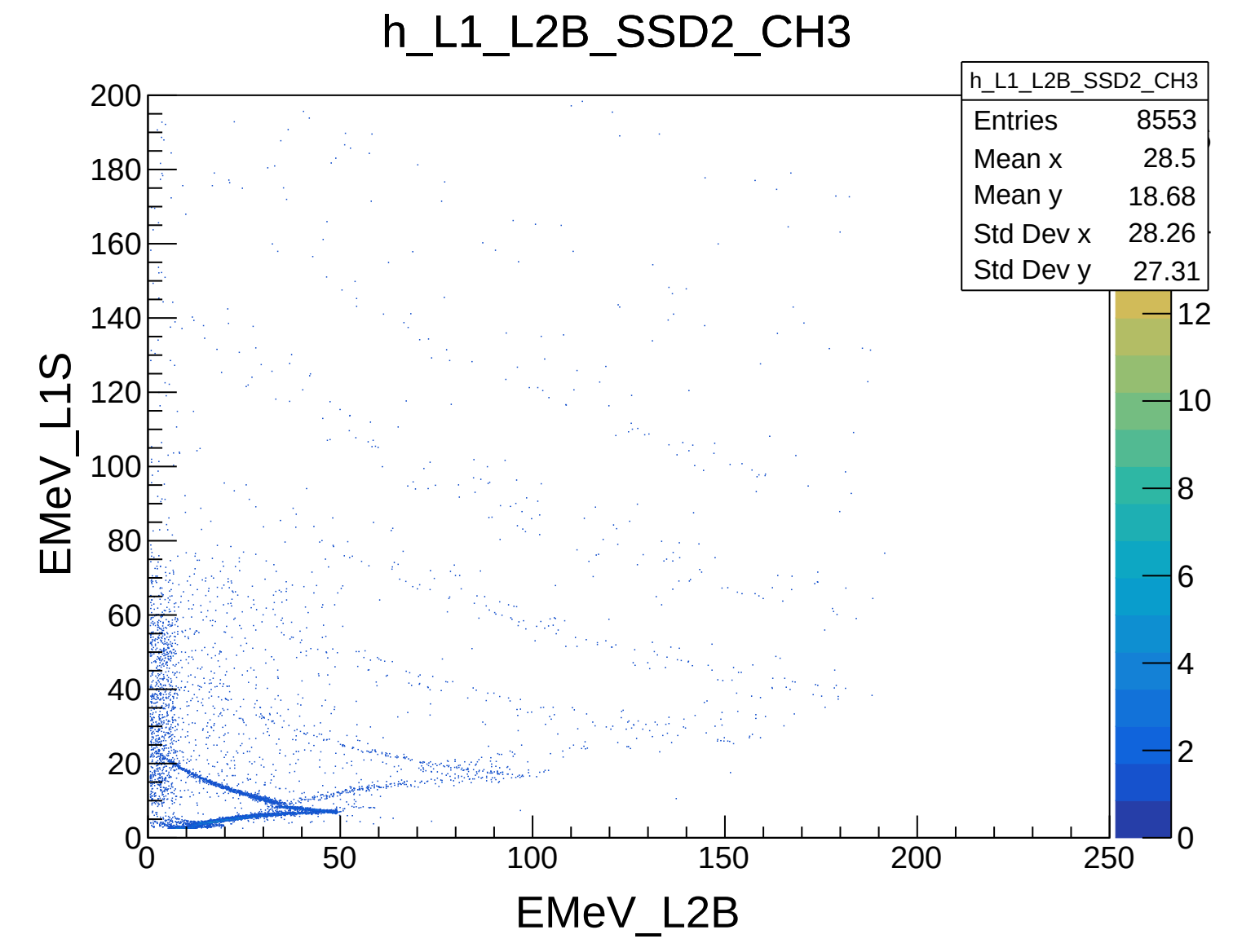
h_L1_L2B_SSD2_CH3
h_L1_L2B_SSD2_CH3
Entries 8553
Mean x 28.5
Mean y 18.68
Std Dev x 28.26
Std Dev y 27.31
EMeV_L1S
EMeV_L2B
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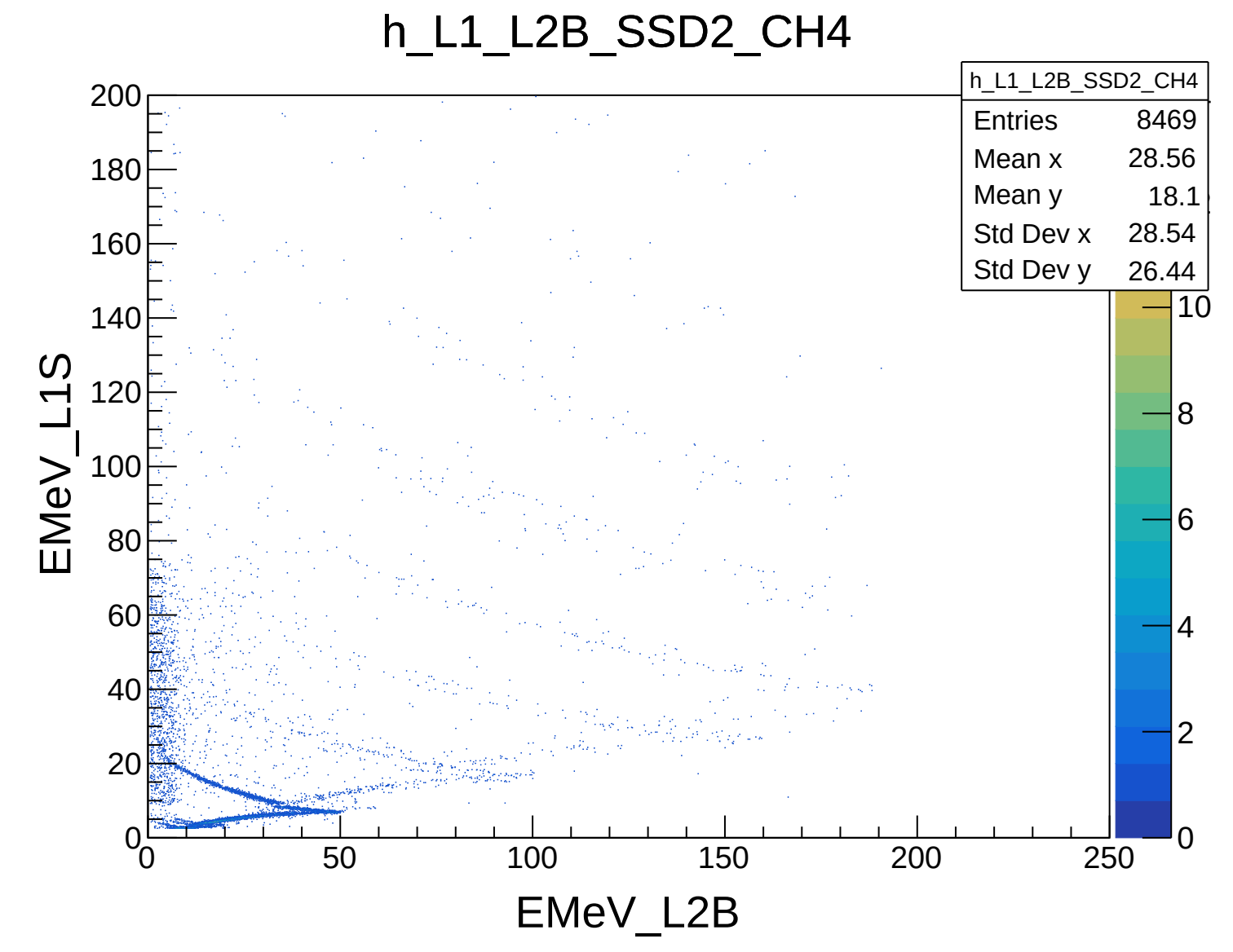
12


h_L1_L2B_SSD2_CH4
h_L1_L2B_SSD2_CH4
Entries 8469
Mean x 28.56
Mean y 18.1
Std Dev x 28.54
Std Dev y 26.44
EMeV_L1S
EMeV_L2B
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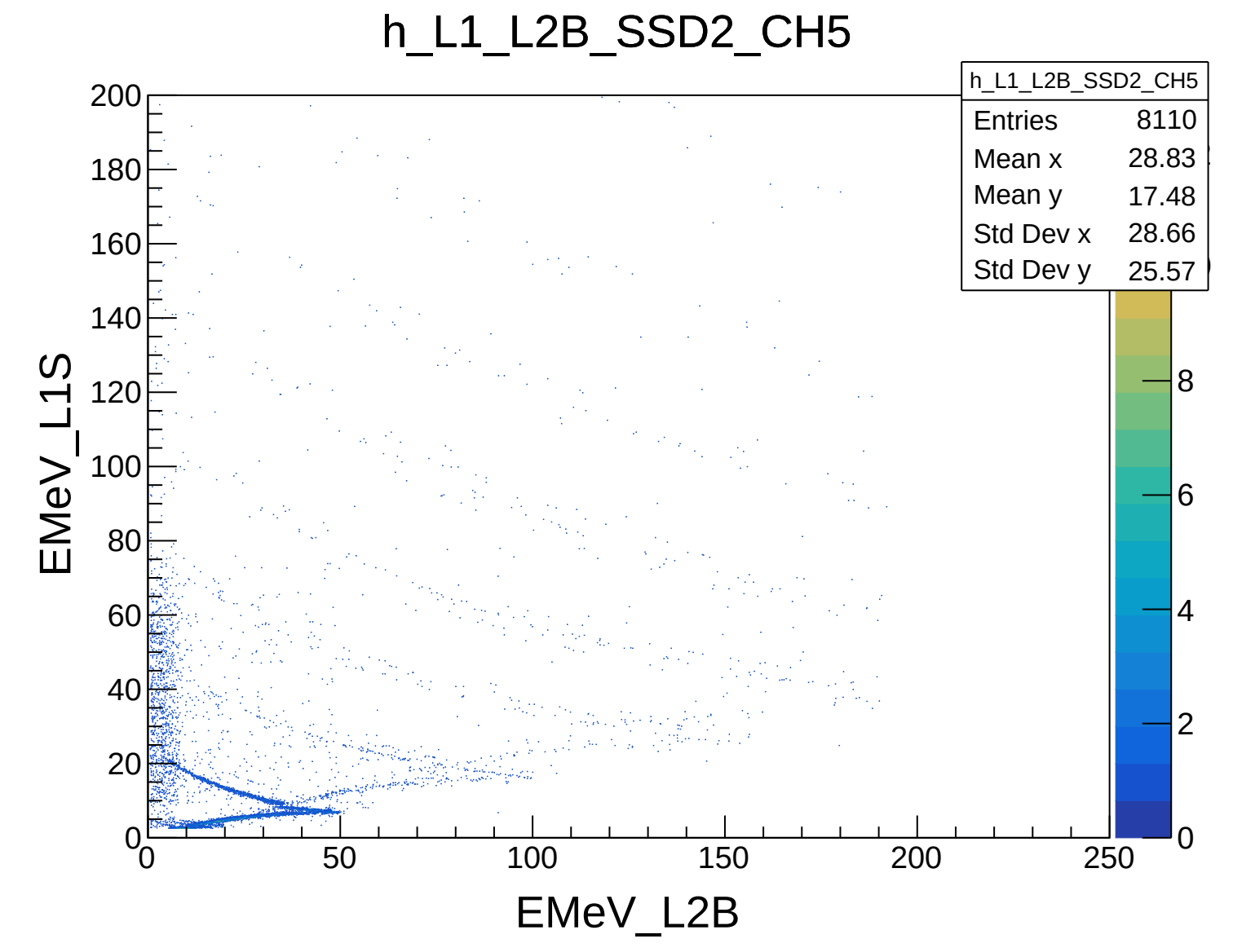
h_L1_L2B_SSD2_CH5
h_L1_L2B_SSD2_CH5
Entries 8110
Mean x 28.83
Mean y 17.48
Std Dev x 28.66
Std Dev y 25.57
EMeV_L1S
EMeV_L2B
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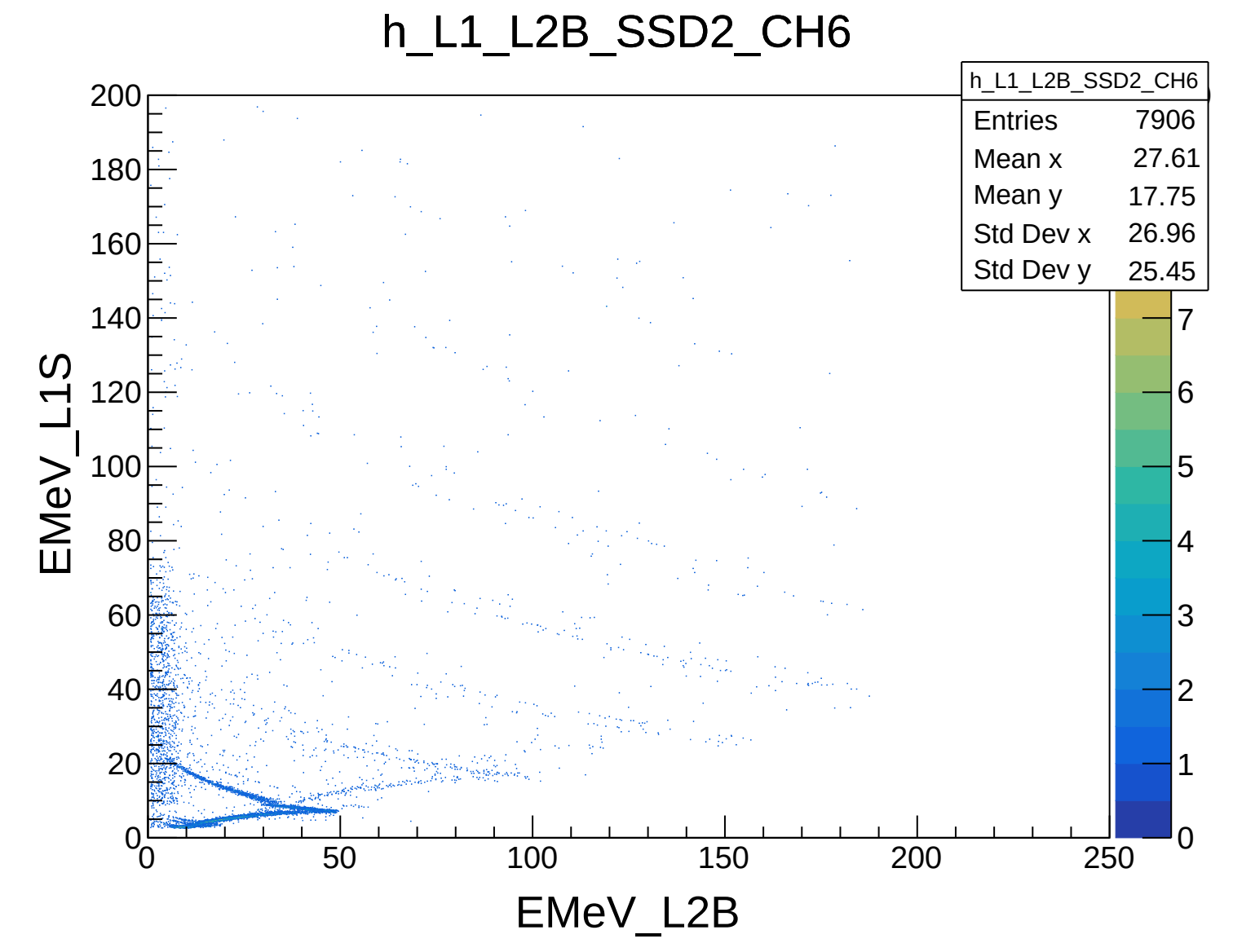
h_L1_L2B_SSD2_CH6
h_L1_L2B_SSD2_CH6
Entries 7906
Mean x 27.61
Mean y 17.75
Std Dev x 26.96
Std Dev y 25.45
EMeV_L1S
EMeV_L2B
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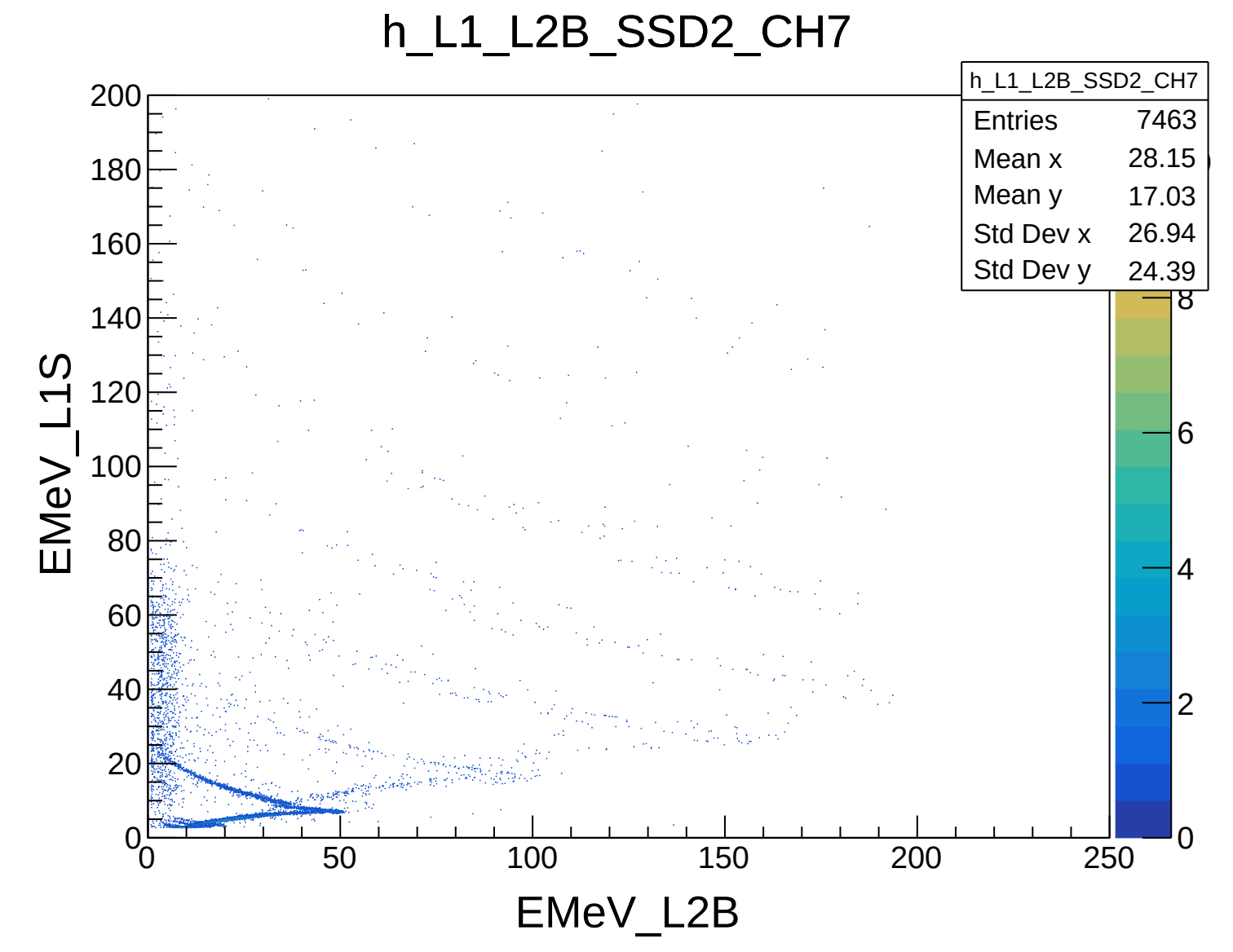
h_L1_L2B_SSD2_CH7
h_L1_L2B_SSD2_CH7
Entries 7463
Mean x 28.15
Mean y 17.03
Std Dev x 26.94
Std Dev y 24.39
EMeV_L1S
EMeV_L2B
0
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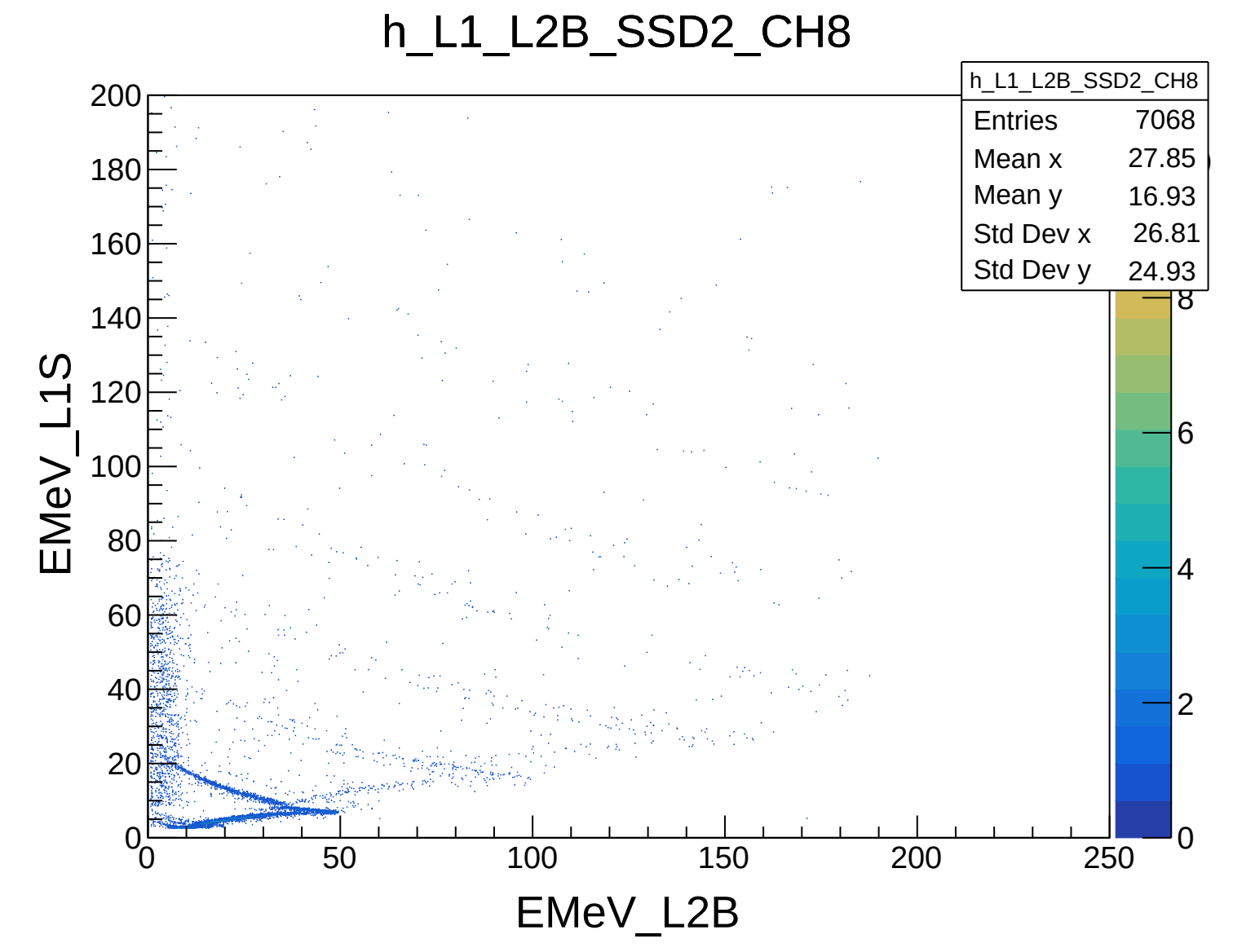
h_L1_L2B_SSD2_CH8
h_L1_L2B_SSD2_CH8
Entries 7068
Mean x 27.85
Mean y 16.93
Std Dev x 26.81
Std Dev y 24.93
EMeV_L1S
EMeV_L2B
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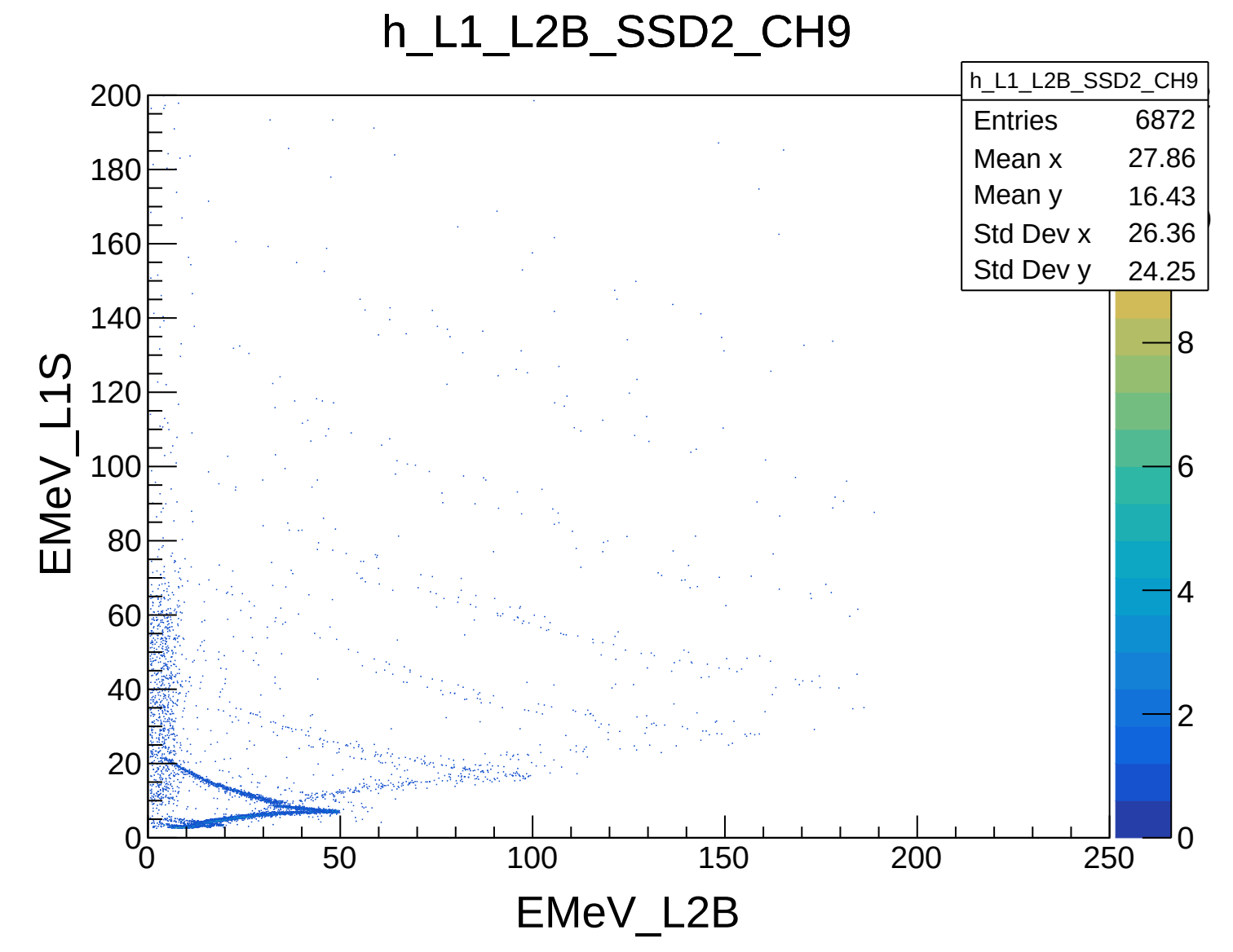
h_L1_L2B_SSD2_CH9
h_L1_L2B_SSD2_CH9
Entries 6872
Mean x 27.86
Mean y 16.43
Std Dev x 26.36
Std Dev y 24.25
EMeV_L1S
EMeV_L2B
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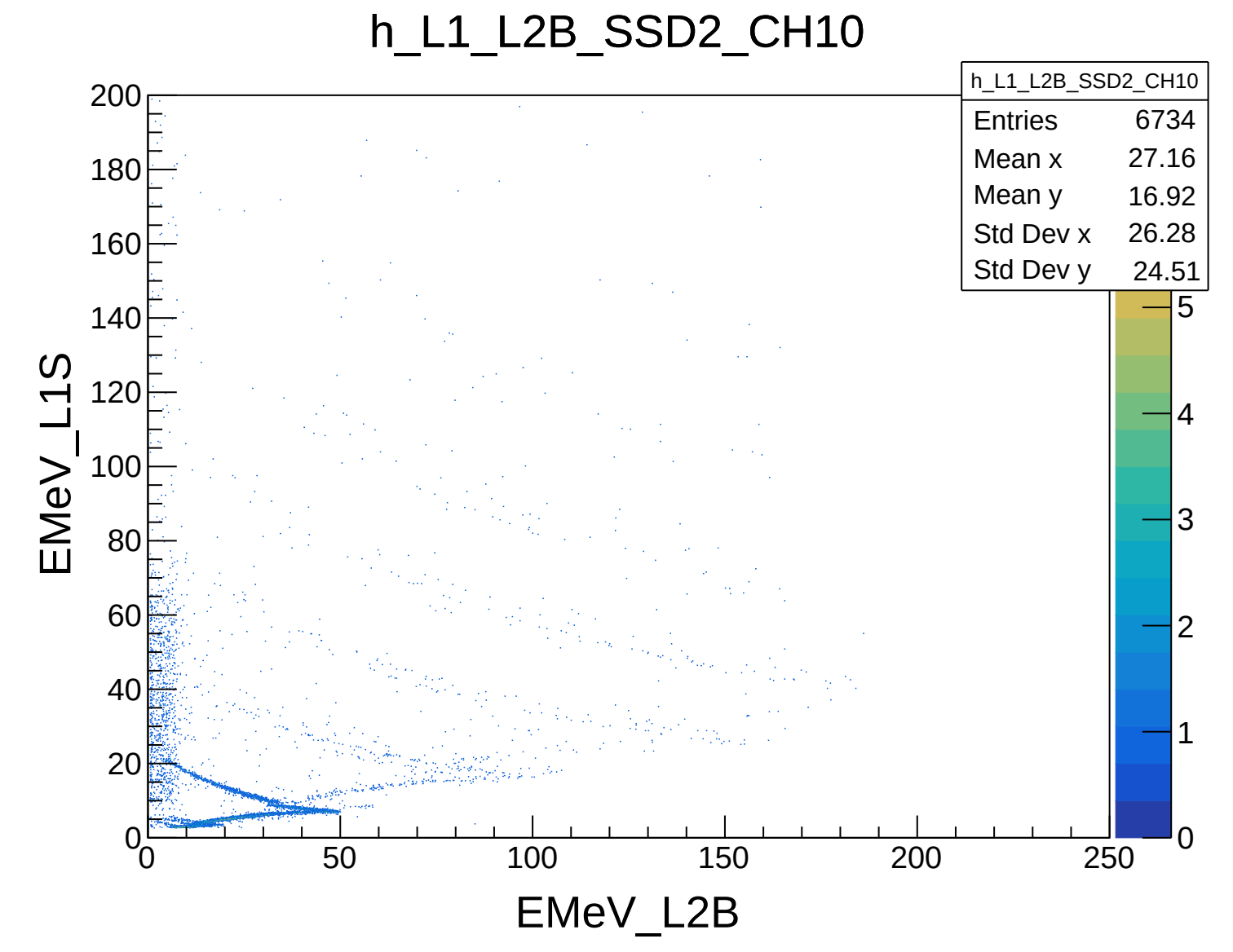
h_L1_L2B_SSD2_CH10
h_L1_L2B_SSD2_CH10
Entries 6734
Mean x 27.16
Mean y 16.92
Std Dev x 26.28
Std Dev y 24.51
EMeV_L1S
EMeV_L2B
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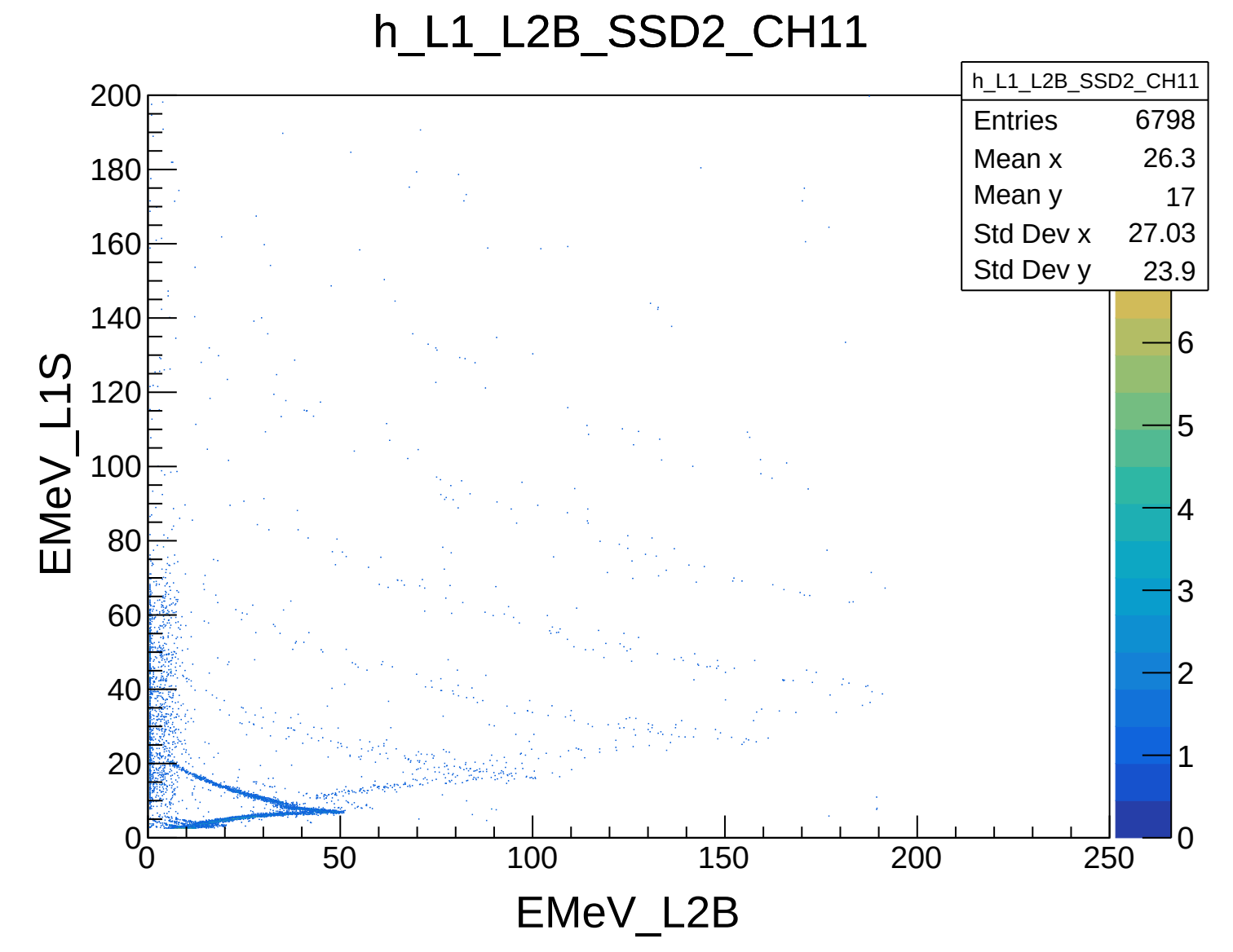
h_L1_L2B_SSD2_CH11
h_L1_L2B_SSD2_CH11
Entries 6798
Mean x 26.3
Mean y 17
Std Dev x 27.03
Std Dev y 23.9
EMeV_L1S
EMeV_L2B
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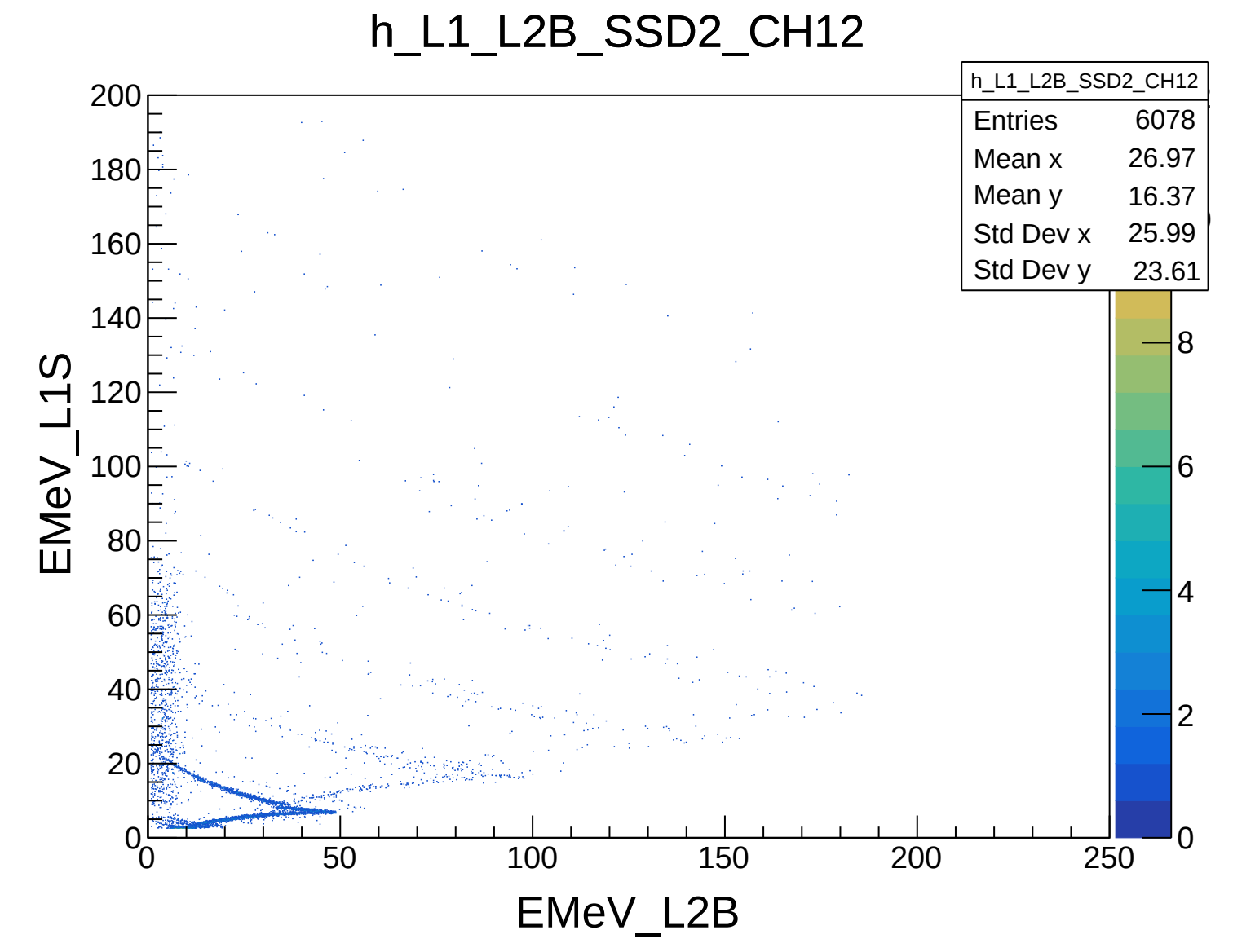
h_L1_L2B_SSD2_CH12
h_L1_L2B_SSD2_CH12
Entries 6078
Mean x 26.97
Mean y 16.37
Std Dev x 25.99
Std Dev y 23.61
EMeV_L1S
EMeV_L2B
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80
100
120
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160
180
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50
100
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2
4
6
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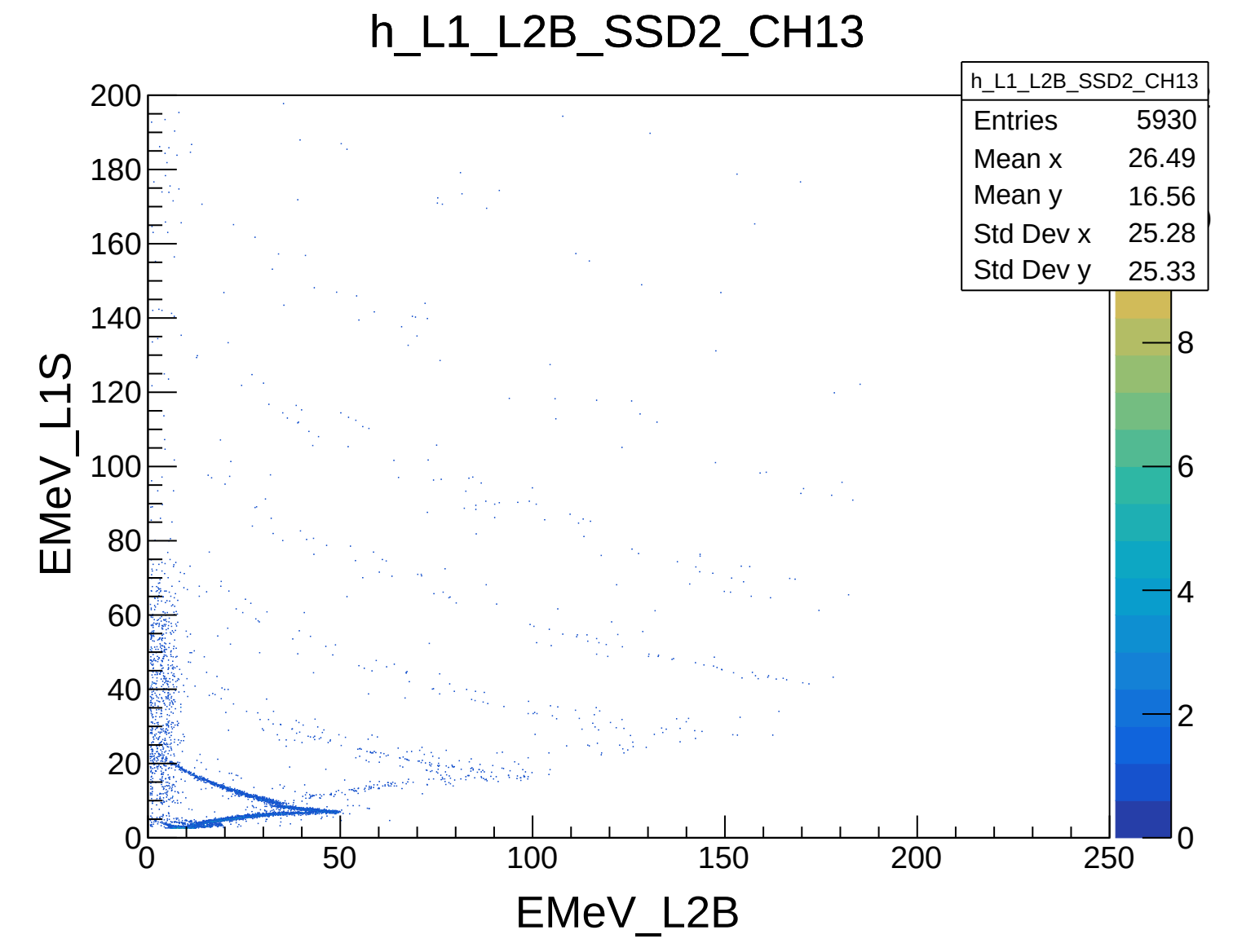
h_L1_L2B_SSD2_CH13
h_L1_L2B_SSD2_CH13
Entries 5930
Mean x 26.49
Mean y 16.56
Std Dev x 25.28
Std Dev y 25.33
EMeV_L1S
EMeV_L2B
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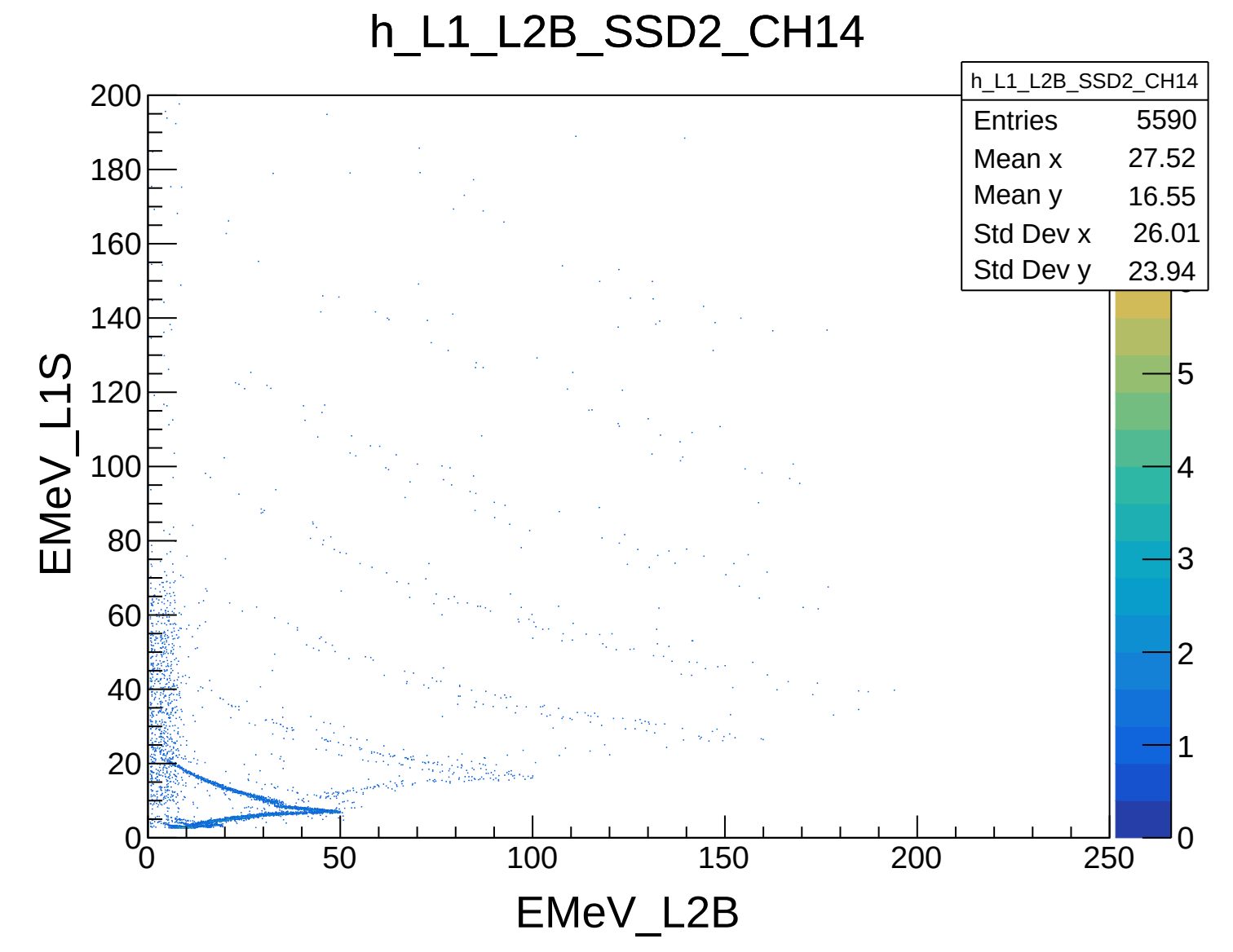
h_L1_L2B_SSD2_CH14
h_L1_L2B_SSD2_CH14
Entries 5590
Mean x 27.52
Mean y 16.55
Std Dev x 26.01
Std Dev y 23.94
EMeV_L1S
EMeV_L2B
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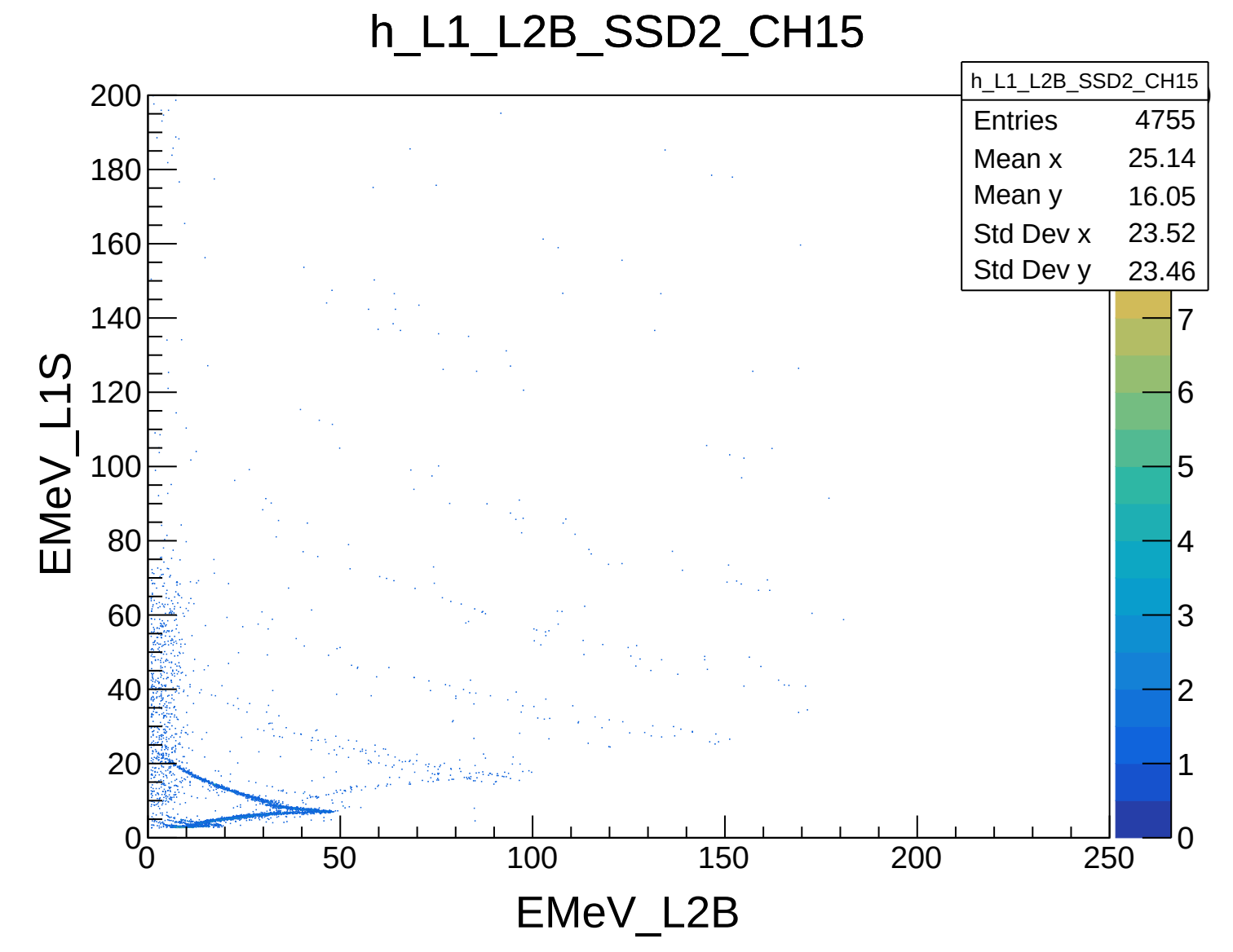
h_L1_L2B_SSD2_CH15
h_L1_L2B_SSD2_CH15
Entries 4755
Mean x 25.14
Mean y 16.05
Std Dev x 23.52
Std Dev y 23.46
EMeV_L1S
EMeV_L2B
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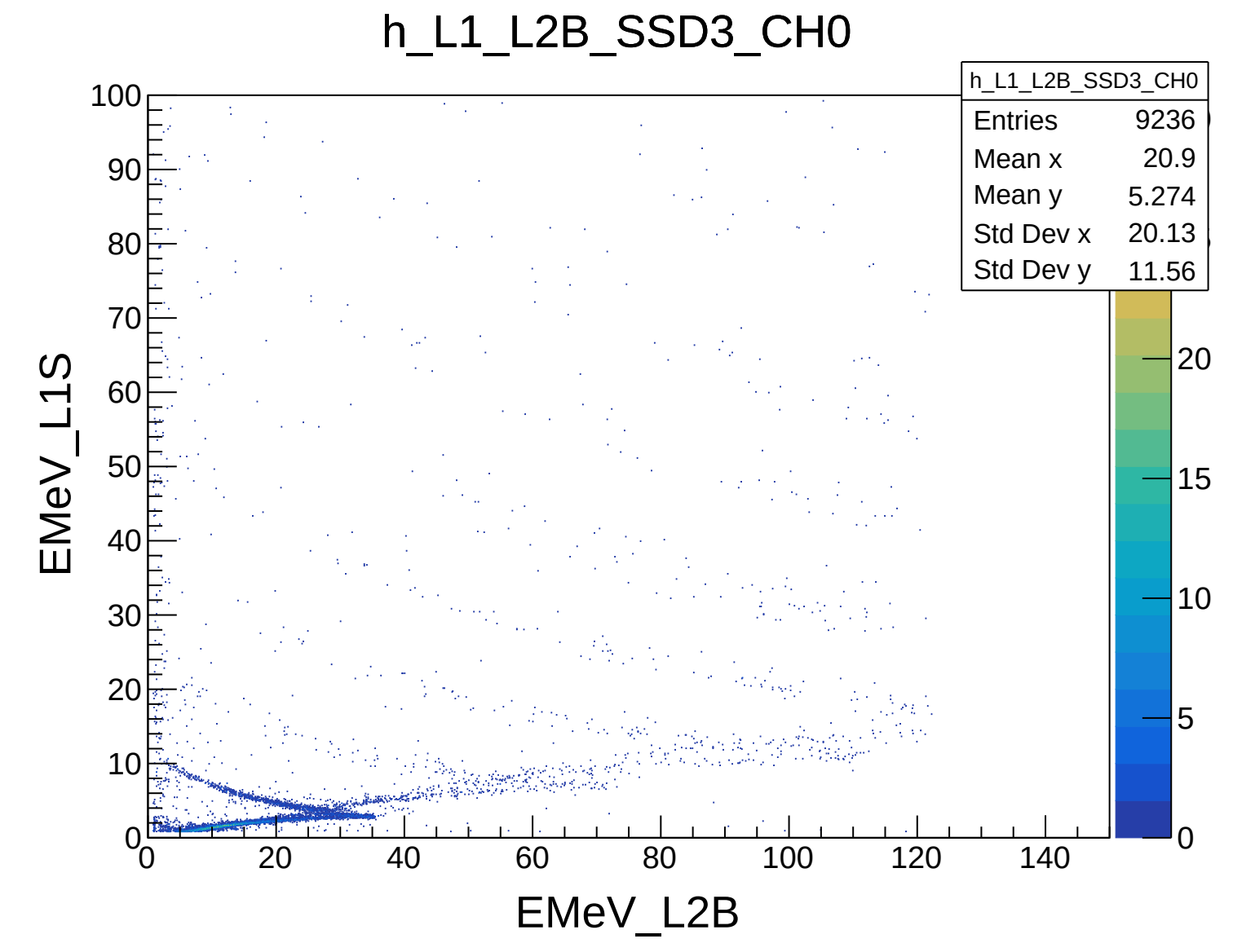
h_L1_L2B_SSD3_CH0
h_L1_L2B_SSD3_CH0
Entries 9236
Mean x 20.9
Mean y 5.274
Std Dev x 20.13
Std Dev y 11.56
EMeV_L1S
EMeV_L2B
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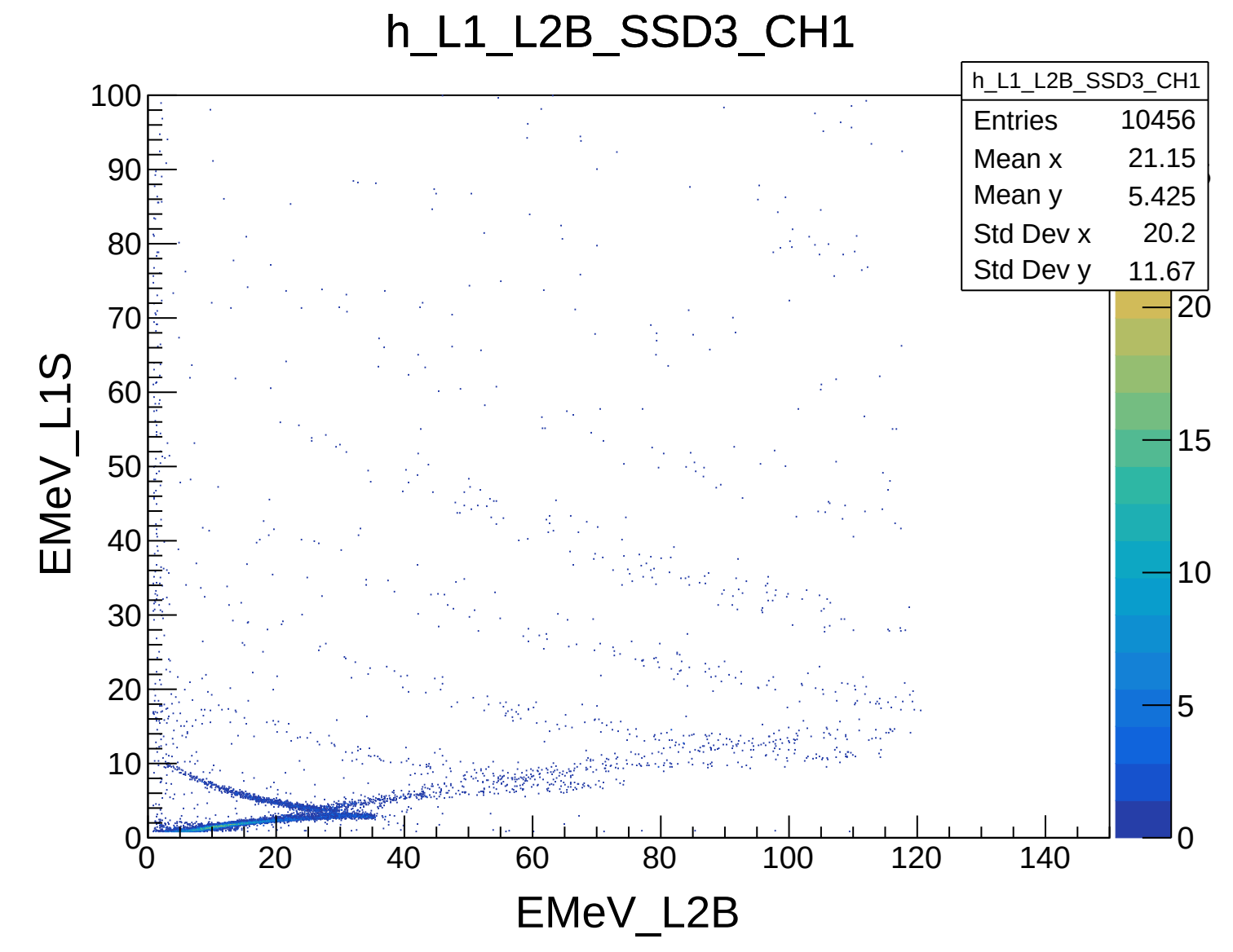
h_L1_L2B_SSD3_CH1
h_L1_L2B_SSD3_CH1
Entries 10456
Mean x 21.15
Mean y 5.425
Std Dev x 20.2
Std Dev y 11.67
EMeV_L1S
EMeV_L2B
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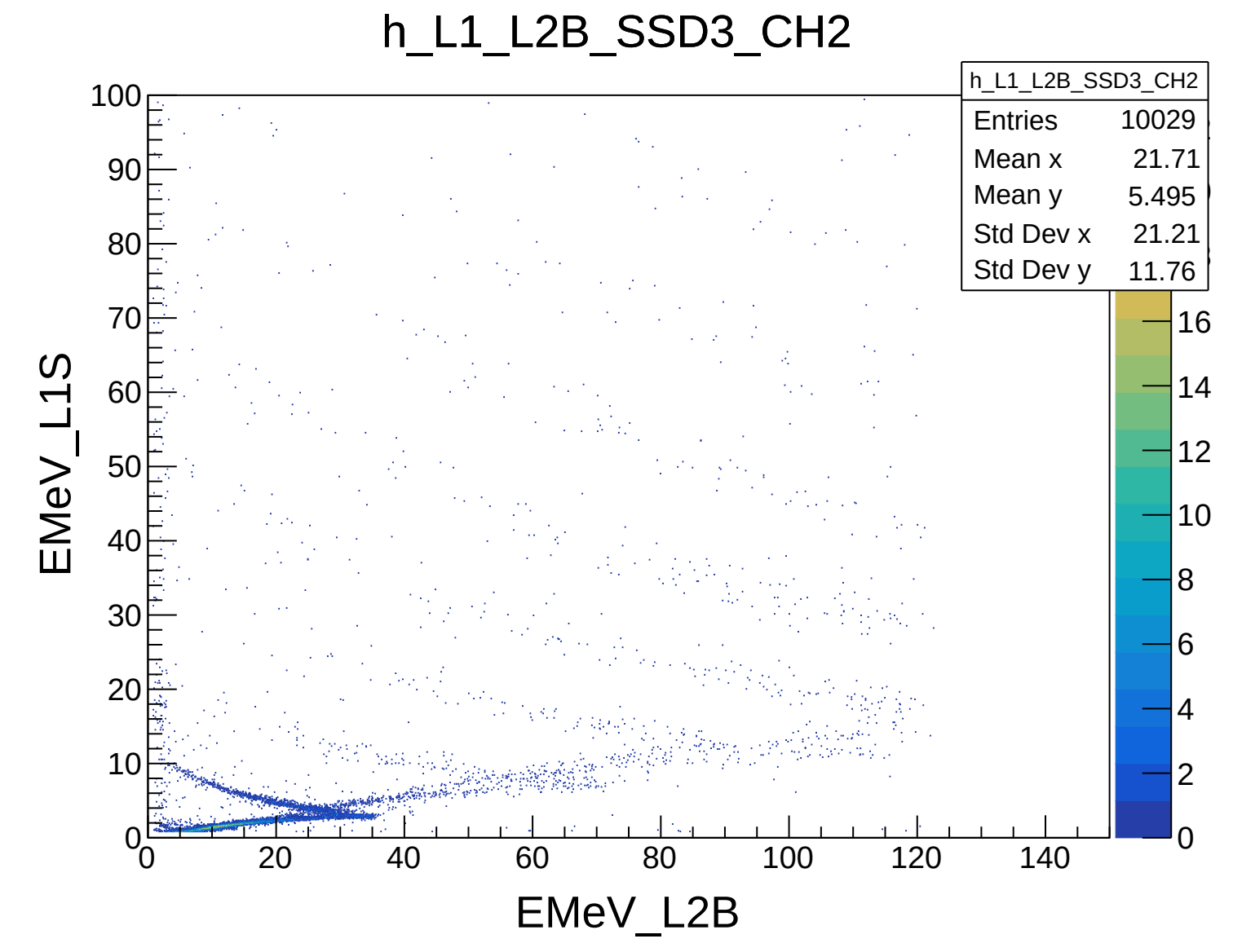
h_L1_L2B_SSD3_CH2
h_L1_L2B_SSD3_CH2
Entries 10029
Mean x 21.71
Mean y 5.495
Std Dev x 21.21
Std Dev y 11.76
EMeV_L1S
EMeV_L2B
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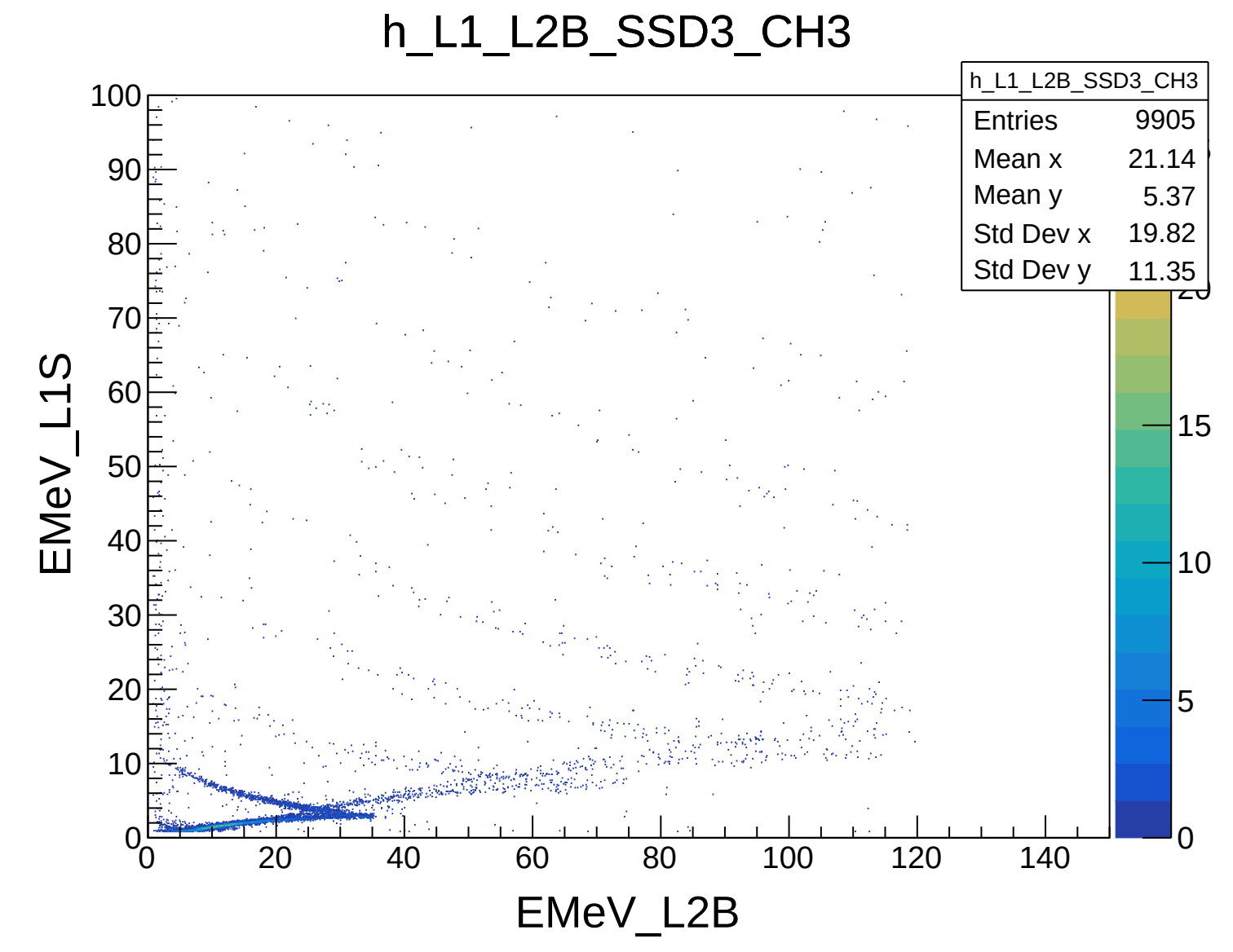
h_L1_L2B_SSD3_CH3
h_L1_L2B_SSD3_CH3
Entries 9905
Mean x 21.14
Mean y 5.37
Std Dev x 19.82
Std Dev y 11.35
EMeV_L1S
EMeV_L2B
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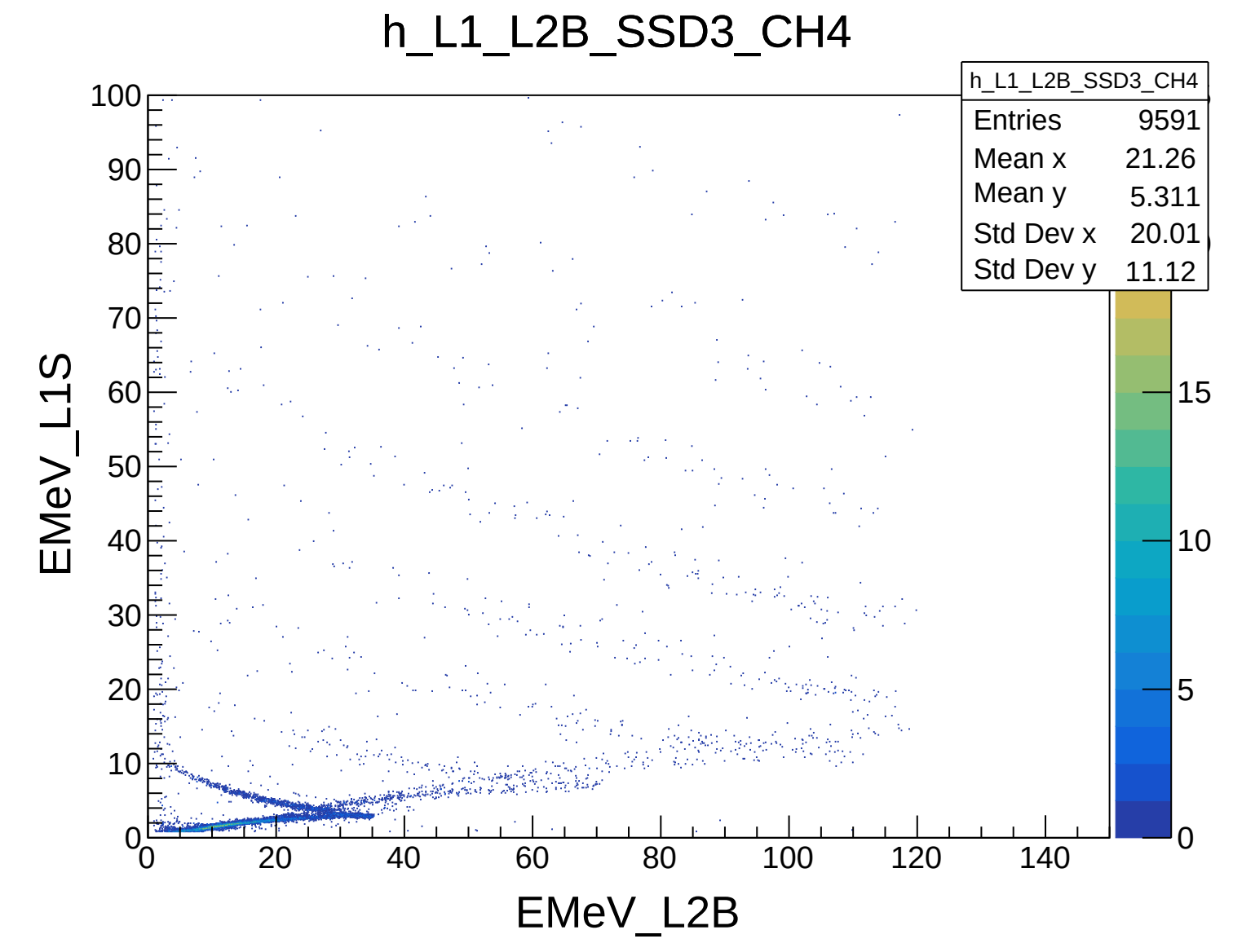
h_L1_L2B_SSD3_CH4
h_L1_L2B_SSD3_CH4
Entries 9591
Mean x 21.26
Mean y 5.311
Std Dev x 20.01
Std Dev y 11.12
EMeV_L1S
EMeV_L2B
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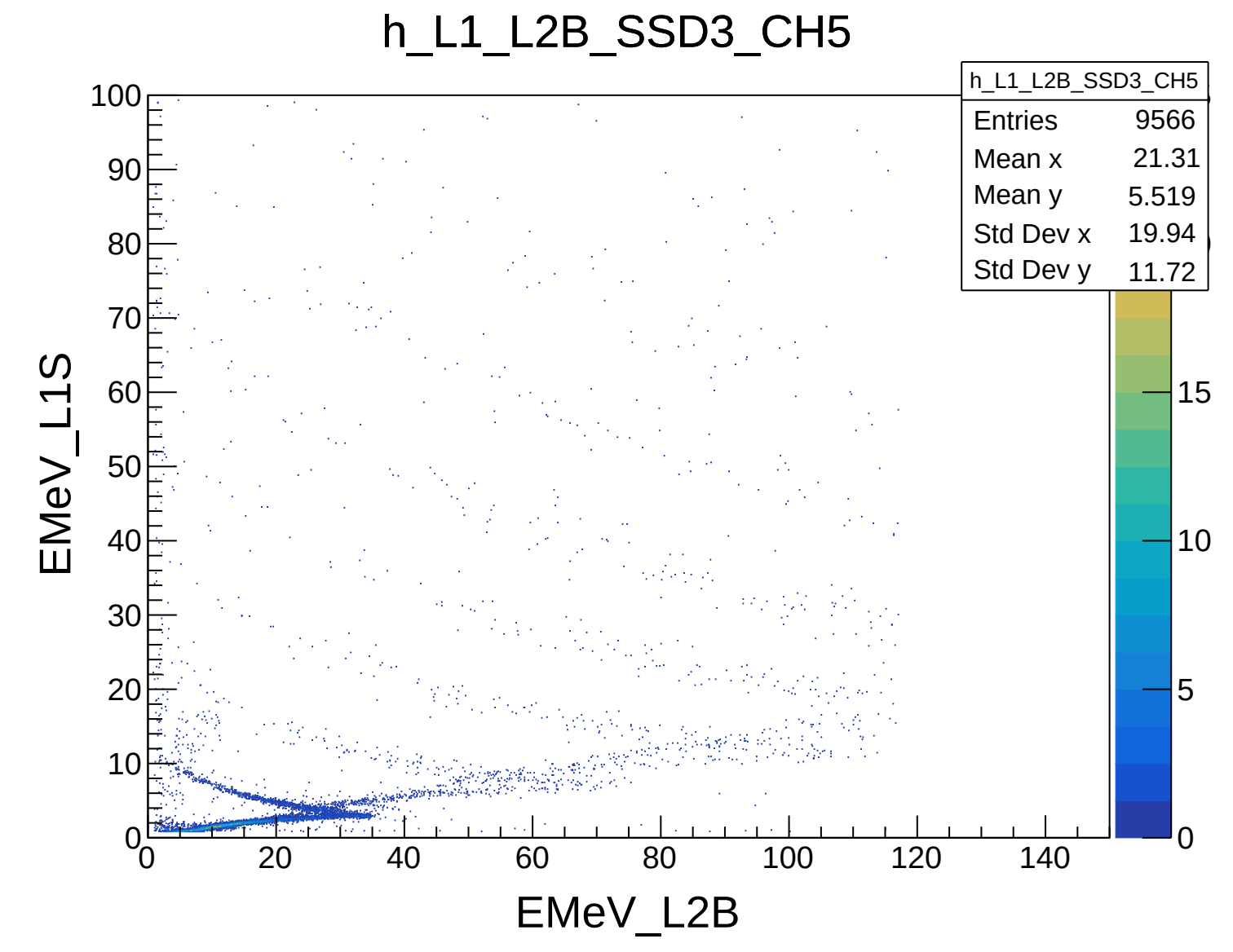
h_L1_L2B_SSD3_CH5
h_L1_L2B_SSD3_CH5
Entries 9566
Mean x 21.31
Mean y 5.519
Std Dev x 19.94
Std Dev y 11.72
EMeV_L1S
EMeV_L2B
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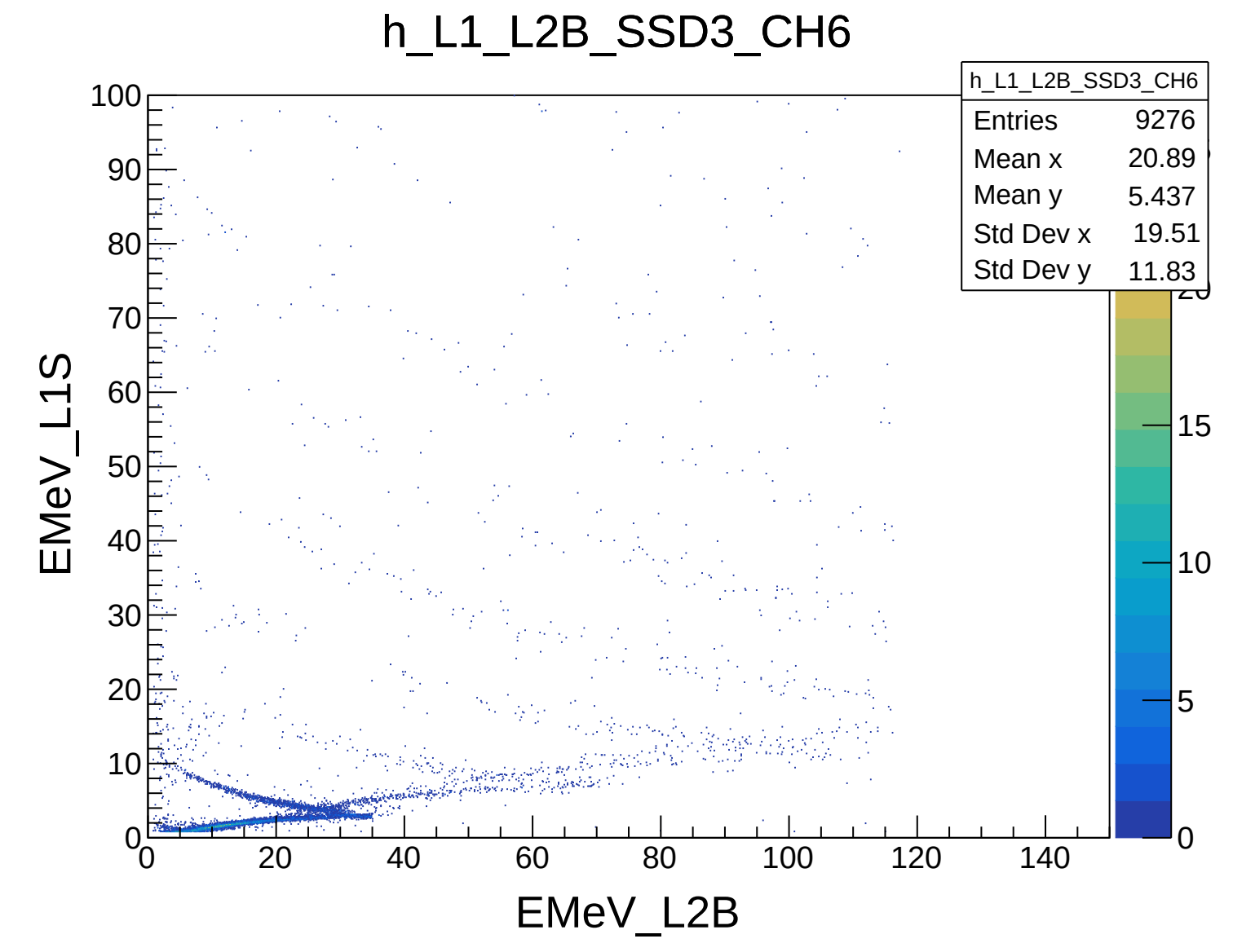
h_L1_L2B_SSD3_CH6
h_L1_L2B_SSD3_CH6
Entries 9276
Mean x 20.89
Mean y 5.437
Std Dev x 19.51
Std Dev y 11.83
EMeV_L1S
EMeV_L2B
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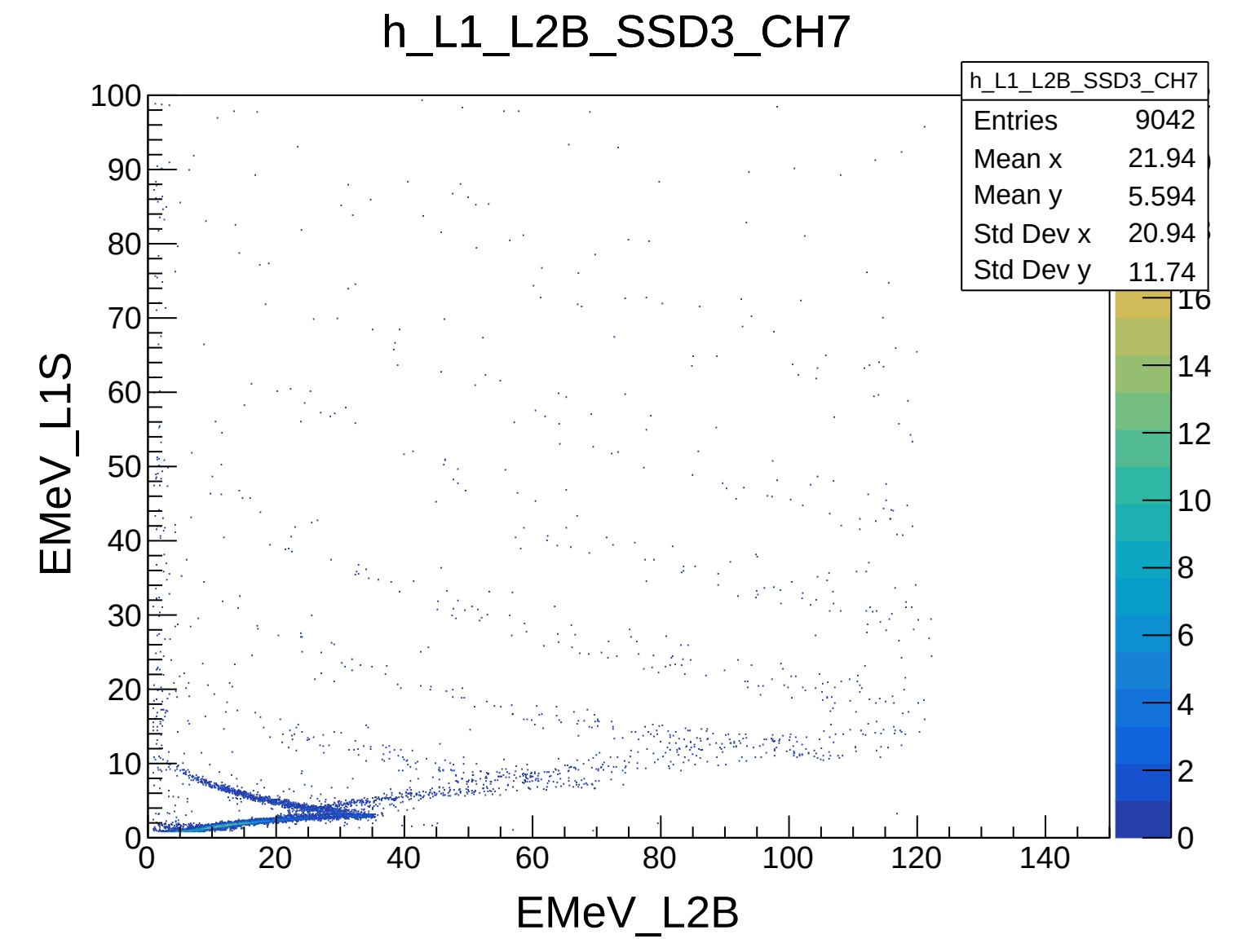
h_L1_L2B_SSD3_CH7
h_L1_L2B_SSD3_CH7
Entries 9042
Mean x 21.94
Mean y 5.594
Std Dev x 20.94
Std Dev y 11.74
EMeV_L1S
EMeV_L2B
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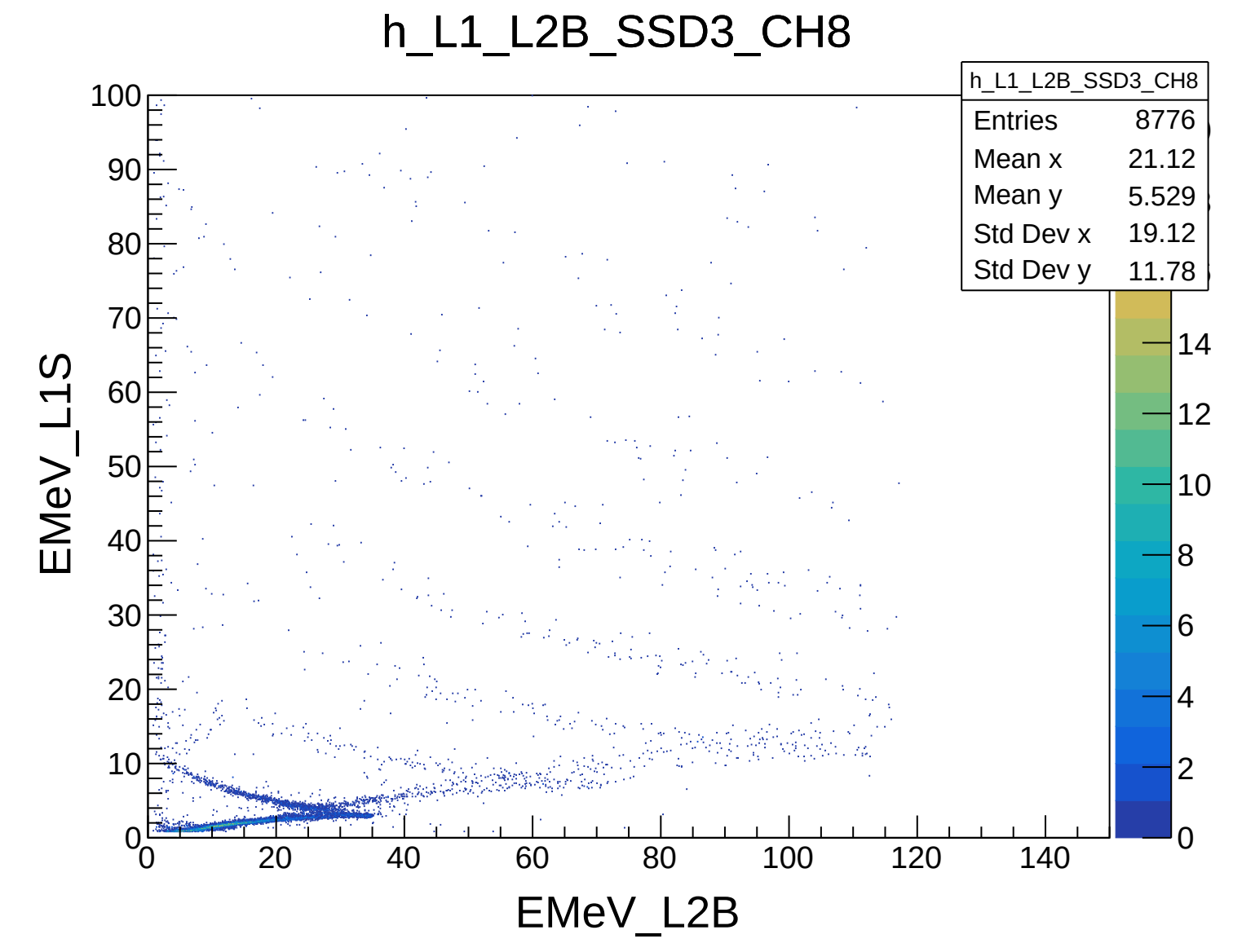
h_L1_L2B_SSD3_CH8
h_L1_L2B_SSD3_CH8
Entries 8776
Mean x 21.12
Mean y 5.529
Std Dev x 19.12
Std Dev y 11.78
EMeV_L1S
EMeV_L2B
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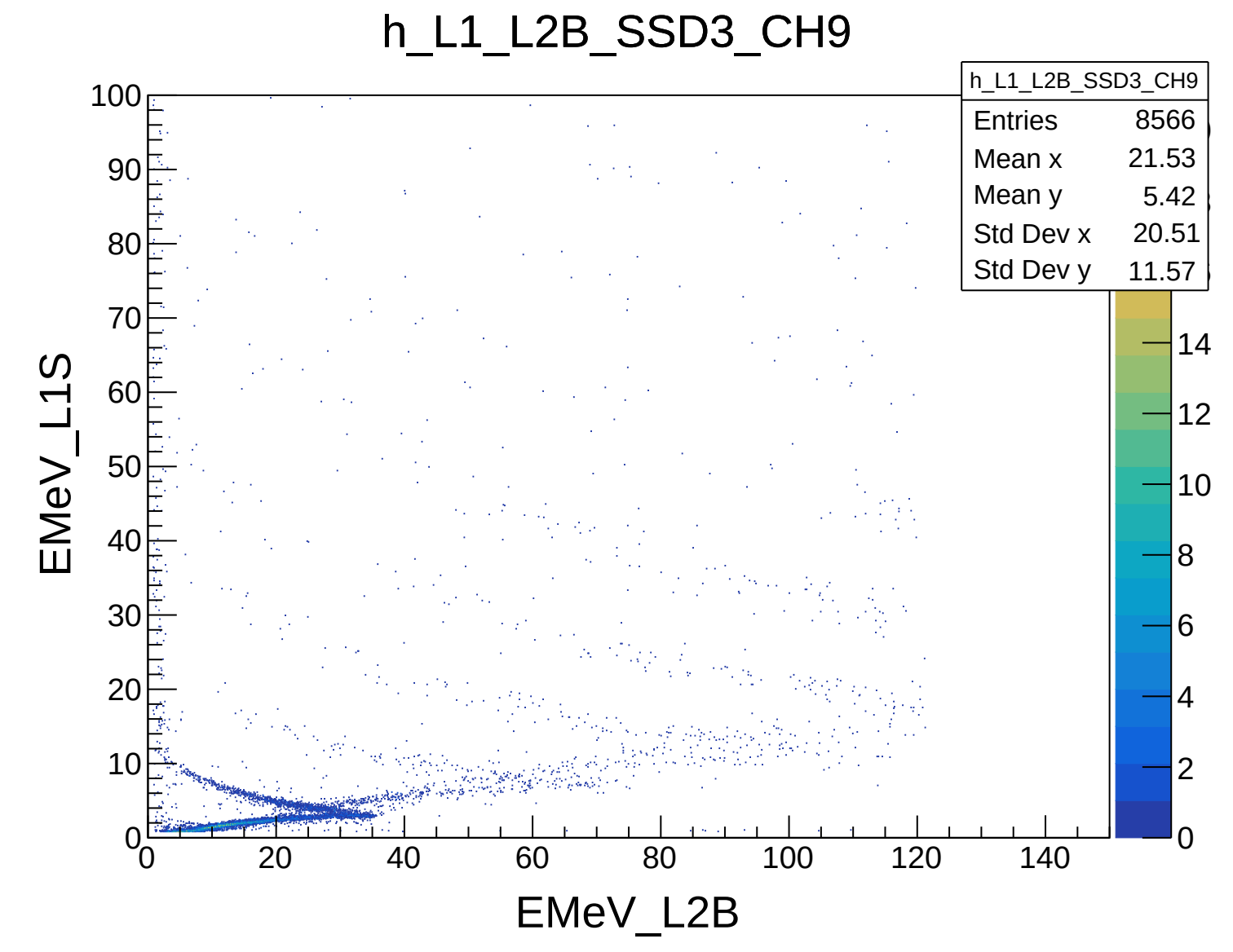
h_L1_L2B_SSD3_CH9
h_L1_L2B_SSD3_CH9
Entries 8566
Mean x 21.53
Mean y 5.42
Std Dev x 20.51
Std Dev y 11.57
EMeV_L1S
EMeV_L2B
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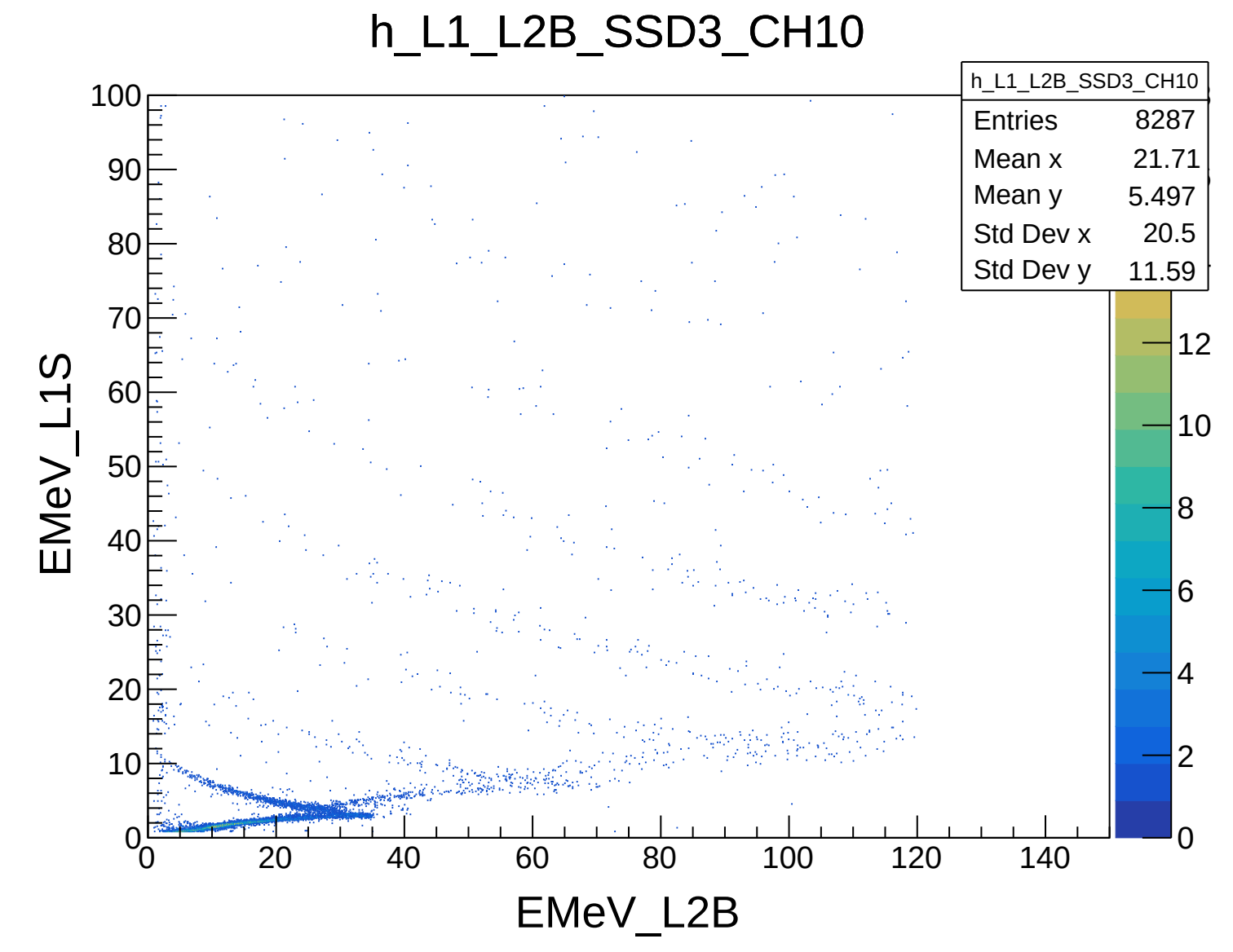
h_L1_L2B_SSD3_CH10
h_L1_L2B_SSD3_CH10
Entries 8287
Mean x 21.71
Mean y 5.497
Std Dev x 20.5
Std Dev y 11.59
EMeV_L1S
EMeV_L2B
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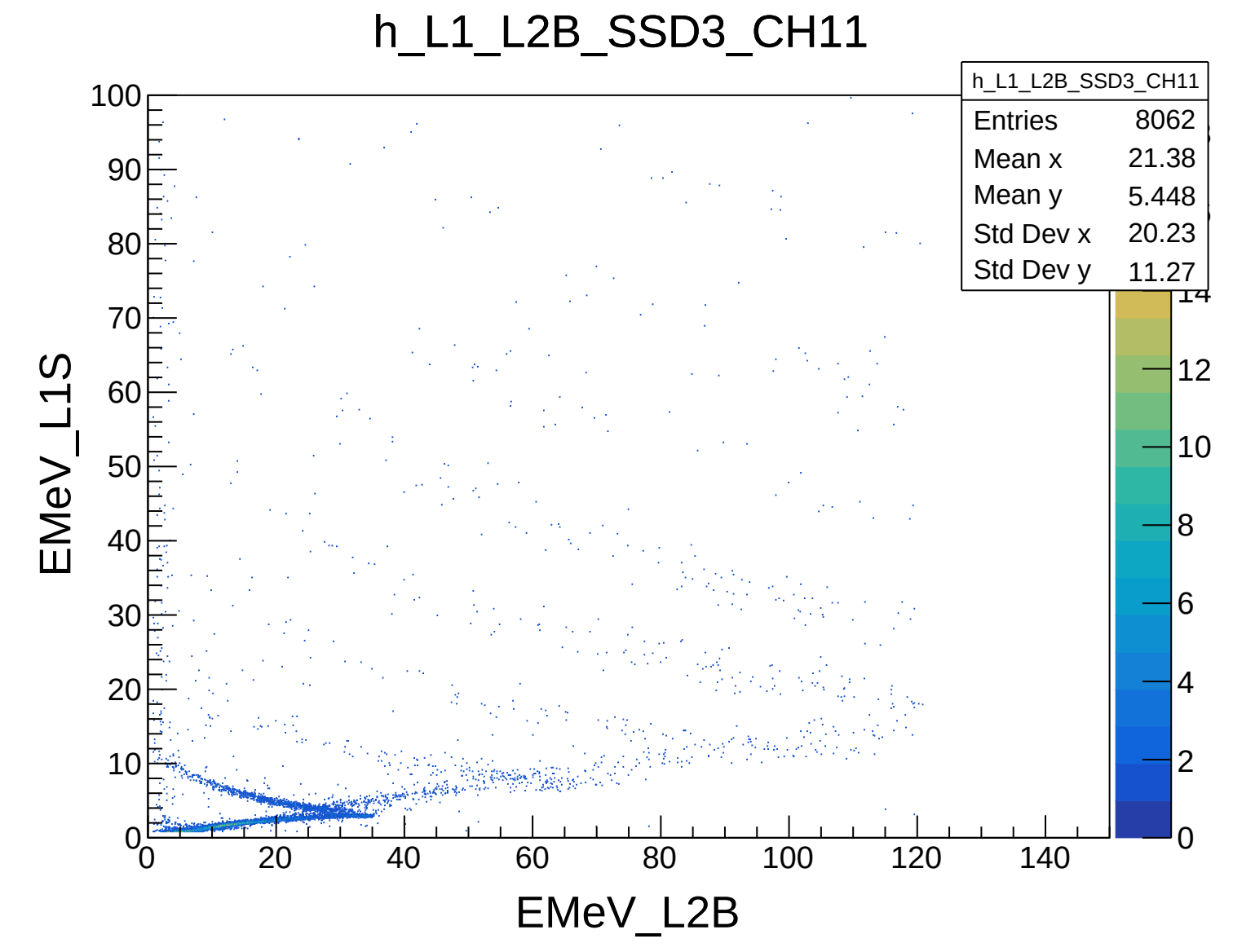
h_L1_L2B_SSD3_CH11
h_L1_L2B_SSD3_CH11
Entries 8062
Mean x 21.38
Mean y 5.448
Std Dev x 20.23
Std Dev y 11.27
EMeV_L1S
EMeV_L2B
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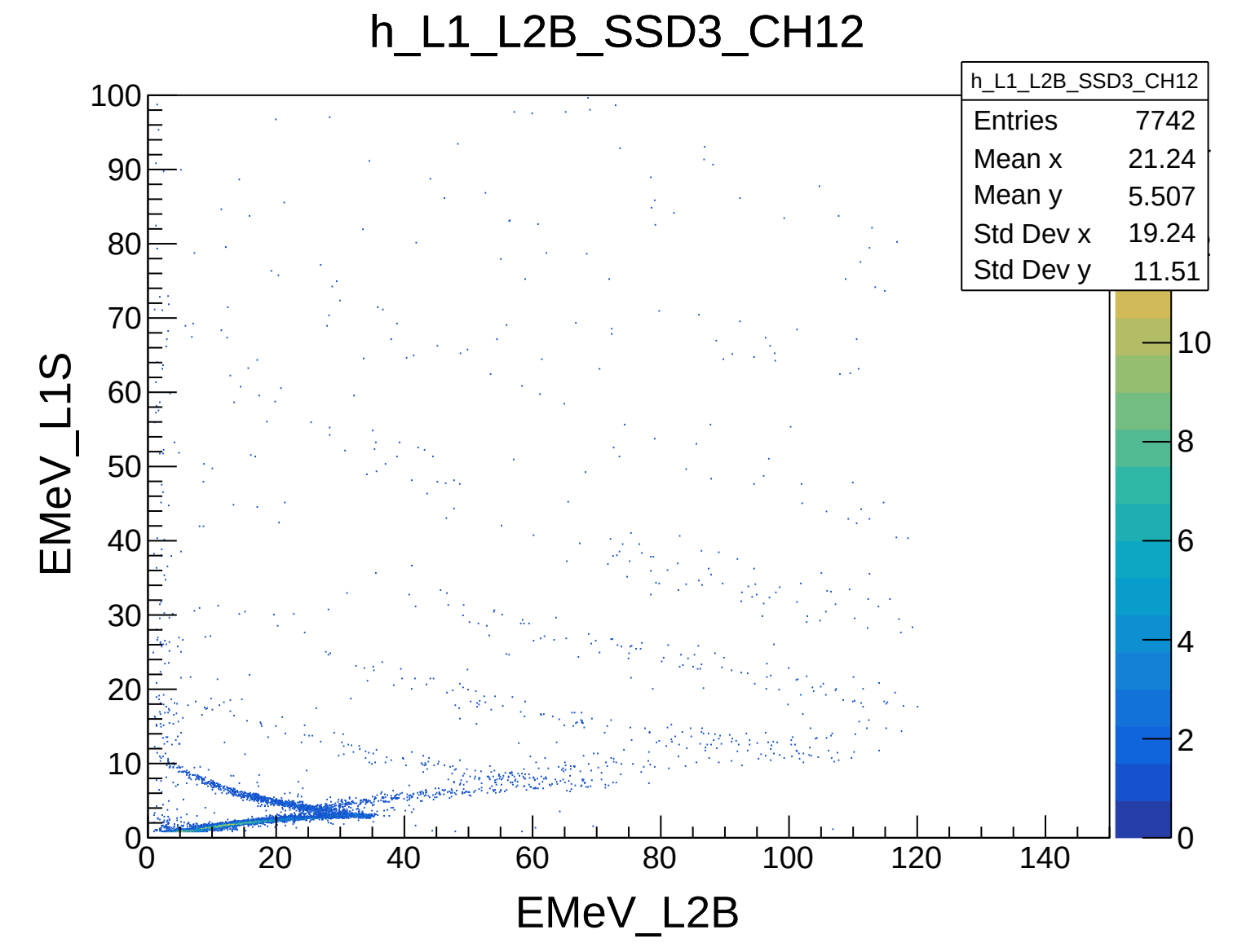
h_L1_L2B_SSD3_CH12
h_L1_L2B_SSD3_CH12
Entries 7742
Mean x 21.24
Mean y 5.507
Std Dev x 19.24
Std Dev y 11.51
EMeV_L1S
EMeV_L2B
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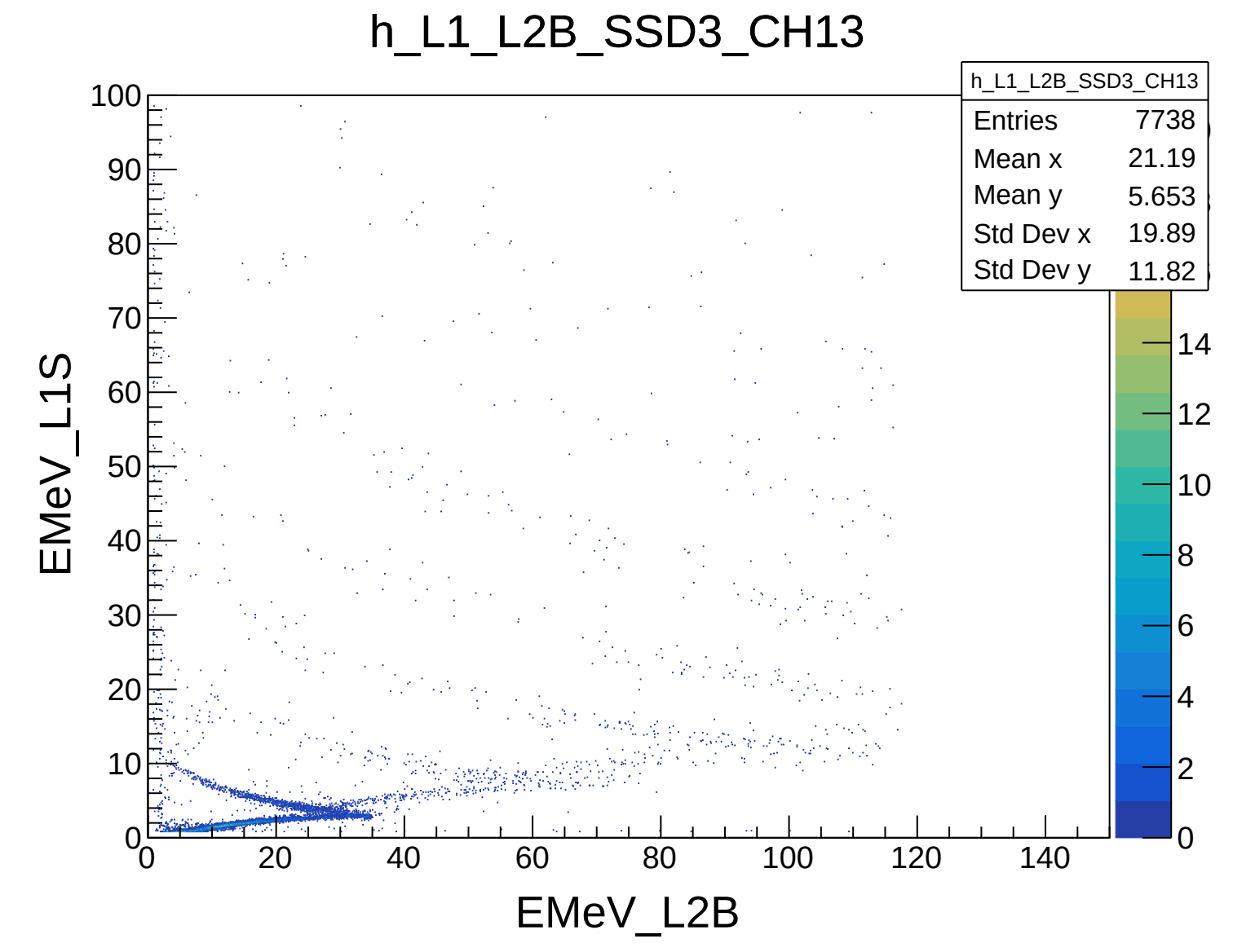
h_L1_L2B_SSD3_CH13
h_L1_L2B_SSD3_CH13
Entries 7738
Mean x 21.19
Mean y 5.653
Std Dev x 19.89
Std Dev y 11.82
EMeV_L1S
EMeV_L2B
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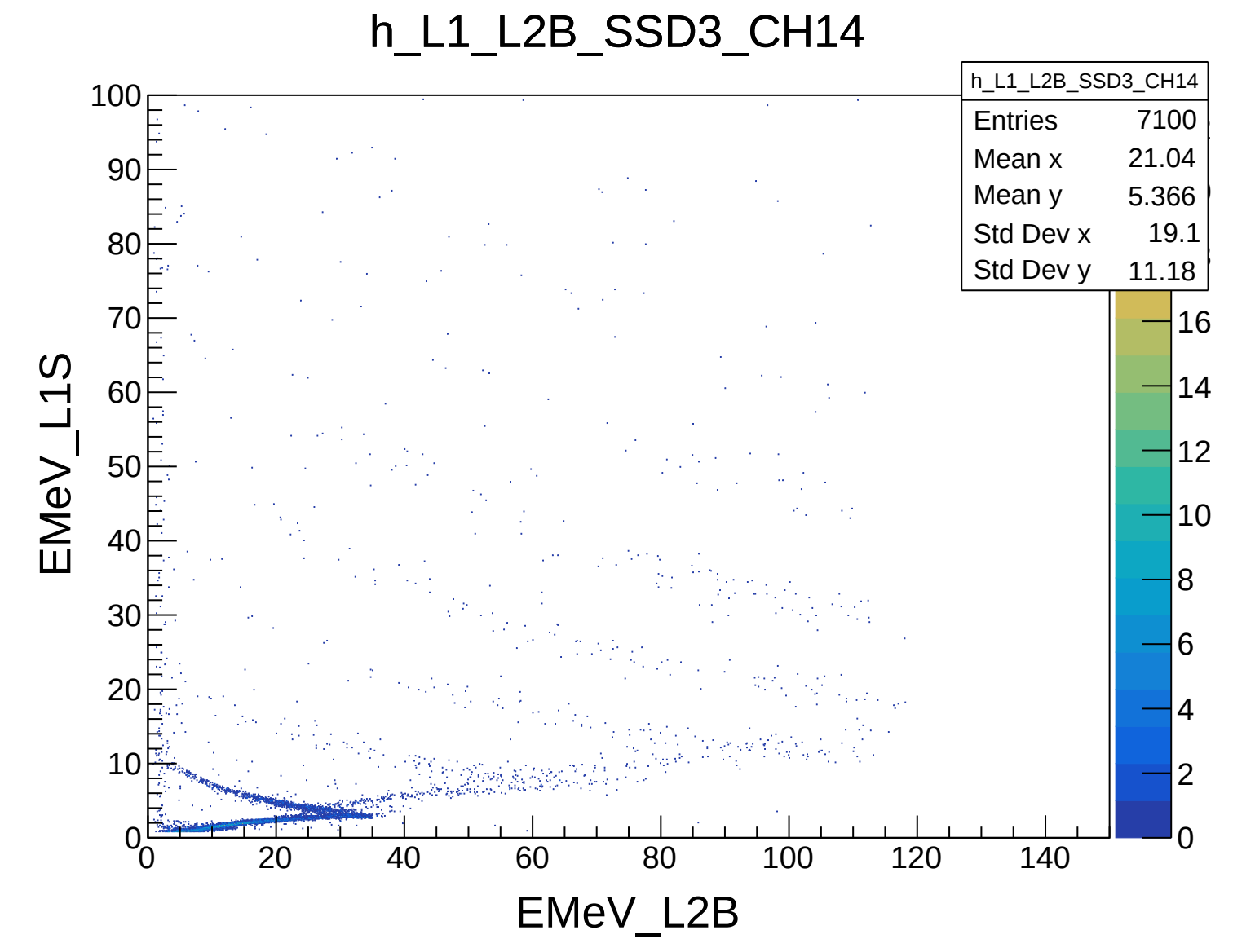
h_L1_L2B_SSD3_CH14
h_L1_L2B_SSD3_CH14
Entries 7100
Mean x 21.04
Mean y 5.366
Std Dev x 19.1
Std Dev y 11.18
EMeV_L1S
EMeV_L2B
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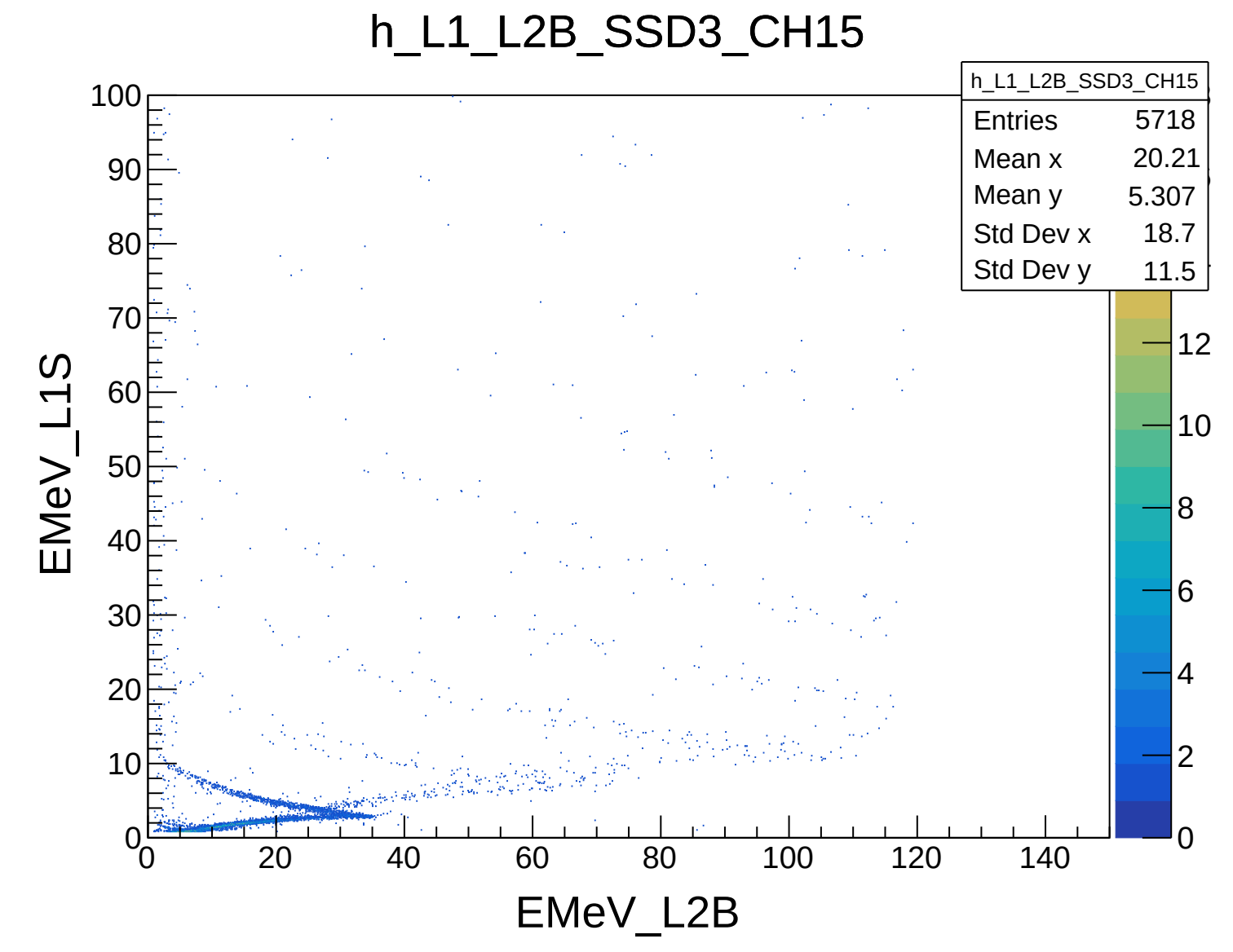
h_L1_L2B_SSD3_CH15
h_L1_L2B_SSD3_CH15
Entries 5718
Mean x 20.21
Mean y 5.307
Std Dev x 18.7
Std Dev y 11.5
EMeV_L1S
EMeV_L2B
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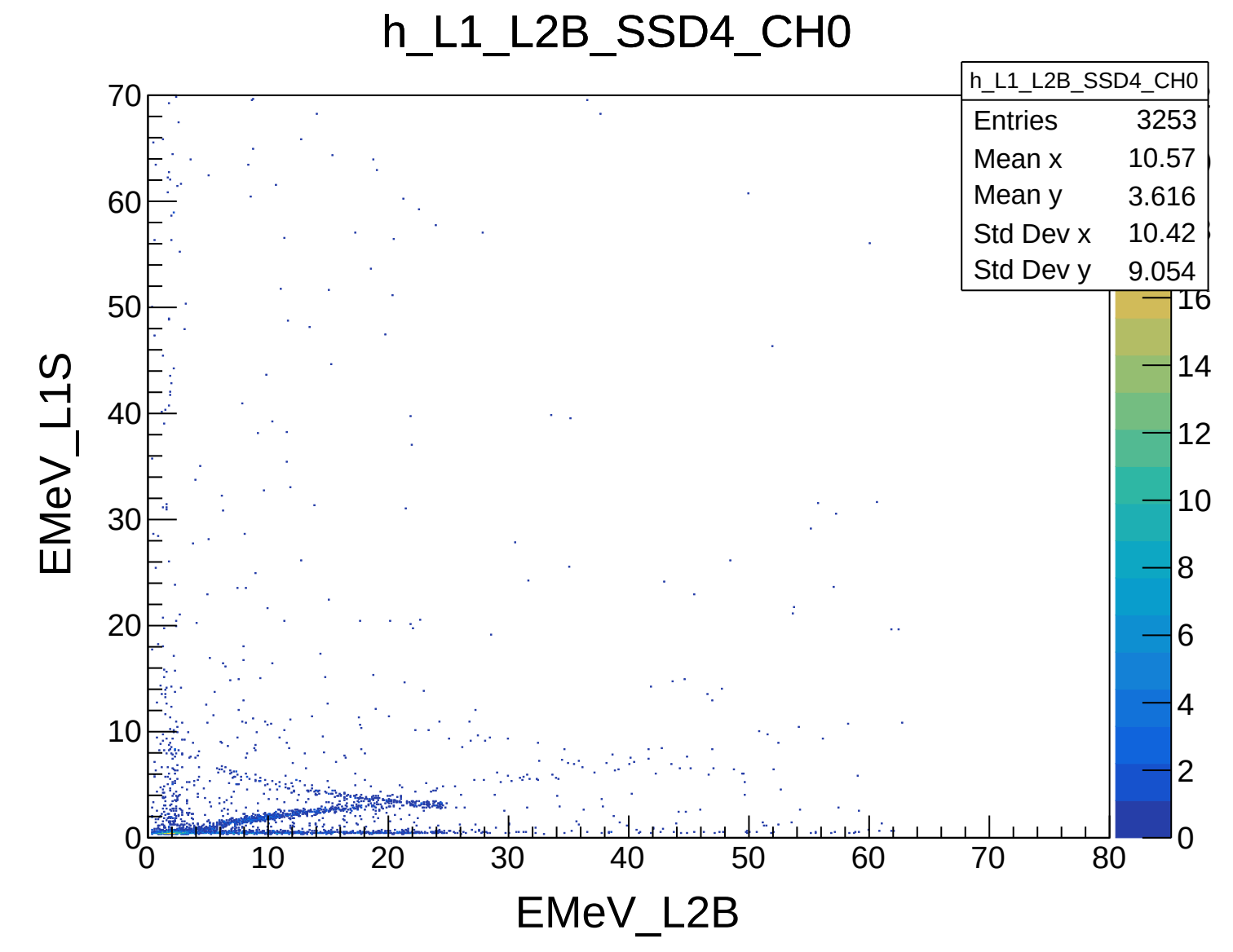
h_L1_L2B_SSD4_CH0
h_L1_L2B_SSD4_CH0
Entries 3253
Mean x 10.57
Mean y 3.616
Std Dev x 10.42
Std Dev y 9.054
EMeV_L1S
EMeV_L2B
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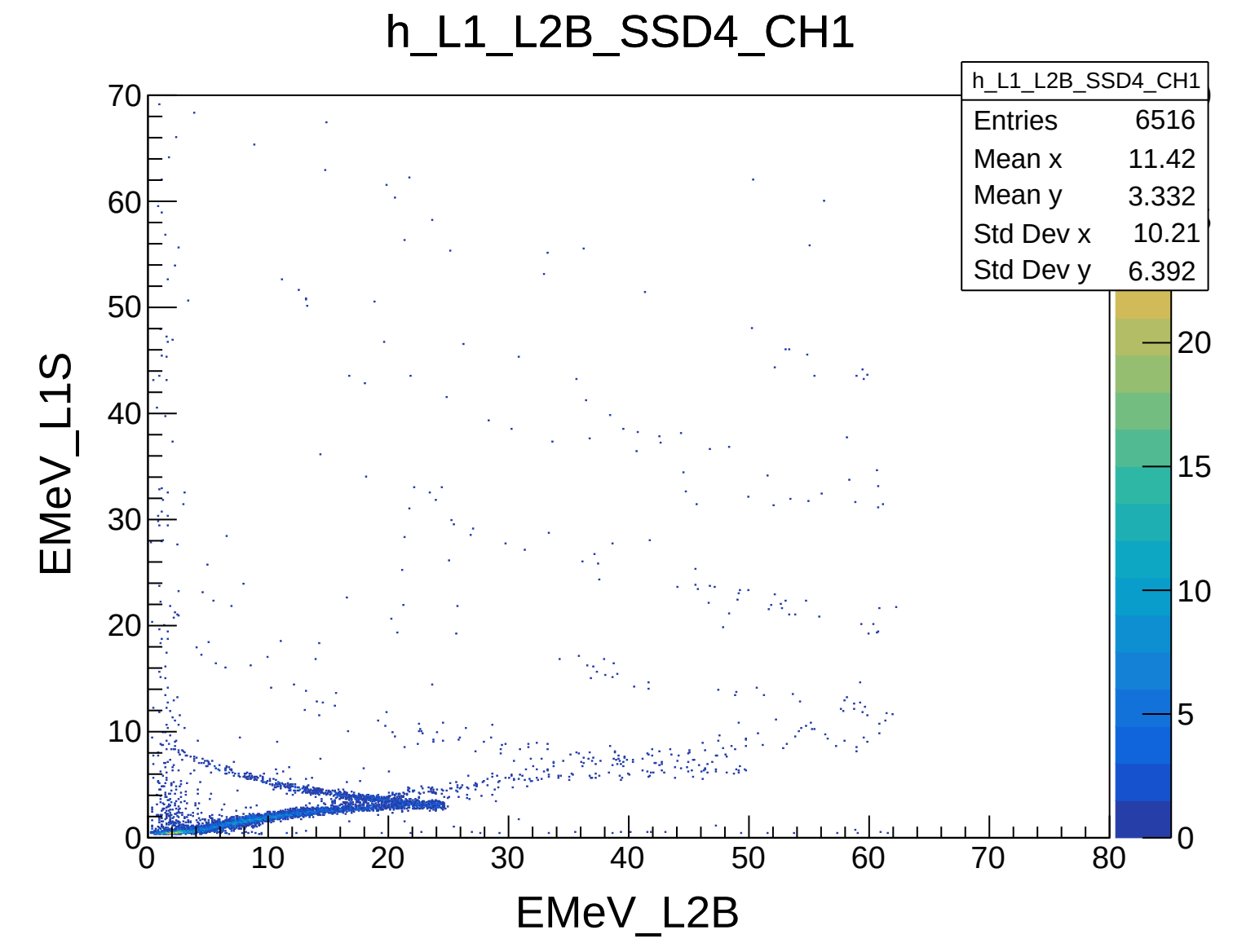
h_L1_L2B_SSD4_CH1
h_L1_L2B_SSD4_CH1
Entries 6516
Mean x 11.42
Mean y 3.332
Std Dev x 10.21
Std Dev y 6.392
EMeV_L1S
EMeV_L2B
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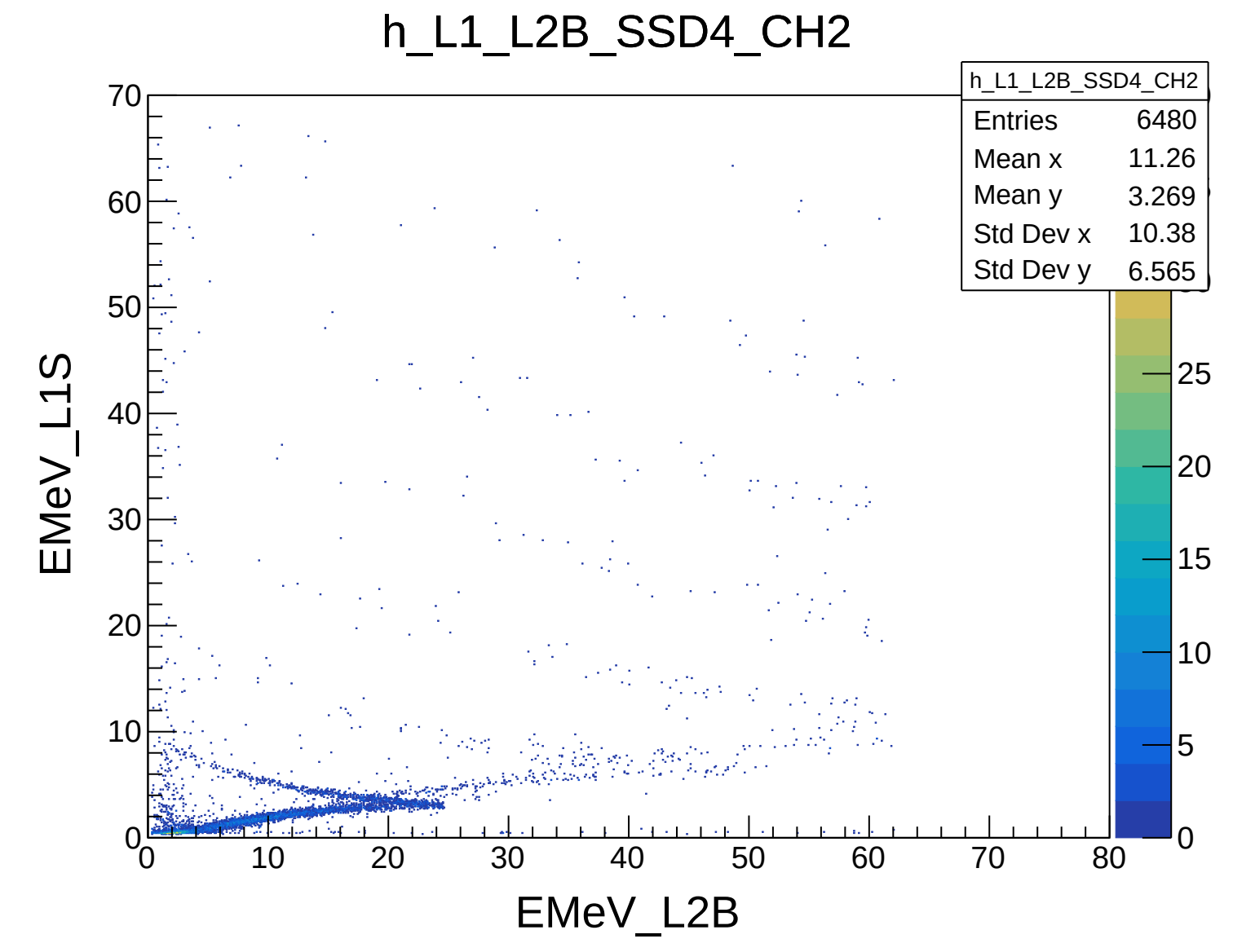
h_L1_L2B_SSD4_CH2
h_L1_L2B_SSD4_CH2
Entries 6480
Mean x 11.26
Mean y 3.269
Std Dev x 10.38
Std Dev y 6.565
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EMeV_L2B
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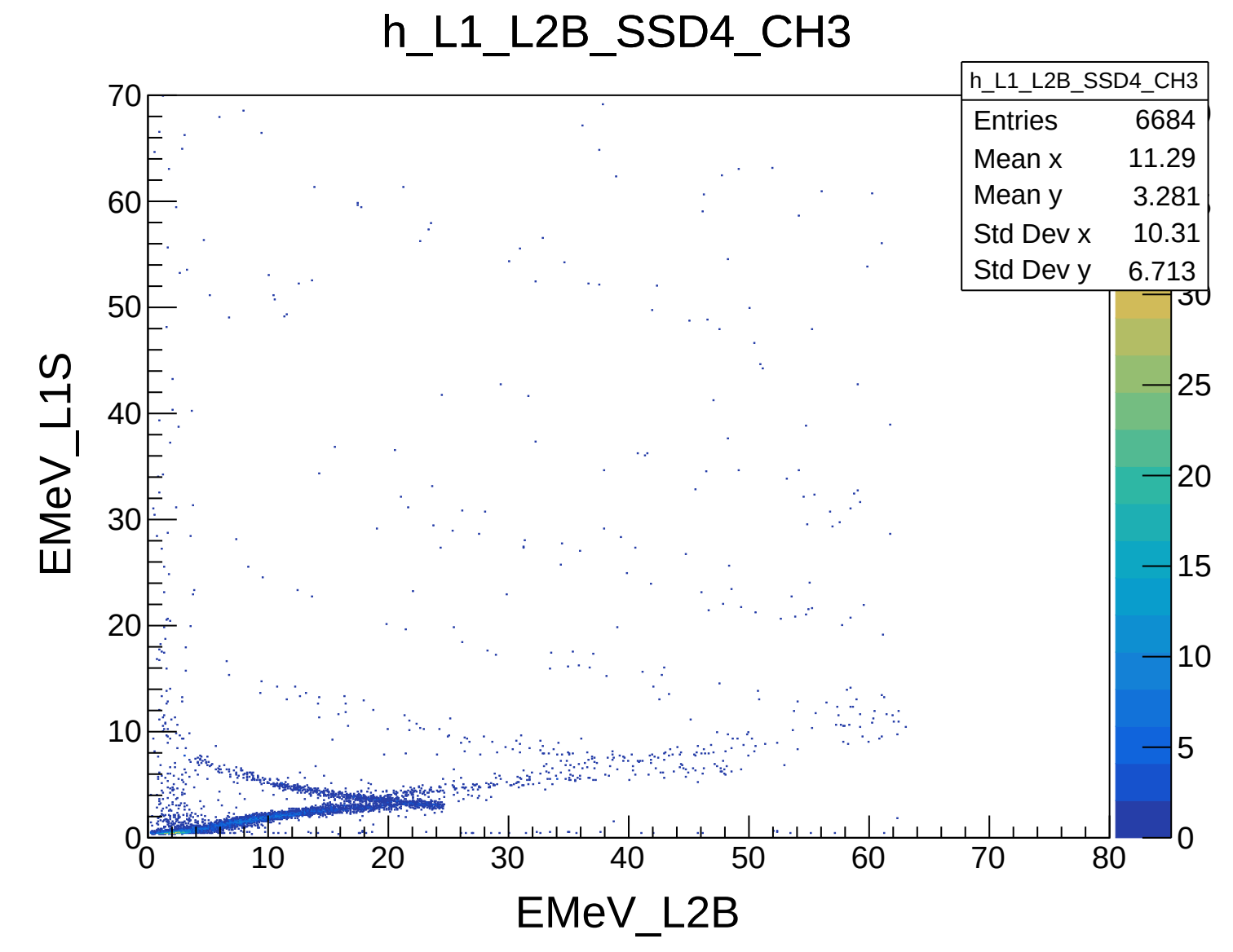
h_L1_L2B_SSD4_CH3
h_L1_L2B_SSD4_CH3
Entries 6684
Mean x 11.29
Mean y 3.281
Std Dev x 10.31
Std Dev y 6.713
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EMeV_L2B
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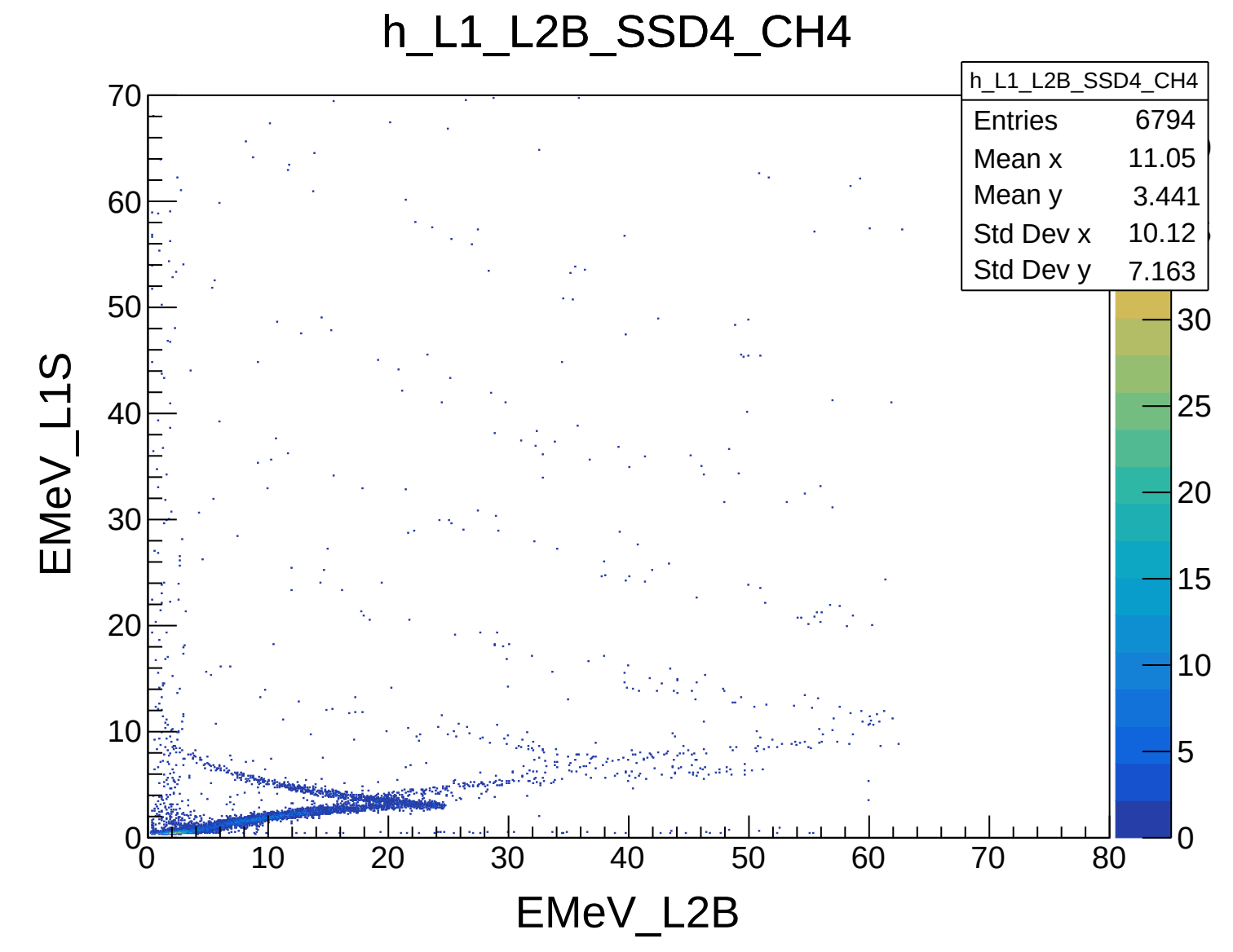
h_L1_L2B_SSD4_CH4
h_L1_L2B_SSD4_CH4
Entries 6794
Mean x 11.05
Mean y 3.441
Std Dev x 10.12
Std Dev y 7.163
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EMeV_L2B
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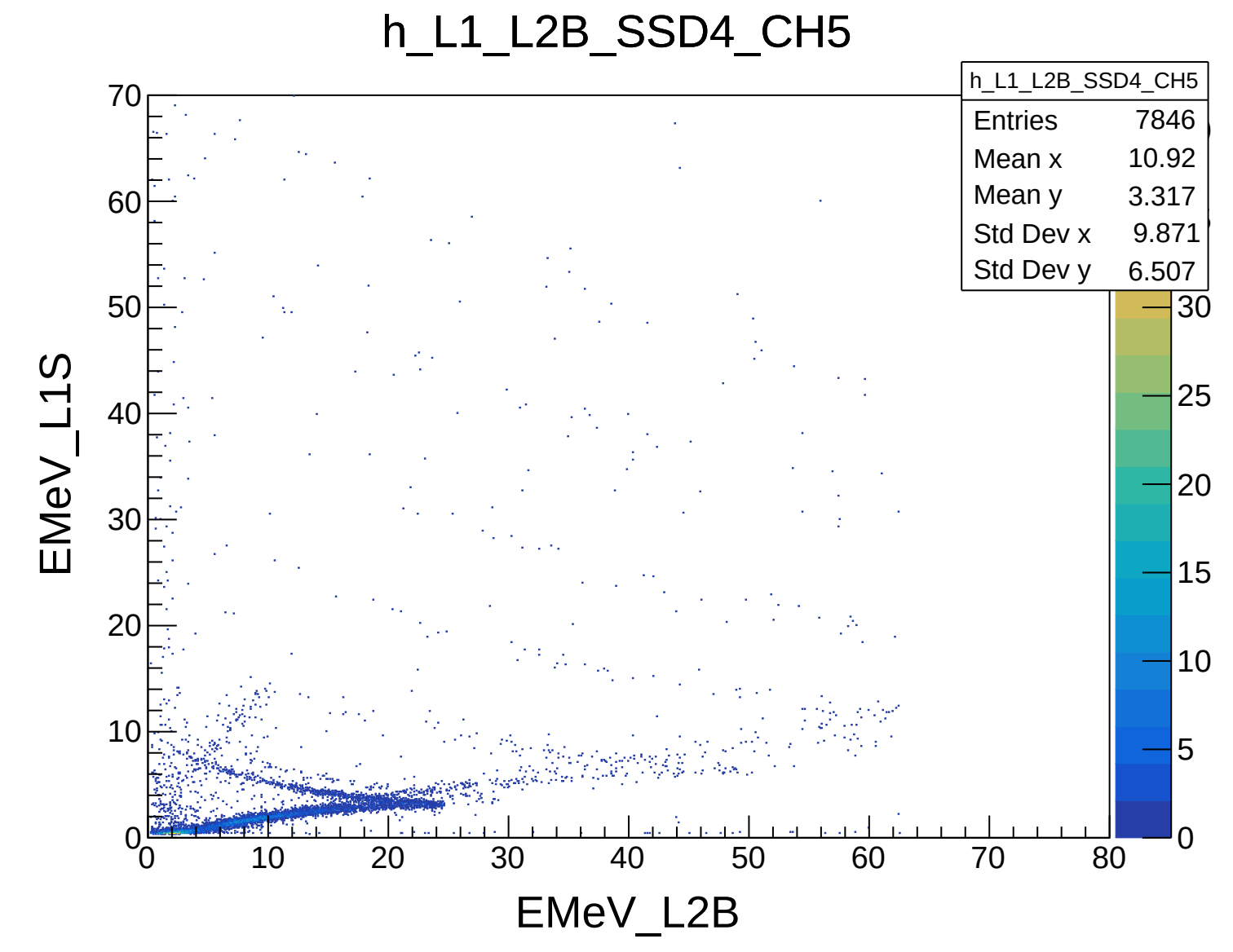
h_L1_L2B_SSD4_CH5
h_L1_L2B_SSD4_CH5
Entries 7846
Mean x 10.92
Mean y 3.317
Std Dev x 9.871
Std Dev y 6.507
EMeV_L1S
EMeV_L2B
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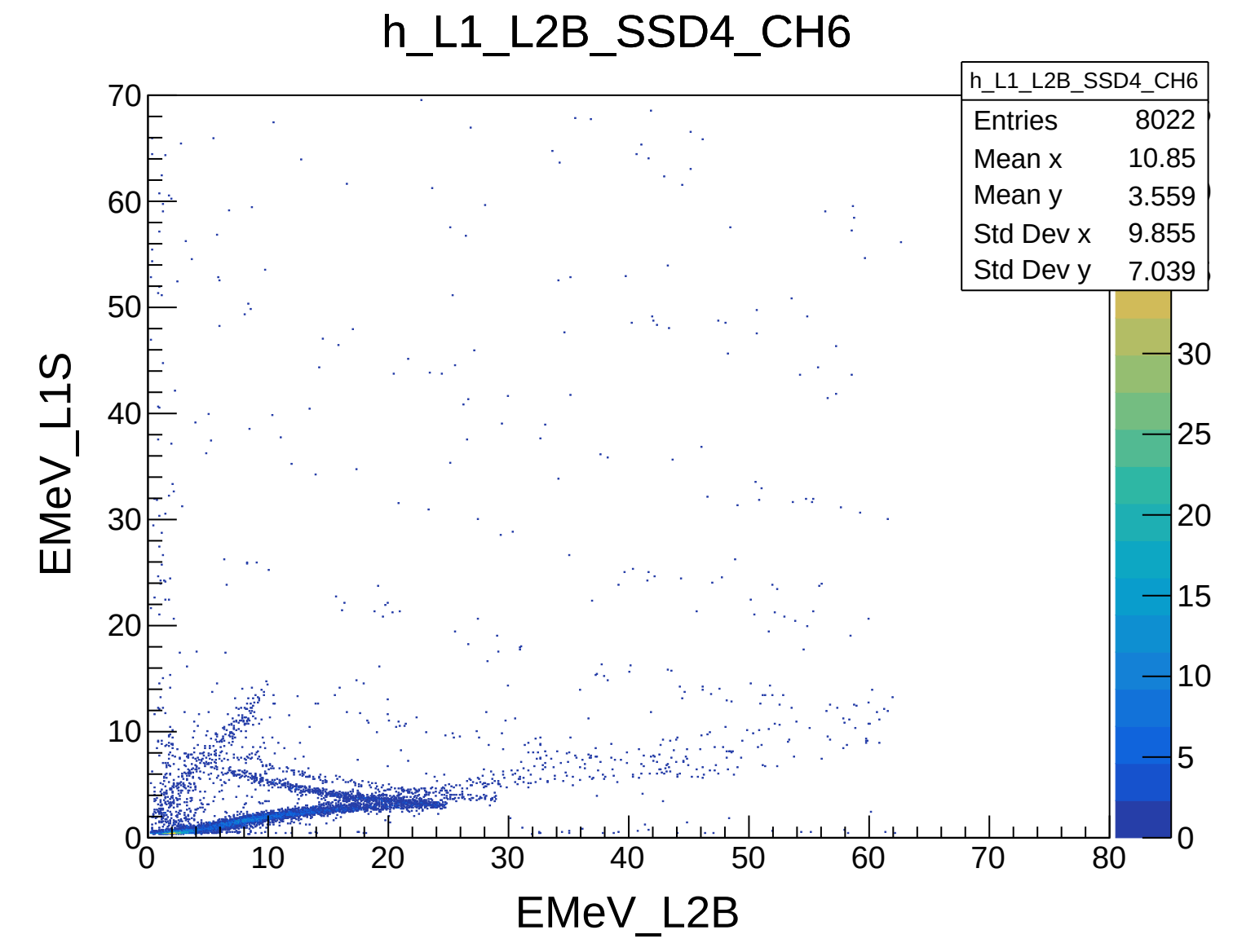
h_L1_L2B_SSD4_CH6
h_L1_L2B_SSD4_CH6
Entries 8022
Mean x 10.85
Mean y 3.559
Std Dev x 9.855
Std Dev y 7.039
EMeV_L1S
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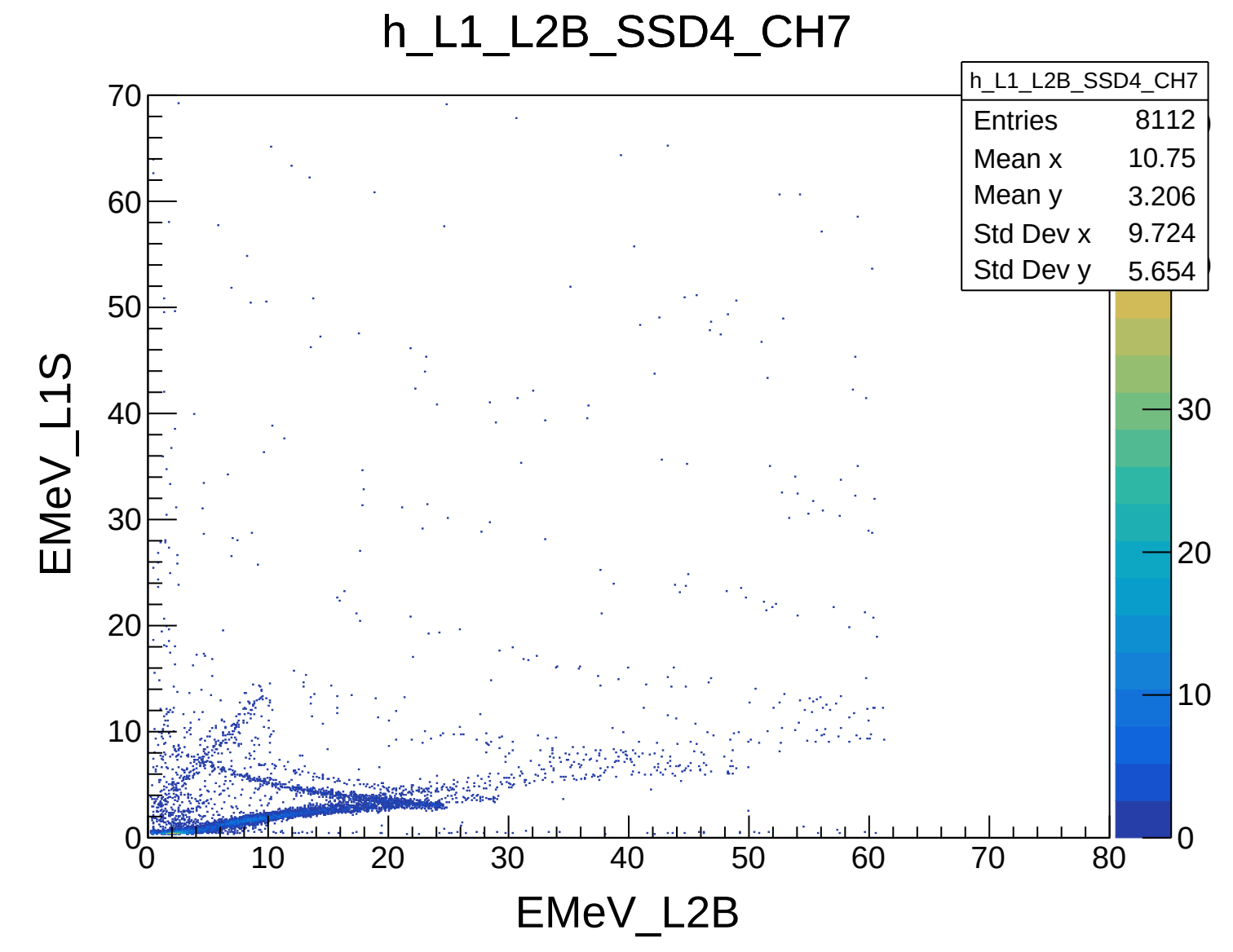
h_L1_L2B_SSD4_CH7
h_L1_L2B_SSD4_CH7
Entries 8112
Mean x 10.75
Mean y 3.206
Std Dev x 9.724
Std Dev y 5.654
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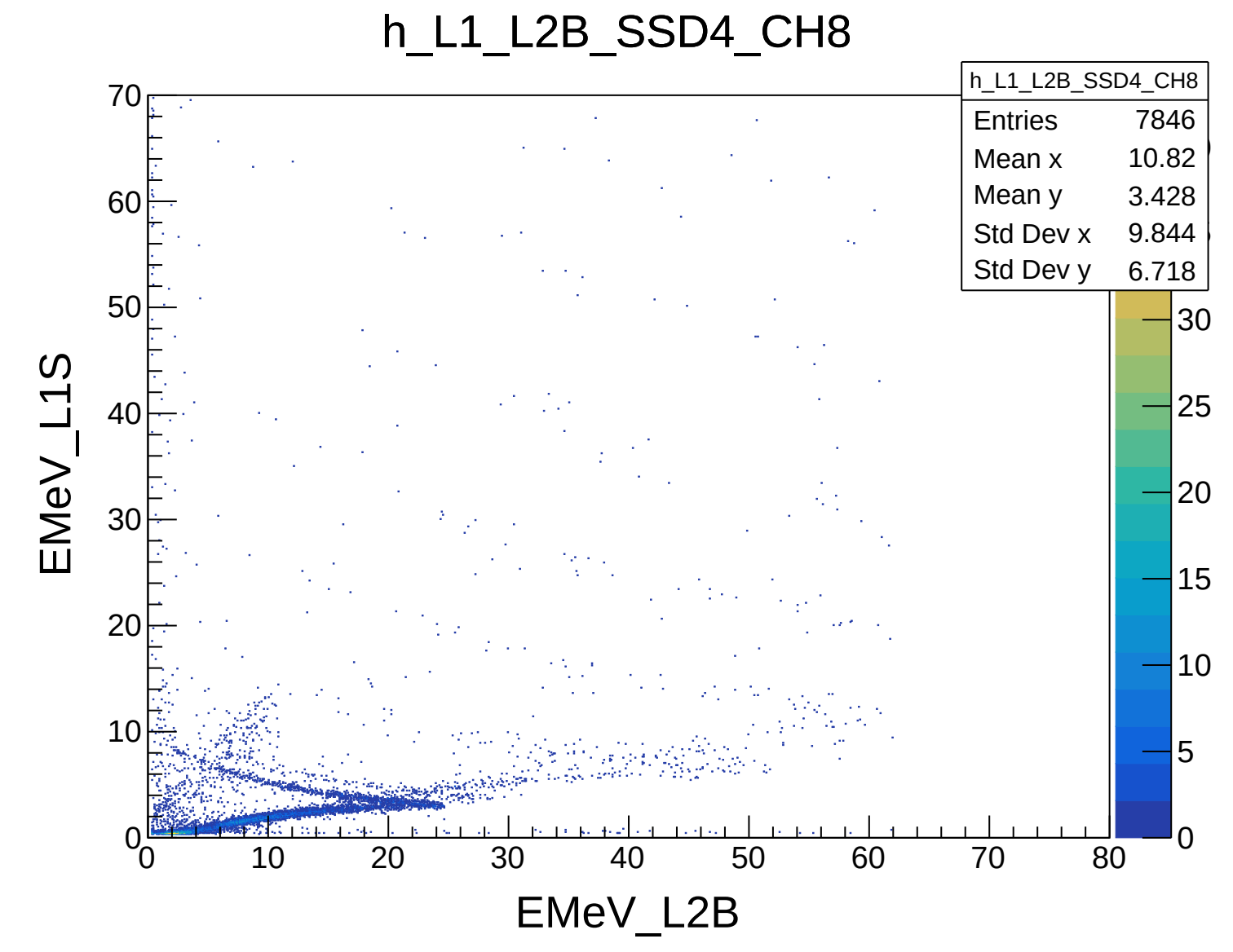
h_L1_L2B_SSD4_CH8
h_L1_L2B_SSD4_CH8
Entries 7846
Mean x 10.82
Mean y 3.428
Std Dev x 9.844
Std Dev y 6.718
EMeV_L1S
EMeV_L2B
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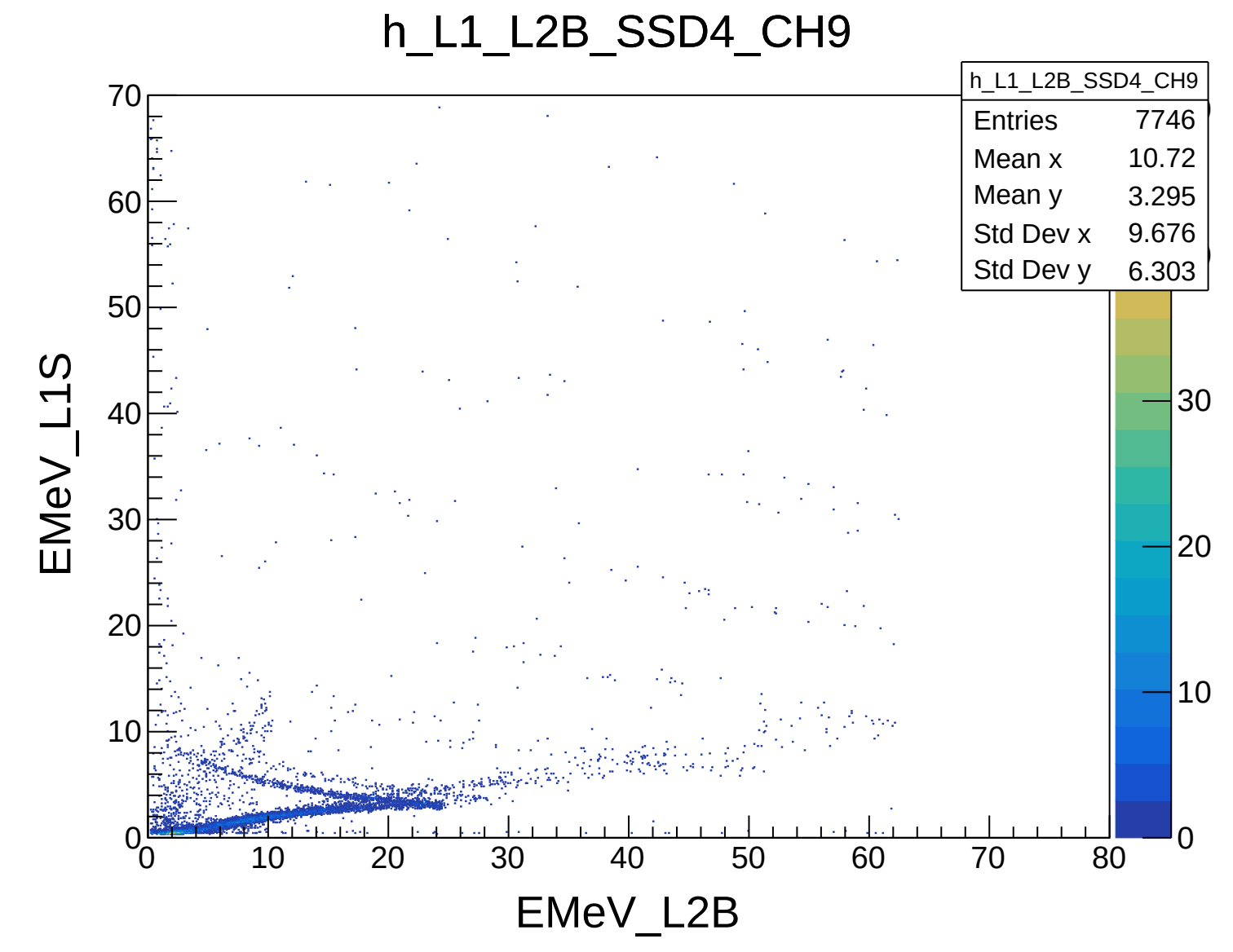
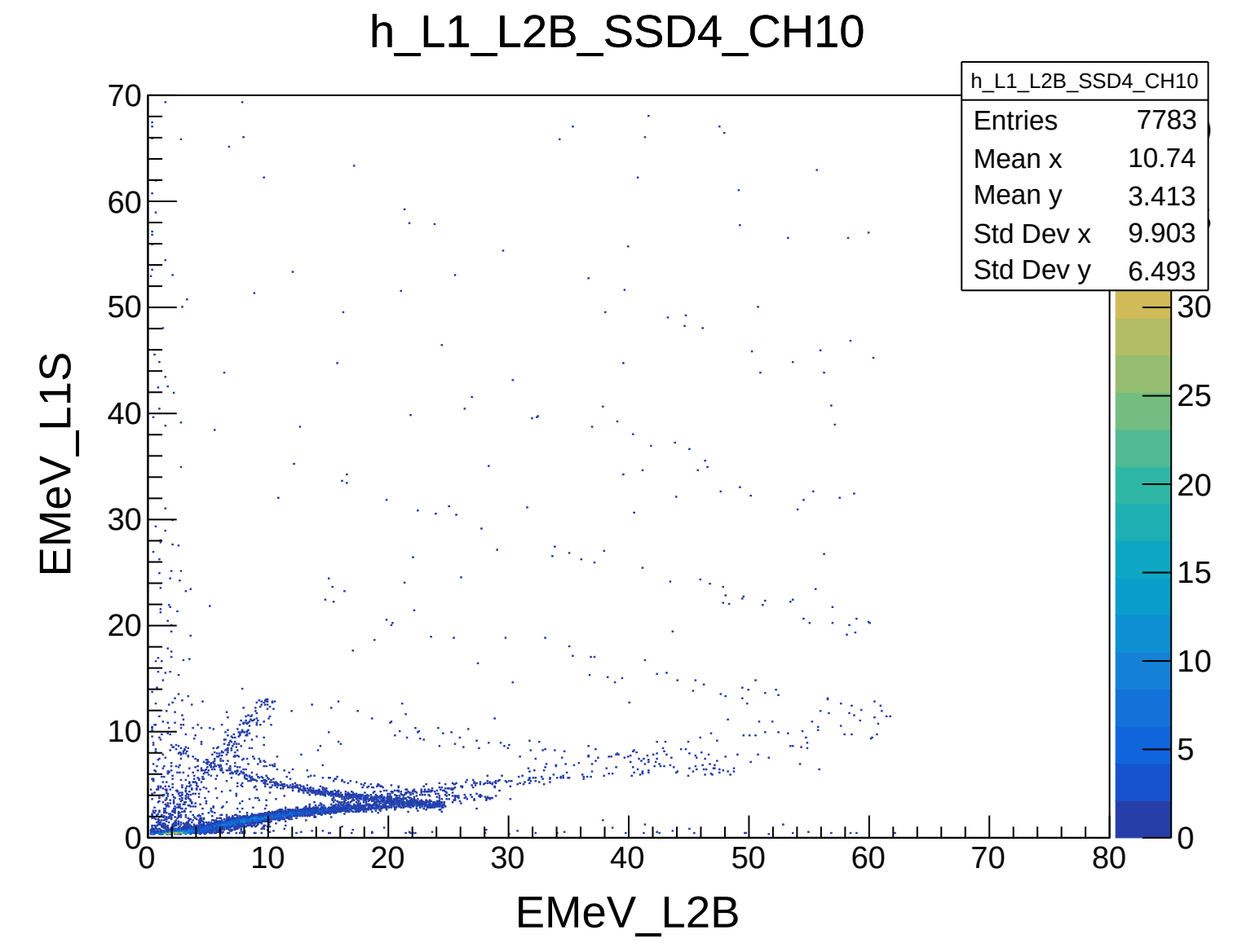
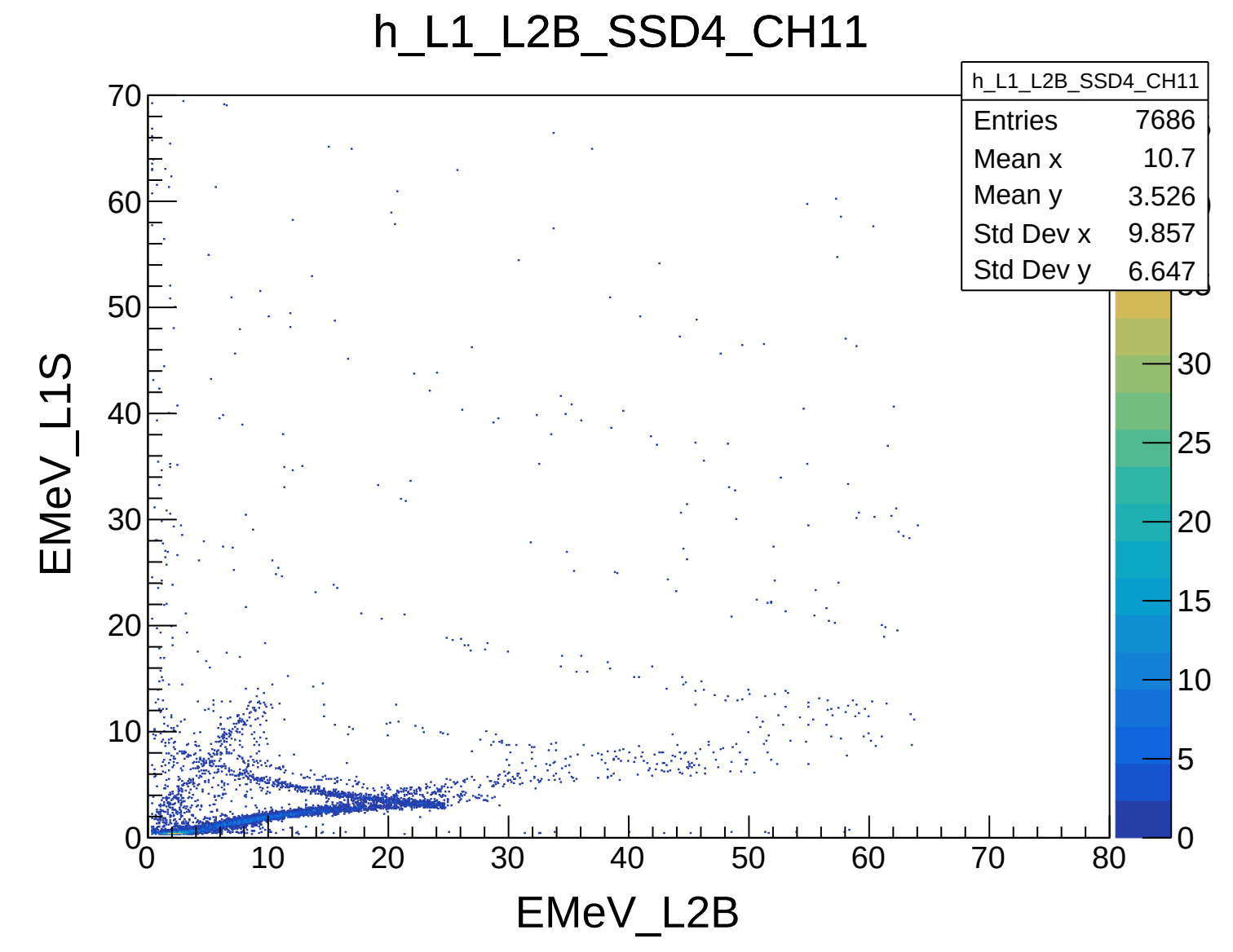
25
30


h_L1_L2B_SSD4_CH9
h_L1_L2B_SSD4_CH9
Entries 7746
Mean x 10.72
Mean y 3.295
Std Dev x 9.676
Std Dev y 6.303
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80


h_L1_L2B_SSD4_CH10
h_L1_L2B_SSD4_CH10
Entries 7783
Mean x 10.74
Mean y 3.413
Std Dev x 9.903
Std Dev y 6.493
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
0
5
10
15
20
25
30


h_L1_L2B_SSD4_CH11
h_L1_L2B_SSD4_CH11
Entries 7686
Mean x 10.7
Mean y 3.526
Std Dev x 9.857
Std Dev y 6.647
EMeV_L1S
EMeV_L2B
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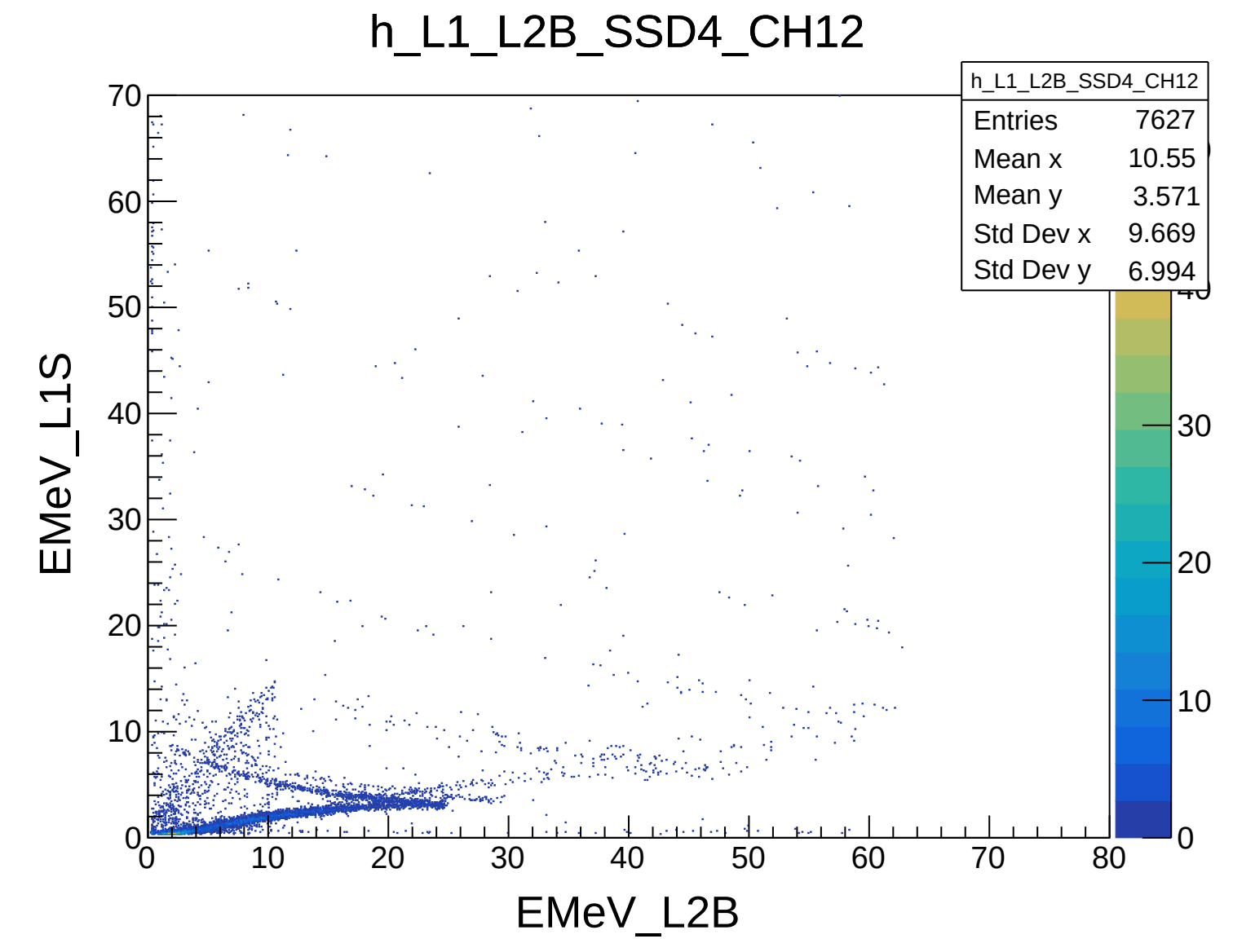
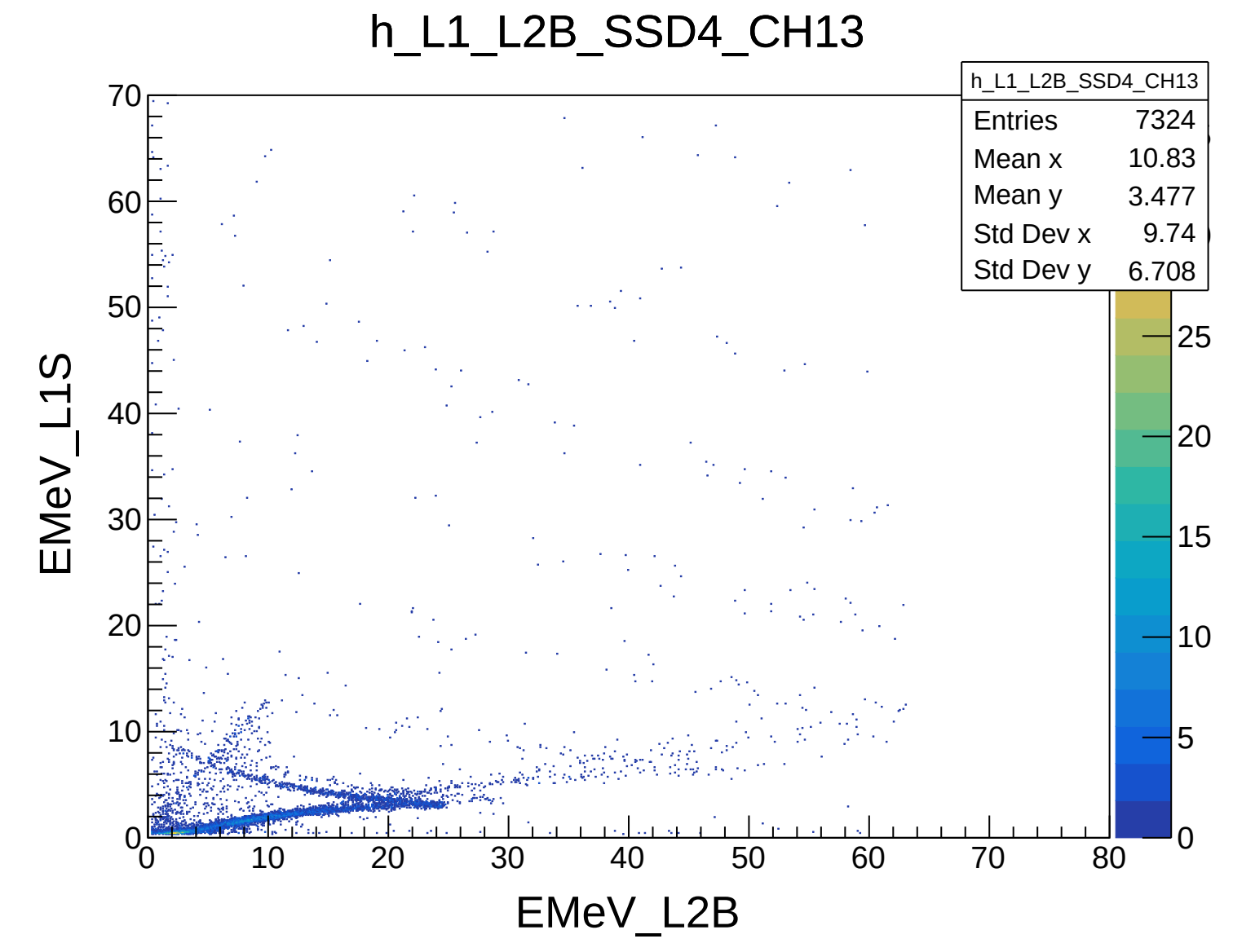
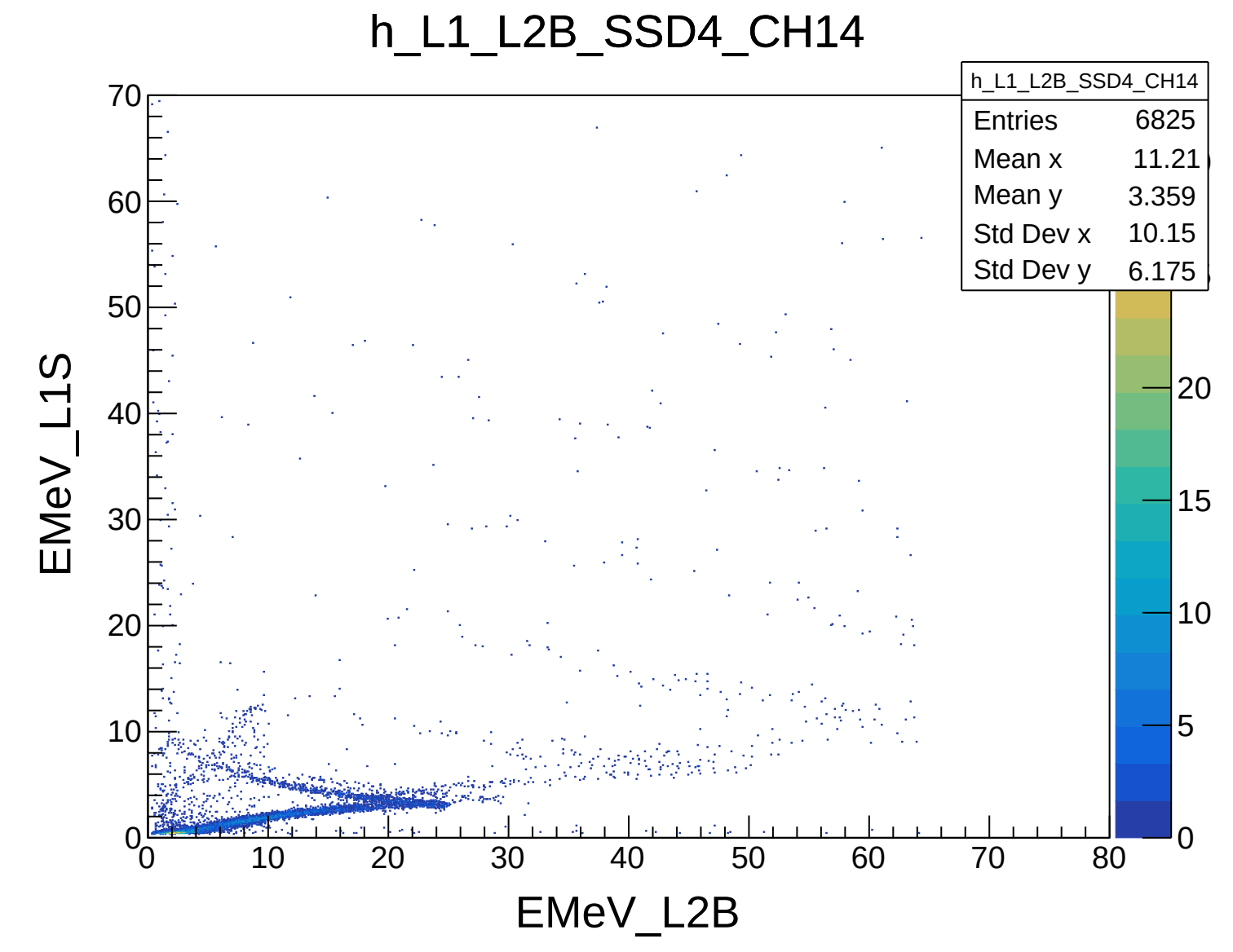
10
20
30
40
50
60
70
80
0
5
10
15
20
25
30


h_L1_L2B_SSD4_CH12
h_L1_L2B_SSD4_CH12
Entries 7627
Mean x 10.55
Mean y 3.571
Std Dev x 9.669
Std Dev y 6.994
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80


h_L1_L2B_SSD4_CH13
h_L1_L2B_SSD4_CH13
Entries 7324
Mean x 10.83
Mean y 3.477
Std Dev x 9.74
Std Dev y 6.708
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
0
5
10
15
20
25


h_L1_L2B_SSD4_CH14
h_L1_L2B_SSD4_CH14
Entries 6825
Mean x 11.21
Mean y 3.359
Std Dev x 10.15
Std Dev y 6.175
EMeV_L1S
EMeV_L2B
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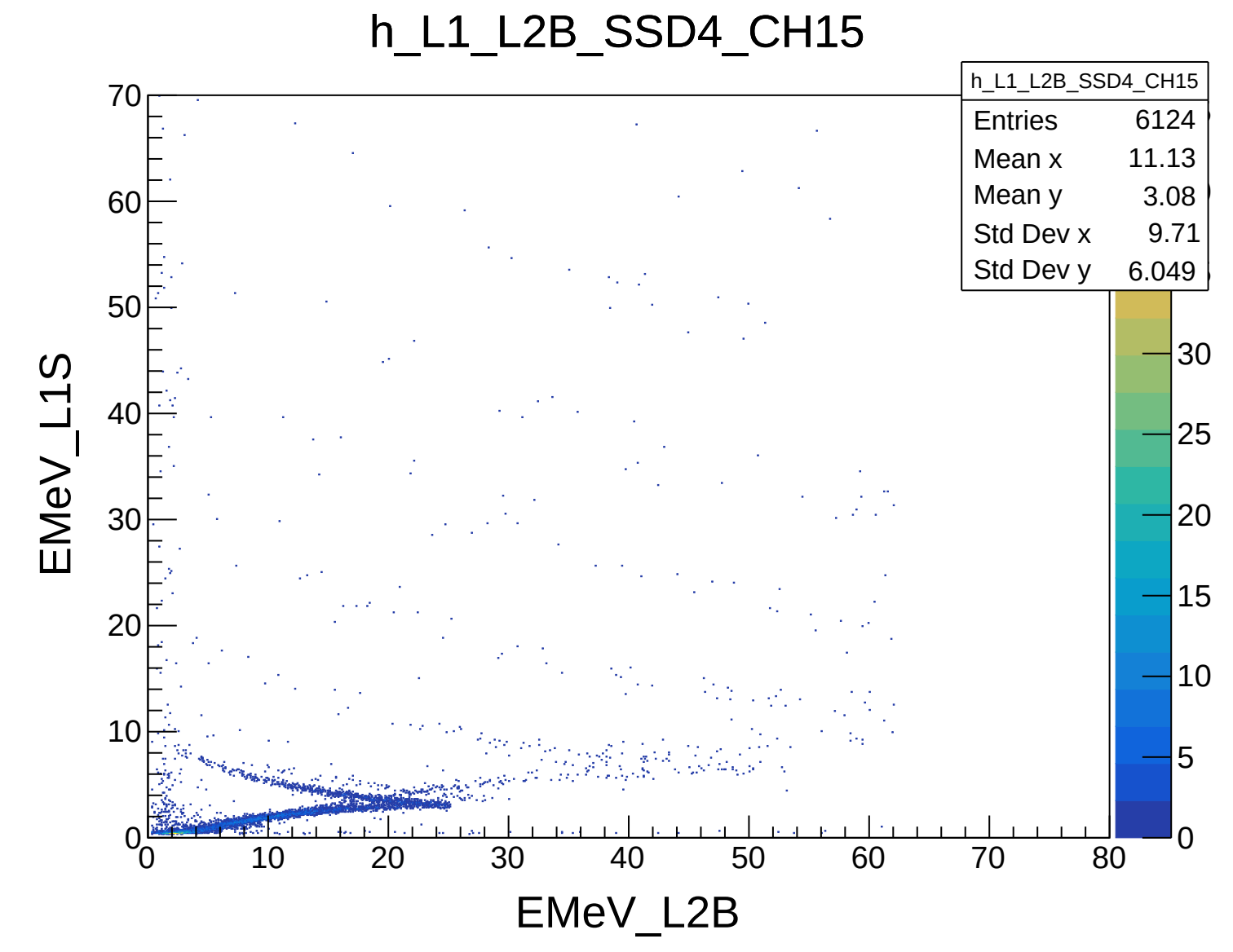
10
20
30
40
50
60
70
80
5
15


h_L1_L2B_SSD4_CH15
h_L1_L2B_SSD4_CH15
Entries 6124
Mean x 11.13
Mean y 3.08
Std Dev x 9.71
Std Dev y 6.049
EMeV_L1S
EMeV_L2B
0
10
20
30
40
50
60
70
80
0
5
10
15
20
25
30