Main pin-mapping table (center columns 12–13 grouped under **CM4 CARRIER 40-pin GPIO mapping**):

i.MxBMP ALT6	i.MxBMP ALT5	i.MxBMP ALT4	i.MxBMP ALT3	i.MxBMP ALT2	i.MxBMP ALT1	i.MxBMP ALT0	DTS Enableable ALT	Default Functions	i.MxBMP Name	Name	Pin	Pin	Name	i.MxBMP Name	Default Functions	DTS Enableable ALT	i.MxBMP ALT0	i.MxBMP ALT1	i.MxBMP ALT2	i.MxBMP ALT3	i.MxBMP ALT4	i.MxBMP ALT5	i.MxBMP ALT6
										3.3V	1	2	5V										
GPIO3_IO25		I2C5_SDA	PWM1_OUT	SAI1_TX_BCLK	SAI5_MCLK		ALTS	I2C5 SDA	GPIO3.IO[25]	GPIO2	3	4	5V										
GPIO3_IO21	PDM_BIT_STREAM0	I2C5_SCL	PWM2_OUT	SAI1_TX_DATA2	SAI5_RX_DATA0		ALTS	I2C5 SCL	GPIO3.IO[21]	GPIO3	5	6	GND										
GPIO2_IO08	UART3_TX	I2C2_SCL		USDHC1_DATA6			ALT4	GPIO	GPIO2.IO[8]	GPIO4	7	8	GPIO14	GPIO4.IO[21]	UART1 RX	ALTS	SAI2_RX_SYNC	SAI5_TX_SYNC	SAI5_TX_DATA1	SAI2_RX_DATA1	UART1_TX	GPIO4_IO21	PDM_BIT_STREAM2
										GND	9	10	GPIO15	GPIO4.IO[22]	UART1 RX	ALTS	SAI2_RX_BCLK	SAI5_TX_BCLK			UART1_RX	GPIO4_IO22	PDM_BIT_STREAM1
PDM_BIT_STREAM3	GPIO2_IO23	UART1_RTS_B	SAI2_TX_DATA1	ENET_QOS_1588_EVENT2_OUT	SAI5_TX_DATA0	SAI2_RX_DATA0	ALT4	GPIO	GPIO2.IO[23]	GPIO17	11	12	GPIO18	GPIO5.IO[13]	GPIO	ALT0	ECSPI2_SS0	UART6_RTS_B				GPIO5_IO13	
	GPIO2_IO05	UART2_RX	I2C4_SDA		ENET1_RGMII_RD1	USDHC1_DATA3	ALT0	GPIO	GPIO2.IO[5]	GPIO27	13	14	GND										
	GPIO2_IO00	UART1_TX	I2C5_SCL		ENET1_MDC	USDHC1_CLK	ALT0	GPIO	GPIO2.IO[0]	GPIO22	15	16	GPIO23	GPIO2.IO[1]	GPIO	ALT0	USDHC1_CMD	ENET1_MDIO		I2C5_SDA	UART1_RX	GPIO2_IO01	
										3.3V	17	18	GPIO24	GPIO2.IO[2]	GPIO	ALT0	USDHC1_DATA0	ENET1_RGMII_TD1		I2C5_SCL	UART1_RTS_B	GPIO2_IO02	
	GPIO5_IO07	SAI7_RX_BCLK	I2C2_SDA	I2C1_SDA	UART3_TX	ECSPI1_MOSI	ALTS	SPI1 MOSI	GPIO5.IO[7]	GPIO10	19	20	GND										
	GPIO5_IO08	SAI7_RX_DATA0	I2C2_SCL		UART3_CTS_B	ECSPI1_MISO	ALTS	SPI1 MISO	GPIO5.IO[8]	GPIO9	21	22	GPIO25	GPIO2.IO[3]	GPIO	ALT0	USDHC1_DATA1	ENET1_RGMII_TD0		I2C6_SDA	SAI7_RX_SYNC	GPIO2_IO03	
	GPIO5_IO06	SAI7_RX_SYNC	I2C1_SCL		UART3_RX	ECSPI1_SCLK	ALTS	SPI1 SCLK	GPIO5.IO[6]	GPIO11	23	24	GPIO8	GPIO5.IO[9]	SPI1 CS	ALT3	ECSPI1_SS0	UART3_RTS_B	I2C2_SDA	SAI7_TX_SYNC	I2C3_SCL	GPIO5_IO09	
										GND	25	26	GPIO7	GPIO4.IO[26]	GPIO	ALT3	SAI2_TX_DATA0	SAI5_TX_DATA3	ENET_QOS_1588_EVENT2_IN	FLEXCAN2_TX	ENET_QOS_1588_EVENT2_AUX_IN	GPIO4_IO26	
GPIO3_IO20		PDM_CLK		PWM3_OUT	SAI1_TX_DATA1	SAI5_RX_BCLK	ALTS	I2C6 SDA	GPIO3.IO[20]	GPIO0	27	28	GPIO1	GPIO3.IO[19]	I2C6 SCL	ALTS	SAI5_RX_SYNC	SAI1_TX_DATA0	PWM4_OUT	I2C6_SCL	GPIO3_IO19		
GPIO2_IO09	UART3_RX		I2C2_SDA		ENET1_RX_ER	USDHC1_DATA7	ALT4	GPIO	GPIO2.IO[9]	GPIO5	29	30	GND										
SAI3_MCLK	GPIO4_IO27	ENET_QOS_1588_EVENT3_AUX_IN	FLEXCAN2_RX	ENET_QOS_1588_EVENT3_IN	SAI5_MCLK	SAI2_MCLK	ALT3	GPIO	GPIO4.IO[27]	GPIO6	31	32	GPIO12	GPIO5.IO[2]	PWM4	ALTS	SAI3_MCLK	PWM4_OUT	SAI5_MCLK			SPDIF1_OUT	GPIO5_IO02
	GPIO5_IO05		GPT1_COMPARE3		PWM1_OUT	SPDIF1_EXT_CLK	ALTS	PWM1	GPIO5.IO[5]	GPIO13	33	34	GND										
	GPIO5_IO12	CCM_CLKO1	SAI7_MCLK		UART4_CTS_B	ECSPI2_MISO	ALT0	GPIO	GPIO5.IO[12]	GPIO19	35	36	GPIO16	GPIO4.IO[24]	GPIO	ALT4	SAI2_TX_SYNC	SAI5_TX_DATA1	ENET_QOS_1588_EVENT3_OUT	SAI2_TX_DATA1	UART1_CTS_B	GPIO4_IO24	PDM_BIT_STREAM2
	GPIO2_IO04	UART2_TX	I2C4_SCL		ENET1_RGMII_RD0	USDHC1_DATA2	ALT0	GPIO	GPIO2.IO[4]	GPIO26	37	38	GPIO20	GPIO5.IO[11]	GPIO	ALT0	ECSPI2_SCLK	UART4_TX	I2C3_SDA	SAI7_TX_DATA0		GPIO5_IO11	
										GND	39	40	GPIO21	GPIO5.IO[10]	GPIO	ALT0	ECSPI2_SCLK	UART4_RX	I2C3_SCL	SAI7_TX_BCLK		GPIO5_IO10	

Special Functions Pins

Pins	Default Functions	Usable ALT	i.MxBMP ALT0	i.MxBMP ALT1	i.MxBMP ALT2	i.MxBMP ALT3	i.MxBMP ALT4	i.MxBMP ALTS	i.MxBMP ALT6
GPIO44	I2C2 SDA	ALTS	I2C2_SDA	ENET_QOS_1588_EVENT1_OUT	USDHC3_WP	ECSPI1_SS0		GPIO5_IO17	
GPIO45	I2C2 SCL	ALTS	I2C2_SCL	ENET_QOS_1588_EVENT1_IN	USDHC3_CD_B	ECSPI1_MISO	ENET_QOS_1588_EVENT1_AUX_IN	GPIO5_IO16	