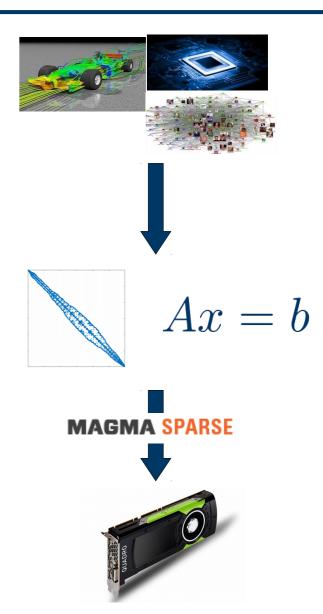


Overcoming Load Imbalance for Irregular Sparse Matrices

Goran Flegar, Hartwig Anzt



- GPU-accelerated sparse linear algebra library
 - Focus: linear systems







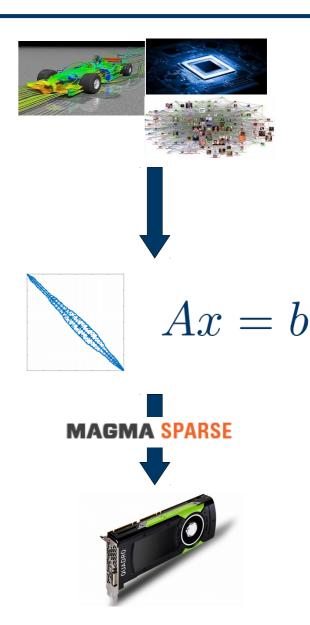


- GPU-accelerated sparse linear algebra library
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 - Iterative, Krylov-subspace based linear solvers
 - SpMV
 - BLAS-1 operations









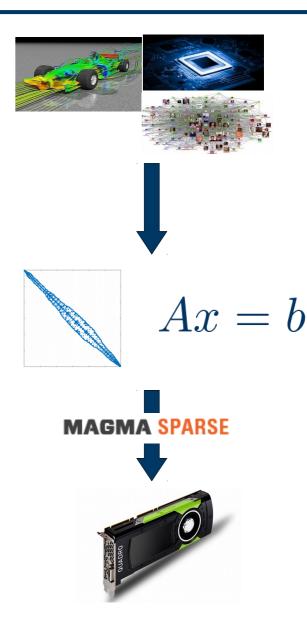


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 - Sparse matrix formats & SpMV
 - accelerate each iteration of the solver









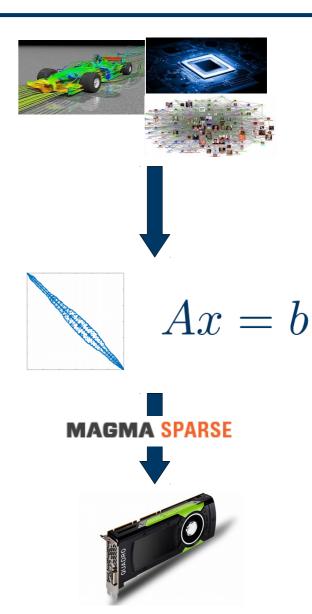


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 - reduce the number of iterations









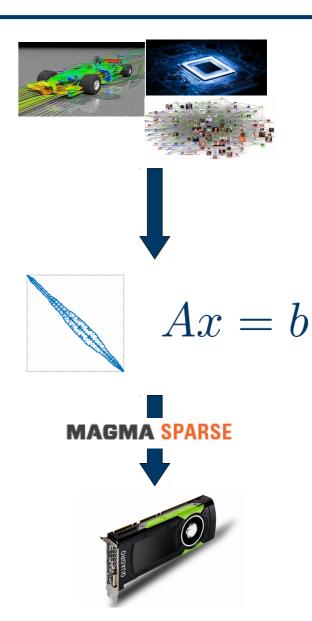


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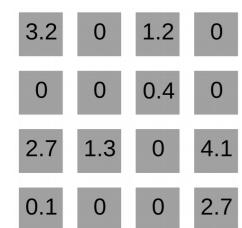


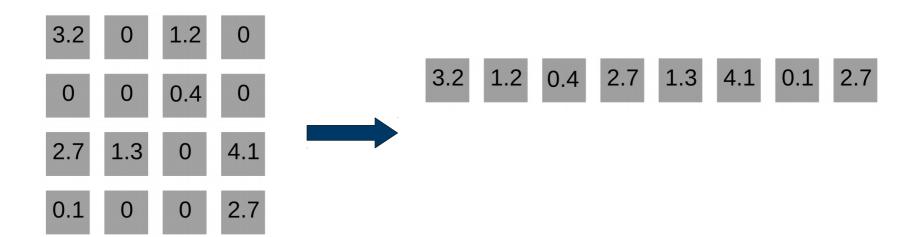


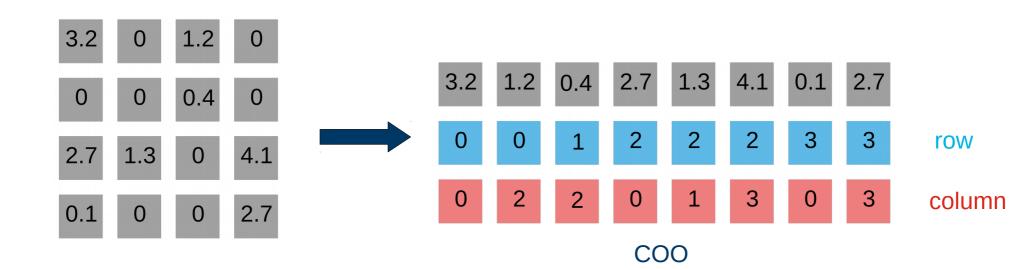






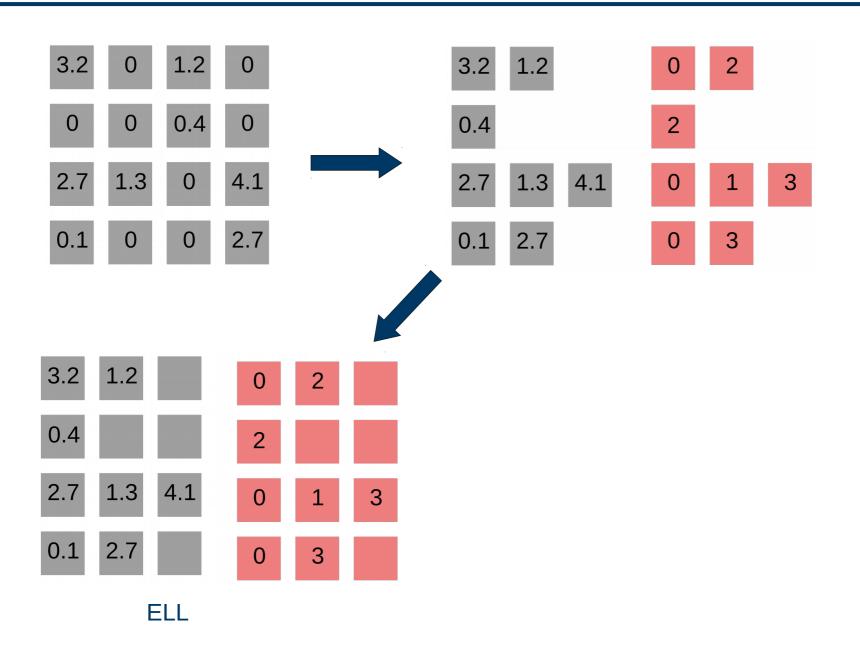




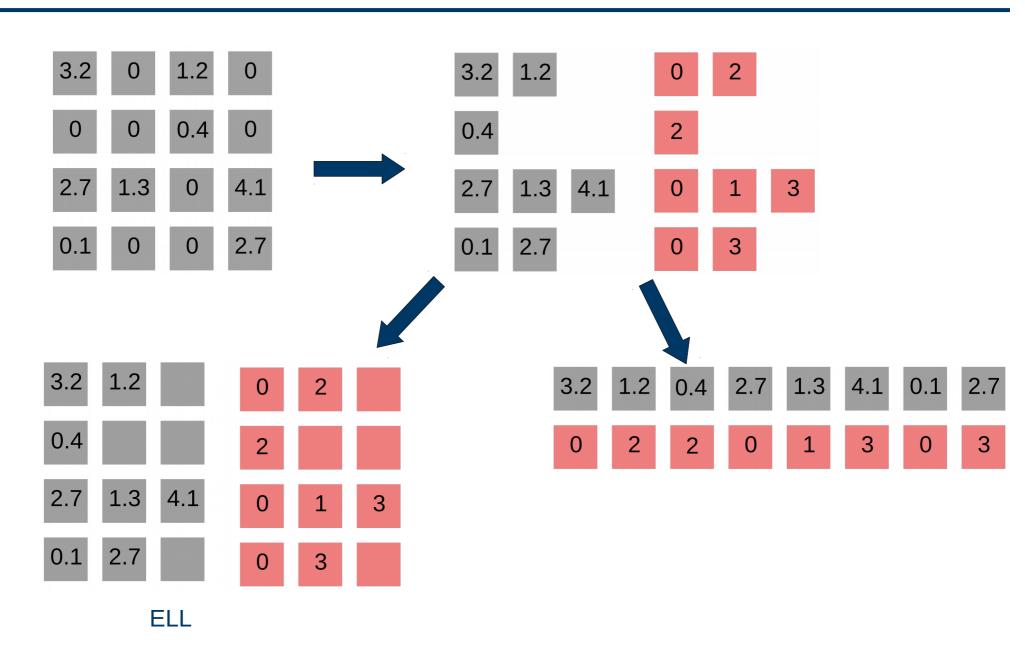


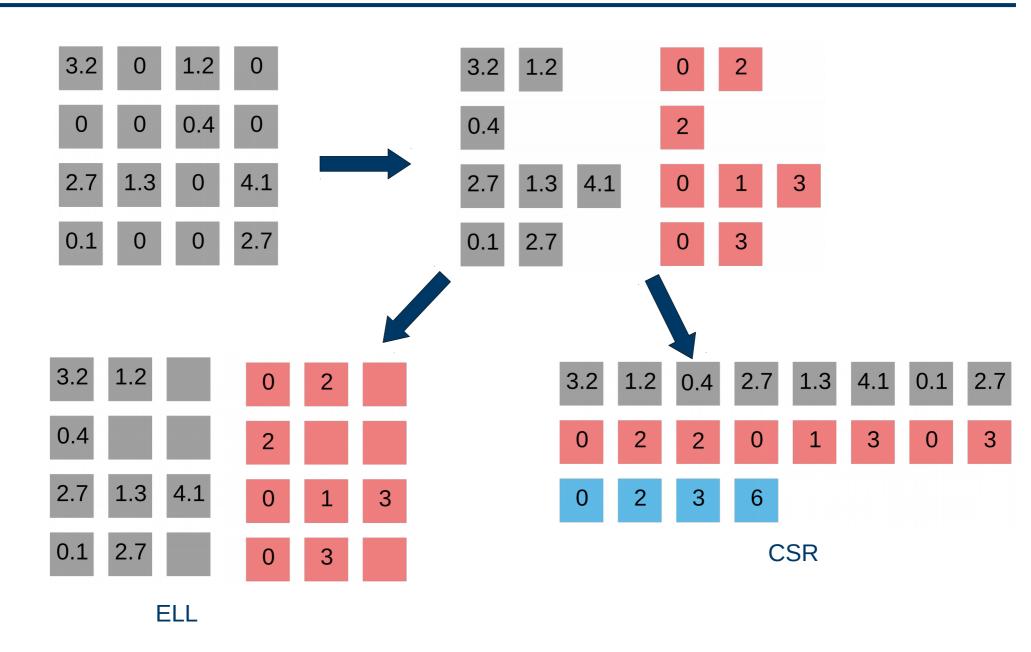
3.2 0	1.2 0		3.2 1.2
0 0	0.4 0		0.4
2.7 1.3	0 4.1		2.7 1.3 4.1
0.1 0	0 2.7		0.1 2.7

3.2 0 1.2 0	3.2 1.2	0 2		
0 0 0.4 0	0.4	2		
2.7 1.3 0 4.1	2.7 1.3 4.1	0 1 3		
0.1 0 0 2.7	0.1 2.7	0 3		

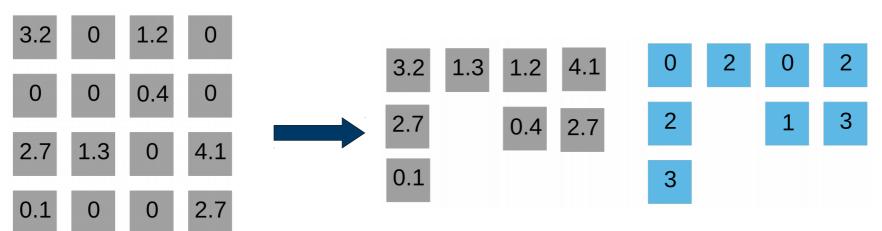




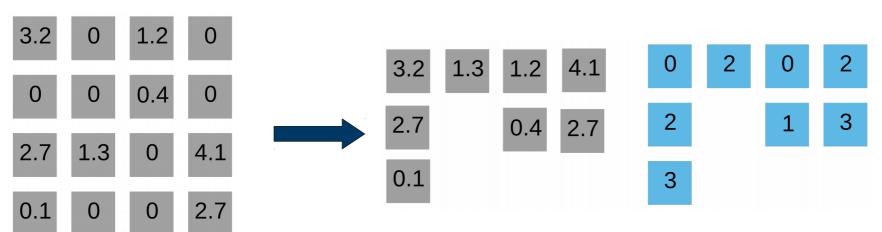




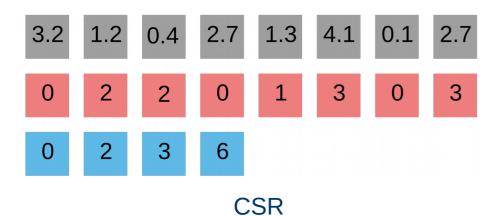




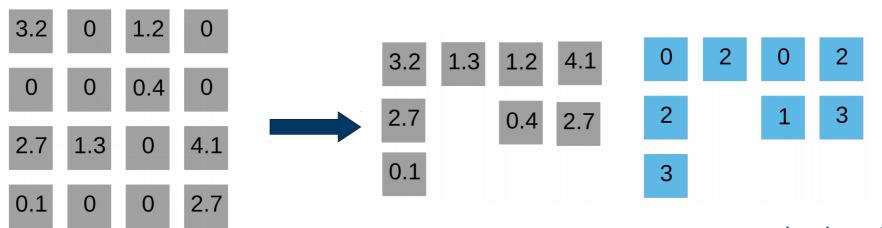
... leads to CSC



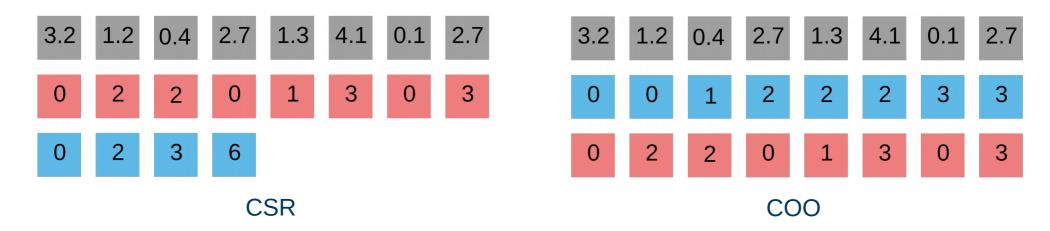
... leads to CSC



"Standard" approach

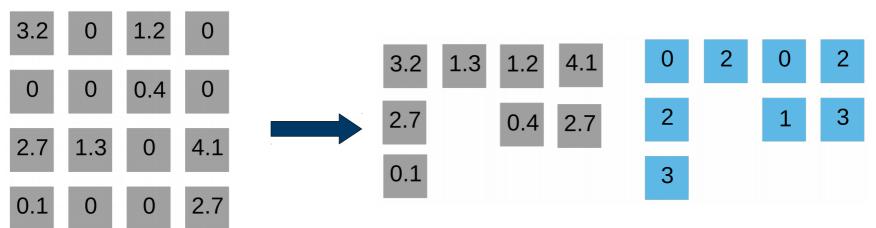


... leads to CSC

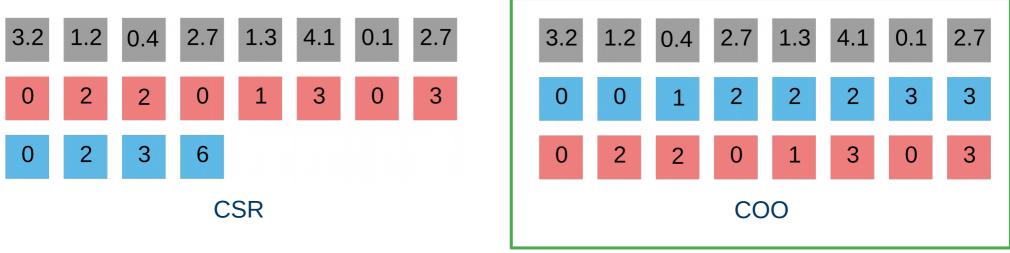


"Standard" approach

Considered inferior to CSR (memory consumption)



... leads to CSC



"Standard" approach

Considered inferior to CSR (memory consumption)

3.2	1.2	0.4	2.7	1.3	4.1	0.1	2.7	Values (val)
0	2	2	0	1	3	0	3	Column indexes (colidx)
0	2	3	6					Row pointers (rowptr)

3.2 | 1.2 | 0.4 | 2.7 | 1.3 | 4.1 | 0.1 | 2.7 | Values (val)

0 2 2 0 1 3 0 3 Column indexes (colidx)

0 2 3 6 Row pointers (rowptr)

y := Ax

```
3.2 1.2 0.4 2.7 1.3 4.1 0.1 2.7 Values (val)

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0 2 3 6 Row pointers (rowptr)

y := Ax
1 void SpMV_CSR(int m, int *rowptr, int *colidx, float *val, float *x, float *y)
```

```
void SpMV_CSR(int m, int *rowptr, int *colidx, float *val, float *x, float *y) {
  for (int i = 0; i < m; ++i) {
    for (int j = rowptr[i]; j < rowptr[i+1]; ++j)
      y[i] += val[j] * x [ colidx[j] ];
}</pre>
```

```
3.2 1.2 0.4 2.7 1.3 4.1 0.1 2.7 Values (val)

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y := Ax
void SpMV_CSR(int m, int *rowptr, int *colidx, float *val, float *x, float *y) {
for (int i = 0; i < m; ++i) {
for (int j = rowptr[i]; j < rowptr[i+1]; ++j) Bell & Garland '08
    y[i] += val[j] * x [ colidx[j] ]; • parallelize outer loop
```

~ cuSPARSE SpMV

Load imbalance! Non-coalescence!

Bell & Garland '08

parallelize outer loop

~ cuSPARSE SpMV

for (int i = 0; i < m; ++i) {

for (int j = rowptr[i]; j < rowptr[i+1]; ++j)</pre>

y[i] += val[j] * x [colidx[j]];

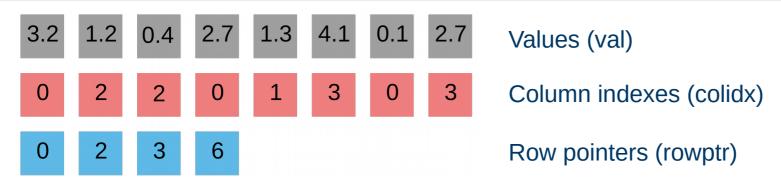


$$y := Ax$$

Specialized formats

Load imbalance! Non-coalescence!

- HYB (ELL + COO) [cuSPARSE]
- CSR5 [Liu, Vinter '15], CSR-I [Flegar, Quintana '17]
- SELL-P [Kreutzer et al.] good memory access, parallelizes well
- ... a few new ones every year



$$y := Ax$$

Specialized formats

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```
void SpMV_CSR(int m, int *rowptr, int *colidx, float *val, float *x, float *y) {
  for (int i = 0; i < m; ++i) {
    for (int j = rowptr[i]; j < rowptr[i+1]; ++j)
      y[i] += val[j] * x [ colidx[j] ];
}
</pre>
```

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void SpMV_CSR(int m, int *rowptr, int *colidx, float *val, float *x, float *y) {
   for (int i = 0; i < m; ++i) {
     for (int j = rowptr[i]; j < rowptr[i+1]; ++j)
       y[i] += val[j] * x [ colidx[j] ];
   }
                               Collapse the two loops into one.
  void SpMV_CSR(int m, int *rowptr, int *colidx, float *val, float *x, float *y) {
    int row = -1, next_row = 0, nnz = rowptr[m];
    for (int i = 0; i < nnz; ++i) {
        while (i >= next_row) next_row = rowptr[++row+1];
        y[row] += val[i] * x[ colidx[i] ];
 }}
                               Split the loop into equal chunks.
  const int T = thread_count;
  void SpMV_CSRI(int m, int *rowptr, int *colidx, float *val, float *x, float *y) {
    int row = -1, next_row = 0, nnz = rowptr[m];
    for (int k = 0; k < T; ++k) {
      for (int i = k*nnz / T; i < (k+1)*nnz / T; ++i) {
6
7
        while (i >= next_row) next_row = rowptr[++row+1];
        y[row] += val[i] * x[ colidx[i] ];
 | }}}
```

```
void SpMV_CSR(int m, int *rowptr, int *colidx, float *val, float *x, float *y) {
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3
    int row = -1, next_row = 0, nnz = rowptr[m];
   for (int k = 0; k < T; ++k) { Parallelize this!
5
      for (int i = k*nnz / T; i < (k+1)*nnz / T; ++i) {
6
7
        while (i >= next_row) next_row = rowptr[++row+1];
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3.2	1.2	0.4	2.7	1.3	4.1	0.1	2.7	Values (val)
0	0	1	2	2	2	3	3	Row indexes (rowidx)
0	2	2	0	1	3	0	3	Column indexes (colidx)

```
      3.2
      1.2
      0.4
      2.7
      1.3
      4.1
      0.1
      2.7
      Values (val)

      0
      0
      1
      2
      2
      2
      3
      3
      Row indexes (rowidx)

      0
      2
      2
      0
      1
      3
      0
      3
      Column indexes (colidx)
```

```
void SpMV_COO(int m, int *rowidx, int *colidx, float *val, float *x, float *y) {
  for (int i = 0; i < nnz; ++i) {
     y[rowidx[i]] += val[i] * x[colidx[i]];
}
</pre>
```

```
      3.2
      1.2
      0.4
      2.7
      1.3
      4.1
      0.1
      2.7
      Values (val)

      0
      0
      1
      2
      2
      2
      3
      3
      Row indexes (rowidx)

      0
      2
      2
      0
      1
      3
      0
      3
      Column indexes (colidx)
```

```
void SpMV_COO(int m, int *rowidx, int *colidx, float *val, float *x, float *y) {
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     y[rowidx[i]] += val[i] * x[colidx[i]];
}</pre>
```



Split the loop into equal chunks.

```
const int T = thread_count;
void SpMV_COO(int m, int *rowidx, int *colidx, float *val, float *x, float *y) {
  for (int k = 0; k < T; ++k) {
    for (int i = k*nnz / T; i < (k+1)*nnz / T; ++i) {
      y[rowidx[i]] += val[i] * x[colidx[i]];
}</pre>
```

```
      3.2
      1.2
      0.4
      2.7
      1.3
      4.1
      0.1
      2.7
      Values (val)

      0
      0
      1
      2
      2
      2
      3
      3
      Row indexes (rowidx)

      0
      2
      2
      0
      1
      3
      0
      3
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```
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    for (int i = k*nnz / T; i < (k+1)*nnz / T; ++i) {
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}</pre>
```

COO vs CSR-I SpMV

COO:

```
const int T = thread_count;
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      y[rowidx[i]] += val[i] * x[colidx[i]];
}
</pre>
```

CSR-I:

```
const int T = thread_count;
void SpMV_CSRI(int m, int *rowptr, int *colidx, float *val, float *x, float *y) {
   int row = -1, next_row = 0, nnz = rowptr[m];
   for (int k = 0; k < T; ++k) {
      for (int i = k*nnz / T; i < (k+1)*nnz / T; ++i) {
      while (i >= next_row) next_row = rowptr[++row+1];
      y[row] += val[i] * x[ colidx[i] ];
}
}}
```

COO vs CSR-I SpMV

COO:

}}}

```
const int T = thread_count;
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    for (int k = 0; k < T; ++k) {
        for (int i = k*nnz / T; i < (k+1)*nnz / T; ++i) {
            [y[rowidx[i]]] += val[i] * x[colidx[i]];
    }

CSR-I:

const int T = thread_count;
void SpMV_CSRI(int m, int *rowptr, int *colidx, float *val, float *x, float *y) {
        int row = -1, next_row = 0, nnz = rowptr[m];
        for (int k = 0; k < T; ++k) {
            for (int i = k*nnz / T; i < (k+1)*nnz / T; ++i) {
                while (i >= next_row) next_row = rowptr[++row+1];
                y[row] += val[i] * x[colidx[i]];
```

Race conditions!



COO vs CSR-I SpMV

COO:

```
const int T = thread_count;
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    for (int k = 0; k < T; ++k) {
      for (int i = k*nnz / T; i < (k+1)*nnz / T; ++i) {
        y[rowidx[i]] += val[i] * x[colidx[i]];
6 }}
```

CSR-I:

```
const int T = thread_count;
  void SpMV_CSRI(int m, int *rowptr, int *colidx, float *val, float *x, float *y) {
    int row = -1, next_row = 0, nnz = rowptr[m];
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7
        while (i >= next_row) next_row = rowptr[++row+1];
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 }}}
```

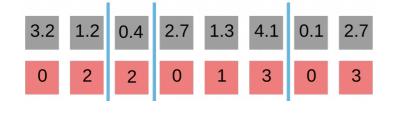
Use atomics

Race conditions! • Accumulate partial result into registers

CUDA thread = 1 lane of a 32-wide SIMD unit (warp) – shared cache lines!

Spreading out threads causes strided memory access.

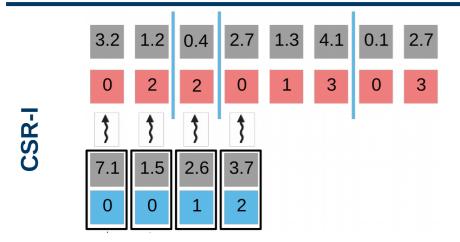
Assign one warp per chunk.

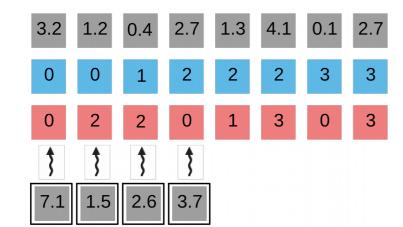


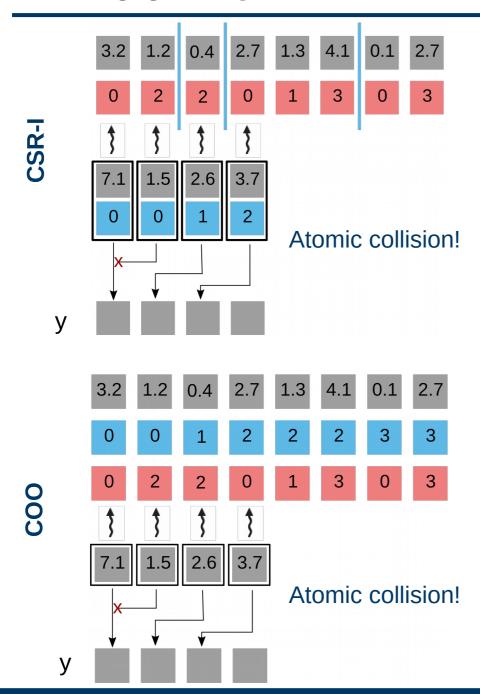
0.4

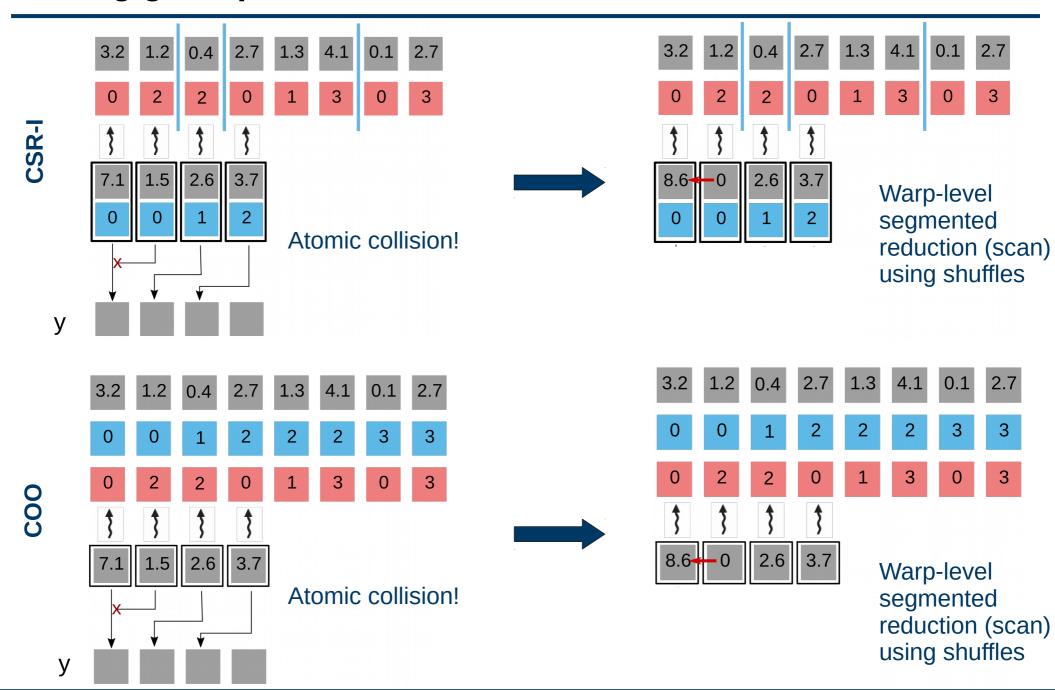
3.2	1.2	0.4	2.7	1.3	4.1	0.1	2.7
0	0	1	2	2	2	3	3
0	2	2	0	1	3	0	3

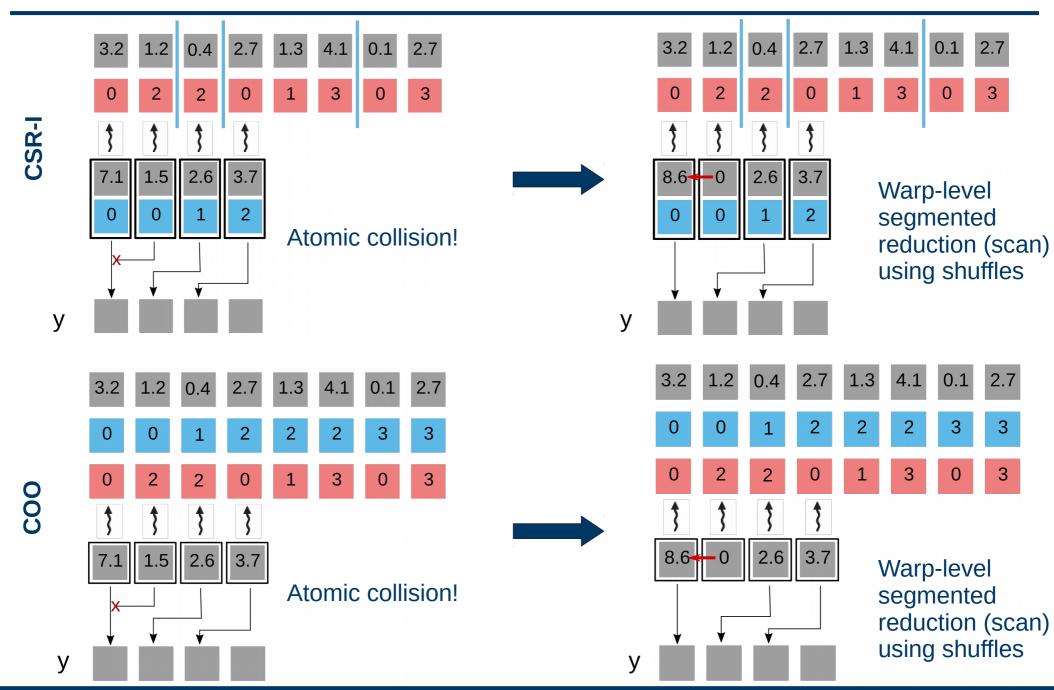






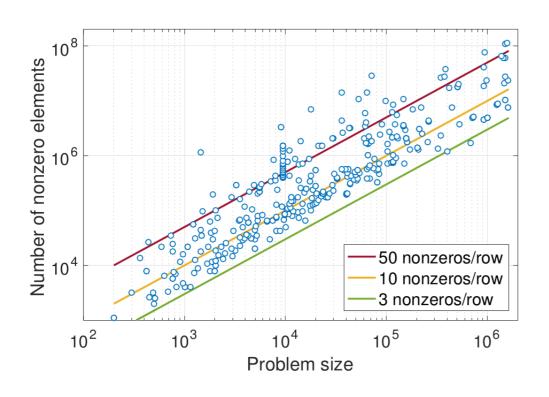


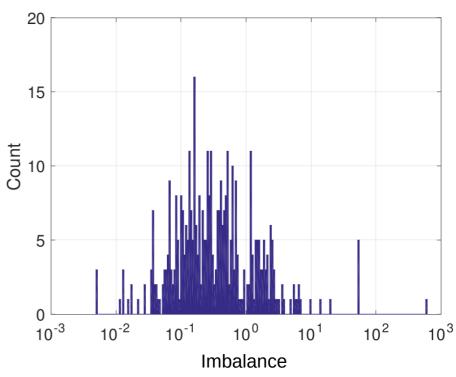




Test matrices

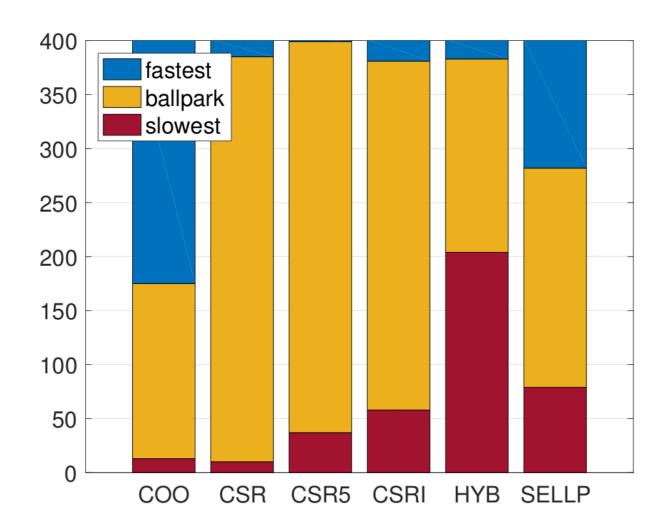
400 matrices from SuiteSparse matrix collection







Performance / format histogram

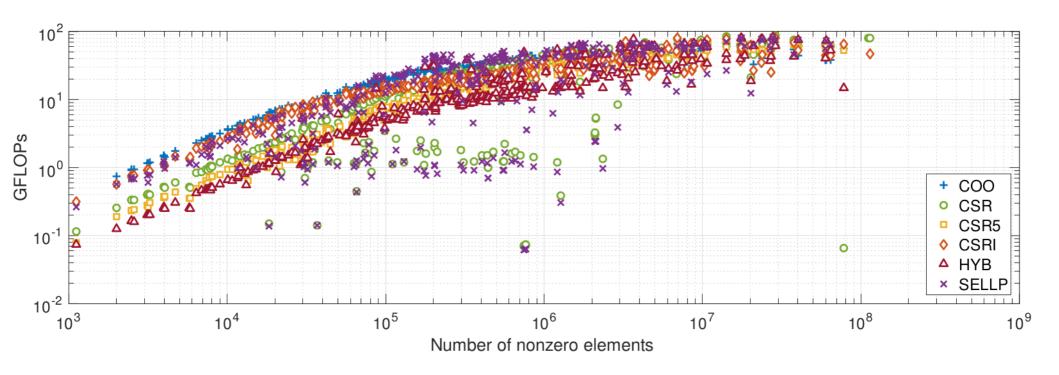


COO wins most of the cases!

* P100 on Piz-Daint supercomputer @ CSCS



(Too) detailed performance plot



COO is superior for small matrices!



Basic statistics

Kernel	min	max	average	median	standard-dev.
C00	24.29	64.32	38.86	37.24	9.16
CSR	0.07	87.43	32.77	30.43	20.07
CSR5	9.66	75.56	31.79	27.15	15.58
CSRI	13.47	81.21	31.85	26.84	14.44
HYB	6.64	82.43	27.98	18.74	20.22
SELLP	0.06	82.62	36.42	38.64	22.46

COO has good average & small deviation!

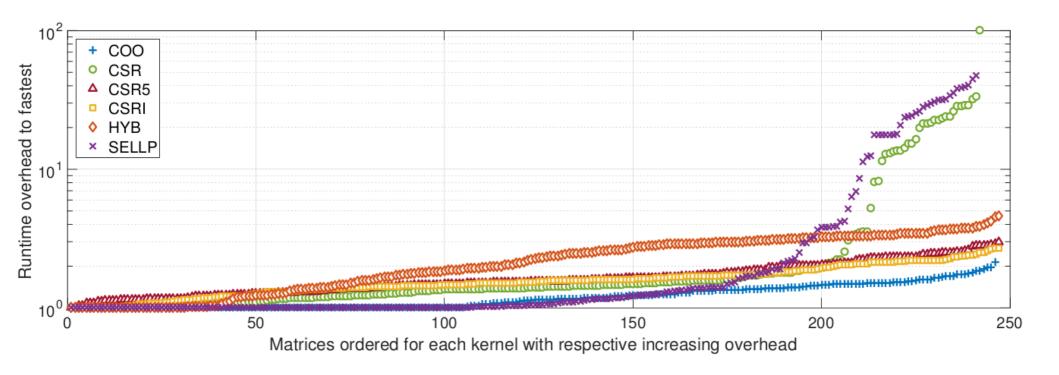


Basic statistics

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C00	24.29	64.32	38.86	37.24		9.16			
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CSRI	13.47	81.21	21 95	26.84		11 11			
HYB	6.64	82.43							
SELLP	0.06	82.62							
			GFLOPs	10 ¹					
			GFI	10 ⁰					
				10 ⁻¹					
				COO	CSR	CSR5	CSRI	HYB	SELLP

COO has good average & small deviation!

Runtime comparison



COO is never "slow"!



Conclusion

No "holy grail" format / algorithm for SpMV.

• COO is a good all-rounder.

Re-visiting "forgotten" formats may pay of.

Atomics + warp shuffles are sometimes a good alternative to reduction.

Thank you! Questions?

All functionalities are part of the MAGMA-sparse project.

MAGMA SPARSE

ROUTINES BiCG, BiCGSTAB, Block-Asynchronous Jacobi, CG,

CGS, GMRES, IDR, Iterative refinement, LOBPCG,

LSQR, QMR, TFQMR

PRECONDITIONERS ILU / IC, Jacobi, ParlLU, ParlLUT, Block Jacobi, ISAI

KERNELS SpMV, SpMM

DATA FORMATS CSR, ELL, SELL-P, CSR5, HYB

http://icl.cs.utk.edu/magma/



github.com/gflegar/talks/tree/master/sc 2017

This research is based on a cooperation between Hartwig Anzt (Karlsruhe Institute of Technology, University of Tennessee) and Goran Flegar (Universidad Jaume I).





