

Flexible-Size Batched LU for Small Matrices and its Integration into Block-Jacobi Preconditioning

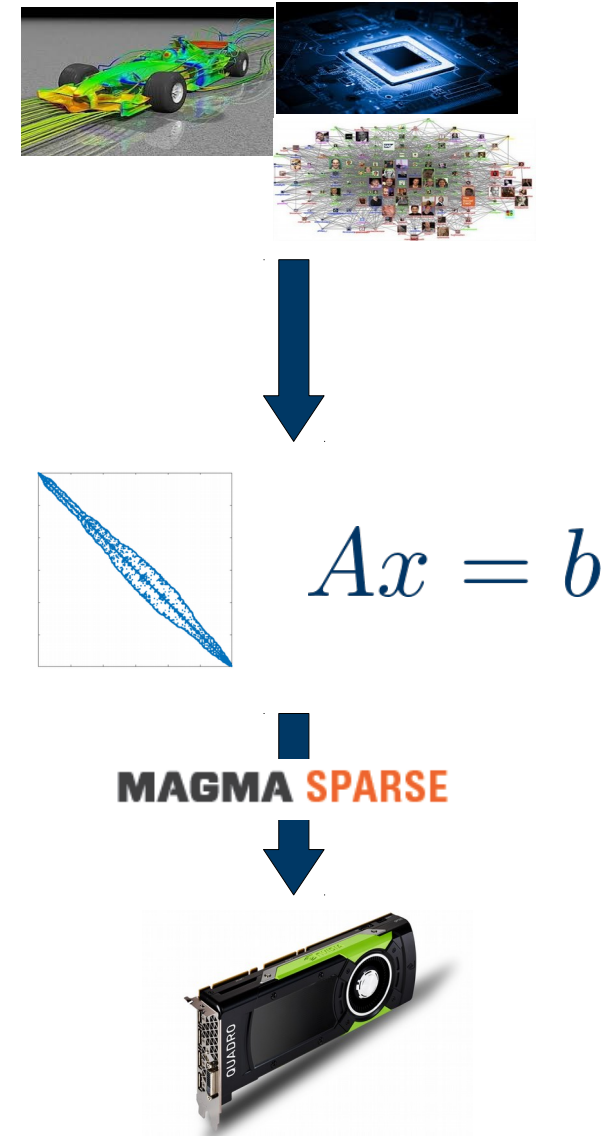
Hartwig Anzt, Jack Dongarra, [Goran Flegar](#), Enrique S. Quintana-Ortí



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MAGMA-sparse software library

- GPU-accelerated sparse linear algebra library
 - Focus: linear systems

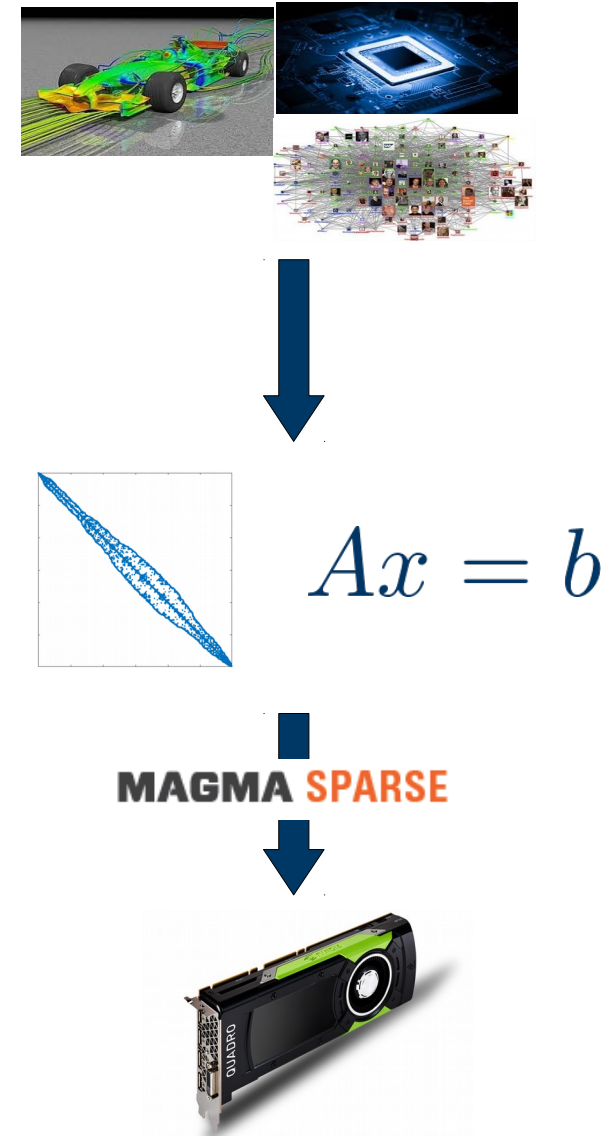


Joint effort: Innovative Computing Lab at University of Tennessee, Knoxville; Karlsruhe Institute of Technology; University Jaume I



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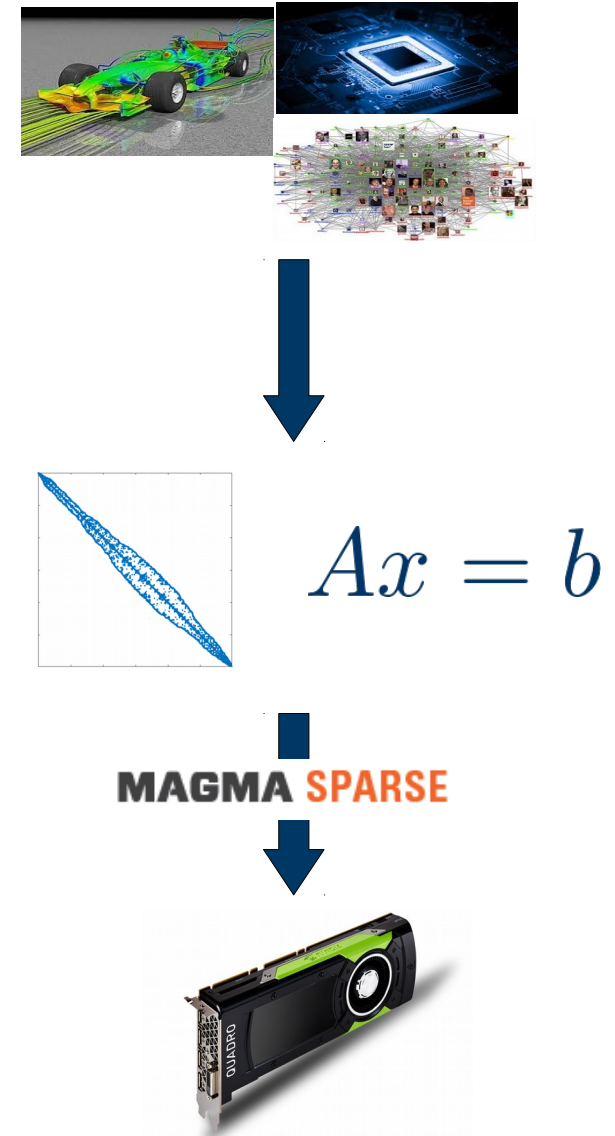
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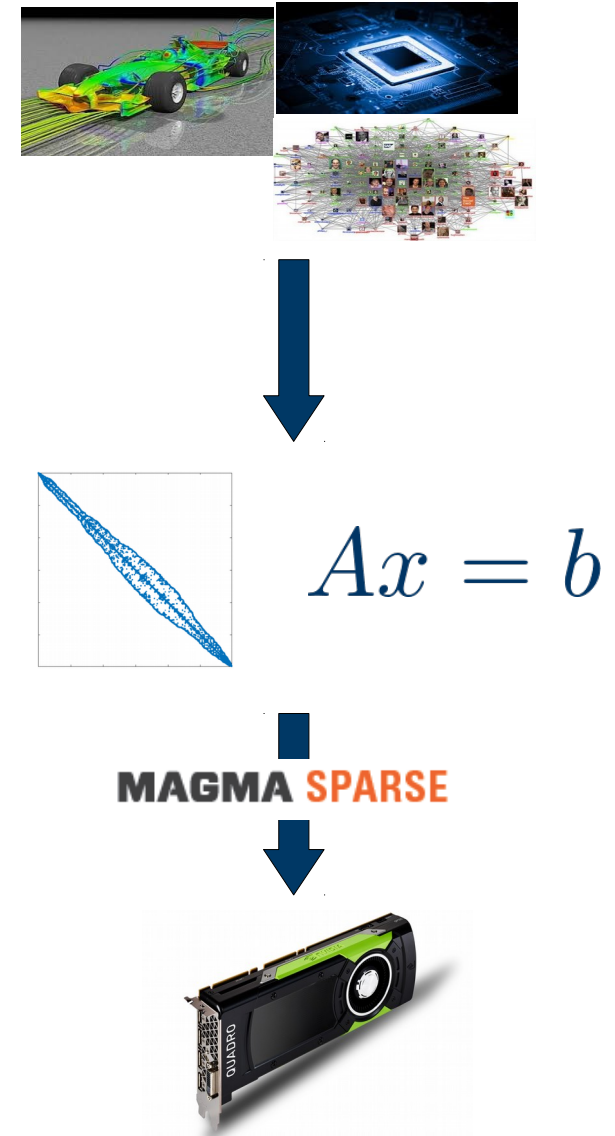
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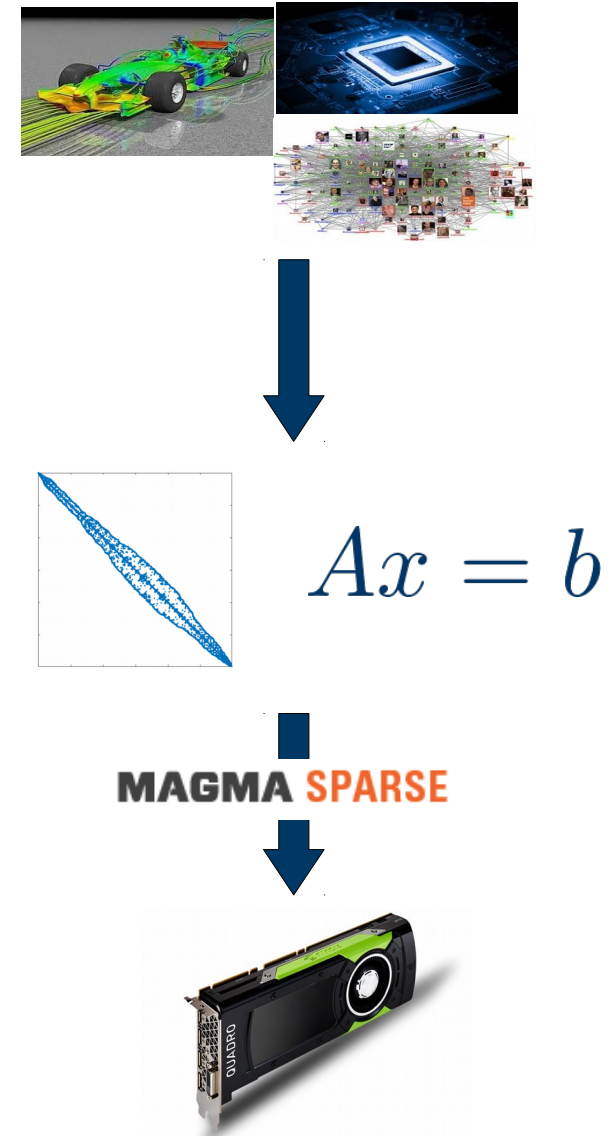
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Generate the preconditioner matrix, and store it in a form suitable for application

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Preconditioner setup



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Trade-off:

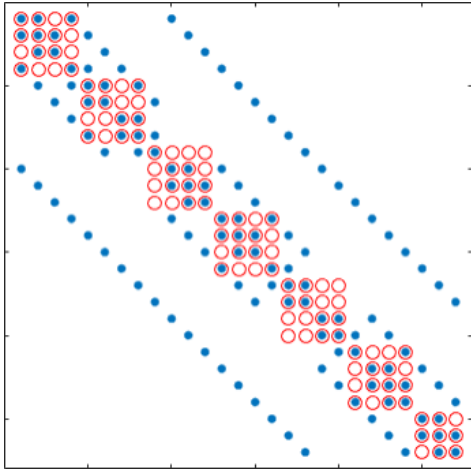
faster convergence,
but more work per iteration

Block-Jacobi Preconditioning

- Current focus: improve performance for problems with inherent block structure
 - Usually blocks are smaller than 30×30 (blocks can be of different sizes!)

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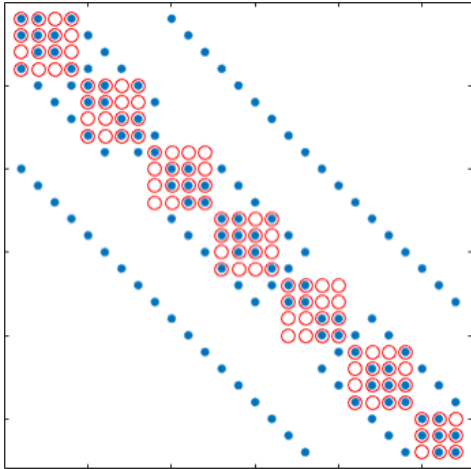
- Block-Jacobi preconditioning
 - Use only diagonal blocks for approximation

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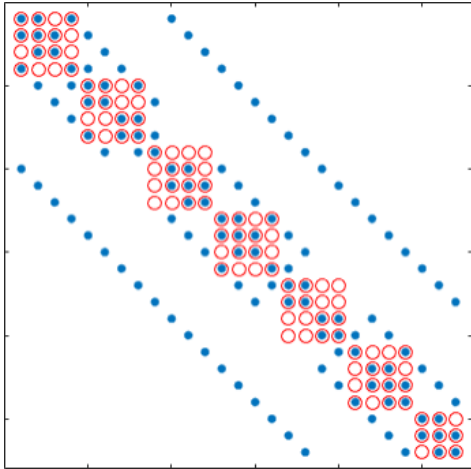
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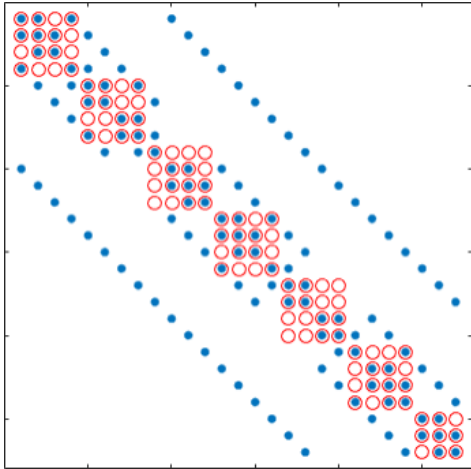
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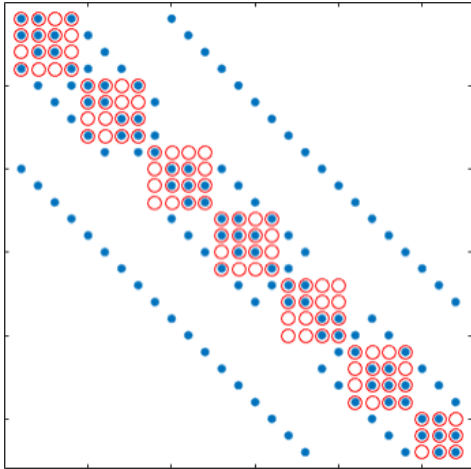
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$$\begin{aligned} \longrightarrow D_i y_i = z_i &\longrightarrow D_i = L_i U_i \\ &U_i y_i = w_i \\ &L_i w_i = z_i \end{aligned}$$

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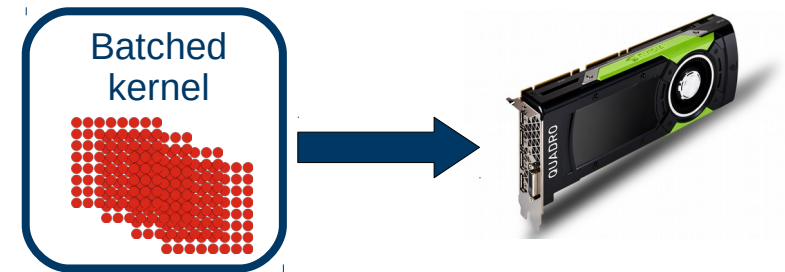
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$$\longrightarrow D_i y_i = z_i \longrightarrow \begin{array}{l} \boxed{D_i = L_i U_i} \text{ Setup} \\ \boxed{\begin{array}{l} U_i y_i = w_i \\ L_i w_i = z_i \end{array}} \text{ Application} \end{array}$$

Solving 30-by-30 systems in sequence on
a GPU with several thousand cores
wastes computational resources!

Batched routines

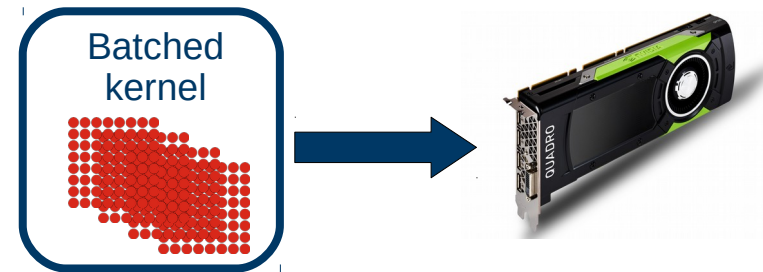
Launch a **single kernel** which applies an operation to **multiple independent data entities** in parallel.



** Measured on NVIDIA P100*

Batched routines

Launch a **single kernel** which applies an operation to **multiple independent data entities** in parallel.



- There is no standard BLAS & LAPACK interface
- Most implementations only support problems of equal sizes
- High performance libraries are not optimized for small blocks
 - cuBLAS batched trsv: **~25 Gflop/s** *
 - MAGMA-sparse SpMV: **60 – 90 Gflop/s** *

** Measured on NVIDIA P100*

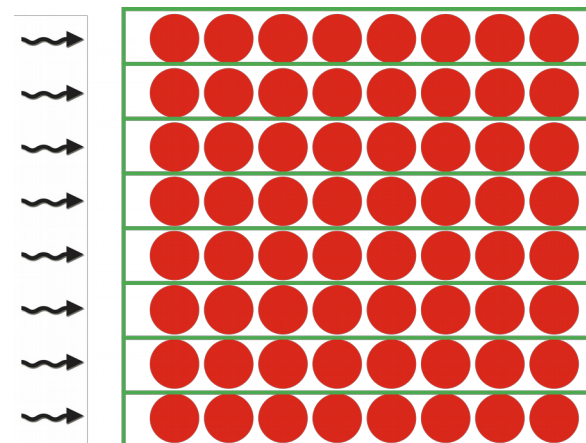
MAGMA-sparse LU & trsv outline

- Assign one warp to each problem
 - hardware SIMD unit, represented as a group of 32 threads in CUDA



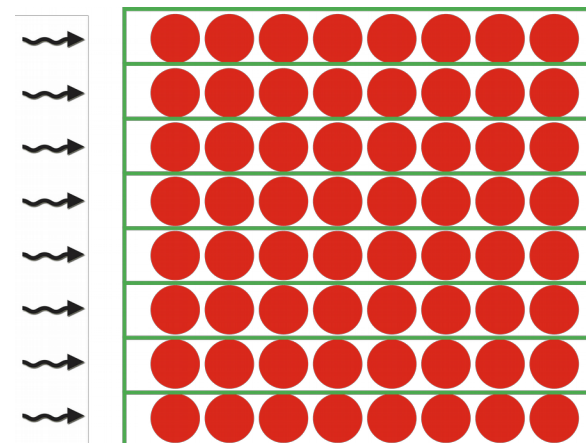
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- Assign **one warp to each problem**
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- Process each row by a single thread
 - Able to support problems of size up to 32-by-32
 - keep the entire row in thread's **registers**
 - Communicate data between rows via **warp-shuffles**
 - Current implementation: **use padding for problems of smaller sizes**
 - Future work: **multiple smaller problems per warp**



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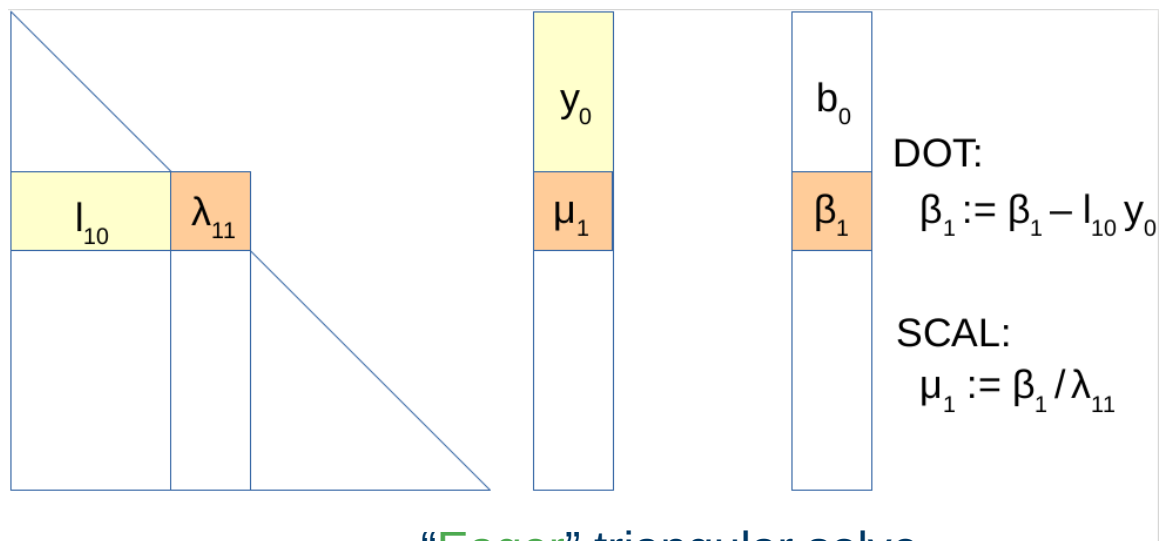
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- Use implicit pivoting
 - Do not explicitly swap rows, “re-assign” the threads instead



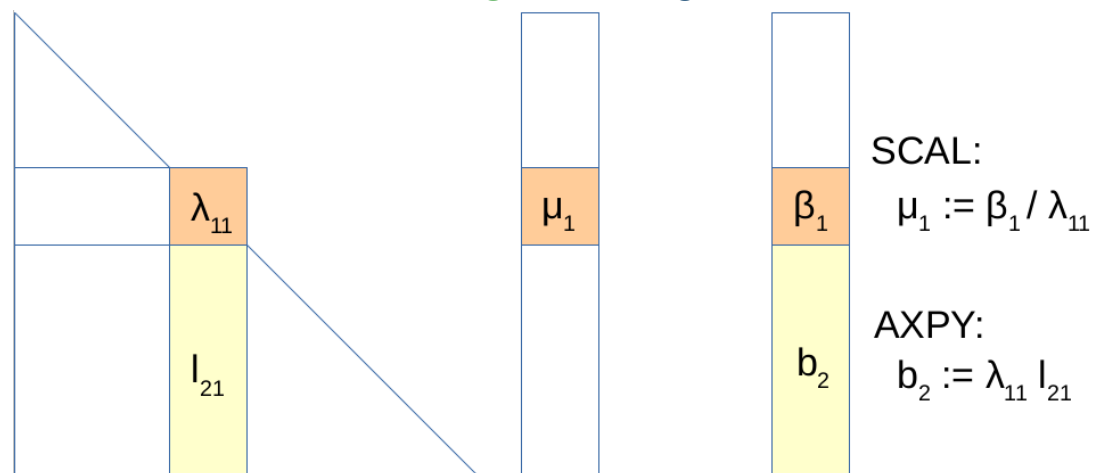
MAGMA-sparse LU & trsv outline

- Use “eager” triangular solves
 - Cast solution vector updates in terms of axpy, not in terms of dot product!

“Lazy” triangular solve



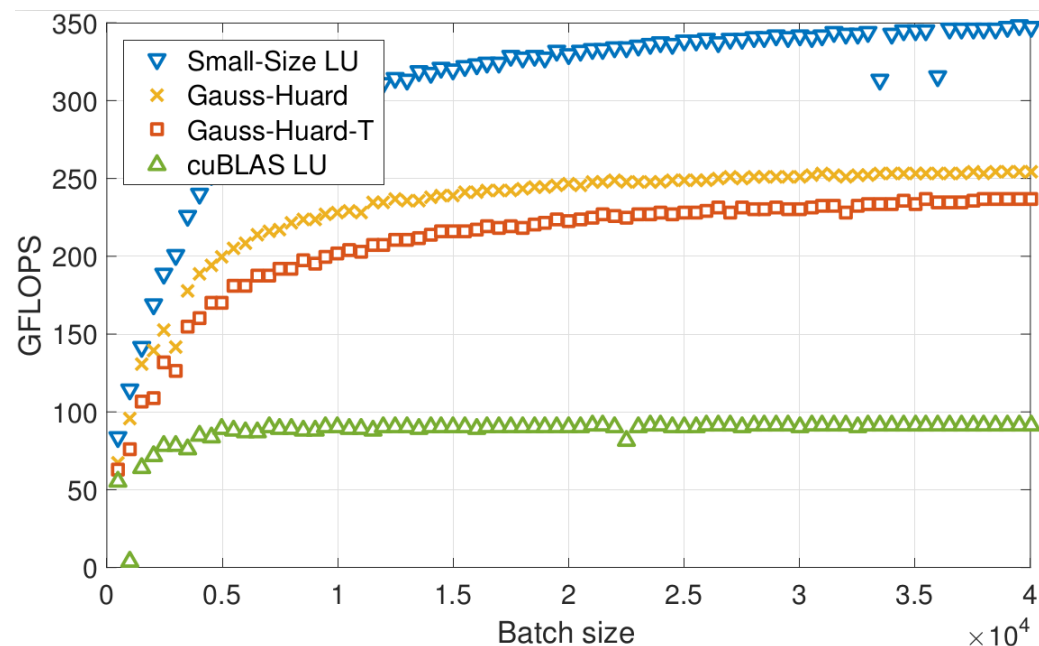
“Eager” triangular solve



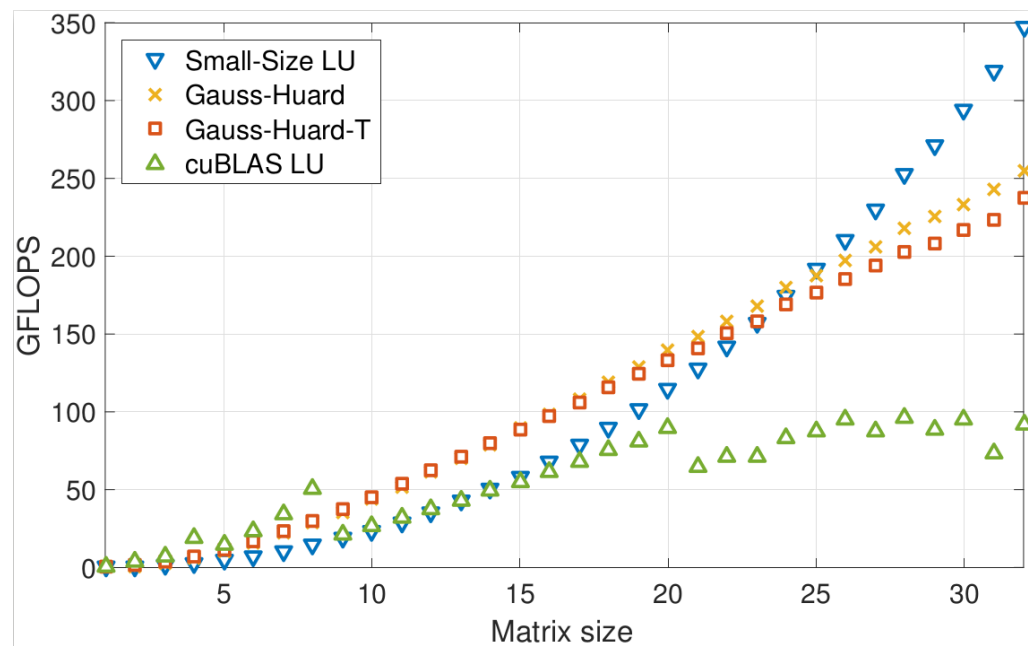
LU decomposition performance

- Comparisson of MAGMA-sparse vs cuBLAS batched LU decomposition
- Gauss-Huard(-T) is a similar approach, using a different algorithm for decomposition/solves *

Fixed problem size (32)



Fixed batch size (40,000)

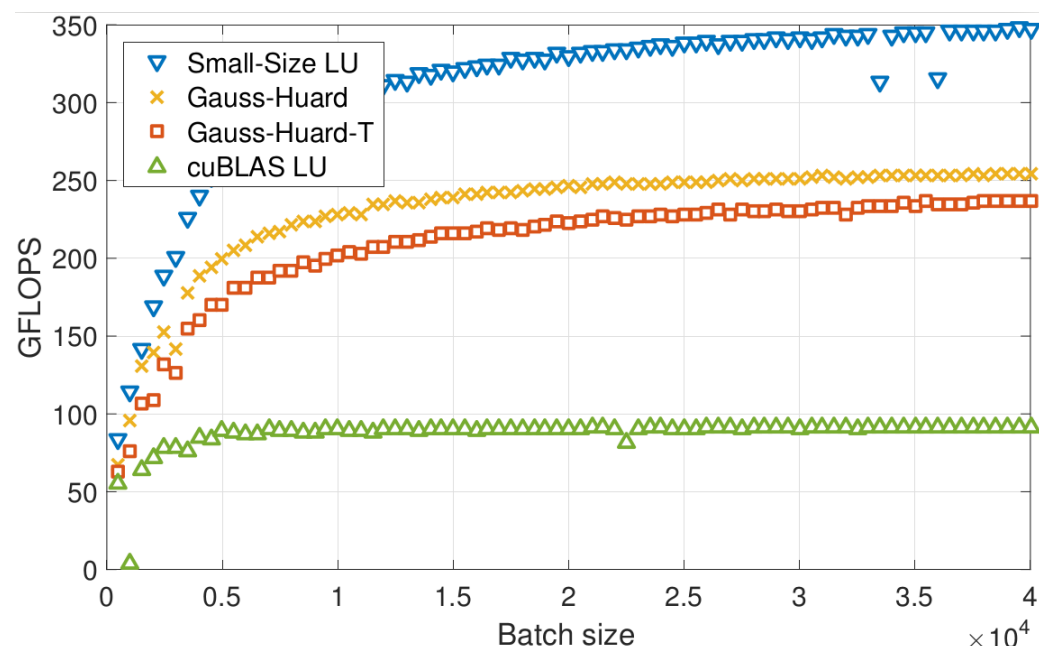


* Anzt et al., Variable-Size Batched Gauss-Huard for Block-Jacobi Preconditioning, ICCS'17

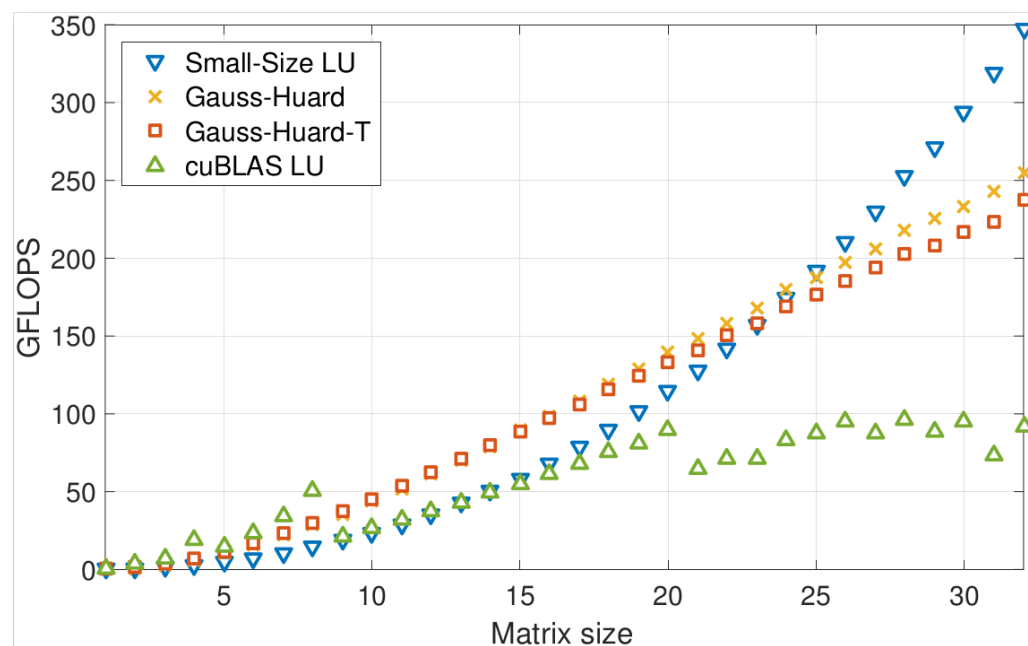
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MAGMA-sparse LU can also:

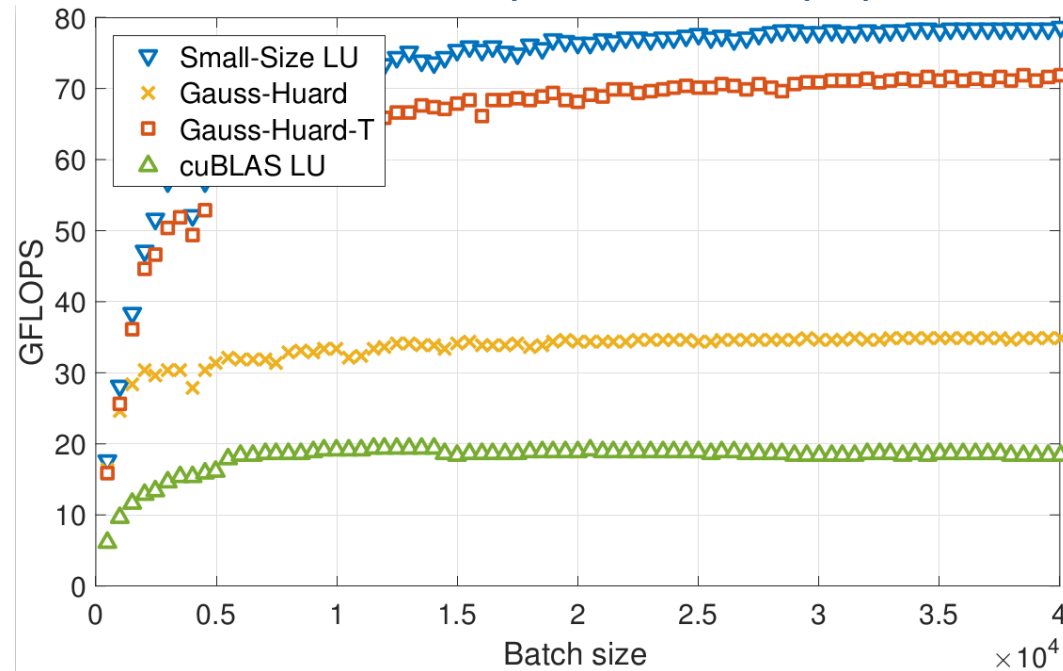
- Handle problems of different sizes
- Integrate diagonal block extraction and diagonal block decomposition into a single kernel

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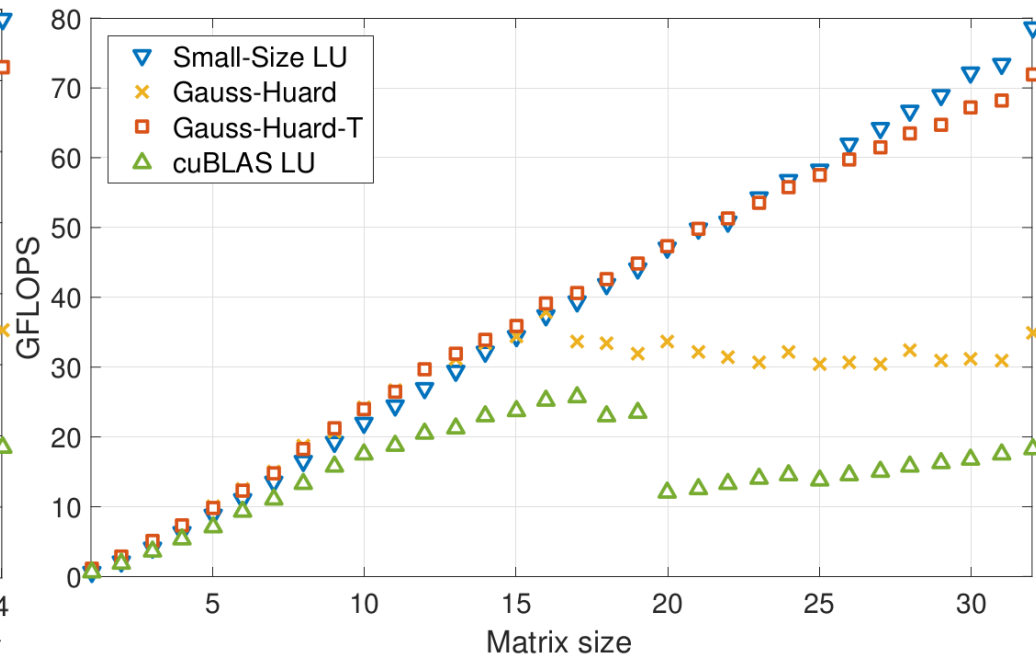
Triangular solve performance

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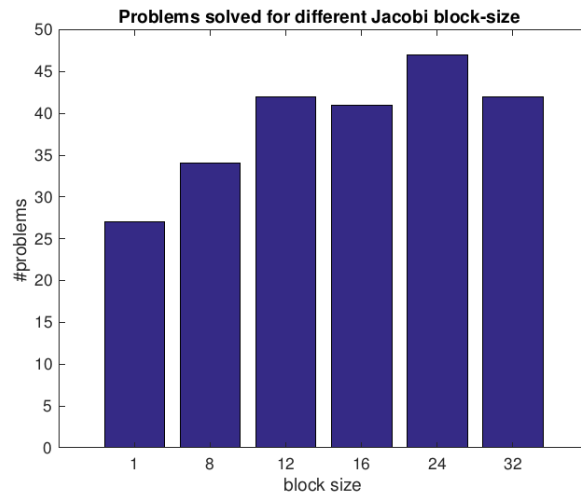


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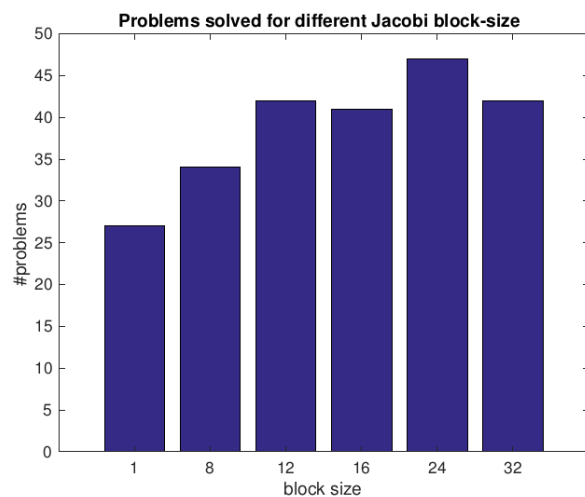
Complete solver runtime

56 problems from SuitSparse

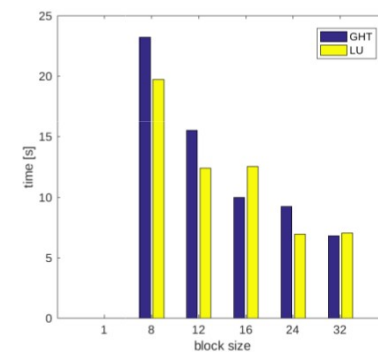
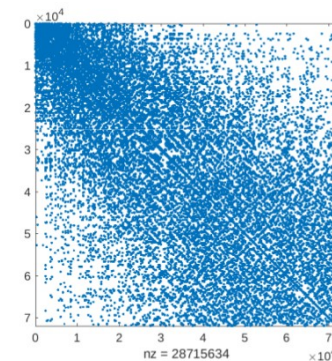


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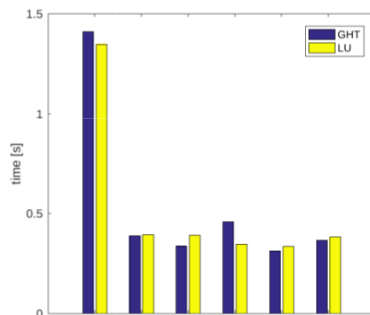
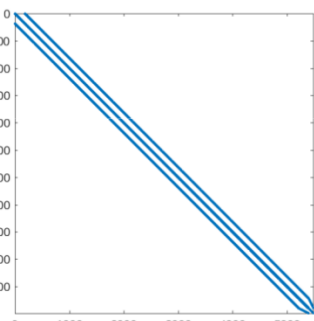
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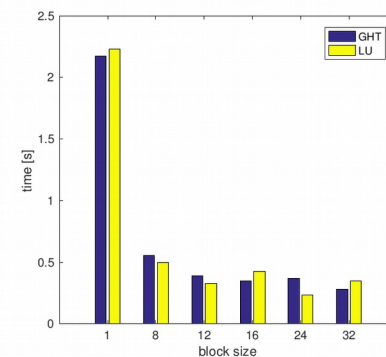
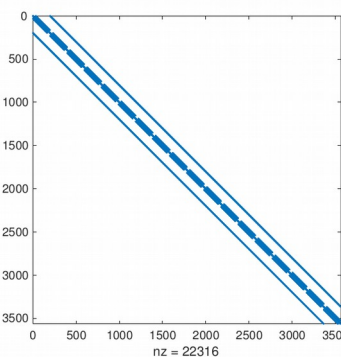
nd24k



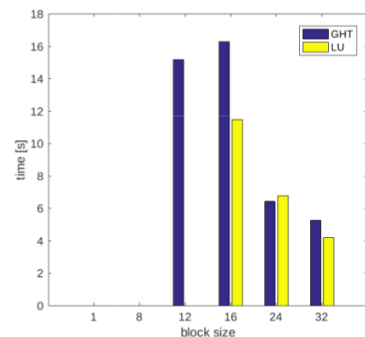
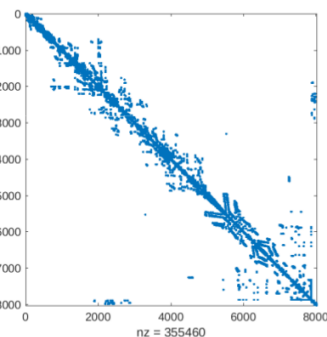
s2rmt3m1



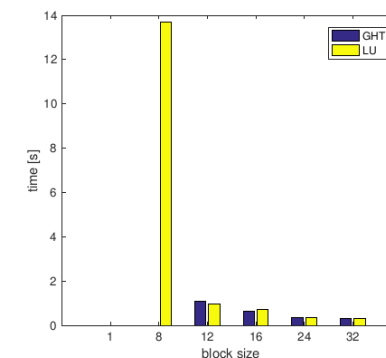
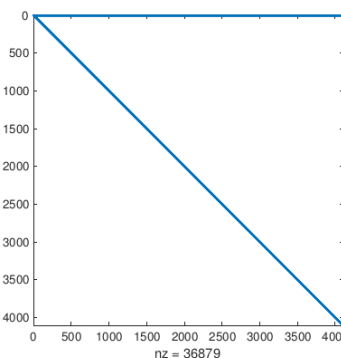
saylr4



bcsstk38



Chebyshev3



Conclusion

“Solving many **small** problems in sequence on manycore hardware wastes computational resources! We can design **batched routines** which apply the same operation on a set of independent data entities.”

Workshop on batched BLAS*

- Effort to **standardize** the batched BLAS interface

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- **Global synchronization** between two batched calls.

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Instead provide BLAS which operates on a part of memory/core hierarchy?

- E.g. block, warp, thread level BLAS for CUDA.
- Let users build their own batched routines from these building blocks.

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Thank you! Questions?

All functionalities are part of the MAGMA-sparse project.

MAGMA SPARSE

ROUTINES BiCG, BiCGSTAB, Block-Asynchronous Jacobi, CG, CGS, GMRES, IDR, Iterative refinement, LOBPCG, LSQR, QMR, TFQMR

PRECONDITIONERS ILU / IC, Jacobi, ParILU, ParILUT, Block Jacobi, ISAI

KERNELS SpMV, SpMM

DATA FORMATS CSR, ELL, SELL-P, CSR5, HYB

<http://icl.cs.utk.edu/magma/>

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github.com/gflegar/talks/icpp_2017

This research is based on a cooperation between Hartwig Anzt, Jack Dongarra (University of Tennessee), Goran Flegar and Enrique S. Quintana-Ortí (Universitat Jaume I).



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