Experience with Triton Lowering and Optimization for Qualcomm[®] Hexagon™ NPU Target

Javed Absar, Principal Engineer, Qualcomm Technologies International, Ltd. Muthu M. Baskaran, Principal Engineer, Qualcomm Technologies, Inc.

Contents

- What is Triton?
- Triton to Linalg
- Triton-Linalg to Hexagon
- Use case example
- Discussions

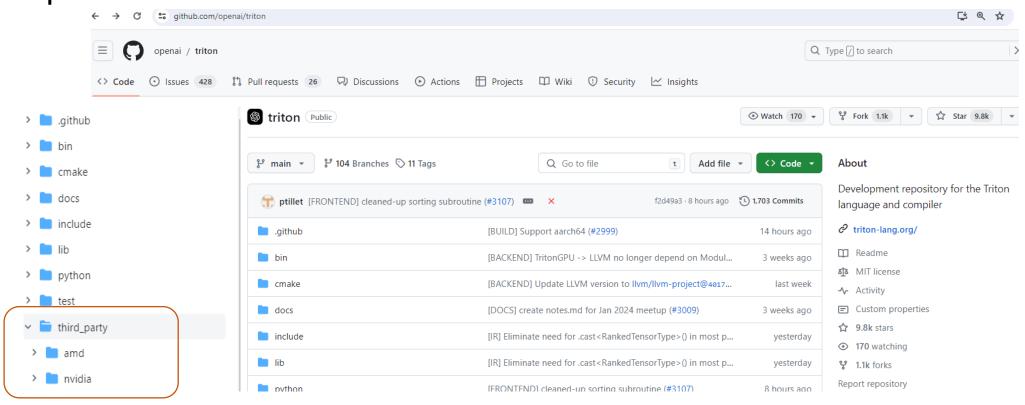
What is Triton?

- Python DSL to write ML kernels
 - Low development time / high performance
- Language and Compiler



What is Triton?

- Pioneered at Open-Al for NVIDIA GPUs
- Open-sourced



Softmax using Torch

$$softmax(X)_{i} = \frac{e^{X_{i}-X_{max}}}{\sum_{i=1}^{N} e^{X_{i}-X_{max}}}$$

```
@torch.jit.script
def naive softmax(x):
    """Compute row-wise softmax of X using native pytorch.
    We subtract the maximum element in order to avoid overflows. Softmax is invariant to
    this shift.
    0.000
    # read MN elements ; write M elements
   x max = x.max(dim=1)[0]
    # read MN + M elements ; write MN elements
    z = x - x \max[:, None]
    # read MN elements ; write MN elements
    numerator = torch.exp(z)
    # read MN elements ; write M elements
    denominator = numerator.sum(dim=1)
    # read MN + M elements ; write MN elements
    ret = numerator / denominator[:, None]
    # in total: read 5MN + 2M elements ; wrote 3MN + 2M elements
    return ret
```

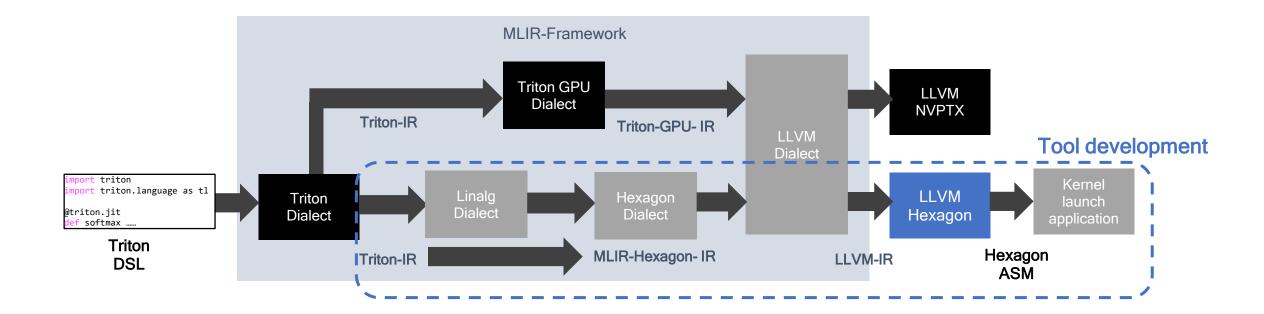
Softmax using Triton

```
# Triton softmax kernel works as follows: each program loads a row of the input matrix X,
# normalizes it and writes back the result to the output Y.
@torch.jit.script
def softmax kernel(output ptr, input ptr, input row stride, output row stride, n cols, BLOCK SIZE: tl.constexpr):
    # The rows of the softmax are independent, so we parallelize across those
    row idx = tl.program id(0)
    # The stride represents how much we need to increase the pointer to advance 1 row
    row start ptr = input ptr + row idx * input row stride
    col offsets = tl.arange(0, BLOCK SIZE)
    input ptrs = row start ptr + col offsets
    # Load the row into SRAM, using a mask since BLOCK SIZE may be > than n cols
    row = tl.load(input ptrs, mask=col offsets < n cols, other=-float('inf'))</pre>
    # Subtract maximum for numerical stability
    row minus max = row - tl.max(row, axis=0)
    # Note that exponentiation in Triton is fast but approximate (i.e., think expf in CUDA)
    numerator = tl.exp(row minus max)
    denominator = tl.sum(numerator, axis=0)
    softmax output = numerator / denominator
    # Write back output to DRAM
    output row start ptr = output ptr + row idx * output row stride
    output ptrs = output row start ptr + col offsets
    tl.store(output ptrs, softmax output, mask=col offsets < n cols)</pre>
```

Our Triton Work

- Started last year
- Small team
- Two approaches
 - Direct from Triton-IR to LLVM-IR
 - Triton to Linalg

Our Triton Flow



Target Architecture

- Hexagon Processors
 - 4-way multi-threaded VLIW
 - Hexagon Vector eXtensions (HVX) SIMD co-processor
 - Vector registers, vector compute elements, and dedicated memory
 - Two vector lengths 512 bits (64B), 1024 bits (128B)

Triton Lowering

$$softmax(X)_{i} = \frac{e^{X_{i}-X_{max}}}{\sum_{i=1}^{N} e^{X_{i}-X_{max}}}$$

```
# Triton softmax kernel works as follows: each program loads a row of the input matrix X,
# normalizes it and writes back the result to the output Y.
@torch.jit.script
def softmax kernel(output ptr, input ptr, input row stride, output row stride, n cols, BLOCK SIZE: tl.constexpr):
    # The rows of the softmax are independent, so we parallelize across those
    row idx = tl.program id(0)
    # The stride represents how much we need to increase the pointer to advance 1 row
    row start ptr = input ptr + row idx * input row stride
    col offsets = tl.arange(0, BLOCK SIZE)
    input ptrs = row start ptr + col offsets
    # Load the row into SRAM, using a mask since BLOCK SIZE may be > than n cols
    row = tl.load(input ptrs, mask=col offsets < n cols, other=-float('inf'))</pre>
    # Subtract maximum for numerical stability
    row minus max = row - tl.max(row, axis=0)
    # Note that exponentiation in Triton is fast but approximate (i.e., think expf in CUDA)
    numerator = tl.exp(row minus max)
    denominator = tl.sum(numerator, axis=0)
    softmax output = numerator / denominator
    # Write back output to DRAM
    output row start ptr = output ptr + row idx * output row stride
    output ptrs = output row start ptr + col offsets
    tl.store(output ptrs, softmax output, mask=col offsets < n cols)</pre>
```

Triton IR

```
tt.func public @softmax (%arg0: !tt.ptr<f32, 1> ... ) {
   \%0 = \text{tt.make range } \{\text{end} = 1024 : i32, \text{start} = 0 : i32\} : \text{tensor} < 1024 \times i32 > loc(\#loc2)
   %1 = arith.muli %arg6, %arg2 : i32 loc(#loc3)
   %2 = tt.addptr %arg1, %1 : !tt.ptr<f32, 1>, i32 loc(#loc4)
    . . .
    %9 = tt.load %6, %8, %cst {cache = 1 : i32, evict = 1 : i32, isVolatile = false} : tensor<1024xf32> loc(#loc1)
   %10 = "tt.reduce"(%9) ({
    ^bb0(%arg9: f32 loc(unknown), %arg10: f32 loc(unknown)):
     %23 = arith.maximumf %arg9, %arg10 : f32 loc(#loc28)
      tt.reduce.return %23 : f32 loc(#loc24)
    }) {axis = 0 : i32} : (tensor<1024xf32>) -> f32 loc(#loc24)
   %11 = tt.splat %10 : (f32) -> tensor<1024xf32> loc(#loc12)
   %12 = arith.subf %9, %11 : tensor<1024xf32> loc(#loc12)
   %13 = math.exp %12 : tensor<1024xf32> loc(#loc13)
   %14 = "tt.reduce"(%13) ({
    ^bb0(%arg9: f32 loc(unknown), %arg10: f32 loc(unknown)):
     %23 = arith.addf %arg9, %arg10 : f32 loc(#loc29)
      tt.reduce.return %23 : f32 loc(#loc26)
    }) {axis = 0 : i32} : (tensor<1024xf32>) -> f32 loc(#loc26)
    tt.return loc(#loc23)
  } loc(#loc)
} loc(#loc)
```

Linalg Conversion (Microsoft Team)

```
%6 = bufferization.to tensor %alloc restrict writable : memref<1024xf32>
   %7 = bufferization.alloc tensor() : tensor<f32>
    %inserted = tensor.insert %cst into %7[] : tensor<f32>
    %reduced = linalg.reduce ins(%6 : tensor<1024xf32>) outs(%inserted : tensor<f32>)
        dimensions = [0] (%in: f32, %init: f32) {
        %21 = arith.maximumf %in, %init : f32
        linalg.yield %21 : f32
    %extracted = tensor.extract %reduced[] : tensor<f32>
    %8 = tensor.empty() : tensor<1024xf32>
    %9 = linalg.fill ins(%extracted : f32) outs(%8 : tensor<1024xf32>) -> tensor<1024xf32>
    %10 = linalg.generic {indexing maps = [#map, #map, #map], iterator types = ["parallel"]}
      ins(%6, %9 : tensor<1024xf32>, tensor<1024xf32>) outs(%6 : tensor<1024xf32>) {
    ^bb0(%in: f32, %in 7: f32, %out: f32):
     %21 = arith.subf %in, %in 7 : f32
     linalg.yield %21 : f32
    } -> tensor<1024xf32>
    %11 = linalg.generic {indexing maps = [#map, #map],
                          iterator types = ["parallel"]}
      ins(%10 : tensor<1024xf32>) outs(%10 : tensor<1024xf32>) {
    ^bb0(%in: f32, %out: f32):
     |\%21 = math.exp \%in : f32
     linalg.yield %21 : f32
      -> tensor<1024xf32>
```

Fusion

```
%6 = bufferization.to_tensor %alloc restrict writable : memref<1024xf32>
    %7 = bufferization.alloc tensor() : tensor<f32>
    %inserted = tensor.insert %cst into %7[] : tensor<f32>
    %8 = linalg.generic {indexing maps = [#map, #map1], iterator types = ["reduction"]} ins(%6 : tensor<1024xf32>)
outs(%inserted : tensor<f32>) {
    ^bb0(%in: f32, %out: f32):
     %18 = arith.maximumf %in, %out : f32
     linalg.yield %18 : f32
    } -> tensor<f32>
    %extracted = tensor.extract %8[] : tensor<f32>
    %9 = bufferization.alloc tensor() : tensor<f32>
    %inserted 2 = tensor.insert %cst 0 into %9[] : tensor<f32>
    %10 = linalg.generic {indexing_maps = [#map, #map1], iterator_types = ["reduction"]} ins(%6 : tensor<1024xf32>)
outs(%inserted 2 : tensor<f32>) {
    ^bb0(%in: f32, %out: f32):
     %18 = arith.subf %in, %extracted : f32
      %19 = math.exp %18 : f32
      %20 = arith.addf %19, %out : f32
     linalg.yield %20 : f32
    } -> tensor<f32>
    %extracted 3 = tensor.extract %10[] : tensor<f32>
    %11 = tensor.empty() : tensor<1024xf32>
    %12 = linalg.generic {indexing_maps = [#map, #map], iterator_types = ["parallel"]} ins(%6 : tensor<1024xf32>) outs(%11 :
tensor<1024xf32>) {
    ^bb0(%in: f32, %out: f32):
      %18 = arith.subf %in, %extracted : f32
      %19 = math.exp %18 : f32
     %20 = arith.divf %19, %extracted_3 : f32
     linalg.yield %20 : f32
     -> tensor<1024xf32>
```

Tiling/Bufferization/...

```
%8 = scf.for %arg15 = %c0 to %c1024 step %c32 iter args(%arg16 = %alloc 4) -> (memref<f32>) {
   %subview 9 = memref.subview %alloc[%arg15] [32] [1] : memref<1024xf32> to memref<32xf32, strided<[1], offset: ?>>
   %16 = vector.transfer_read %subview_9[%c0], %cst_1 {in_bounds = [true]} : memref<32xf32, strided<[1], offset: ?>>, vector<32xf32>
   %17 = memref.load %arg16[] : memref<f32>
   %18 = vector.broadcast %7 : f32 to vector<32xf32>
   %19 = arith.subf %16, %18 fastmath<fast> : vector<32xf32>
   %20 = math.exp %19 fastmath<fast> : vector<32xf32>
   %21 = vector.reduction <add>, %20, %17 fastmath<fast> : vector<32xf32> into f32
   %22 = vector.insertelement %21, %cst[%c0 : index] : vector<1xf32>
   %23 = vector.extract %22[0] : f32 from vector<1xf32>
   %24 = vector.broadcast %23 : f32 to vector<f32>
   %25 = vector.extractelement %24[] : vector<f32>
   memref.store %25, %arg16[] : memref<f32>
    scf.yield %arg16 : memref<f32>
 %9 = memref.load %8[] : memref<f32>
 %alloc 5 = memref.alloc() {alignment = 64 : i64} : memref<1024xf32>
 %10 = scf.for %arg15 = %c0 to %c1024 step %c32 iter_args(%arg16 = %alloc_5) -> (memref<1024xf32>)
   %subview 9 = memref.subview %alloc[%arg15] [32] [1] : memref<1024xf32> to memref<32xf32, strided<[1], offset: ?>>
   %subview 10 = memref.subview %arg16[%arg15] [32] [1] : memref<1024xf32> to memref<32xf32, strided<[1], offset: ?>>
   %16 = vector.transfer read %subview 9[%c0], %cst 1 {in bounds = [true]} : memref<32xf32, strided<[1], offset: ?>>, vector<32xf32>
   %17 = vector.broadcast %7 : f32 to vector<32xf32>
   %18 = arith.subf %16, %17 fastmath<fast> : vector<32xf32>
   %19 = math.exp %18 fastmath<fast> : vector<32xf32>
   %20 = vector.broadcast %9 : f32 to vector<32xf32>
   %21 = arith.divf %19, %20 fastmath<fast> : vector<32xf32>
   vector.transfer write %21, %subview 10[%c0] {in bounds = [true]} : vector<32xf32>, memref<32xf32, strided<[1], offset: ?>>
   %subview 11 = memref.subview %arg16[%arg15] [32] [1] : memref<1024xf32> to memref<32xf32, strided<[1], offset: ?>>
   memref.copy %subview 10, %subview 11 : memref<32xf32, strided<[1], offset: ?>> to memref<32xf32, strided<[1], offset: ?>>
    scf.yield %arg16 : memref<1024xf32>
```

LLVM-IR

```
^bb11: // pred: ^bb10
%155 = llvm.getelementptr %40[%153] : (!llvm.ptr, i64) -> !llvm.ptr, f32
%156 = llvm.getelementptr %155[%29] : (!llvm.ptr, i64) -> !llvm.ptr, f32
%157 = llvm.load %156 {alignment = 4 : i64} : !llvm.ptr -> vector<32xf32>
%158 = llvm.mlir.undef : vector<32xf32>
%159 = llvm.insertelement %107, %158[%25 : i32] : vector<32xf32>
%160 = 11vm.shufflevector %159, %158
       %161 = llvm.fsub %157, %160 {fastmathFlags = #llvm.fastmath<fast>} : vector<32xf32>
%162 = llvm.intr.exp(%161) {fastmathFlags = #llvm.fastmath<fast>} : (vector<32xf32>) -> vector<32xf32>
%163 = llvm.mlir.undef : vector<32xf32>
%164 = llvm.insertelement %139, %163[%25 : i32] : vector<32xf32>
%165 = 11vm.shufflevector %164, %163
      %166 = llvm.fdiv %162, %165 {fastmathFlags = #llvm.fastmath<fast>} : vector<32xf32>
%167 = llvm.getelementptr %150[%153] : (!llvm.ptr, i64) -> !llvm.ptr, f32
%168 = llvm.getelementptr %167[%29] : (!llvm.ptr, i64) -> !llvm.ptr, f32
llvm.store %166, %168 {alignment = 4 : i64} : vector<32xf32>, !llvm.ptr
%169 = llvm.mul %12, %15 : i64
%170 = llvm.mlir.zero : !llvm.ptr
```

Example 2

$$y = \frac{x - E[x]}{\sqrt{(var(x) + \epsilon)}} * w + b$$

```
@triton.jit
def layer norm fwd fused(
    X, Y, W, B, Mean, Rstd, stride, N, eps, BLOCK SIZE: tl.constexpr):
    # Map the program id to the row of X and Y it should compute.
    row = tl.program id(0)
   Y += row * stride
   X += row * stride
   # Compute mean
    mean = 0
    mean = tl.zeros([BLOCK SIZE], dtype=tl.float32)
    for off in range(0, N, BLOCK SIZE):
        cols = off + tl.arange(0, BLOCK SIZE)
        a = tl.load(X + cols, mask=cols < N, other=0.).to(tl.float32)
        mean += a
    mean = tl.sum( mean, axis=0) / N
    # Compute variance
    var = tl.zeros([BLOCK SIZE], dtype=tl.float32)
    for off in range(0, N, BLOCK SIZE):
        cols = off + tl.arange(0, BLOCK SIZE)
        x = tl.load(X + cols, mask=cols < N, other=0.).to(tl.float32)</pre>
        x = tl.where(cols < N, x - mean, 0.)
        var += x * x
    var = tl.sum( var, axis=0) / N
    rstd = 1 / tl.sqrt(var + eps)
    # Write mean / rstd
    t1.store(Mean + row, mean)
```

Example 2

```
y = \frac{x - E[x]}{\sqrt{(var(x) + \epsilon)}} * w + b
```

```
// X - E[X]
%15 = linalg.generic {indexing maps = [#map, #map, #map], iterator_types = ["parallel"]}
                ins(%10, %14 : tensor<256xf32>, tensor<256xf32>) outs(%10 : tensor<256xf32>) {
 ^bb0(%in: f32, %in 19: f32, %out: f32):
  %33 = arith.subf %in, %in_19 : f32
  linalg.yield %33 : f32
} -> tensor<256xf32>
// Mask: x = tl.where(block < N COLS, x - mean, 0.)</pre>
%16 = linalg.generic {indexing maps = [#map, #map, #map], iterator types = ["parallel"]}
      ins(%7, %15, %1 : tensor<256xi1>, tensor<256xf32>, tensor<256xf32>) outs(%15 : tensor<256xf32>) {
^bb0(%in: i1, %in 19: f32, %in 20: f32, %out: f32):
  %33 = arith.select %in, %in 19, %in 20 : f32
  linalg.yield %33 : f32
} -> tensor<256xf32>
// (X-E[X])^2
%17 = linalg.generic {indexing maps = [#map, #map, #map], iterator_types = ["parallel"]}
                        ins(%16, %16 : tensor<256xf32>, tensor<256xf32>) outs(%16 : tensor<256xf32>) {
 ^bb0(%in: f32, %in 19: f32, %out: f32):
  %33 = arith.mulf %in, %in 19 : f32
  linalg.yield %33 : f32
} -> tensor<256xf32>
// E[X-E[X]]
%reduced 7 = linalg.reduce ins(%17 : tensor<256xf32>) outs(%inserted 6 : tensor<f32>) dimensions = [0]
   (%in: f32, %init: f32) {
    %33 = arith.addf %in, %init : f32
    linalg.yield %33 : f32
   } ..
```

Fuse, Vectorized core

$$y = \frac{x - E[x]}{\sqrt{(var(x) + \epsilon)}} * w + b$$

```
%alloc 20 = memref.alloc() {alignment = 64 : i64} : memref<256xf32>
  %12 = scf.for %arg14 = %c0 to %c256 step %c32 iter args(%arg15 = %alloc 20) -> (memref<256xf32>) {
    %subview 24 = memref.subview %alloc[%arg14] [32] [1] : memref<256xf32> to memref<32xf32, strided<[1], offset: ?>>
    %subview 25 = memref.subview %alloc 14[%arg14] [32] [1] : memref<256xf32> to memref<32xf32, strided<[1], offset: ?>>
    %subview 26 = memref.subview %alloc 17[%arg14] [32] [1] : memref<256xf32> to memref<32xf32, strided<[1], offset: ?>>
    %subview_27 = memref.subview %arg15[%arg14] [32] [1] : memref<256xf32> to memref<32xf32, strided<[1], offset: ?>>
    %13 = vector.transfer read %subview 24[%c0], %cst 3 {in bounds = [true]} : memref<32xf32, strided<[1], offset: ?>>, vector<32xf32>
    %14 = vector.transfer read %subview 25[%c0], %cst 3 {in bounds = [true]} : memref<32xf32, strided<[1], offset: ?>>, vector<32xf32>
    %15 = vector.transfer read %subview 26[%c0], %cst 3 {in bounds = [true]} : memref<32xf32, strided<[1], offset: ?>>, vector<32xf32>
    %16 = vector.broadcast %4 : f32 to vector<32xf32>
    %17 = arith.subf %13, %16 fastmath<fast> : vector<32xf32>
    %18 = vector.broadcast %arg14 : index to vector<32xindex>
    %19 = arith.addi %18, %cst 2 : vector<32xindex>
    %20 = arith.index cast %19 : vector<32xindex> to vector<32xi32>
    %21 = arith.cmpi slt, %20, %cst 1 : vector<32xi32>
    %22 = arith.select %21, %17, %cst 0 : vector<32xi1>, vector<32xf32>
    %23 = vector.broadcast %10 : f32 to vector<32xf32>
    %24 = arith.mulf %22, %23 fastmath<fast> : vector<32xf32>
    %25 = arith.mulf %24, %14 fastmath<fast> : vector<32xf32>
    %26 = arith.addf %25, %15 fastmath<fast> : vector<32xf32>
    vector.transfer write %26, %subview 27[%c0] {in bounds = [true]} : vector<32xf32>, memref<32xf32, strided<[1], offset: ?>>
    %subview 28 = memref.subview %arg15[%arg14] [32] [1] : memref<256xf32> to memref<32xf32, strided<[1], offset: ?>>
    memref.copy %subview 27, %subview 28: memref<32xf32, strided<[1], offset: ?>> to memref<32xf32, strided<[1], offset: ?>>
    scf.yield %arg15 : memref<256xf32>
```

Discussions

Triton – efficient GPU / CPU? Kernel writing

Triton-Linalg versus direct approach

Adapting Triton for Hexagon Target (multi-threading, vectorization, ..)

Other options...



Follow us on: in 💆 🗿 🕟 🚯









For more information, visit us at:

qualcomm.com & qualcomm.com/blog

Nothing in these materials is an offer to sell any of the components or devices referenced herein.

© Qualcomm Technologies, Inc. and/or its affiliated companies. All Rights Reserved.

Qualcomm and Hexagon are trademarks or registered trademarks of Qualcomm Incorporated. Other products and brand names may be trademarks or registered trademarks of their respective owners.

References in this presentation to "Qualcomm" may mean Qualcomm Incorporated, Qualcomm Technologies, Inc., and/or other subsidiaries or business units within the Qualcomm corporate structure, as applicable. Qualcomm Incorporated includes our licensing business, QTL, and the vast majority of our patent portfolio. Qualcomm Technologies, Inc., a subsidiary of Qualcomm Incorporated, operates, along with its subsidiaries, substantially all of our engineering, research and development functions, and substantially all of our products and services businesses, including our QCT semiconductor

Snapdragon and Qualcomm branded products are products of Qualcomm Technologies, Inc. and/or its subsidiaries. Qualcomm patented technologies are licensed by Qualcomm Incorporated.