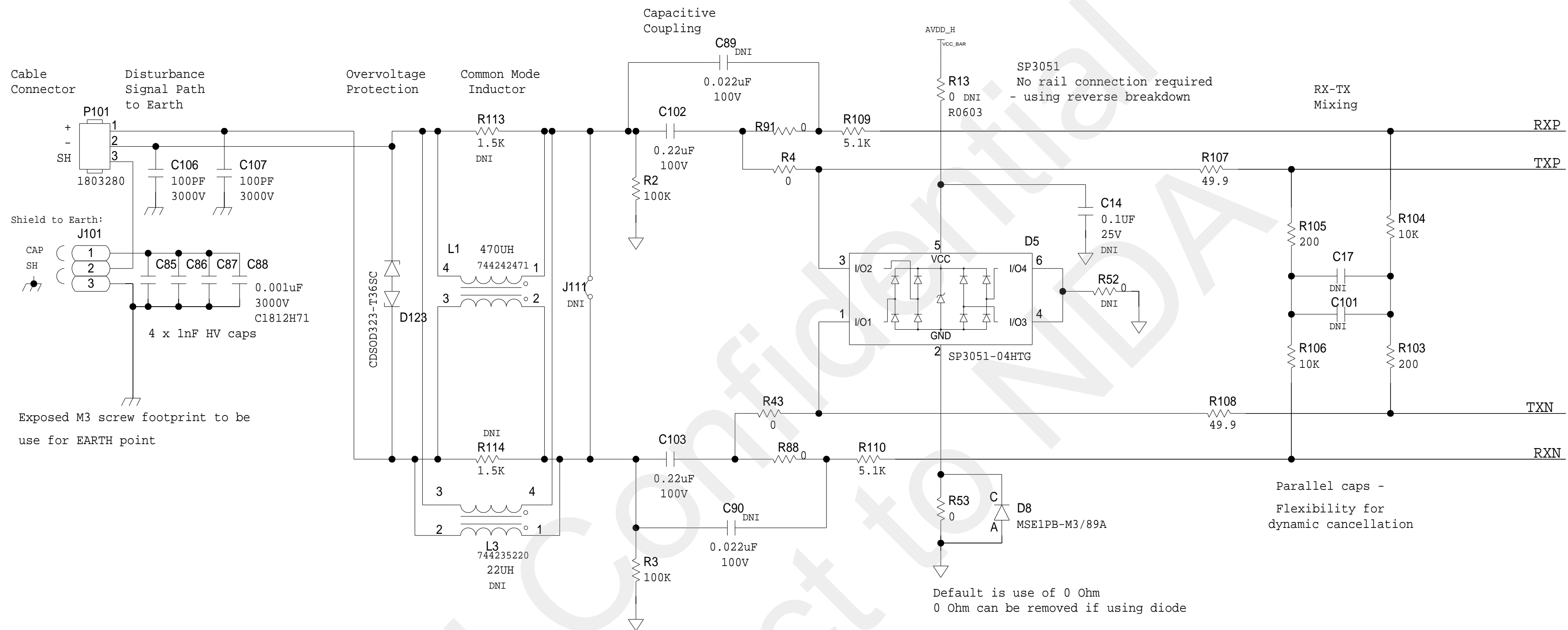
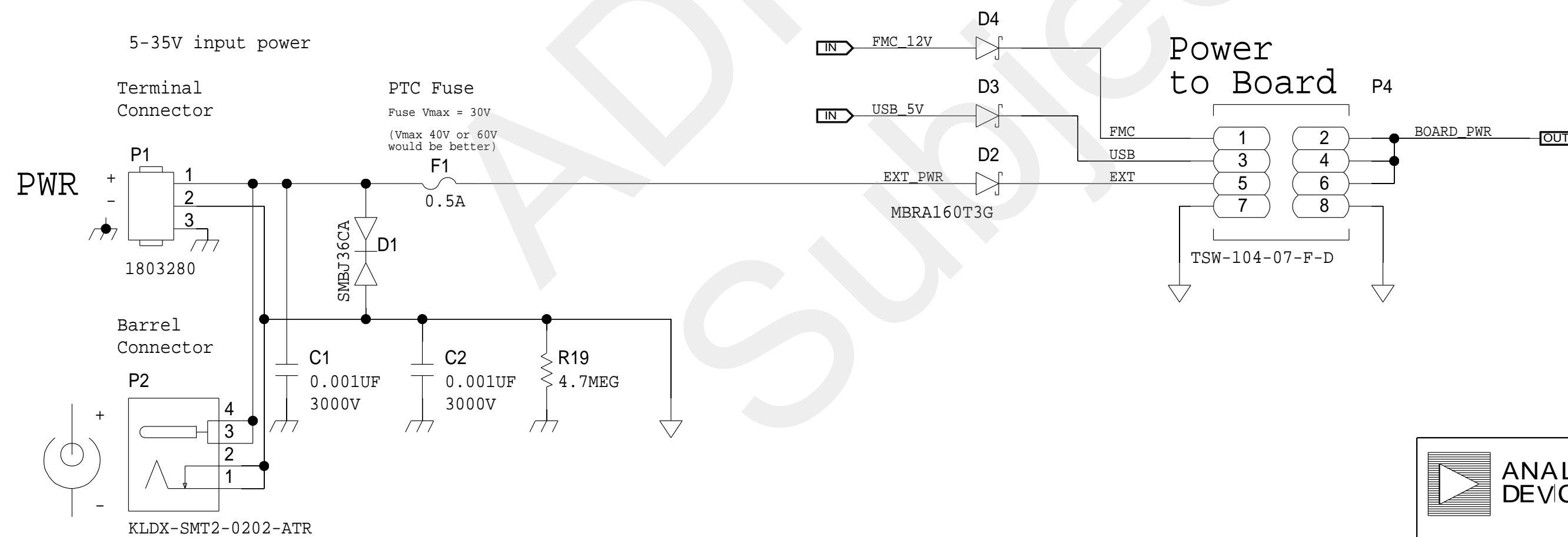


ADIN1100 CABLE CONNECTION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



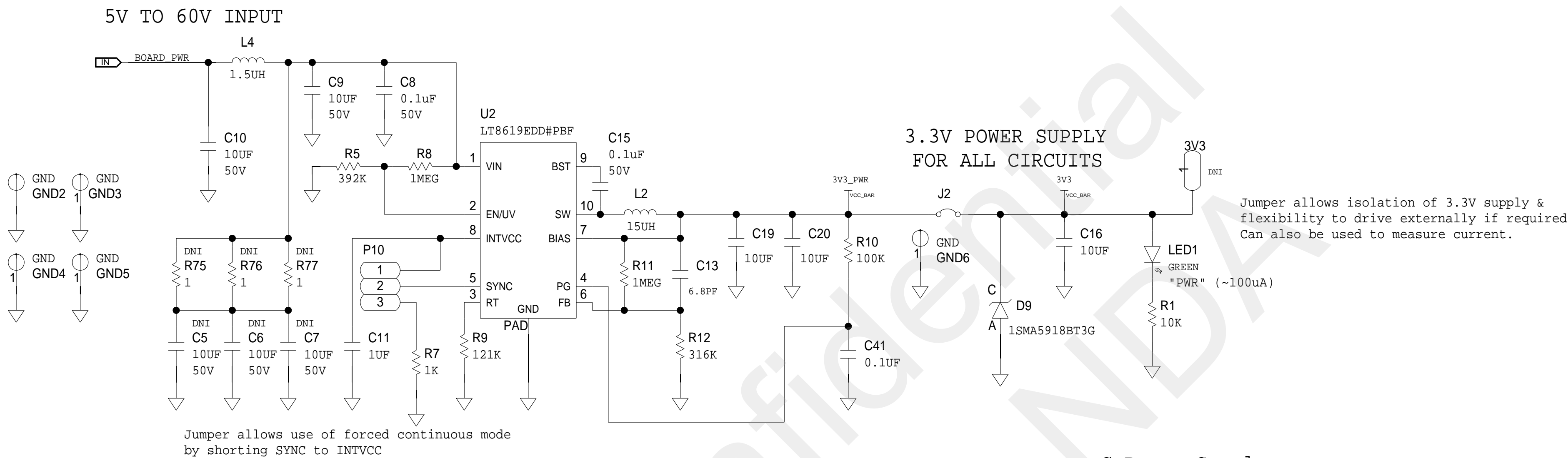
BOARD POWER



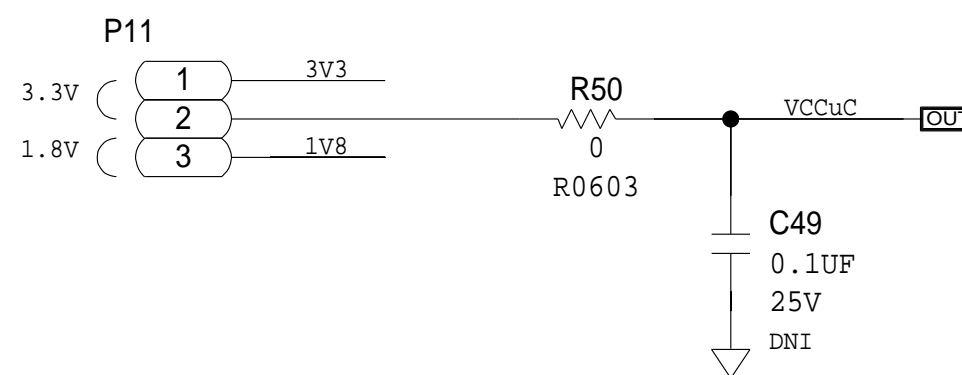
ANALOG DEVICES				SCHEMATIC			
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DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02-063798		REV B			
PTD ENGINEER TRACEY JOHNSON		SIZE C	SCALE 1:1	SHEET 2	OF 7		

BOARD POWER SUPPLY

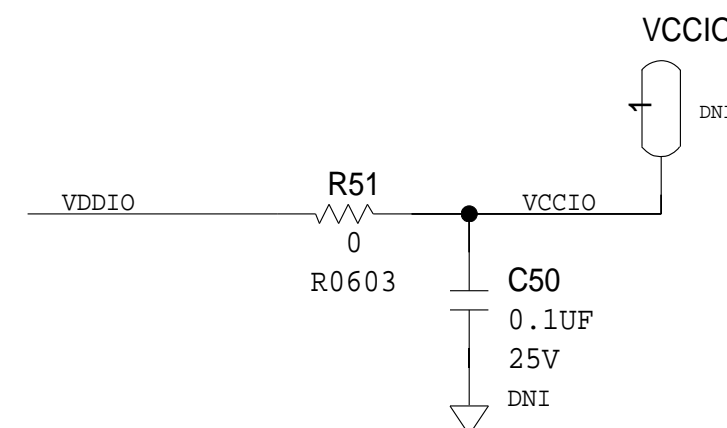
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



uC Power Supply



FMC I/O Supply connected to PHY VDDIO



0 Ohm resistors can be replaced with ferrite bead if needed

SCHEMATIC			
HW TYPE : Customer Evaluation			
Product: ADIN1100			
EVAL-ADIN1100FMCZ			
DESIGN VIEW	DRAWING NO.		REV
<DESIGN_VIEW>	02-063798		B
PTD ENGINEER TRACEY JOHNSON	SIZE C	SCALE 1:1	SHEET 3 OF 7

ADIN1100

Pin	Function
1	TXD_2
2	TXD_3/MEDIA_CNV
3	LED
4	LINK_ST/PHYAD_2
5	RESET_N
6	GND
7	CLK25_REF
8	XTAL_I/CLK_IN
9	XTAL_O
10	NC
11	TXN
12	RXN
13	RXP
14	TXP
15	AVDD_H
16	AVDD_L
17	CEXT_1
18	CEXT_2
19	CEXT_3
20	NC
21	CEXT_4
22	DLDO_1P1
23	DVDD_1P1
24	INT_N
25	MDIO
26	MDC
27	RXD_3/PHYAD_1
28	RXD_2/PHYAD_0
29	RXD_1/MS_SEL
30	BI
31	RXD_0/TX2P4_ENB
32	RX_CLK/MACIF_SELO
33	RX_DV/SWPD_ENB
34	RX_ER/MACIF_SEL1
35	TX_ER
36	TX_EN
37	TX_CLK
38	TXD_0
39	TXD_1
40	PAD

ADIN1100 SUPPLY PIN SELECTION & DECOUPLING

0 Ohm resistors can be replaced with ferrite bead if needed

Label supply jumper options clearly

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
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CLOCK

Cap divider if RMII_REF_CLK signal > 2.5Vp-p
Choose C4, such that:
 $C4 = [2.5(13pF + C_{pcb})] / [V_{p-p} - 2.5]$
If signal < 2.5Vp-p, remove C3 and C4 = 1nF
Same applies to C18 & C55 for EXT_CLK signal

External Clock option (or from FMC)

CRYSTAL TO BE PLACED AS CLOSE TO ADIN1100 AS POSSIBLE

Y3 i/p & o/p cap values need to be chosen in conjunction with the PCB capacitance.
Cap value = $(2 \times \text{Xtal Load}) - C_{pcb} - 3pF$
Xtal Load = 10pF, Assume $C_{pcb} = 1.5pF$
Cap value = $(2 \times 10pF) - 1.5pF - 3pF = 15.5pF$

H/W PIN CONFIG

Depending on internal weak pull-downs for low setting
High setting is achieved by closing switch to connect to 10k pull-up to VDDIO.

SCHEMATIC

HW TYPE : Customer Evaluation Product: ADIN1100 EVAL-ADIN1100FMCZ			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-063798		REV B
PTD ENGINEER TRACEY JOHNSON	SIZE C	SCALE 1:1	SHEET 4 OF 7

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CLOCK

R73 DNI

0

C3 10pF

C4 68pF

RMIREF_CLK

IN

Cap divider if RMIREF_CLK signal > 2.5Vp-p
 Choose C4, such that:
 $C4 = [2.5(13pF + C_{pcb})] / [V_{p-p} - 2.5]$
 If signal < 2.5Vp-p, remove C3 and C4 = 1nF
 Same applies to C18 & C55 for EXT_CLK signal

R86 DNI

0

C55 1000pF

EXT_CLK

1

J1 DNI

5 4 3 2

5-1814832-2

External Clock option
 (or from FMC)

C18 10pF

R72

0

XTAL 0

R87 0

Y3 25.000MEGHZ

IN/OUT

IN/OUT

GND

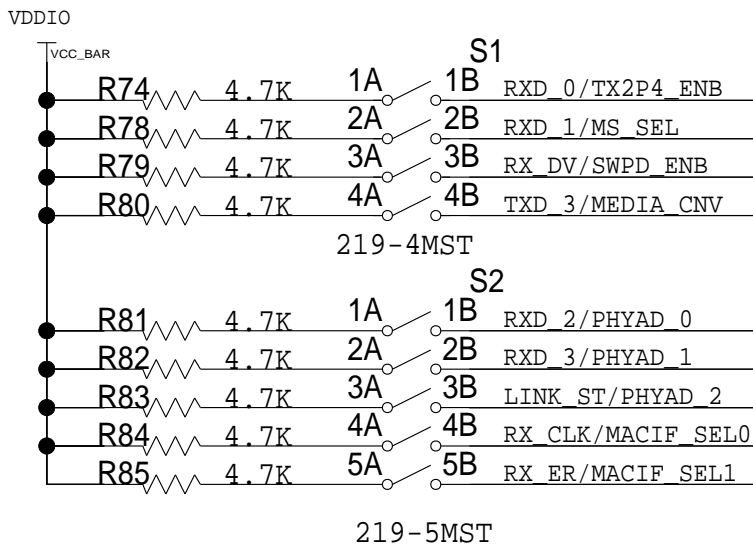
2 4

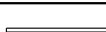
C84 15pF

AL TO BE PLACED AS CLOSE TO ADIN1100 AS POSSIBLE

p & o/p cap values need to be chosen in conjunction
 the PCB capacitance.
 $value = (2 \times Xtal\ Cload) - C_{pcb} - 3pF$
 $Cload = 10pF$, Assume $C_{pcb} = 1.5pF$
 $value = (2 \times 10pF) - 1.5pF - 3pF = 15.5pF$

Depending on internal weak pull-downs for low setting
high setting is achieved by closing switch to connect
to 10k pull-up to VDDIO.

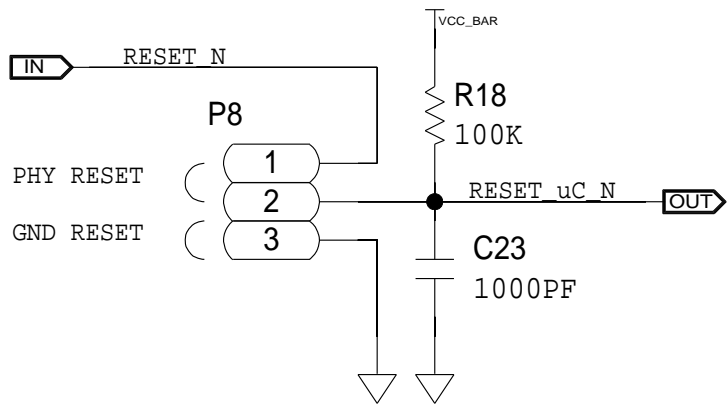


 <div> <p>ANALOG DEVICES</p> <p>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES.</p> <p>THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.</p> </div>	<h1>SCHEMATIC</h1>				
	<p>HW TYPE : Customer Evaluation</p> <p>Product: ADIN1100</p> <p>EVAL-ADIN1100FMCZ</p>				
	<p>DESIGN VIEW</p> <p><DESIGN_VIEW></p>		<p>DRAWING NO.</p> <p>02-063798</p>		<p>REV</p> <p>B</p>
	<p>PTD ENGINEER TRACEY JOHNSON</p>		<p>SIZE</p> <p>C</p>	<p>SCALE</p> <p>1:1</p>	<p>SHEET 4 OF 7</p>

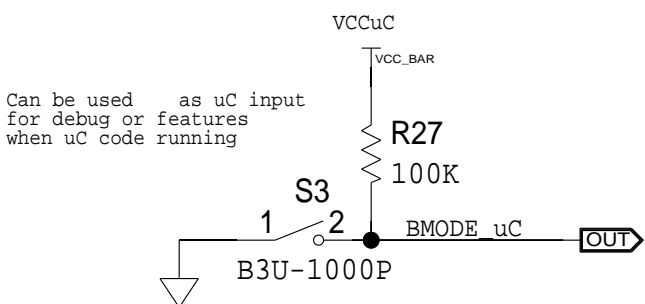
Cortex M4 uC

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

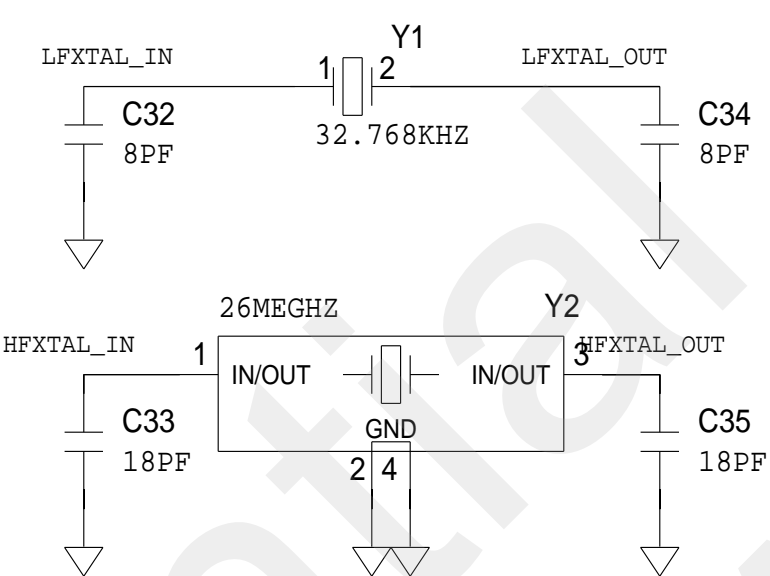
uC RESET



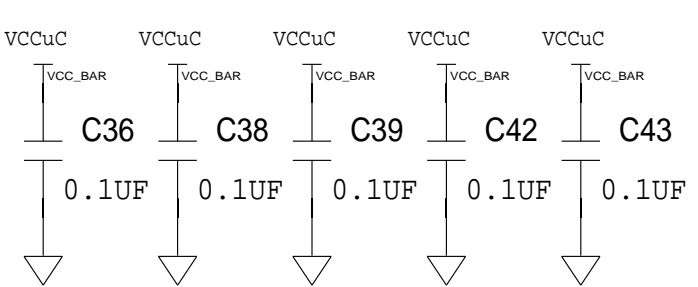
uC (UART) Bootload



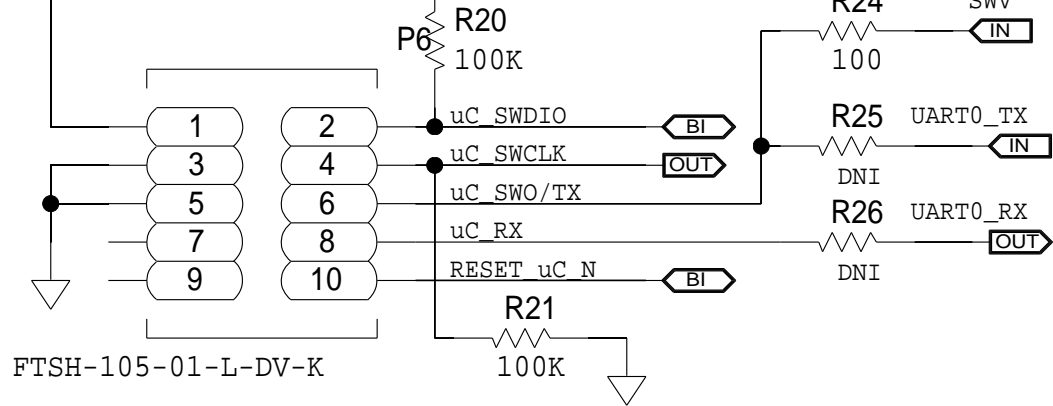
uC Clocks



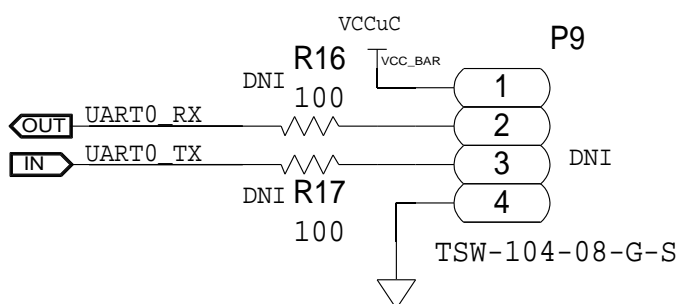
uC Decoupling Caps



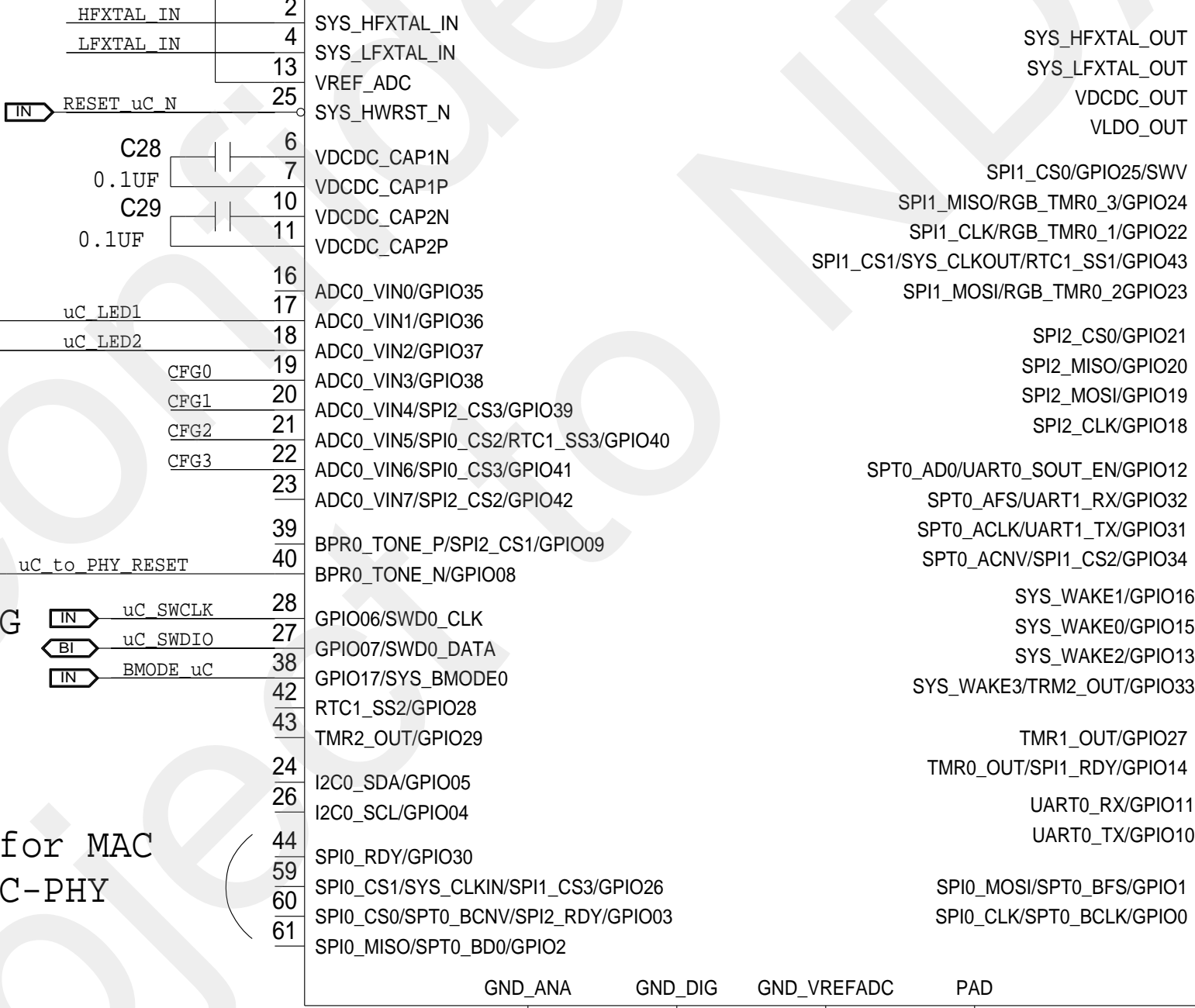
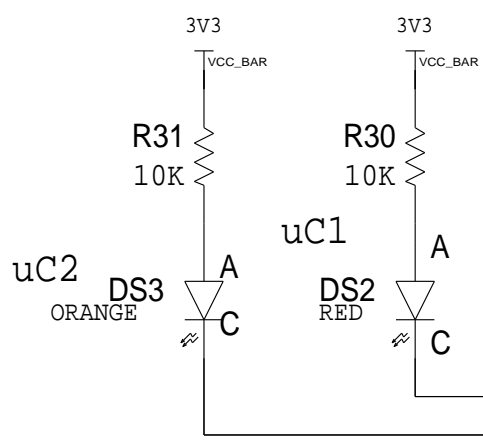
uC JTAG



ADI DEBUG

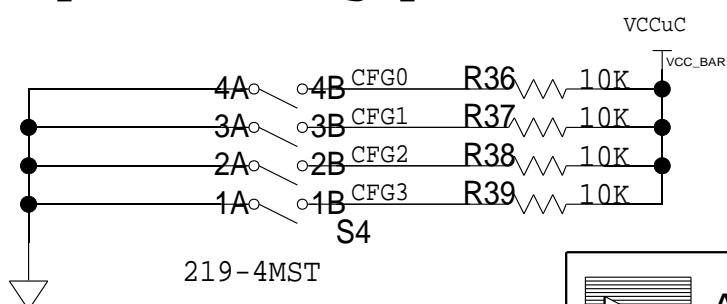


LEDs

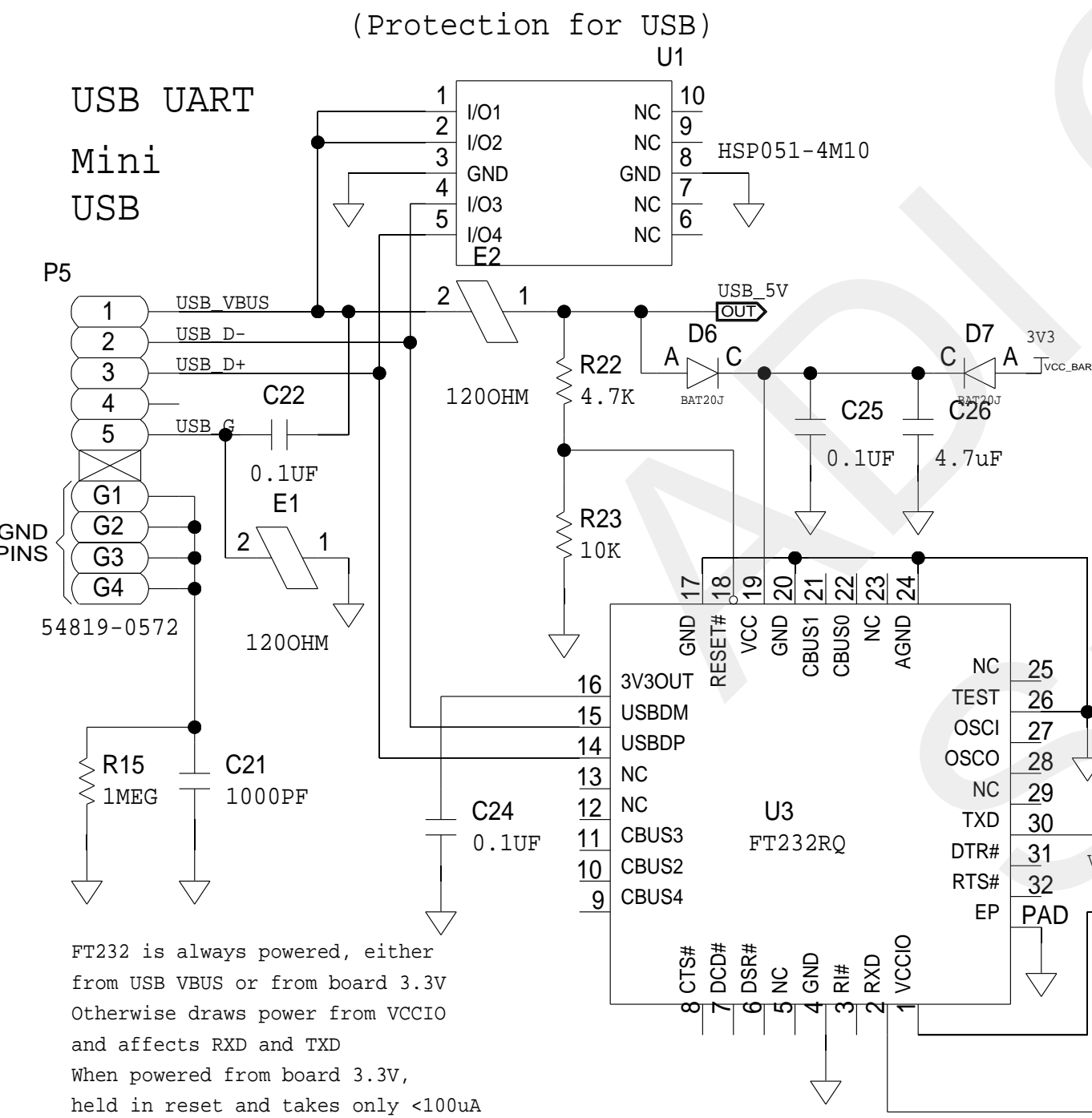


SPI0 for MAC on MAC-PHY board

Spare Config pins



USB UART Mini USB



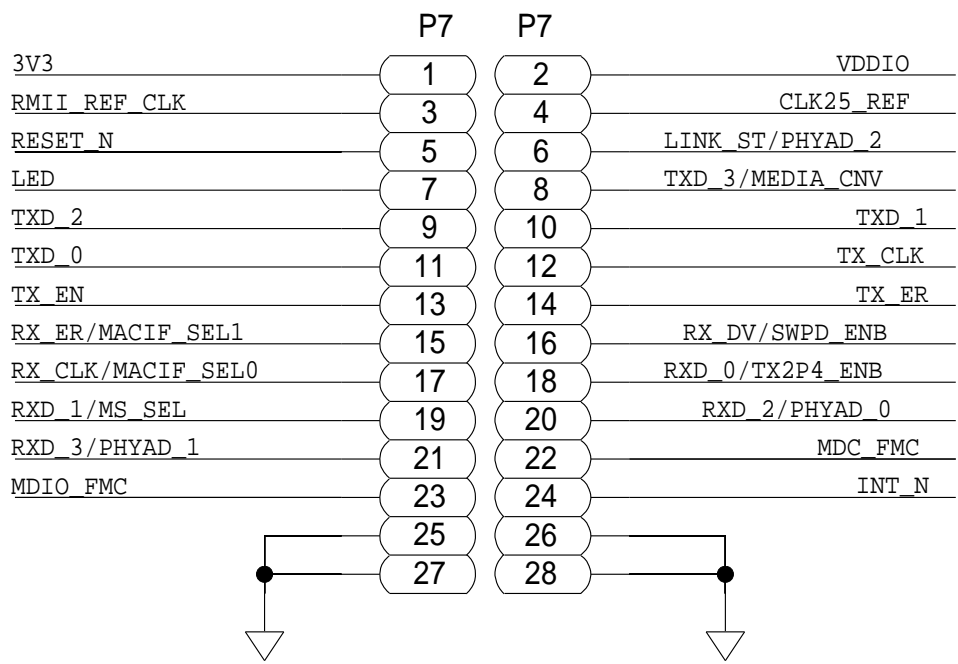
FT232 is always powered, either from USB VBUS or from board 3.3V. Otherwise draws power from VCCIO and affects RXD and TXD. When powered from board 3.3V, held in reset and takes only <100uA.

SCHEMATIC

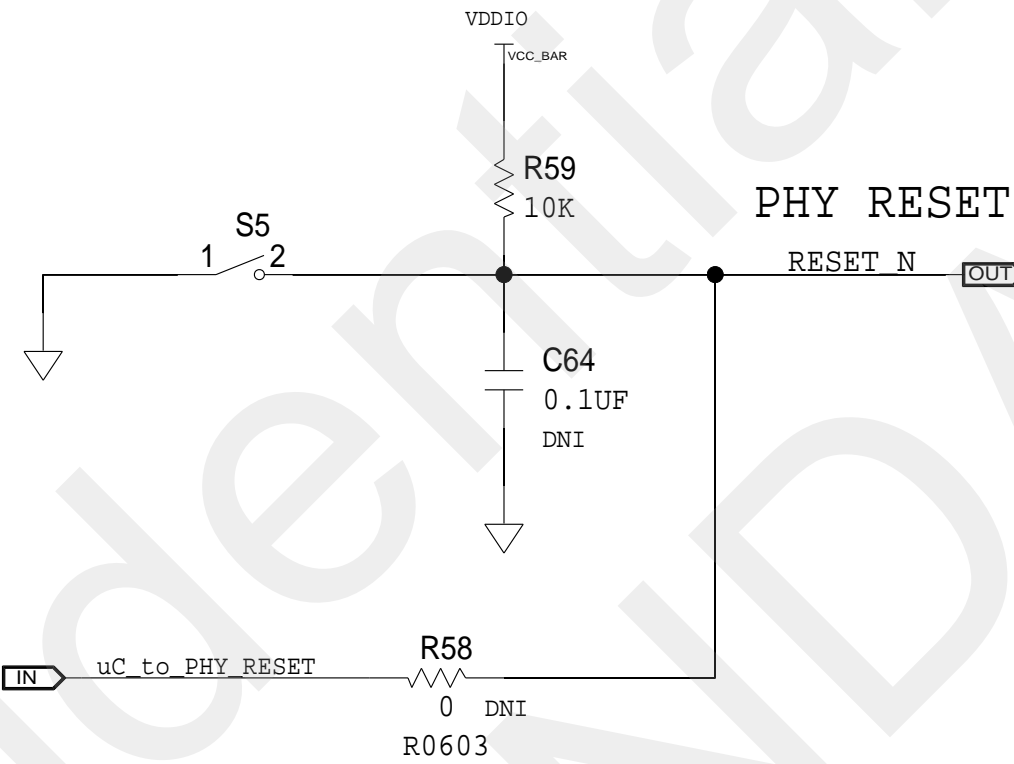
HW TYPE : Customer Evaluation			
Product: ADIN1100			
EVAL-ADIN1100FMCZ			
DESIGN VIEW	DRAWING NO.		REV
<DESIGN_VIEW>	02-063798		B
PTD ENGINEER TRACEY JOHNSON	SIZE C	SCALE 1:1	SHEET 5 OF 7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

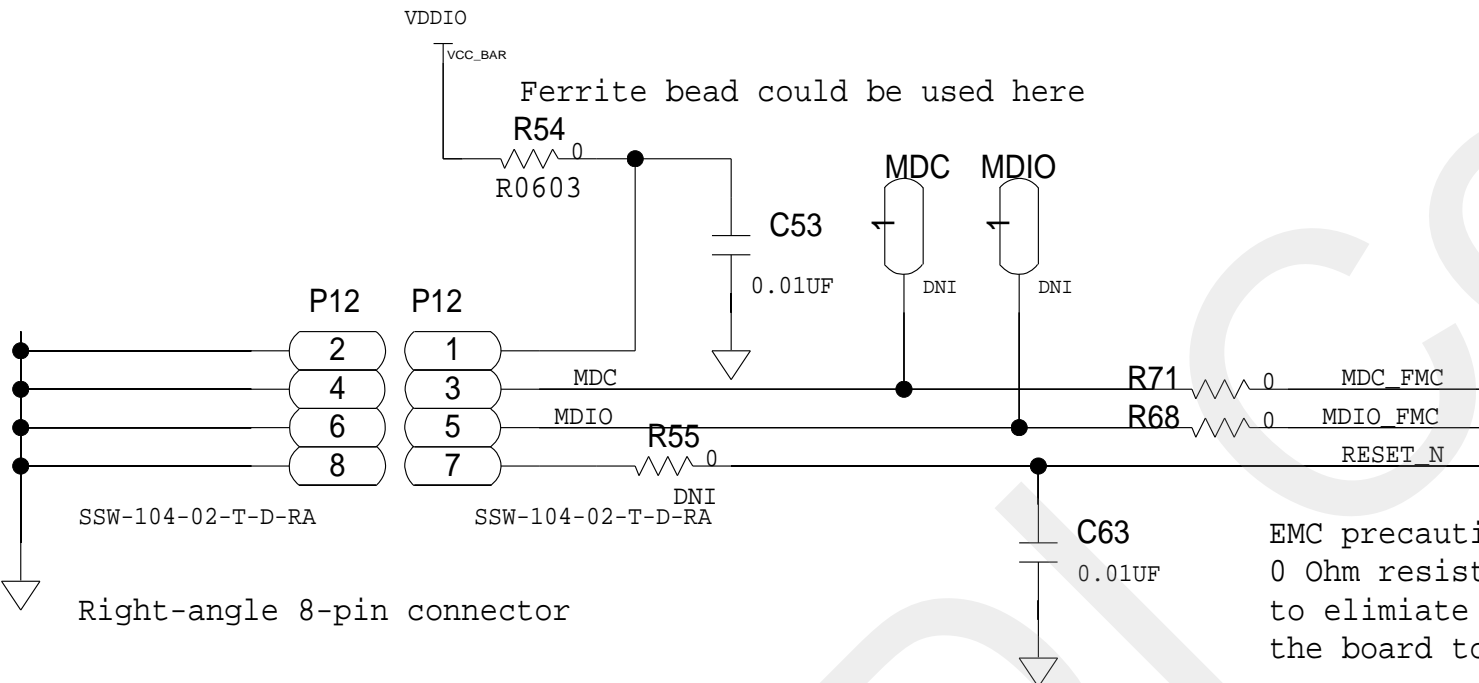
MII HEADER



BOARD RESET

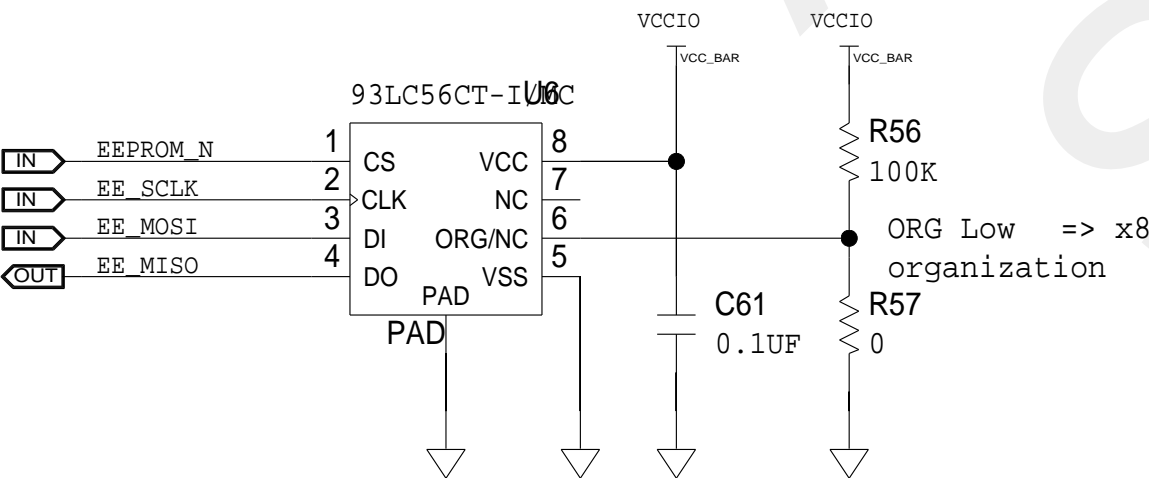


MDIO 8-PIN CONNECTOR



BOARD EEPROM

EEPROM to identify the board type & revision & unique ID



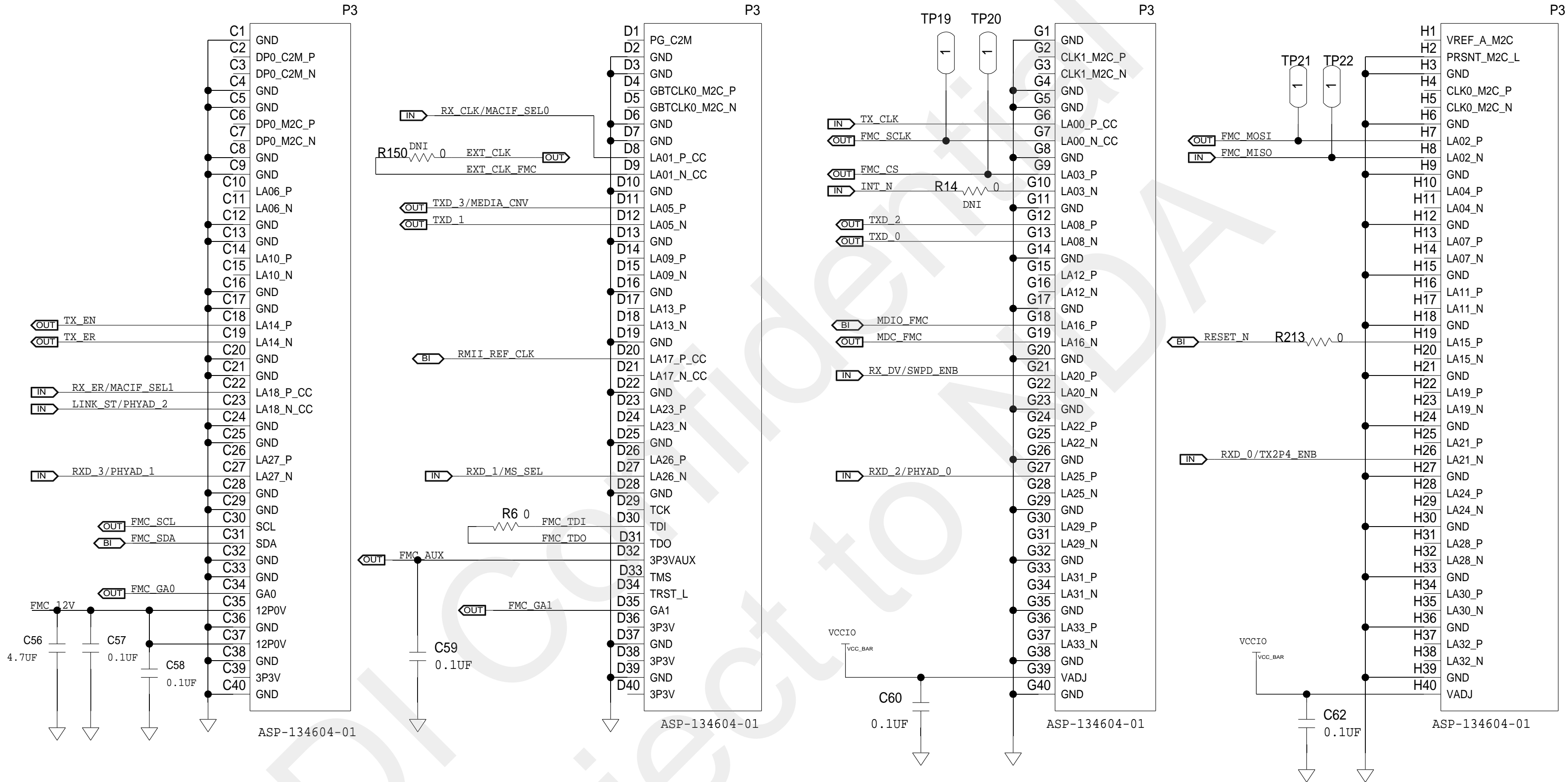
SCHEMATIC			
HW TYPE : Customer Evaluation			
Product: ADIN1100			
EVAL-ADIN1100FMCZ			
DESIGN VIEW	DRAWING NO.		REV
<DESIGN_VIEW>	02-063798		B
PTD ENGINEER TRACEY JOHNSON	SIZE C	SCALE 1:1	SHEET 6 OF 7

FMC CONNECTOR

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

Spare SPI interface connected to testpoints



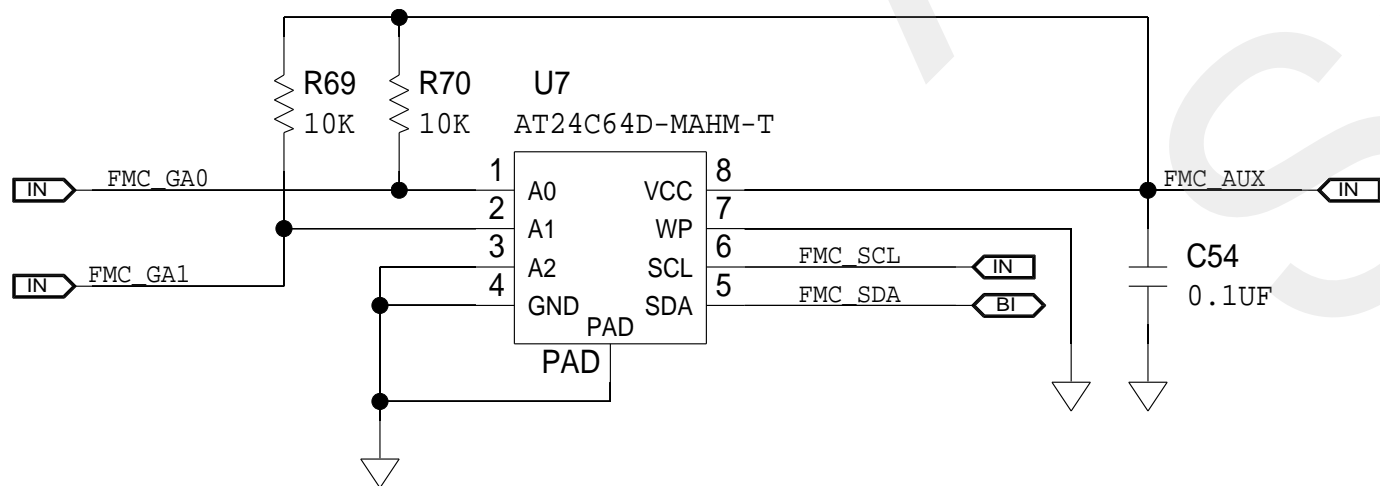
ASP-134604-01

ASP-134604-01

ASP-134604-01

ASP-134604-01

FMC EEPROM
EEPROM required in VITAS57.1 Standard



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SCHEMATIC

HW TYPE : Customer Evaluation
Product: ADIN1100
EVAL-ADIN1100FMCZ

DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-063798	REV B
PTD ENGINEER TRACEY JOHNSON	SIZE C	SCALE 1:1
SHEET 7 OF 7		