Evaluation Board User Guide
UG-ADIN1300

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Evaluation Board for the ADIN1300 Robust, Industrial Low Latency Gigabit Ethernet PHY

FEATURES

Single external 5V supply
FMC connector for MII interface, MDIO & Status signals
Accessible surface-mount configuration resistors & dial switches

EVALUATION KIT CONTENTS

EV-ADIN1300FMCZ evaluation board
MDIO Interface Dongle

ADDITIONAL EQUIPMENT NEEDED

Power supply to connect to EXT_5V connector or +5V barrel adaptor to connect to P4.
Ethernet cable
USB cable
PC running Windows 7 upward
ADIN1300 Datasheet

GENERAL DESCRIPTION

This user guide describes the evaluation board (EV-ADIN1300FMCZ), designed to allow the user to easily evaluate the key features of the ADIN1300 Industrial Gigabit Ethernet PHY. The board is powered from an external single 5V supply rail, which can be supplied either via P4 plug or EXT_5V terminal block. For additional flexibility, the board can be supplied direct from the FMC connector (node name "12V_FPGA") or from an external 12V source via "EXT_12V" terminal block. f the 12 V rail option is used, it is regulated down to +5 V on board by an ADP7105-5.

All chip supplies are regulated from the +5 V rail providing nominally:

- VDDIO = 2.5 V (configurable as 1.8 V/2.5 V/3.3 V)
- AVDD3P3 = 3.3 V
- VDD0P9 = 0.9V
- DVDD= 3.3 V (non-chip supply)

An FMC connector (P3) is provided for ease of connection to a master FPGA system, while connector P5 provides an alternative means for MDIO control. The board is also fitted with a 25MHz crystal (Y1). Complete specifications for the ADIN1300 product itself can be found in the ADIN1300 datasheet, which should be consulted in conjunction with this user guide when using the evaluation board.

EVALUATION BOARD

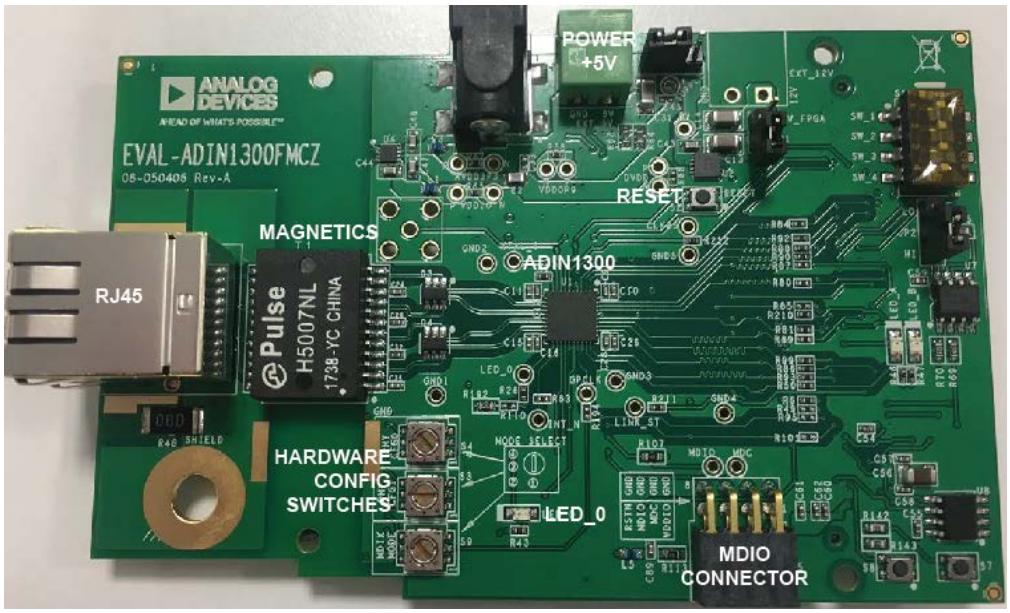

Figure 1. Overview of ADIN1300 Evaluation board

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REVISION HISTORY

6/20—Revision PrE: Added Continuous Frame Generator mode. Added ability to load scripts.

5/27—Revision PrD: Added Read/Write Field to GUI. ADIN1300 hardware schematic updated to REV B.

3/19—Revision PrC: Updated to add Frame Generator/Checker and Cable diagnostic Tab.

2/19—Revision PrB: Updated to add Test Modes, Loopback, Clock Pin control tabs.

12/18—Revision PrA: Initial Version

GETTING STARTED

QUICK START STEPS

To set up the EV-ADIN1300FMCZ and use with the Analog Devices GUI, take the following steps:

1. Connect +5V power to the ADIN1300 board via the EXT_5V or the barrel connector
2. Connect USB cable to the MDIO interface dongle. Connect USB cable to PC. When connecting the MDIO interface dongle to PC for the first time, drivers will automatically be installed. Wait until the driver install is complete before proceeding to the next step.
3. Connect the MDIO interface dongle to the ADIN1300 board, ensuring the ADuCM3029 Microcontroller faces up, see Figure 1. The MDIO interface dongle is not keyed.
4. Launch the ADIN1300 software from the Analog Devices folder in the start menu.
5. Connect Ethernet cable to the RJ-45 connector and to another PHY device.

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The ADIN1300 board operates from a single external supply rail. It can be powered from either +5 V or +12 V as follows. When supplying the board with +5 V, user has option to apply +5 V via P4 or to the connector EXT_5V, with JP3 configured for 5V/'A'.

Alternatively, the board can be powered from an FMC-supplied +12V supply in which case JP1 should be removed and JP3 set to position 12V/'B'. A final option is to use an external +12 V applied to the EXT_12V connector and JP3 configured for 12V/'B', in this case the on-board ADP7105 generates the required +5 V power for the board. Figure 2 shows an overview of the power supply configuration on the board.

From the +5 V "SUPPLY", the rest of the board power requirements are generated. Two ADP223 devices generate the various power rails, AVDD3P3, VDDIO, VDD0P9 and DVDD, the default nominal voltages are listed in Table 1.

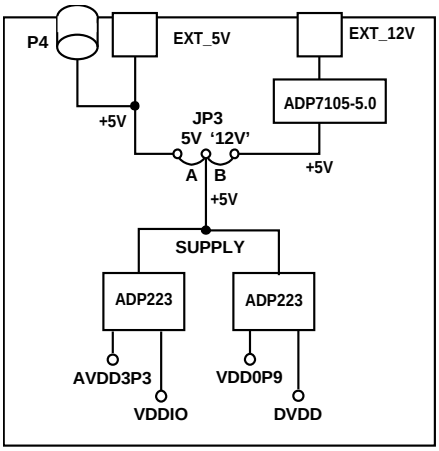

Figure 2. Overview of Power Supplies

The VDDIO voltage rail defaults to 2.5 V with the installed components, it may be adjusted if other VDDIO voltages are required by changing the value of R12 accordingly as detailed in Table 1.

Table 1. Default Power Supply Configuration

Supply Rail	Nominal Voltage	Adjustment
AVDD3P3	3.3V	N/A
VDDIO	2.5V	1.8 V with R16 = 130kΩ 2.5 V with R16= 200kΩ 3.3 V with R16 = 280kΩ
VDD0P9	0.9V	N/A
DVDD	3.3V	N/A

Table 2 gives an overview of the board current for various operating modes.

Table 2. Board Quiescent Current (EXT_5V = +5 V)

Board Status	Typical Quiescent Current
On power-up	30 mA initially 6.5 mA in EDPD
While in Hardware Power Down (RESET_N held low)	6.5 mA
10BASE-TX	50 mA
100BASE-TX	60 mA
1000BASE-T	145 mA

POWER SEQUENCING

There are no power sequencing requirements with the ADIN1300 device. The board is powered from one voltage rail applied to the board, 5V or 12V as described above.

When using the ADIN1300 evaluation board with the MDIO interface dongle, there is currently a known sequence requirement for the MDIO interface dongle, this may be resolved later via software. Ideally the MDIO interface dongle should be powered from the USB cable prior to connection to ADIN1300 board. Alternatively if issues are observed simply restart the GUI to resolve any board connection issues.

BOARD USAGE OPTIONS

The board can be can be used in 2 general modes. In standalone mode, the board can be used to evaluate the ADIN1300 in IEEE 802.3 test modes, establish links with a link partner and evaluate the performance of the chip. In this mode the board should be powered with 5 V at the EXT_5V connector.

The second mode is to plug the board into an FPGA development board which provides an FMC LPC connector. In this mode, the MII interfaces, clocks and LEDs can be connected to an FPGA where the MAC and upper layers can be implemented for evaluation of the ADIN1300 in a full system. In this case, an external 12 V supply at the EXT+12V connector is preferable, but the FPGA option can also be used.

JUMPER OPTIONS

A minimal number of jumpers on the evaluation board must be set for the required operating setup before using the board. The functions of these jumper options are described in Table 4. The default setup is highlighted in Table 3.

Table 3. Default Link Options

Link No.	Position	Function
JP1	Not inserted	Default connection is to EXT_5V
JP2	B ("HI")	This link selects high or low for the WP of U7.
JP3	A ("5V")	This link connects EXT_5V to the regulators.

Table 4. Jumper Functions

Jumper No.	Function
JP1	This jumper sets the 12 V supply source for the ADP7105 which provides a +5 V rail for other on-board circuit needs. The ADP7105 is powered from a 12 V rail which can originate from the 12V_FPGA supply rail if an FPGA is connected to the FMC connector, JP1 can be left open in this case. Alternatively an external +12 V rail can be applied to the EXT_12V connector and used to power the ADP7105, in this case, insert JP1.
JP2	JP2 sets the write mode of the AT24C02D-SSHM-T EEPROM (U7). Position A ("LO") — Enable writing to the EEPROM. Position B ("HI") — Write protect the EEPROM (default).
JP3	This sets the 5 V supply source "SUPPLY". Position A ("5V") — P2 or EXT_5V are the supply source (default). Position B ("12V") — FPGA via the FMC connector or EXT_12V is 12 V supply source.

CLOCK OPTIONS

The evaluation board provides options to supply the ADIN1300 clock requirements from an on-board crystal oscillator or alternatively from an external clock applied to J1.

There are a number of crystal oscillators on the ADIN1300 evaluation board and MDIO interface dongle

- Y1 is a 25 MHz crystal connected across the ADIN1300 XTAL_I/XTAL_O pins.
- Y2 is a 32.678 kHz crystal used on the MDIO board for the ADuCM3029
- Y3 is a 26 MHz crystal used on the MDIO board for the ADuCM3029

R120 must be populated and R15 removed if the signal applied to J1 is to be used by the ADIN1300. See Component Recommendations section in the Datasheet for more information.

The ADIN1300 can also be configured to provide a 25MHz clock output on the CLK25_REF pin which is available on the FMC connector. The source of this clock is the on-board XTAL (Y1). Note that when a pin reset is applied to the ADIN1300 the clock disappears for the duration of the reset and needs to be re-enabled via software following the reset. This clock can be used to synchronously clock the FPGA logic. If a reset for ADIN1300 is required without CLK25_REF stopping, then a software reset should be used instead. Alternatively, GP_CLK is also available on the FMC connector and this pin can be configured to output several different clocks from the ADIN1300. See the ADIN1300 datasheet for more detailed information.

ON BOARD EEPROM AND LEDS

Also found on the evaluation board are two FPGA controllable LEDs, 4 DIP switches, and 2 un-programmed I2C EEPROMS.

The AT24C02D-SSHM-T (U7) can be programmed with voltage settings so that the FPGA provides the correct voltages on its supply rails. The write address of the EEPROM is 0b[10100 [GA1] [GA0] 0] and the read address is 0b[10100 [GA1] [GA0] 1]. CAT24C32WI-GT3 (U8) can be used for storing configuration information for networking applications. The write address of the EEPROM is 0xA0 and the read address is 0xA1

ADIN1300 LED PIN

There is one LED pin on the ADIN1300. The LED pin can be configured in various operating modes using the MDIO interface dongle –full details are available in the Register map of the ADIN1300 Datasheet. By default LED_0 is on when a link is established and it blinks when there is activity.

The LED_0 pin is also shared with the PHY_CFG0 Pin Configuration function and it may therefore be necessary that the voltage level on the pin be at a certain value on power on and reset in order to configure the ADIN1300 as required. See STATUS LED section of ADIN1300 datasheet for further details.

REV A Evaluation Board

The Rev A ADIN1300 evaluation board has LED0 configured for Mode 3 & 4 by default, with R191 and R192 resistors populated. If user wishes for PHY_CFG0 to be used in Mode 1 or 2, remove R191 and R192 and insert R110.

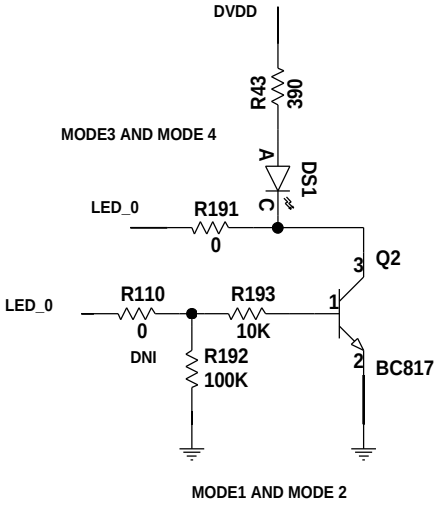

Figure 3. REV A Hardware LED0 Configuration

REV B Evaluation Board

The Rev B ADIN1300 evaluation board has a rotary switch to allow easy configuration for all modes. The LED0 is driven from AVDD3P3.

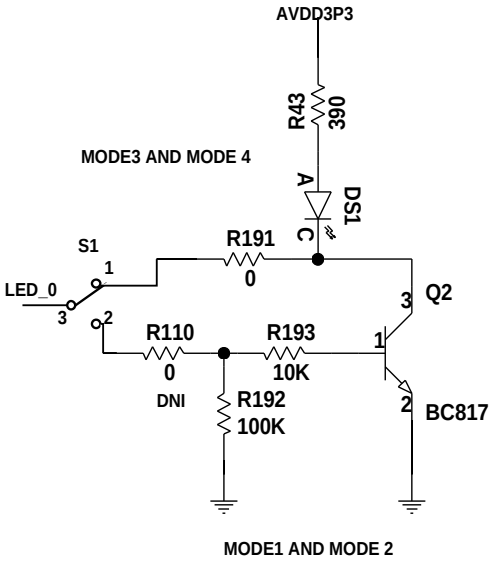

Figure 4. REV B Hardware LED0 Configuration

MAC INTERFACE

The MDIO interface dongle can be accessed directly through the P5 connector for users wishing to connect their own MAC interface with the PHY.

Alternatively, included in the evaluation kit is an MDIO interface dongle for interfacing with the ADIN1300 evaluation board via the ADI evaluation GUI running on the PC.

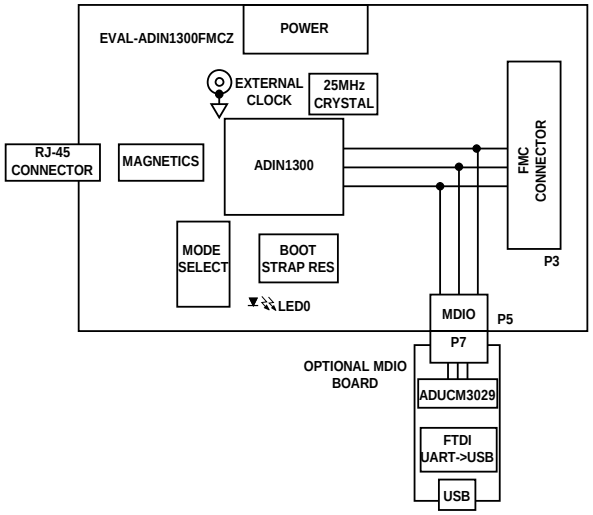

Figure 5. Simplified overview of ADIN1300 board with MDIO board connected

MDIO INTERFACE DONGLE

This board contains an ADuCM3029 microcontroller and FT232 UART to USB interface. The schematic is shown in Figure 9.

If using the MDIO interface dongle, ensure to first connect the USB cable to the board, then connect the board to the ADIN1300 board with the ADuCM3029 facing up.

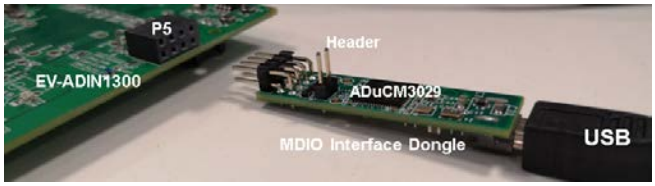

Figure 6. Connection of MDIO Interface Dongle to ADIN1300 hardware

There are two LEDs on this board, DS7 and DS8. When the powered USB cable is initially connected to the MDIO interface dongle, the diode DS8 will light. When the GUI establishes communication with the board, both DS7 and DS8 will flash and continue to flash while the GUI is active and the board is selected as the local board within the GUI.

The MDIO interface dongle has two push-buttons on the underside of the board, S5 and S6 as shown in Figure 1.

- S5 is for Download/Reboot purposes
- S6 is to reset the ADuCM3029.

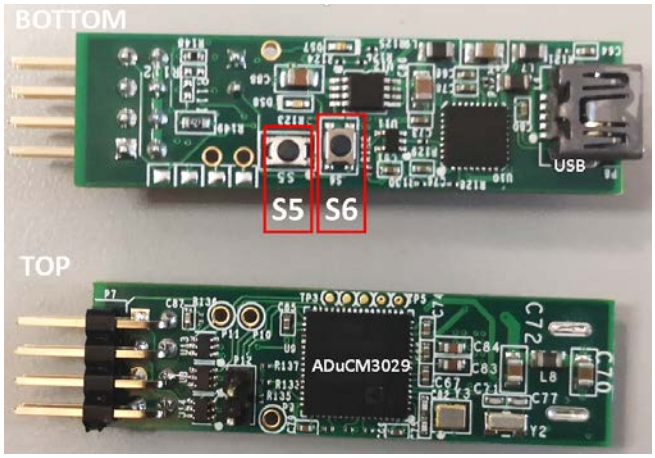

Figure 7. Overview of MDIO Interface Dongle

CONFIGURATION PINS SETUP

The board is configured as detailed in Table 5. ADIN1300 configuration settings can be changed by manipulating the resistors listed in the right-hand column. The "Configuration Pins" section of the ADIN1300 datasheet details all available options. Figure 4 highlights the location of the resistors on the underside of the PCB. The speed configuration is configured via 2 rotary switches S3 and S4, the MDIX mode is controlled using S9. Table 5 highlights the different configurations available.

Table 5. Configuration Settings

Configuration Option	Relevant Pins	Resistor Settings
PHY Address = 0b00000	RXD_3/PHYAD_3 RXD_2/PHYAD_2 RXD_1/PHYAD_1 RXD_0/PHYAD_0	R22, R29, R31, R37 = DNI R23, R30, R32, R38 = DNI Using internal pull-down resistors.
MDIX configuration = Auto MDIX	GP_CLK/RX_ER/MDIX_MODE	**S9 position Mode** 1 Mode 1, Manual MDI 2 Mode 2, Manual MDIX 3 Mode 3, Auto MDIX – Prefer MDIX 4 Mode 4, Auto MDIX – Prefer MDI (default)
PHY Configuration - Downspeed, EDPD, EEE, Software powerdown, Forced speed	LINK_ST/PHY_CFG1 LED_0/COUT/TX_ER/PHY_CFG0	Controlled by Switches S3 and S4 to provide the various configuration options as documented in ADIN1300 datasheet Table 10. Default configuration PHY_CFG1/S3 = 1 or 2 (Boards shipped in pairs will have one set to '1' and other set to '2') PHY_CFG0 (S4) = 4
MAC Interface Selection	RX_CTL/RX_DV/CRS_DV/MACIF_SEL1 RXC/RX_CLK/MACIF_SEL0	R8, R9 = DNI R27, R28, = DNI Using internal pull-down resistors => MAC interface default selection = RGMII RXC/TXC 2ns delay

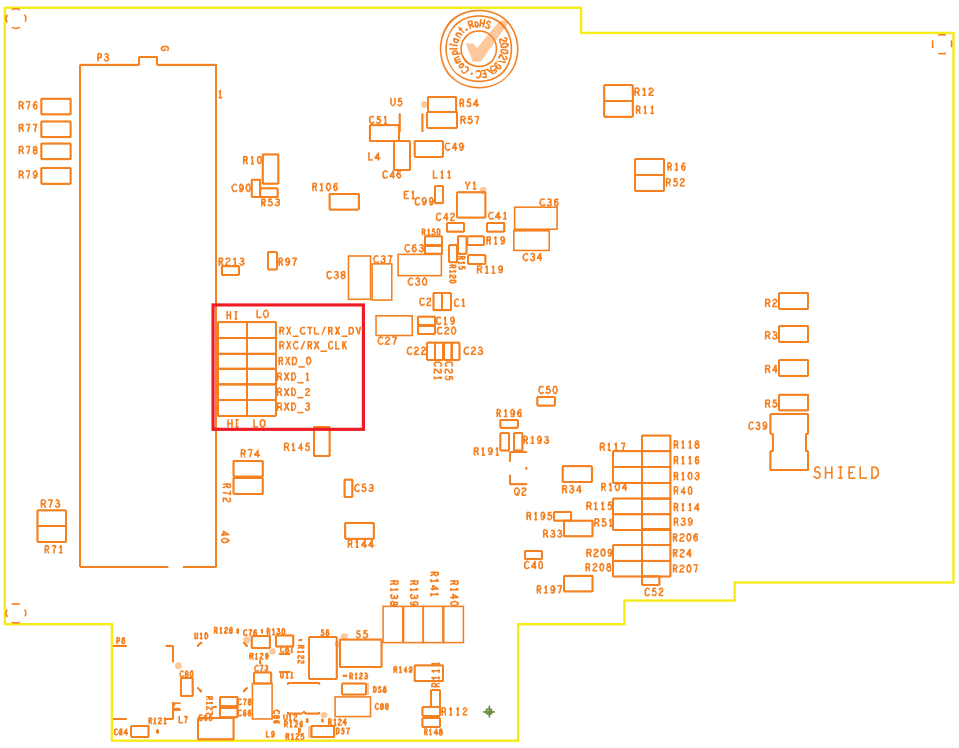

Figure 8. Configuration Resistor Placement – underside of PCB.

SOFTWARE OVERVIEW

INSTALLING THE ADIN1300 SOFTWARE

The EV-ADIN1300FMCZ evaluation kit requires software to be installed on your PC before you begin using the evaluation board. The installation installs the ADIN1300 GUI and associated documentation (datasheet and user guide).

The MDIO interface dongle uses an FTDI chip for UART to USB communication, it requires installation of drivers for the FTDI chip. These drivers are available at: www.ftdichip.com/Drivers/CDM/CDM21228_Setup.zip

The evaluation board software must be installed before connecting the evaluation board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

The default location for installation of the software is C\Analog Devices folder.

Evaluation board Software GUI installation

To install the evaluation board software,

1. Launch the installer file to begin the evaluation board software installation.
2. A dialog box may appear asking for permission to allow the program to make changes to your computer. Click **Yes**.
3. The software install will pop up a welcome screen, click **Next**

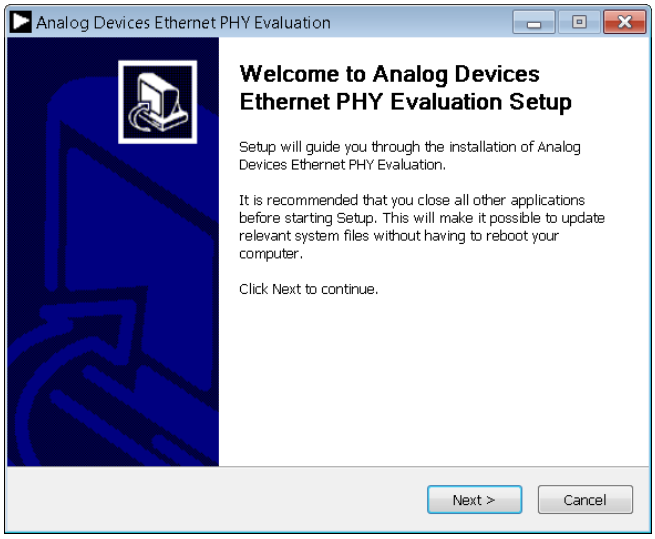

Figure 9. Installation process

4. The software will launch with overview of what is being installed and recommendations in terms of hardware power up, read and click **Next**

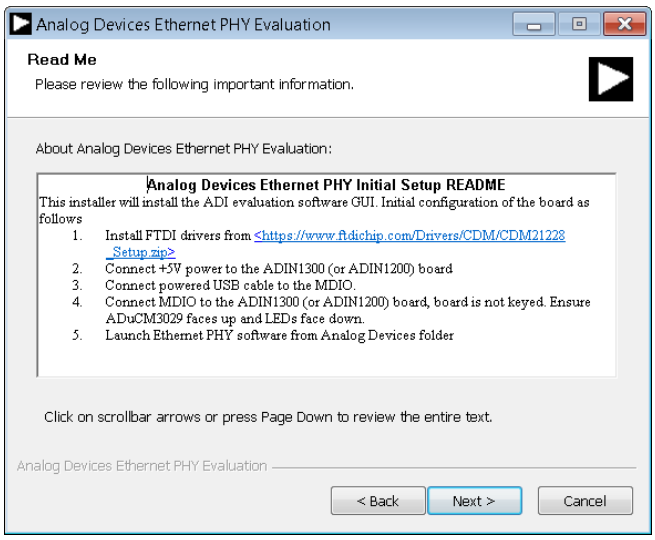

Figure 10. Installation process

5. A license agreement appears. Read the agreement, and then select **I Agree** to allow the installation to proceed.

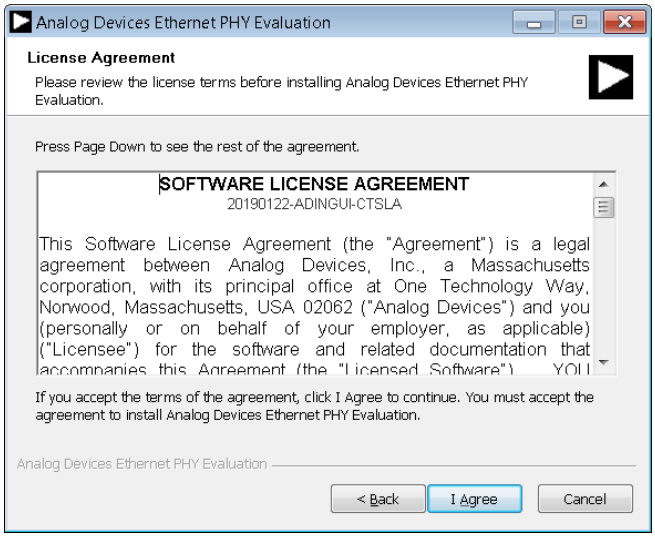

Figure 11. Evaluation Board Software Installation: Accepting the License Agreement

6. Select the location to install the software, and then click **Install**.

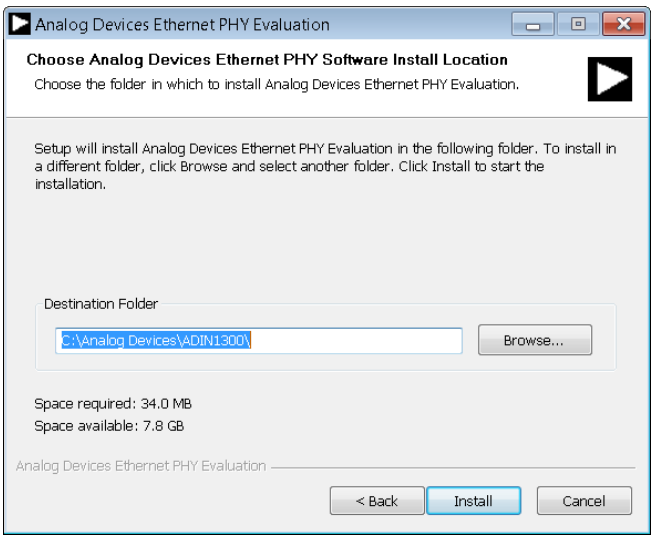

Figure 12. Installation location

7. A dialog box informs you when the installation is complete, click **Finish** to continue.

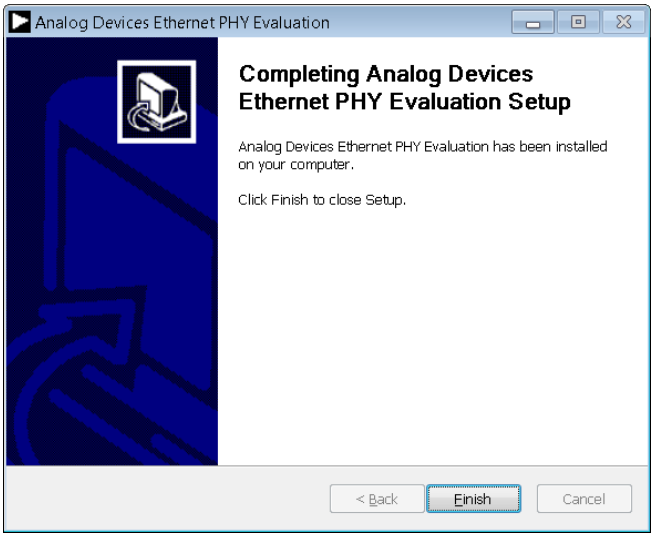

Figure 13. Installation complete

8. The software is installed into the Analog Devices folder on your machine. The software can be accessed via windows explorer via C:\Analog Devices\ADIN1300 Evaluation Software or alternatively through the start menu.

INITIAL SETUP

To set up the EV-ADIN1300FMCZ and use with the Analog Devices GUI, take the following steps:

1. Connect +5V power to the ADIN1300 board via the EXT_5V or the barrel connector
2. Connect USB cable to the MDIO interface dongle. Connect USB cable to PC. When connecting the board to PC for the first time, drivers will automatically be installed. Wait until the driver install is complete before proceeding to the next step.
3. Connect the MDIO interface dongle to the ADIN1300 board, ensuring the ADuCM3029 Microcontroller faces up, see Figure 1. The MDIO interface dongle is not keyed.
4. Launch the ADIN1300 software from the Analog Devices folder in the start menu.

EVALUATION SOFTWARE

When the software is launched, the following GUI panel will open.

The main areas of the GUI are as follows:

1. Board display showing connected evaluation hardware
2. User buttons
3. Link Properties tab
4. Register Access tab
5. Clock Pin Control
6. Loopback
7. Test Modes
8. Frame Checker
9. Cable Diagnostics
10. Board information/linking status
11. Activity log information

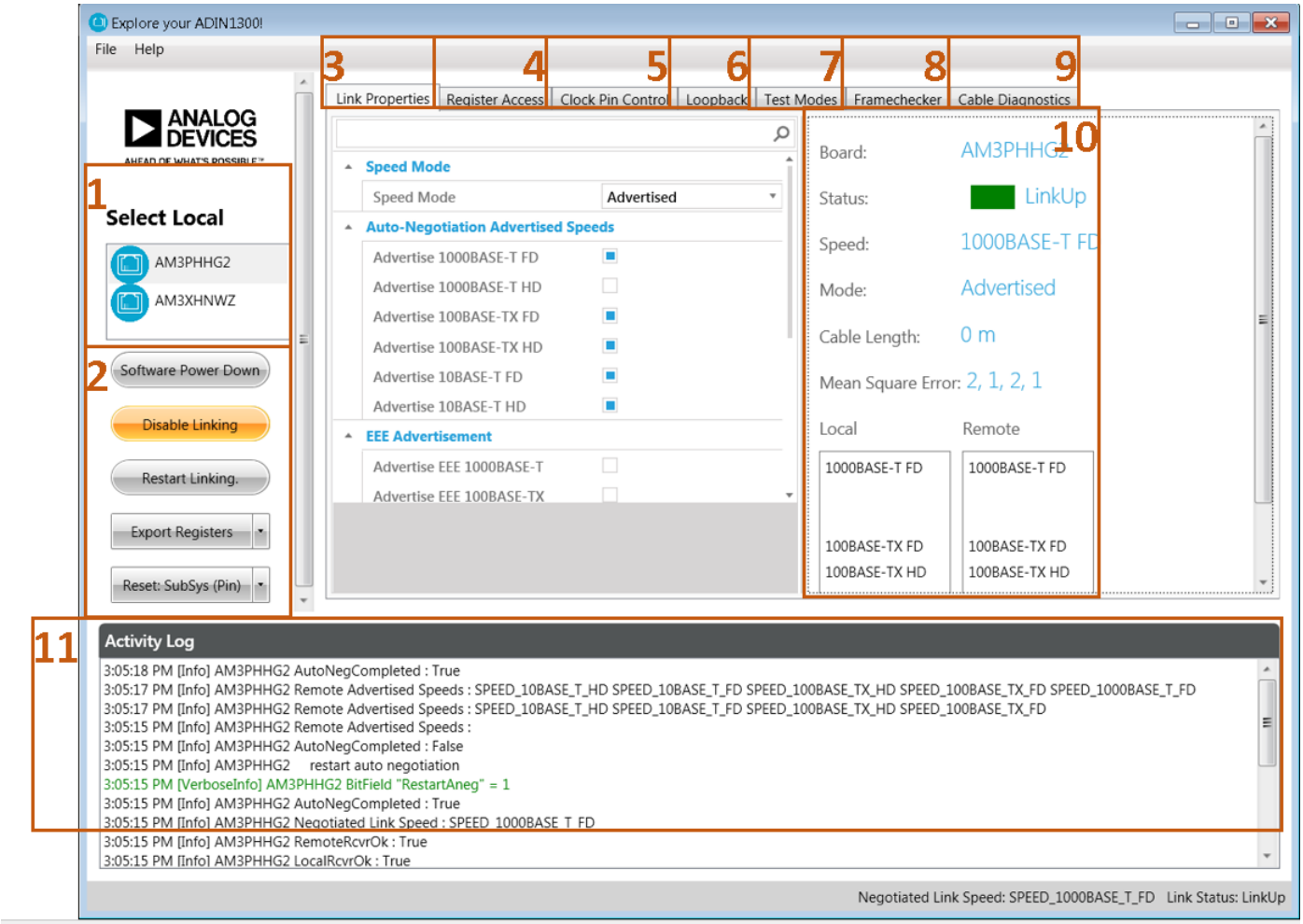

Figure 14. Main GUI Panel

DETAILED OVERVIEW

Board display showing connected EV-ADIN1300FMCZ hardware.

In the "Select Local" field, a unique hardware identifier is shown for each MDIO interface dongle connected to the PC. In the example shown in Figure 13, there are two MDIO interface dongles connected to the same PC.

The user can choose which device is addressed as the Local in this field, by clicking on the appropriate board identifier, it will be highlighted when selected. When selected, all register control, displayed Link Properties and local board information in other sections of the GUI apply to the selected board.

Figure 15. Select which MDIO Interface Dongle is being addressed

User buttons

These buttons allow user to control basic operation of the GUI and device.

Figure 16. Basic user buttons

1. **Software power down/Up:** Allows user to put the device into software power down mode where the analog and digital circuits are placed into low power state, most clocks are gated off and no link will be brought up. Click the button to enable software power down, the button will change to orange color, click again to exit from software power down and restart linking. When software power down is asserted, the other buttons for the selected device are greyed out and disabled.
2. **Disable/Enable Linking:** If a link is up and user wishes to disable linking, click this button.
3. **Restart Linking:** If user has changed software configuration and wishes to restart linking process with a new configuration, click this button. If Link has already been established, the link will first be brought down, then restarted.
4. **Export Registers:** Click this button to do a data dump to the "Activity log" field. From there the register dump can be saved to text format for later offline review. Right click and "Save as" to save to a log file.

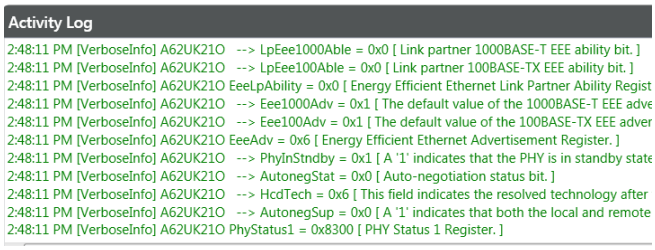

Figure 17. Activity log – displaying export registers

5. **Reset:** This dropdown allows user to initiate different types of resets

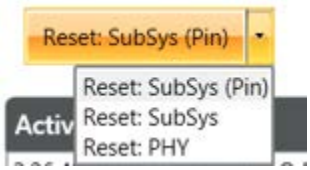

Figure 18. Reset Options

   a. Sub-System Software Reset with Pin Configuration
      i. "**SubSys (Pin)"** reset performs a reset of the Sub-system with the Sub-system requesting a new set of hardware configuration pin settings from the chip during the software reset sequence.
      ii. GeSftRst = 1, GESftRstCfgEn = 1
   b. Sub-System Software Reset:
      i. "**SubSys**" reset performs a reset of the Sub-system with the Sub-system requesting previously stored hardware configuration pin settings to be reloaded during the software reset sequence.
      ii. GeSftRst = 1, GESftRstCfgEn = 0
   c. PHY Core Software Reset:
      i. "**PHY**" reset: SftRst bit resets the PHY core registers.

Link Properties tab

The Link Properties tab gives user access to the main linking configurations within the device. This window has a slider to access all the controls. When a control is selected, the GUI will provide a prompt describing the function at the bottom of the linking control box.

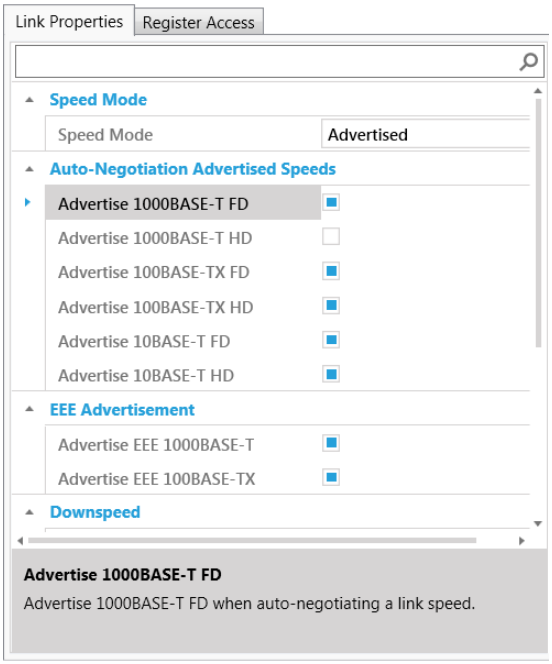

Figure 19. Link Properties Control

Speed Mode: For the selected device, user can choose to select from Advertised or Forced. This choice prepopulates the remaining user controls for the Link Properties tab as follows:

1. **Advertised**:
    a. Auto-Negotiated Advertised Speeds: Checkbox availability of all Auto-Negotiated Advertised speeds available. User can select/deselect as required. All speed options are available here. Default advertised will reflect Hardware configuration pins.
    b. EEE Advertisement: Checkbox to allow user advertise Energy Efficient Ethernet (EEE) as a speed option for 1000BASE-T and 100BASE-TX.
    c. Downspeed: Checkbox to allow user enable Downspeed which allows the PHY to change down to a lower speed after a number of attempts to bring up a link at the highest advertised speed.
        i. Downspeed Retries sets the number of time the PHY will attempt to bring up a link. Default is 4.
    d. MDIX: Dropdown box to choose between Auto MDIX, FixedMDI or FixedMDIX
    e. Energy Detect PowerDown Mode: dropdown to choose between disabled, enabled or EnabledWithPeriodicPulseTx
    f. Master/Slave: Dropdown option, defaults to Slave
2. **Forced** : Subset of control available in Forced mode
    a. Forced Speeds: Dropdown box to choose the required speed
    b. MDIX: Dropdown box to choose between Auto, FixedMDI or FixedMDIX
    c. Energy Detect Powerdown Mode: Dropdown to choose between disabled, enabled or EnabledWithPeriodicPulseTx
    d. Master/Slave: dropdown option, defaults to Slave

Register Access tab

The 'Browse" tab in the Register Access field allows user to review the bank of registers and edit register fields or bit fields as required.

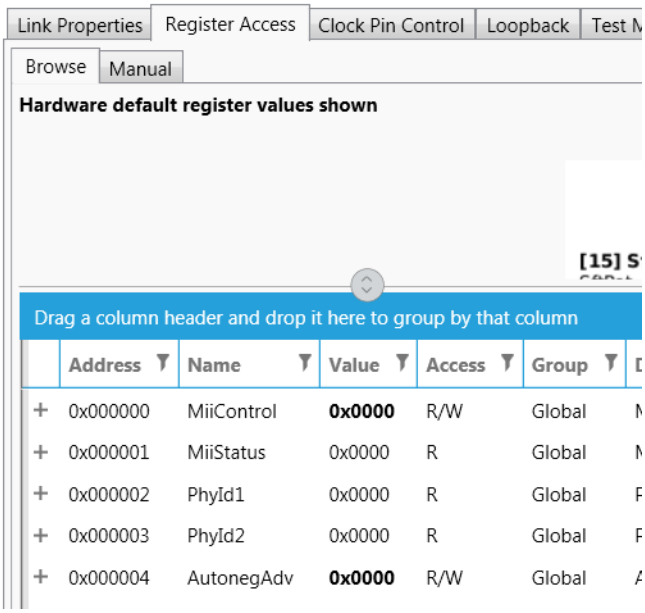

Figure 20. Register Access – full register map

The "Manual" tab enables user to perform basic reads from and write to individual registers in the ADIN1300.

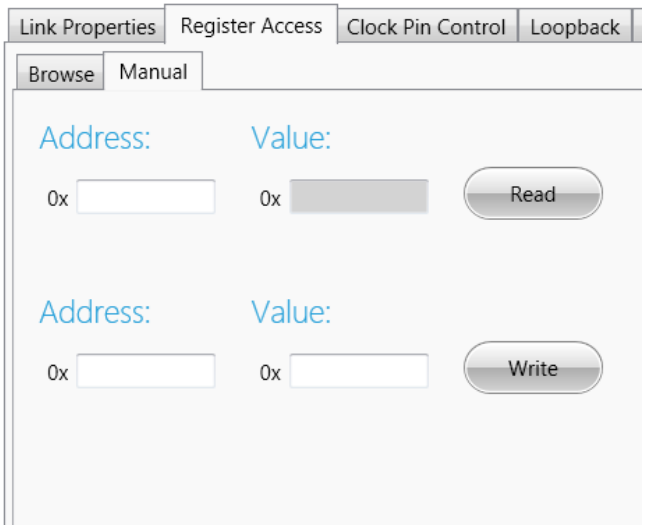

Figure 21. Register Access

The direct register read/write access can also be accessed from the right of the Activity log panel, just slide the arrow over to the left to expose it.

Figure 22. Register Access

Clock Pin Control

This section provides user ability to control what clock is applied to the GP_CLK pin and also enable the CLK25REF.

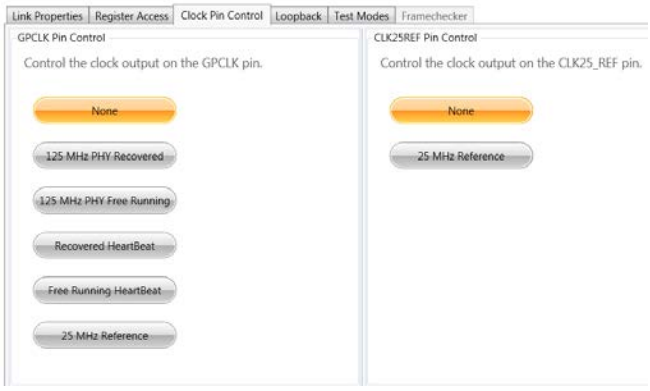

Figure 23. Clock Pin Control

Loopback

The various loopback modes are available in this tab. Consult the datasheet for full description of each loopback mode.

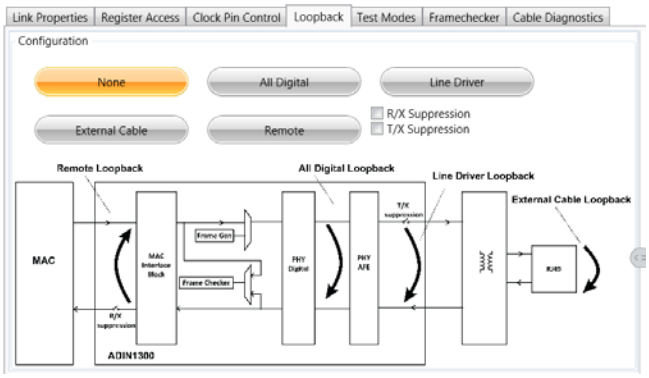

Figure 24. Loopback Modes

Testmodes

The Test Modes tab allows user initiate the various test mode functions in the device. Select the appropriate test mode and click the 'Execute Test' button.

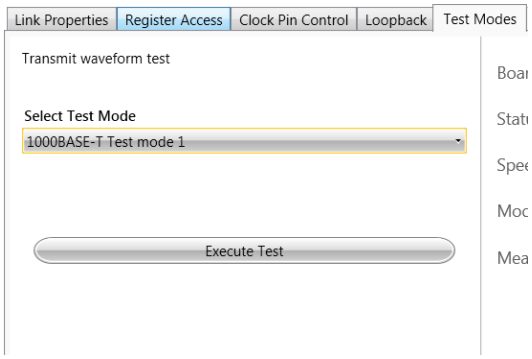

Figure 25. Testmodes

Framechecker

The Framechecker tab provides access to the frame generator & frame checker features of the ADIN1300.

The user can control the number of frames generated by the generator, the frame length and the content of the frame. The user has option to have the frame generator run in burst mode or run continuously. When running continuously, the Terminate button allows user to halt frame generation.

The Loopback button allows user to enable the remote device to loopback the data to the local device. Ensure to select the appropriate device, e.g. decide which of the connected boards is the local, configure that to generate frames, then configure the other devices in remote loopback.

The checker information displayed on the screen accumulates the number of frames sent and shows the number of errors observed.

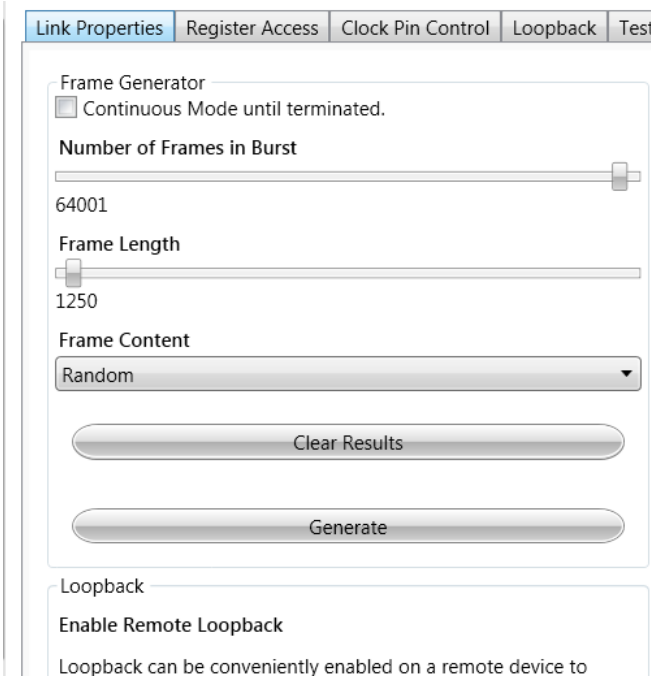

Figure 26. Overview of Frame Generation/Checker

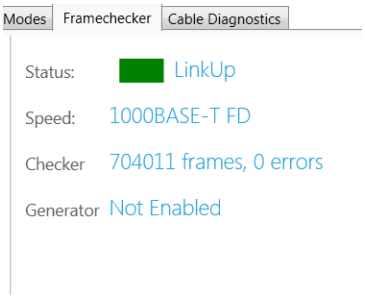

Figure 27. Display of Frame Generator status and Frame Checker result

Cable Diagnostics

The cable diagnostic feature allows user to diagnose issues with the link. There are various features within the device, some that are available when the Link is up and quantify the quality of the link, e.g. MSE level and estimated cable length. These are displayed on the main Link Properties tab.

The features contained in the Cable diagnostic tab are the ones that can be run when the link is disabled such as checking for shorts, opens and identifying the distance to the first fault. The LinkEn bit must be clear to run these checks, there

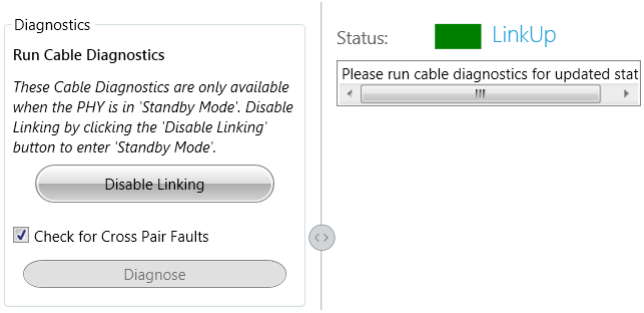

Figure 28. Cable diagnostics Configuration, when Link is up

Click the disable linking button to set LinkEn =0 to allow diagnostics to be run.

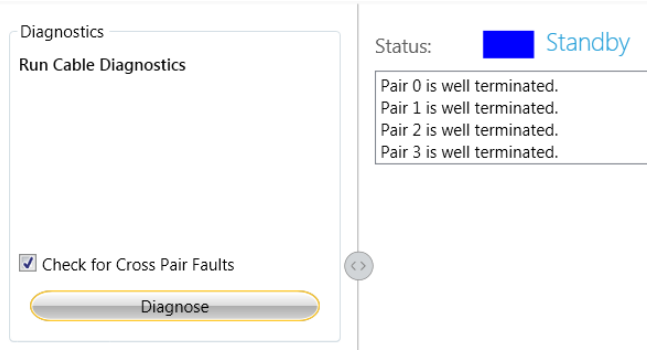

Figure 29. Cable diagnostics Configuration, when Link is disabled by clicking "Disable Linking" button, with a cable connected to a remote PHY

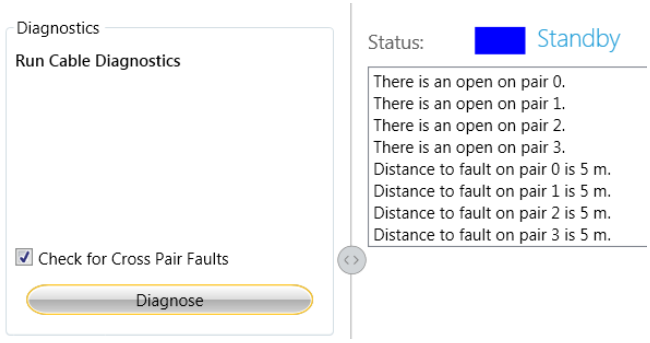

Figure 30. Cable diagnostics Configuration, when Cable is open

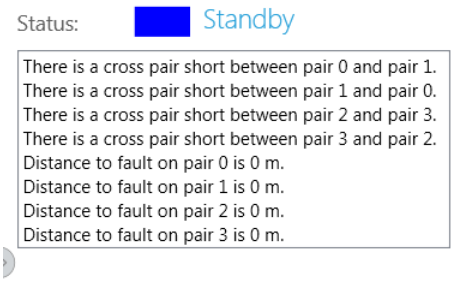

Figure 31. Cable diagnostics Configuration, when Cable is crossed

Board information/linking status

This section displays the current status of the selected PHY chip (as determined in the "Select local" section), including whether a link is established, the speed of the link and the speed mode. The local and remote fields show the advertised speeds that are available in the local device (the selected device/board) and also what the remote PHY is returning.

If the user switches between two boards in "Select local" section, the information shown in these fields will be updated to reflect the information provided from the board defined as local.

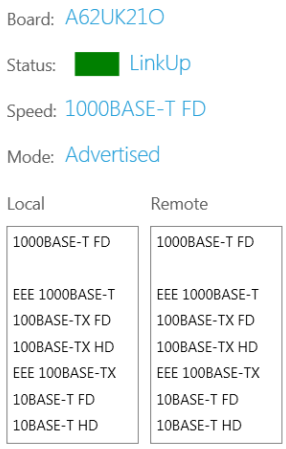

Figure 32. Board status information

The LED shows the status of the selected PHY, depending on how the user has the device configured.

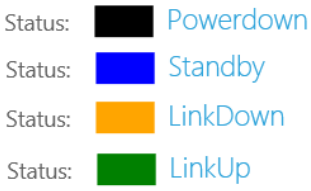

Figure 33. Status LED

Activity log information

The activity log reports status information and register writes issues to the selected board. It captures the activity in the GUI corresponding to user button presses and information on whether a link is established.

The board ID is recorded with each bit field change, so it is clear which device is being addressed.

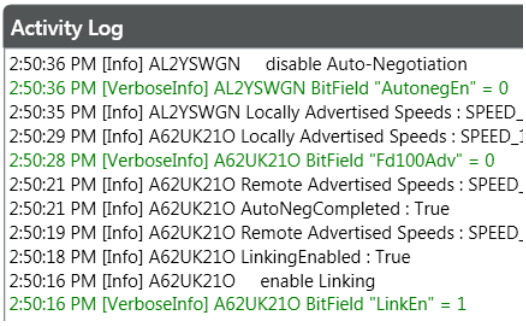

Figure 34. Board status information

The activity log can be cleared by right-clicking and selecting "Clear". The contents of the activity field can be exported for offline review by right-clicking and choosing "Save as". The file saved is a text file, with default location in the Analog Devices ->ADIN1300 folder.

Loading a script file

The GUI allows user to load a sequence of register commands from a file. The file is located in the ADIN1300 folder and called "registers_scripts.json"

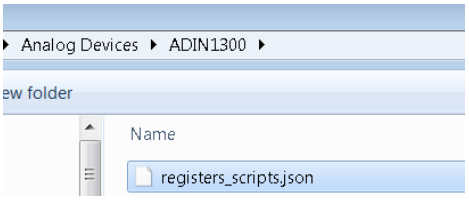

Figure 35. Location of the script file

The register commands can be loaded with either the register name or the register address as shown in the simple examples in the file. The commands are loaded sequentially, so create the sequence of write commands using a text editor, ensure to copy the exact syntax and match the register names with that in the datasheet (otherwise errors will be reported in the activity log). Give your script a unique and meaningful name. Example shown below for "SftPd Down&Up" routine.

```
{
 "Name": "SftPd Down&Up",
 "RegisterAccesses": [
  {
   "MemoryMap" : "GEPhy",
   "RegisterName": "SftPd",
   "Value": 1
  },
  {
   "MemoryMap" : "GEPhy",
   "RegisterName": "SftPd",
   "Value": 0
  },
 ]
},
```

Within the GUI window, there are two dropdown options under the Activity log where the script file can be selected and which section of the script to run. Click the button to load selected script.

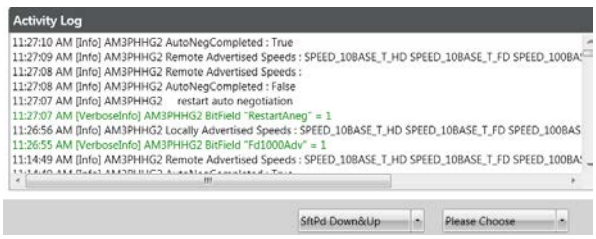

Figure 36. Script load – dropdown buttons

TROUBLESHOOTING

INSTALLATION TIPS

- Always allow the installation to fully complete (the software is a two part installation: the ADI package installer (GUI and documentation) and the FTDI drivers which can be found at www.ftdichip.com/Drivers/CDM/CDM21228_Setup.zip). The installation may require a restart of the PC.
- When you first plug in the MDIO interface dongle via the USB cable, allow the New Found Hardware Wizard to run completely. Though this may take some time, it is required prior to starting the software.
- Where the board does not appear to be functioning, ensure the following:
    - Power is applied to the ADIN1300 evaluation board
    - Powered USB connector is applied to the MDIO interface dongle.
    - Both boards are connected together.
    - Ethernet cables connected
    - Launch software

SOFTWARE TIPS

If the software does not read any data back, observe if there are any messages in the Activity log. There is one known communication bug in the connection of the MDIO interface dongle and ADIN1300 evaluation board as discussed below:

MDIO Board communications – Known Issue

A known behavior when using the MDIO interface dongle with the ADIN1300 board is related to how the boards are powered/connected together. If user connects MDIO interface dongle to ADIN1300 board before connecting USB power to dongle AND user has GUI open, there is a possibility the GUI may not properly establish communications with the MDIO board.

The GUI polls for the MDIO interface dongle regularly and if an error in MDIO communications is found, it will be flagged in the activity log and highlighted in red font, see Figure 12. The message will also include prompt how to resolve the issue.

In this example, user is advised to reset the MDIO interface dongle through Button S6. There are two buttons on the underside of the MDIO interface dongle, identify S6 and reset. This will restart the MDIO interface dongle. If S6 restart does not resolve communications, exit the GUI and re-launch.

Future software revisions will look to resolve.

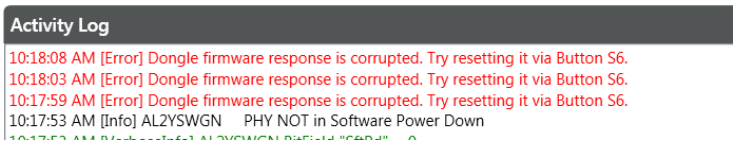

Figure 37. Example Activity log when MDIO board is not responding

HARDWARE TIPS

Check that power is applied to the both boards as discussed above. Measure the voltage at various points on the ADIN1300 board using the Test points (DVDD, VDD0P9, 5V, AVDD3P3, VDDIO) Crosscheck the voltages versus the detail in Table 1.

No Link established

- Check the cables are connected correctly to the RJ-45 connector and between boards or PHY pairs.
- Where using two ADIN1300 boards, check both boards are powered.
- Check the Hardware configuration is appropriate for required linking arrangement
    - If changes have been made to PHY_CFG0/1switch configuration, review corresponding LED0 arrangement for MODEx operation.

LED0 not blinking, but Link Established reported in GUI

By default LED_0 is on when a link is established and it blinks when there is activity. The ADIN1300 evaluation board is configured for Mode 3 & 4 by default, with R191 and R192 resistors populated. If user wishes for PHY_CFG0 to be used in Mode 1 or 2, remove R191 and R192 and insert R110. If changes have been made to PHY_CFG0/1 switch configuration, review corresponding LED0 arrangement for MODEx operation.

LAYOUT GUIDELINES

BOARD STACK-UP

The evaluation board consists of a four layer board. Top Layer, Layer 2, Layer 3 and Bottom Layer. All layers have a copper pour, with exception being around sensitive traces for the MAC and MDI interfaces.

GROUND PLANES

The top and bottom layers carry mainly signal and routing from the ADIN1300. The two inner layers are used for ground planes. Layer 2 is a full ground plane. Layer 3 contains primarily ground with area dedicated to DVDD and VDDIO power planes. While the ADIN1300 is a mixed signal device, there is just one type of ground return, GND.

ISOLATION GUIDELINES

Transformer layout

There should be no metal layers directly underneath the transformer to minimize any noise coupling across the transformer.

RJ-45 layout

For good EMC performance, it is recommended to use a metal shielded RJ-45 connector with the shield connected to chassis ground. There should be an isolation gap between the chassis ground and the IC GND with consistent isolation across all layers.

POWER SUPPLY DECOUPLING

From a PCB layout point of view, it is very important to locate the decoupling capacitors as close as possible to the power and GND pins to minimize the inductance.

MAC INTERFACE

When routing the TX/RX traces, ensure to match the lengths of the pairs. Avoid crossover of the signals where possible. Stubs should be avoided on all signal traces. It is recommended to route traces on the same layer.

MANAGEMENT INTERFACE

MDI interface

Traces running from the MDI_[x]_P/N pins of the ADIN1300 to the Magnetics must be on the same side of the board (no vias), kept as short as possible (less than 1" in length) and individual trace impedance of these tracks kept below 50 Ω, with differential impedance of 100 Ω for each pair. The same recommendations apply for traces running from the magnetics to the RJ45 connector.

Impedance should be kept constant throughout as any discontinuities could impact signal integrity.

Each pair must be routed together, trace widths the same throughout, trace lengths should be kept equal where possible and avoid any right angles on these traces (use curves in traces or 45° angles). Stubs should be avoided on all signal traces. It is recommended to route traces on the same layer.

PLACEMENT OF THE TVS

It is recommended to place the TVS close to the ADIN1300 device, to ensure minimal track inductance between the external protection and internal protection within the device.

THERMAL CONSIDERATIONS

The ADIN1300 is packaged in an LFCSP package. This package is designed with an exposed paddle which must be soldered to the PCB for mechanical and thermal reasons. The exposed paddle acts to conduct heat away from the package and into the PCB. By incorporating an array of thermal vias in the PCB thermal paddle, heat is dissipated more effectively into the inner metal layers of the PCB.

When designing the PCB layout for optimum thermal performance, we recommend to use a 3x3 array of vias under the paddle.

Note the initial evaluation board (Rev A) has an exposed solder land pattern on the board to which the device is soldered, however, it does not currently incorporate a fully populated array of vias underneath the paddle, future revisions of hardware will include.

This LFCSP package includes two exposed power bars adjacent to the exposed pad at the top and bottom, highlighted red in Figure 4. These are connected to internal power rails, the area around these is a keep-out zone. Keep these areas clear of traces or vias.

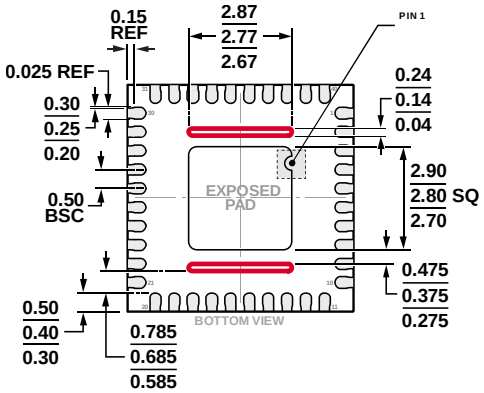

Figure 38. LFCSP simplified package drawing highlighting keepout area for power bars on underside of package

EVALUATION BOARD SCHEMATIC AND ARTWORK

REV A SCHEMATIC

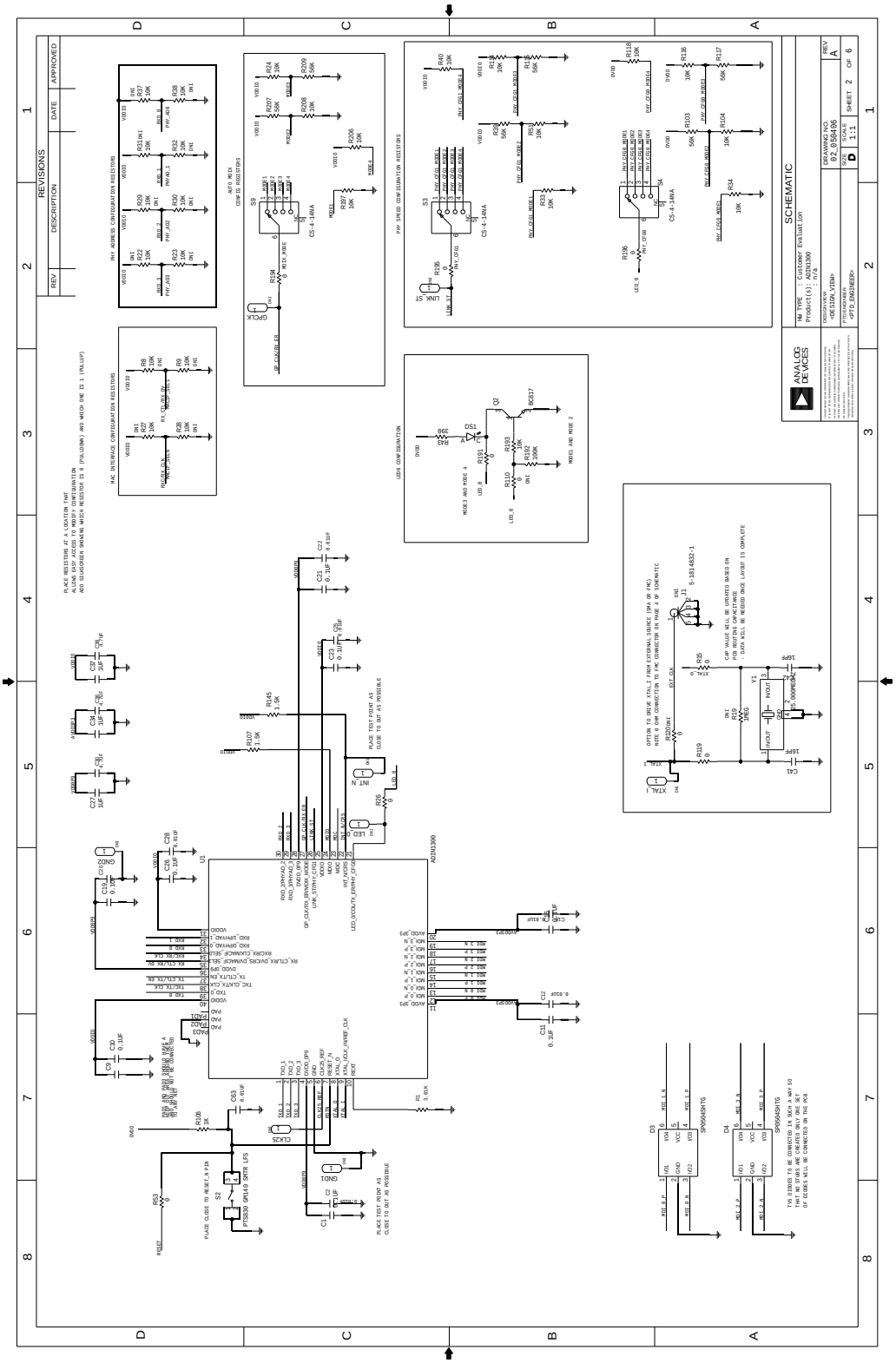

Figure 39. Schematic – page 1.

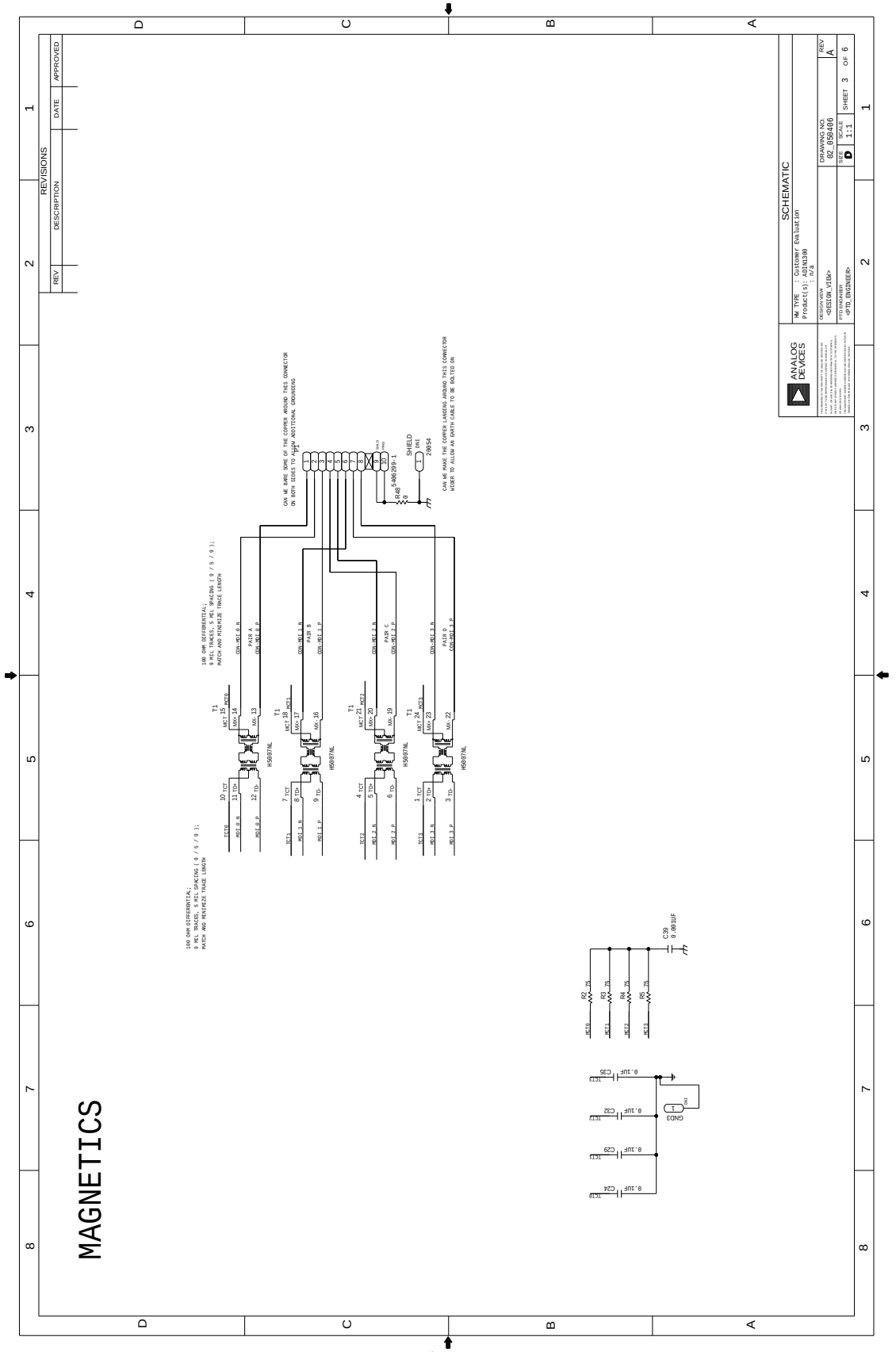

Figure 40. Schematic – page 2.

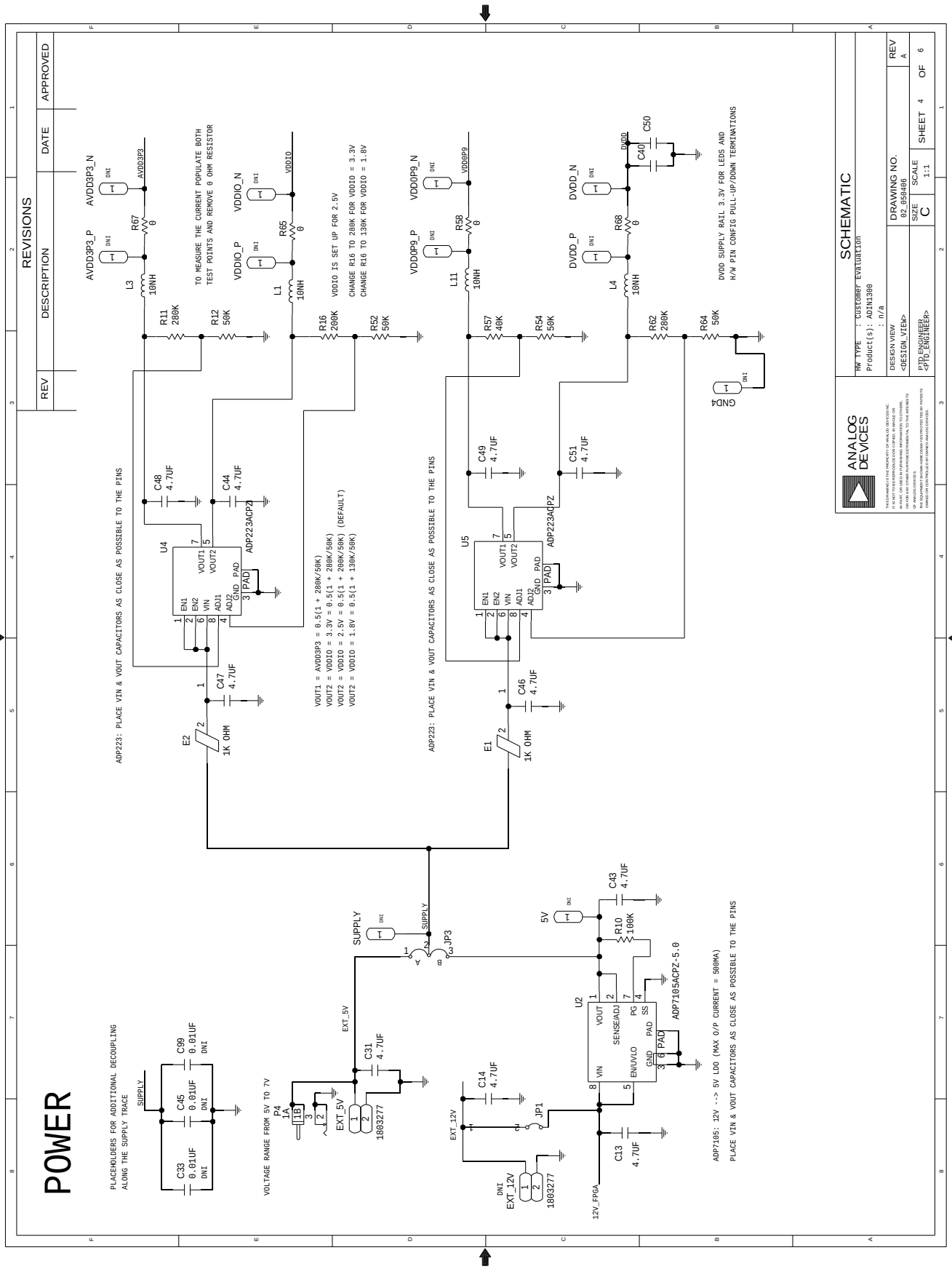

Figure 41. Schematic – page 3.

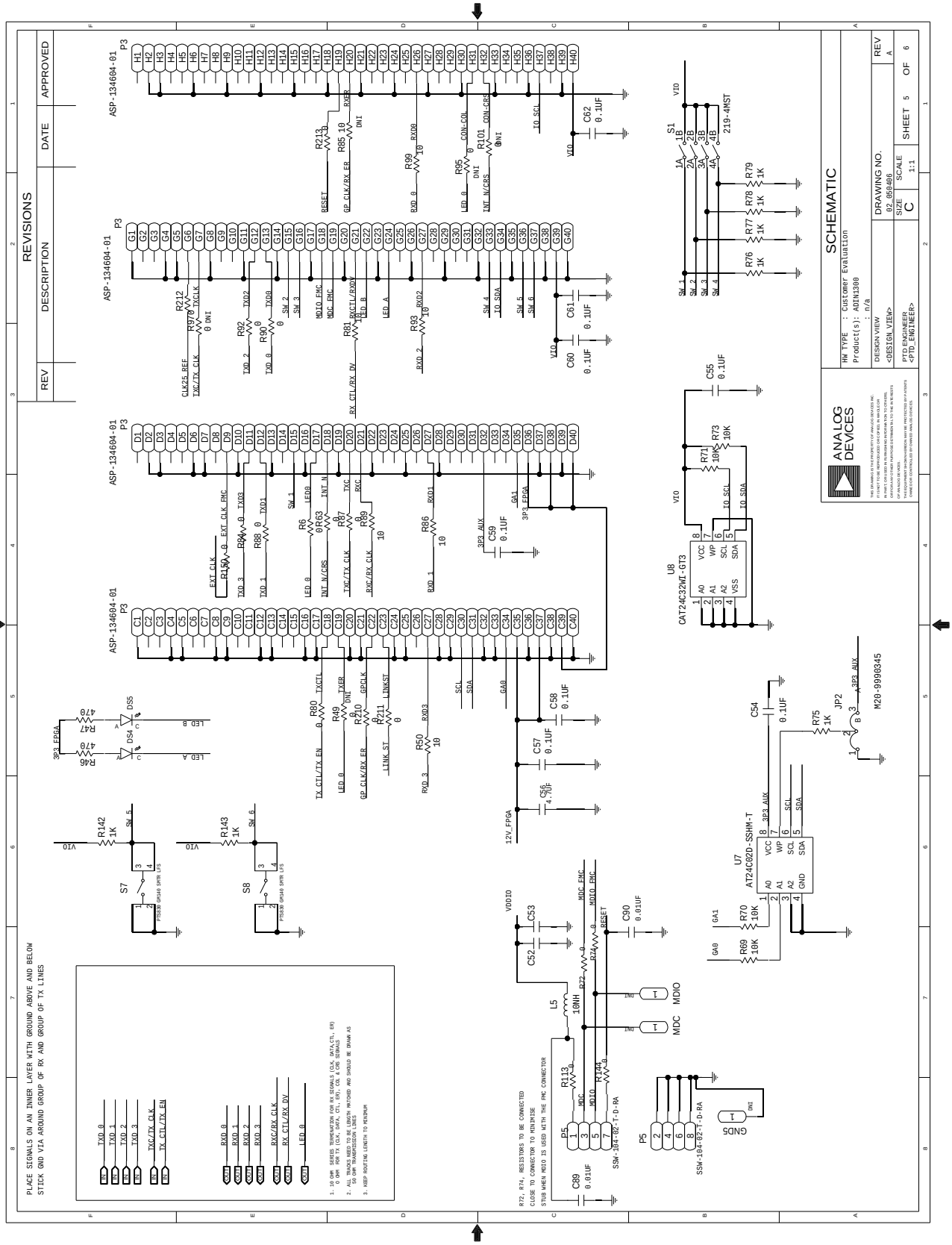

Figure 42. Schematic – page 4.

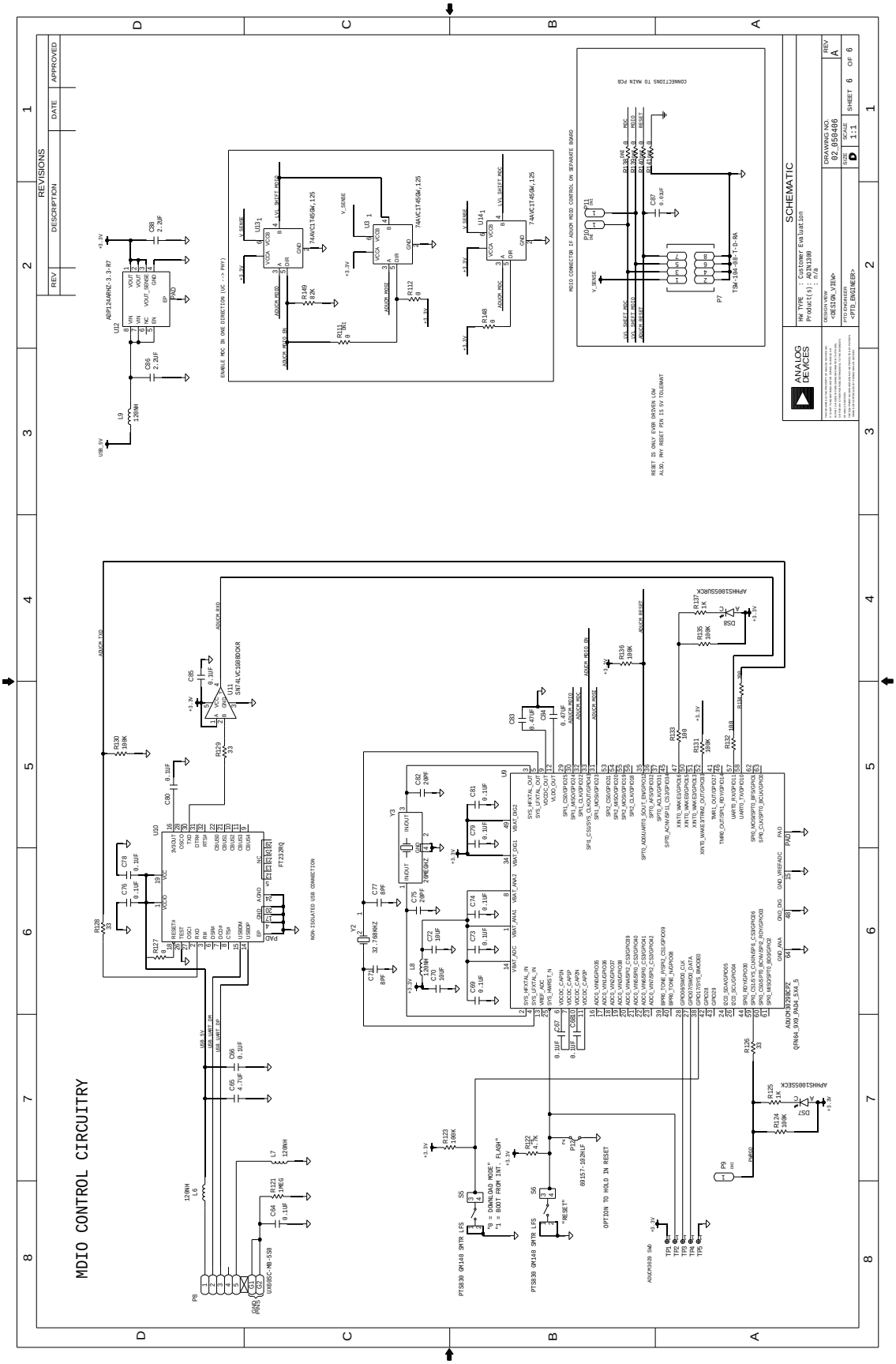

Figure 43. Schematic – page 5.

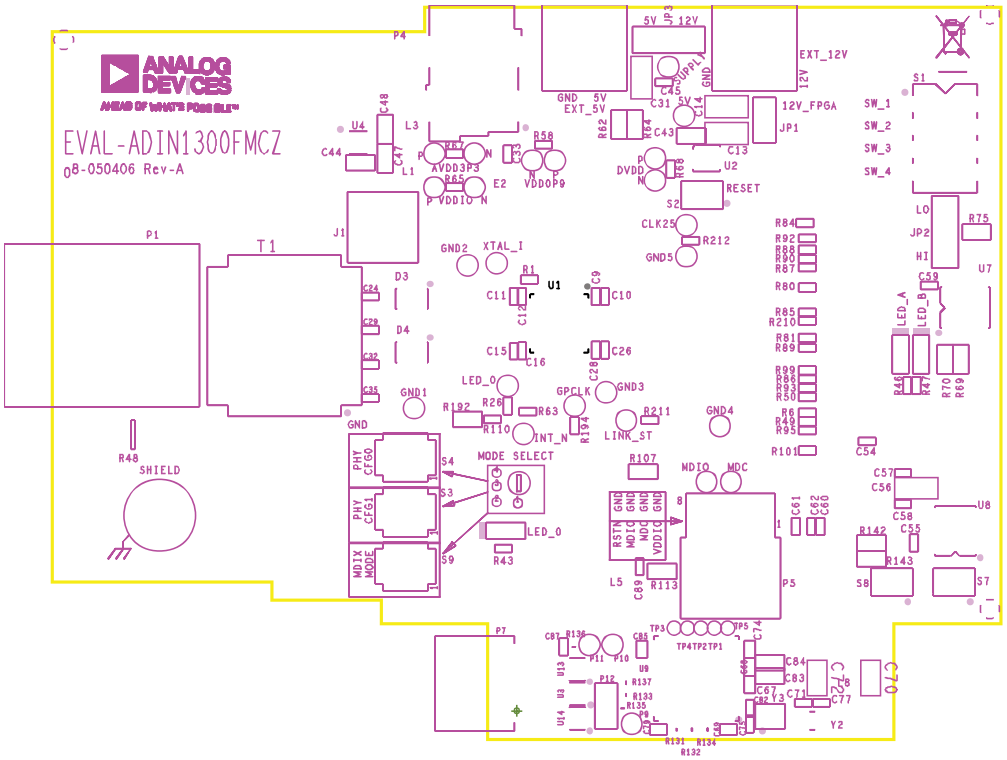

Figure 44. Silkscreen Top

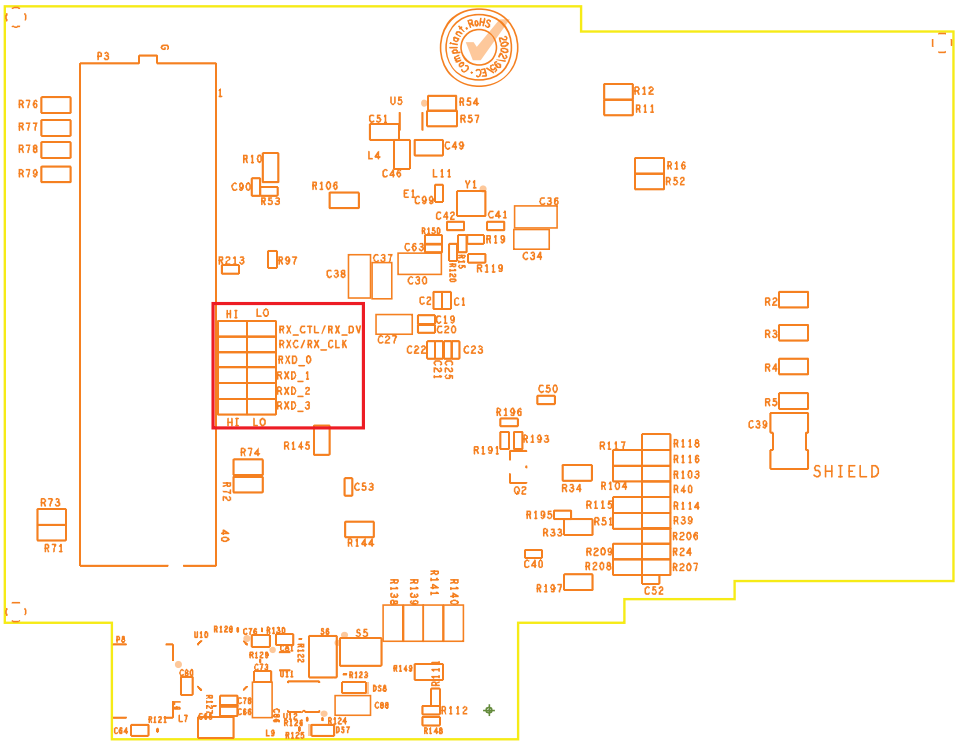

Figure 45. Silkscreen Bottom

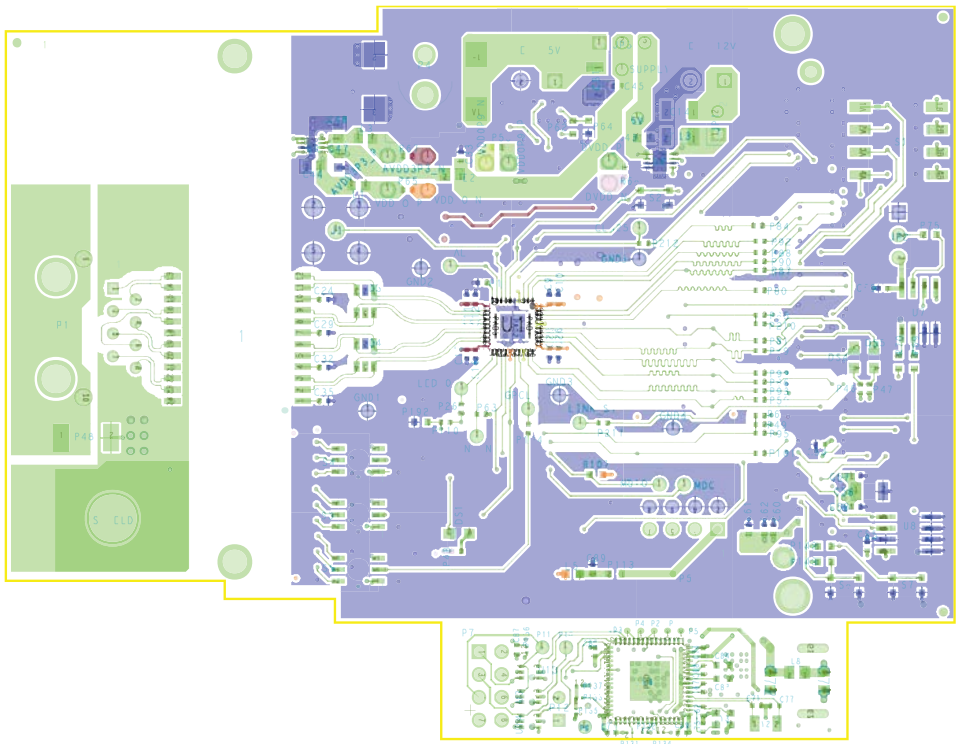

Figure 46. Top PCB Layer

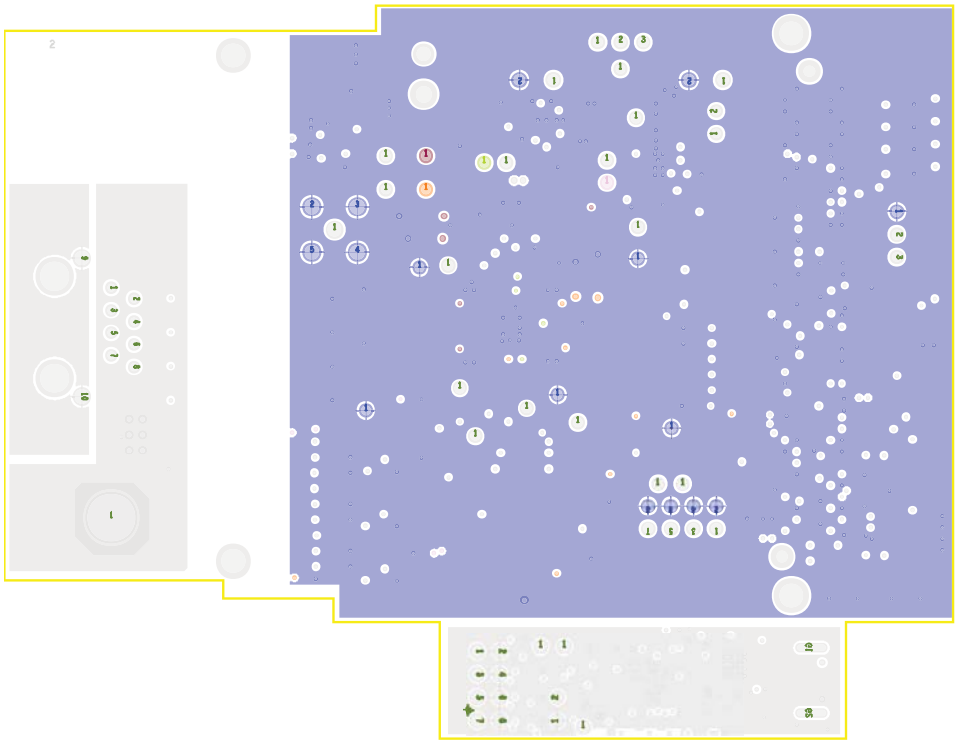

Figure 47.Inner PCB Layer 1 (GND)

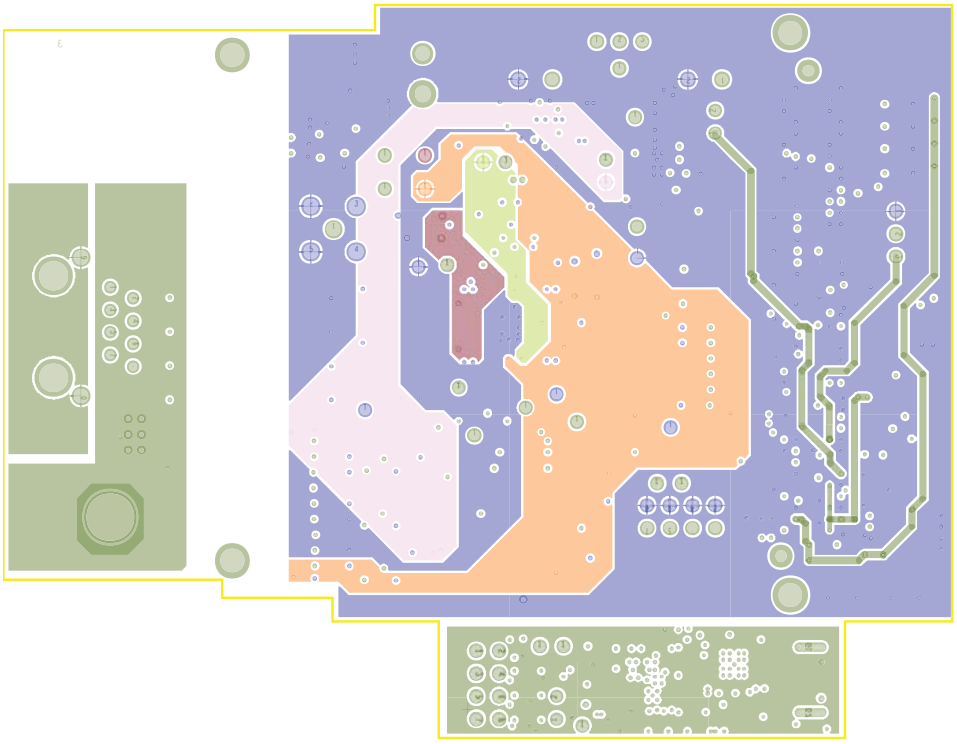

Figure 48. Inner PCB Layer 2(Power)

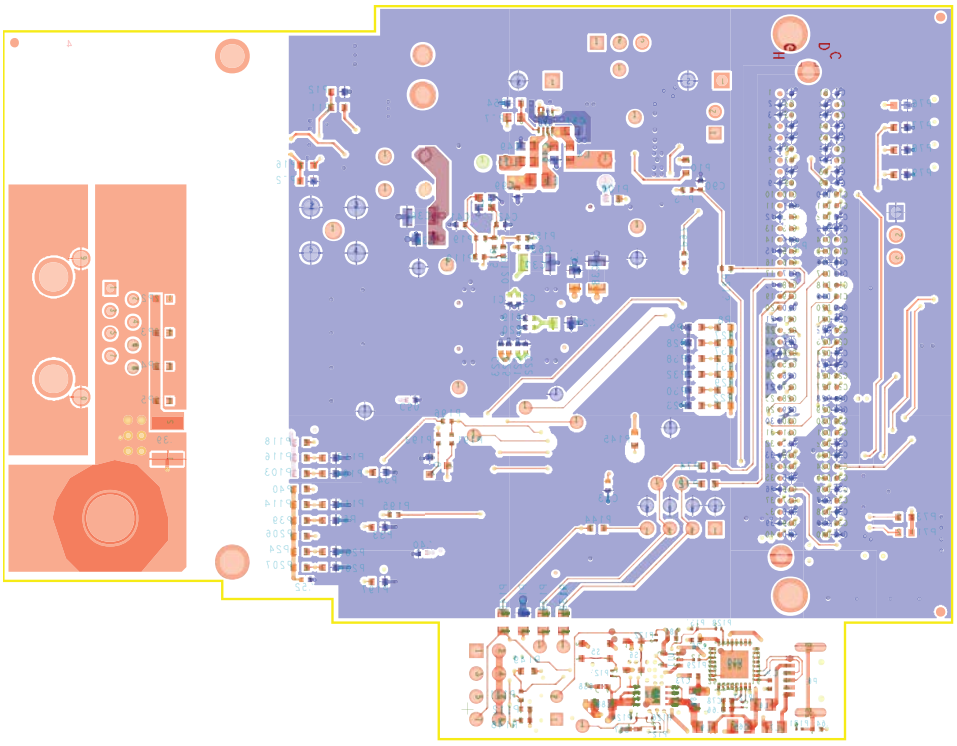

Figure 49. Bottom PCB Layer

REV B SCHEMATIC

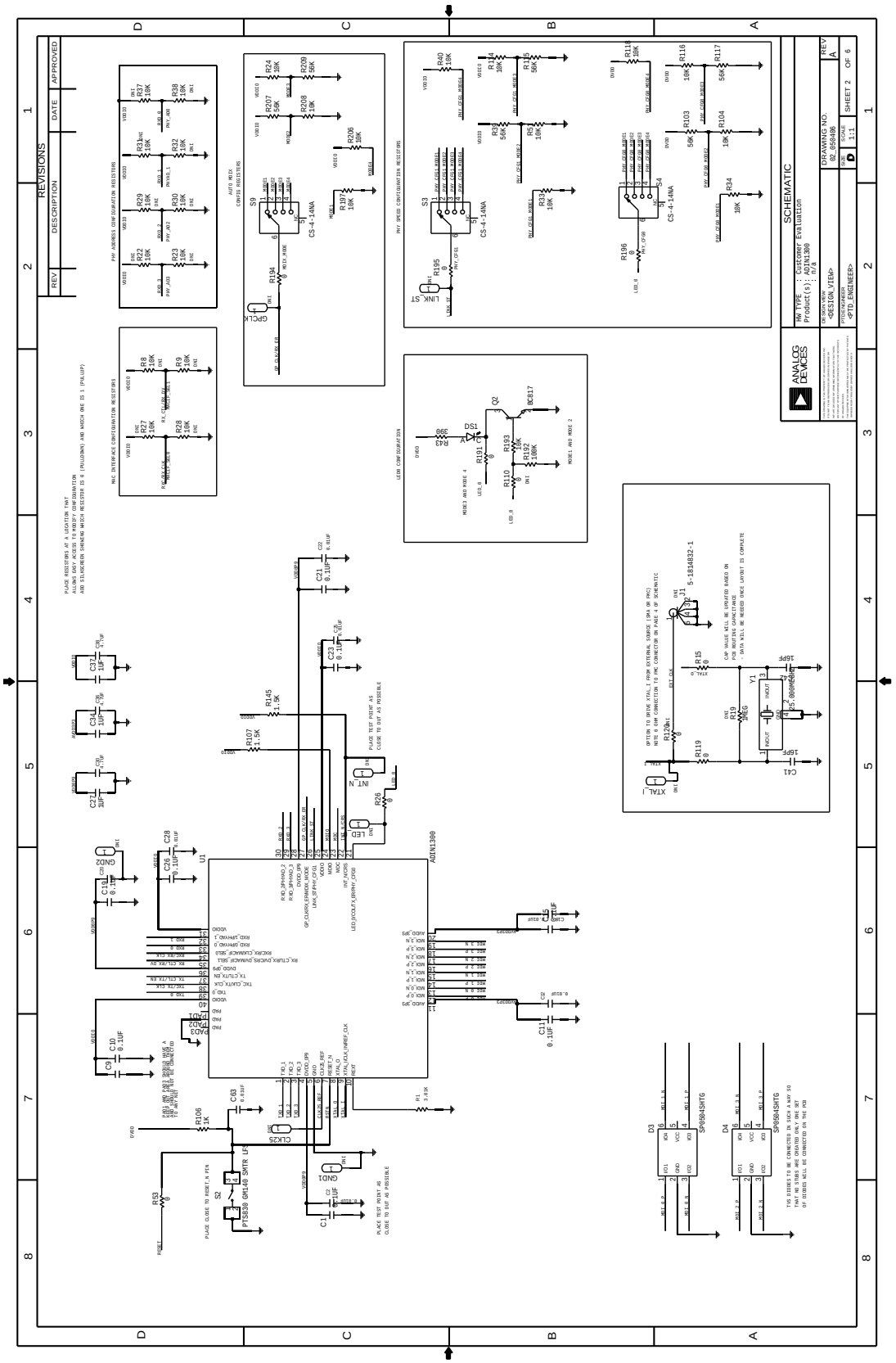

Figure 50. Rev B Schematic – Page 1

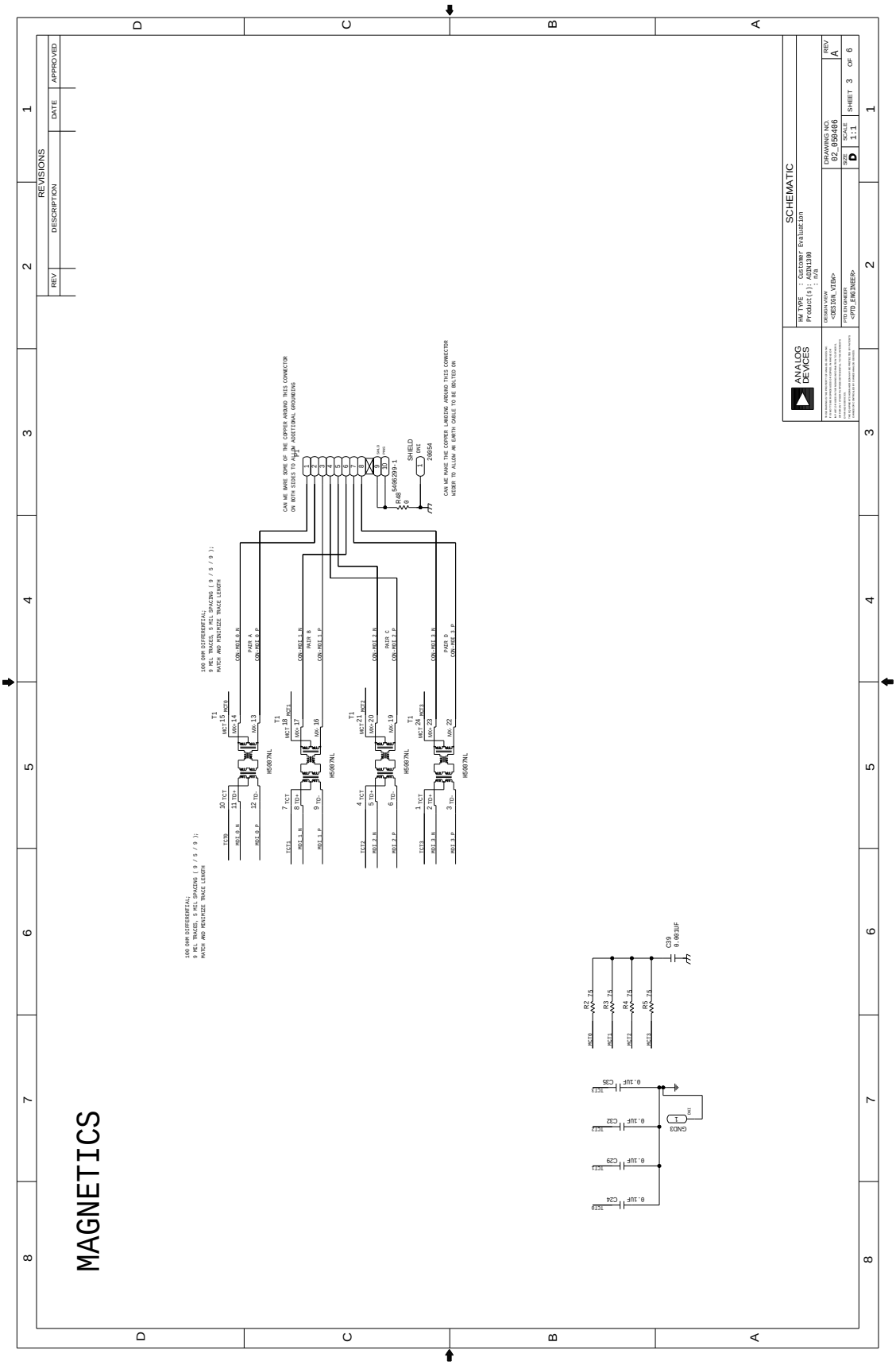

Figure 51. Rev B Schematic – Page 2

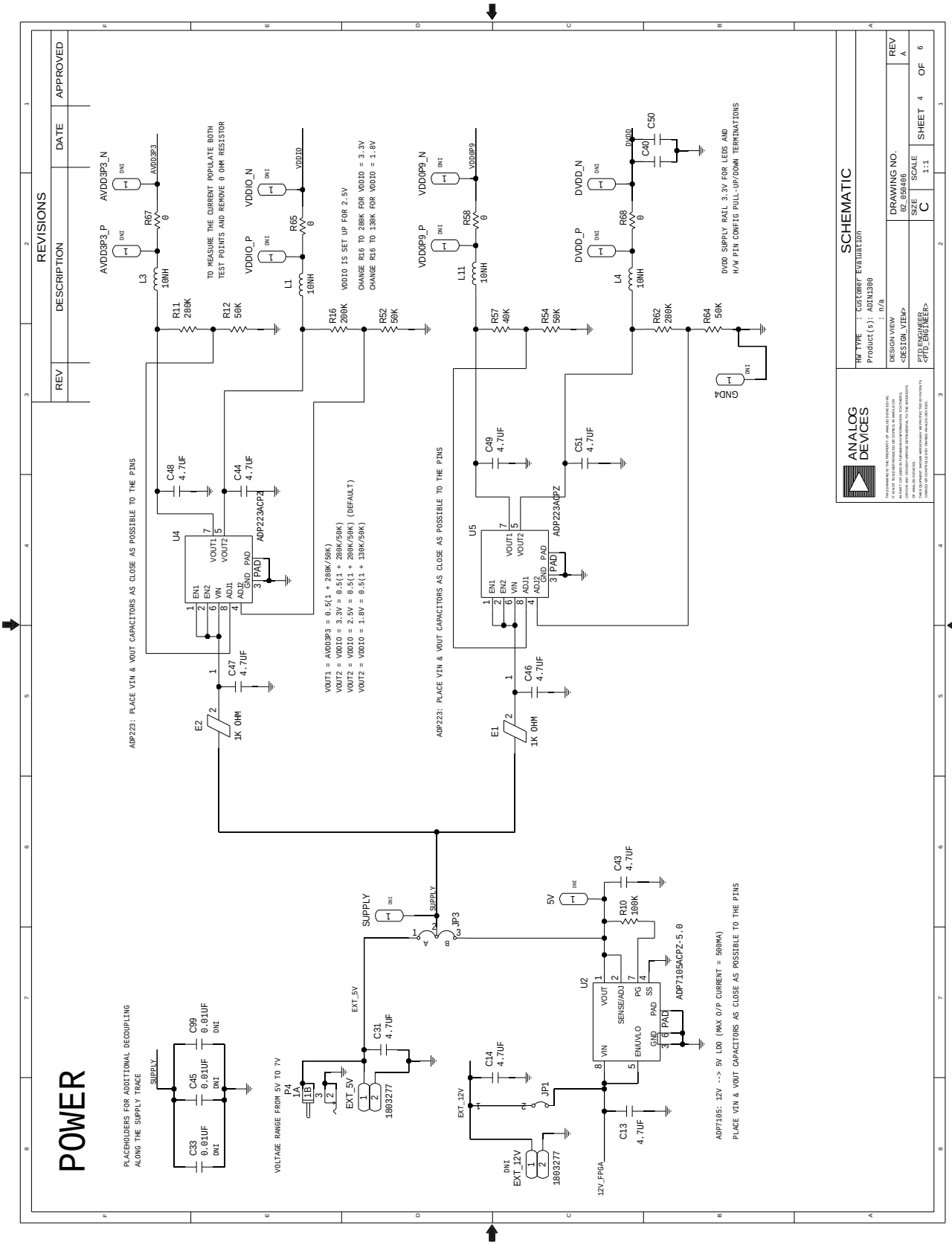

Figure 52. Rev B Schematic – Page 3

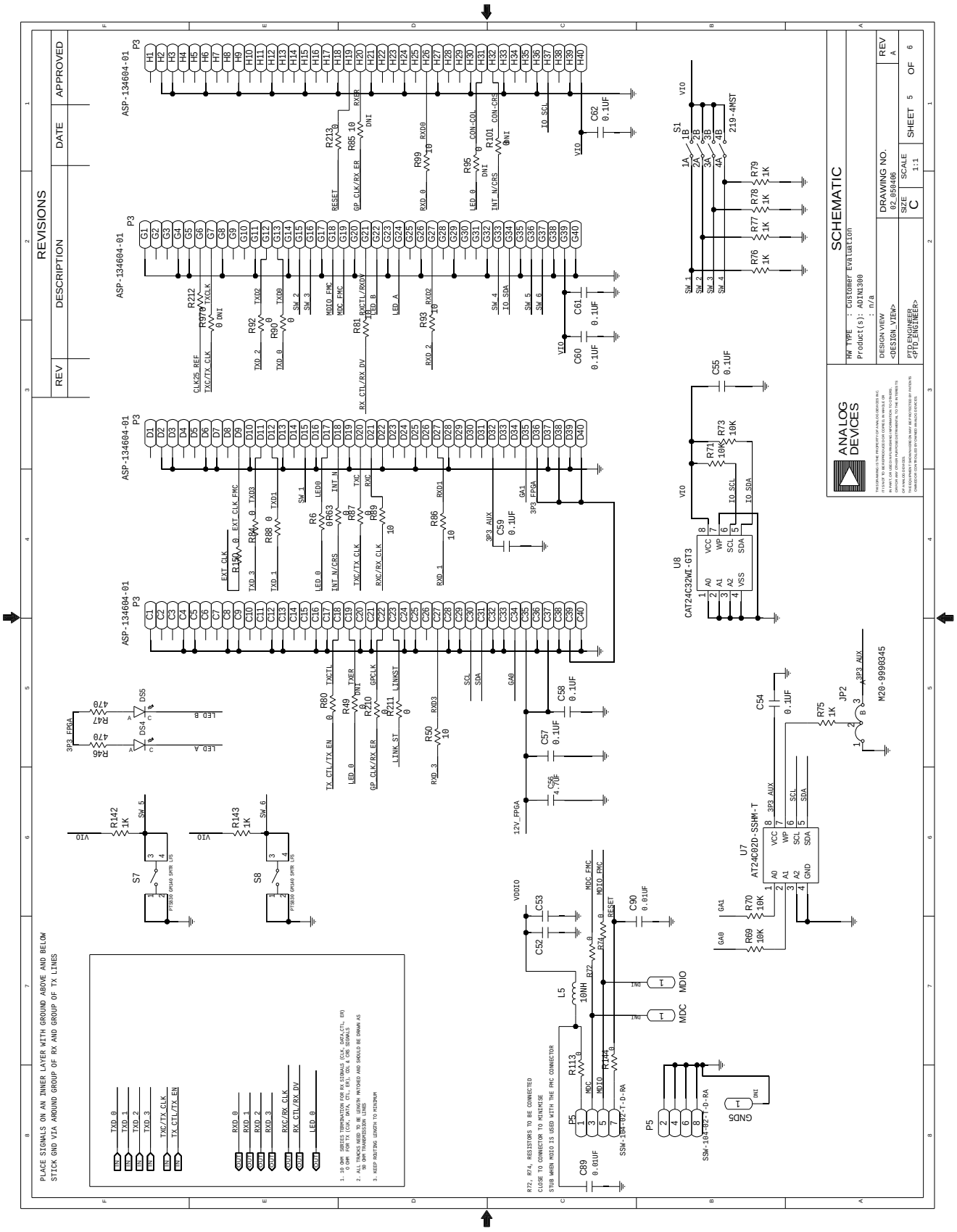

Figure 53. Rev B Schematic – Page 4

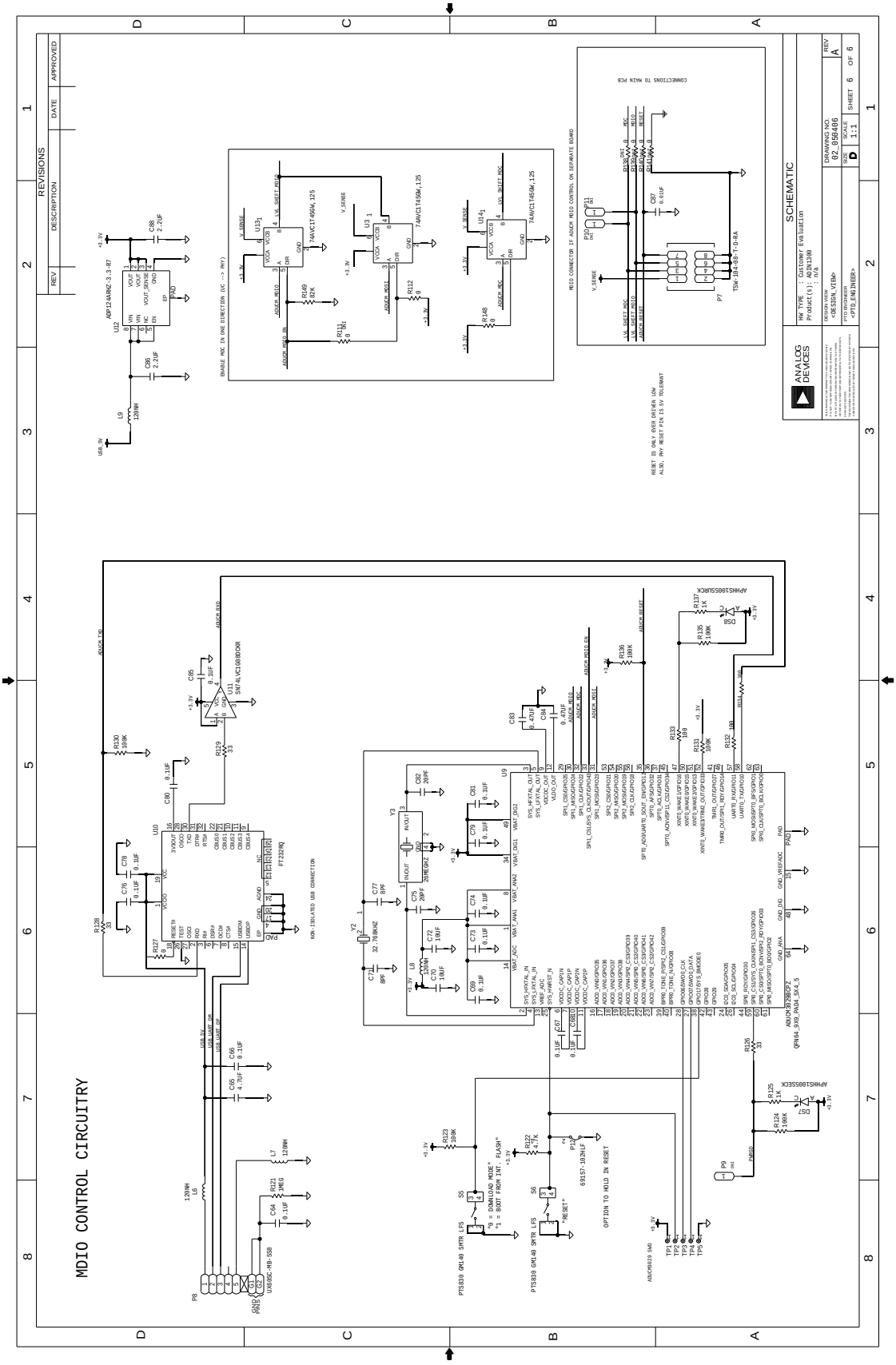

Figure 54. Rev B Schematic – Page 5

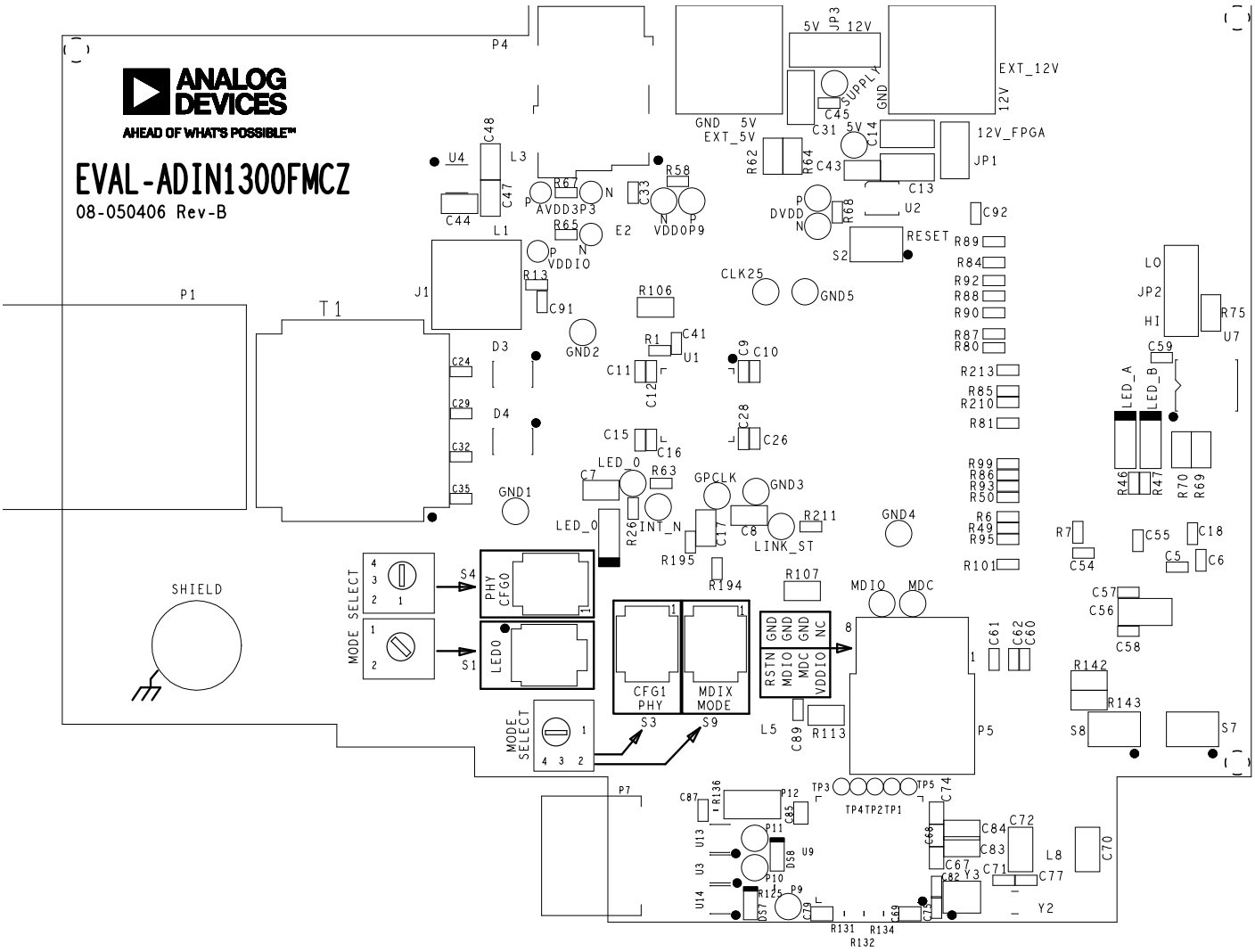

Figure 55. Rev B Schematic Silkscreen Top

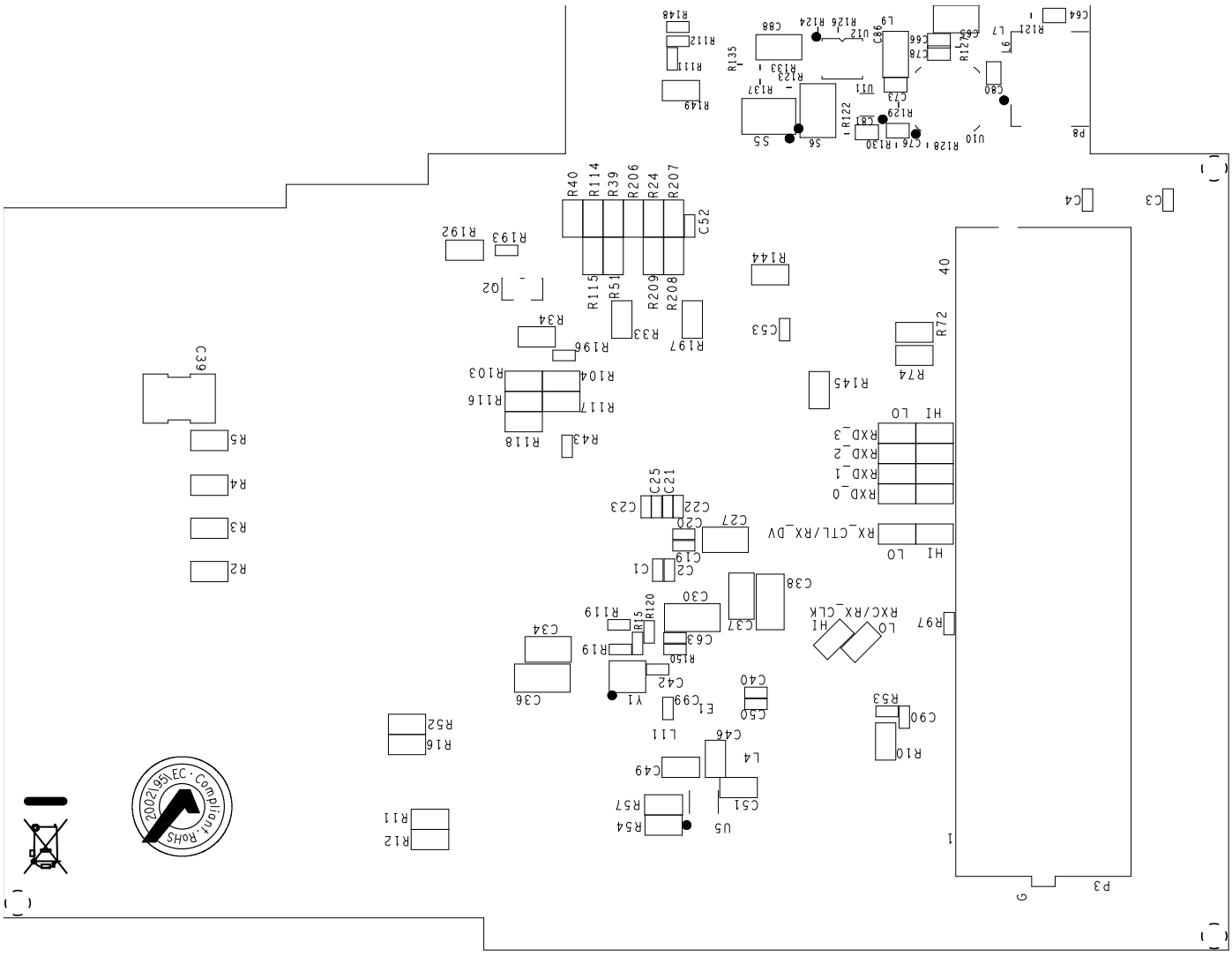

Figure 56. Rev B Schematic Silkscreen Bottom

ORDERING INFORMATION

BILL OF MATERIALS

Table 6.

Quantity	Reference Designator	Description	Part Number	Supplier
16	C1,C10,C11,C15,C19,C21,C23,C26,C54,C55,C57,C58,C59,C60,C61,C62	0.1uF, 16V, 10% C0402, CER X7R	530L104KT16T	AMERICAN TECHNICAL CERAMICS
16	C2,C9,C12,C16,C20,C22,C25,C28,C40,C50,C52,C53,C63,C87,C89,C90	0.01uF, 25V, 10% C0402, CER X7R	C1005X7R1E103K050EB	TDK
7	C13,C14,C30,C31,C36,C38,C56	4.7uF, 25V, 10% C1206, CER X7R	C1206C475K3RACTU	KEMET
4	C24,C29,C32,C35	0.1uF, 50V, 10% C0402, CER X7R	C1005X7R1H104K050BE	TDK
3	C27,C34,C37	1uF, 100V, 10% C0805, CER X7R	C2012X7S2A105K	TDK
1	C39	0.001uF, 3000V, 10% C1812, CER X7R	C1812C102KHRACTU	KEMET
2	C41,C42	16pF, 50V, 2% C0402, CER COG	GJM1555C1H160GB01D	MURATA
7	C43,C44,C46,C47,C48,C49,C51	4.7uF, 10V, 10% C0603, CER X6S	GRM185C81A475KE11D	MURATA
13	C64,C66,C67,C68,C69,C73,C74,C76,C78,C79,C80,C81,C85	0.1uF, 50V, 10% C0402, CER X7R	CGA2B3X7R1H104K050BB	TDK
1	C65	4.7uF, 50V, 10% C0805, CER X7R	GRM21BZ71H475KE15L	MURATA
2	C70,C72	10uF, 25V, 10% C0805, CER X5R	C2012X5R1E106K085AC	TDK
2	C71,C77	8pF, 16V, +/-0.5pF, C0402, CER C0G	0402YA8R0DAT2A	AVX CORPORATION
2	C75,C82	20pF, 16V, 5%, C0402, CER X7R	0402YA200JAT2A	AVX CORPORATION
2	C83,C84	0.47uF, 35V, 10%, C0603, CER X7R	GMK107B7474KAHT	TAIYO YUDEN
2	C86,C88	2.2uF, 50V, 10%, C0805, CER X7R	UMK212BB7225KG-T	TAIYO YUDEN
2	D3,D4	DIO TVS ARRAYS, LOW CAP ESD PROTECTION, SOT23_6	SP0504SHTG	LITTELFUSE, INC.
3	DS1,DS4,DS5	LED RED CLEAR, 660NM WAVELENGTH PEAK, 0805	SML-LX0805SRC-TR	LUMEX INC.
1	DS7	LED UNI-COLOR ORANGE, 610NM, 0402	APHHS1005SECK	KINGBRIGHT ELECTRONIC
1	DS8	LED HYPER RED SMD, 0402	APHHS1005SURCK	KINGBRIGHT
2	E1,E2	IND FERRITE BEAD 1K OHM 0805	BK2125HS102-T	TAIYO YUDEN
1	EXT_5V	CONN-PCB HEADER RT 3.81MM	1803277	PHOENIX CONTACT
1	JP1	CONN-PCB BERG JMPR ST MALE 2P, 1X M000385	69157-102HLF	AMPHENOL FCI
2	JP2,JP3	CONN-PCB 3POS MALE HDR UNSHROUDED SINGLE ROW, 2.54MM PITCH, 3MM SOLDER TAIL	M20-9990345	HARWIN
5	L1,L3,L4,L5,L11	IND HI FREQ WIREWOUND, 10nH, 0603	LQW18AN10NG10D	MURATA MANUFACTURING
4	L6,L7,L8,L9	IND SM, 120nH, 0805	BLM21BB750SN1B	MURATA MANUFACTURING
1	P1	CONN-PCB MODULAR JASCK ASSEMBLY, SINGLE PORT, O POS, SHIELDED	5406299-1	TE CONNECTIVITY
1	P12	CONN-PCB BERG JMPR ST MALE 2P	69157-102HLF	AMPHENOL FCI

Quantity	Reference Designator	Description	Part Number	Supplier
1	P3	CONN-PCB SGNL-END ARRAY MALE 160POS	ASP-134604-01	SAMTEC
1	P4	CONN-PCB POWER JACK	PJ-002AH-SMT-TR	CUI
1	P5	CONN-PCB 8POS SOCKET STRIP DOUBLE ROW RA, 2.54MM PITCH 2.54MM SOLDER TAIL	SSW-104-02-T-D-RA	SAMTEC INC.
1	P7	CONN-PCB HDR RA MALE	TSW-104-08-T-D-RA	SAMTEC
1	P8	CONN-PCB RCPT MINI USB2.0, SHELL TH	UX60SC-MB-5S8	HIROSE ELECTRIC
1	Q2	TRAN NPN GEN PURPOSE, SOT23	BC817	NXP SEMICONDUCTORS
1	R1	3.01k, 1%, 1/10W, 0402, RES PRECISION THICK FILM CHIP	ERJ-2RKF3011X	PANASONIC
1	R10	100k, 1%, 1/10W, 0603, RES THICK FILM CHIP	CR0603-FX-1003ELF	BOURNS
6	R39,R103,R115,R117,R207,R209	56k, 1%, 1/16W, 0603, RES FILM SMD 0603	MC 0.063W 0603 1% 56K.	MULTICOMP (SPC)
16	R24,R33,R34,R40,R51,R69,R70,R71,R73,R104,R114,R116,R118,R197,R206,R208	10k, 1%, 1/16W, 0603, RES THICK FILM CHIP	MC0063W0603110K	MULTICOMP (SPC)
8	R75,R76,R77,R78,R79,R106,R142,R143	1k, 1%, 1/16W, 0603, RES THICK FILM CHIP	MC0063W060311K	MULTICOMP (SPC)
2	R107,R145	1.5k, 1%, 1/16W, 0603, RES THICK FILM CHIP	MC 0.063W 0603 1% 1K5	MULTICOMP (SPC)
2	R11,R62	280k, 0.1%, 1/10W, 0603,RES METAL FILM HIGH REL	ERA-3AEB2803V	PANASONIC
27	R6,R15,R26,R53,R58,R63,R65,R67,R68,R80,R84,R87,R88,R90,R92,R112,R119,R148,R150,R191,R194,R195,R196,R210,R211,R212,R213	0R, 1%, 1/16W, 0402,RES THICK FILM CHIP	MC00625W040210R	MULTICOMP (SPC)
4	R72,R74,R113,R144	0R, 1%, 1/16W, 0603,RES THICK FILM CHIP	MC0603WG00000T5E-TC	MULTICOMP (SPC)
4	R12,R52,R54,R64	50k, 0.1%, 0.15W, 0603,RES METAL FILM	PNM0603E5002BST5	VISHAY
1	R121	1M, 1%, 1/20W, 0201,RES PRECISION THICK FILM CHIP	ERJ-1GNF1004C	PANASONIC
1	R122	4.7k, 1%, 1/20W, 0201, RES Precision Thick Film	MC0201L6F4701SE	MULTICOMP (SPC)
6	R123,R124,R130,R131,R135,R136	100k, 1%, 1/20W, 0201,RES PRECISION THICK FILM CHIP	ERJ-1GNF1003C	PANASONIC
2	R125,R137	1k, 1%, 1/20W, 0201,RES PRECISION THICK FILM CHIP	ERJ-1GNF1001C	PANASONIC
3	R126,R128,R129	33R, 1%, 1/20W, 0201RES PREC THICK FILM CHIP	ERJ-1GNF33R0C	PANASONIC
1	R127	0R, 5%, 1/20W, 0201,RES THICK FILM CHIP	CR0201-J/-000GLF	BOURNS
3	R132,R133,R134	100R, 1%, 1/20W, 0201, RES PREC THICK FILM CHIP	ERJ-1GNF1000C	PANASONIC
1	R149	82k, 1%, 1/16W, 0603, RES FILM	MC 0.063W 0603 1% 82K.	MULTICOMP (SPC)
1	R16	200k, 1%, 1/10W, 0603, RES PRECISION THICK FILM CHIP	ERJ-3EKF2003V	PANASONIC
1	R192	100k, 1%, 1/10W, 0603, RES GEN PURPOSE CHIP	RC0603JR-07100KL	YAGEO

Quantity	Reference Designator	Description	Part Number	Supplier
1	R193	10k, 1%, 1/10W, 0402, RES PRECISION THICK FILM CHIP	ERJ-2RKF1002X	PANASONIC
4	R2,R3,R4,R5	75R, 1%, 1/10W, 0603, RES PRECISION THICK FILM CHIP R0603	ERJ-3EKF75R0V	PANASONIC
1	R43	390R, 5%, 1/16W, 0402, RES FILM SMD	ERJ-2GEJ391X	PANASONIC
2	R46,R47	470R, 1%, 1/16W, 0402, RES GEN PURPOSE CHIP	RC0402FR-07470RL	YAGEO
1	R48	0R, 1W, 500V, 2512, RES THICK FILM CHIP 2512	CRCW25120000Z0EG	VISHAY
6	R50,R81,R86,R89,R93,R99	10R, 1%, 1/16W, 0402, RES THICK FILM CHIP	MC00625W0402110R	MULTICOMP (SPC)
1	R57	40k, 0.1%, 0.15W, 0603, RES PREC THIN FILM CHIP	PAT0603E4002BST1	VISHAY
1	S1	SWITCH 4 POS SMT	219-4MST	CTS
5	S2,S5,S6,S7,S8	SW TACTILE, MICROMINIATURE TOP ACTUATED, SPST-NO	PTS830 GM140 SMTR LFS	C&K
3	S3,S4,S9	SW ROTARY SP4T J-HOOK LEAD	CS-4-14NA	NIDEC COPAL ELECTRONICS
1	T1	XFMR 1000BASE-T MAGNETIC MODULES	H5007NL	PULSE ELECTRONICS
1	U1	IC-ADI ROBUST, LOW LATENCY 10/11/1000 GIGABIT ETHERNET PHY, PRELIM	ADIN1300	ANALOG DEVICES
1	U10	IC USB SERIAL UART, FT232RQ	FT232RQ	FTDI CHIP
1	U11	IC-TTL SINGLE POSITIVE AND GATE, SC70-5	SN74LVC1G08DCKR	TEXAS INSTRUMENTS
1	U12	IC-ADI CMOS LOW QUIESCENT CURRENT	ADP124ARHZ-3.3-R7	ANALOG DEVICES
3	U3,U13,U14	IC-TTL DUAL SUPPLY TRANSCEIVER, 3 STATE	74AVC1T45GW,125	NXP SEMICONDUCTORS
1	U2	IC-ADI 500mA, LOW NOISE LDO REG WITH SOFT START	ADP7105ACPZ-5.0-R7	ANALOG DEVICES
2	U4,U5	IC-ADI ADJ HI PSRR VOLTAGE REGULATOR	ADP223ACPZ-R7	ANALOG DEVICES
1	U7	IC I2C COMPATIBLE SERIAL EEPROM 2KBIT	AT24C02D-SSHM-T	ATMEL
1	U8	IC-CMOS I2C SERIAL EEPROM, 32KB	CAT24C32WI-GT3	ONSEMI
1	U9	IC-ADI ULTRA LOW PWR ARM CORTEX-M3 MCU	ADUCM3029BCPZ	ANALOG DEVICES
1	Y1	25.000MHz CRYSTAL, 10PPM, 10PF LOAD CAP	FA-128_25.000000MHZ_10.0_+10-10	SEIKO EPSON
1	Y2	32.768kHz CRYSTAL TUNING FORK, 20PPM, 6PF LOAD CAP	ABS07-120-32.768KHZ-T	ABRACON CORP.
1	Y2	32.768kHz CRYSTAL TUNING FORK, 20PPM, 6PF LOAD CAP	ABS07-120-32.768KHZ-T	ABRACON CORP.
1	Y3	26MHz CRYSTAL, 30PPM 10PF LOAD CAP	ECS-260-10-36Q-ES-TR	ECS, INC.
The following components are part of the PCB but are NOT populated:				
26	5V,AVDD3P3_N,AVDD3P3_P,CLK25,DVDD_N,DVDD_P,GND1,GND2,GND3,GND4,GND5,GPCLK,INT_N,LED_0,LINK_ST,MDC,MDIO,P9,	CONN-PCB MICRO PIN	1405-2	KEYSTONE ELECTRONICS

Quantity	Reference Designator	Description	Part Number	Supplier
	P10,P11,SUPPLY,VDD0P9_N,VDD0P9_P,VDDIO_N,VDDIO_P,XTAL_I			
3	C33,C45,C99	0.01uF, 10%, 25V, 0402, CAP CER X7R, COMMERCIAL GRADE	C1005X7R1E103K050EB	TDK
1	EXT_12V	CONN-PCB HEADER RT 3.81MM	1803277	PHOENIX CONTACT
1	J1	CONN-PCB STRAIGHT SMA PCB DIE CAST	5-1814832-1	TE CONNECTIVITY LTD
7	R49,R95,R97,R101,R110,R111,R120	0R, 1%, 50V, 0402, RES THICK FILM CHIP	MC00625W040210R	MULTICOMP (SPC)
4	R138,R139,R140,R141	0R, 0805, RES THIN FILM CHIP	MC 0.1W 0805 0R	MULTICOMP (SPC)
1	R19	1M, 1%, 1/10W, 0402, RES PRECISION THICK FILM CHIP	ERJ-2RKF1004X	PANASONIC
12	R8,R9,R22,R23,R27,R28,R29,R30,R31,R32,R37,R38	10k, 1%, 1/16W, 0603, RES THICK FILM CHIP	MC0063W0603110K	MULTICOMP (SPC)
1	R85	10R, 1%, 1/16W, 0402, RES THICK FILM CHIP	MC00625W0402110R	MULTICOMP (SPC)
1	SHIELD	CONN-PCB 4MM SOCKET	20054	RAPID

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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