

## Evaluating the ADIN1100 Robust, Industrial, Low Power 10BASE-T1L Ethernet PHY

### FEATURES

- Operates from a single, external 5-30 V supply or from USB**
- On-board ARM Cortex ADuCM4050 microcontroller**
- FMC connector for MII/RMII interface, MDIO signals, and status signals**
- Flexible MDIO interface options**
- Accessible hardware configuration pin switches**

### EVALUATION KIT CONTENTS

- Two EVAL-ADIN1100FMCZ evaluation boards**
- Two mini USB cables**

### EQUIPMENT NEEDED

**Power supply (choose one of the following):**

- 5-30 V power supply rail to connect to the P1 connector**
- 5-30 V barrel adaptor to connect to the P2 plug**
- USB cable**
- FPGA master supply connected via FMC connector**

**Single pair ethernet cable**

**USB cable**

**PC running Windows 7 and upward**

### SOFTWARE NEEDED

**Ethernet PHY software GUI**

**FTDI USB driver**

**Basic UART terminal**

### DOCUMENTS NEEDED

**ADIN1100 data sheet**

### GENERAL DESCRIPTION

The EVAL-ADIN1100FMCZ allows simplified evaluation of the key features of the ADIN1100 robust, industrial, low power 10BASE-T1L Ethernet physical layer (PHY). The EVAL-ADIN1100FMCZ is powered by a single, external, 5-30 V BOARD\_PWR supply rail that can be supplied either via the P1 connector or via the P2 plug. Alternatively the board can be powered from USB via the P5 connector or from the 12V FMC supply. The supply of choice is selected via the P4 link (see Figure 1).

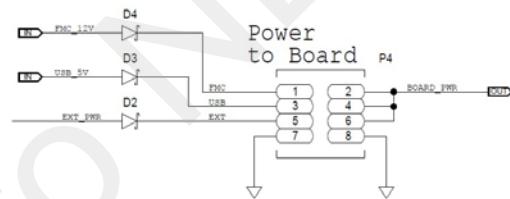


Figure 1. Schematic Snapshot – BOARD\_PWR

All ADIN1100 supplies are regulated from the BOARD\_PWR rail, providing supply rails required for AVDD\_H, AVDD\_L, VDDIO and DVDD\_1P1.

The P3 field programmable gate array (FPGA) mezzanine connector (FMC) connector is provided for connection to a master FPGA system for the media access control (MAC) interface and management data input/output (MDIO) control. The P12 connector and ADuCM4050 provide two alternative means for MDIO control. The EVAL-ADIN1100FMCZ is fitted with a 25 MHz crystal (Y3).

For complete specifications for the ADIN1100 device, see the ADIN1100 data sheet, which must be consulted in conjunction with this user guide when using the EVAL-ADIN1100FMCZ.

### Rev. PrA

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## REVISION HISTORY

05/2020—Revision PrA: Initial Internal Version

## EVAL-ADIN1100FMCZ



Figure 2. EVAL-ADIN1100FMCZ

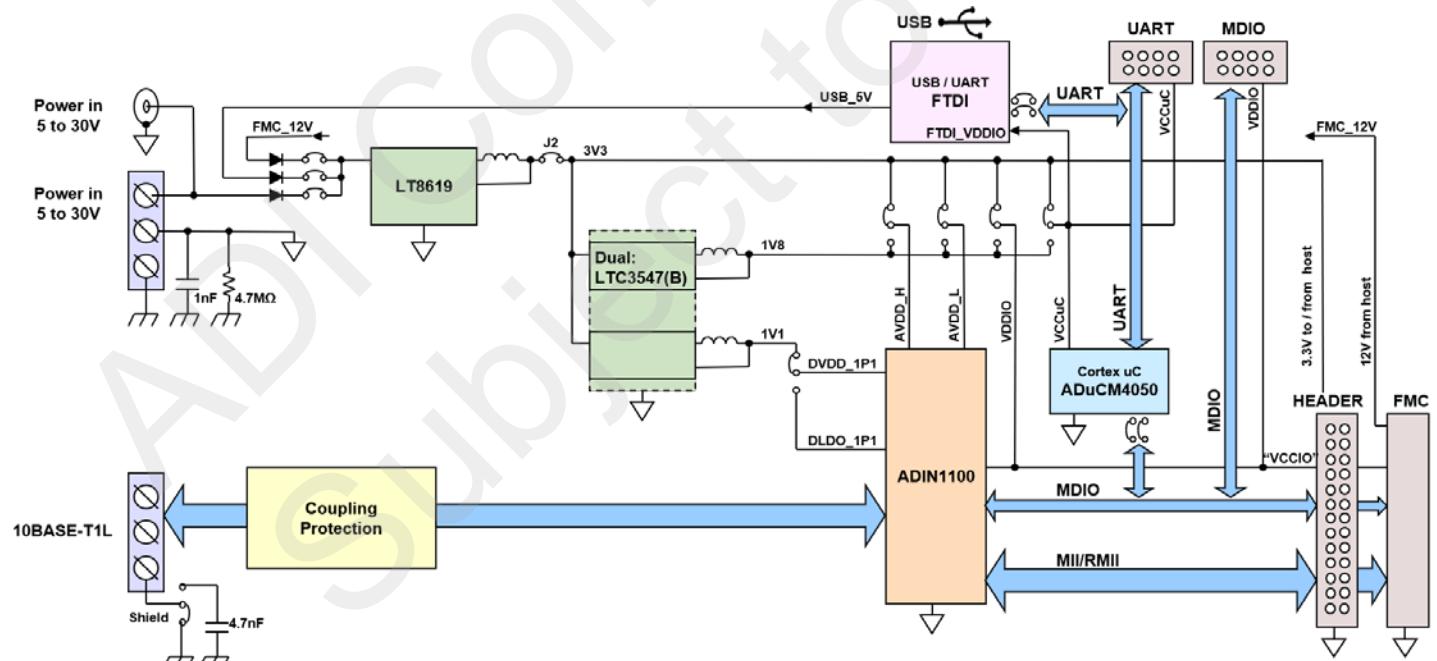


Figure 3. EVAL-ADIN1100FMCZ Functional Block Diagram

## EVALUATION BOARD HARDWARE

### POWER SUPPLIES

The EVAL-ADIN1100FMCZ is powered by a single, external, 5-30 V BOARD\_PWR supply rail that can be supplied either via the P1 connector or via the P2 plug. Alternatively the board can be powered from USB via the P5 connector or from the 12V FMC supply. The supply of choice is selected via the P4 link (see Figure 4).

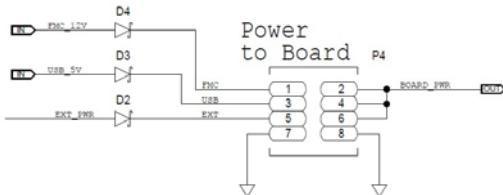


Figure 4. Schematic Snapshot – BOARD\_PWR

All ADIN1100 supplies are regulated from the BOARD\_PWR rail, providing supply rails required for AVDD\_H, AVDD\_L, VDDIO and DVDD\_1P1. The rest of the EVAL-ADIN1100FMCZ power requirements are generated from BOARD\_PWR supply. The LT8619 regulator generates a 3.3 V rail from which the LTC3547 regulator in turn generates a 1.8 V and 1.1 V rail. The ADIN1100 DVDD\_1P1 rail can be set up to use its own internally generated DLDO\_1P1 rail or the LTC3547-generated 1.1 V rail via the P17 link. AVDD\_H, AVDD\_L and VDDIO can be configured for 1.8 V or 3.3 V rail connection via the P13, P14 and P15 link respectively. Alternatively AVDD\_H, AVDD\_L and VDDIO can be shorted together via P19 & P20 and their value determined by a single link connection of P13, P14 or P15. See Figure 5.

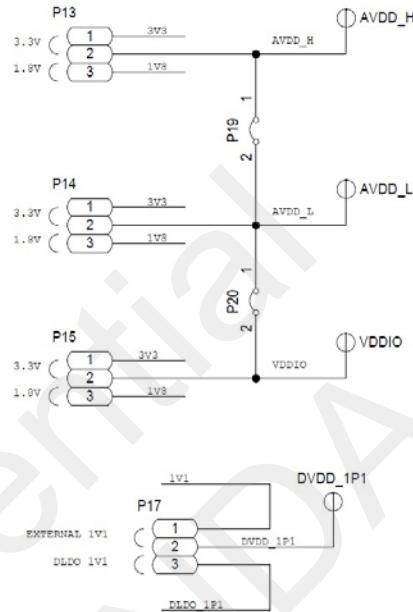


Figure 5. Schematic Snapshot – ADIN1100 Power Supply Rails

The ADuCM4050 microcontroller supply can be supplied from either the 3.3 V or 1.8 V rail (via P11 link). The FMC I/O supply (VCCIO) is connected to the ADIN1100 VDDIO supply via a 0 Ω resistor (R51). Table 1 captures the default position of all board link configurations.

Table 1. Default Board Link Configuration

Link no.	Default Position	Link Function
J101 P4	Earth EXT	Shield shorted either directly to Earth, or via 4nF cap. FMC - Connects 12V FMC supply to the input of LT8619. USB - Connects 5V USB supply to the input of the LT8619.
P10	Burst	EXT - Connects externally supplied power from P1 or P2 to the input of LT8619. FORCED CURRENT - (H) Force Continuous mode of operation of LT8619. PULSE SKIP (o/c) - Pulse-Skipping mode of operation of LT8619. BURST (L) - Burst mode of operation of LT8619.
J2 P11	Inserted 3V3	This link supplies 3.3V rail to circuitry on the board, beyond the LT8619. ADuCM4050 supply voltage – choice of 3.3V or 1.8V.
P13 P14 P15	3V3	AVDD_H supply voltage – choice of 3.3V or 1.8V. AVDD_L supply voltage – choice of 3.3V or 1.8V. VDDIO supply voltage – choice of 3.3V or 1.8V.
P17	DVDD_1P1	DVDD_1P1 supply voltage – choice of EXT 1V1 rail or internally generated DLDO_1P1 (silkscreen label "DVDD_1P1")
P19 P20	Not inserted Not inserted	Option to short AVDD_H to AVDD_L. Option to short AVDD_L to VDDIO.
P8	PHY RESET	Option to hold ADuCM4050 in reset (GND RESET) or short it to the PHY RESET_N (PHY RESET).

Table 2 shows an overview of the EVAL-ADIN1100FMCZ supply rail current for various operating modes.

**Table 2. EVAL-ADIN1100FMCZ Quiescent Current  
(External Supply Rail = 24V)**

Board Status	Typical Quiescent Current
ADIN1100 & ADuCM4050 held in hardware reset. (P8 @ GND RESET & RESET_N held low via S5)	1 mA
On power-up (ADIN1100 & ADuCM4050 not held in reset)	11 mA

## POWER SEQUENCING

There is no particular power sequence required for the ADIN1100 device.

When using the EVAL-ADIN1100FMCZ with the GUI via the USB interface, if issues are observed, restart the GUI software to resolve any board connection issues.

## HARDWARE CONFIGURATION PINS SETUP

The ADIN1100 hardware configuration pin settings can be changed by manipulating S1 and S2 switch settings found on the right-hand-side of the EVAL-ADIN1100FMCZ board (highlighted in Figure 6). Table 3 lists the default switch configuration settings on the board. When the switch is OFF, the hardware configuration pin is pulled low via an internal pulldown resistor and when the switch is ON, the pin is pulled high via an external 4.7 kΩ pull-up resistor.



Figure 6. Hardware Configuration Pins Switches Location.

**Table 3. Default Switch Position**

Switch/ Pin no.	Default Position	Default Switch Position Function
S1/Pin1	OFF	TX2P4_ENB – 1 Vpk-pk/2.4 Vpk-pk transmit amplitude mode
S1/Pin2	OFF	MS_SEL – Prefer slave selection
S1/Pin3	ON	SWPD_ENB – ADIN1100 <u>not</u> in SWPD
S1/Pin4	OFF	MEDIA_CNV – Disable Media Converter mode
S2/Pin1	OFF	PHYAD_0 – PHY H/W Address 0x0
S2/Pin2	OFF	PHYAD_1 – PHY H/W Address 0x0
S2/Pin3	OFF	PHYAD_2 – PHY H/W Address 0x0
S2/Pin4	ON	MACIF_SEL0 – MII interface selected
S2/Pin5	ON	MACIF_SEL1 – MII interface selected

## ON-BOARD ADUCM4050 MICROCONTROLLER

The EVAL-ADIN1100FMCZ has an on-board ADuCM4050 which can be used to read/write to the ADIN1100 PHY over the MDIO interface using the USB connection. This allows interaction with the ADIN1100 device via the Ethernet PHY software GUI running on the PC.

### ADuCM4050 Configuration Switches

The ADuCM4050 has 4 associated configuration switches which are pulled low when the switch is in the ON position and pulled high when in the OFF position (Figure 7). By default, all four configuration pins are pulled low.

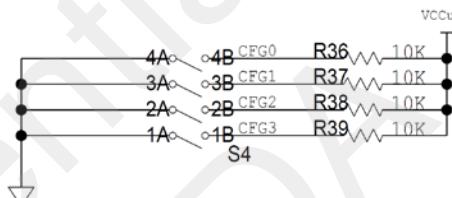


Figure 7. ADuCM4050 Config Switches

**Table 4. Default Switch Position**

Switch/ Pin no.	Default Position	Default Switch Position Function
S4/Pin1	ON (1)	CFG3 – ADuCM4050 Config pin 3
S4/Pin2	ON (1)	CFG2 – ADuCM4050 Config pin 2
S4/Pin3	ON (1)	CFG1 – ADuCM4050 Config pin 1
S4/Pin4	ON (1)	CFG0 – ADuCM4050 Config pin 0

**Table 5. ADuCM4050 Config Switch Modes**

CFG[3:0] <sup>1</sup>	Operating Mode <sup>2</sup>
0000	Not defined <sup>3</sup>
0001	Not defined <sup>3</sup>
0010	Not defined <sup>3</sup>
0011	Not defined <sup>3</sup>
0100	Not defined <sup>3</sup>
0101	Not defined <sup>3</sup>
0110	Not defined <sup>3</sup>
0111	Enable LED & continuously report MSE value to UART if link is present.
1000	Not defined <sup>3</sup>
1001	Not defined <sup>3</sup>
1010	Not defined <sup>3</sup>
1011	Not defined <sup>3</sup>
1100	Not defined <sup>3</sup>
1101	Not defined <sup>3</sup>
1110	Not defined <sup>3</sup>
1111	Search for the PHY, enable & configure LED to blink rate 0x3636, use GUI to interface with ADIN1100.

<sup>1</sup> 0 means switch is OFF (i.e. pin is pulled high), 1 means switch is ON (i.e. pin is pulled low).

<sup>2</sup> The UART terminal or GUI can be used to interact with the board for all of the ADuCM4050 configuration switch settings.

<sup>3</sup> "Not defined" means that the ADuCM4050 makes no autonomous attempt to interact with the ADIN1100 PHY.

### ADuCM4050 MSE Result

The Mean Square Error (MSE) result returned when the ADuCM4050 switches are configured CFG[3:0] = [OFF, ON, ON, ON] indicates link quality. It is in fact the reciprocal of SNR. To meet the 1e-9 Bit Error Rate (BER) mandated by the IEEE802.3cg Standard (clause 146.5.5.1), an SNR of 20.05dB (i.e. MSE of -20.05dB) is required. So a result equal to, or below -20dB is considered compliant with the Standard.

As listed in Table 5, when CFG[3:0] = [OFF, ON, ON, ON], the MSE value of the link is continuously written to the UART and can be read using Termite RS232 terminal (or equivalent) software (assuming there is a valid link in place between two link partners).

### ADuCM4050 LEDs

There are two LEDs associated with the ADuCM4050 – labelled “uC1” and “uC2”. When the ADuCM4050 has been programmed and is ready for use, the orange uC2 led flashes once. The red LED turns on if a fault occurs and blinks once upon programming the ADuCM4050, or power-on or hardware reset.

### ADIN1100 LED PIN

There is one LED pin (labelled “LED”) on the ADIN1100. The LED pin can be configured in various operating modes via the MDIO interface (see the ADIN1100 data sheet).

On first silicon, by default, the LED pin is disabled (this will be enabled by default on the next revision of silicon). However, the ADuCM4050 has been programmed to enable the LED and cause it to illuminate when a link is established, and flash when there is activity. These LED configuration commands are written to the ADIN1100 in one of two configurations – when all four ADuCM4050 configuration pins (silkscreen label “CONFIG 0-3”) are ON (i.e. tied low) and when CONFIG-3 is OFF and CONFIG-[2:0] are all ON – see Table 5.

Note that if an action performed by the GUI causes the PHY to reset without the ADuCM4050 re-enabling the LED, a pre-loaded script can be run using the GUI in order to re-issue the commands to re-enable the LED. See the Loading a Script File section. Performing a hardware reset using the S5 button on the board will also cause the LED to be re-enabled, assuming one of the two previously mentioned configurations of the “CONFIG 0-3” switches is in place.

### MDIO INTERFACE

The MDIO interface of the ADIN1100 can be accessed in a number of ways as highlighted in Figure 8:

1. UART/USB access via the ADuCM4050.
2. FMC connector access via an FPGA host.
3. Using the 8-pin P12 header.
4. The MDIO interface signals are also accessible on the P7 header.

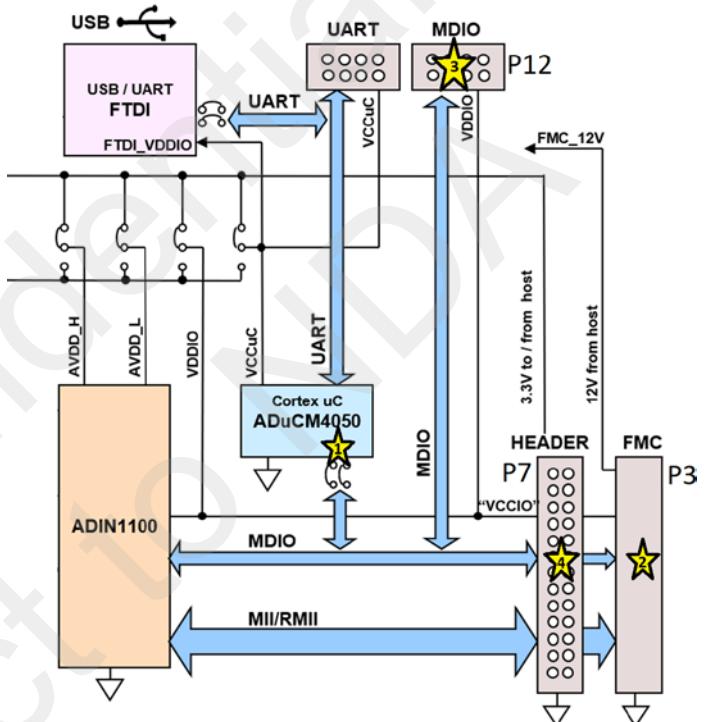


Figure 8. MDIO Interface Options

## EVALUATION BOARD USAGE OPTIONS

The EVAL-ADIN1100FMCZ can be used in two general modes. In standalone mode (Figure 9), the EVAL-ADIN1100FMCZ can be used to evaluate the ADIN1100 in IEEE 802.3 test modes, establish links with a link partner, and evaluate the performance of the chip. In standalone mode, power the EVAL-ADIN1100FMCZ with a 5-30 V supply at the P1 or P2 connector or alternatively via USB.

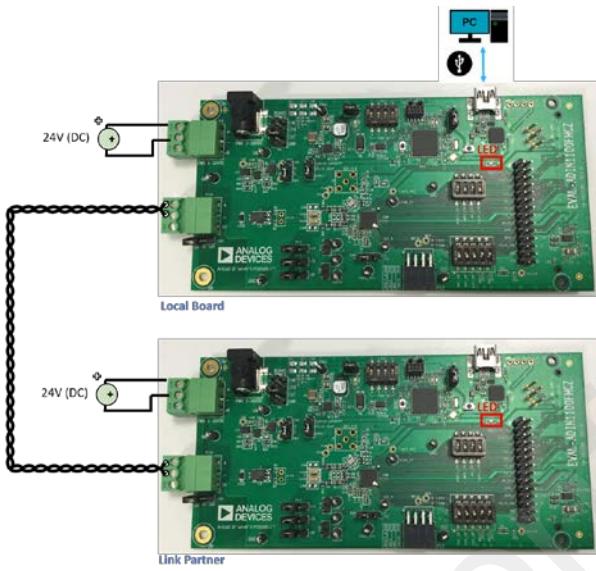


Figure 9. Image of 2 boards hooked together with cable.

Alternative to standalone mode, the EVAL-ADIN1100FMCZ has an FMC low pin count (LPC) connector, which can be plugged into an FPGA development board. When used with an FPGA board, the media independent interfaces (MII/RMII), clocks, and MDIO interface can be connected to the FPGA board where the MAC and upper layers can be implemented for evaluation of the ADIN1100 in a full system. In this case, the board can be powered from the 12 V FMC supply.

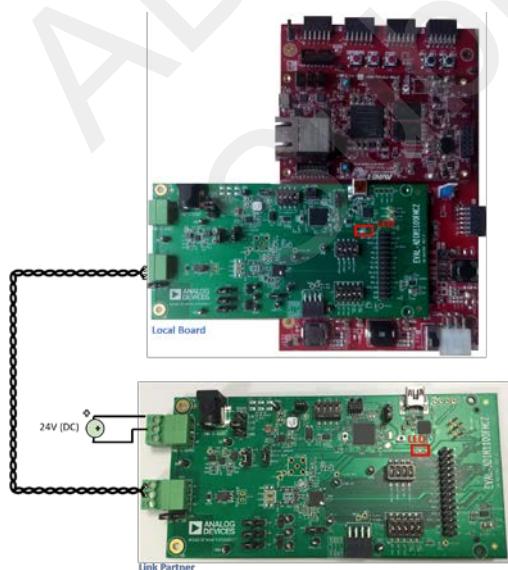


Figure 10. Image of board plugged into MAC host via FMC connector.

## CLOCK OPTIONS

The crystal oscillators on the EVAL-ADIN1100FMCZ include the following:

- Y1 is a 32.768 kHz crystal used for the on-board ADuCM4050.
- Y2 is a 26 MHz crystal used for the on-board ADuCM4050.
- Y3 is a 25 MHz crystal connected across the XTAL\_I pin and XTAL\_O pin of the ADIN1100.

As shown in Figure 11, the EVAL-ADIN1100FMCZ provides the option to supply the ADIN1100 clock requirements from either an on-board crystal oscillator (Y3), or an external clock (EXT\_CLK) applied to the J1 connector. The FMC connector provides a third alternative (RMII\_REF\_CLK) to supply the ADIN1100 clock signal.

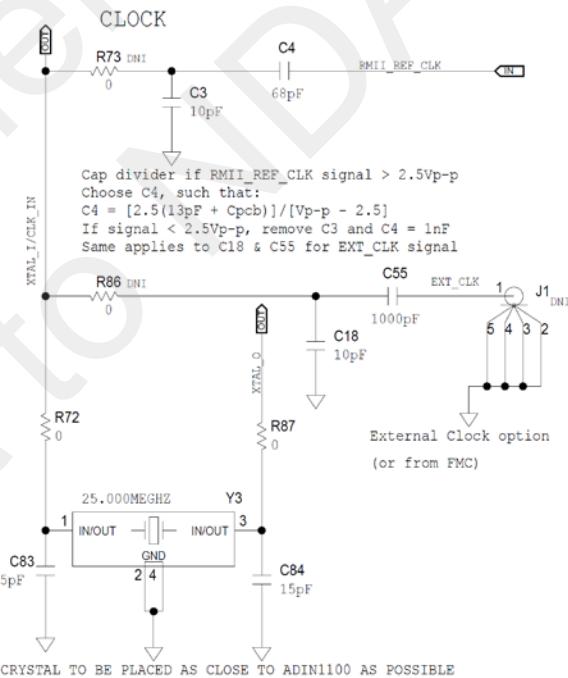


Figure 11. Schematic snapshot – clocking options

When a 25 MHz external clock is applied to the J1 connector, the R86 resistor must be populated and the R72 and R87 resistors must be removed to disconnect the Y1 crystal. The 25 MHz clock must be a sine or square wave signal with an input range of 0.8 Vpk-pk to 2.5 Vpk-pk. See the ADIN1100 data sheet for more information.

For RMII mode, a 50 MHz clock must be used. This could be provided from the host via the FMC connector – RMII\_REF\_CLK – in which case the R73 resistor must be populated and the R72, R86 and R87 resistors removed.

In either of the cases where an external clock, other than the on-board 25 MHz crystal, is being provided to the ADIN1100, this signal must be capacitively coupled and divided down such that the maximum amplitude does not exceed 2.5 Vp-p. If the

clock signal is less than 2.5 Vpk-pk, then C18 (in the case of the J1-supplied clock) and C3 (in the case of the FMC-supplied clock) are not required and a 1 nF coupling capacitor (C55 or C4 respectively) is recommended. If the clock signal is greater than 2.5 Vpk-pk, then C3 or C18 should be 10pF and C55 or C4 chosen such that the signal does not exceed 2.5 Vpk-pk.

The ADIN1100 also provides a 25 MHz reference clock output from the crystal oscillator on the CLK25\_REF pin, which is available on the P7 header.

## RESET OPTIONS

The S5 push-button switch is used to reset both the ADIN1100 PHY and the ADuCM4050 microcontroller (P8 is by default in the “PHY RESET” position – see Figure 12). Alternatively, the RESET\_N signal can be driven from the FMC connector (not shown in Figure 12). A third way to reset the PHY is from the ADuCM4050 output (signal name = uC\_to\_PHY\_RESET). In this case P8 should be left unconnected, such that the ADuCM4050 uC\_to\_PHY\_RESET signal does not also drive the RESET\_uC\_N signal to reset the ADuCM4050 itself. The P8 link also facilitates the option to hold the ADuCM4050 in reset using the “GND RESET” position.

### BOARD RESET



Figure 12. EVAL-ADIN1100FMCZ reset options.

## ON-BOARD EEPROMS

The EVAL-ADIN1100FMCZ has one unprogrammed, I<sup>2</sup>C EEPROM, U7 – labelled “FMC EEPROM”. U7 can be programmed with voltage settings to allow the FPGA board to provide the correct voltages on the supply rails. The write address of the EEPROM is 0b[10100 [GA1] [GA0] 0] and the read address is 0b[10100 [GA1] [GA0] 1].

The EVAL-ADIN1100FMCZ also has an SPI EEPROM, U6, which could be used to store the board type, revision and unique ID but as yet, is unprogrammed.

## PROGRAMMING THE ADUCM4050

The ADuCM4050 is programmed out-of-the box, so unless a new hex file is being downloaded to the ADuCM4050, it is not necessary to program it in order to use the EVAL-ADIN1100FMCZ evaluation board. The default behavior of the configuration switches based on the pre-loaded hex file is listed in Table 5.

In order to program the ADuCM4050, use the following steps:

1. Ensure the mini USB cable is connected between the EVAL-ADIN1100FMCZ board and the PC and open the CrossCore serial flash programmer software.

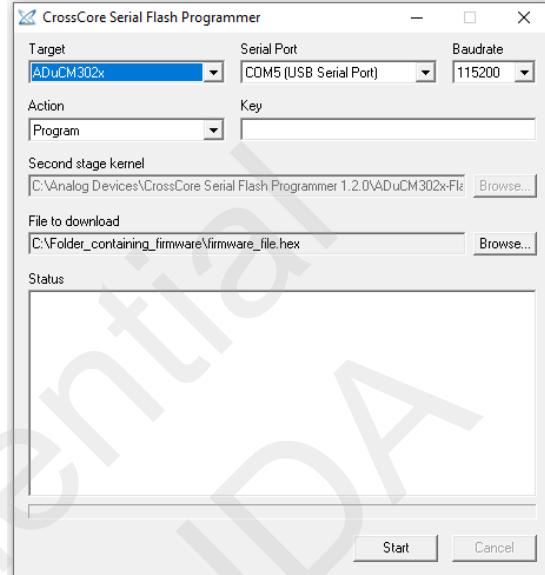


Figure 13. CrossCore Serial Flash Programmer.

2. Set the CrossCore Serial Flash programmer according to Figure 13 (COM port may vary depending on the PC).
3. Browse to select the hex file to download.
4. On the EVAL-ADIN1100FMCZ board, simultaneously press buttons S3 (BOOT) and S5 (RESET). Hold and release the RESET button first, followed by the BOOT button. Now the ADuCM4050 microcontroller is in the programming state.
5. Click Start and the code should start to download with updates provided in the Status window and progress bar across the bottom of the window.
6. After programming, press & release RESET button (S5).

## INTERACTING WITH THE PHY USING UART TERMINAL WINDOW

To interact with the PHY using a UART terminal window such as Termite, the ADuCM4050 configuration switches (Table 5) can be in any configuration.

Launch the UART terminal window and ensure the relevant COM port is selected. Type ‘?<newline>’ to get a list of possible commands (see Figure 14). Typing ‘info’<newline> displays the board information of the evaluation board connected to the active COM port, while typing ‘reset’<newline> resets the ADuCM4050. The other two relevant commands in order to read/write from/to the ADIN1100 are:

- ‘mdiord\_cl45 <PhyAddr>, <RegAddress in hex>’<newline>
- ‘mdiowr\_cl45 <PhyAddr>, <RegAddress in hex>, <Data>’<newline>

where “RegAddress” is a concatenation of the ADIN1100 Device Address & Register Address per the ADIN1100 datasheet e.g. AN\_STATUS register address would be inserted as “0x07006C”.

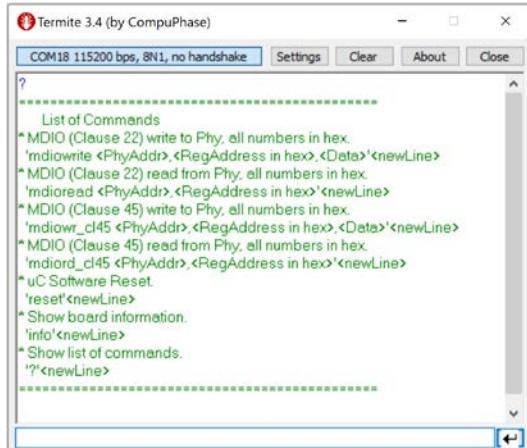


Figure 14. Termite UART Terminal Window.

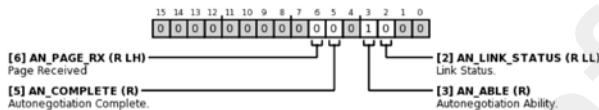


Figure 15. AN\_STATUS Register Contents.

Figure 16 example:

1. The AN\_STATUS register is initially read with a value of 0x006C, meaning that the AN\_LINK\_STATUS bit (device address 0x07, register address 0x0201, bit 2) is a 1 and a valid link is present.
2. Subsequently, the CRSM\_SFT\_PD bit (device address 0x1E, register address 0x8812, bit 0) is set to a 1 which puts the PHY on one side of the link into software power-down.

3. The next command written checks that the previous write took effect and that the CRSM\_SFT\_PD bit is indeed read back as a 1.
4. A subsequent check of the AN\_STATUS register contents reveals that the AN\_LINK\_STATUS bit is now a 0 and there is no longer a valid link present.
5. Next the CRSM\_SFT\_PD bit is cleared to 0.
6. And subsequently readback to ensure it is read as a 0.
7. Finally, the AN\_STATUS register is read once more and it can be seen that the AN\_LINK\_STATUS bit is once more a 1 and there is a valid link present.



Figure 16. AN\_STATUS Read with/without Valid Link.

## SOFTWARE OVERVIEW

### INSTALLING THE ETHERNET PHY SOFTWARE

The Ethernet PHY software GUI requires the installation of the Ethernet PHY software and the installation of the FTDI USB drivers. Both installations must be complete before connecting the EVAL-ADIN1100FMCZ to the USB port of the PC to ensure that the evaluation system is properly recognized when connected to the PC.

First, install the Ethernet PHY software and the associated documentation. The installation steps are listed in the following section. The default location for the Ethernet PHY software GUI installation is the C:\Analog Devices\ADIN1100 folder.

When the Ethernet PHY software installation is complete, install the USB communications drivers. The EVAL-ADIN1100FMCZ uses the FT232RQ for UART to USB communication and requires the installation of drivers for the FTDI chip. Locate and install this driver separately. These drivers are available at:  
[www.ftdichip.com/Drivers/CDM/CDM21228\\_Setup.zip](http://www.ftdichip.com/Drivers/CDM/CDM21228_Setup.zip).

#### Ethernet PHY Software GUI Installation

To install the Ethernet PHY software GUI, take the following steps:

1. Launch the installer file to begin the Ethernet PHY software installation.
2. If a window appears asking for permission to allow the program to make changes to the PC, click Yes.
3. The welcome window appears (see Figure 17). Click Next.



Figure 17. Welcome Window

4. The Ethernet PHY software launches. An overview of what is being installed and recommendations in terms of hardware power-up appears. Read the overview and click Next (see Figure 18).

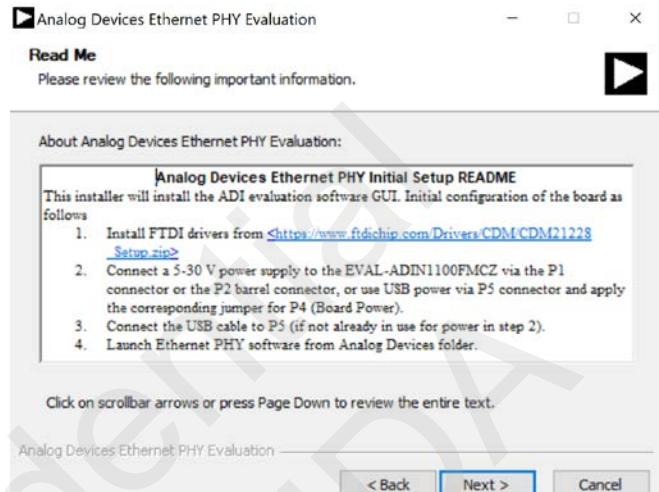


Figure 18. Installation Process Overview

5. A license agreement appears. Read the agreement and click I Agree to allow the installation to proceed (see Figure 19).



Figure 19. Accepting the License Agreement

6. Select a location to install the Ethernet PHY software and then click **Install** (see Figure 20).

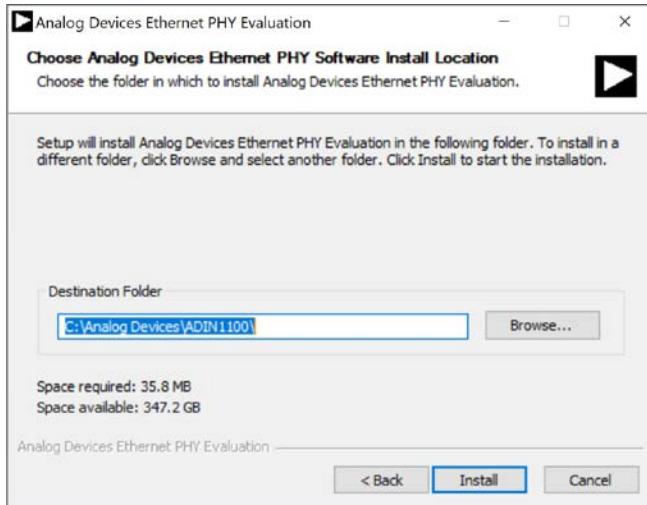


Figure 20. Installation Location

7. A window appears stating that the installation is complete. Click **Finish** to continue (see Figure 21).

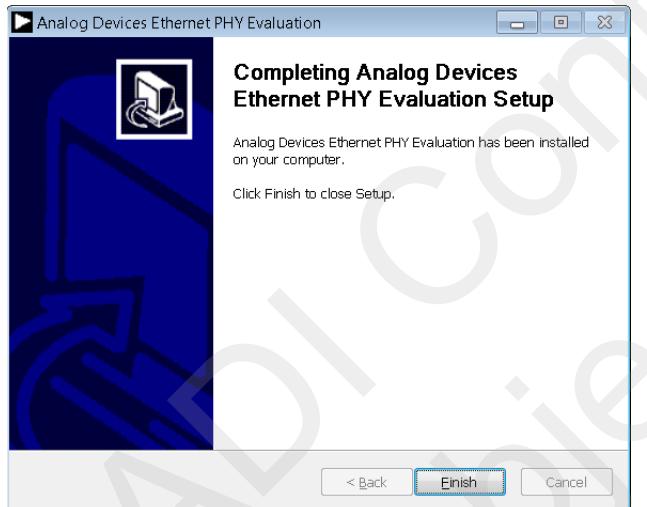


Figure 21. Installation Complete

8. The Ethernet PHY software is automatically installed in the **Analog Devices** folder on the PC. Access the Ethernet PHY software via Windows® explorer at **C:\Analog Devices\ADIN1100** or from the **Start** menu.

## INITIAL EVALUATION BOARD SETUP

To set up the EVAL-ADIN1100FMCZ and use it with the Ethernet PHY software GUI, take the following steps:

1. Connect a 5-30 V power supply to the EVAL-ADIN1100FMCZ via the P1 connector or the P2 barrel connector.
2. Connect the USB cable to P5.
3. Connect the USB cable to the PC. When connecting the EVAL-ADIN1100FMCZ to the PC for the first time, the drivers are automatically installed. Wait until the driver installation is complete before proceeding to the next step.
4. Launch the Ethernet PHY software from the **Analog Devices** folder in the **Start** menu.

## USING THE EVALUATION SOFTWARE

When the Ethernet PHY software is launched, the GUI window shown in Figure 22 appears. Figure 22 shows the GUI features with labels, and Table 6 lists the GUI labels and the corresponding descriptions.

**Table 6. GUI Label Descriptions**

Label	Description
1	<b>Select Local</b> section. Shows connected evaluation hardware. The board name shown corresponds to the EVAL-ADIN1100FMCZ.
2	User buttons.
3	<b>Link Properties</b> tab. Use this tab to change the PHY configuration.
4	<b>Register Access</b> tab. Allows the user read or write device registers. (4b) shows an option to have the Manual Register Access always on the main GUI screen by pulling the <> arrows to the left. This is not shown by default.
5	<b>Test Modes</b> tab. Provides access to the various test modes on the device.
6	<b>Frame Generator/Checker</b> tab. Configures and enables the frame generator and frame checker.
7	Board status information window. This window provides an overview of the PHY status, activity, reads, and writes issued to the selected device.
8	<b>Activity Log</b> section. Section shows read, write, and status activity for the selected PHY.
9	Dropdown menu to load a script file. This allows the user to load a script file with a sequence of write commands to load to the device.



Figure 22. Main GUI Window  
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## GUI DETAILED OVERVIEW

### BOARD DISPLAY SHOWING CONNECTED EVAL-ADIN1100FMCZ HARDWARE

In the **Select Local** section, a unique hardware identifier is shown for each EVAL-ADIN1100FMCZ board connected to the PC. In the example shown in Figure 23, there are two EVAL-ADIN1100FMCZ boards connected to the same PC (AU54KUSA and AU5F2ILS).

The Ethernet PHY software GUI can only communicate with one EVAL-ADIN1100FMCZ evaluation board at a time. To choose which evaluation board is addressed as the local board in this section, click the appropriate device identifier to select and highlight it. All register controls, displayed link properties, and local board information in other sections of the GUI apply to the selected EVAL-ADIN1100FMCZ evaluation board.

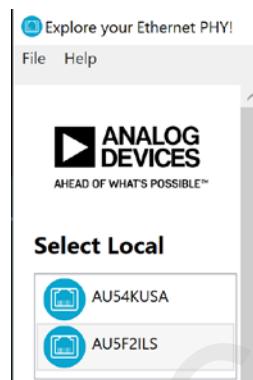


Figure 23. MDIO Interface Dongle Selection

In order to more easily identify which board is which, it is recommended to set the boards to different hardware PHY addresses using the S2 hardware configuration pin switch on the evaluation board. Figure 24 shows an overlaid snapshot of the GUI whereby one board (unique identifier AU53CSS0) is at PHY Address 7 and the other (unique identifier AU4VVV4Q) is at PHY Address 0. The PHY address is easily identifiable on the physical board connected to the PC by looking at the S2 switch configuration.



Figure 24. Recommended Method of Board Identification

### USER BUTTONS SECTION

Use the buttons in this section to control the basic operation of the GUI and the ADIN1100 device.



Figure 25. Basic User Buttons

#### Software Power-Down and Power-Up

Click **Software Power Down** to place the selected device into software power-down mode where the analog and digital circuits are placed into a low power state. Most clocks are gated off, any signal or energy on the MDI pins are ignored and no link will be brought up. The MAC Interface output pins are asserted low. The management interface registers are accessible, and the part can be configured using software. Click **Software Power Down** to enable a software power-down. The button color changes to orange and the button label changes to **Software Power Up**. Click **Software Power Up** to exit from the software power-down and restart linking. When the software power-down is asserted, the other buttons for the selected device are grey and disabled.

#### Auto-Neg Restart

If the software configuration has been changed, click **Auto-Neg Restart** to restart the linking process with the new configuration. If the link has already been established, the link is first brought down and then restarted.

#### Export Registers



Figure 26. Export Registers Dropdown Menu

Click **Export Registers** to perform a data dump to the **Activity Log** section. Note that two clicks are required – one to make your selection and a second to press the orange button to perform the action. The register dump can be saved to text format for offline review. Right click within the **Activity Log** and click **Save as** to save the data to a log file.

```

Activity Log
20:10:18 [VerboseInfo] AUS4KUSA_LED_CNTRL = 0x1 [ LED Control Register ]
20:10:18 [VerboseInfo] AUS4KUSA_LED_BLINK_TIME_CNTRL = 0x505 [ LED Blink Time Control Register ]
20:10:18 [VerboseInfo] AUS4KUSA_CRSRM_STAT = 0x5 [ CRSRM Status Register ]
20:10:18 [VerboseInfo] AUS4KUSA_CRSRM_MAC_IF_RST = 0x0 [ CRSRM PHY MAC Interface Reset Register ]
20:10:18 [VerboseInfo] AUS4KUSA_CRSRM_PHY_SUBSYS_RST = 0x0 [ CRSRM PHY Subsystem Reset Register ]
20:10:18 [VerboseInfo] AUS4KUSA_CRSRM_SFT_PD = 0x0 [ CRSRM Software Powerdown ]
20:10:18 [VerboseInfo] AUS4KUSA_CRSRM_SFT_PD_CNTRL = 0x0 [ CRSRM Software Power-Down Control Register ]
20:10:18 [VerboseInfo] AUS4KUSA_CRSRM_SFT_RST = 0x0 [ CRSRM Software Reset Register ]

```

Figure 27. Activity Log with Export Registers Displayed

## Reset

Click **Reset** to use the dropdown menu to initiate different resets. Again, like the Export Registers button, two clicks are required – one to make your selection and a second to press the orange button to perform the action. The reset options include the following:

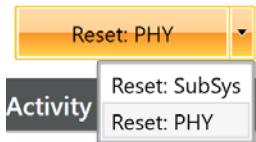


Figure 28. Reset Options

- **PHY Core Software Reset:** click **Reset: PHY** to perform a reset where the CRSRM\_SFT\_RST bit resets the PHY core registers. When this bit is set, a full initialization of the chip, almost equivalent to a hardware reset, is done. See the ADIN1100 datasheet for further details.
- **PHY Subsystem Reset:** click **Reset: SubSys** to perform a reset of the PHY subsystem. All of the PHY digital circuitry is reset and any existing link will drop. The management registers are not initialized by this reset, and access to all the management registers is available during the PHY subsystem reset. The CRSRM\_PHY\_SUBSYS\_RST bit is set to 1 to perform this reset operation.

## LINK PROPERTIES TAB

The **Link Properties** tab provides user access to the main linking configurations within the device. When a control is selected, the GUI provides a prompt describing the function at the bottom of the linking control box (see Figure 29).

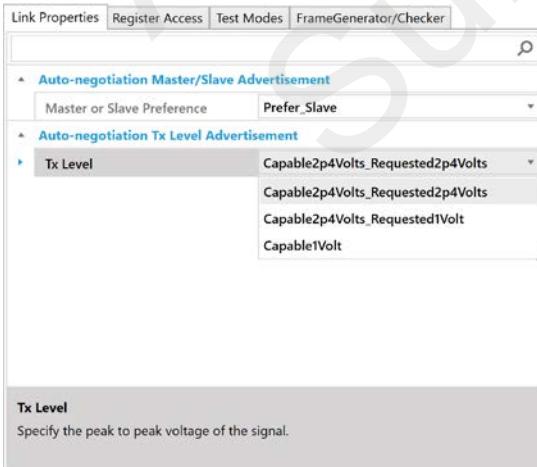


Figure 29. Link Properties Tab

## Master or Slave Preference

For the selected device, prefer master or prefer slave can be chosen. Auto-Negotiation is used to resolve master or slave status. During Auto-Negotiation, when prefer slave is selected, and the remote end is prefer or forced Master, the local PHY will be set to slave (and remote to master). When the remote end is prefer or forced slave, the local PHY will be set to master (and remote to slave).

Note, Auto-Negotiation is enabled by default for the ADIN1100 and it is strongly recommended that Auto-Negotiation is always enabled.

## Transmit Amplitude

The Tx Level drop-down can be used to configure the required transmit amplitude mode for the intended application. The ADIN1100 can be configured by default to be:

- Capable of 2.4 V pk-pk and request 2.4 V pk-pk transmit level
- Capable of 2.4 V pk-pk and request 1.0 V pk-pk transmit level
- Capable of 1.0 V pk-pk.

Auto-Negotiation will determine the transmit level that the link will operate at.

## REGISTER ACCESS TAB

The **Browse** tab within the **Register Access** tab allows the user to review the bank of registers and edit the register fields or bit fields as required (see Figure 30). Note that the Address field is a concatenation of the Device Address and Register Address as listed in the ADIN1100 datasheet.

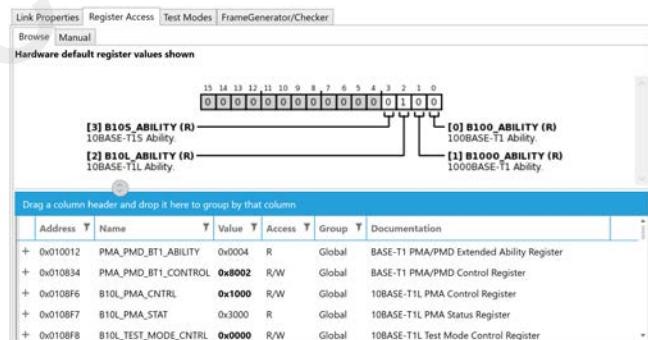


Figure 30. Register Access Tab Full Register Map

The **Manual** tab within the **Register Access** tab allows the user to perform basic reads from and writes to individual ADIN1100 registers (see Figure 31). Again, the “Address” field here is a concatenation of the Device Address and Register Address as listed in the ADIN1100 datasheet.

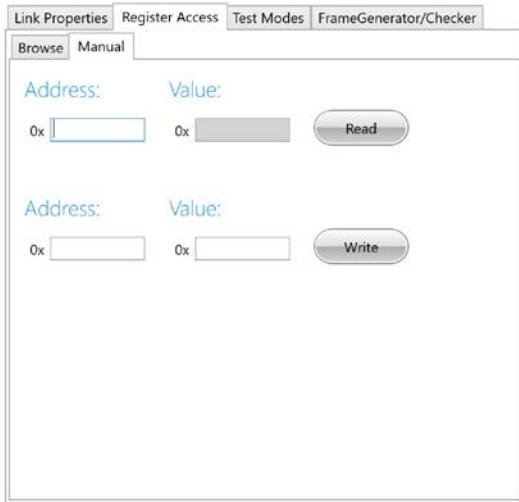


Figure 31. Register Access Tab

Access to the Manual tab of the Register Access section is also available on the right hand side of the **Activity Log** section. To access this function, slide the arrow to the left to expose it (see Figure 32).



Figure 32. Activity Log Section Register Access

## TESTMODES TAB

Use this tab to initiate the various test mode functions in the device. Select the appropriate test mode and click **Apply Mode** (see Figure 33).

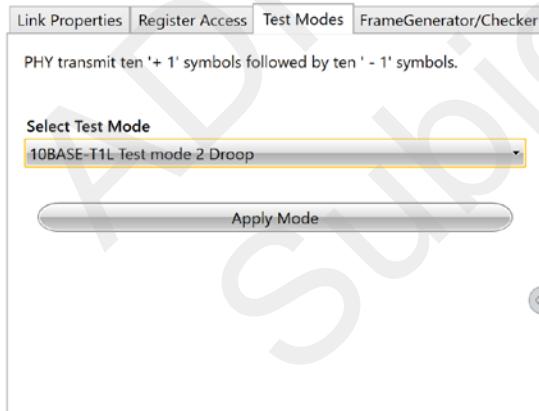


Figure 33. Test Modes Tab

## FRAME GENERATOR/CHECKER TAB

This tab provides access to the frame generator and frame checker features of the ADIN1100 (see Figure 34).

Control the number of frames generated by the generator, the frame length, and the content of the frame within this tab. Choose to have the frame generator to either run in burst mode or run continuously. To halt the frame generator when the frame

generator is running continuously, use the **Terminate** button (note that the **Generate** button becomes the **Terminate** button once the Frame Generator is active).

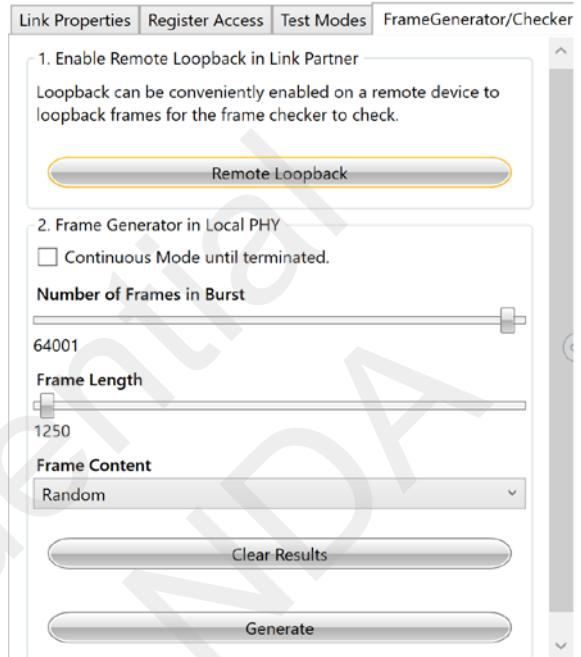


Figure 34. Overview of Frame Generator and Frame Checker

The Frame Generator can be used with & without Remote Loopback enabled.

### Using the Frame Generator with Remote Loopback enabled

Before initiating the routine, choose which connected board (under the **Select Local** section) is to be considered the “local” and “link partner” board.

1. Configure the link partner board in remote loopback using the **Remote Loopback** button (see Figure 35).
2. Enable the Frame Generator on the local board (see Figure 36) by clicking **Generate**.
3. The ADIN1100 device which generates the frames also receives frames looped by the link partner ADIN1100. The frame checker information displayed on the screen accumulates the number of frames sent and shows the number of errors observed (see Figure 37).

### Using the Frame Generator without Remote Loopback enabled

Before initiating the routine, choose which connected board (under the **Select Local** section) is to be considered the “local” and “link partner” board.

1. Enable the Frame Generator on the local board by clicking the **Generate** button.
2. Observe the frame checker information by selecting the link partner board.

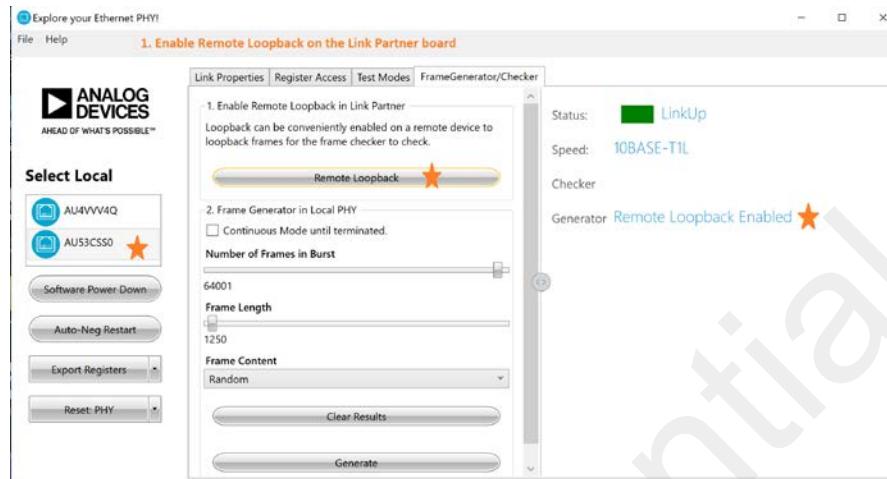


Figure 35. Frame Generator with Remote Loopback enabled – step1

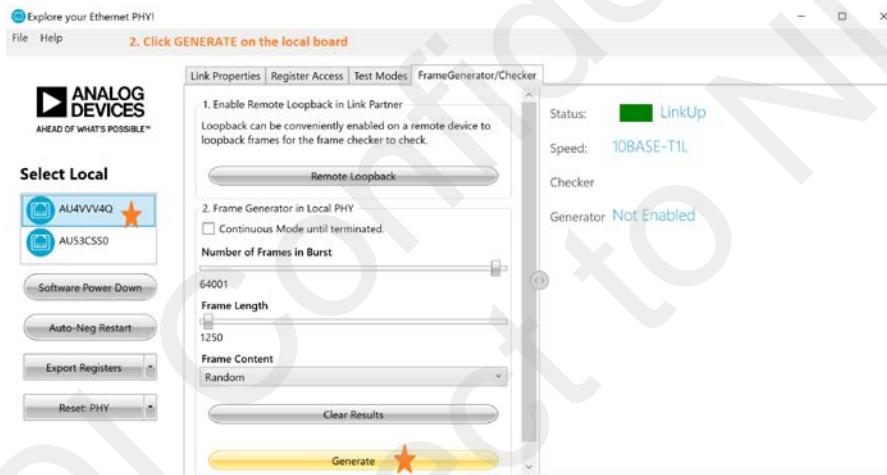


Figure 36. Frame Generator with Remote Loopback enabled – step2

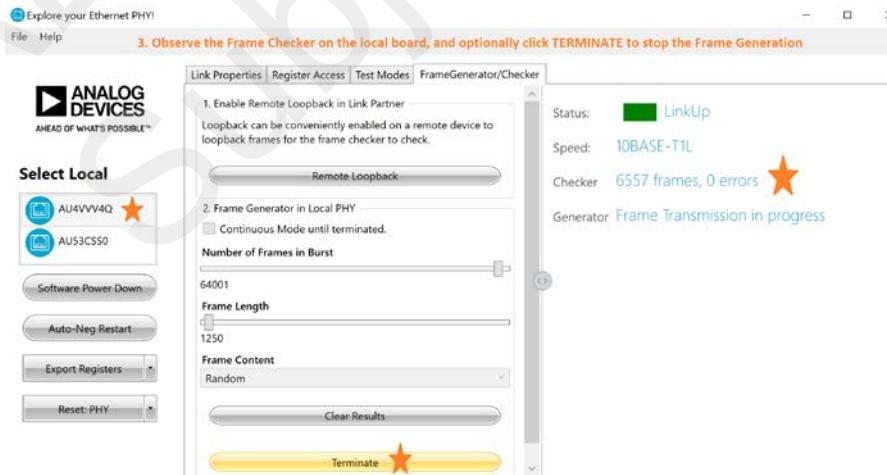


Figure 37. Frame Generator with Remote Loopback enabled – step3

## BOARD STATUS INFORMATION WINDOW

This window displays the current status of the selected PHY chip (as determined in the **Select Local** section), including whether a link is established, the speed of the link (in this case, always 10BASE-T1L), the Auto-Negotiation Status, whether the selected PHY is master or slave and the transmit voltage amplitude. If the user switches between two EVAL-ADIN1100FMCZ boards in the **Select Local** section, the information shown in these fields will be updated to reflect the information provided from the currently selected board.

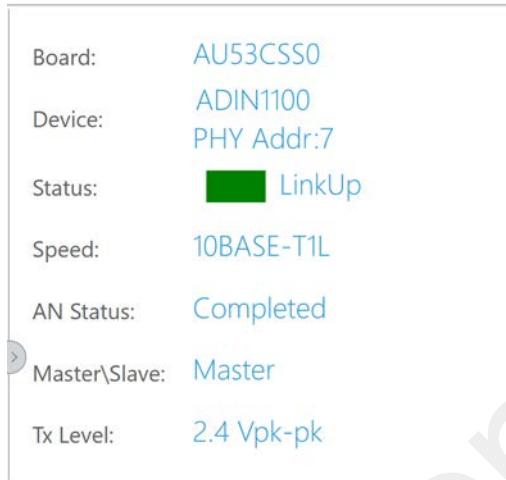


Figure 38. Board Status Information

The GUI displays a color code to show the status of the link depending on how the user has configured the device (see Figure 39).

Status:	Powerdown
Status:	Standby
Status:	LinkDown
Status:	LinkUp

Figure 39. GUI Link Status

## ACTIVITY LOG INFORMATION SECTION

The activity log reports status information and register writes issued to the selected EVAL-ADIN1100FMCZ board (see Figure 40). The activity log captures the activity in the GUI corresponding to the activity on the local PHY, which indicates the various reads, writes, and information on whether a link is established. When the frame generator is enabled, this window shows the frame generator activity. The board identification is recorded with each bit field change to clarify which device is being addressed.

### Activity Log

```

20:13:20 [Info] AU54KUSA restart auto negotiation
20:13:20 [VerboseInfo] AU54KUSA BitField "AN_RESTART" = 1
20:13:14 [Info] AU54KUSA restart auto negotiation
20:13:14 [VerboseInfo] AU54KUSA BitField "AN_RESTART" = 1
20:13:14 [VerboseInfo] AU54KUSA BitField "AN_ADV_B10L_TX_LVL_HI_REQ" = 1
20:13:13 [VerboseInfo] AU54KUSA BitField "AN_ADV_B10L_TX_LVL_HI_ABL" = 1
20:12:49 [Info] AU54KUSA restart auto negotiation
20:12:49 [VerboseInfo] AU54KUSA BitField "AN_RESTART" = 1

```

Figure 40. Activity Log Showing Device Status

To clear the activity log, right click and then click **Clear**. To export the contents of the activity log for offline review, right click and then click **Save as**. The file saved is a text file with a default location in the **Analog Devices > ADIN1100** folder.

## LOADING A SCRIPT FILE

The GUI allows the user to load a sequence of register write commands from a file. Within the GUI window, there is a dropdown menu under the **Activity Log** section where the user can select the script file to run. Click the dropdown menu, choose the script by name, and then click the dropdown menu again to load the selected script. The Activity log displays the register writes issued from the script.

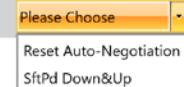
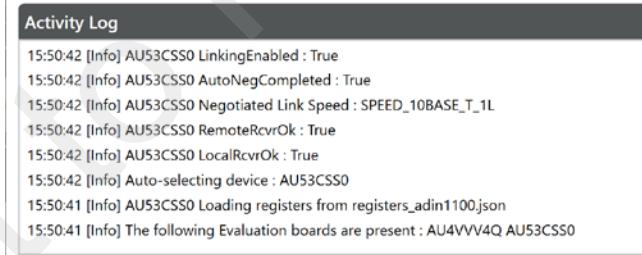


Figure 41. Script File Loading Dropdown Menu

The script file is located in the **ADIN1100** folder and is named **registers\_scripts.json** (see Figure 42).

### analog Devices > ADIN1100

<input type="checkbox"/>	Name
<input checked="" type="checkbox"/>	registers_scripts.json

Figure 42. Script File Location

The register write commands can be loaded with either the register name or the register address, as shown in the simple examples in the file. The commands are loaded sequentially. Create the sequence of write commands using a text editor. Ensure that the exact syntax is copied and match the register names with those in the datasheet to prevent errors reported in the activity log. Give the script a unique name.

When the **SftPd Down&Up** routine is selected, see the following example:

```
{  
    "Name": "SftPd Down&Up",  
    "RegisterAccesses": [  
        {  
            "MemoryMap": "SPEPhy",  
            "RegisterName": "CRSM_SFT_PD",  
            "Value": 1  
        },  
        {  
            "MemoryMap": "SPEPhy",  
            "RegisterName": "CRSM_SFT_PD",  
            "Value": 0  
        },  
    ]  
},
```

## TROUBLESHOOTING

### SOFTWARE INSTALLATION TIPS

Ethernet PHY software installation tips follow:

- Always allow the software installation to be completed, and keep in mind that the Ethernet PHY software is a two-part installation including the ADI package installer (GUI and documentation) and the FTDI drivers which can be found at [www.ftdichip.com/Drivers/CDM/CDM21228\\_Setup.zip](http://www.ftdichip.com/Drivers/CDM/CDM21228_Setup.zip). The installation may require a restart of the PC.
- When the USB cable is first plugged in when in the GUI mode of operation, allow the new-found hardware wizard to run completely. This step is required prior to starting the Ethernet PHY software.
- If the EVAL-ADIN1100FMCZ does not appear in the GUI window, ensure that the following steps have been completed:
  - Power is applied to the EVAL-ADIN1100FMCZ.
  - The powered USB connector is connected to the EVAL-ADIN1100FMCZ.
  - The Ethernet cable is connected between the two boards.
  - The Ethernet PHY software is launched.

### SOFTWARE TIPS

If the Ethernet PHY software does not read any data back, check for any messages in the **Activity Log** section.

### HARDWARE TIPS

Ensure that power is applied to the EVAL-ADIN1100FMCZ.

Measure the voltage at various points on the EVAL-ADIN1100FMCZ using the 3V3, 1V8, 1V1, AVDD\_H, AVDD\_L, VDDIO and DVDD\_1P1 test points.

#### No Link Established

If no link is established, take the following steps to assist debug:

- Ensure that the Ethernet cable is connected properly to the P101 connector and between the EVAL-ADIN1100FMCZ boards or PHY pairs.
- When using two EVAL-ADIN1100FMCZ boards, ensure that both boards are powered.
- Ensure that the hardware configuration is appropriate for the required linking arrangement.

## AYOUT GUIDELINES

### BOARD STACKUP

The EVAL-ADIN1100FMCZ consists of a 4-layer PCB: the top layer, Layer 2, Layer 3, and the bottom layer. All layers have a copper pour, with an extra keep-out area along the left-hand-side of the board close to the Earth trace.

### GROUND PLANES

The top and bottom layers of the EVAL-ADIN1100FMCZ mainly carry signal and routing signals from the ADIN1100. The two inner layers are used for ground planes. Layer 2 is a full ground plane. Layer 3 also has a ground plane but is also used to track the power signals. Although the ADIN1100 is a mixed signal device, it only has one type of ground return, GND.

### POWER SUPPLY DECOUPLING

From a PCB layout point of view, it is important to locate the decoupling capacitors as close as possible to the power supply and GND pins to minimize the inductance.

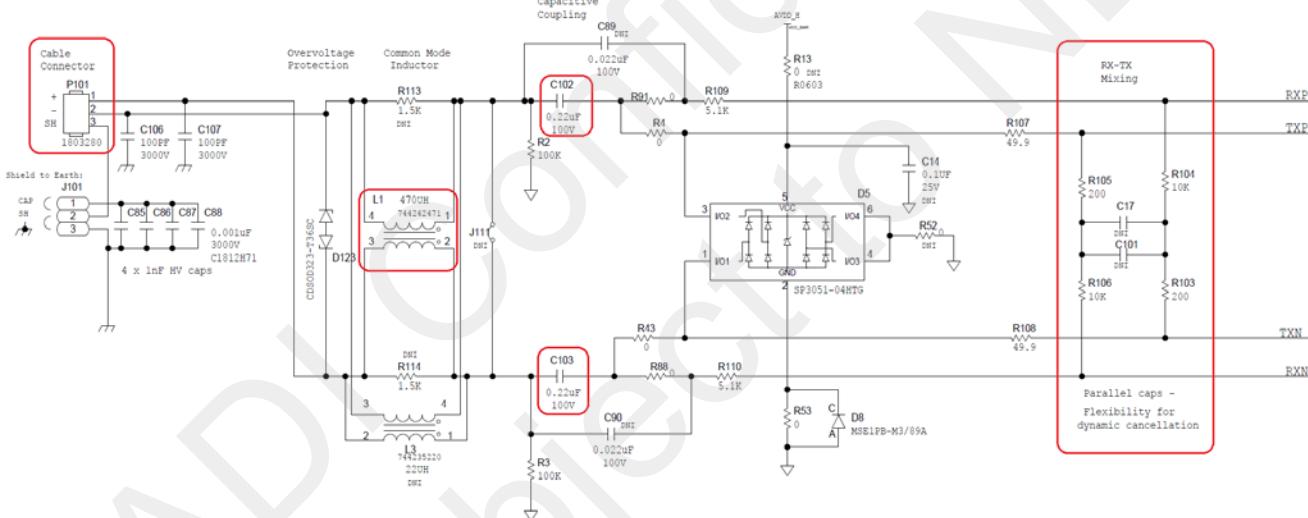


Figure 43. MDI Interface Connections.

### THERMAL CONSIDERATIONS

The ADIN1100 is packaged in an LFCSP package. This package is designed with an exposed paddle which must be soldered to the PCB for mechanical and thermal reasons. The exposed paddle acts to conduct heat away from the package and into the PCB. By incorporating an array of thermal vias in the PCB thermal paddle, heat is dissipated more effectively into the inner metal layers of the PCB. When designing the PCB layout for optimum thermal performance, use a 4 mm × 4 mm array of vias under the paddle.

### MAC INTERFACE

When routing the MAC interface traces, avoid crossover of the signals where possible. Stubs should be avoided on all signal traces. It is recommended to route traces on the same layer.

### MANAGEMENT INTERFACE

#### *MDI interface*

Traces running from the RXP/N and TXP/N pins of the ADIN1100 to the external hybrid circuit (R103-R106, C17, C101) must be, where possible, on the same side of the EVAL-ADIN1100FMCZ and kept as short as possible. The same recommendations apply for traces running through the C102 and C104 series capacitors to the common mode choke and onwards to the cable connector (P101) – see Figure 43. Impedance must be kept constant throughout. Trace lengths must be kept equal where possible and any right angles on these traces must be avoided (use curves or 45° angles in the traces). Stubs must be avoided on all signal traces.

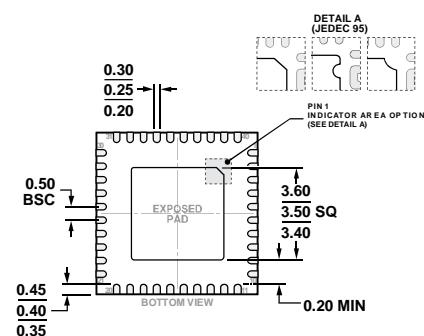
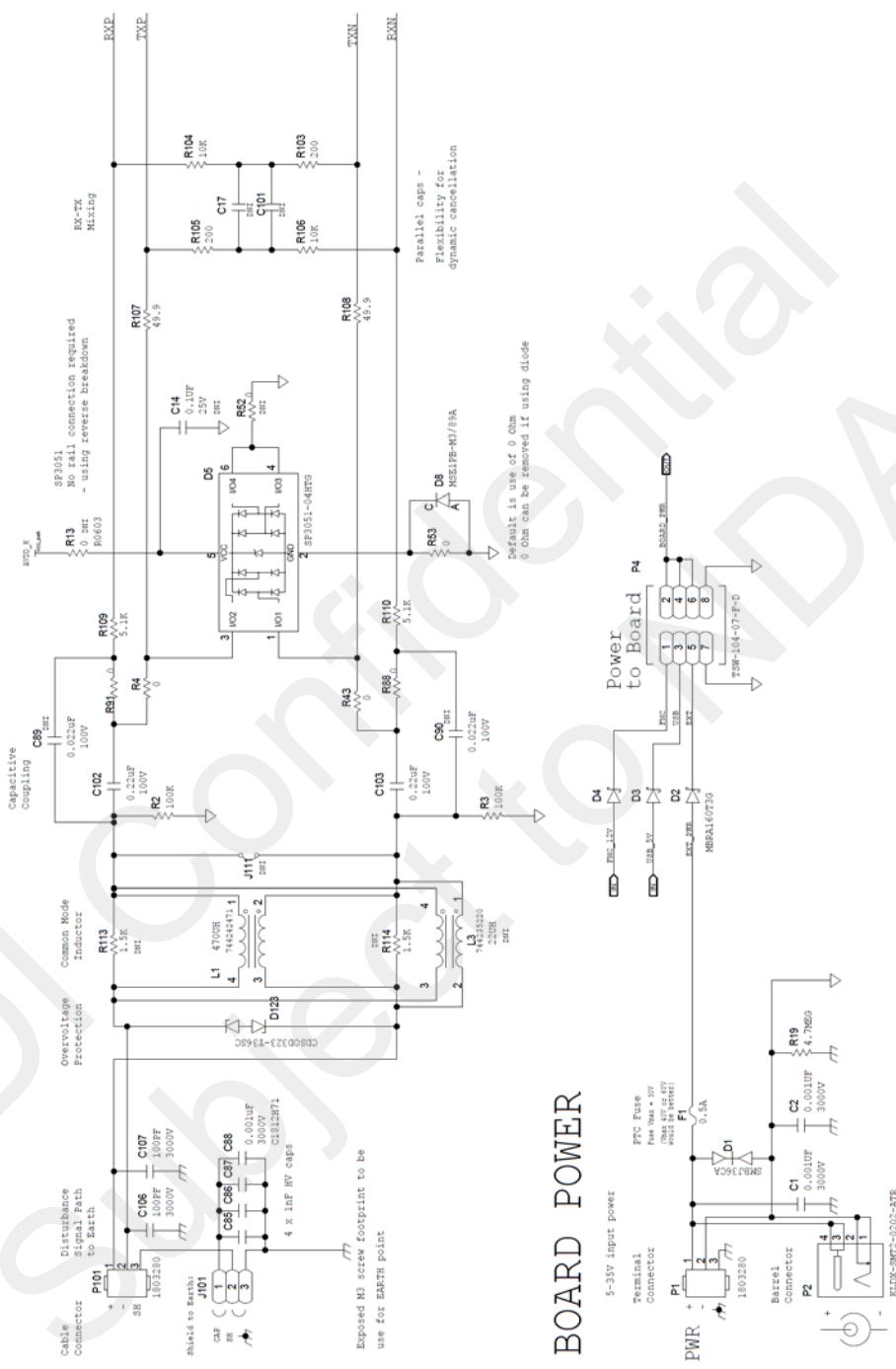


Figure 44. LFCSP Simplified Package Drawing

# EVALUATION BOARD SCHEMATICS AND ARTWORK

ADIN1100 CABLE CONNECTION



*Figure 45. Cable connection & EVAL-ADIN1100FMCZ Board Power*

## BOARD POWER SUPPLY

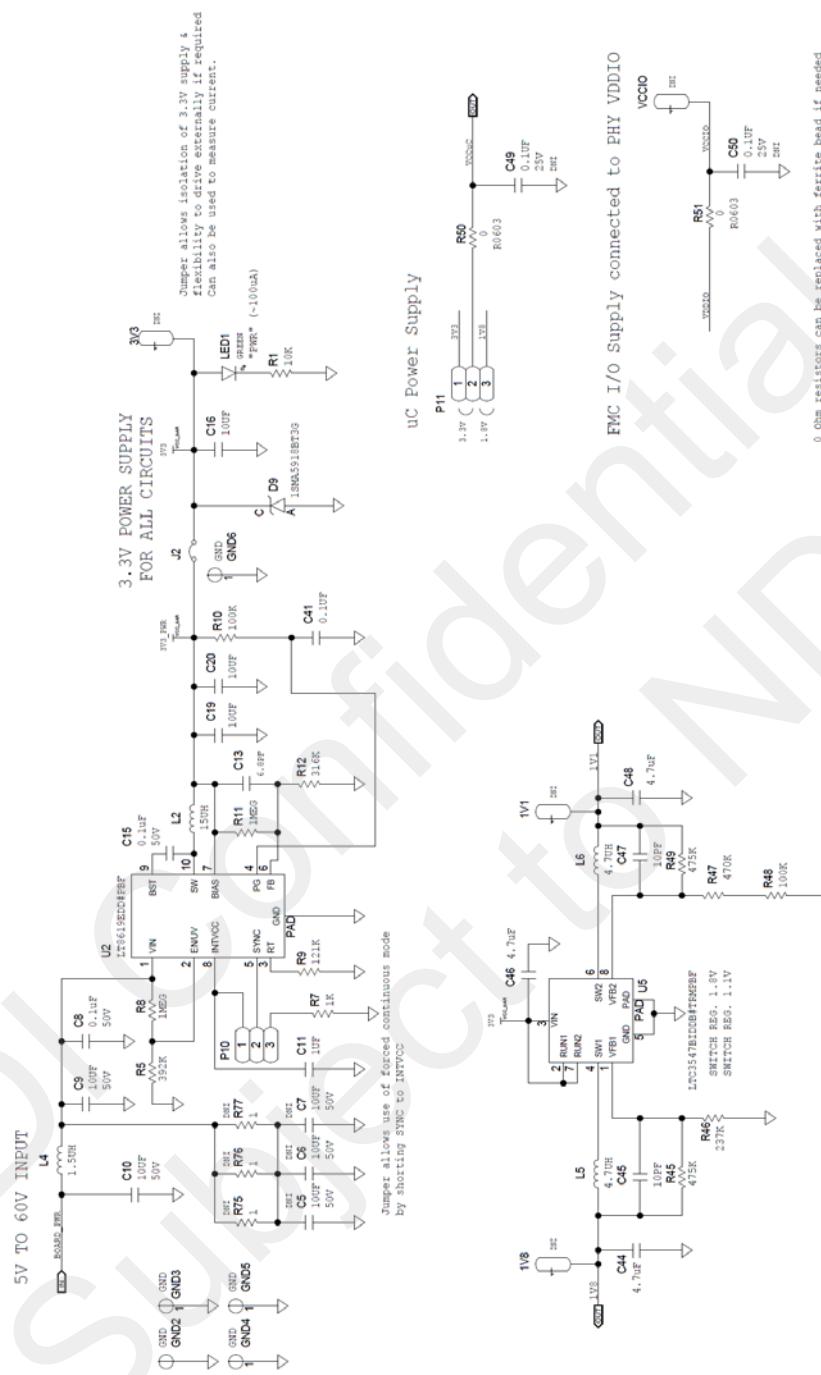


Figure 46. Power Supplies

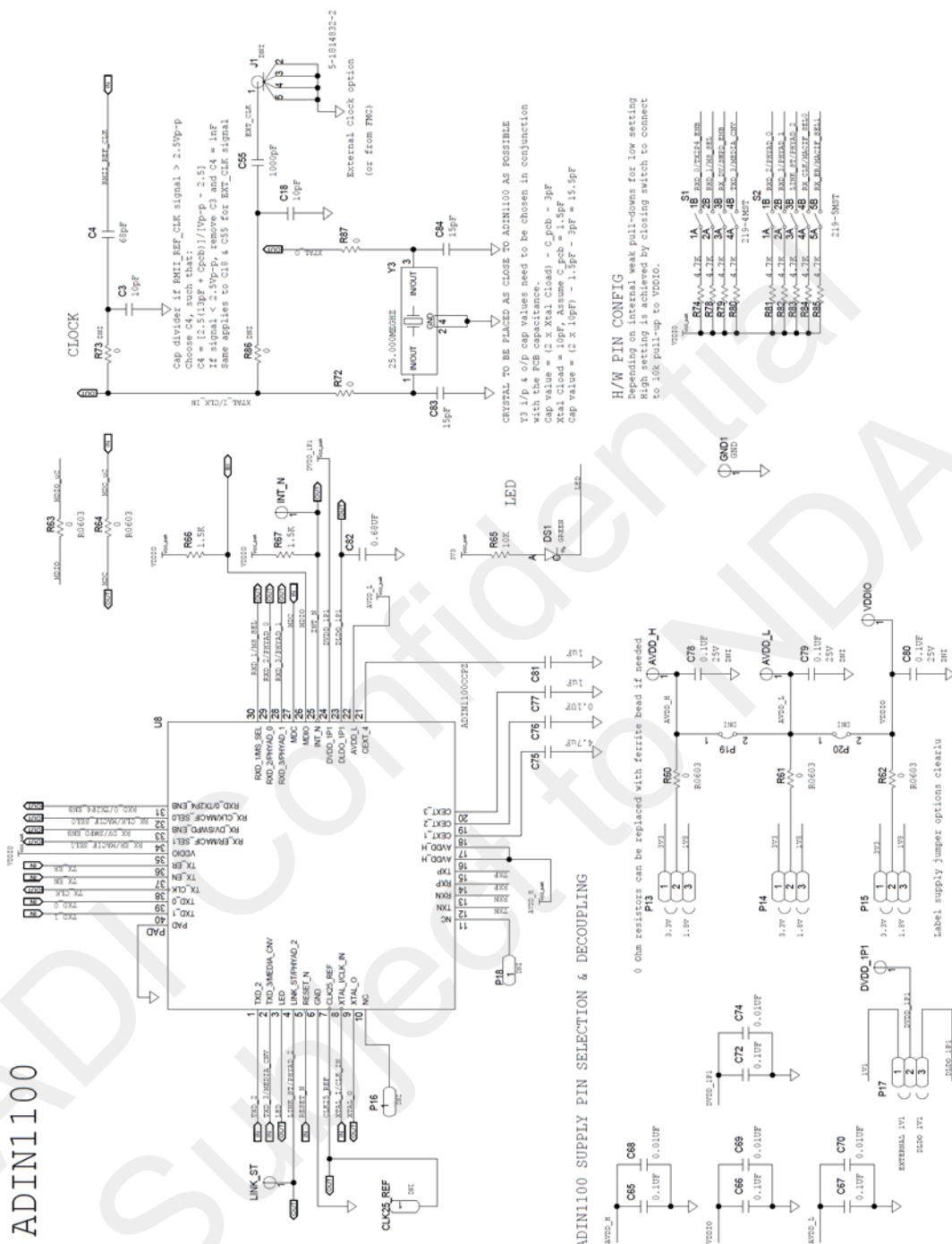
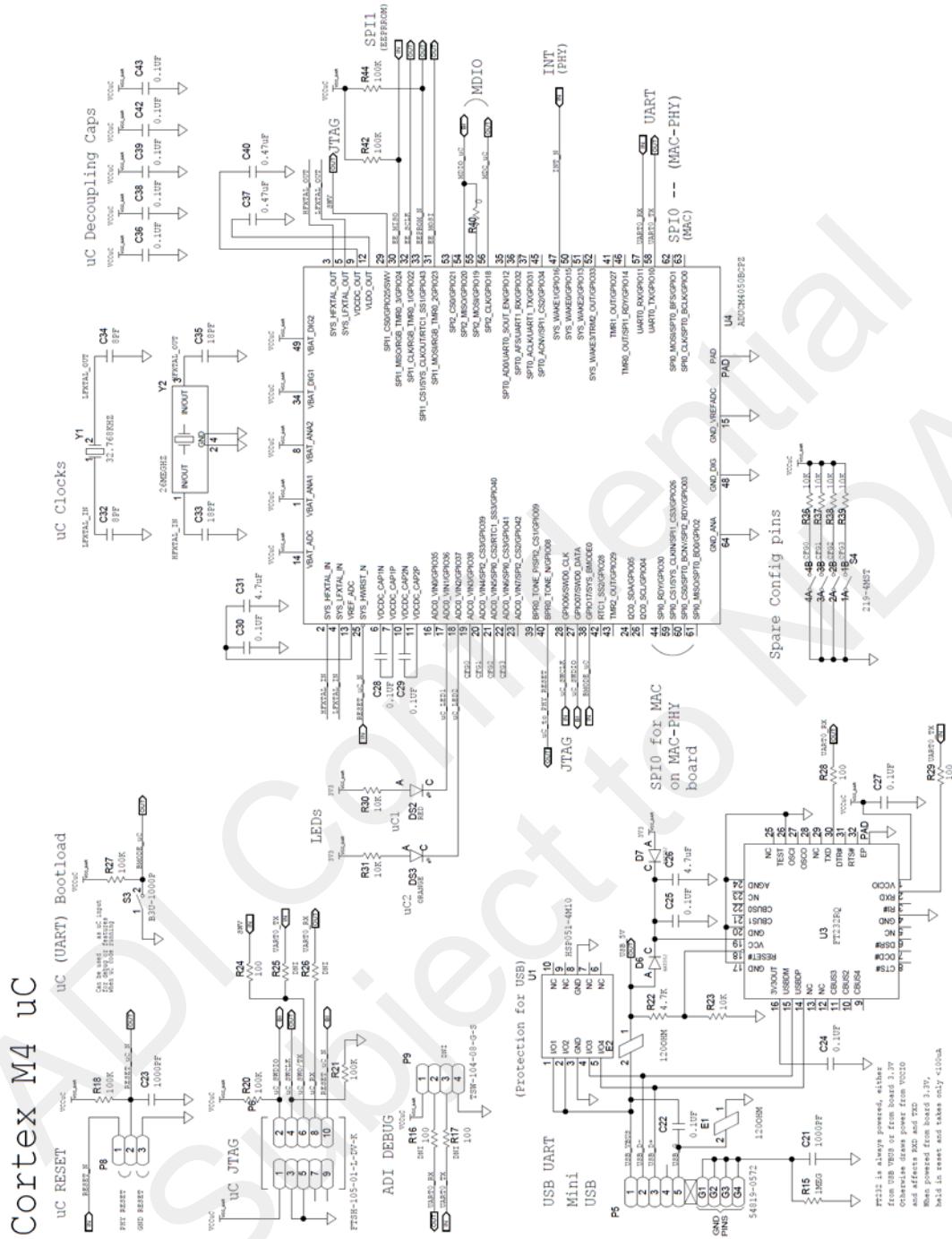
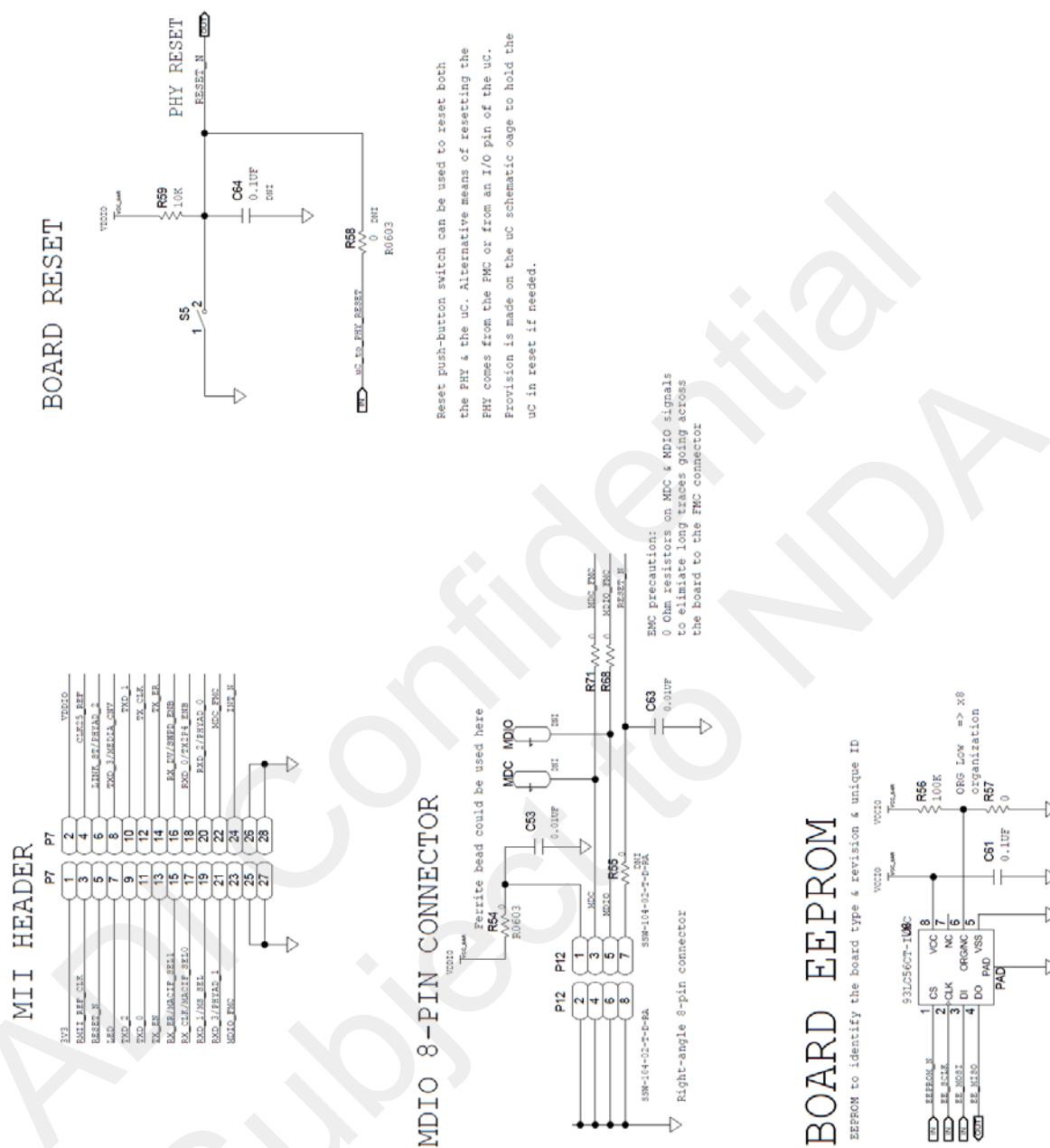


Figure 47. ADIN1100 Connections

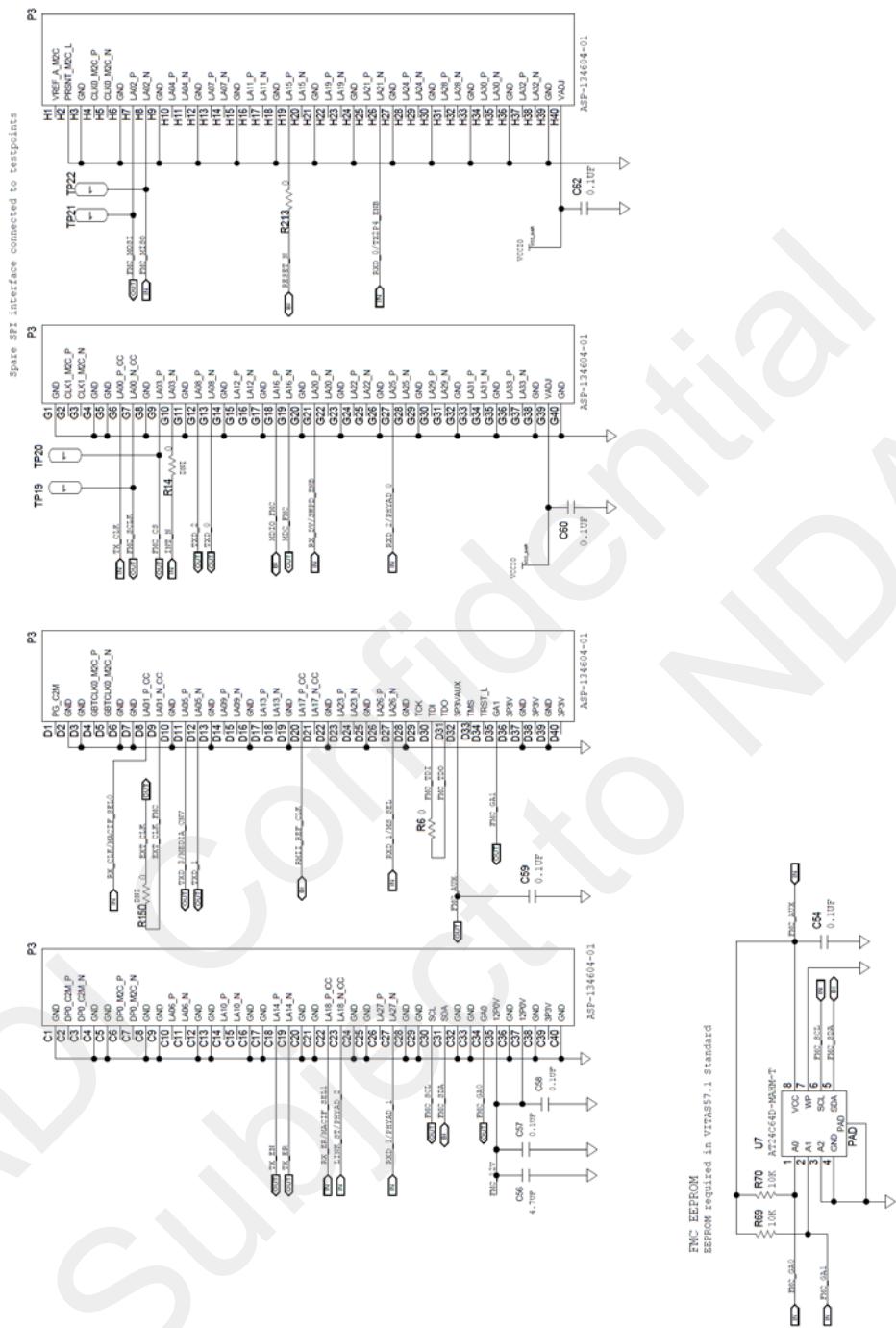


*Figure 48. ADuCM4050 Connections*



*Figure 49. Miscellaneous Circuitry*

FMC CONNECTOR



*Figure 50. FMC Connector*

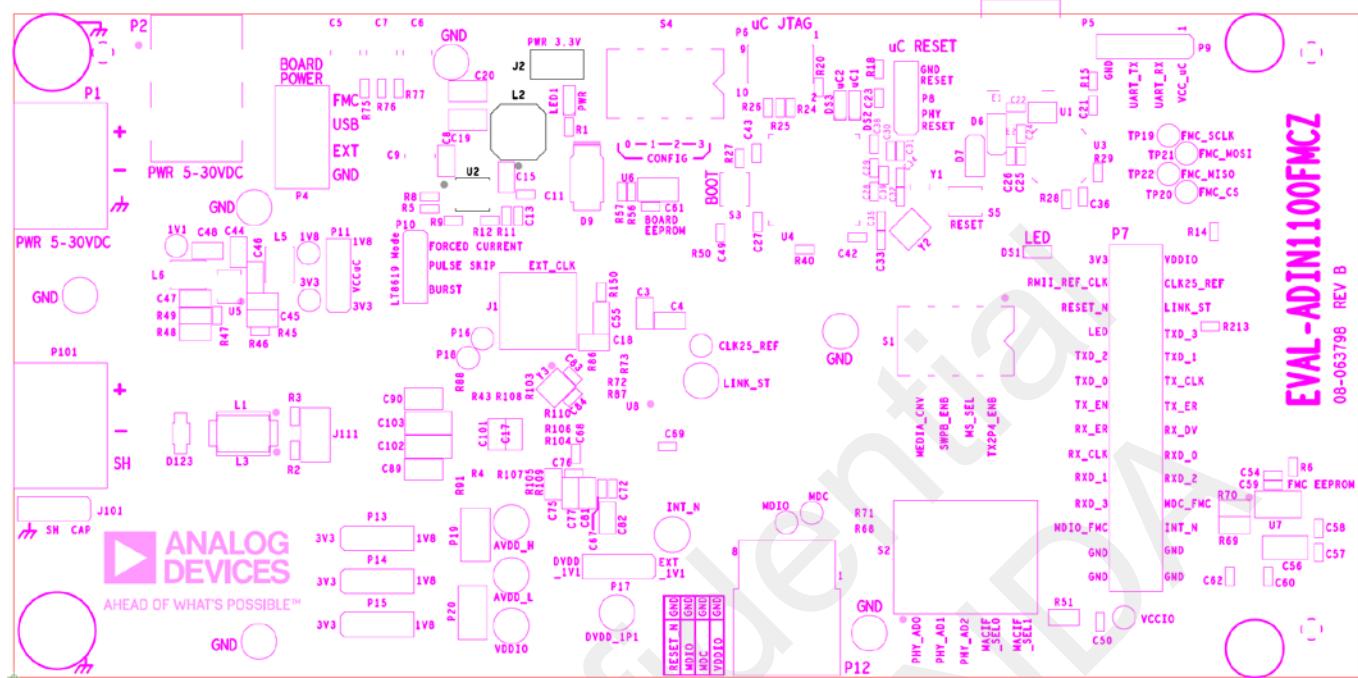


Figure 51. Schematic Silkscreen, Top

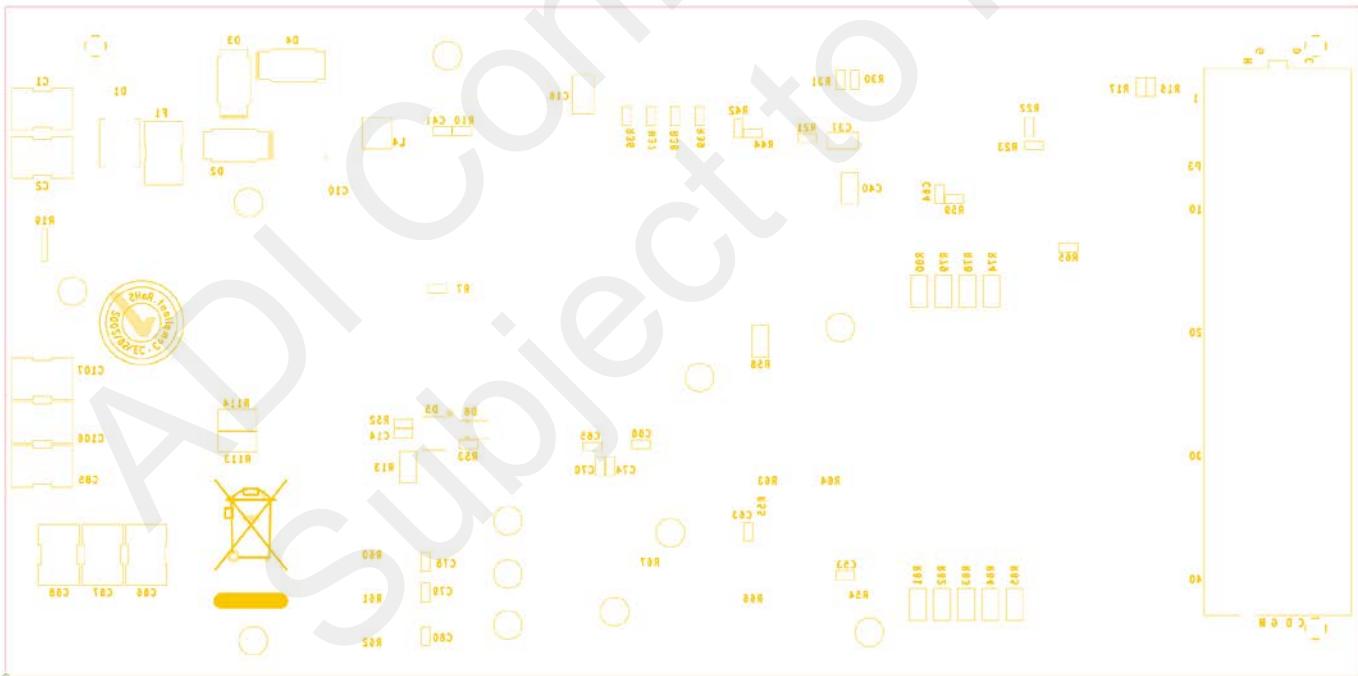


Figure 52. Schematic Silkscreen, Bottom

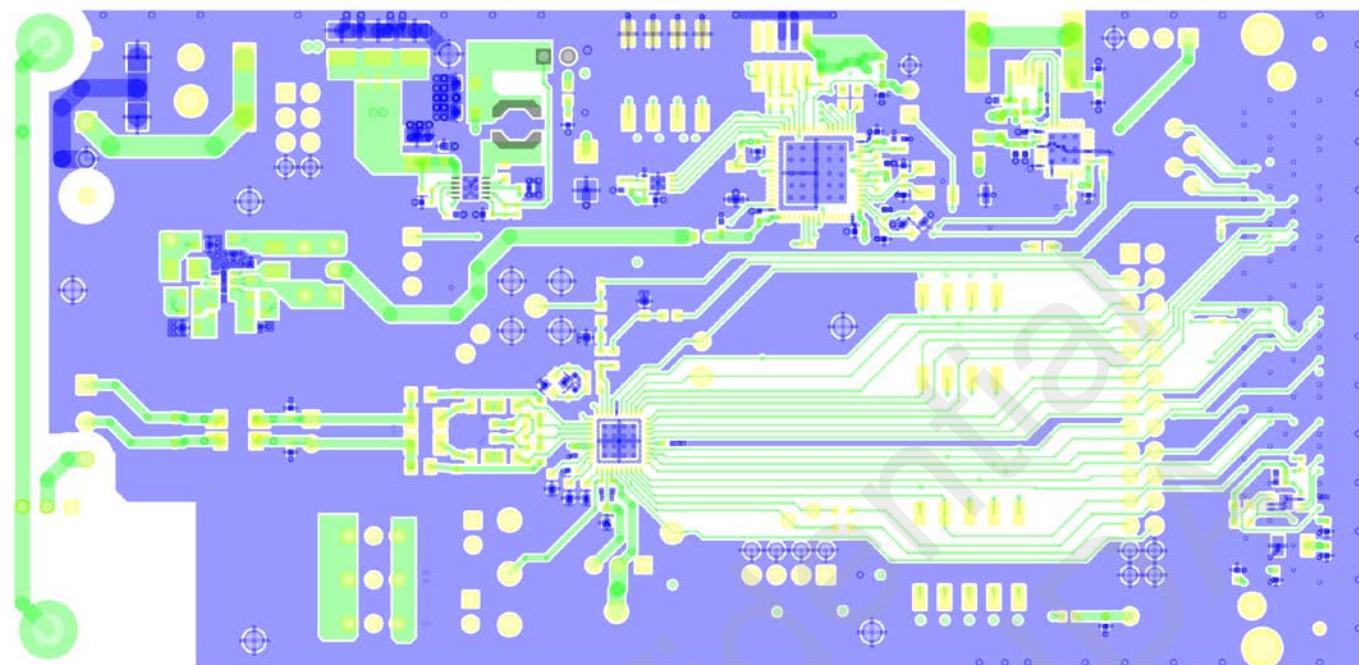


Figure 53. Top Layer

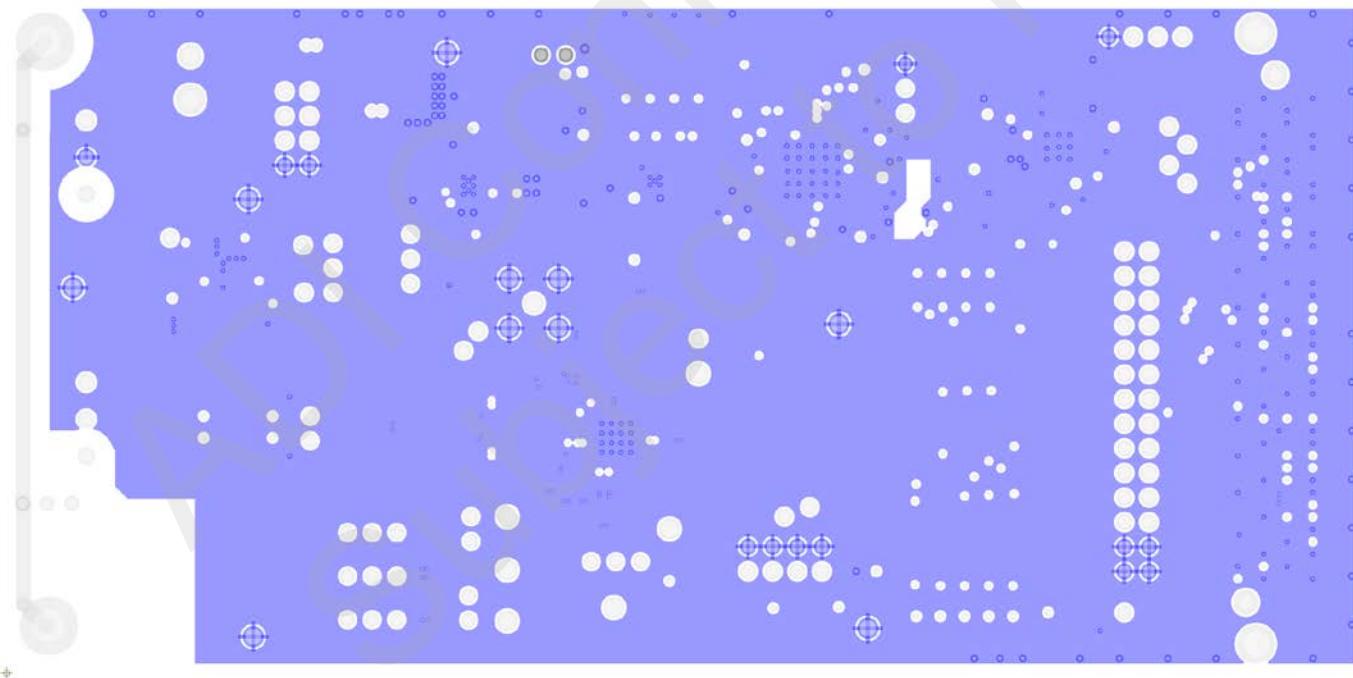


Figure 54. Layer 2, Ground Layer

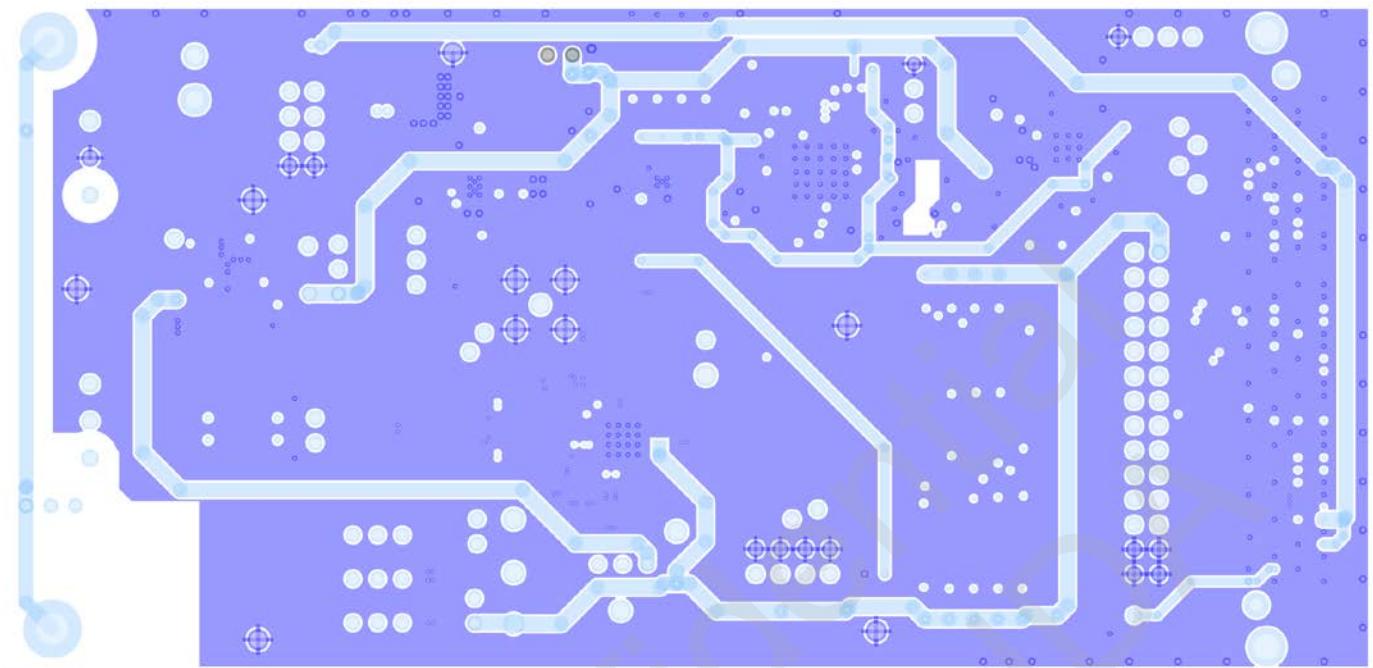


Figure 55. Layer 3, Power and Ground Layer

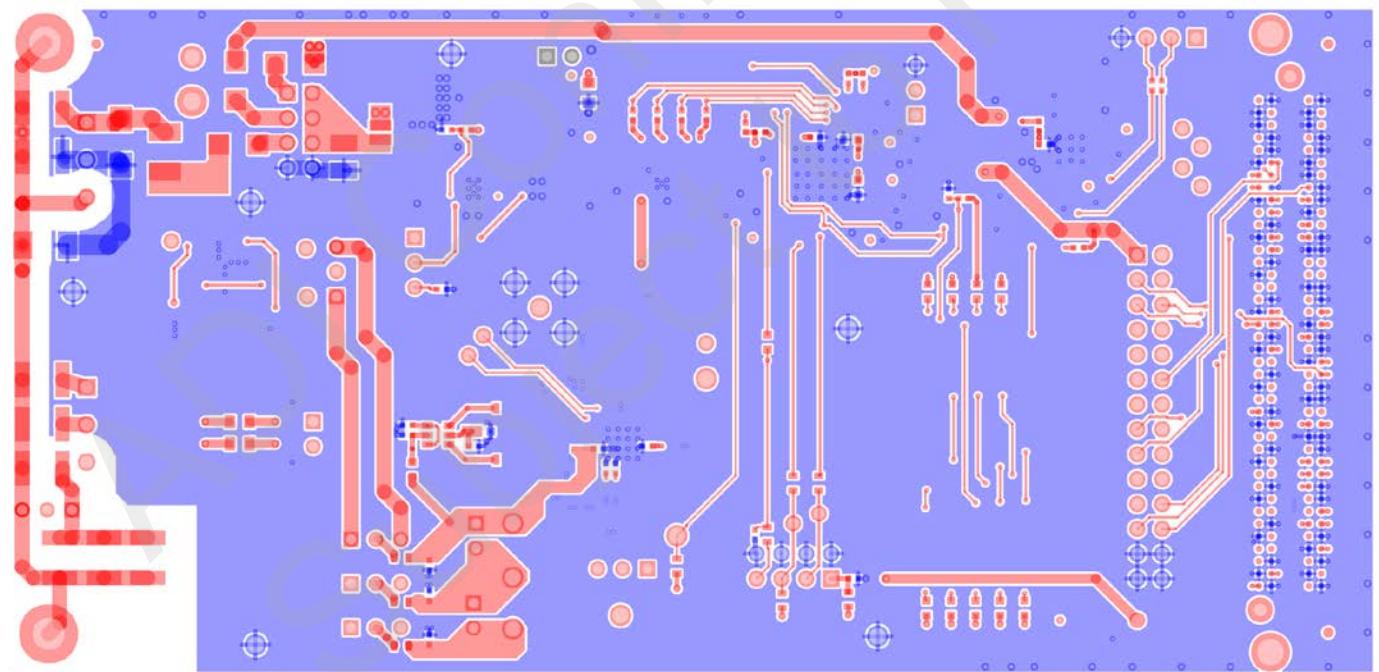


Figure 56. Bottom Layer

## ORDERING INFORMATION

### BILL OF MATERIALS

Table 7.

Qty	Reference Designator	Description	Manufacturer	Part Number
12	AVDD_H, AVDD_L, DVDD_1P1, GND1, GND2, GND3, GND4, GND5, GND6, INT_N, LINK_ST, VDDIO	Black test-point	KEYSTONE ELECTRONICS	CNKEY5005-9TP
6	C1, C2, C85, C86, C87, C88	Ceramic Capacitors, 0.001uF, 3000V, 10%, 1812, X7R	KEMET	C1812C102KHRACTU
2	C9, C10	Ceramic Capacitors, 10uF, 50V, 10%, 1210, X7R	MURATA	GRM32ER71H106KA12L
2	C102, C103	Ceramic Capacitors, 0.22uF, 100V, 10%, 1206, X7R	AVX	12061C224KAZ2A
2	C106, C107	Ceramic Capacitors, 100pF, 3000V, 5%, 1812, COG	KEMET	C1812C101JHGACTU
1	C11	Ceramic Capacitor, 1uF, 6.3V, 10%, 0402, X7R	MURATA	GRM155R70J105KA12D
1	C13	Ceramic Capacitor, 6.8pF, 50V, 0.25pF tol, 0402, NPO (COG)	MURATA	GJM1555C1H6R8CB01D
2	C8, C15	Ceramic Capacitors, 0.1uF, 50V, 10%, 0603, X7R	AVX	06035C104KAT2A
3	C16, C19, C20	Ceramic Capacitors, 10uF, 6.3V, 10%, 0805, X7R	MURATA	GCM21BR70J106KE22L
2	C3, C18	Ceramic Capacitors, 10pF, 50V, 0.5pF tol, 0603, COG	TDK	C1608C0G1H100D080DA
2	C21, C23	Ceramic Capacitors, 1000pF, 50V, 5%, 0402, NPO (COG)	MURATA	GRM1555C1H102JA01
19	C22, C24, C25, C27, C28, C29, C30, C36, C38, C39, C41, C42, C43, C61, C65, C66, C67, C72, C76	Ceramic Capacitors, 0.1uF, 25V, 10%, 0402, X7R	AVX CORPORATION	04023C104KAT2A
2	C26, C31	Ceramic Capacitors, 4.7uF, 6.3V, 20%, 0402, X5R	MURATA	GRM155R60J475ME87D
2	C32, C34	Ceramic Capacitors, 8pF, 16V, 0.5pF tol, 0402, COG	AVX CORPORATION	0402YA8R0DAT2A
2	C33, C35	Ceramic Capacitors, 18pF, 50V, 5%, 0402, NPO (COG)	MURATA	GJM1555C1H180JB01D
2	C37, C40	Ceramic Capacitors, 0.47uF, 16V, 10%, 0603, X7R	MURATA	GCM188R71C474KA55D
1	C4	Ceramic Capacitor, 68pF, 50V, 5%, 0603, NPO	YAGEO	CC0603JRNP09BN680
3	C44, C46, C48	Ceramic Capacitors, 4.7uF, 16V, 10%, 0603, X5R	TDK	C1608X5R1C475K080AC
2	C45, C47	Ceramic Capacitors, 10pF, 50V, 5%, 0603, COG/NPO, High Temp	KEMET	C0603H100J5GAC7867
6	C53, C63, C68, C69, C70, C74	Ceramic Capacitors, 0.01uF, 25V, 10%, 0402, X7R	TDK	C1005X7R1E103K050EB
6	C54, C57, C58, C59, C60, C62	Ceramic Capacitors, 0.01uF, 16V, 10%, 0402, X7R	AMERICAN TECHNICAL CERAMICS	530L104KT16T
1	C55	Ceramic Capacitor, 1000pF, 100V, 5%, 0603, COG	TDK	C1608C0G2A102J
1	C56	Ceramic Capacitor, 4.7uF, 25V, 10%, 1206, X7R	KEMET	C1206C475K3RACTU
1	C75	Ceramic Capacitor, 4.7uF, 16V, 10%, 0603, X6S	MURATA	GRM188C81C475KE11D

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Qty	Reference Designator	Description	Manufacturer	Part Number
2	C77, C81	Ceramic Capacitors, 1uF, 16V, 10%, 0603, X7R	AVX	0603YC105KAT2A
1	C82	Ceramic Capacitor, 0.68uF, 10V, 10%, 0603, X7R	YAGEO	CC0603KRX7R6BB684
2	C83, C84	Ceramic Capacitors, 15pF, 50V, 1%, 0402, COG	MURATA	GCM1555C1H150FA16D
1	D1	Bidirectional TVS Diode	FAIRCHILD SEMICONDUCTOR	SMBJ36CA
1	D123	Bidirectional TVS diode surge/ESD protection, 24A, 36V	BOURNS	CDSOD323-T36SC
3	D2, D3, D4	Schottky power rectifier diode, 60V	ON SEMICONDUCTOR	MBRA160T3G
1	D5	TVS diode array, lightening surge protection, 20A, 6V	LITTELFUSE, INC.	SP3051-04HTG
2	D6, D7	Schottky Diode, 23V, SOD-323	Stmicroelectronics	BAT20J
1	D8	ESD capability rectifier diode, 1A, 100V	VISHAY	MSE1PB-M3/89A
1	D9	Zener diode	ON SEMICONDUCTOR	1SMA5918BT3G
2	DS1, LED	Green LED, 2.65V	KINGBRIGHT ELECTRONIC	KPT-1608LVZGCK
1	DS2, uC1	Red LED, 1.8V	KINGBRIGHT ELECTRONIC	KPT-1608LVSECK-J3-PRV
1	DS3, uC2	Orande LED, 1.8V	KINGBRIGHT ELECTRONIC	KPT-1608LVSECK-J4-PRV
2	E1, E2	Ferrite bead, 0402, 120 Ohm	MURATA MANUFACTURING	BLM15EG121SN1D
1	F1	Polyfuse resettable PTC, 0.5A, 30V	LITTELFUSE, INC.	1812L050/30PR
8	J101, P8, P10, P11, P13, P14, P15, P17	3-position PCB header	MOLEX	22-28-4033
1	J2	PCB jumper/link	AMPHENOL FCI	69157-102HLF
1	L1	Common mode choke, 470uH, 0.35 Ohm DCR, 0.4A	WURTH ELEKTRONIK	744242471
1	L2	Inductor, 15uH, 1.4A, 0.16 Ohm DCR	COILCRAFT INC.	LPS5030-153MRC
1	L4	Inductor, 1.5uH	COILCRAFT INC.	EPL2014-152MLB
2	L5, L6	Inductor, 4.7uH, 0.216 Ohm DCR, 1A	MURATA MANUFACTURING	LQH32PN4R7NN0L
2	P1, P101	Pluggable screw terminal block, 3 ways, pitch 3.81 mm, 1.5 mm <sup>2</sup> (28AWG to 16AWG)	PHOENIX CONTACT	1803280 & MC 1,5/ 3-ST-3,81
1	P12	PCB right-angle header	SAMTEC INC.	SSW-104-02-T-D-RA
1	P2	PCB power jack	KYCON	KLDX-SMT2-0202-ATR
1	P3	FMC connector	SAMTEC	ASP-134604-01
1	P4	8-position PCB header	SAMTEC	TSW-104-07-F-D
1	P5	PCB mini USB connector	MOLEX	54819-0572
1	P6	PCB header	SAMTEC	FTSH-105-01-L-DV-K
1	P7	28-position PCB header	SAMTEC	TSW-114-07-F-D
10	R1, R23, R30, R31, R36, R37, R38, R39, R59, R65	Resistors, 10 kOhm, 1%, 0402	PANASONIC	ERJ-2RKF1002X
8	R10, R18, R20, R21, R27, R42, R44, R56	Resistors, 100 kOhm, 1%, 0402	PANASONIC	ERJ-2RKF1003X
2	R103, R105	Resistors, 200 Ohm, 1%, 0603	PANASONIC	ERJ-3EKF2000V
2	R104, R106	Resistors, 10 kOhm, 1%, 0603	PANASONIC	ERJ-3EKF1002V
2	R107, R108	Resistors, 49.9 Ohm, 0.1%, 0805	TYCO ELECTRONICS	RN73C2A49R9BTG
2	R109, R110	Resistors, 5.1 kOhm, 1%, 0603	PANASONIC	ERJ-3EKF5101V
3	R8, R11, R15	Resistors, 1 MOhm, 1%, 0402	PANASONIC	ERJ-2RKF1004X
1	R12	Resistor, 316 kOhm, 50 V, 1%, 0402	PANASONIC	ERJ-2RKF3163X

Qty	Reference Designator	Description	Manufacturer	Part Number
4	R6, R53, R150, R213	Resistors, 0 Ohm, 50 V, 1%, 0402	MULTICOMP (SPC)	MC00625W040210R
1	R19	Resistor, 4.7 MOhm, 5%, 2010	BOURNS	CHV2010-JW-475ELF
2	R2, R3	Resistors, 100 kOhm, 5%, 0402	PANASONIC	ERJ-2GEJ104X
1	R22	Resistor, 4.7 kOhm, 50 V, 1%, 0402	PANASONIC	ERJ-2RKF4701X
3	R24, R28, R29	Resistors, 100 Ohm, 1%, 0402	PANASONIC	ERJ-2RKF1000X
2	R4, R43	Resistors, 0 Ohm, 0805	MULTICOMP (SPC)	MC 0.1W 0805 0R
2	R40, R57	Resistors, 0 Ohm, 5%, 0402	PANASONIC	ERJ-2GE0R00X
2	R45, R49	Resistors, 475 kOhm, 1%, 0603	PANASONIC	ERJ-3EKF4753V
1	R46	Resistor, 237 kOhm, 1%, 0402	PANASONIC	ERJ-2RKF2373X
1	R47	Resistor, 470 kOhm, 1%, 0402	PANASONIC	ERJ-2RKF4703X
1	R48	Resistor, 100 kOhm, 50 V, 1%, 0603	PANASONIC	ERJ-3EKF1003V
1	R5	Resistor, 392 kOhm, 1%, 0402	YAGEO	RC0402FR-07392KL
11	R50, R51, R60, R61, R62, R63, R64, R72, R87, R88, R91	Resistors, 0 Ohm, 5%, 0603	PANASONIC	ERJ-3GEY0R00V
3	R54, R68, R71	Resistors, 0 Ohm, 1%, 0603	MULTICOMP (SPC)	MC0603WG00000T5E-TC
2	R66, R67	Resistors, 1.5 kOhm, 50 V, 1%, 0603	MULTICOMP (SPC)	MC 0.063W 0603 1% 1K5
2	R69, R70	Resistors, 10 kOhm, 1%, 0603	MULTICOMP (SPC)	MC0063W0603110K
1	R7	Resistor, 1 kOhm, 1%, 0402	PANASONIC	ERJ-2RKF1001X
9	R74, R78, R79, R80, R81, R82, R83, R84, R85	Resistors, 4.7 kOhm, 1%, 0603	MULTICOMP (SPC)	MC 0.063W 0603 1% 4K7.
1	R9	Resistor, 121 kOhm, 1%, 0402	PANASONIC	ERJ-2RKF1213X
2	S1, S4	4-position surface mount switch	CTS	219-4MST
1	S2	5-position surface mount switch	CTS	219-5MST
2	S3, S5	Ultra small push-button switch	OMRON	B3U-1000P
4	TP19, TP20, TP21, TP22	Micro pin test-point	KEYSTONE ELECTRONICS	1405-2
1	U1	4-line ESD protection for high speed lines	ST MICROELECTRONICS	HSP051-4M10
1	U2	LT8619 60V, 1.2A Synchronous monolithic buck regulator	LINEAR TECHNOLOGY	LT8619EDD#PBF
1	U3	USB Serial UART	FTDI CHIP	FT232RQ
1	U4	ADuCM4050 ultra low power ARM cortex microcontroller	ANALOG DEVICES	ADUCM4050BCPZ
1	U5	LTC3547 Dual monolithic synchronous step-down regulator	ANALOG DEVICES	LTC3547BIDDB#TRMPBF
1	U6	2K microwire compatible serial EEPROM	MICROCHIP TECHNOLOGY	93LC56CT-I/MC
1	U7	2-wire serial EEPROM	ATMEL	AT24C64D-MAHM-T
1	U8	ADIN1100 Robust industrial low power 10BASE-T1L ethernet PHY	ANALOG DEVICES	ADIN1100CCPZ
1	Y1	32.768 kHz crystal	ABRACON CORP.	ABS07-120-32.768KHZ-T
1	Y2	26 MHz crystal	ECS, INC.	ECS-260-10-36Q-ES-TR
1	Y3	25 MHz crystal	SEIKO EPSON	FA-128_25.000000MHZ_10.0_-+10-10

Table 8. Not Populated

Qty	Reference Designator	Description	Supplier	Part Number
9	1V1, 1V8, 3V3, CLK25_REF, MDC, MDIO, P16, P18, VCCIO	Test-points	KEYSTONE ELECTRONICS	1405-2
2	C17, C101	Ceramic Capacitors, 4.7 pF, 100 V, 0.1pF tol, 0603, COG	MURATA	GCM1885C2A4R7BA16D
7	C14, C49, C50, C64, C78, C79, C80	Ceramic Capacitors, 0.1 uF, 25 V, 10%, 0402, X7R	AVX CORPORATION	04023C104KAT2A

Qty	Reference Designator	Description	Supplier	Part Number
3	C5, C6, C7	Ceramic Capacitors, 10 uF, 50 V, 10%, 1210, X7R	MURATA	GRM32ER71H106KA12L
2	C89, C90	Ceramic Capacitors, 0.022 uF, 100 V, 10%, 0805, X7R	AVX	08051C223KAT2A
1	J1	SMA	TE CONNECTIVITY LTD	5-1814832-2
3	J111, P19, P20	2-way PCB link	AMPHENOL FCI	69157-102HLF
1	L3	22 uH common mode line filter, 2.65 Ohm	WURTH ELEKTRONIK	744235220
1	P9	4-way header	SAMTEC	TSW-104-08-G-S
2	R113, R114	Resistors, 1.5 kOhm, 1%, 0805	PANASONIC	ERJ-6ENF1501V
4	R13, R58, R73, R86	Resistors, 0 Ohm, 5%, 0603	PANASONIC	ERJ-3GEY0R00V
2	R14, R52	Resistors, 0 Ohm, 50 V, 1%, 0402	MULTICOMP (SPC)	MC00625W040210R
4	R16, R17, R25, R26	Resistors, 100 Ohm, 1%, 0402	PANASONIC	ERJ-2RKF1000X
1	R55	Resistor, 0 Ohm, 1%, 0603	MULTICOMP (SPC)	MC0603WG00000T5E-TC
3	R75, R76, R77	Resistors, 1 Ohm, 1%, 0402	PANASONIC	ERJ-2BQF1R0X

Table 9. Mechanical Parts

Qty	Reference Designator	Description	Supplier	Part Number
1	N/A	USB cable	ASSMANN	AK672M/2-1-R
10	N/A	2.54mm black open-top jumper contact	SULLINS	QPC02SXGN-RC
2	N/A	Black adhesive bump pads	3M	SJ5076

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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