

ZYNC Z7010 DEMO

Variant: [No Variations]

11/30/2020
V1I1

PRELIMINARY

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DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

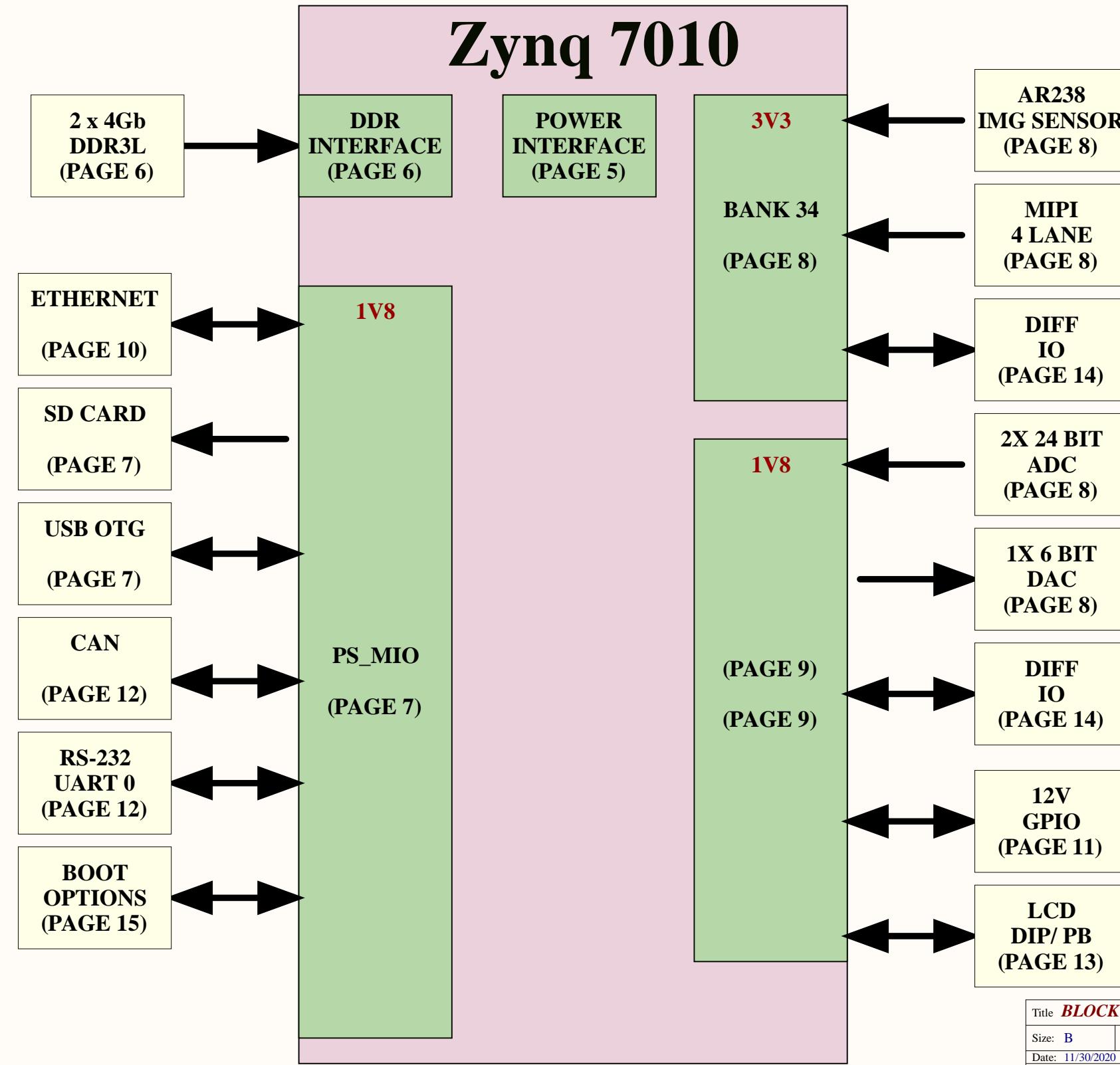
DESIGN NOTE:
Example text for critical design notes.

DESIGN NOTE:
Example text for cautionary design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

Title: COVER SHEET	Mathew Locoteta
Size: B	Number: 1
Revision: V1I1	Middle Island
Date: 11/30/2020	New York, 11953
Time: 12:24:56 PM	United States of America
Sheet 1 of 16	
File: C:\Users\Public\Documents\Altium\Projects\Zync 7000 Demo[1] - COVER PAGE.SchDoc	

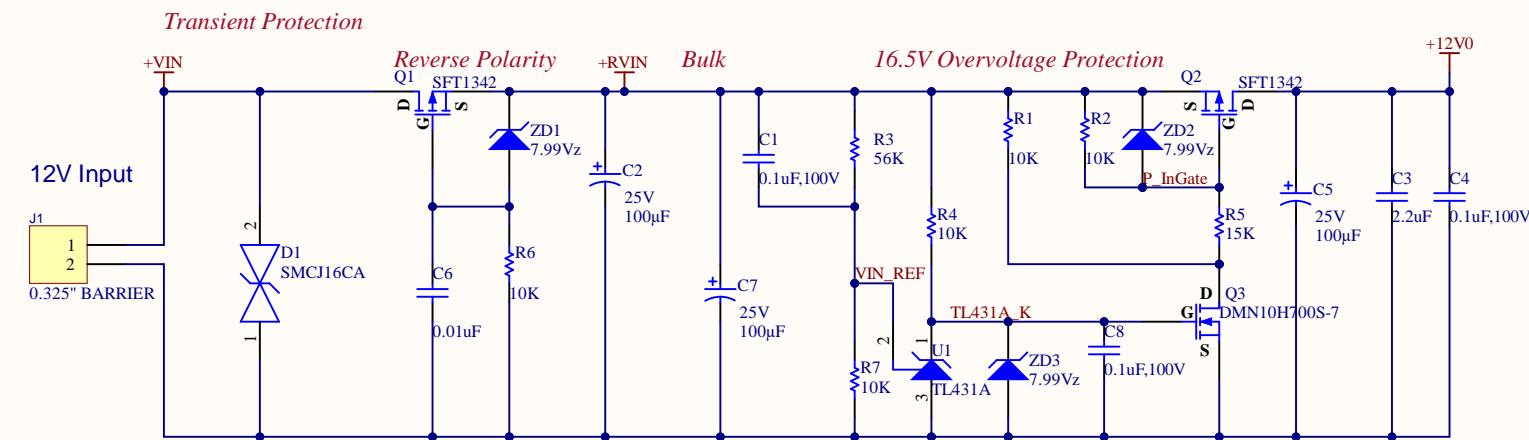
Peripheral Block Diagram



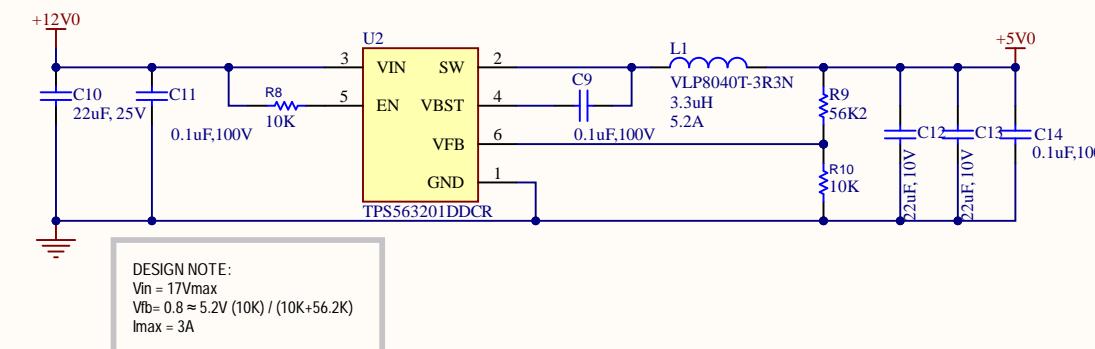
Title BLOCK DIAGRAM			Mathew Locoteta
Size: B	Number: 2	Revision: V1II	85 Artist Lake Dr.
Date: 11/30/2020	Time: 12:24:56 PM	Sheet 2 of 16	Middle Island
File: C:\Users\Public\Documents\Altium\Projects\Zynq 7000 Demo[2] - BLOCK DIAGRAM.SchDoc			New York, 11953
			United States of America

POWER

Input Protection

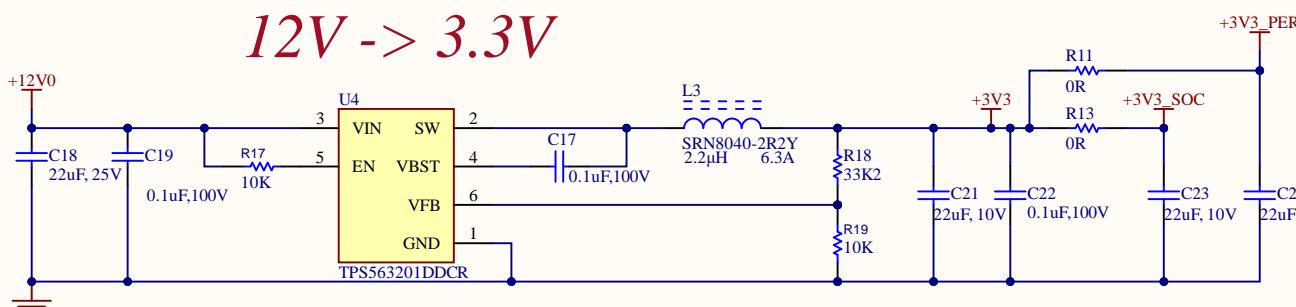


12V -> 5.0V



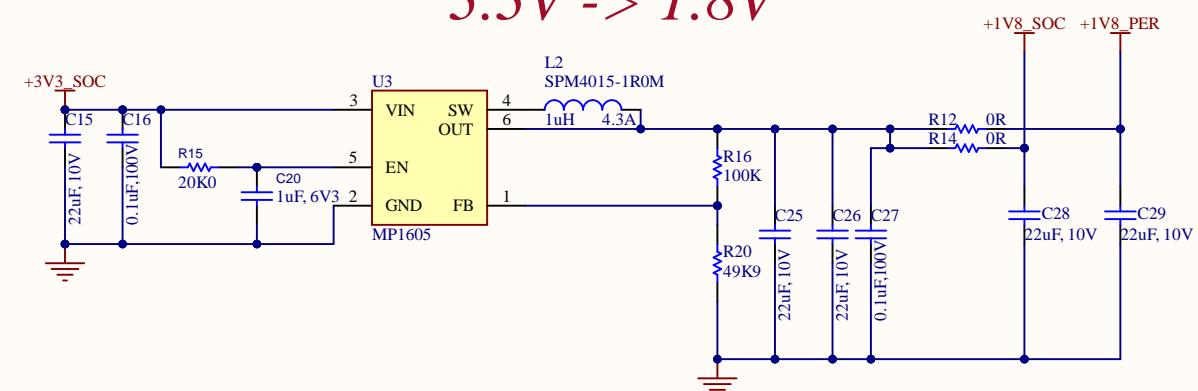
Title POWER INPUT			<i>Mathew Locoteta</i>
Size: B	Number: 3	Revision: V1II	<i>85 Artist Lake Dr. Middle Island New York, 11953 United States of America</i>
Date: 11/30/2020	Time: 12:24:57 PM	Sheet 3 of 16	
File: C:\Users\Public\Documents\Altium\Projects\Zynq 7000 Demo[3] - POWER.SchDoc			

POWER (CONT.)



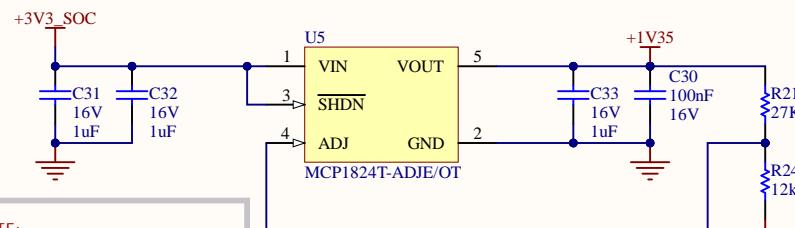
DESIGN NOTE:
 $V_{in} = 17V_{max}$
 $V_{fb} = 0.8 \approx 3.4V (10K) / (10K+33.2K)$
 $I_{max} = 3A$

3.3V -> 1.8V



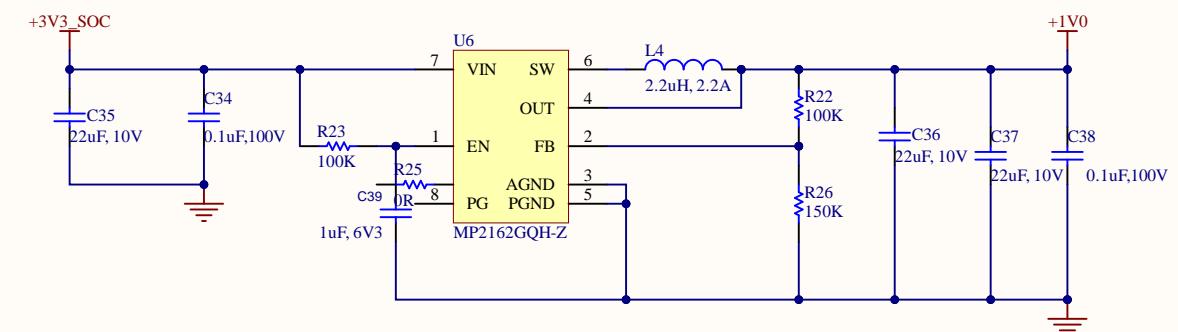
DESIGN NOTE:
 $V_{fb} = 0.6 \approx 1.802V (49.9K) / (100K+49.9K)$
 $I_{max} = 2A$

3.3V -> 1.35V



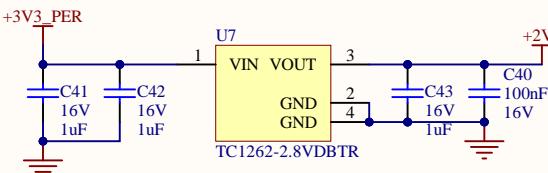
DESIGN NOTE:
 V_{fb} Range = 0.402-0.418 means $V_{out} = 1.31-1.35$
 Need tighter tolerance
 $I_{max} = 300mA$

3.3V -> 1.0V

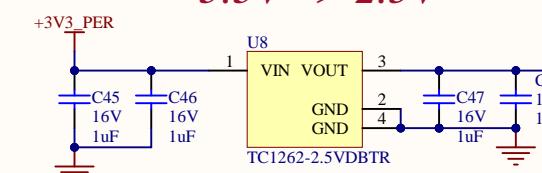


DESIGN NOTE:
 $V_{fb} = 0.6 \approx 1.00V (150K) / (100K+150K)$
 $I_{max} = 2A$

3.3V -> 2.8V



3.3V -> 2.5V



Title **REGULATORS**

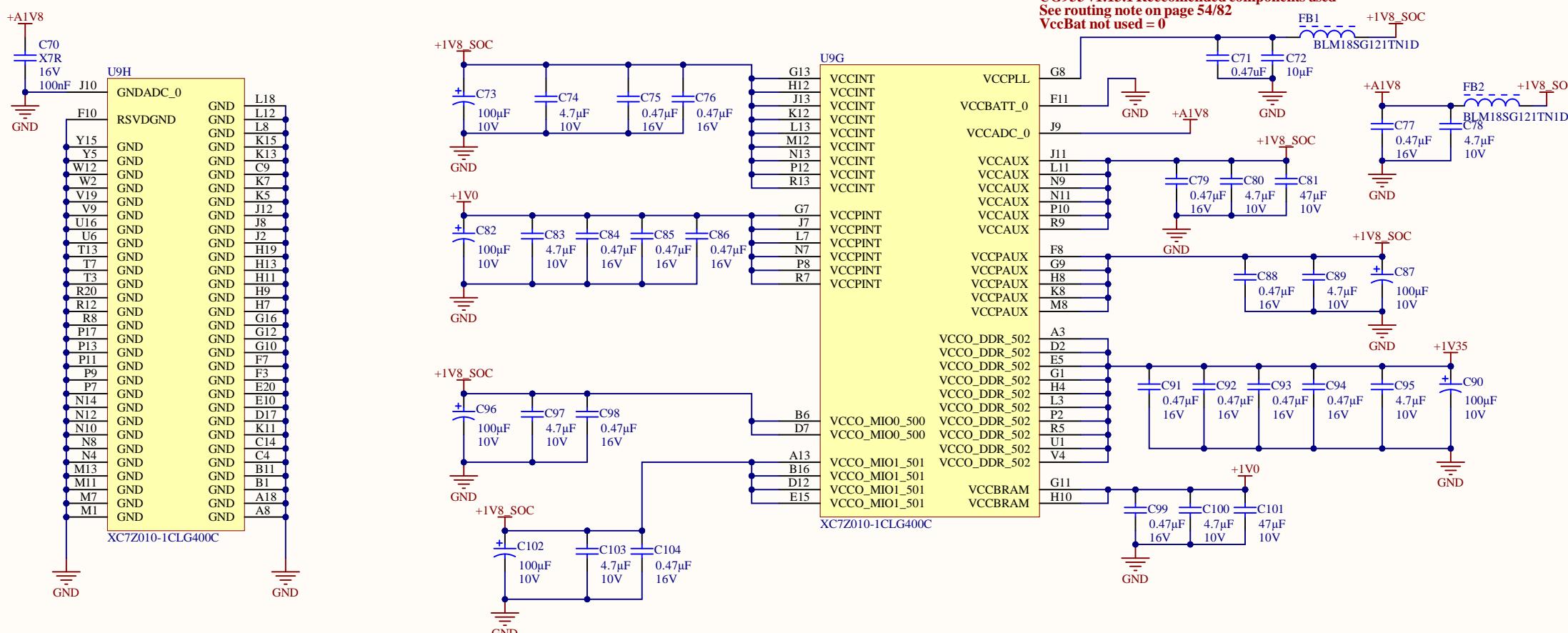
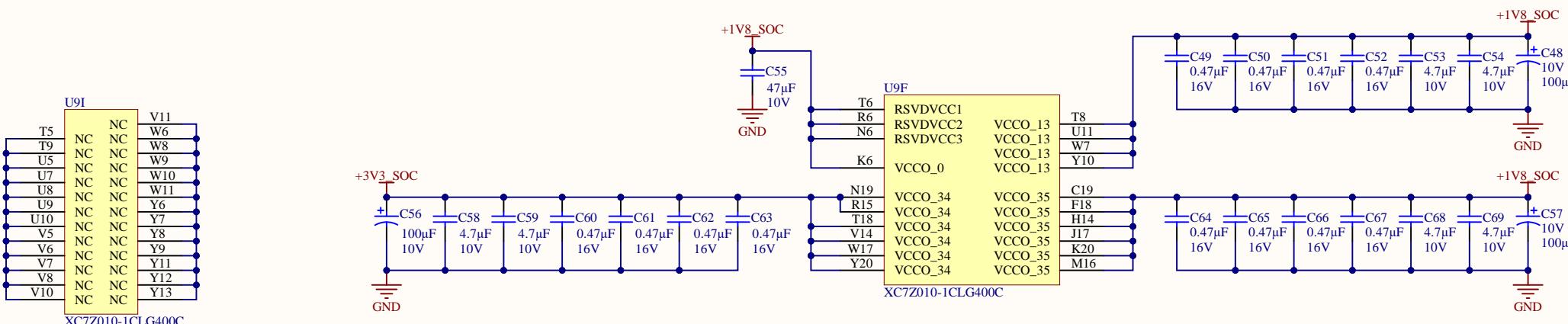
Mathew Locoteta
 85 Artist Lake Dr.
 Middle Island
 New York, 11953
 United States of America

Size: B Number: 4 Revision: V1II

Date: 11/30/2020 Time: 12:24:57 PM Sheet 4 of 16

File: C:\Users\Public\Documents\Altium\Projects\Zyneq 7000 Demo[4] - POWER (CONT).SchDoc

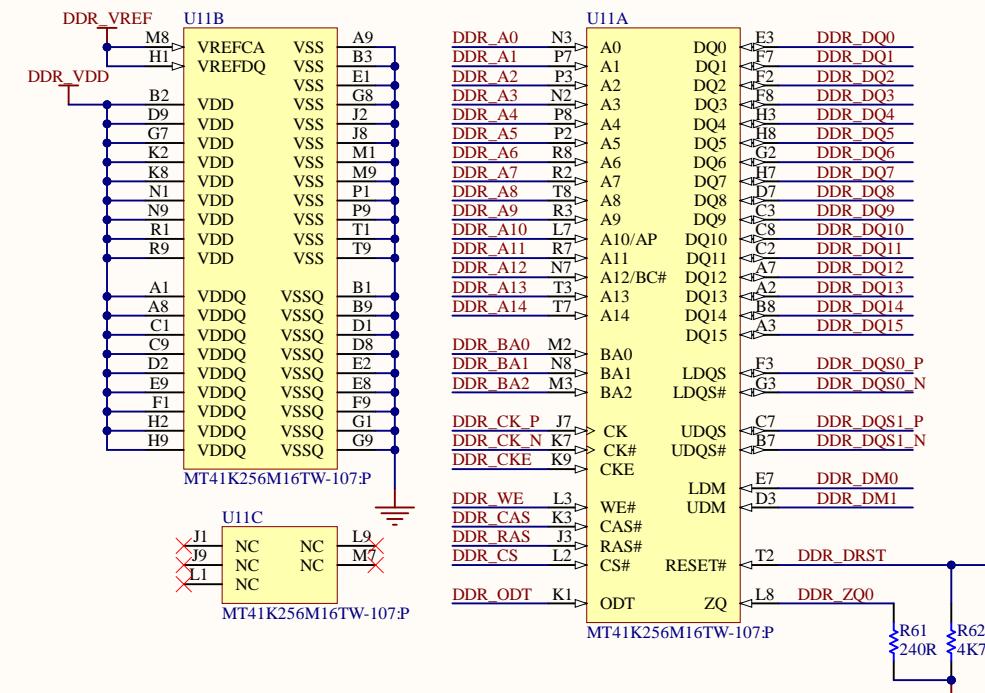
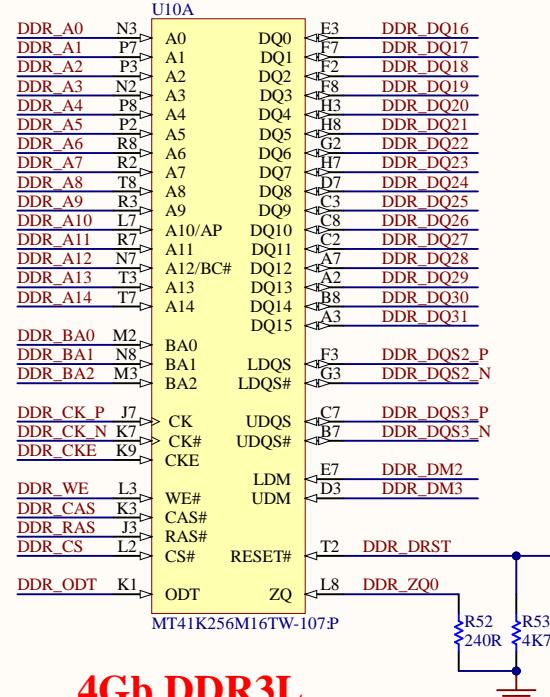
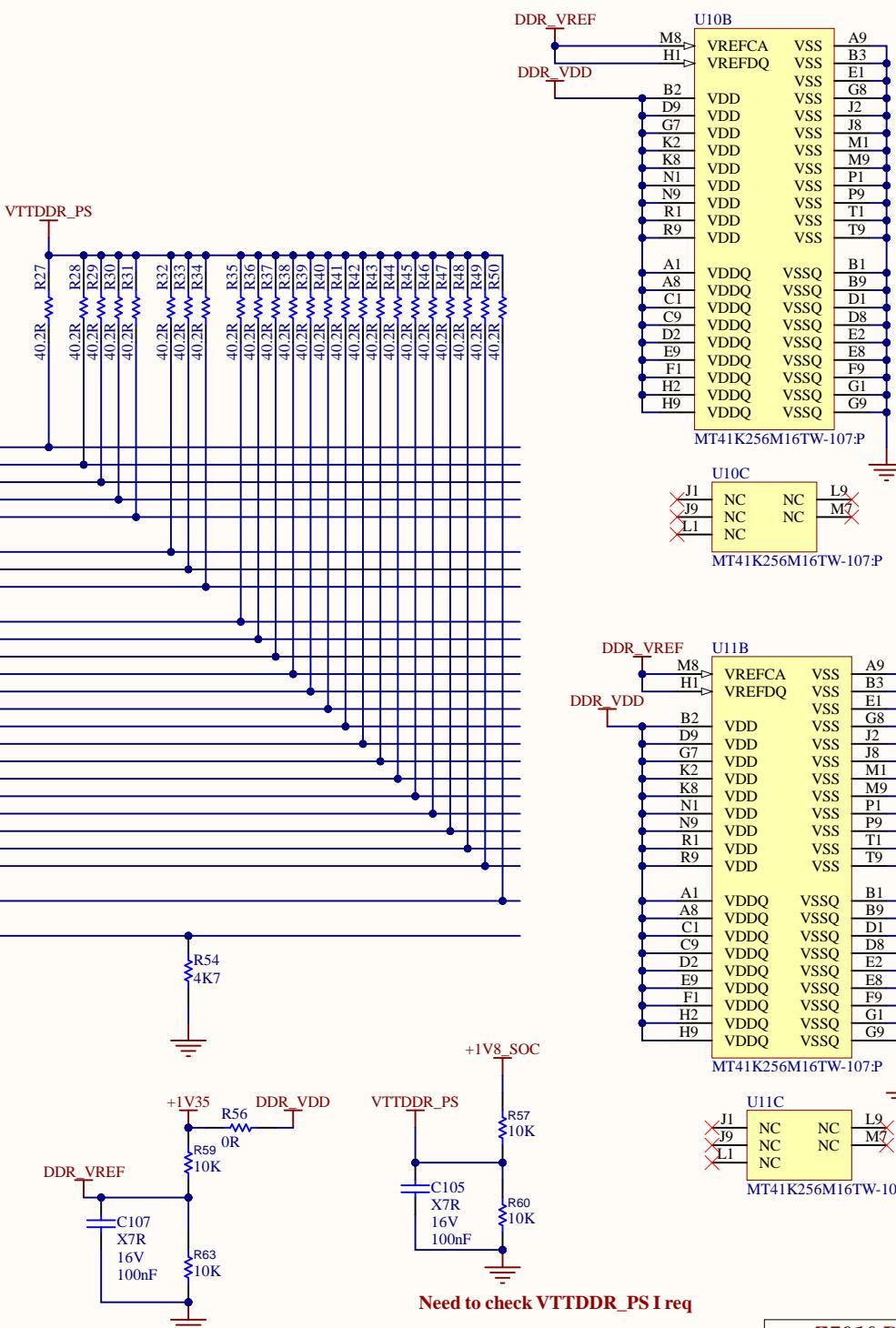
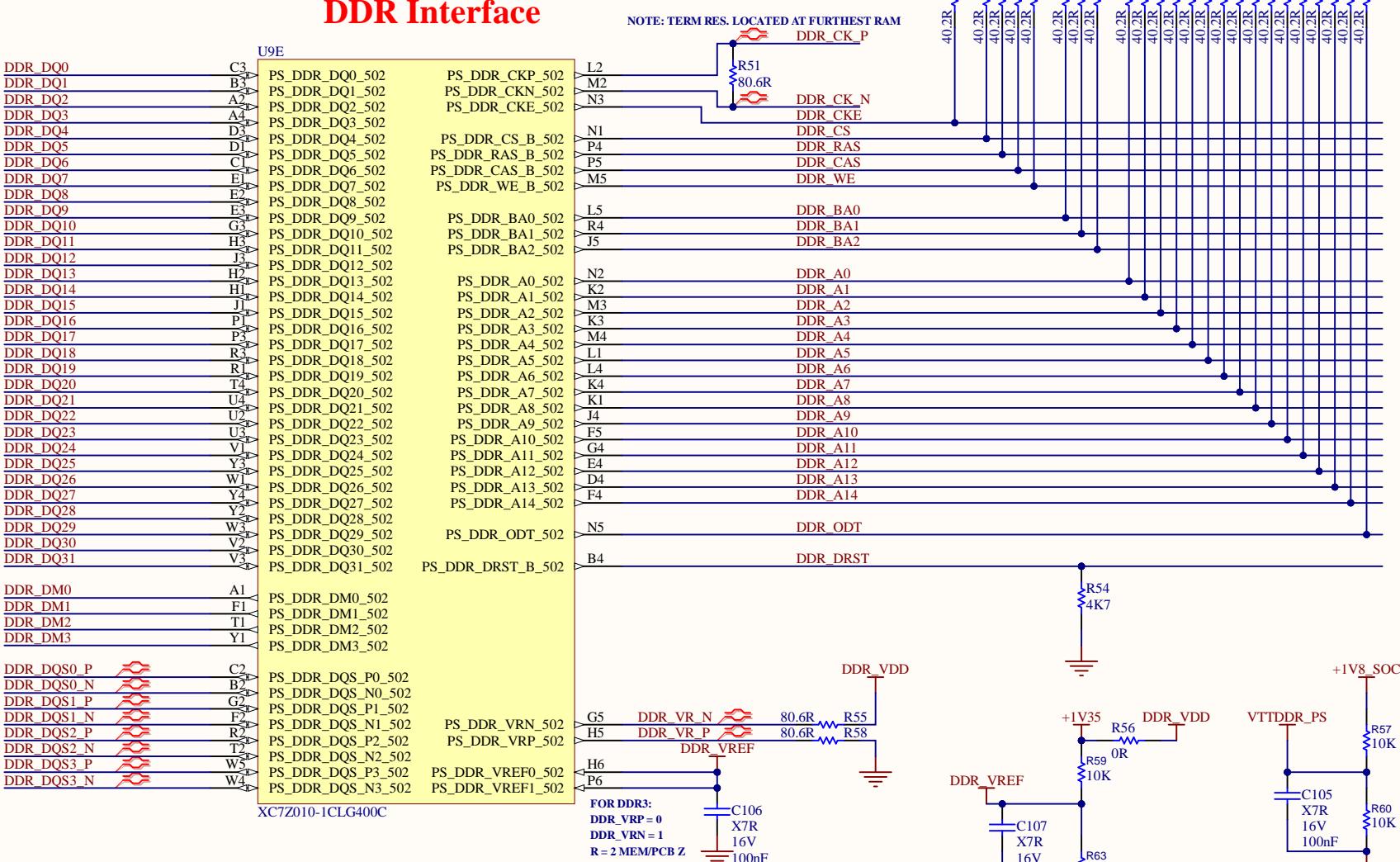
Z7010 POWER



Title Z7010 POWER INF			Mathew Locoteta 85 Artist Lake Dr. Middle Island New York, 11953
Size:	B	Number:	5
Revision:	*		<i>United States of America</i>
Date:	11/30/2020	Time:	12:24:57 PM Sheet 5 of 16
File:	C:\Users\Public\Documents\Altium\Projects\Zyna_7000 Demo\{51 - Z7010 POWER INF SchDoc		

Z7010 DDRC INTERFACE

4Gb DDR3L

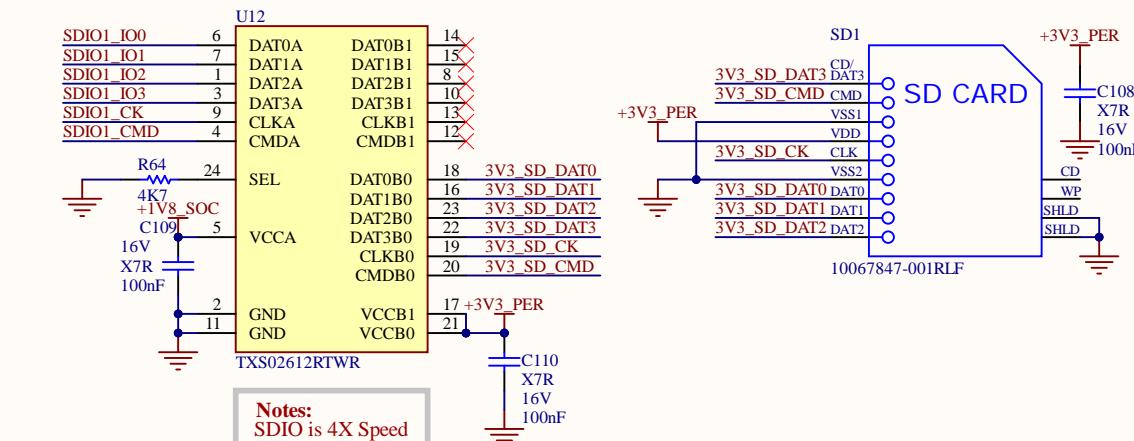
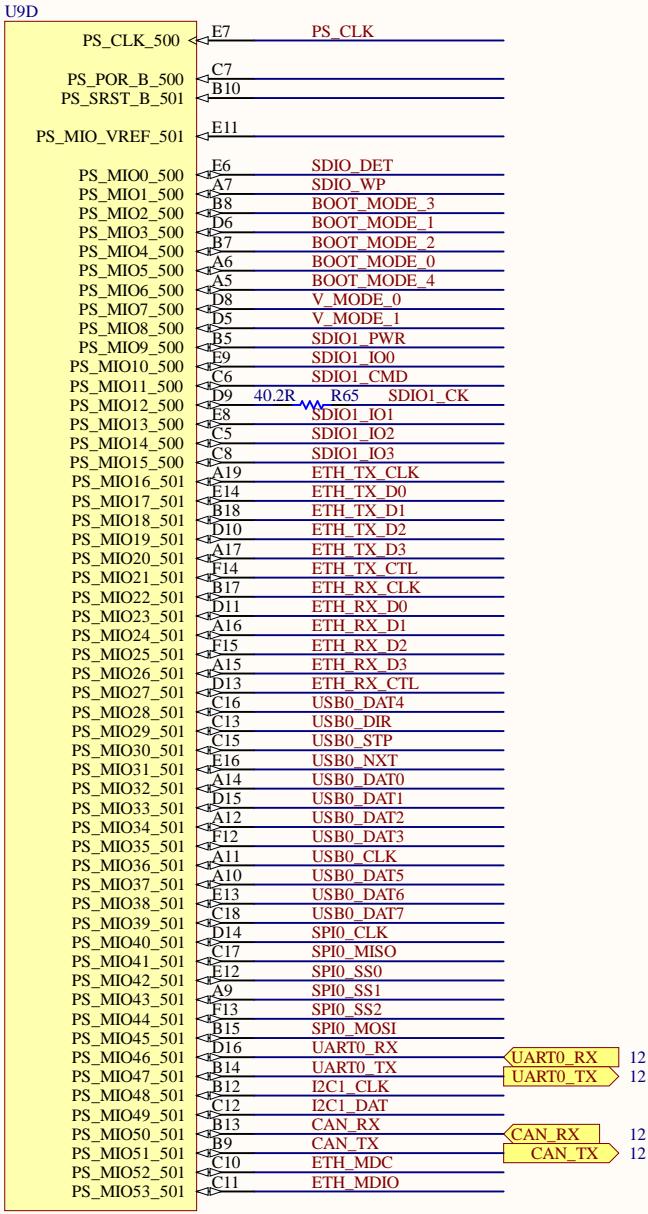


Title: Z7010 DDRC INTERFACE			Mathew Locoteta
Size: B	Number: 6	Revision: V1II	85 Artist Lake Dr.
Date: 11/30/2020	Time: 12:24:57 PM	Sheet 6 of 16	Middle Island
			New York, 11953
			United States of America

File: C:\Users\Public\Documents\Altium\Projects\Zynq 7000 Demo[6] - Z7010 DDR INF.SchDoc

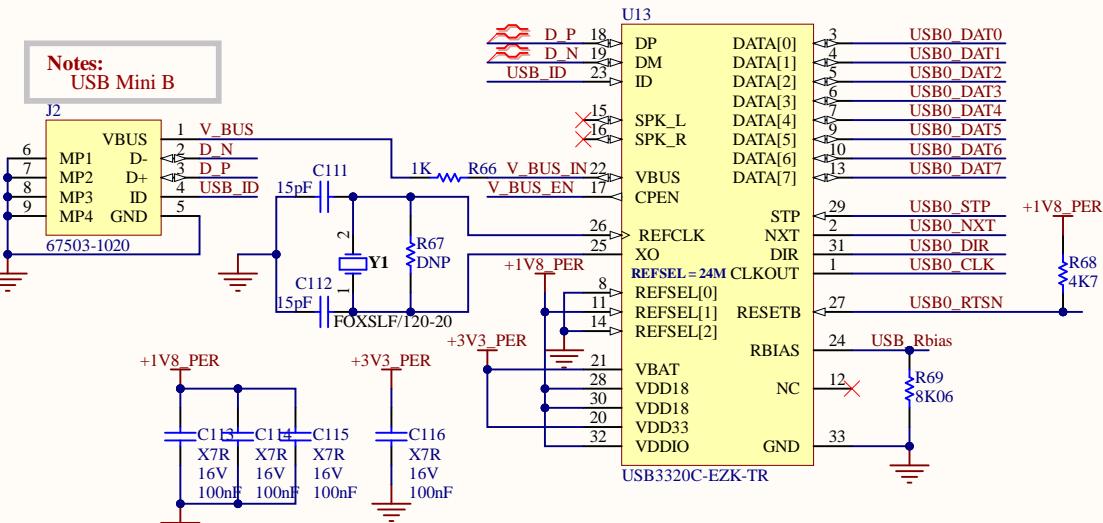
MIO0, MIO1, SD CARD, USB-OTG

SD Card



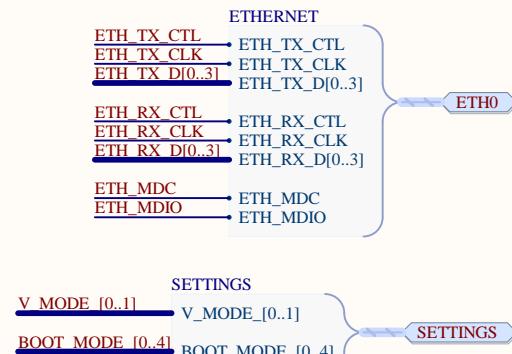
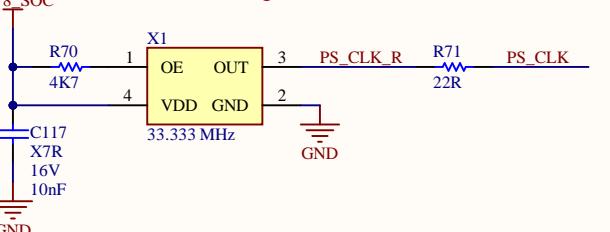
Notes:
SDIO is 4X Speed

USB OTG



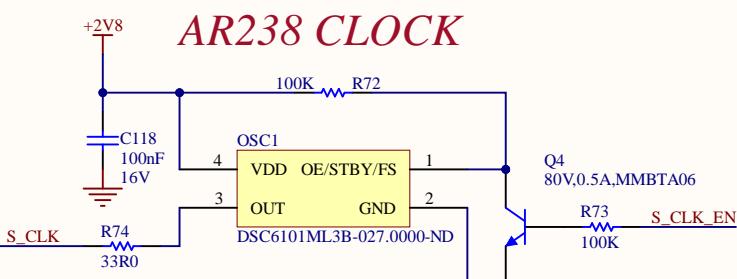
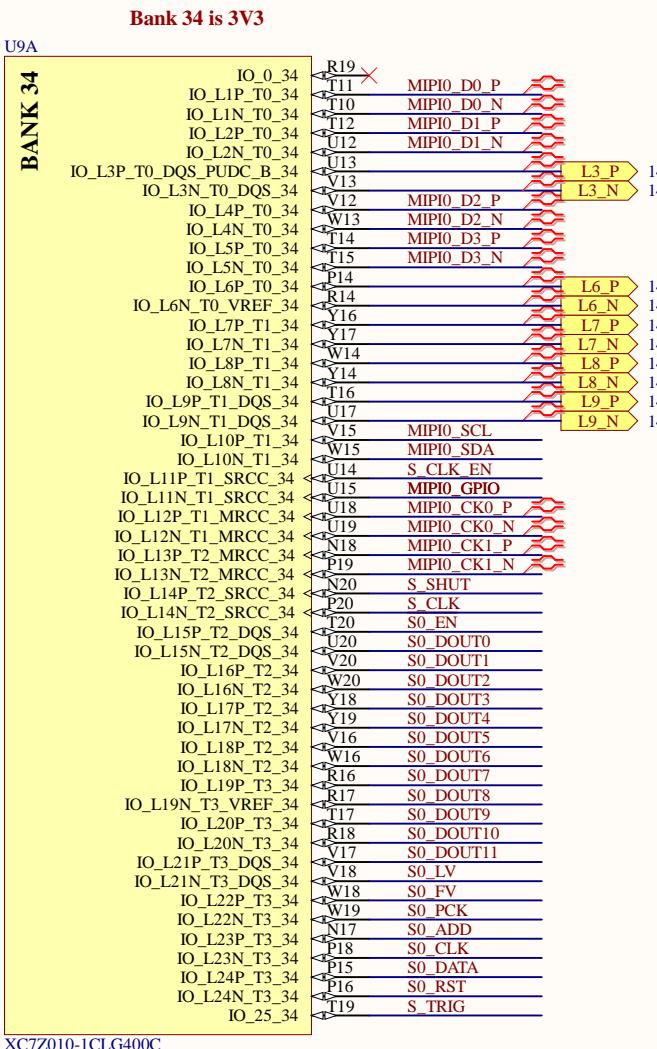
Notes:

33MHz Clock

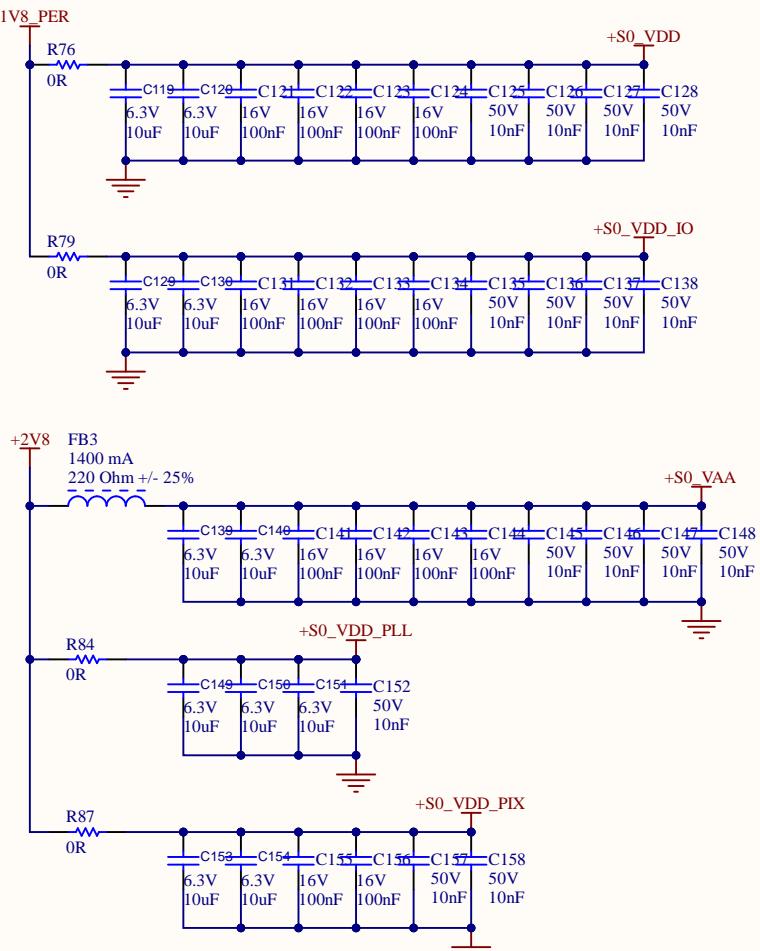


Title: MIO0, MIO1, SD CARD, USB-OTG	Mathew Locoteta 85 Artist Lake Dr. Middle Island New York, 11953
Size: B	Number: 7
Revision: V11	United States of America
Date: 11/30/2020	Time: 12:24:58 PM
File: C:\Users\Public\Documents\Altium\Projects\Zynq 7000 Demo\{7] - MIO0, MIO1, SD, USB, SchDoc	Sheet 7 of 16

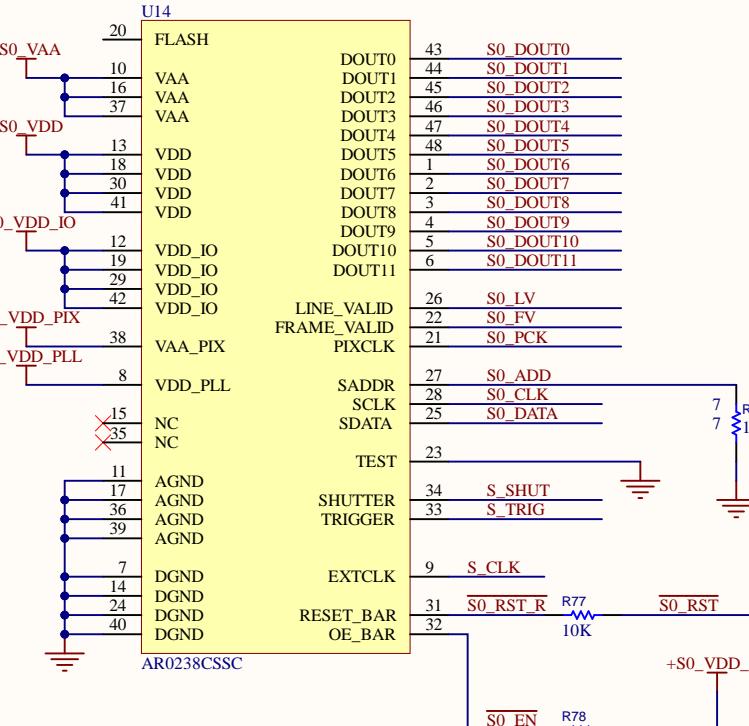
BANK 34, MIPI & AR238



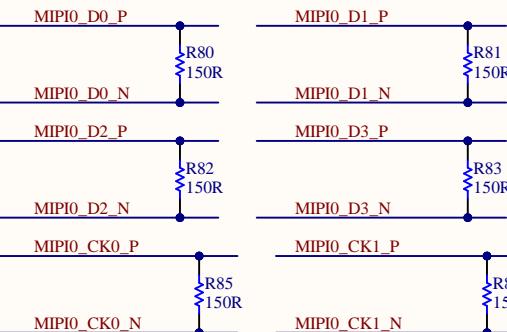
AR238 POWER



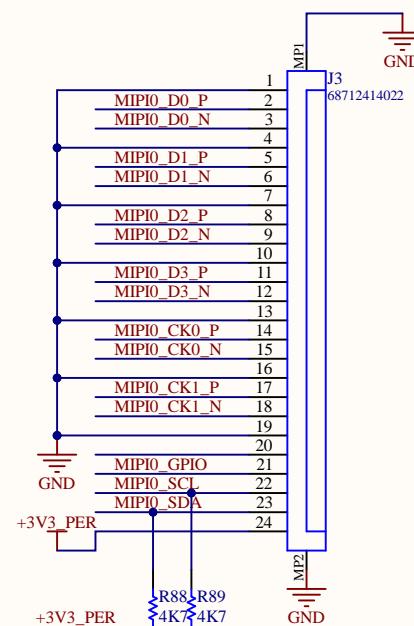
AR238 Image Sensor



MIPI Termination



4 Lane MIPI



Title **BANK 34, MIPI & AR238**

Mathew Locoteta
85 Artist Lake Dr.
Middle Island
New York, 11953

Size: **B** Number:8 Revision:V1II

United States of America

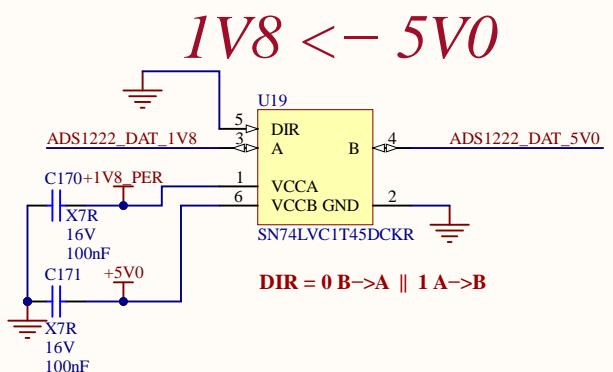
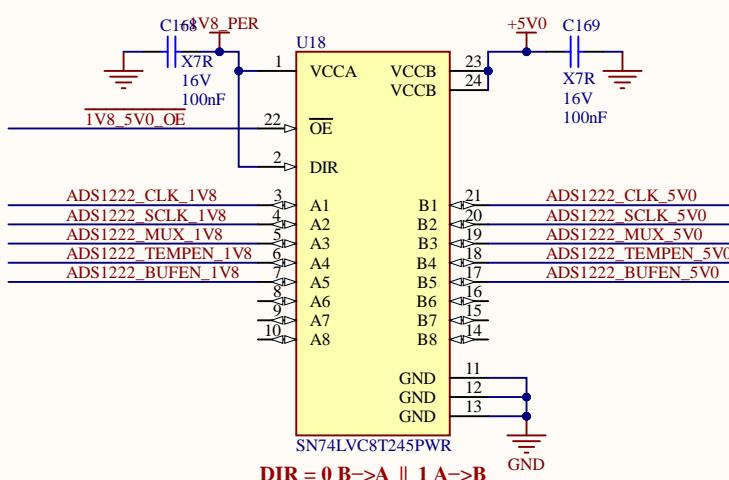
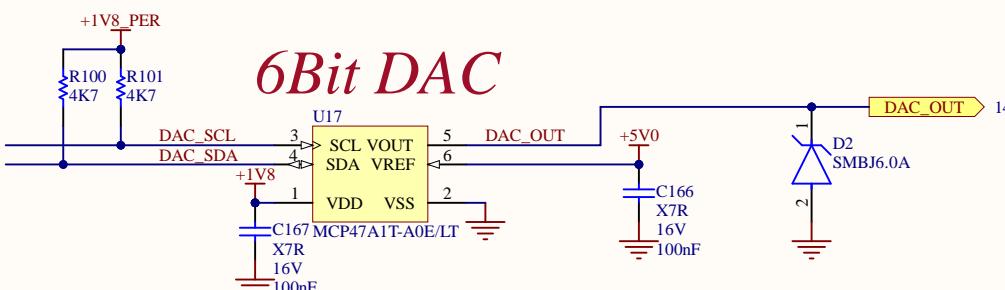
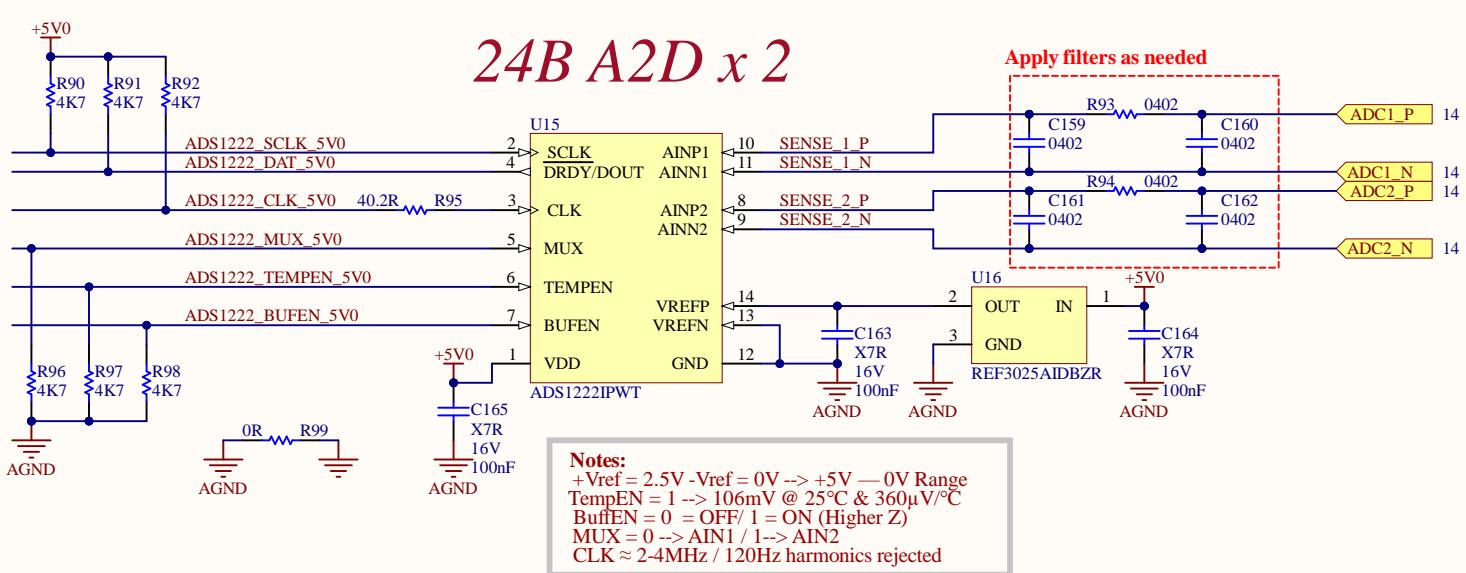
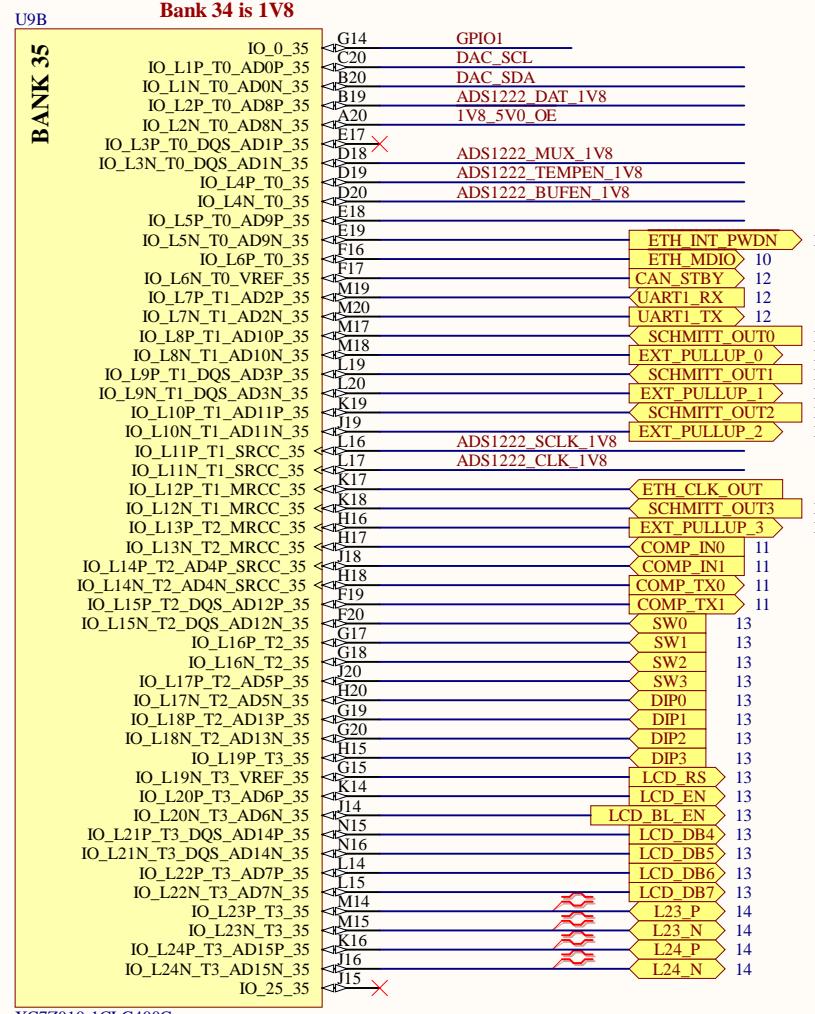
Date: 11/30/2020 Time: 12:24:58 PM Sheet 8 of 16

C:\Users\Public\Documents\Altium\Projects\Zynq 7000 Demo[8] - Z7010 B34, AR238, MIPI.SchDoc

File: C:\Users\Public\Documents\Altium\Projects\Zynq 7000 Demo[8] - Z7010 B34, AR238, MIPI.SchDoc

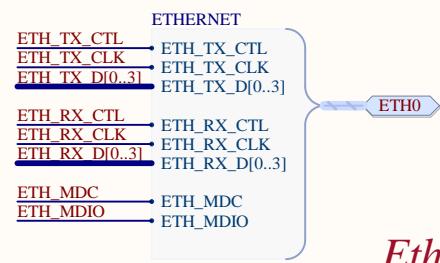
1 2 3 4 5 6

Z7010 B35, ADC, DAC

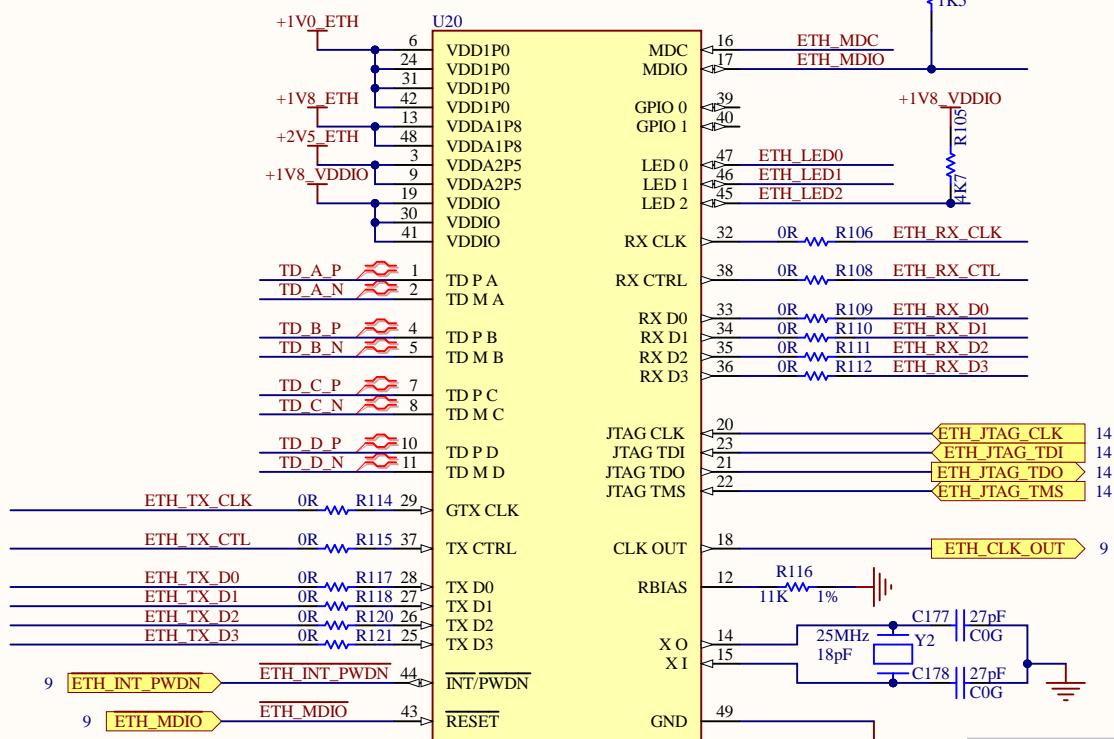


Title Z7010 B35, ADC, DAC		
Size: B	Number: 9	Revision: V1II
Date: 11/30/2020	Time: 12:24:58 PM	Sheet 9 of 16
File: C:\Users\Public\Documents\Altium\Projects\Zyneq 7000 Demo[9] - Z7010 B35, ADC, DAC.SchDoc		

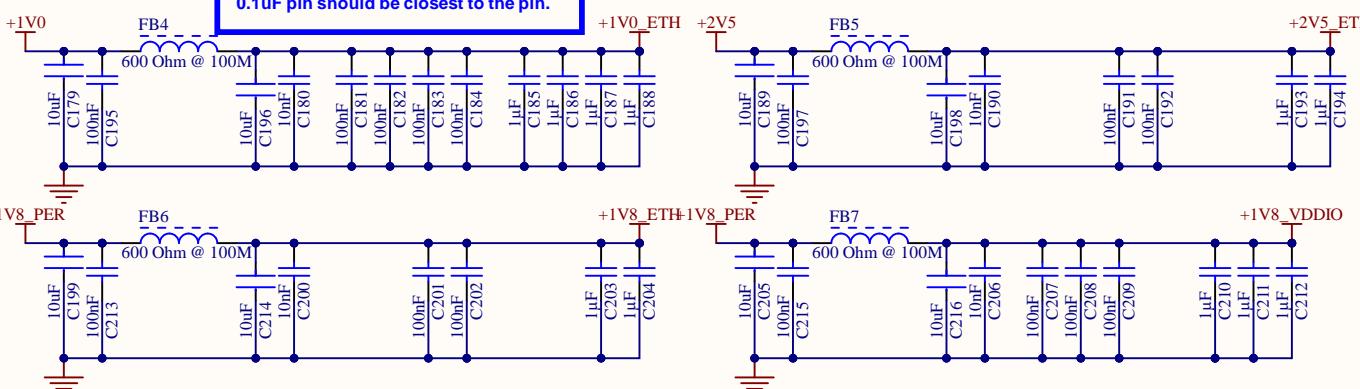
ETHERNET



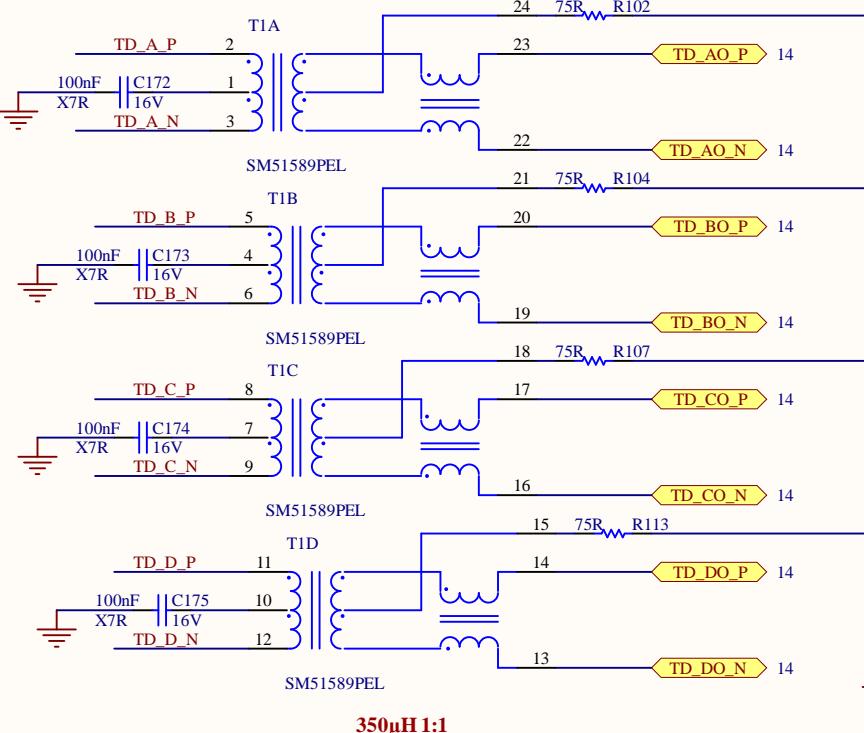
Eth Trans.



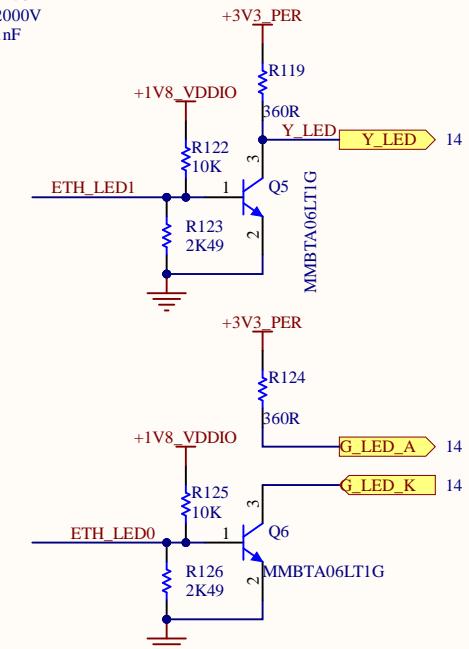
Eth Bypass



Eth XFMR



LED Control



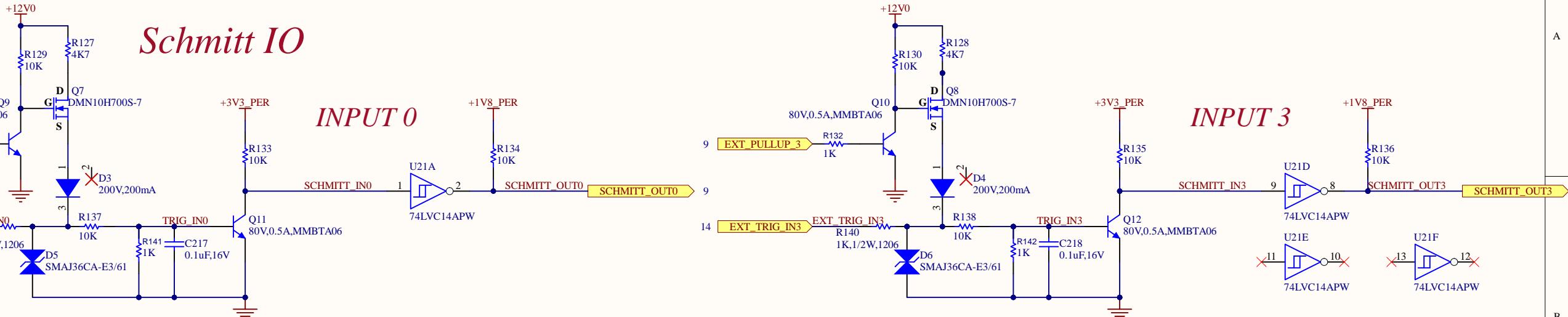
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Size: B	Number: 10	Revision: V1II
Date: 11/30/2020	Time: 12:24:58 PM	Sheet 10 of 16
File: C:\Users\Public\Documents\Altium\Projects\Zynq 7000 Demo\[10] - ETHERNET.SchDoc		

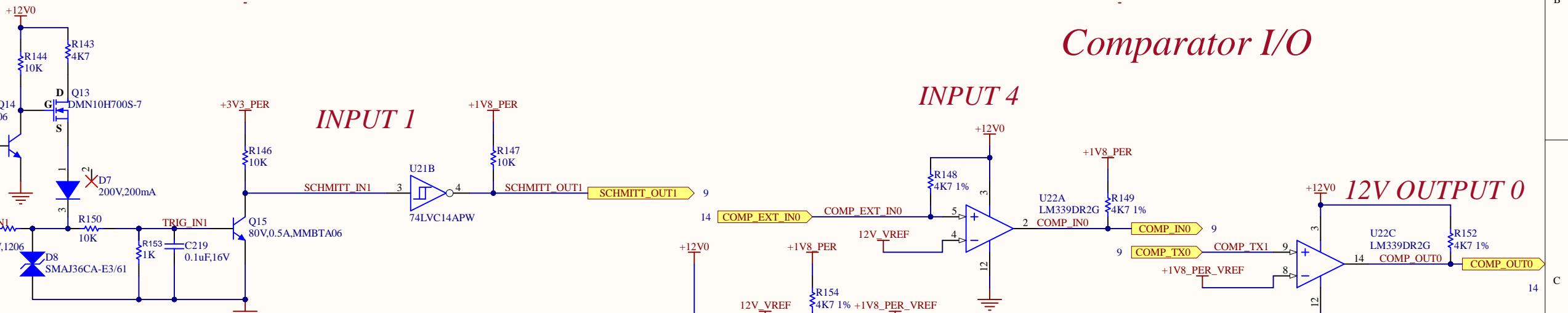
Mathew Locoteta
85 Artist Lake Dr.
Middle Island
New York, 11953
United States of America

PROTECTED IO

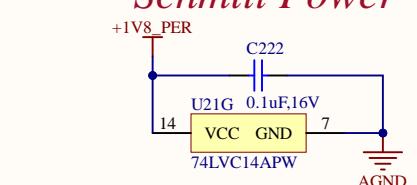
Schmitt IO



Comparator I/O

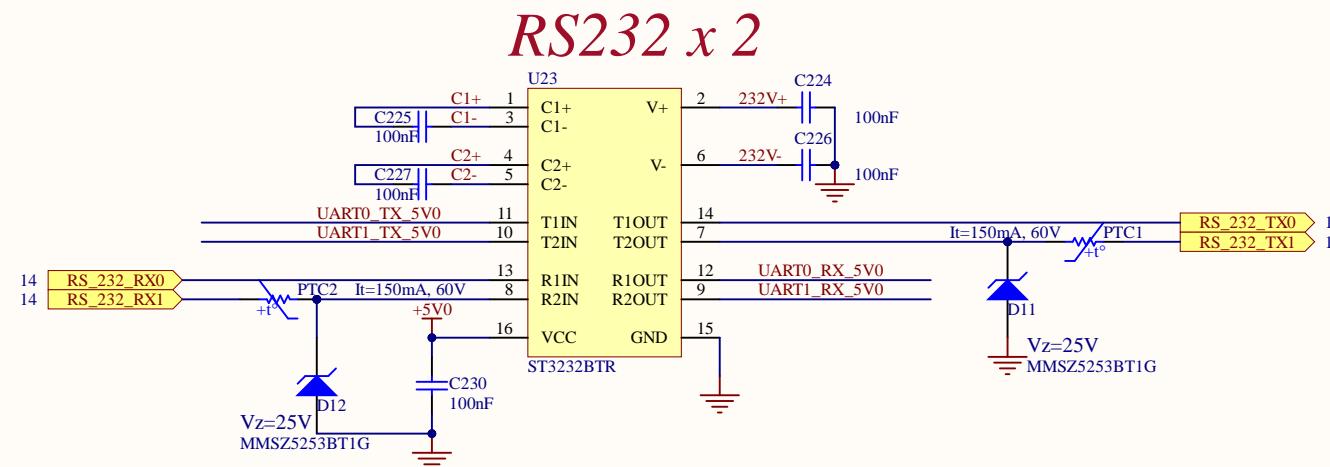


Schmitt Power

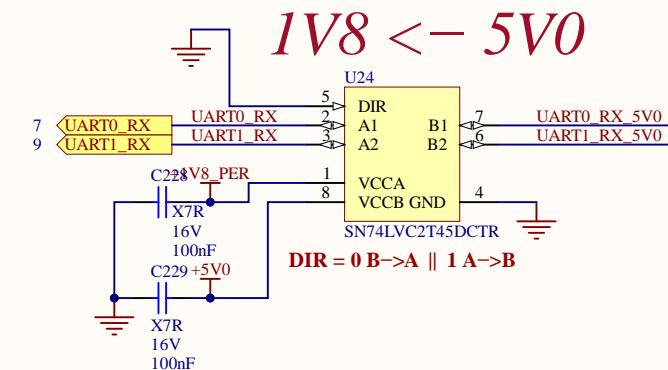


Title PROTECTED IO			Mathew Locoteta
Size: B	Number: 11	Revision: V1II	85 Artist Lake Dr.
Date: 11/30/2020	Time: 12:24:59 PM	Sheet 11 of 16	Middle Island
			New York, 11953
			United States of America
File: C:\Users\Public\Documents\Altium\Projects\Zynq 7000 Demo[11] - PROTECTED IO.SchDoc			

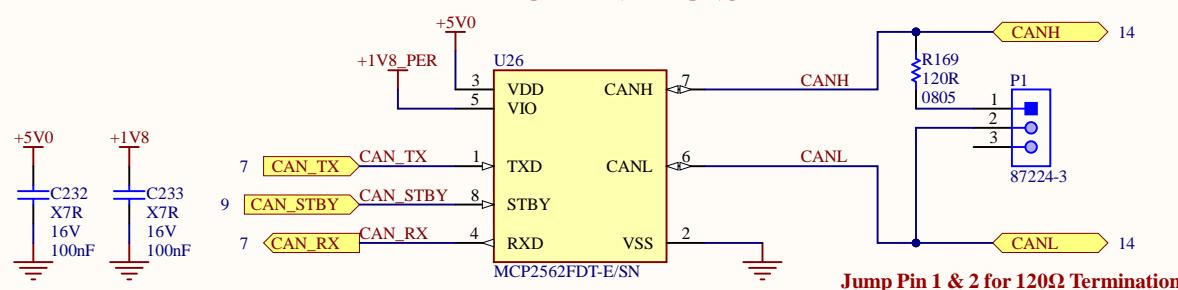
CAN & RS232



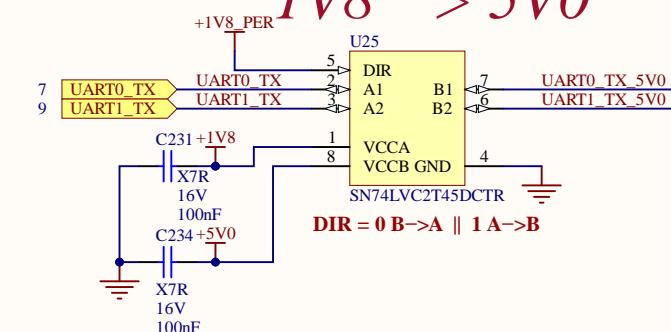
LEVEL SHIFTERS



CANBUS



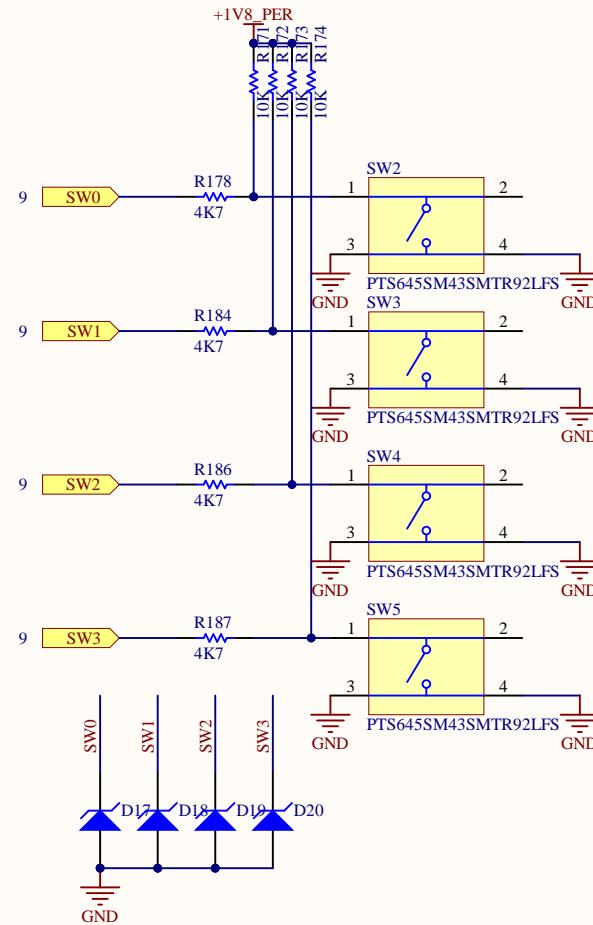
1V8 -> 5V0



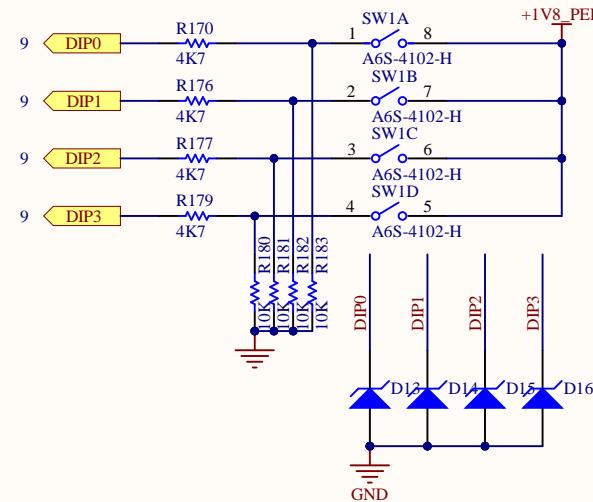
Title CAN & RS232			Mathew Locoteta
Size: B	Number: 12	Revision: V1II	85 Artist Lake Dr. Middle Island New York, 11953
Date: 11/30/2020	Time: 12:24:59 PM	Sheet 12 of 16	United States of America
File: C:\Users\Public\Documents\Altium\Projects\Zynq 7000 Demo\[12] - CAN & RS232.SchDoc			

HMI

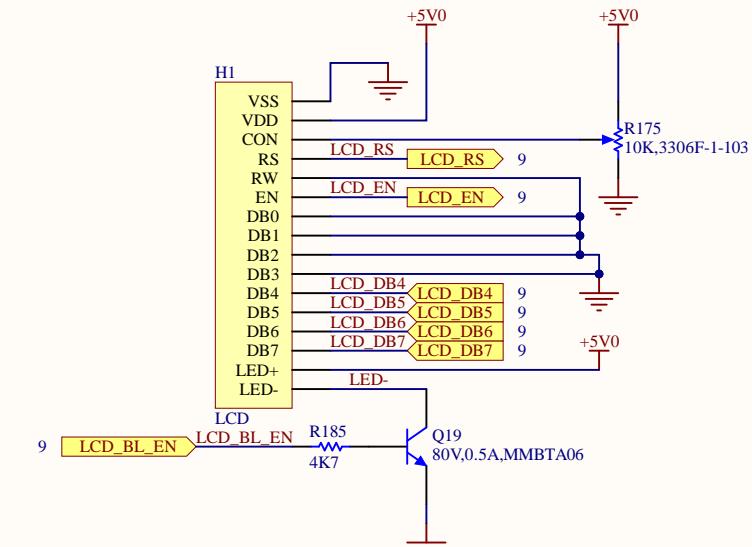
Push Buttons



DIP Switches

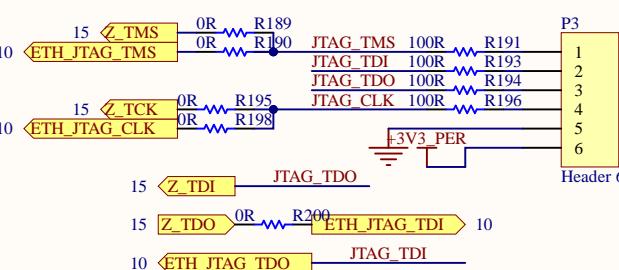


LCD

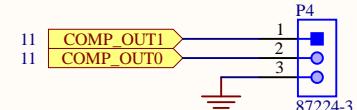


CONNECTORS

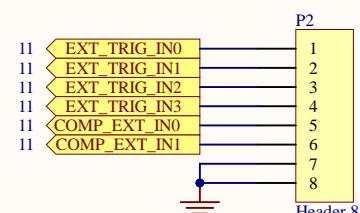
JTAG (Z7010 -> ETH)



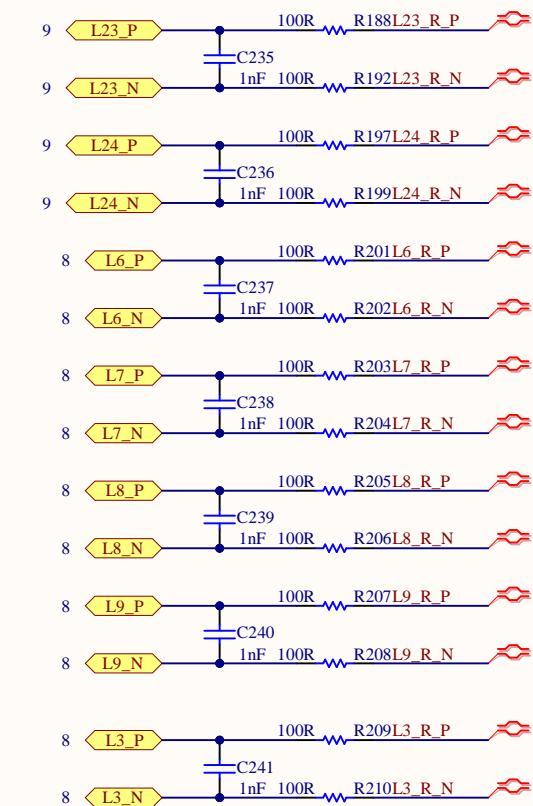
12V Comp Out



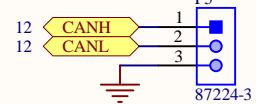
External Trig In



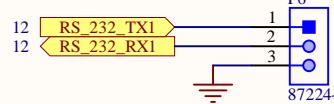
Differential Pairs



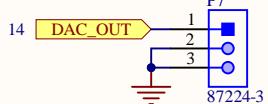
CAN



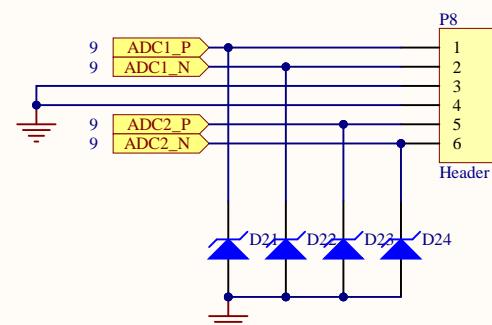
RS-232 -1



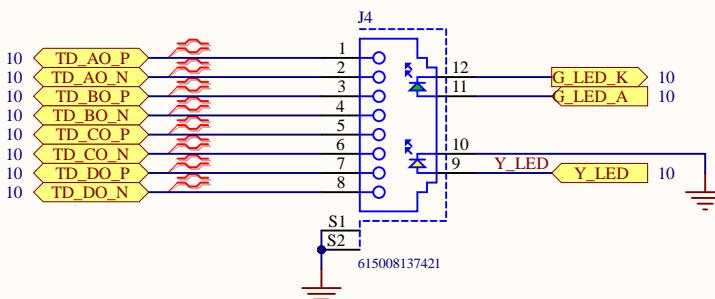
DAC OUT



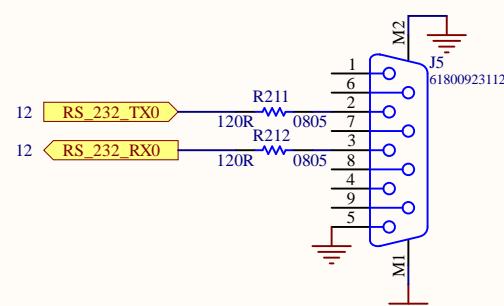
ADC1/ADC2



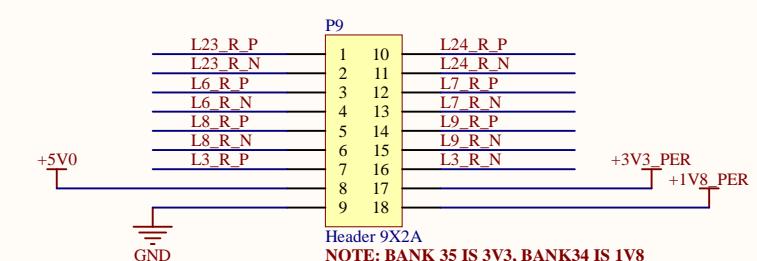
Ethernet Conn



RS-232 -0 DB9 Conn



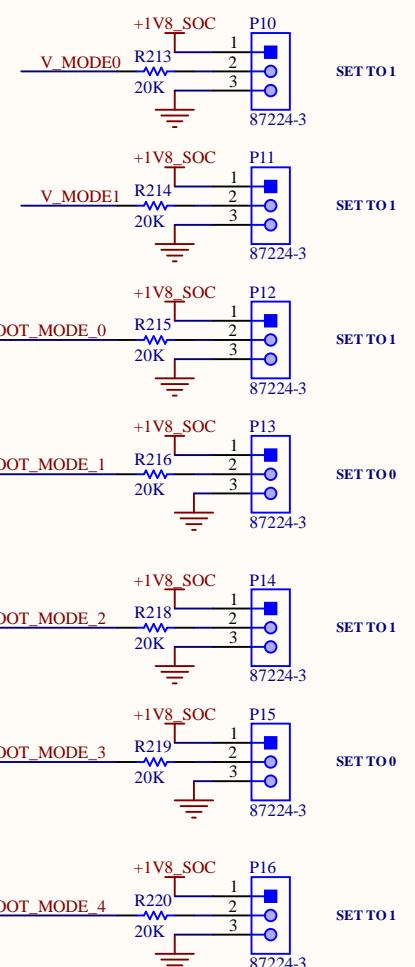
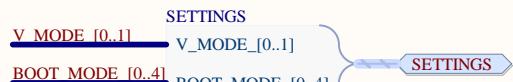
Diff Pair Conn



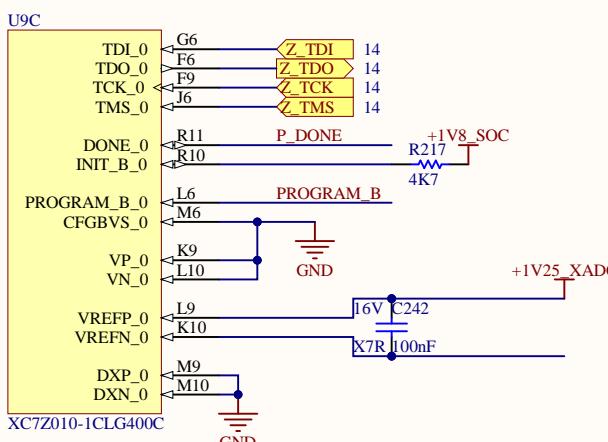
Title CONNECTORS			Mathew Locoteta 85 Artist Lake Dr. Middle Island New York, 11953 United States of America
Size: B	Number: 14	Revision: V1II	
Date: 11/30/2020	Time: 12:24:59 PM	Sheet 14 of 16	
File: C:\Users\Public\Documents\Altium\Projects\Zynq 7000 Demo\14 - CONNECTORS.SchDoc			

BOOT OPTIONS

CONFIG



BANK 0



PROG. BUTTON

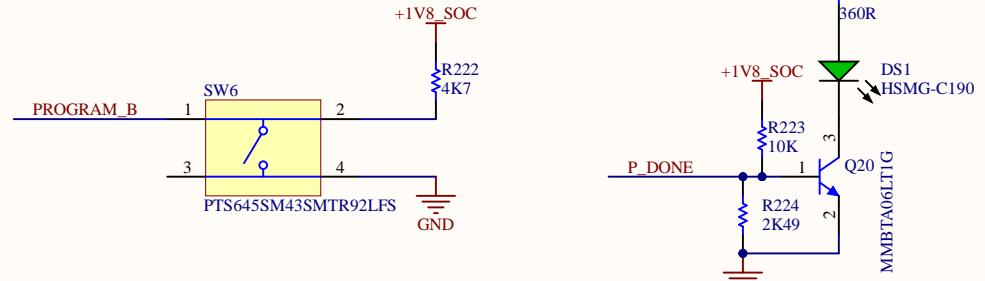


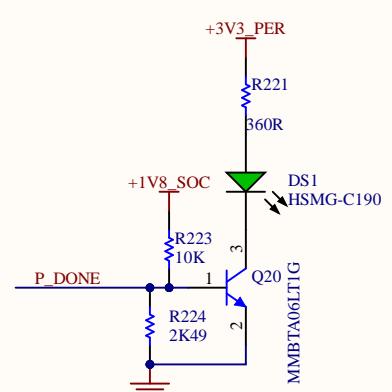
Table 6-4: Boot Mode MIO Strapping Pins

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]					
	VMODE[1]	VMODE[0]	BOOT_MODE[4]	BOOT_MODE[0]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[3]					
Boot Devices												
JTAG Boot Mode; cascaded is most common ⁽¹⁾	0	0	0									
NOR Boot ⁽³⁾	0	0	1									
NAND	0	1	0									
Quad-SPI ⁽³⁾	1	0	0									
SD Card	1	1	0									
Mode for all 3 PLLs												
PLL Enabled			0	Hardware waits for PLL to lock, then executes BootROM.								
PLL Bypassed			1	Allows for a wide PS_CLK frequency range.								
MIO Bank Voltage⁽⁴⁾												
	Bank 1	Bank 0	Voltage Bank 0 includes MIO pins 0 thru 15.									
2.5 V, 3.3 V	0	0	Voltage Bank 1 includes MIO pins 16 thru 53.									
1.8 V	1	1										

Notes:

1. JTAG cascaded mode is most common and is the assumed mode in all the references to JTAG mode except where noted.
2. For secure mode, JTAG is not enabled and MIO[2] is ignored.
3. The Quad-SPI and NOR boot modes support execute-in-place (this support is always non-secure)
4. Voltage Banks 0 and 1 must be set to the same value when an interface spans across these voltage banks. Examples include NOR, 16-bit NAND, and a wide TPIU test port. Other interface configuration may also span the two banks.

DONE LED



Title: BOOT OPTIONS	Mathew Locoteta
Size: B	Number: 15
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REVISION HISTORY

Page	Change	Date	Rev
.....
ALL	Preliminary schematic release	11/30/2020	1.00

Page	To Do	Rev
.....
ALL	Check power requirements: ripple, current, power tree	1.01

Title: DOC REVISION HISTORY			Mathew Locoteta 85 Artist Lake Dr. Middle Island New York, 11953
Size: B	Number: 16	Revision: V1II
Date: 11/30/2020	Time: 12:25:00 PM	Sheet 16 of 16	United States of America
File: C:\Users\Public\Documents\Altium\Projects\Zyneq 7000 Demo[16] - DOC REV HISTORY.SchDoc			