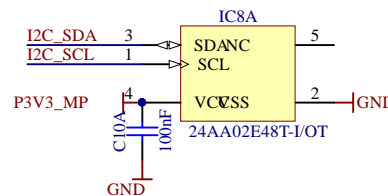
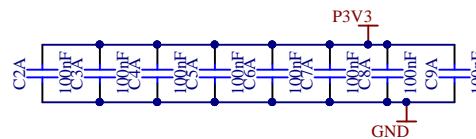
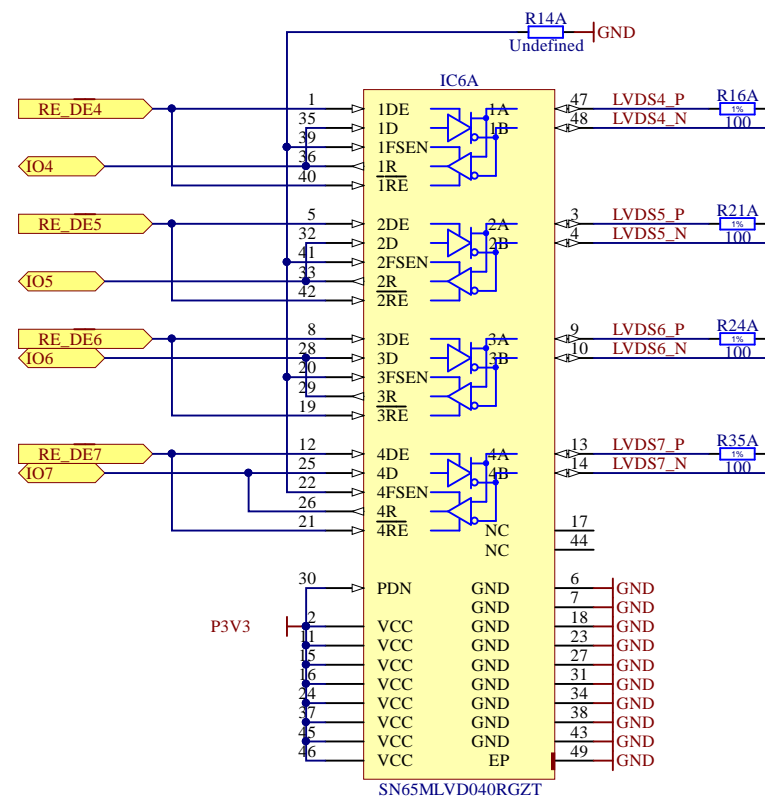
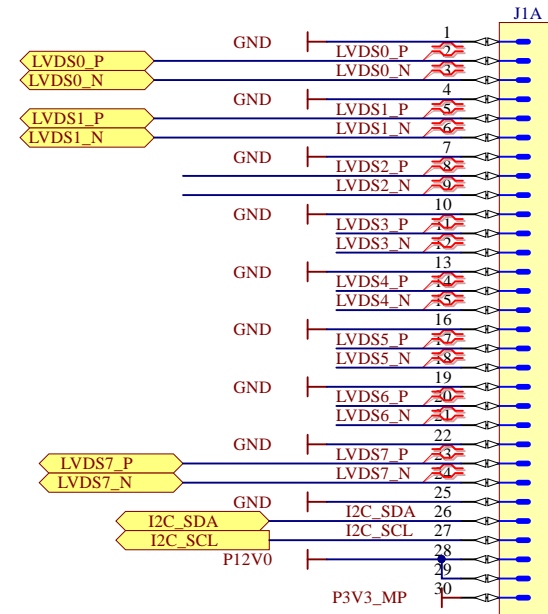
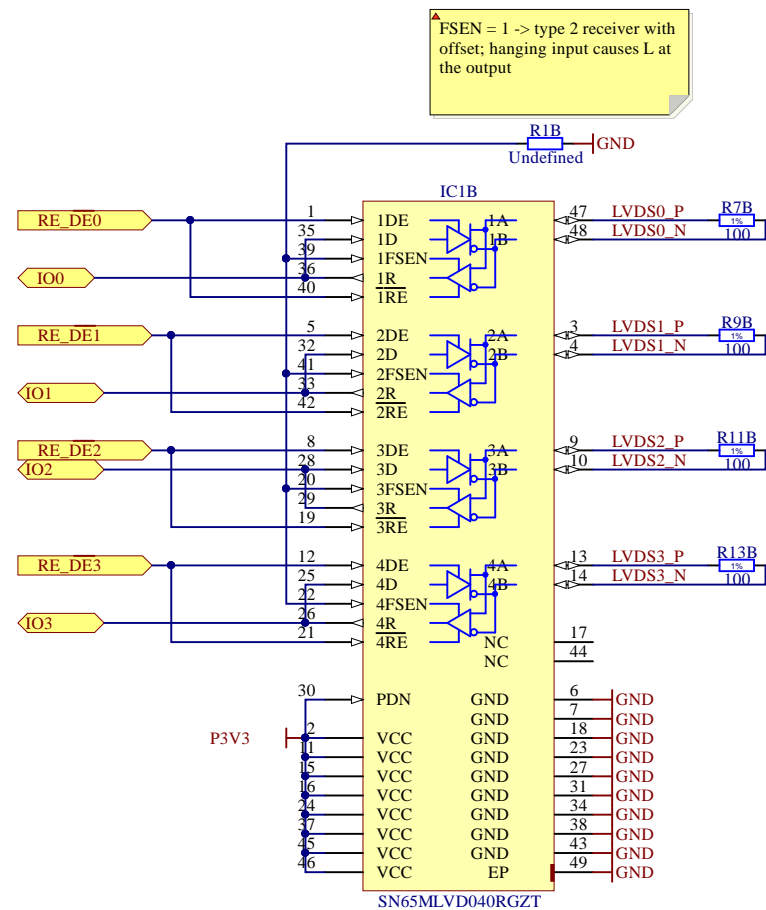
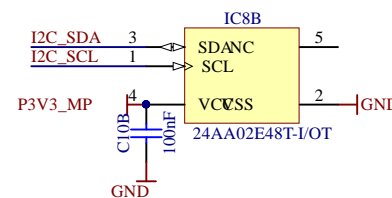
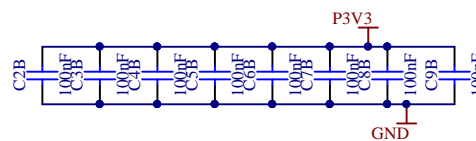
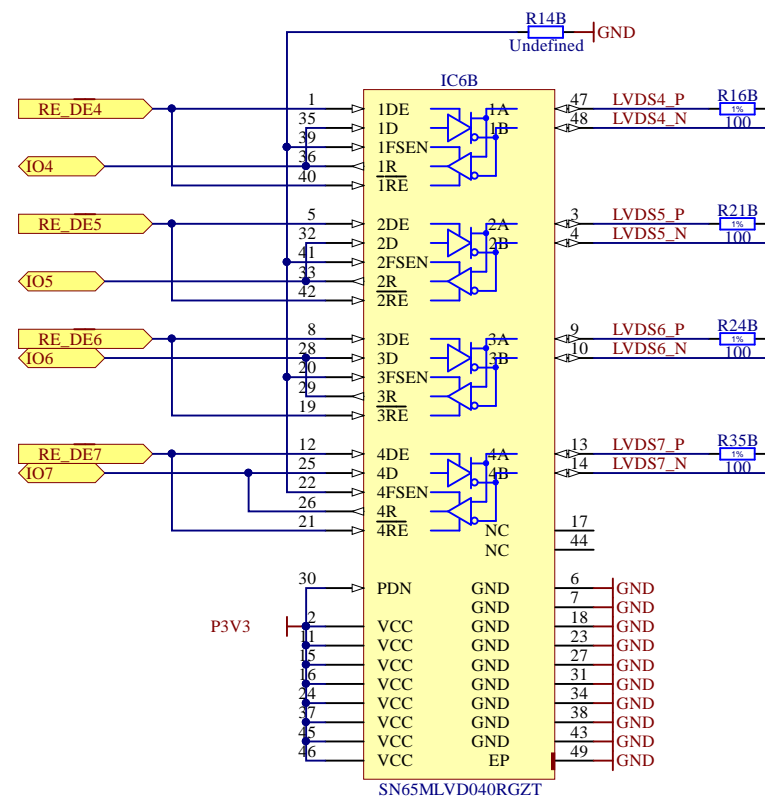
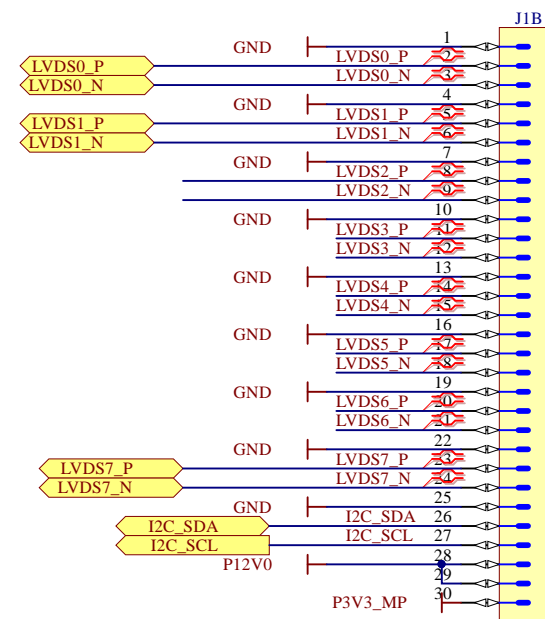


EEM Connector
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A





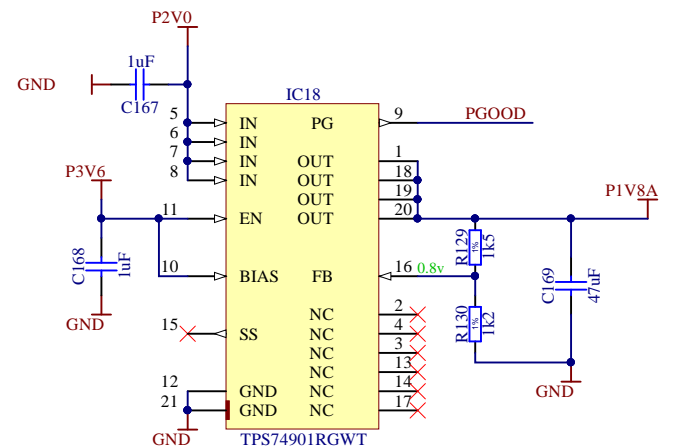
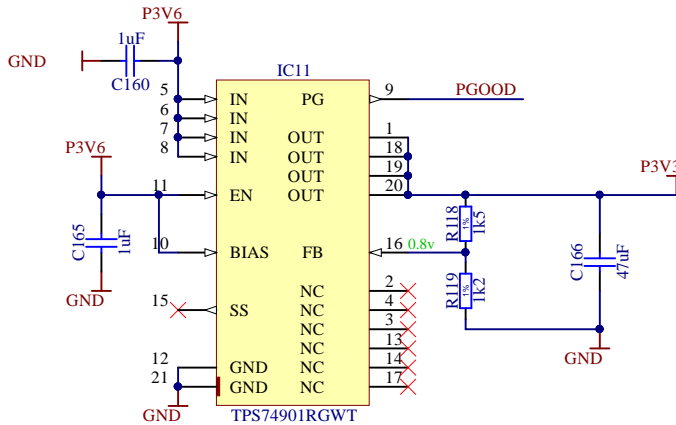
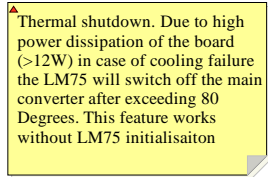
EEM Connector
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I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A



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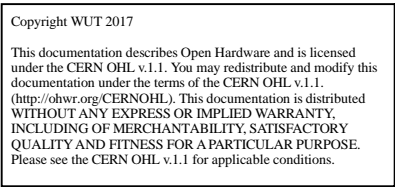
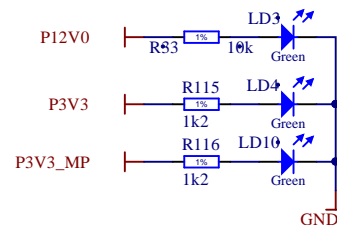
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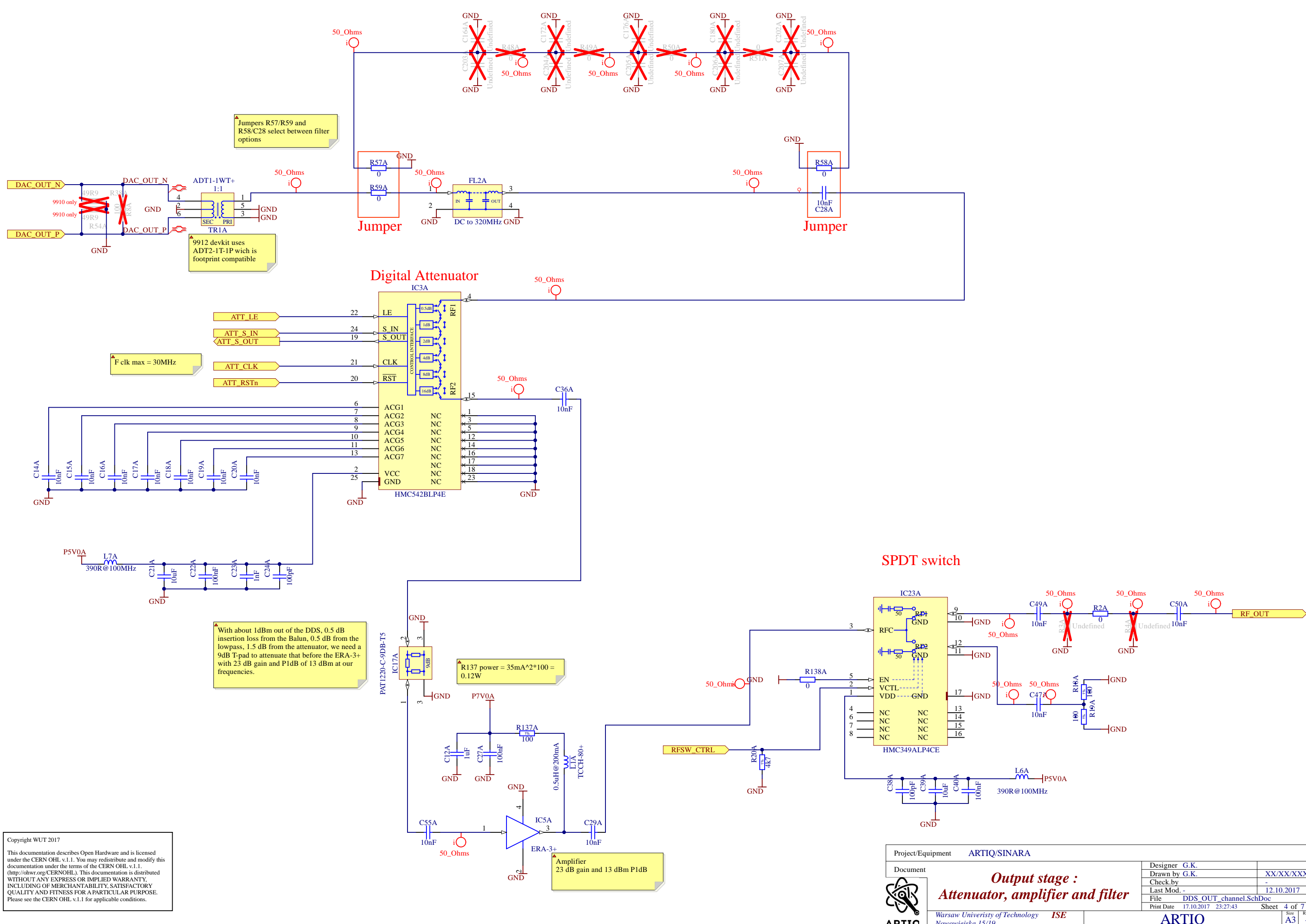
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Document	LVDS to LVTTL interface & EEM connector	
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Drawn by	G.K.	-
Check by	-	17.10.2017
Last Mod.	-	-
File	LVDS_IFC_DDS.SchDoc	Sheet 2 of 7
Print Date	17.10.2017 23:27:42	Size A3 Rev -
Warsaw University of Technology ISE Nowowiejska 15/19		ARTIQ



Power budget (max ratings):	AD9912 variant(mA)	AD9910 variant(mA)
P3V3:		
LVDS interface 4x	660	660
LVDS load 4x24mA	96	96
CPLD	100	100
Si53312-B-GM	240	240
Si453304	-	100
DDS AVDD3	4*(9,(6+31))=133,6	4*29=116
DDS DVDDIO	4*3=12	4*11=44
TOTAL P3V3	1121	1246
TOTAL POWER	3.7	3.9
P1V8:		
DDS AVDD	4*(48+136)=736	4*110=440
DDS DVDD	4*246=984	4*222=888
TOTAL P1V8	1720	1328
TOTAL POWER	3,096	2.39
P5V0		
HMC542BLP4E	4*2.9=11.6	4*2.9=11.6
HMC349LP4C	4*3.5=14	4*3.5=14
TOTAL 5V0	25.6	25.6
TOTAL POWER	0,125	0,125
P7V0		
ERA-3XSM+	4*35=150	4*35=150
TOTAL POWER	1.05	1.05
DC/DC converter losses		
TPS62175 eff. .95	0,05*(.27+0,026)*7,5=0.11	0,05*(.27+0,026)*7,5=0.11
LTM:3.6V eff. .9	0.1*1,321*3,6=0,47	0.1*1,346*3,6=0,48
LTM:2V eff. .87	0.13*1,721*2=0,44	0.13*1.328*2=0.34
LDO losses		
2V->1.8V	0.34	0,26
3.6V->3.3V	0.396	0.4
7.5V->7V	0.135	0.135
7.5V->5V	0,064	0,064
Total power from 12V 9.95W		9.05
Total current from 12V 0.83A		0.75A

- | | | |
|---------|--|------|
| P1V8A | | TP10 |
| P2V0 | | TP11 |
| P3V3 | | TP12 |
| P3V3A | | TP13 |
| P3V3_MP | | TP14 |
| P3V6 | | TP15 |
| P5V0A | | TP16 |
| P7V0A | | TP17 |
| P12V0 | | TP18 |



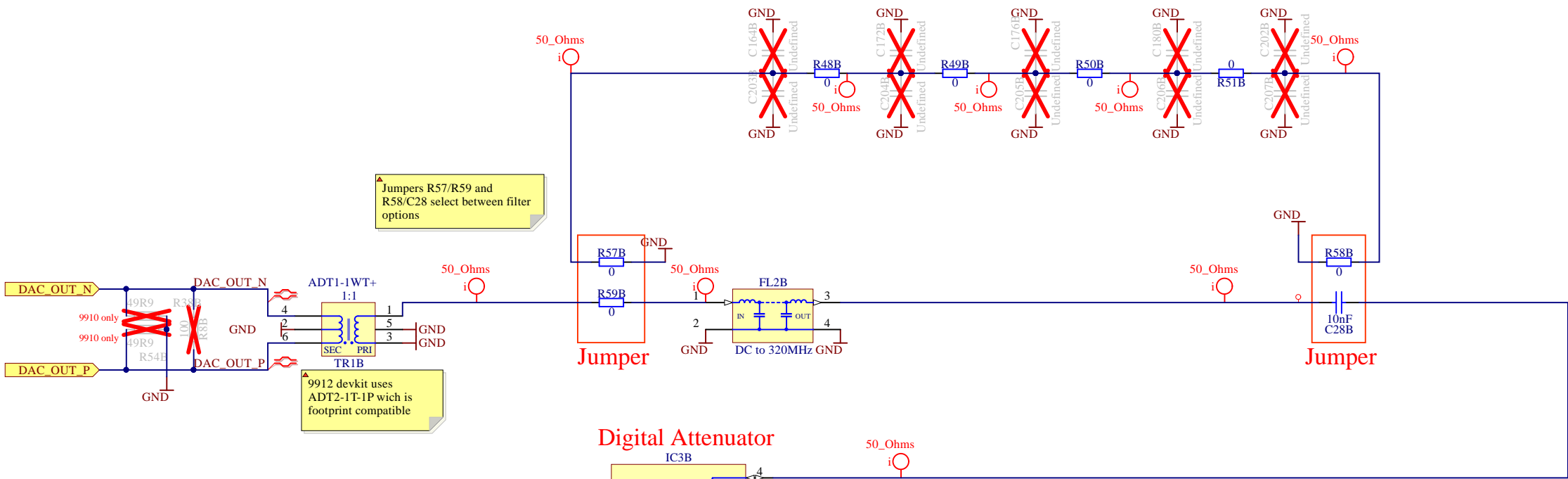


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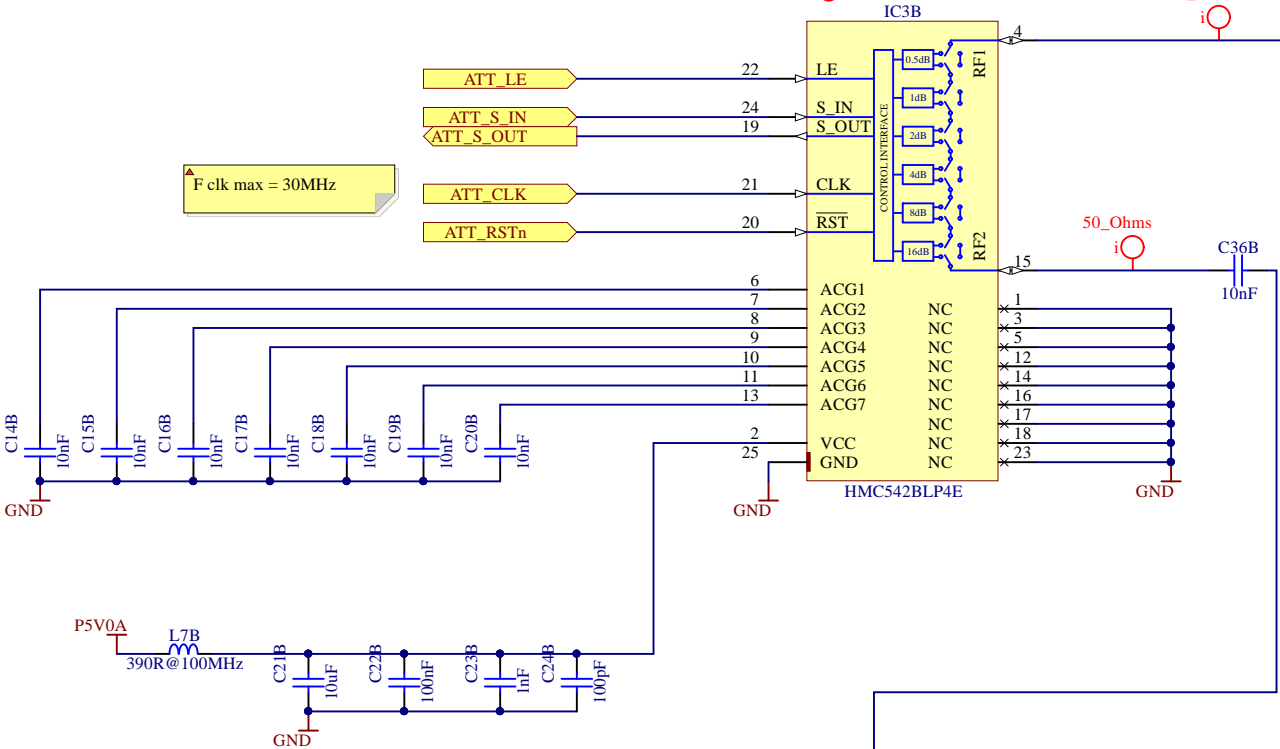
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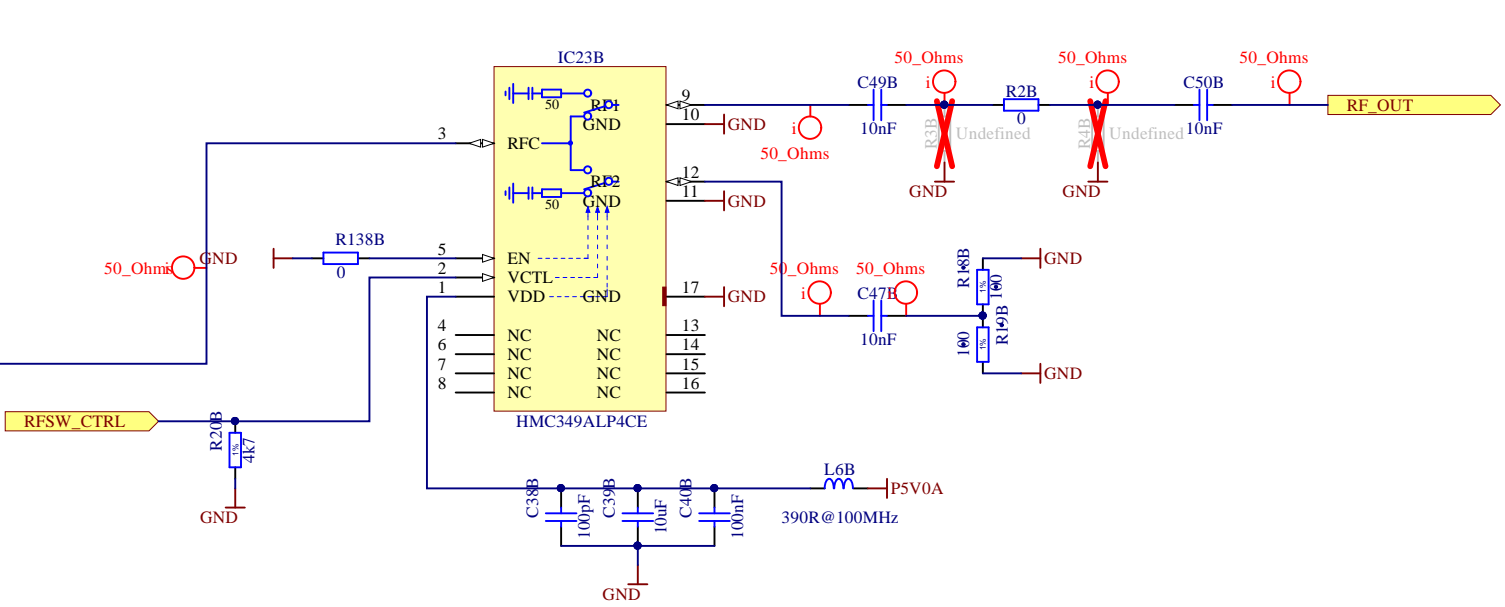
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Digital Attenuator

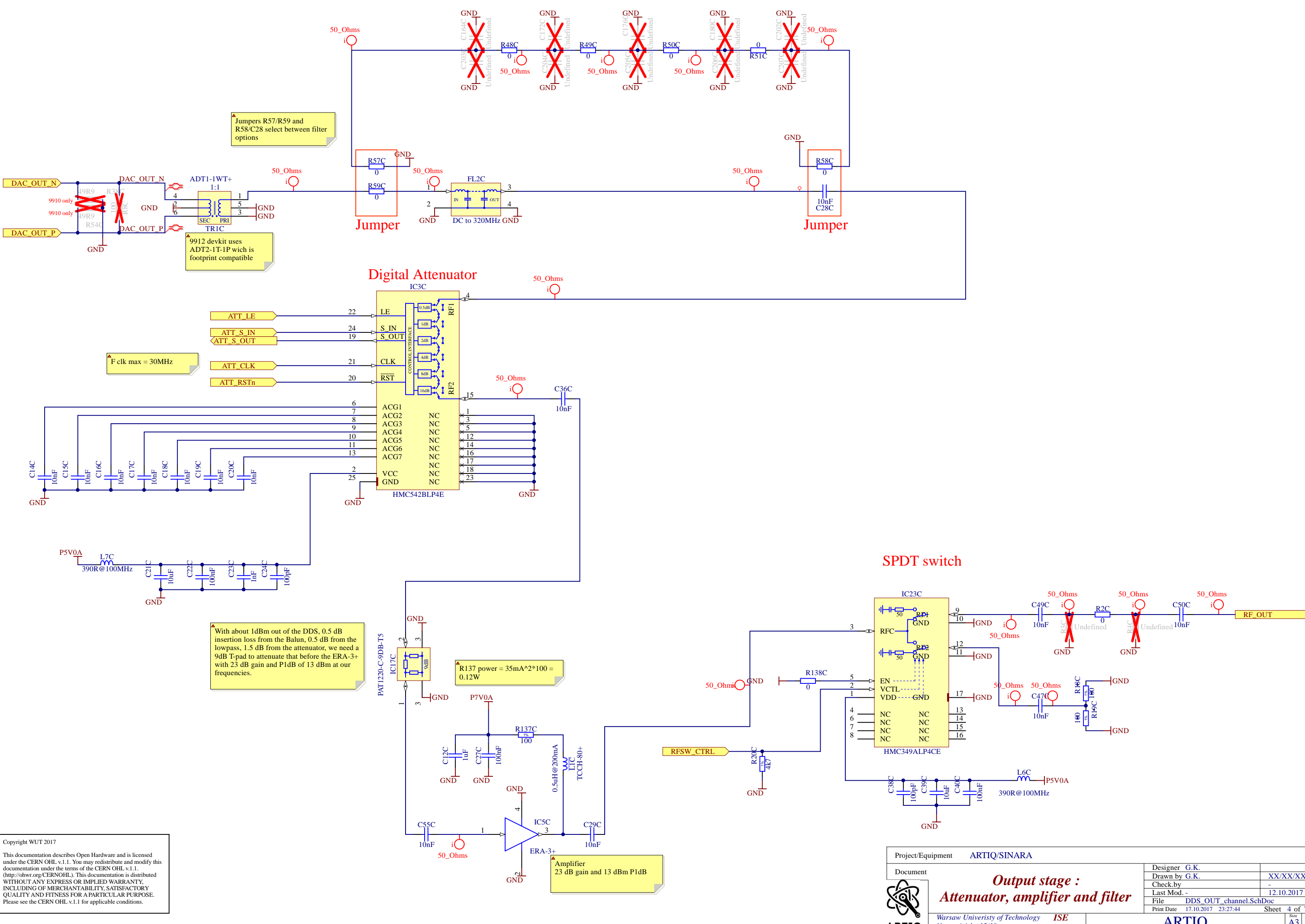


SPDT switch



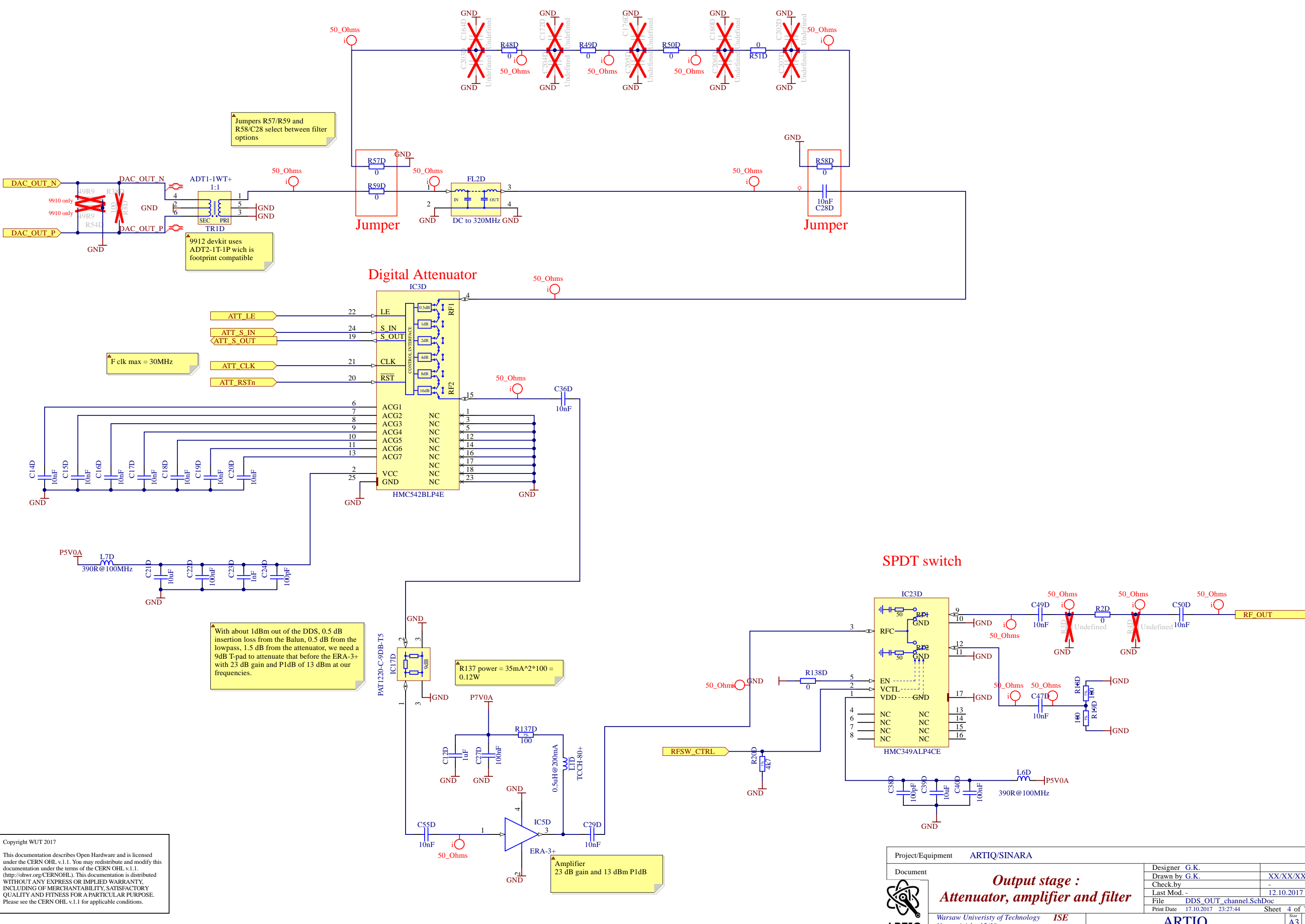
Output stage :
Attenuator, amplifier and filter

Project/Equipment	ARTIQ/SINARA		
Document			
Designer	G.K.		
Drawn by	G.K.		XX/XX/XXXX
Check by	-		-
Last Mod.	-		12.10.2017
File	DDS_OUT_channel.SchDoc		
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Warsaw University of Technology ISE		ARTIQ	
Nowowiejska 15/19		Size	A3
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Project/Equipment		ARTIQ/SINARA	
Document		Output stage : Attenuator, amplifier and filter	
Designer		G.K.	
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Size		A3	
Rev		-	



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ARTIQ

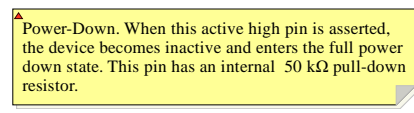
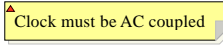
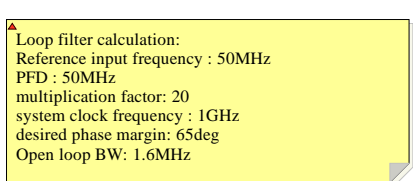
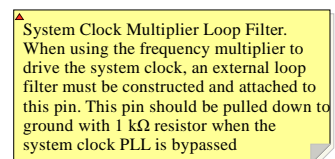
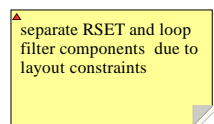
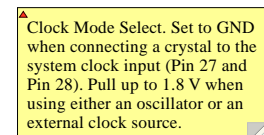
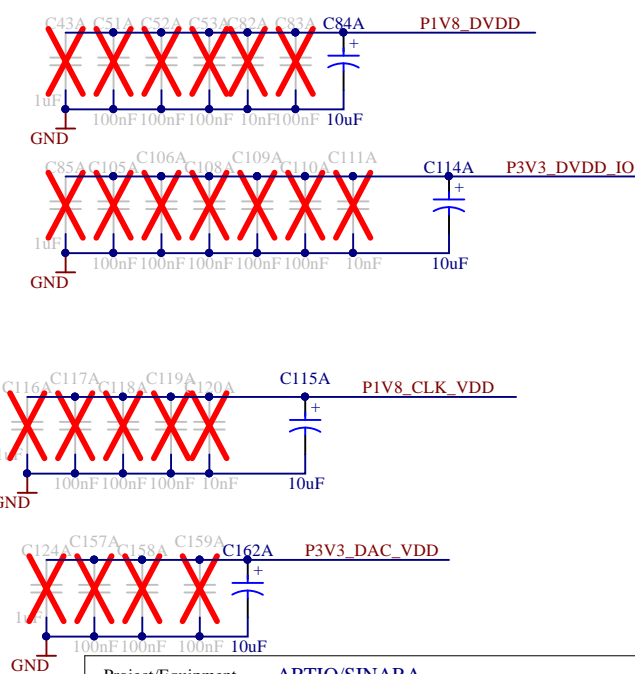
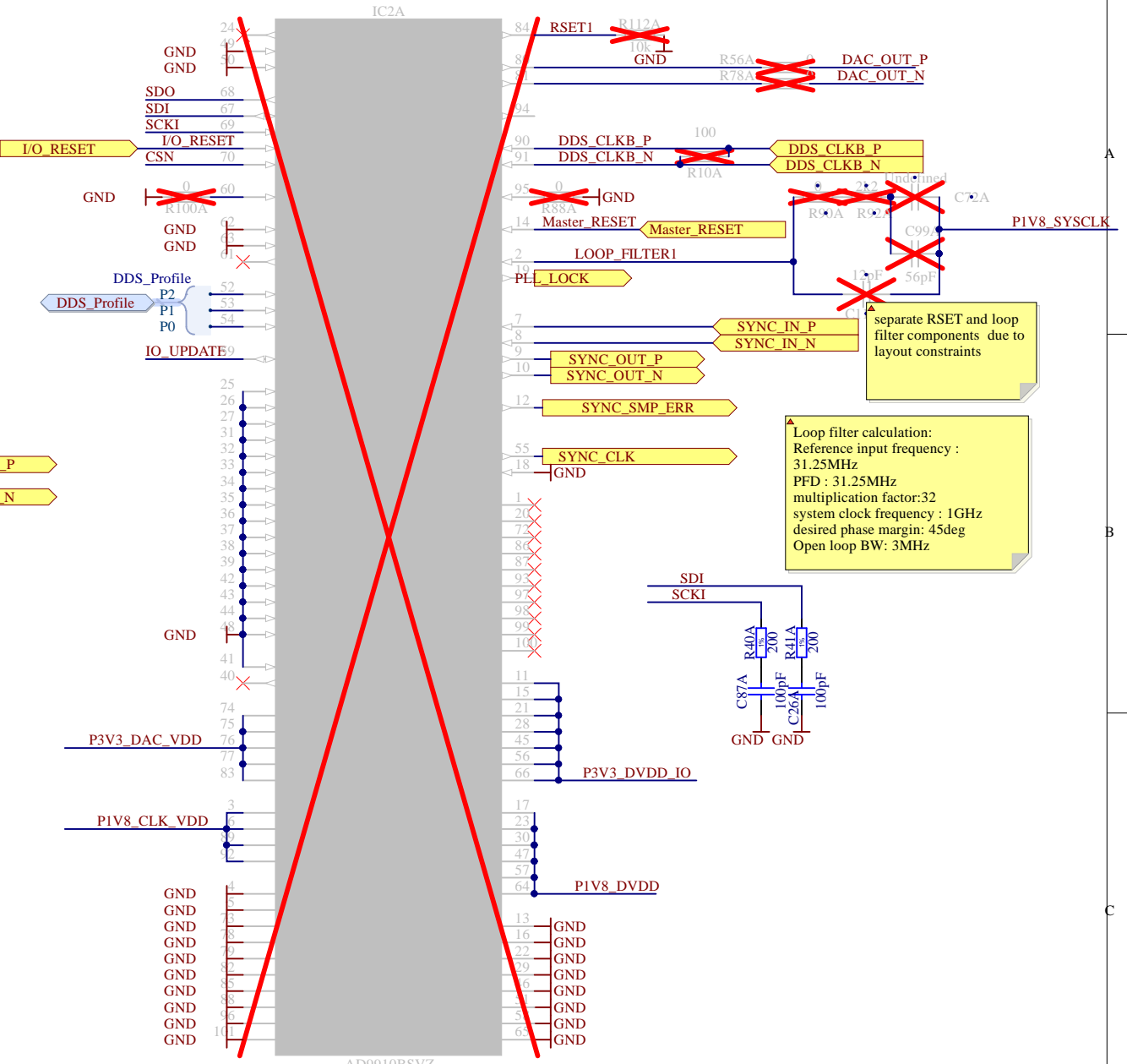
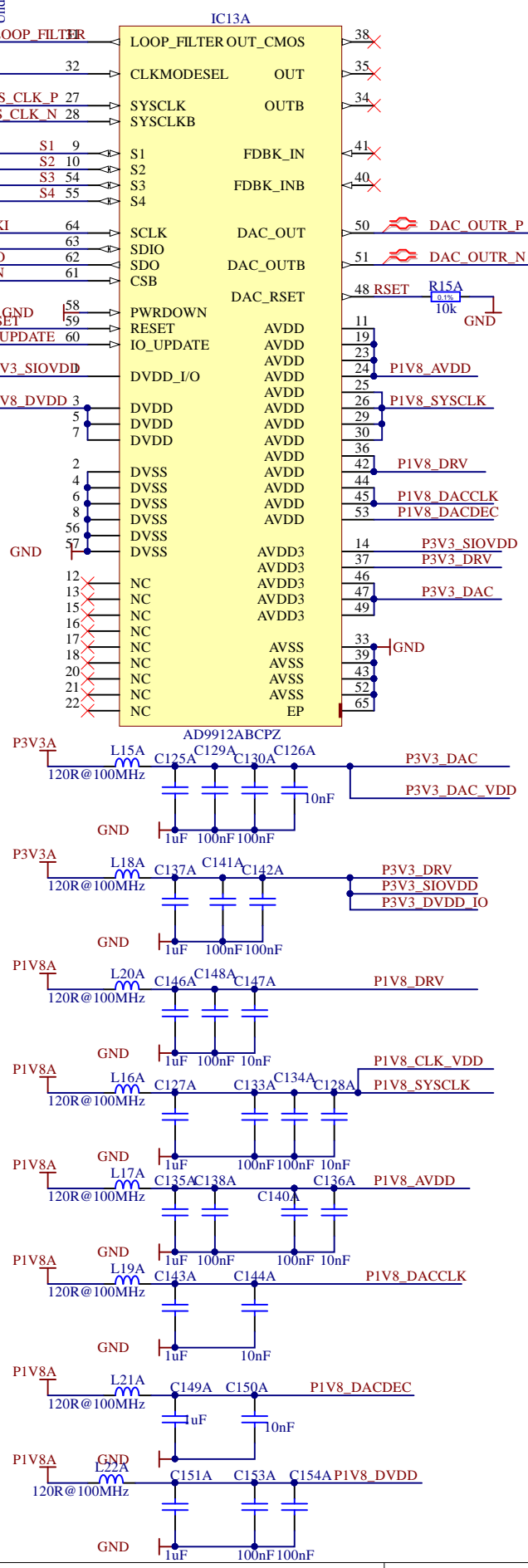


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758



Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Loop filter calculation:
Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

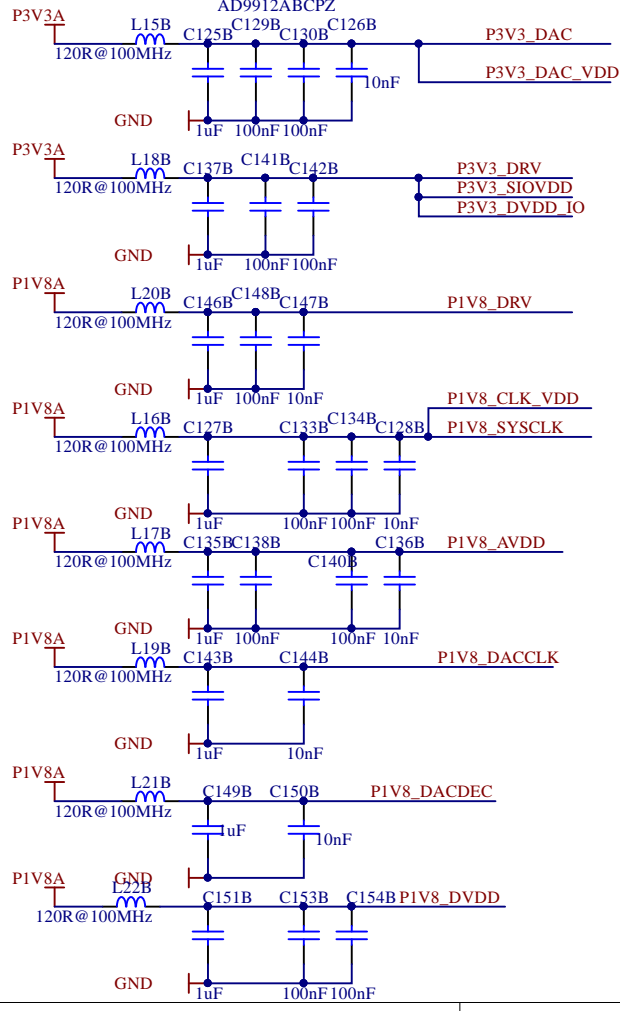
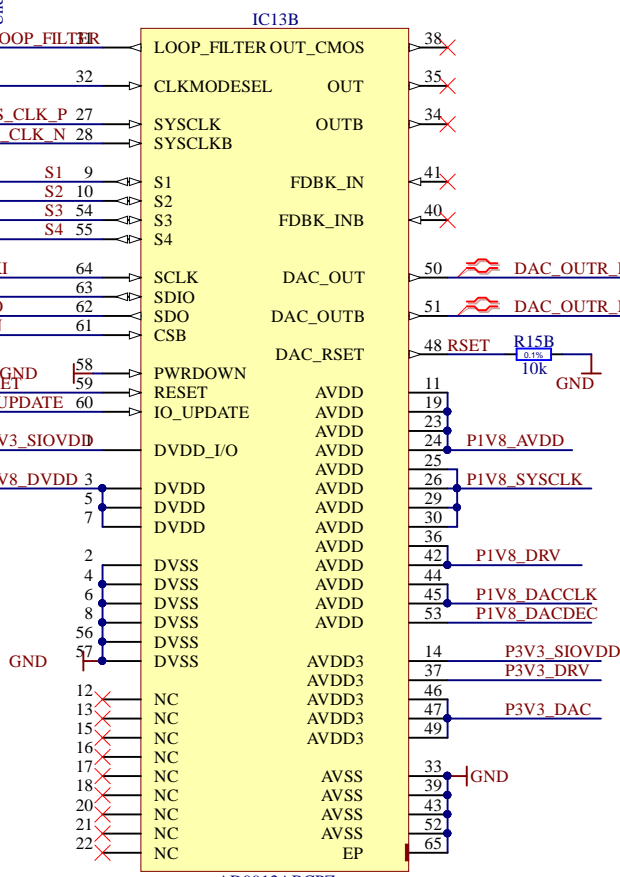
Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

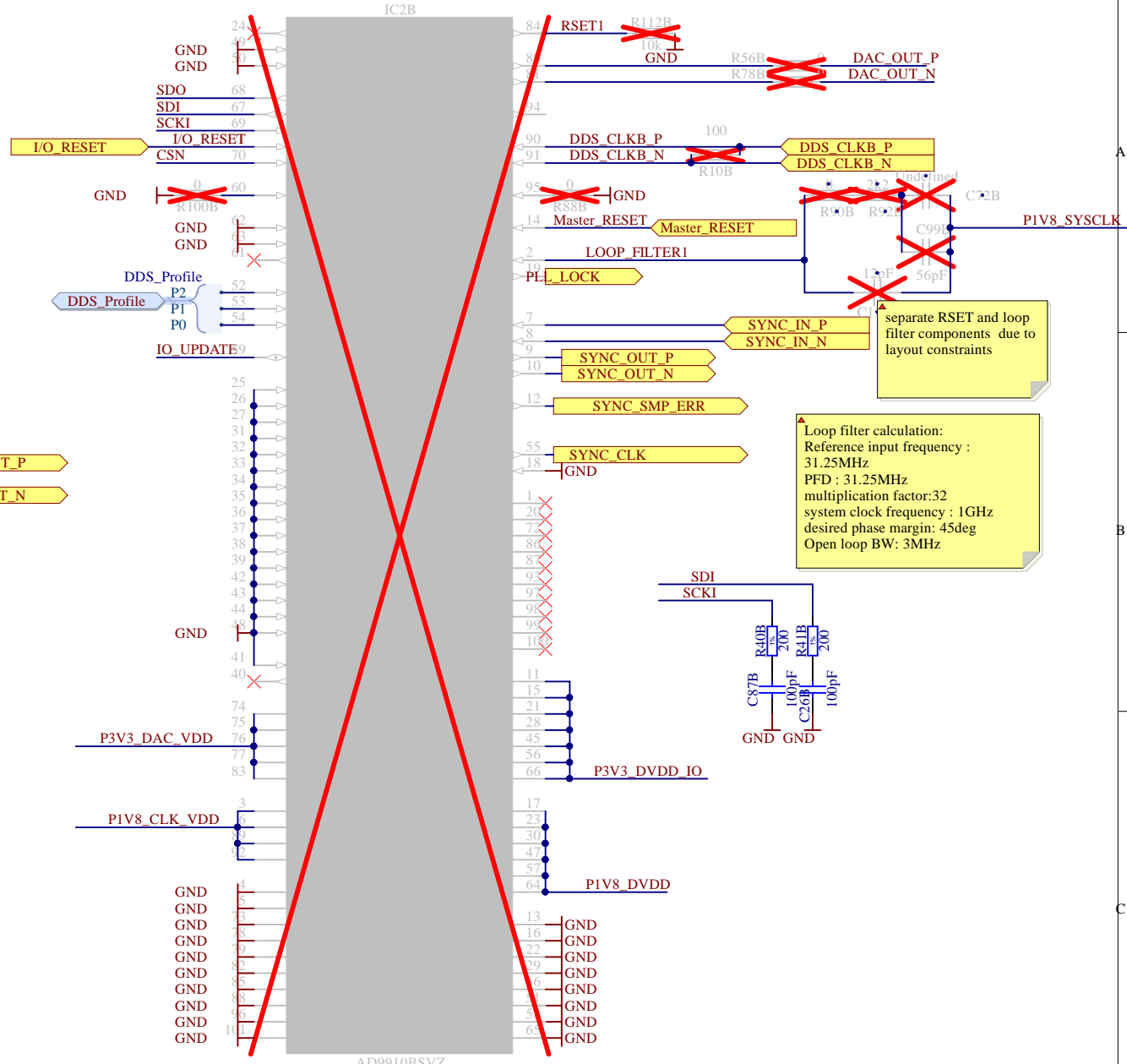
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0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

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PIN37 is not used but must be powered 1.8 or 3.3



DDS_Profile

IO_UPDATE9

IO_UPDATE9

IO_UPDATE9

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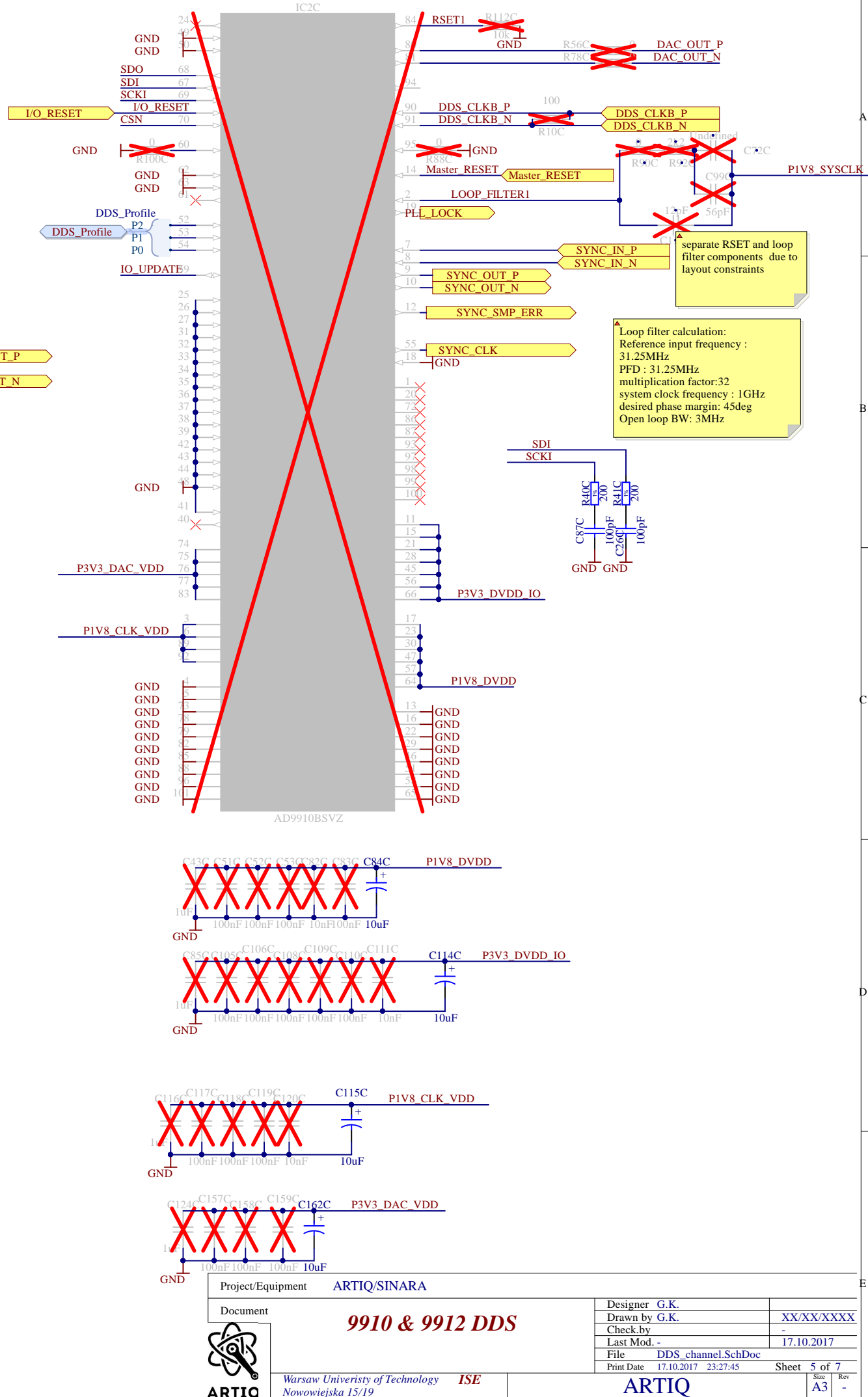
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Check by	-	Last Mod.	17.10.2017
File	DDS_channel.SchDoc	Print Date	17.10.2017 23:27:45
Sheet	5 of 7	Size	A3
Rev	-		



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0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

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Loop filter calculation:
Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

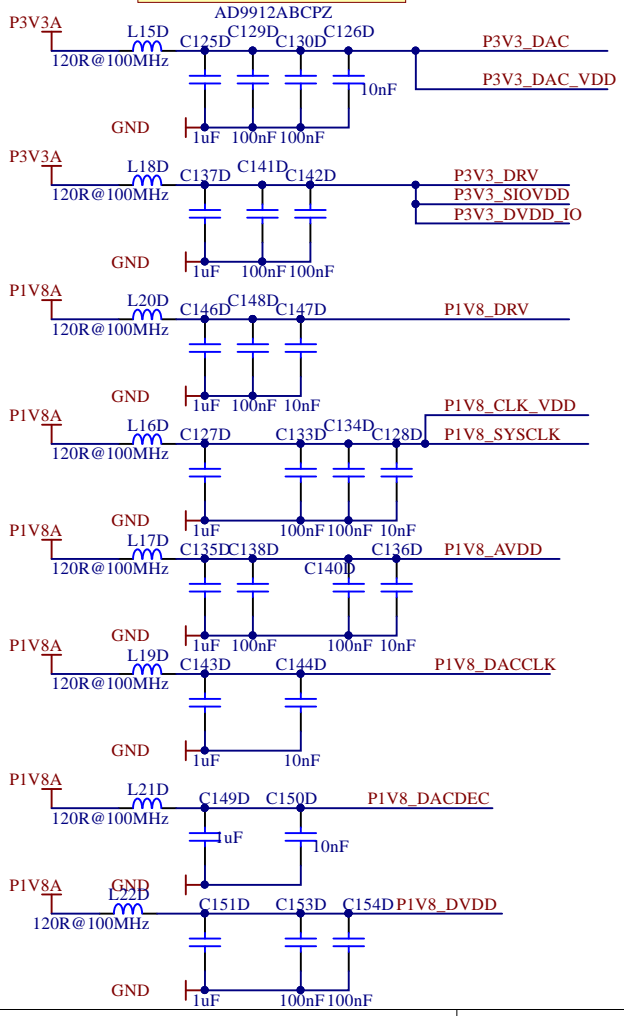
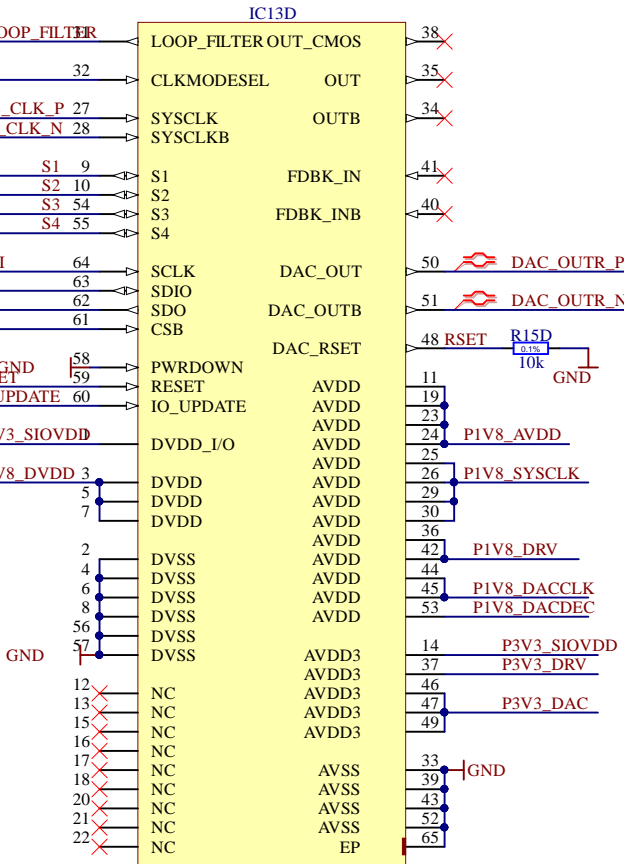
Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

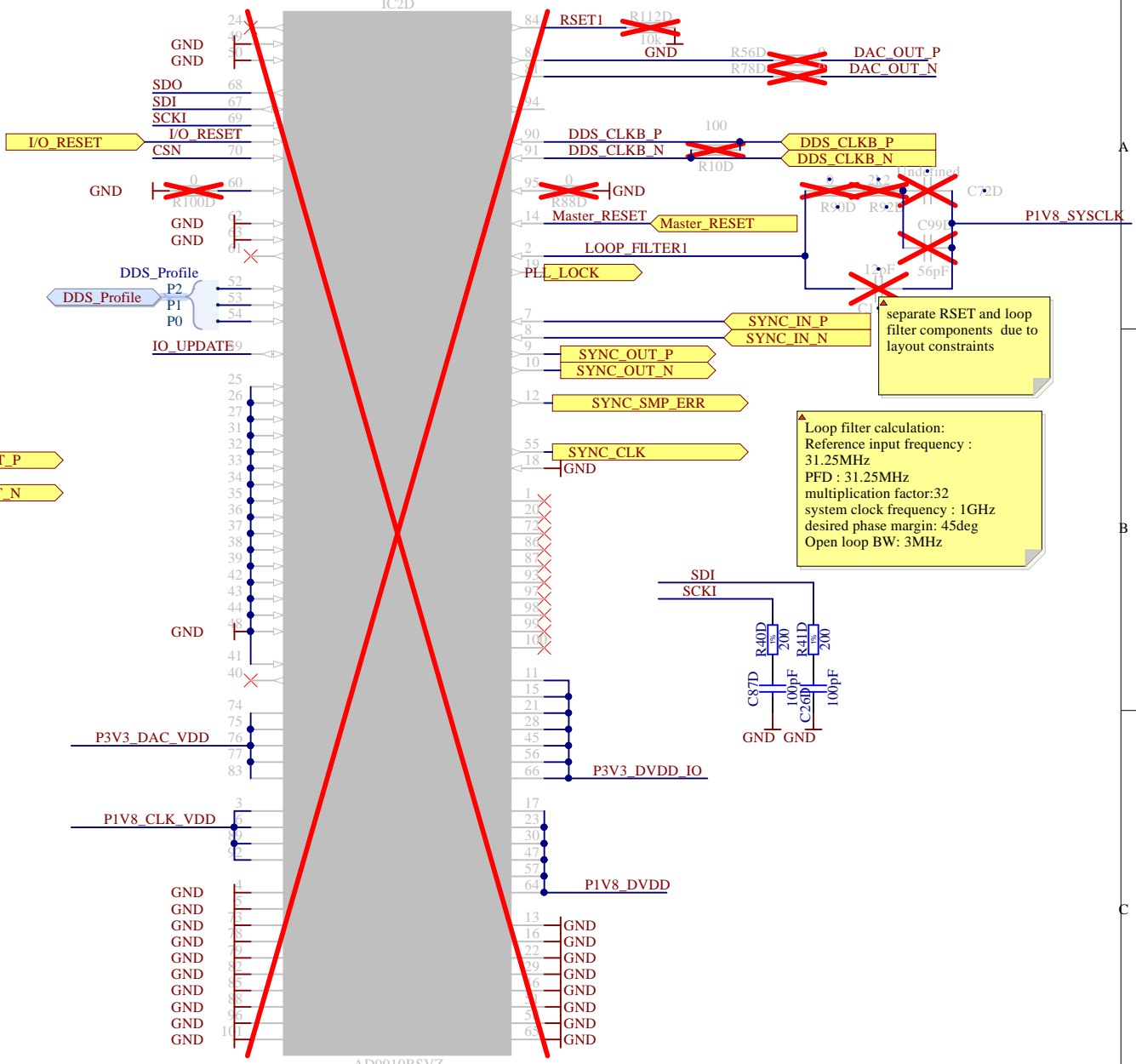
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0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
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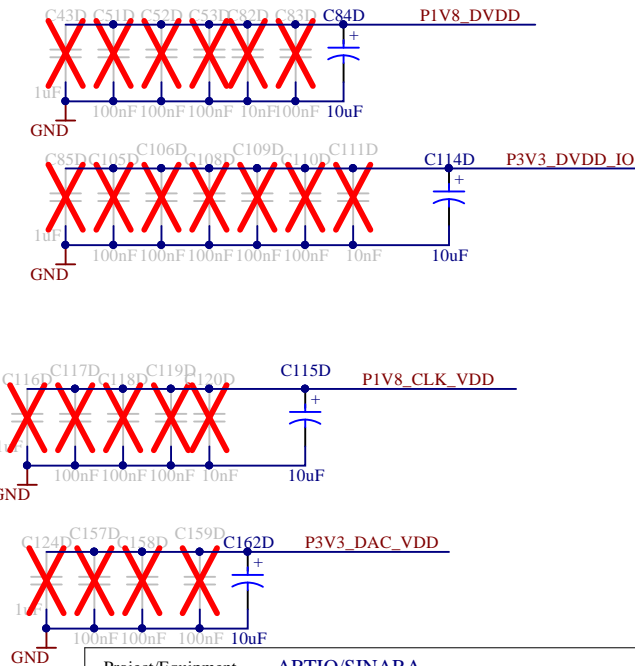
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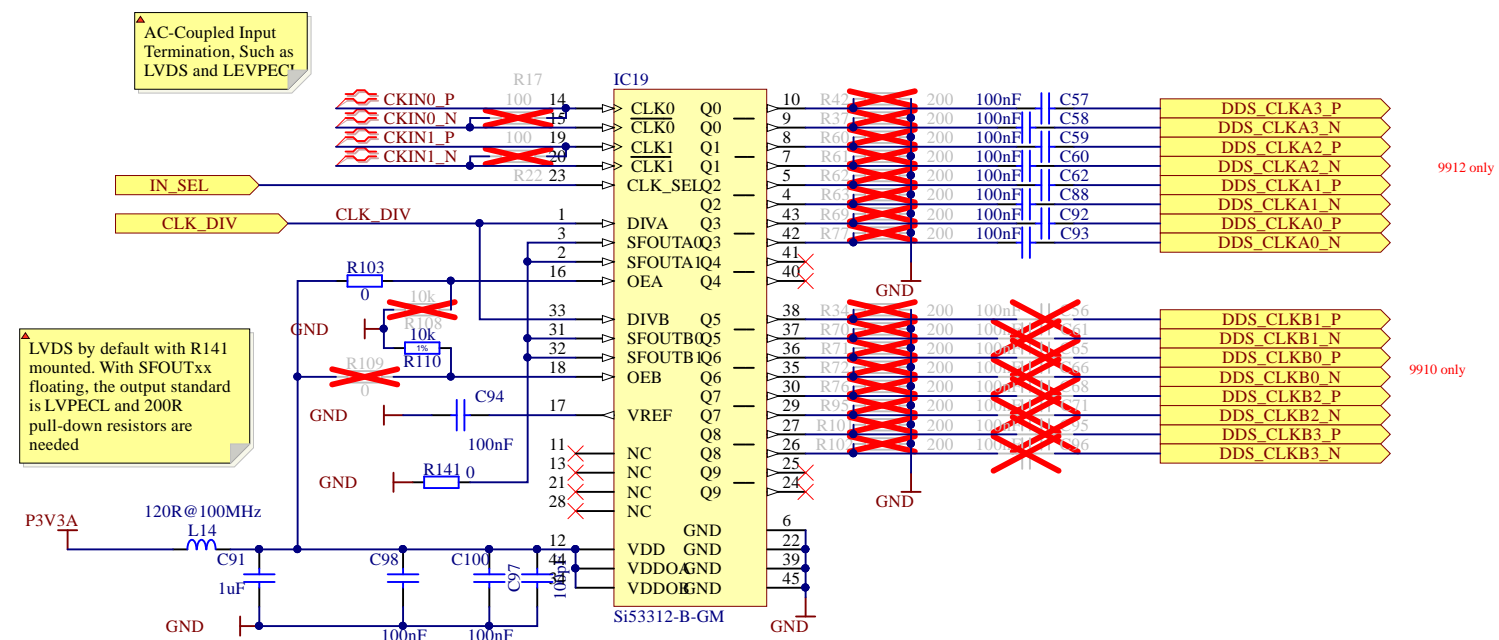


PIN37 is not used but must be powered 1.8 or 3.3

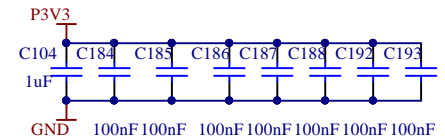
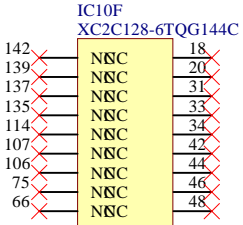
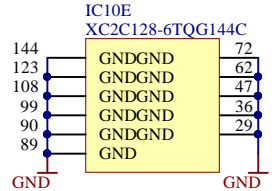
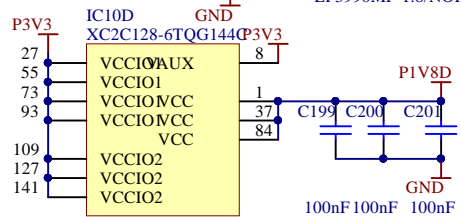
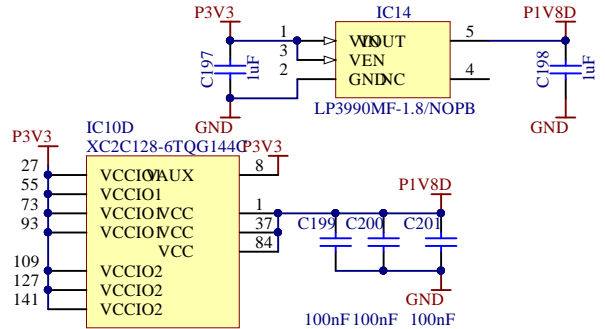
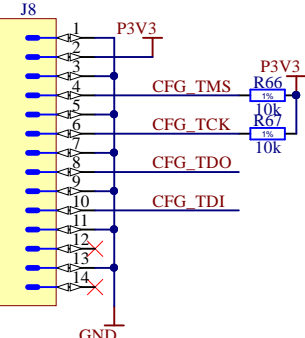
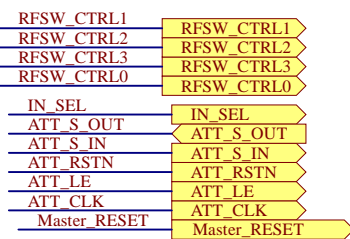
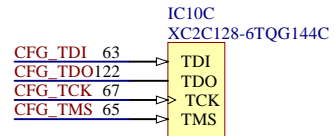
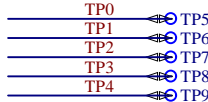
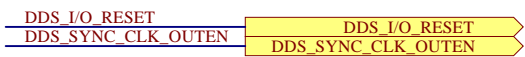
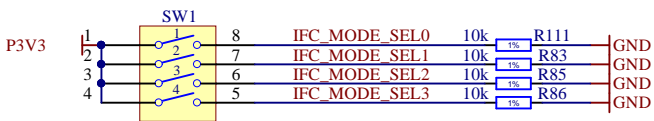
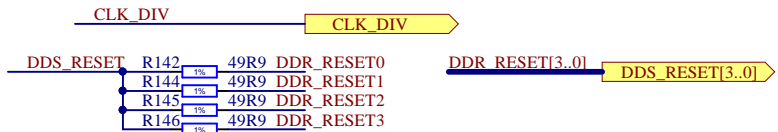
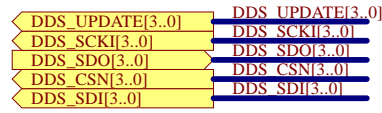
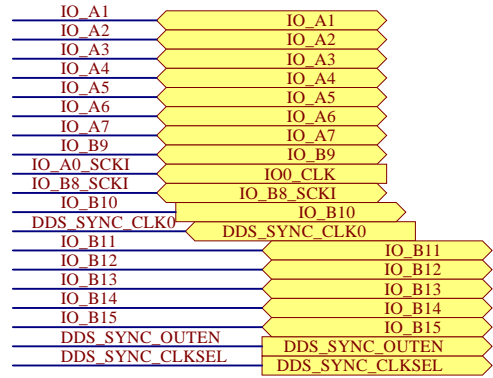
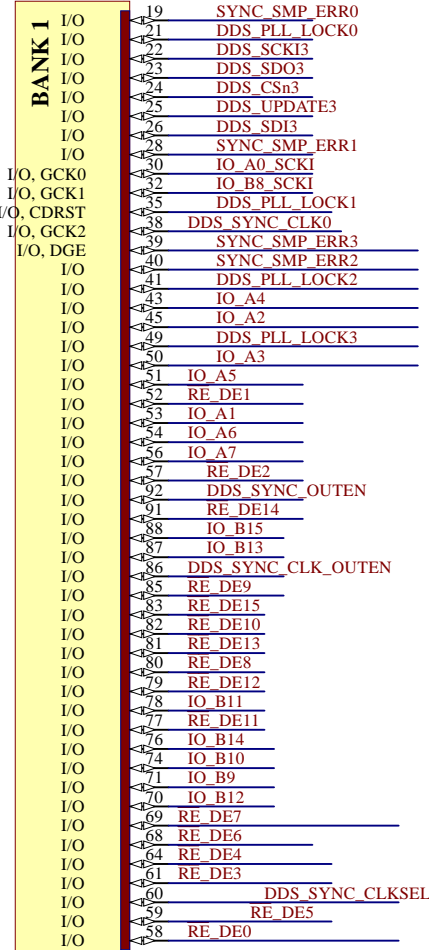


Loop filter calculation:
Reference input frequency : 31.25MHz
PFD : 31.25MHz
multiplication factor:32
system clock frequency : 1GHz
desired phase margin: 45deg
Open loop BW: 3MHz





IC10A
XC2C128-6TQG144C

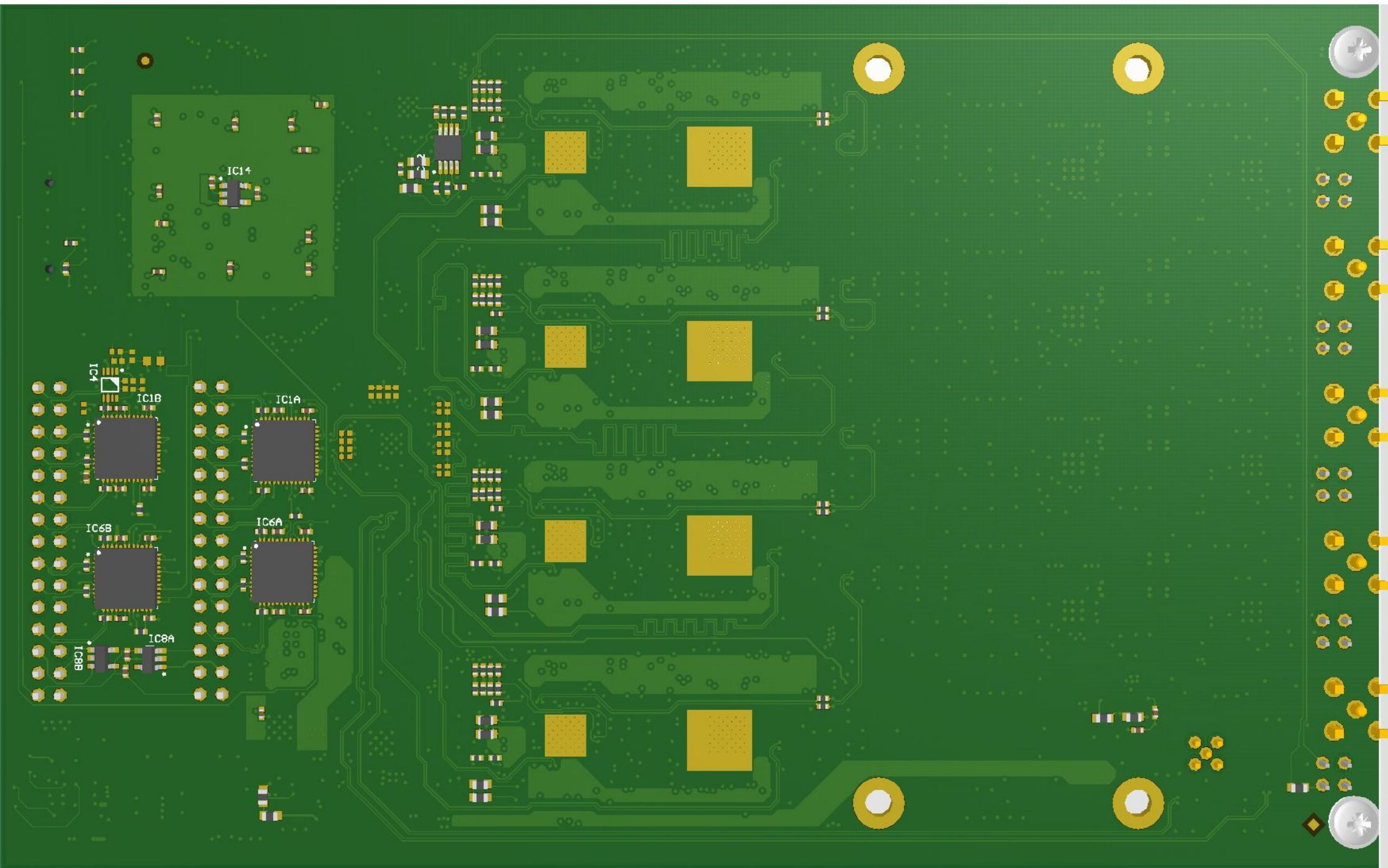


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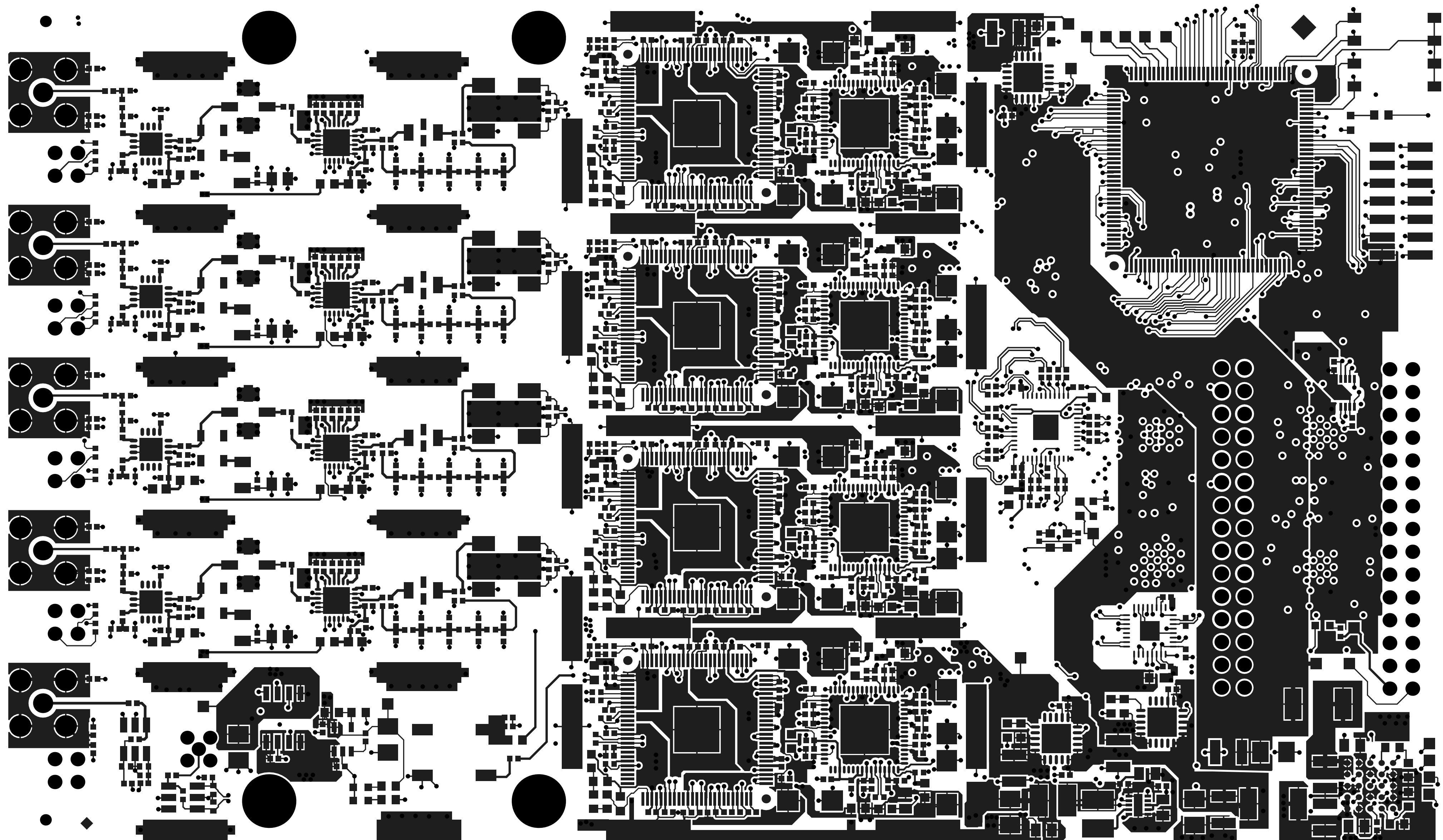
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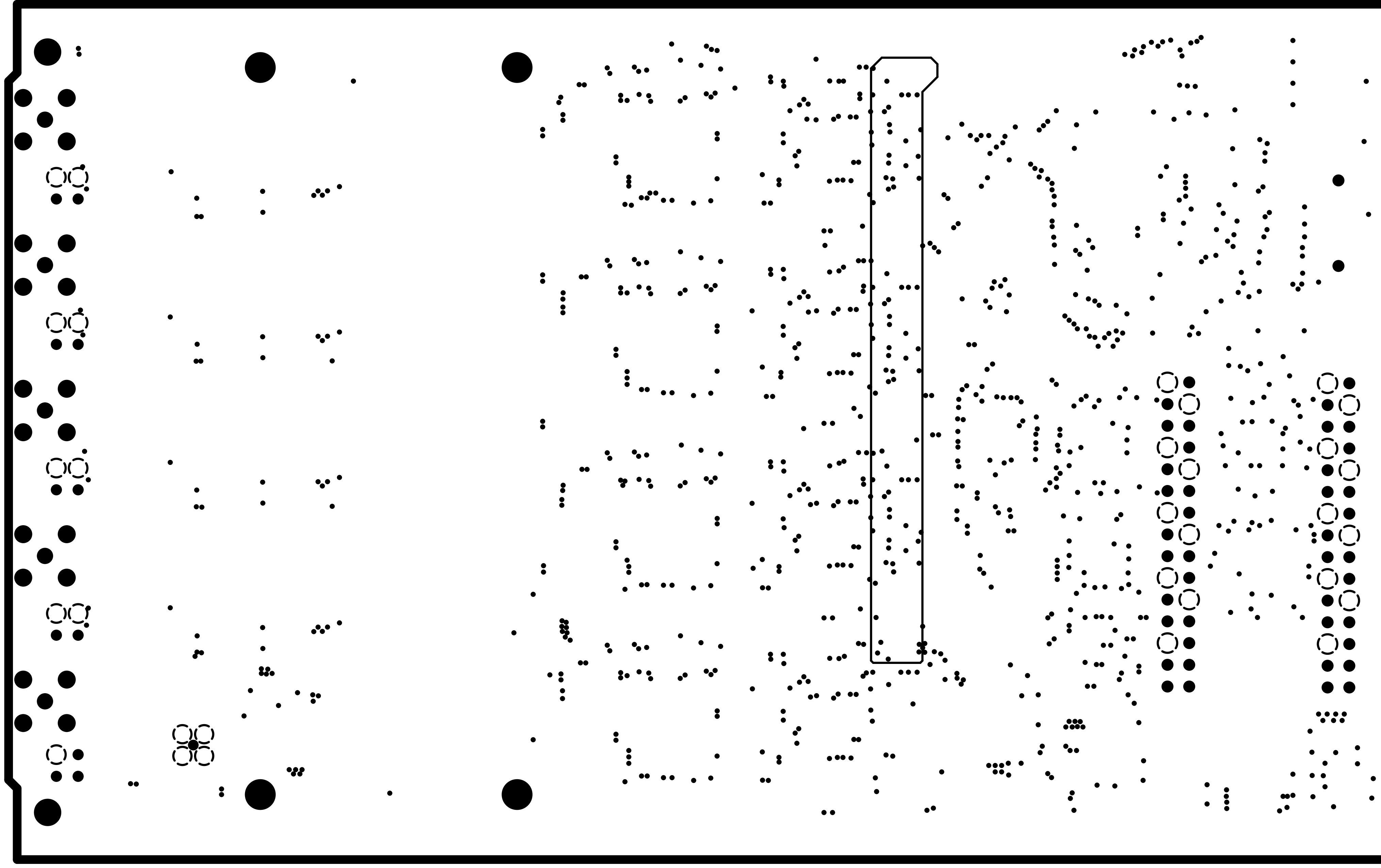
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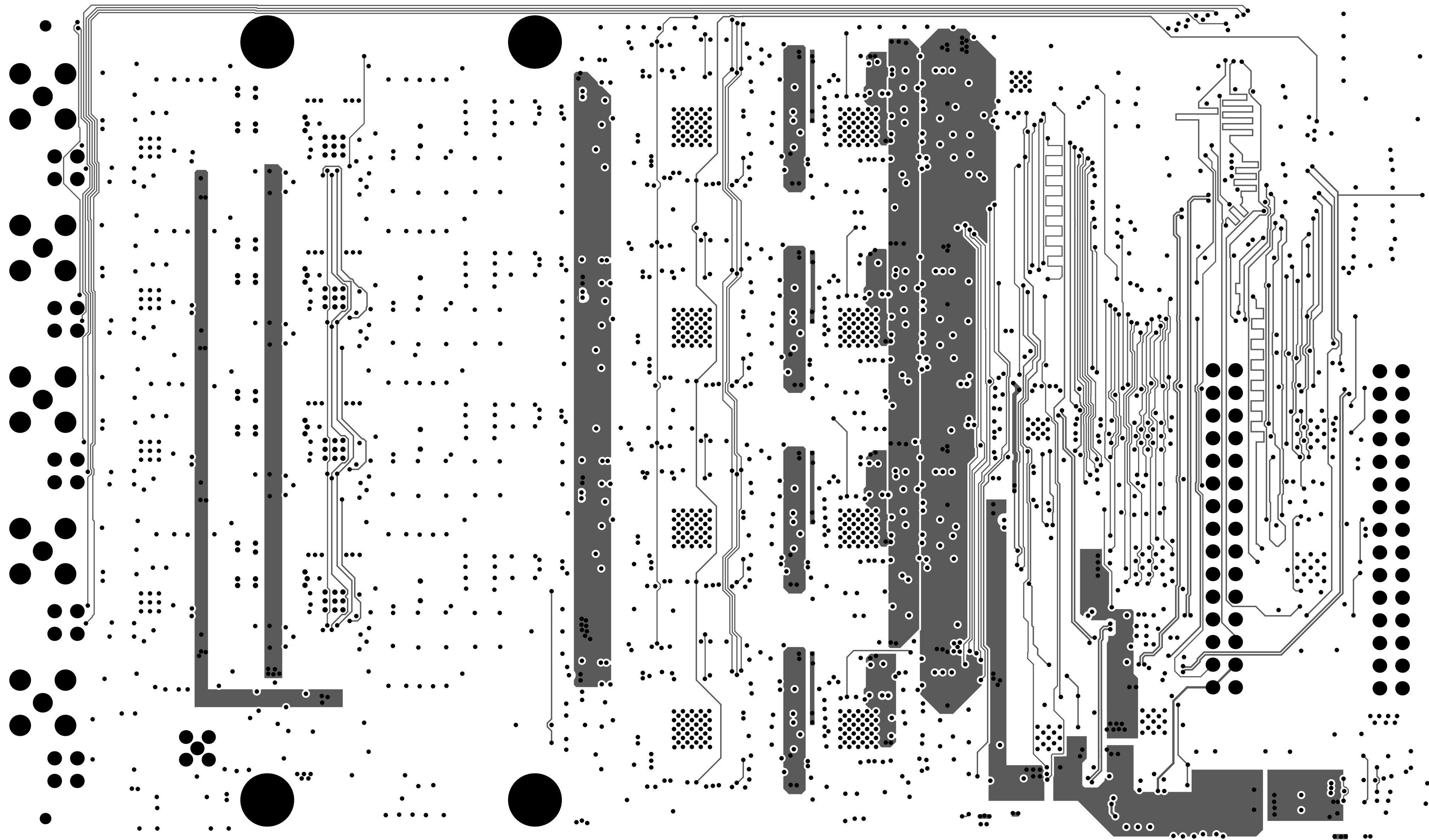


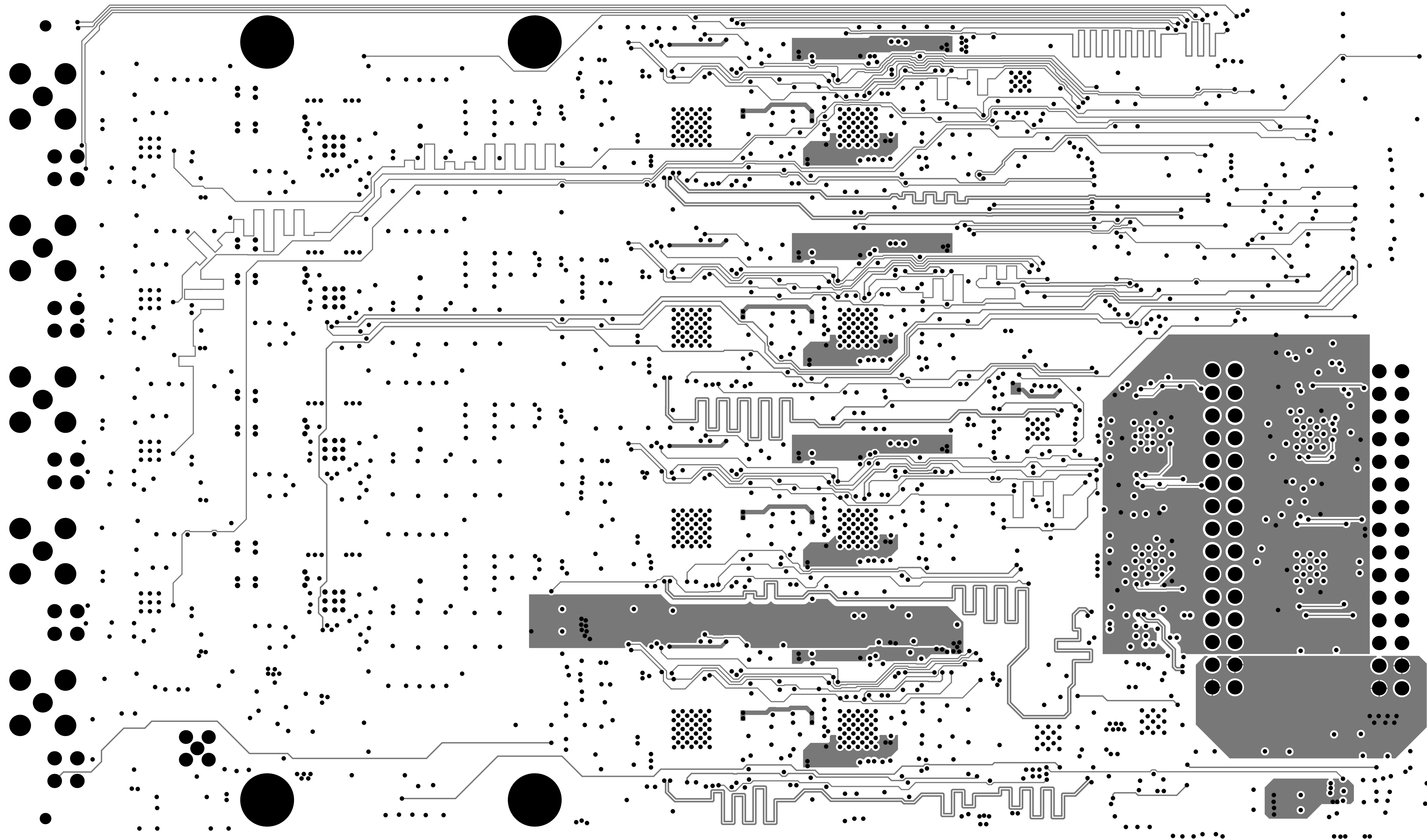


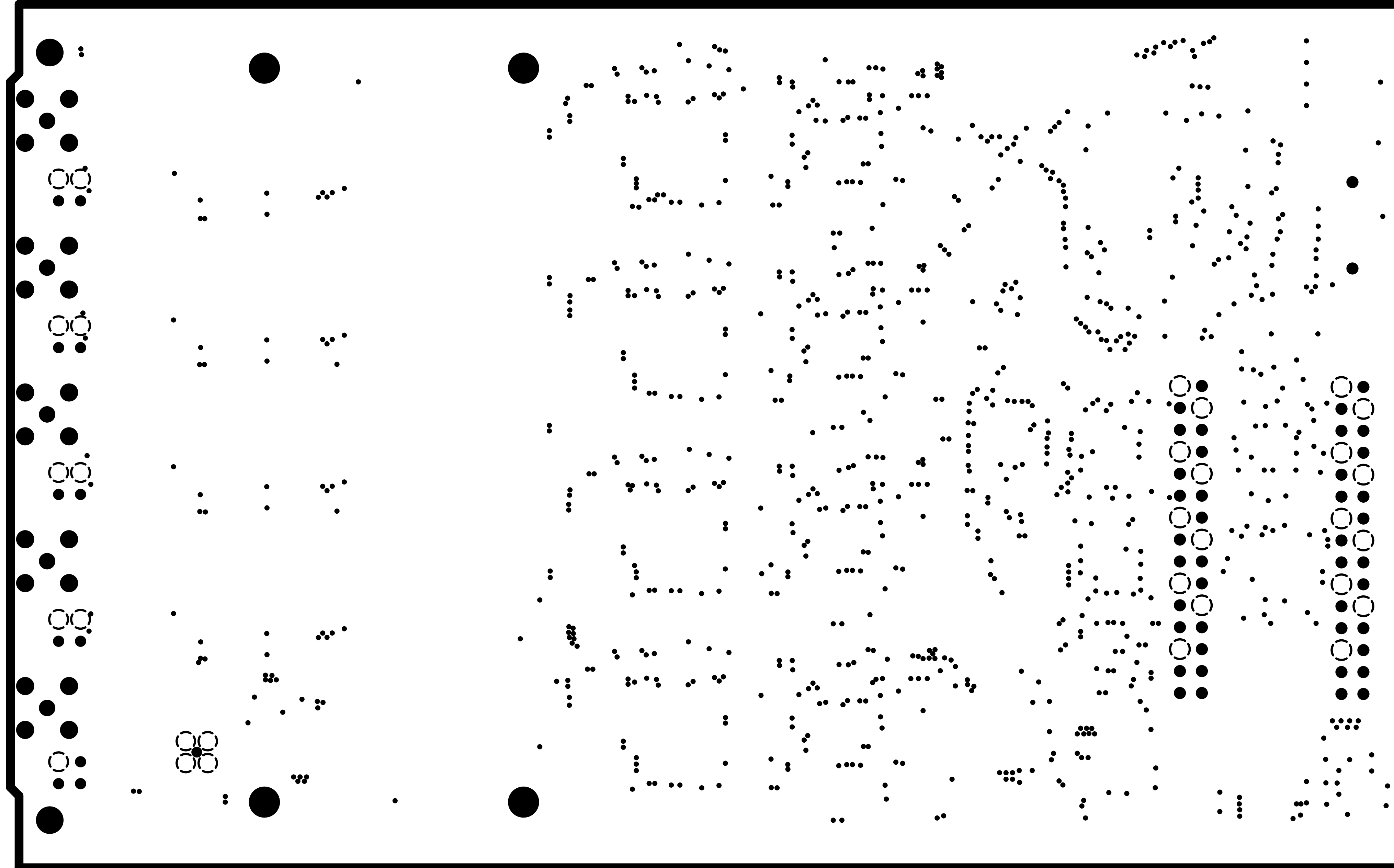


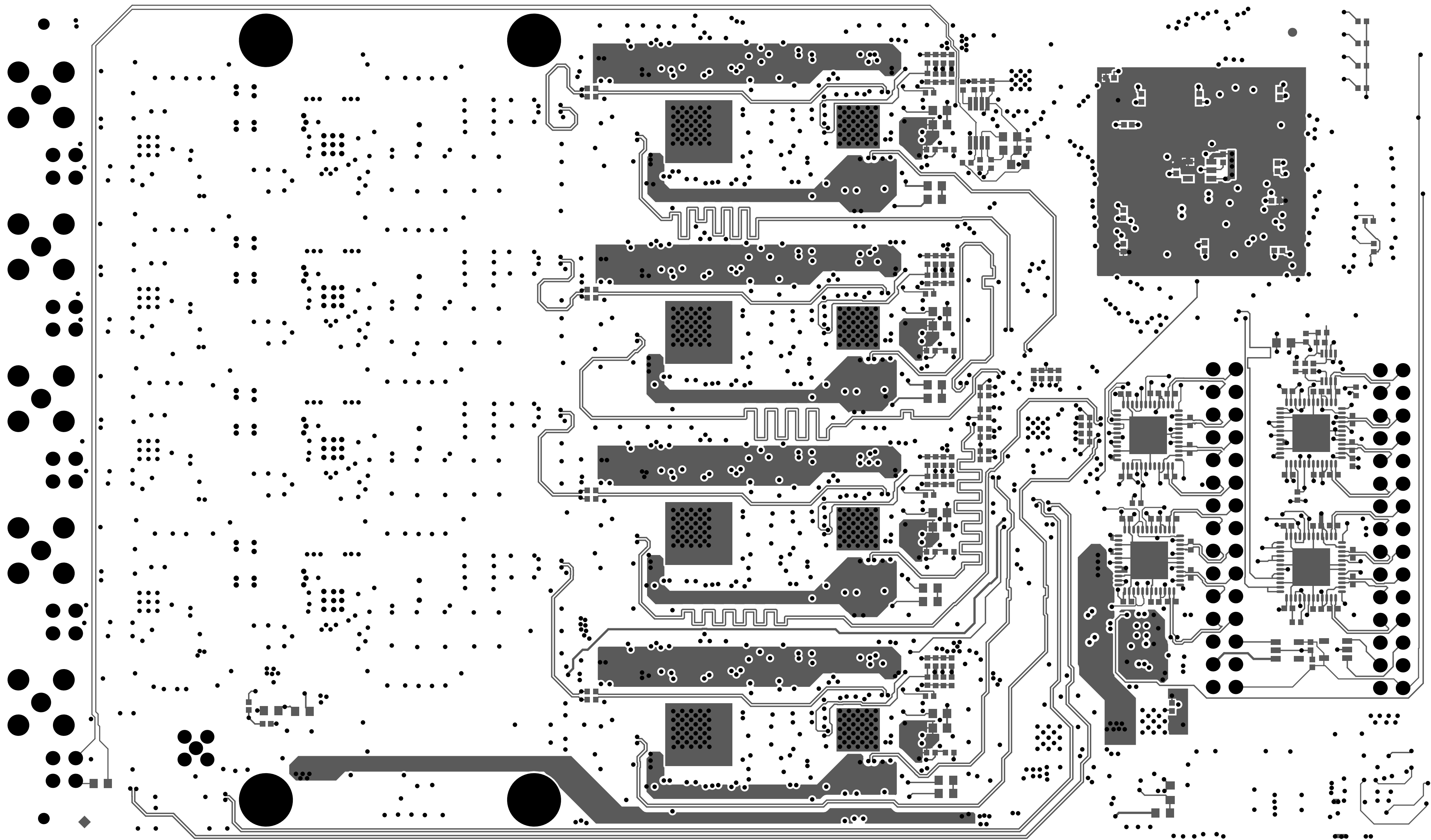














IC1B

AI1I

IC8B

IC8A

