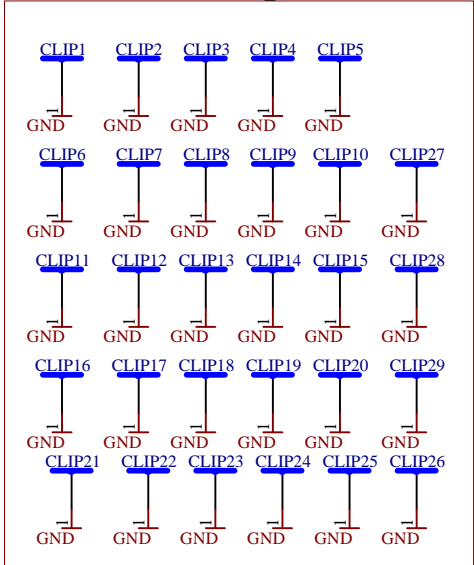


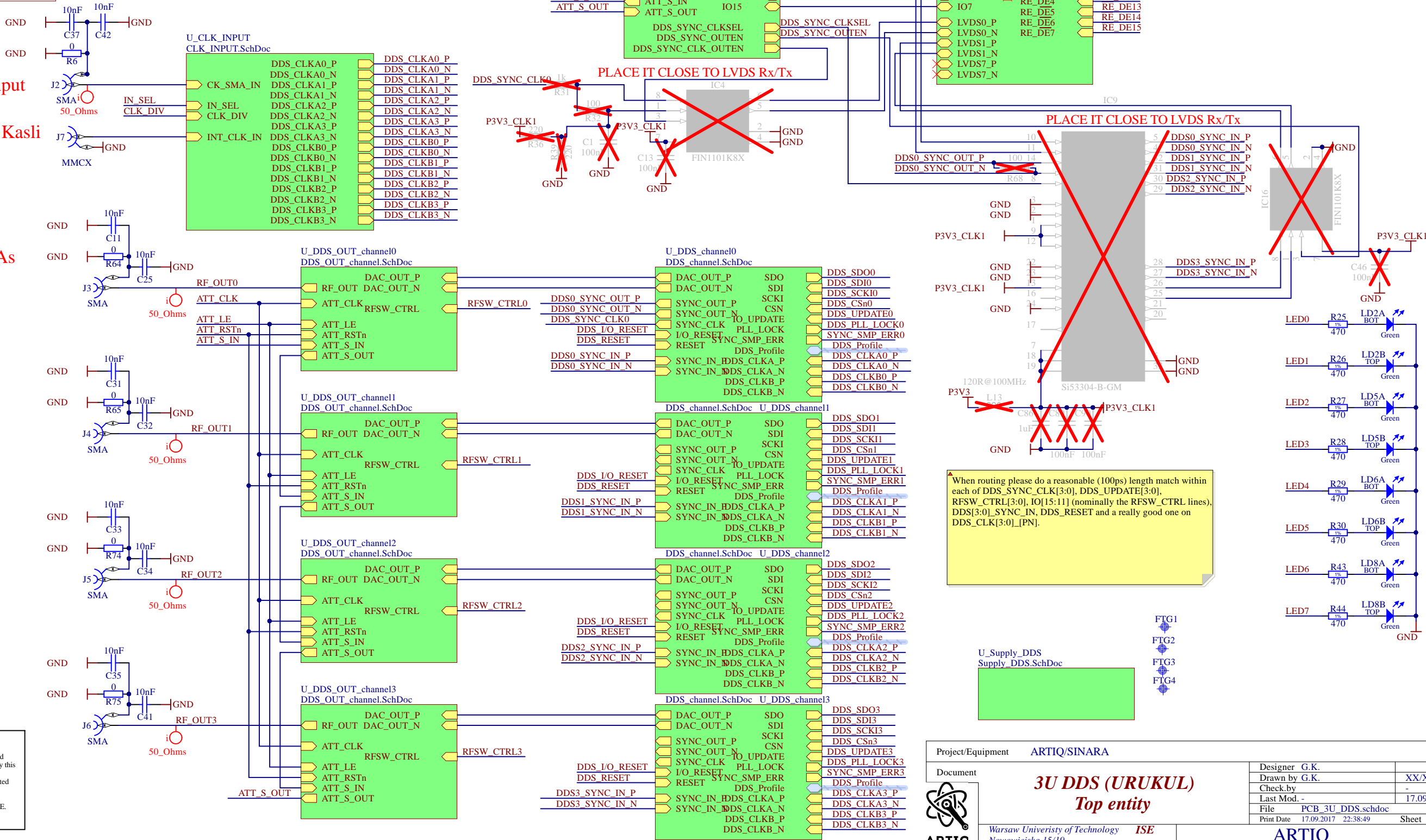
shield clips



Ext clock input

Clock from Kasli

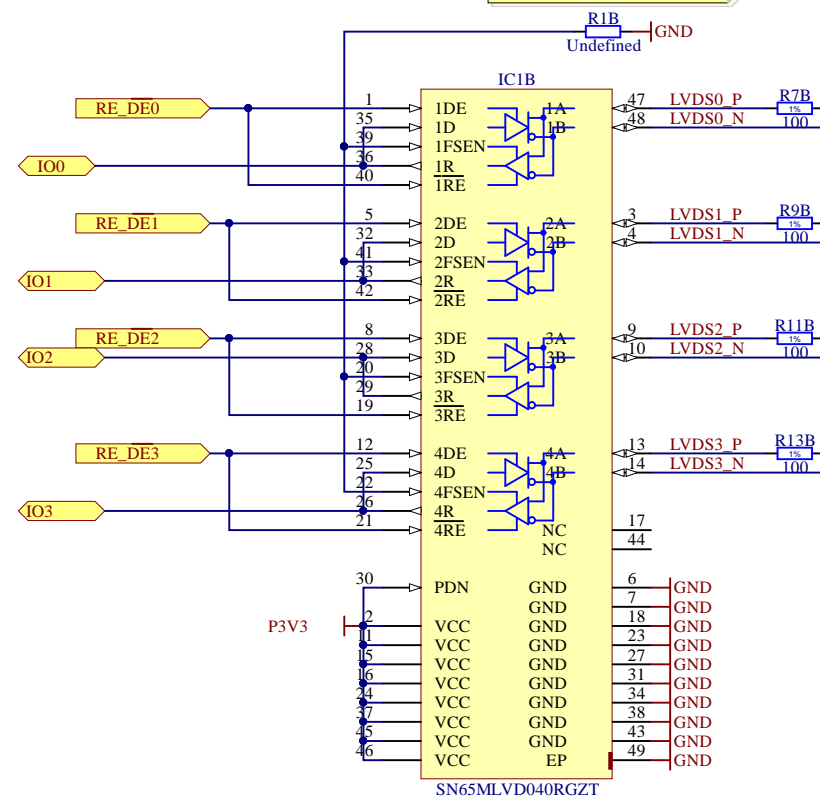
Output SMAs



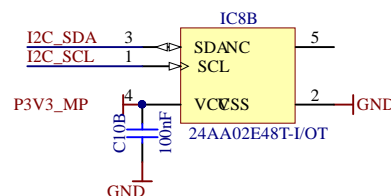
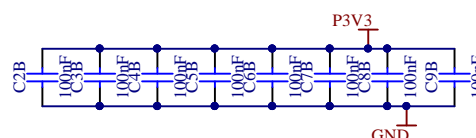
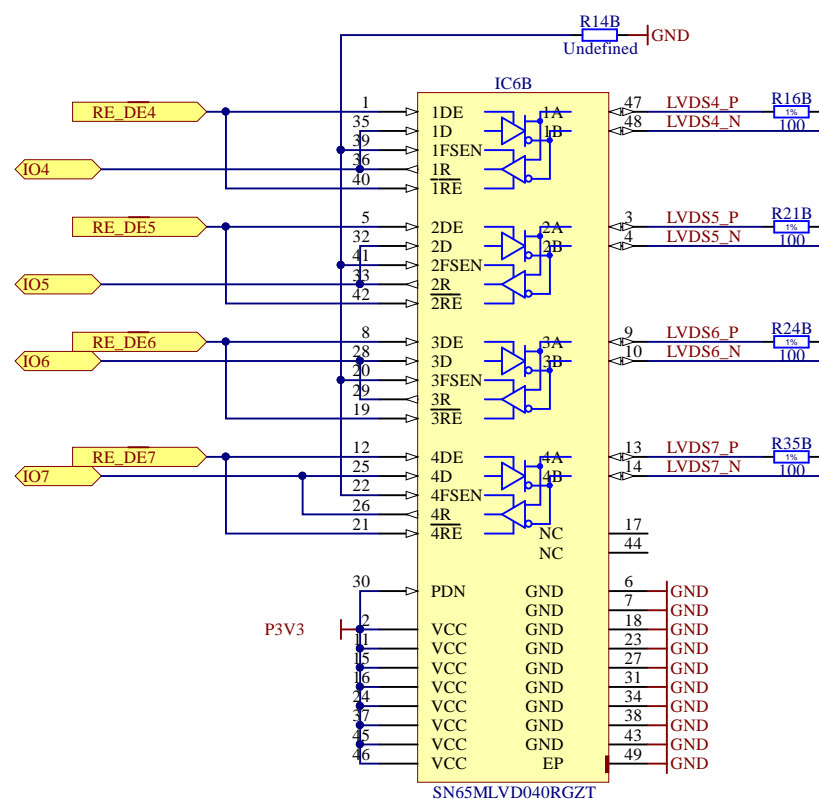
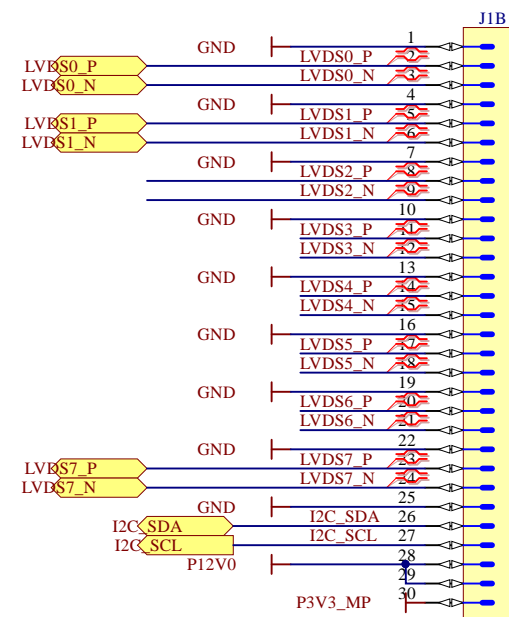
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Project/Equipment		ARTIQ/SINARA	
Document		3U DDS (URUKUL) Top entity	
Designer		G.K.	XX/XX/XXXX
Drawn by		G.K.	-
Check by		-	17.09.2017
Last Mod.		-	-
File		PCB_3U_DDS.schdoc	Sheet 1 of 7
Print Date		17.09.2017 22:38:49	Size A3
Warsaw University of Technology ISE		ARTIQ	
Nowowiejska 15/19		-	

FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output



This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A



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Project/Equipment ARTIQ/SINARA

Document



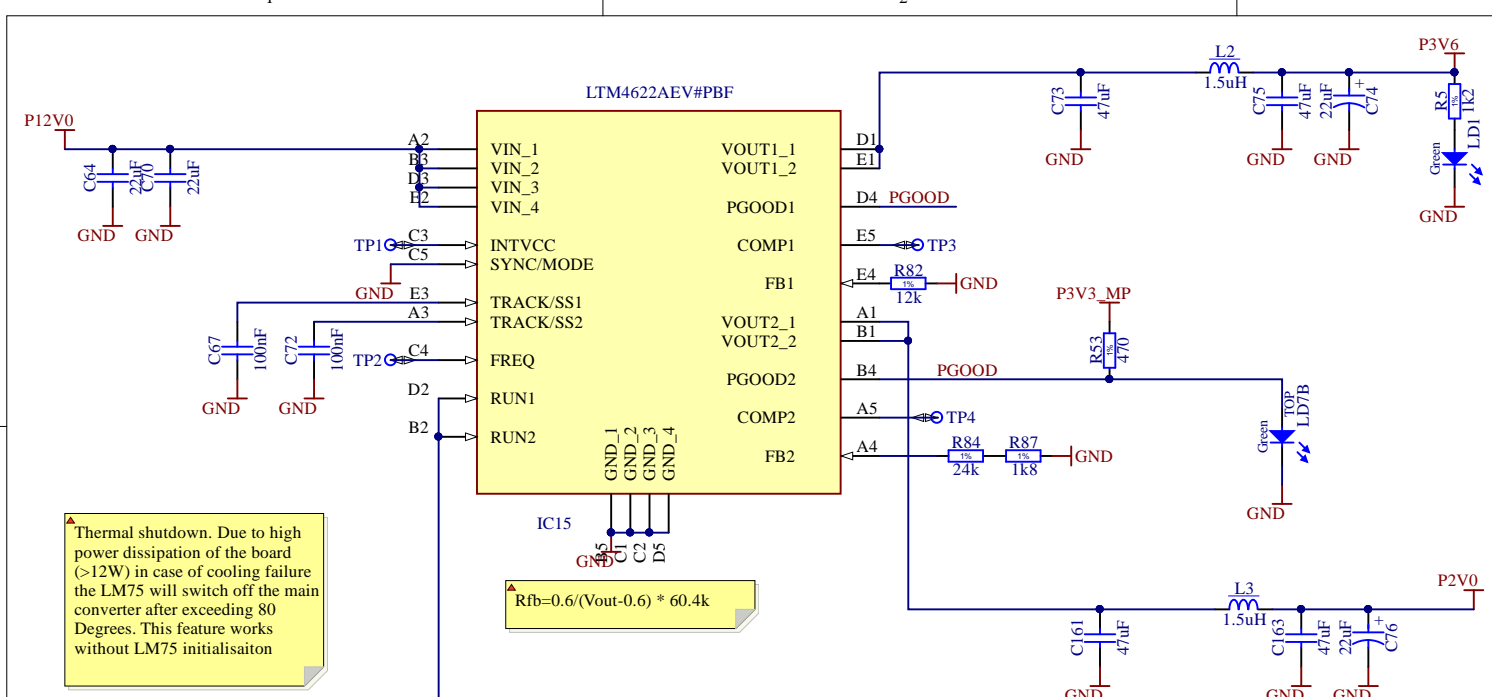
**LVDS to LVTTL
interface & EEM connector**

Warsaw University of Technology ISE
Nowowiejska 15/19

Designer	G.K.	
Drawn by	G.K.	XX/XX/XXXX
Check by	-	17.09.2017
Last Mod.	-	
File	LVDS_IFC_DDS.SchDoc	
Print Date	17.09.2017 22:38:50	Sheet 2 of 7

ARTIQ

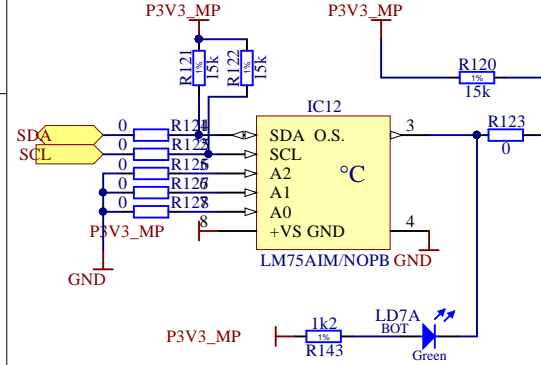
Size A3 Rev -



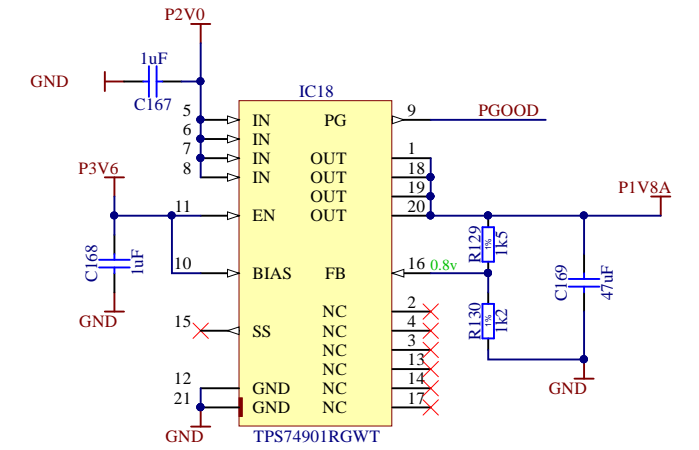
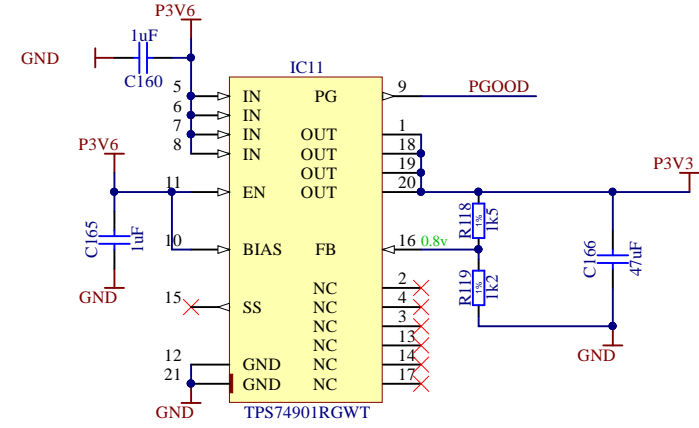
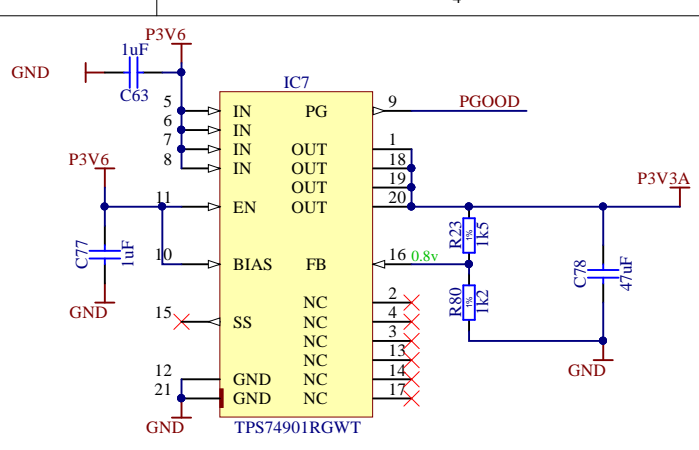
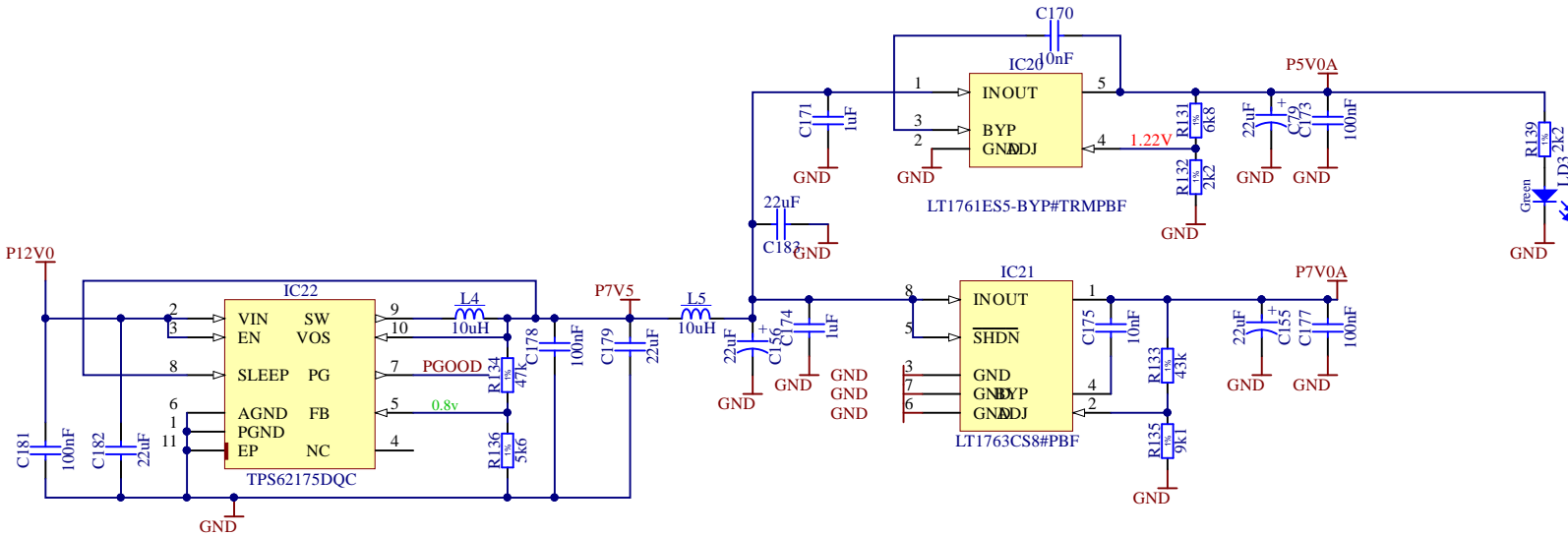
Thermal shutdown. Due to high power dissipation of the board (>12W) in case of cooling failure the LM75 will switch off the main converter after exceeding 80 Degrees. This feature works without LM75 initialisaition

$R_{fb} = 0.6 / (V_{out} - 0.6) * 60.4k$

ADR: 1001 000

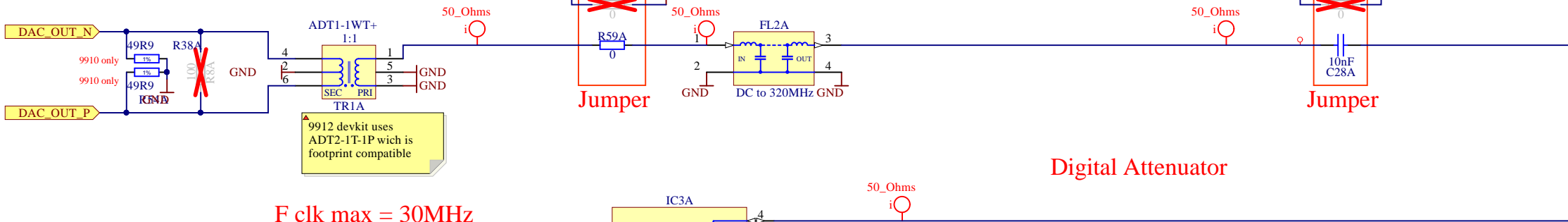


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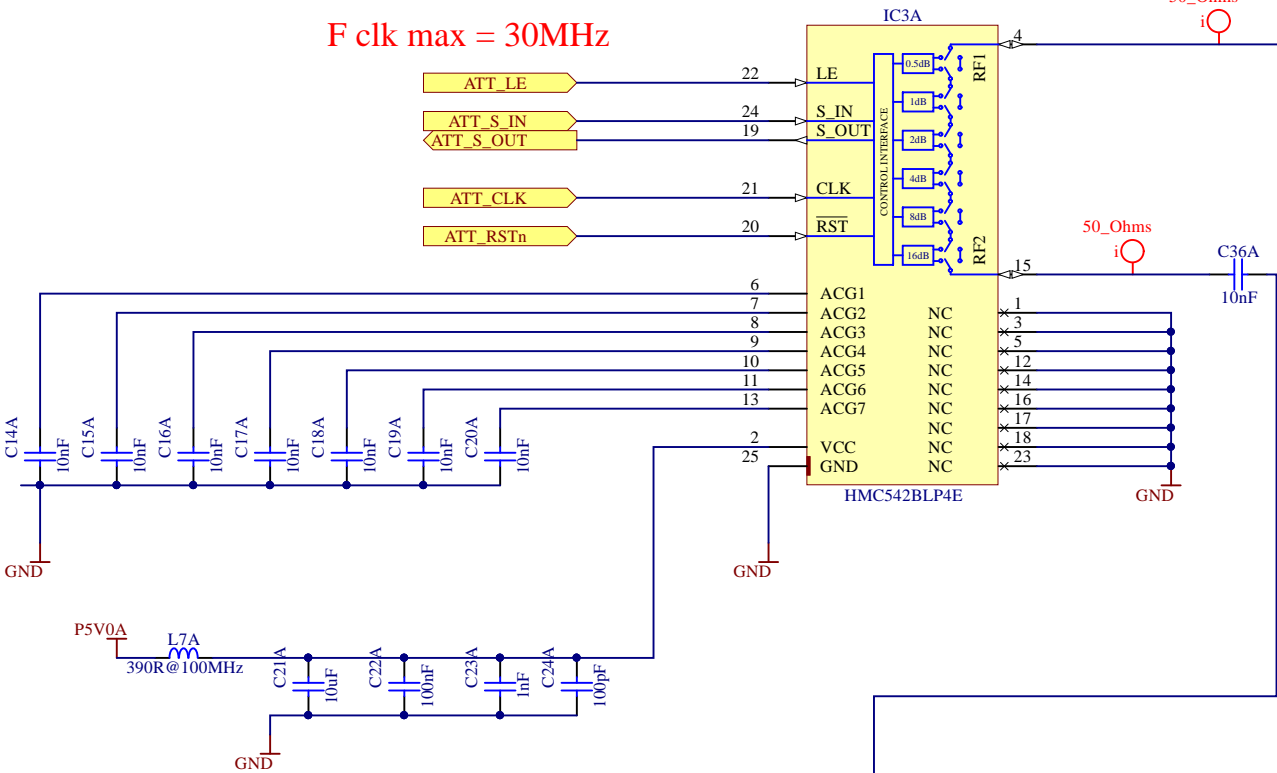


Power budget (max ratings):		
	AD9912 variant(mA)	AD9910 variant(mA)
P3V3:		
LVDS interface 4x	660	660
LVDS load 4x24mA	96	96
CPLD	100	100
ADCLK948	230	230
DDS AVDD3	4*(9,6+31)=133,6	4*29=116
DDS DVDDIO	4*3=12	4*11=44
TOTAL P3V3	1121	1146
TOTAL POWER	3.7	3.7
P1V8:		
DDS AVDD	4*(48+136)=736	4*110=440
DDS DVDD	4*246=984	4*222=888
TOTAL P1V8	1720	1328
TOTAL POWER	3,096	2.39
P5V0		
HMC542BLP4E	4*2.9=11.6	4*2.9=11.6
HMC349LP4C	4*3.5=14	4*3.5=14
TOTAL 5V0	25.6	25.6
TOTAL POWER	0,125	0,125
P7V0		
ERA-3XSM+	4*35=150	4*35=150
TOTAL POWER	1.05	1.05
DC/DC converter losses		
TPS62175 eff. .95	0,05*(.27+0,026)*7,5=0.11	0,05*(.27+0,026)*7,5=0.11
LTM:3.6V eff. .9	0.1*1,321*3,6=0,47	0,1*1,346*3,6=0,48
LTM:2V eff. .87	0.13*1,721*2=0,44	0.13*1.328*2=0.34
LDO losses		
2V->1.8V	0.34	0.26
3.6V->3.3V	0.396	0.4
7.5V->7V	0.135	0.135
7.5V->5V	0,064	0,064
Total power from 12V	9.95W	9.05
Total current from 12V	0.83A	0.75A

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28) for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom Filter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder



F clk max = 30MHz



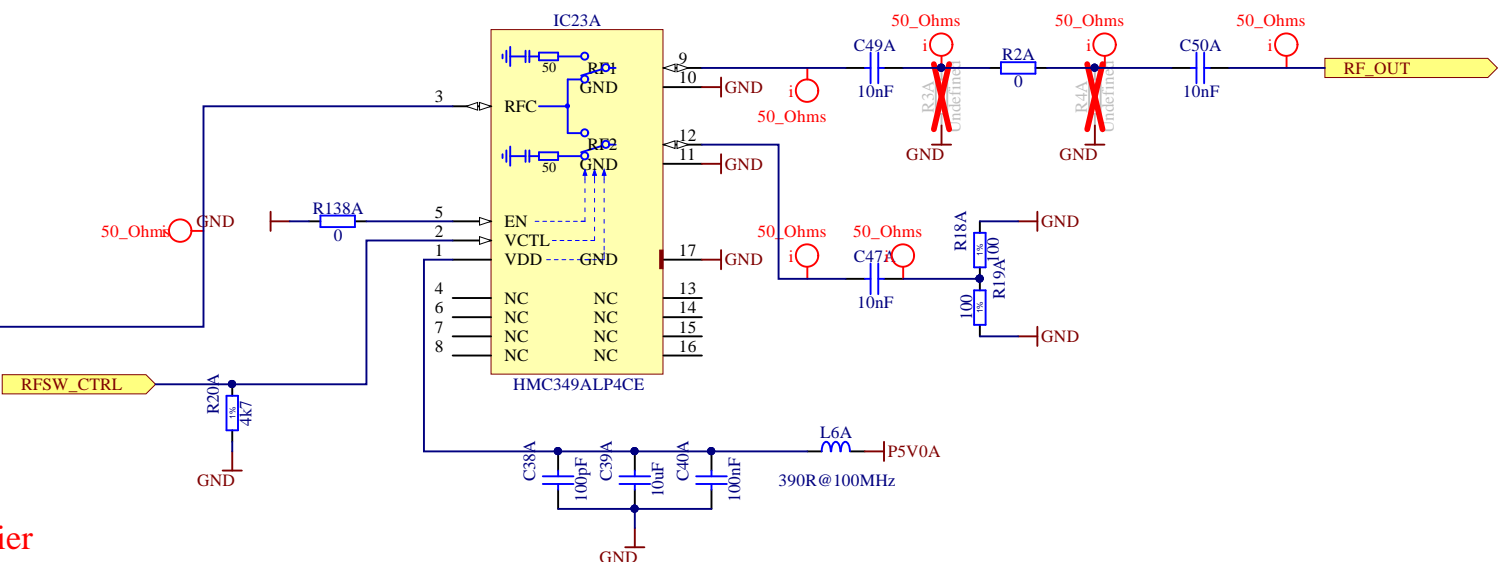
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

$R5 \text{ power} = 65\text{mA}^2 \cdot 39 = 0.16\text{W}$

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Amplifier
~23 dB gain and 13 dBm P1dB

SPDT switch



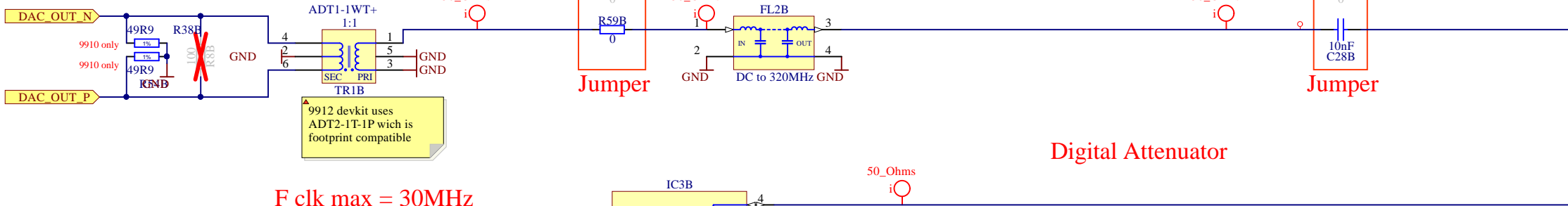
Project/Equipment	ARTIQ/SINARA	Designer	G.K.
Document		Drawn by	G.K.
		Check by	-
		Last Mod.	17.09.2017
File	DDS_OUT_channel.SchDoc	Print Date	17.09.2017 22:38:50
		Sheet	4 of 7
		Size	A3
		Rev	-

Output stage :
Attenuator, amplifier and filter

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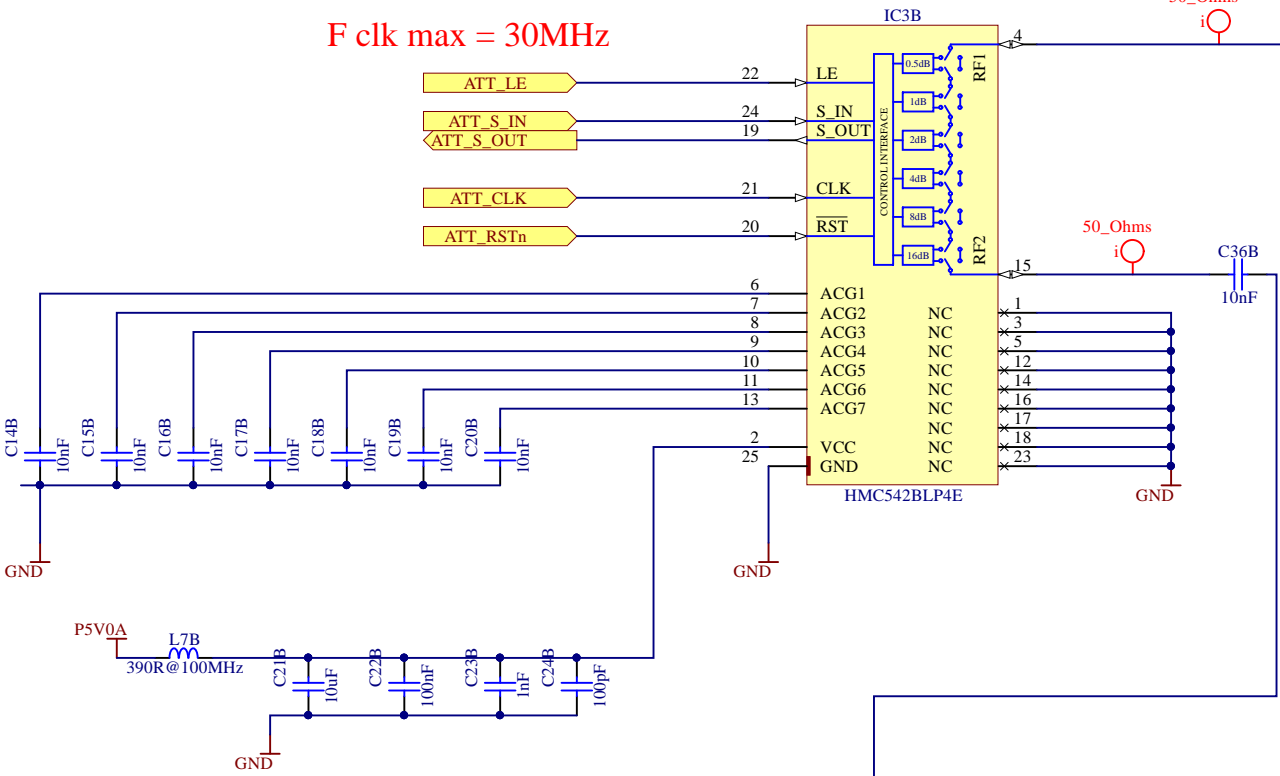
ARTIQ

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For Custom Filter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder



F clk max = 30MHz

Digital Attenuator



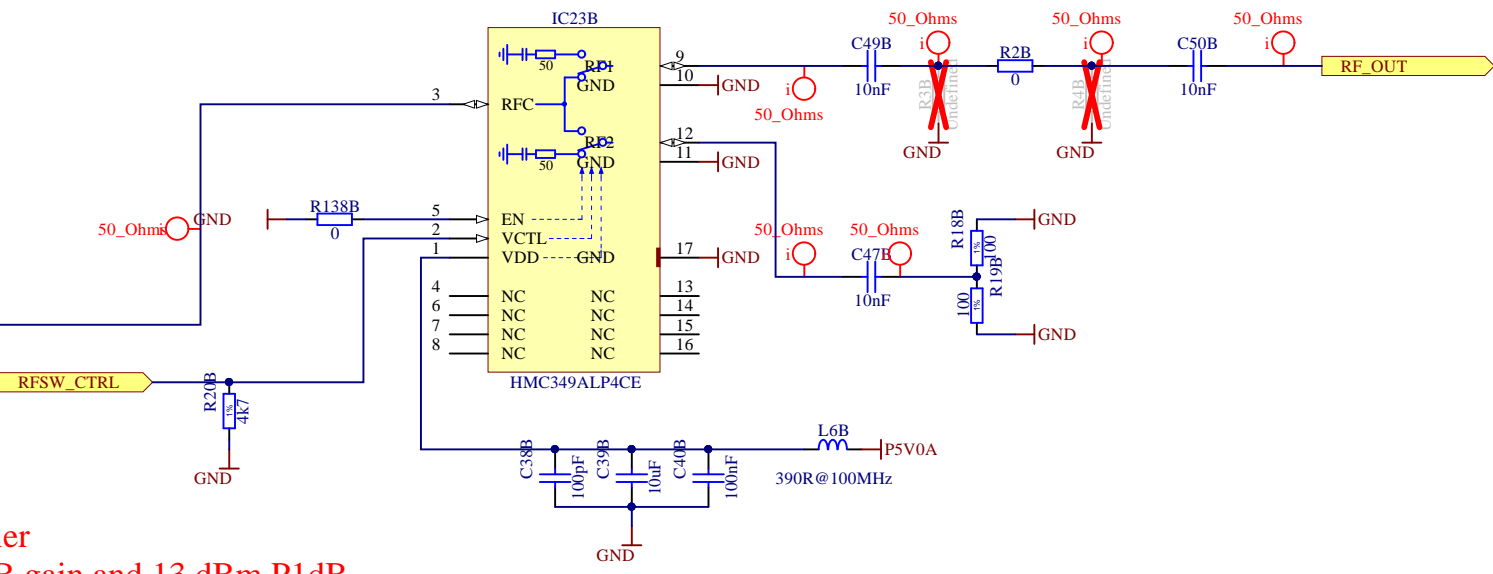
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R5 power = $65\text{mA}^2 \cdot 39 = 0.16\text{W}$

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Amplifier
~23 dB gain and 13 dBm P1dB

SPDT switch



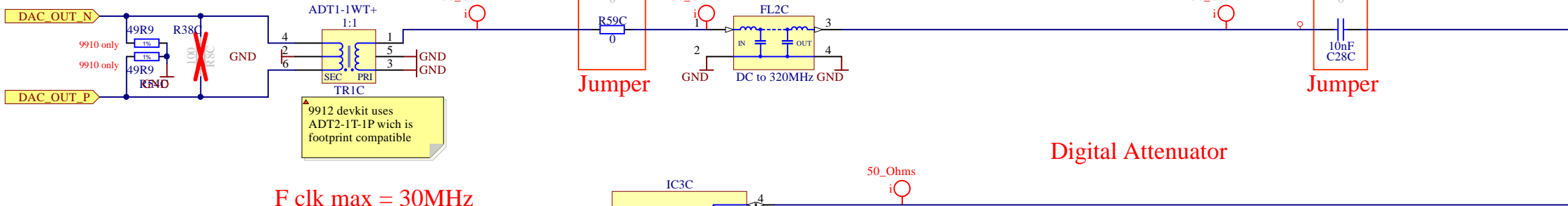
Project/Equipment	ARTIQ/SINARA	Designer	G.K.
Document		Drawn by	G.K.
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		Print Date	17.09.2017 22:38:50
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		Rev	-

Output stage :
Attenuator, amplifier and filter

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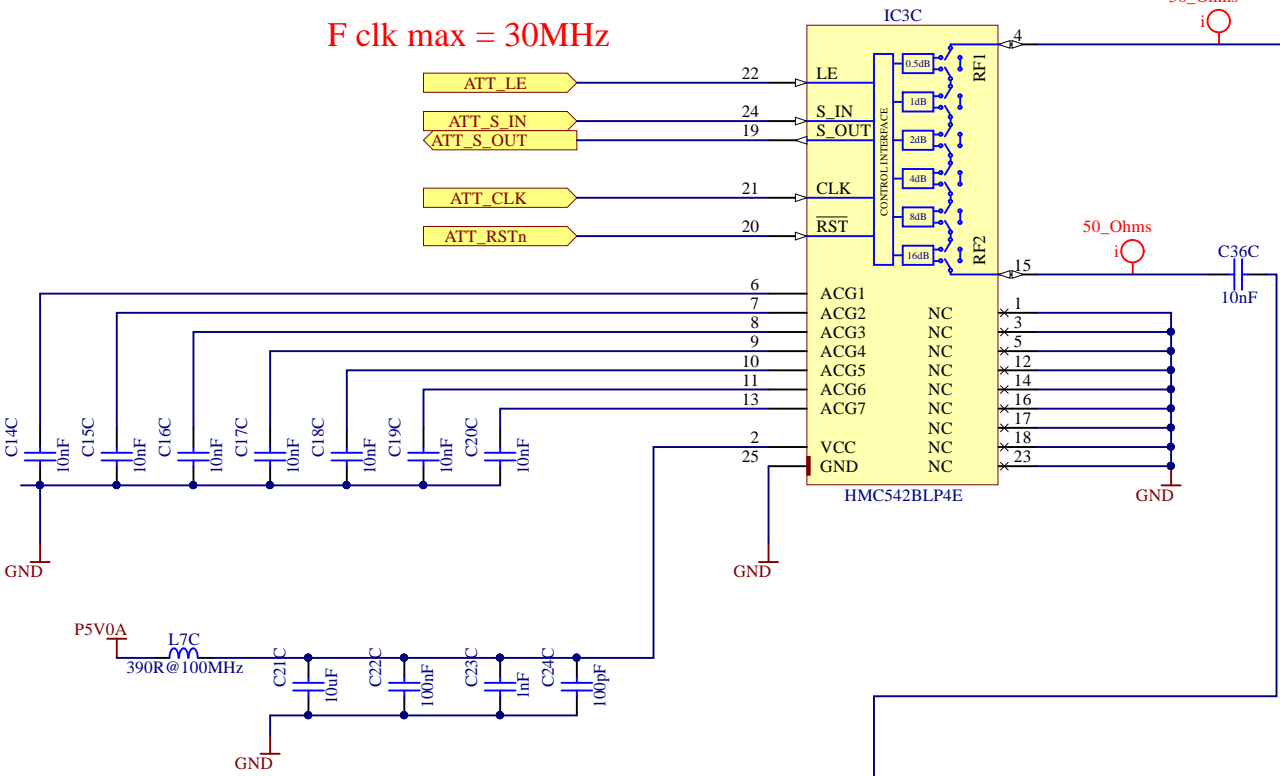
ARTIQ

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F clk max = 30MHz

Digital Attenuator



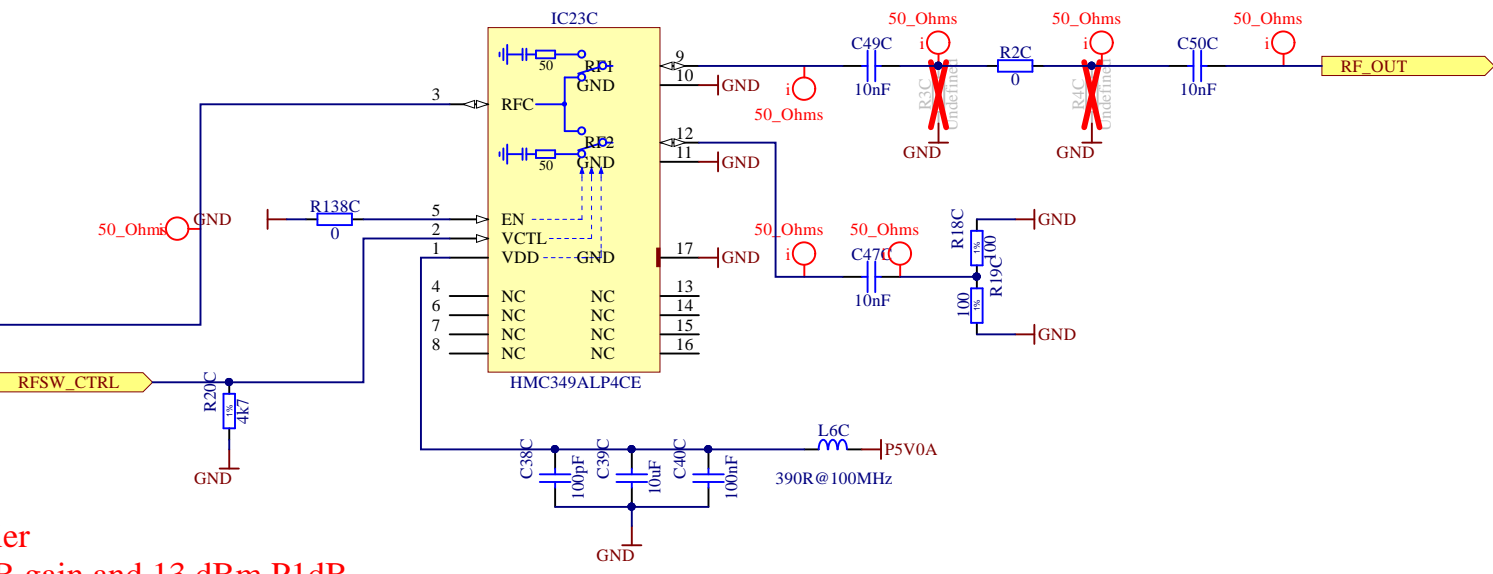
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R5 power = $65\text{mA}^2 \times 39 = 0.16\text{W}$

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Amplifier
~23 dB gain and 13 dBm P1dB

SPDT switch

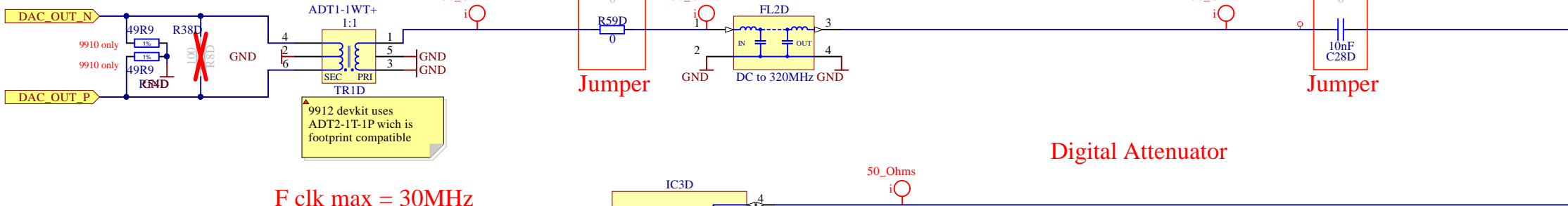


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Document		Designer G.K.	
		Drawn by G.K.	
		Check by -	
		Last Mod. -	
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		Sheet 4 of 7	
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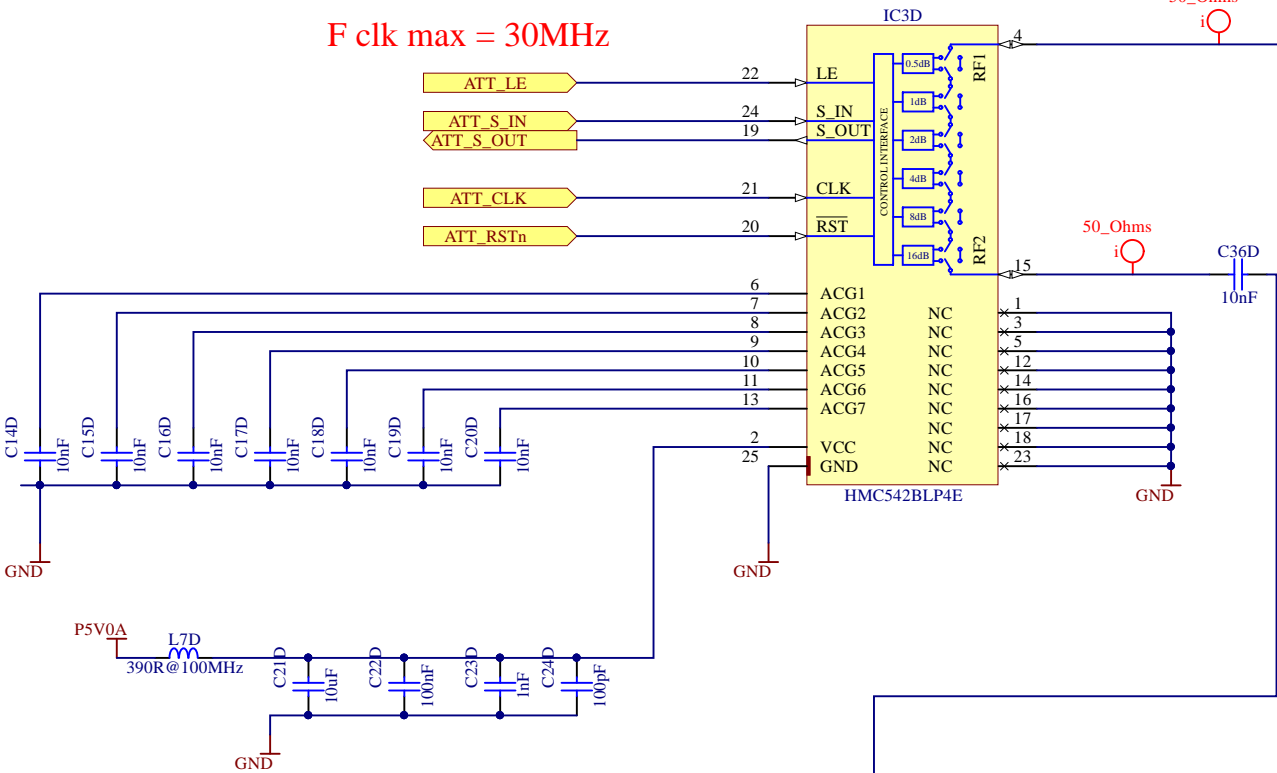
Output stage :
Attenuator, amplifier and filter
Warsaw University of Technology ISE
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ARTIQ

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28) for jumper configuration see ADC_channel sheet
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F clk max = 30MHz



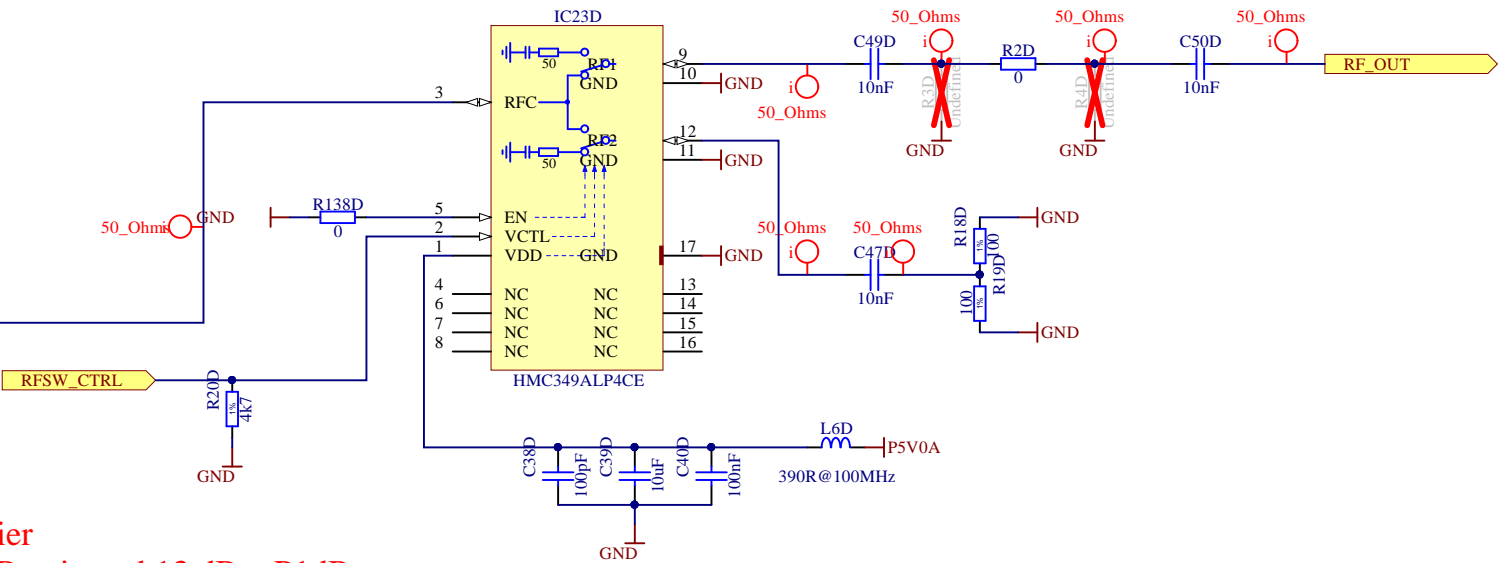
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R5 power = $65\text{mA}^2 \cdot 39 = 0.16\text{W}$

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Amplifier
~23 dB gain and 13 dBm P1dB

SPDT switch



Project/Equipment ARTIQ/SINARA

Document

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Output stage :
Attenuator, amplifier and filter

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Sheet 4 of 7
Size A3
Rev -

ARTIQ

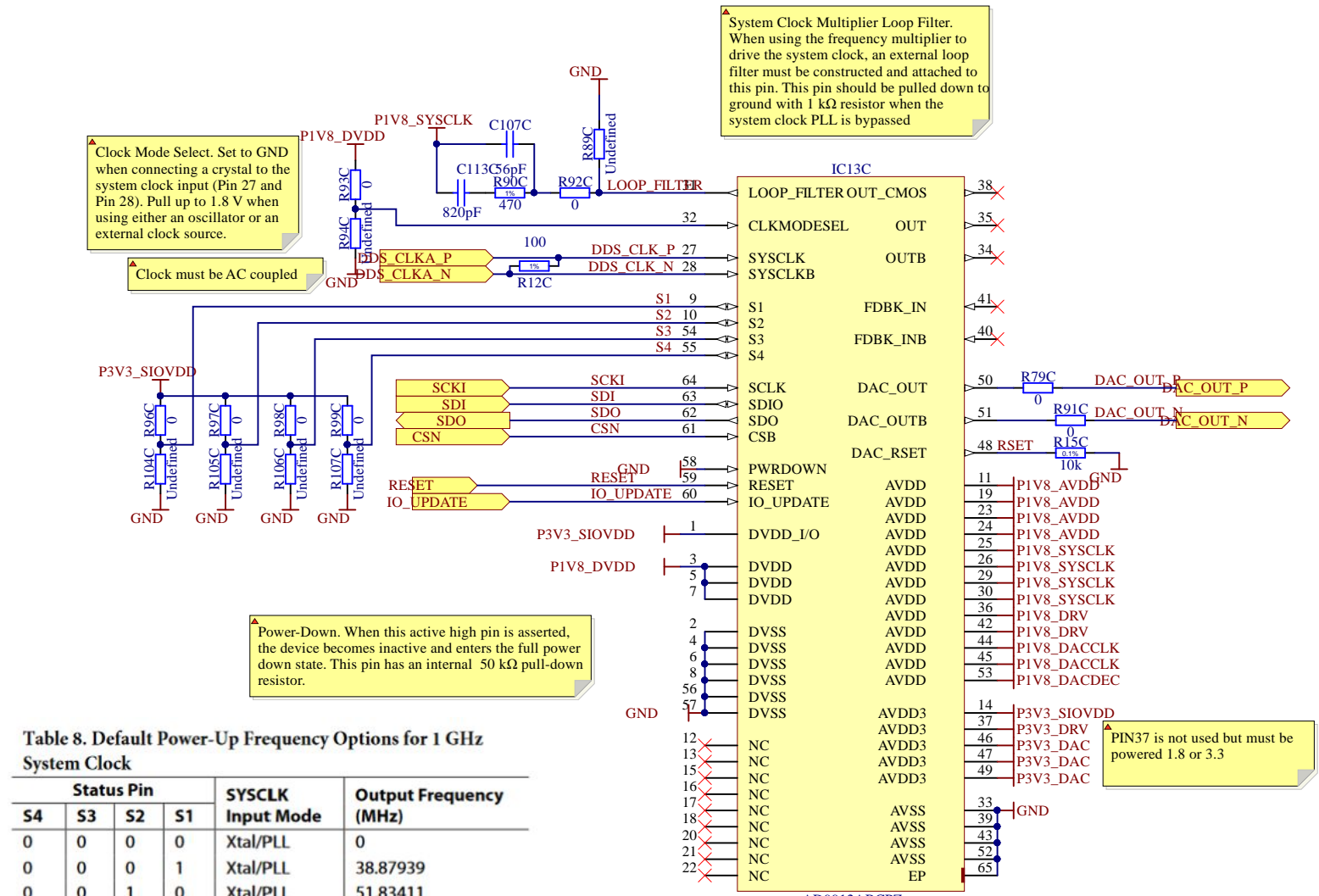
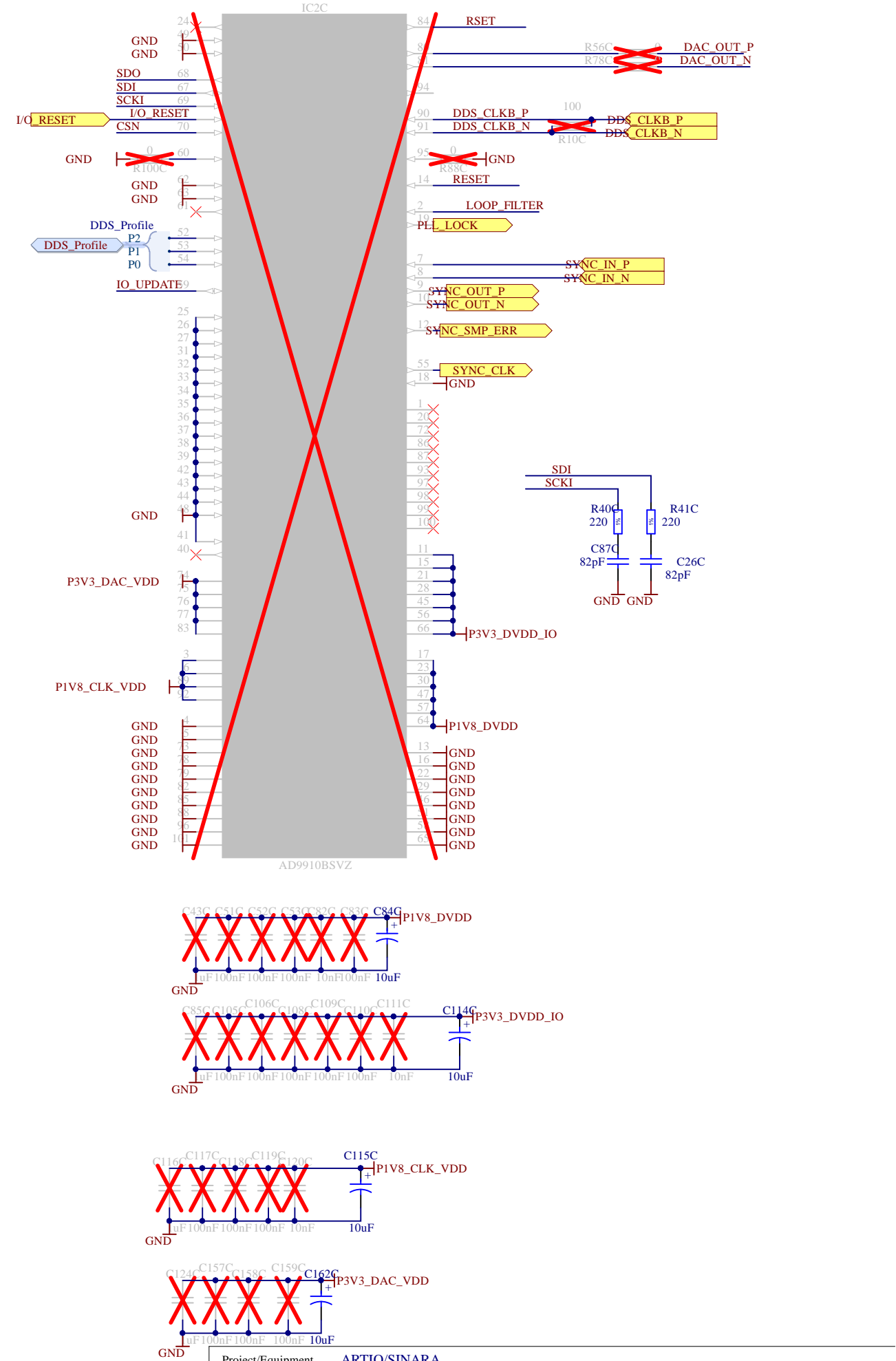


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

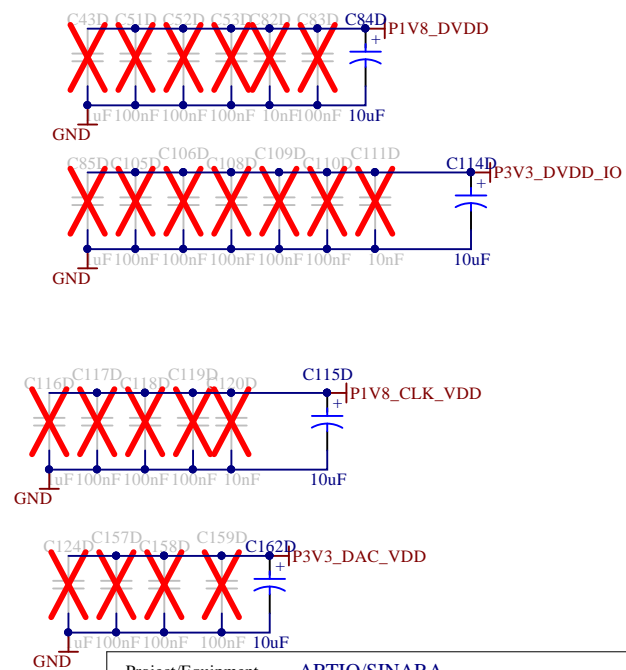
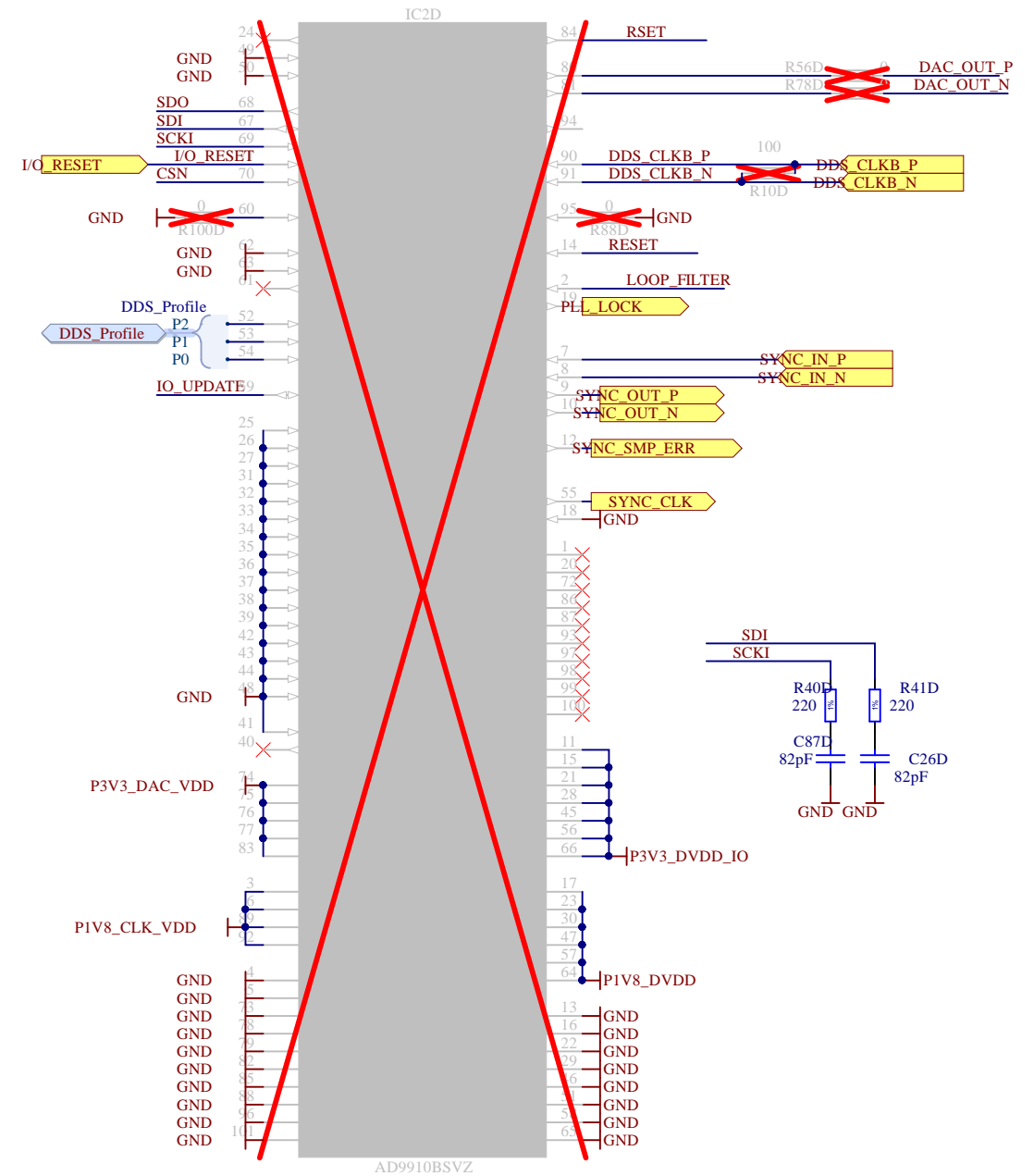
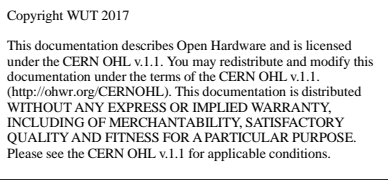
Status Pin	SYSCCLK Input Mode	Output Frequency (MHz)
S4 S3 S2 S1		
0 0 0 0	Xtal/PLL	0
0 0 0 1	Xtal/PLL	38.87939
0 0 1 0	Xtal/PLL	51.83411
0 0 1 1	Xtal/PLL	61.43188
0 1 0 0	Xtal/PLL	77.75879
0 1 0 1	Xtal/PLL	92.14783
0 1 1 0	Xtal/PLL	122.87903
0 1 1 1	Xtal/PLL	155.51758
1 0 0 0	Direct	0
1 0 0 1	Direct	38.87939
1 0 1 0	Direct	51.83411
1 0 1 1	Direct	61.43188
1 1 0 0	Direct	77.75879
1 1 0 1	Direct	92.14783
1 1 1 0	Direct	122.87903
1 1 1 1	Direct	155.51758

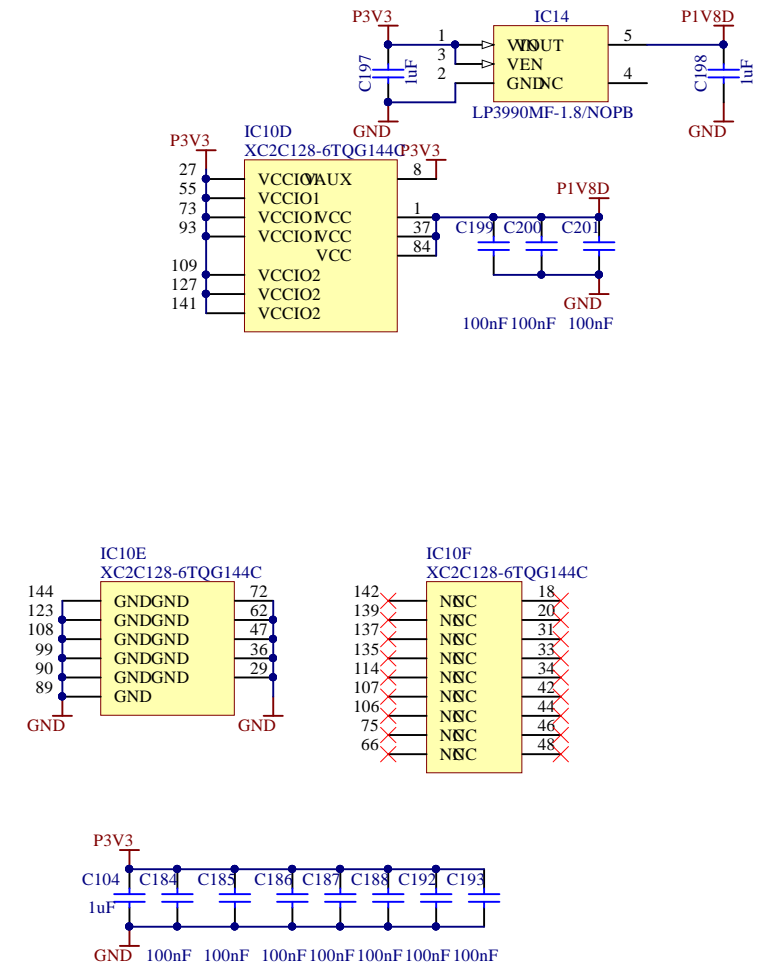
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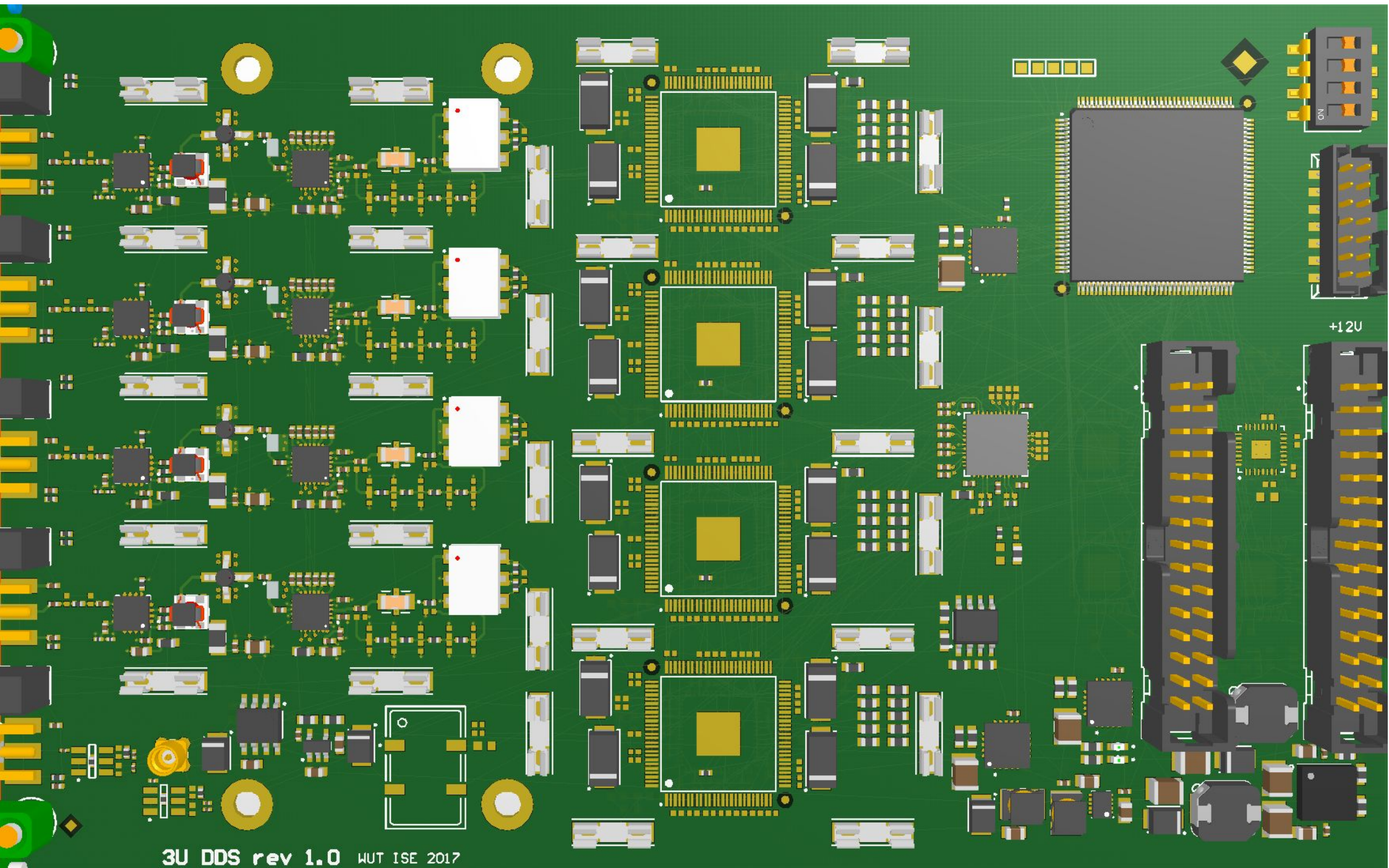
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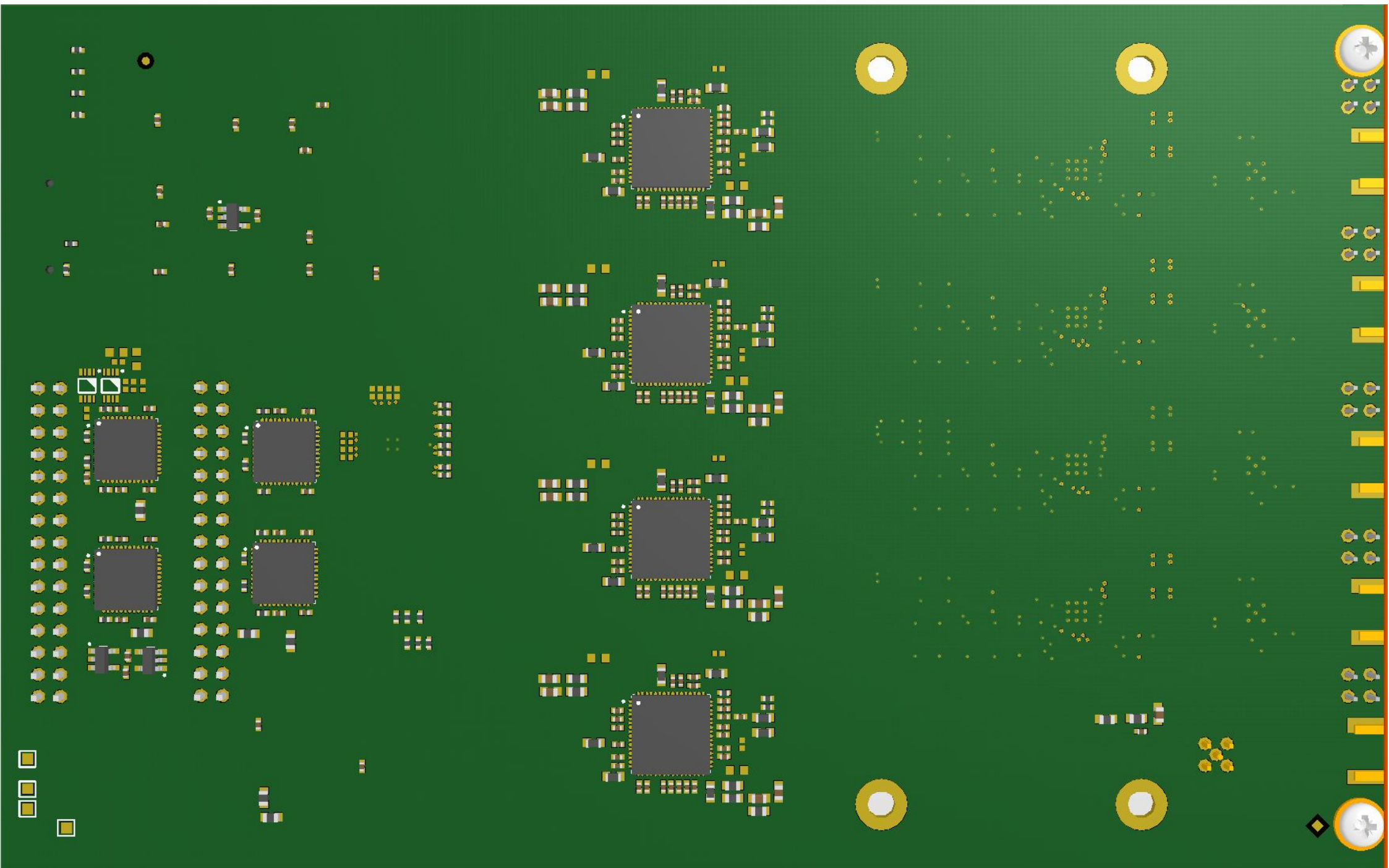
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Print Date	17.09.2017 22:38:52	Size	A3
Warsaw University of Technology ISE		ARTIQ	

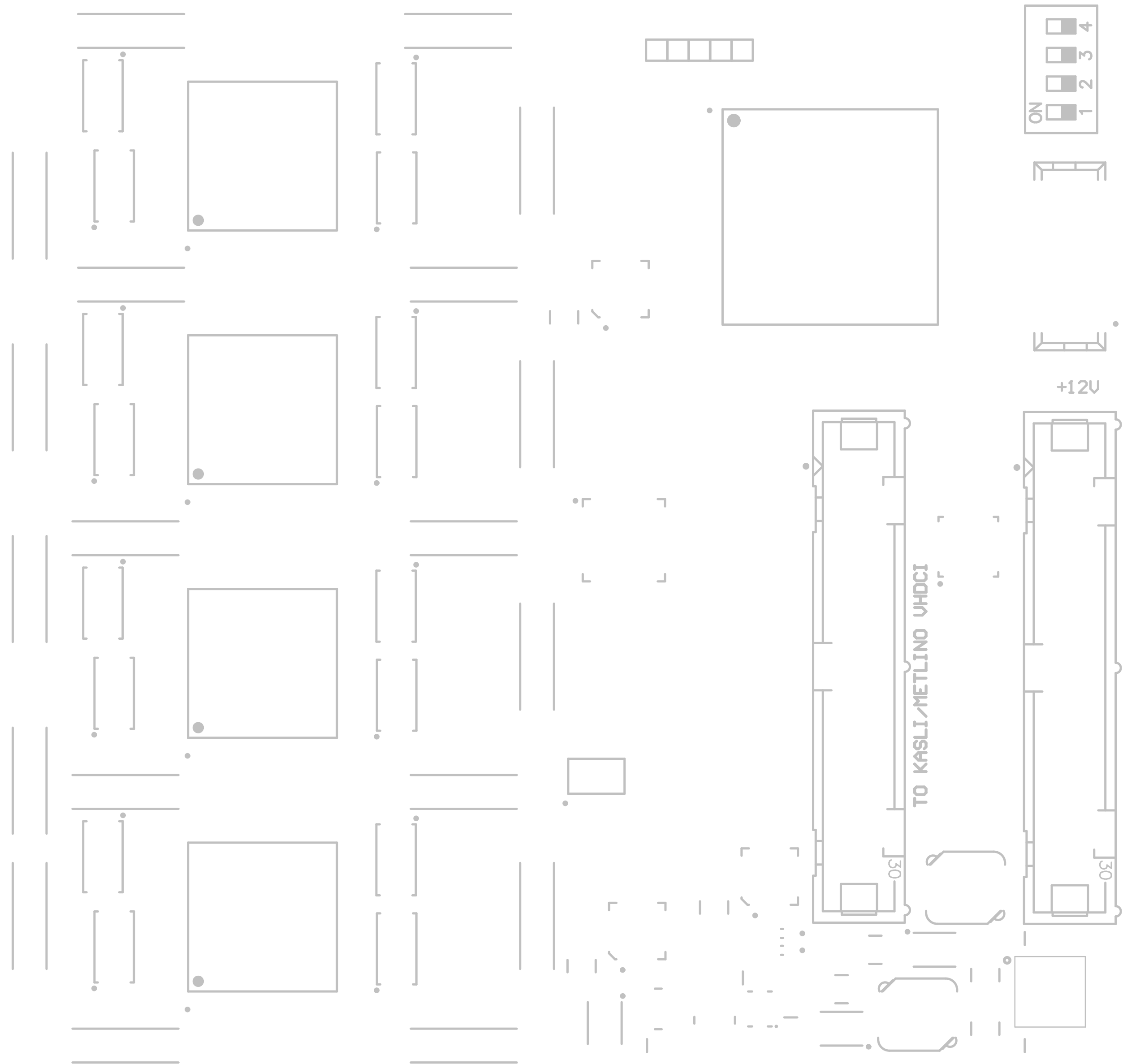


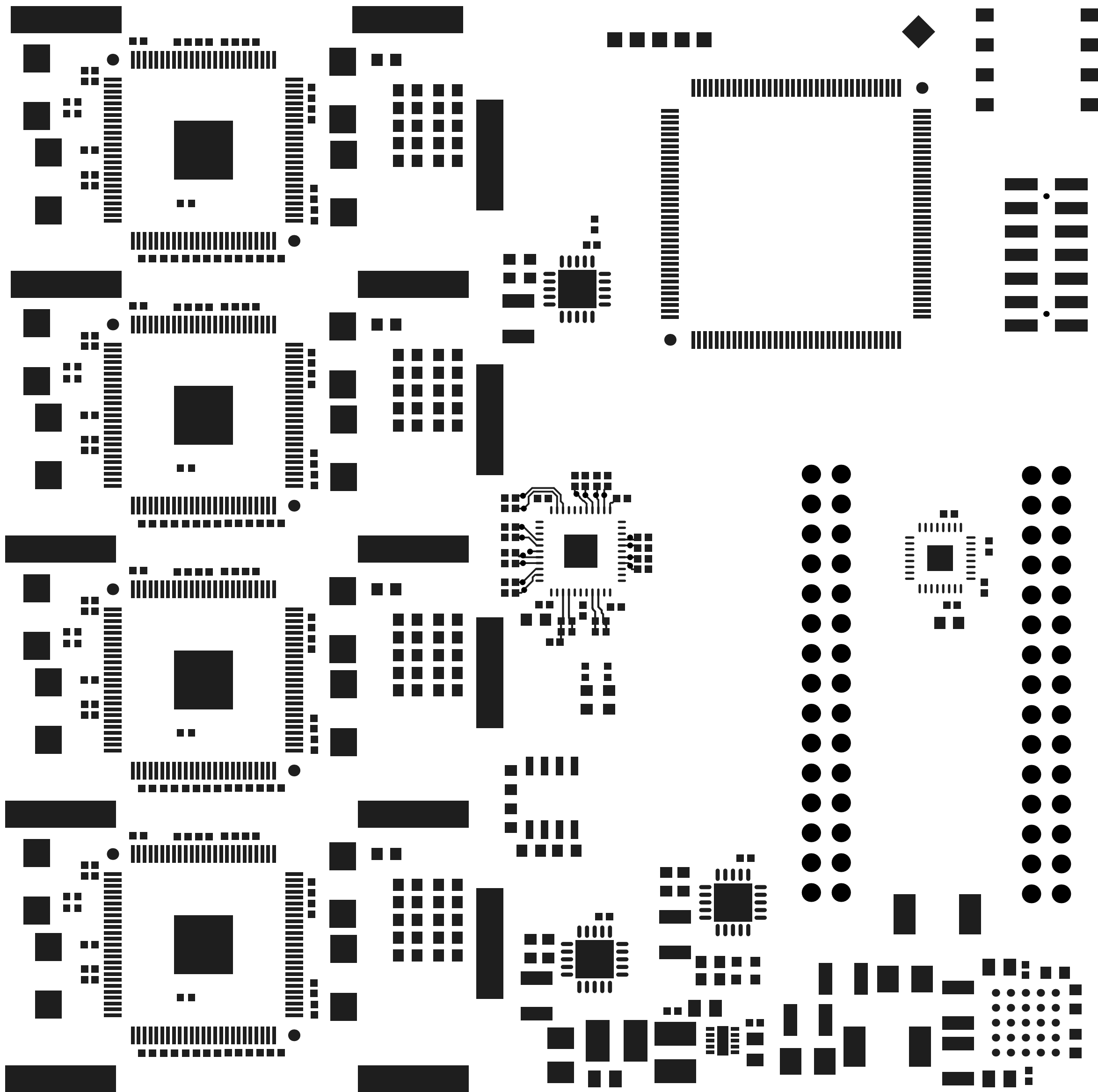
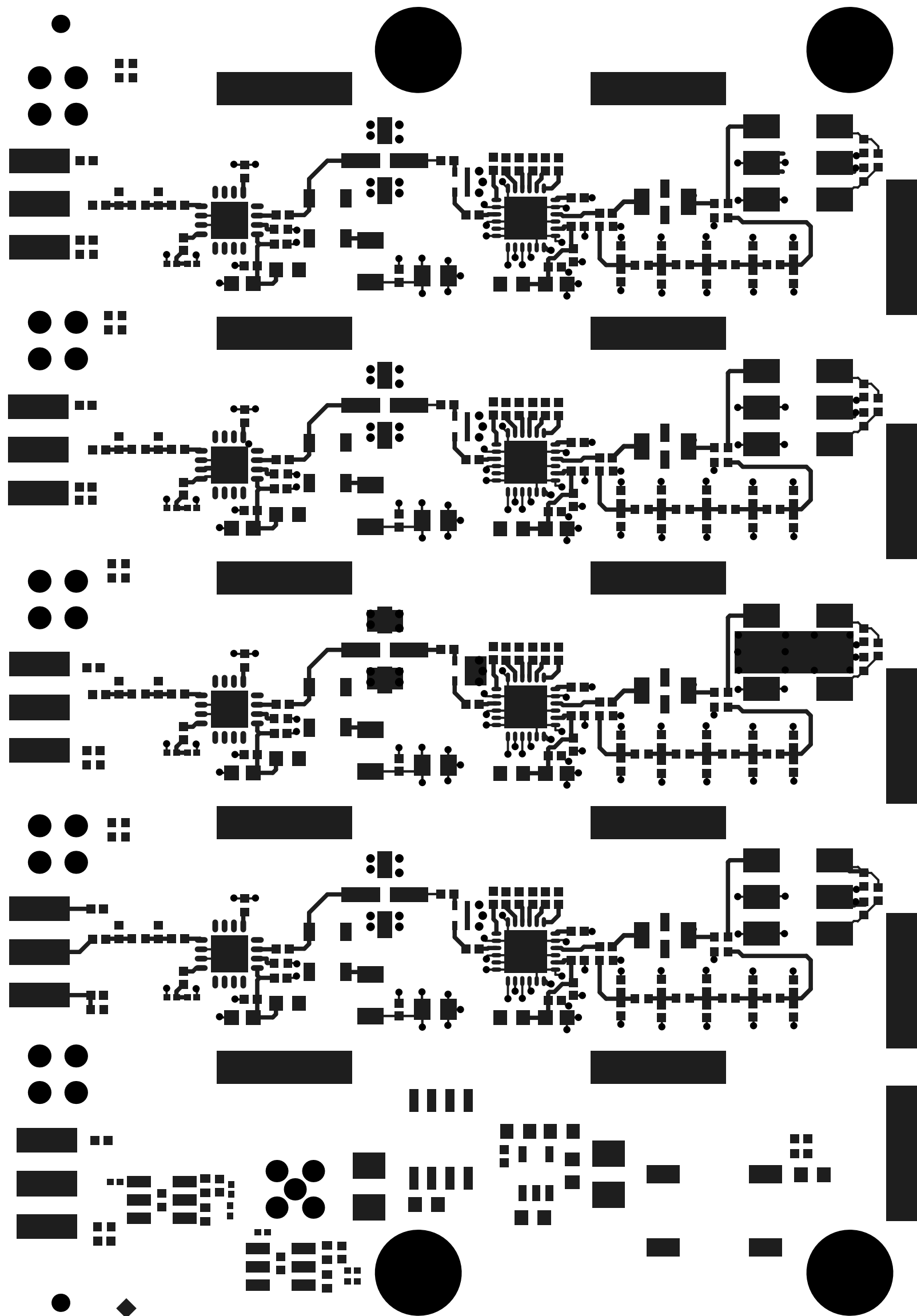


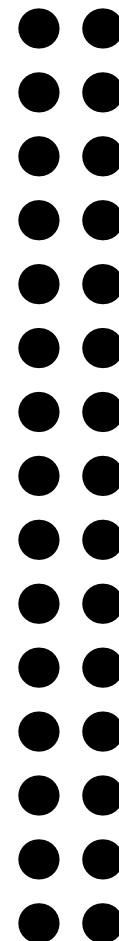
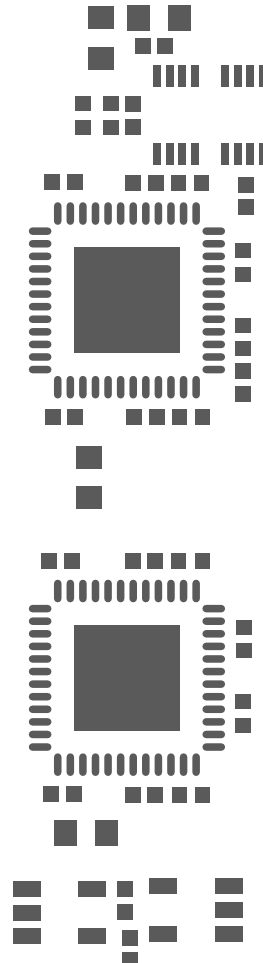
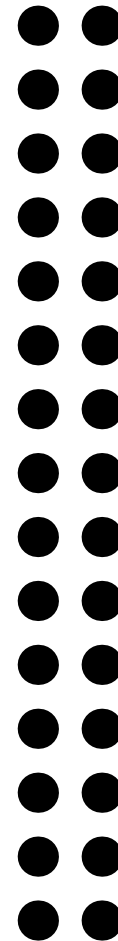
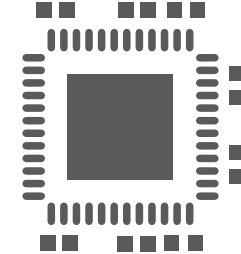
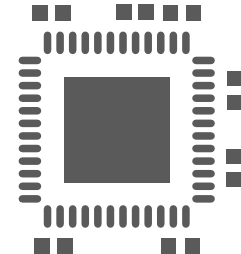
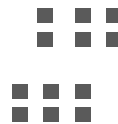
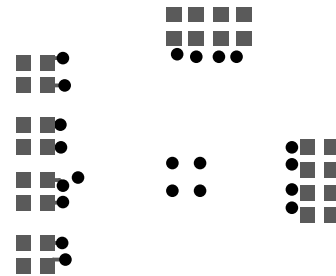
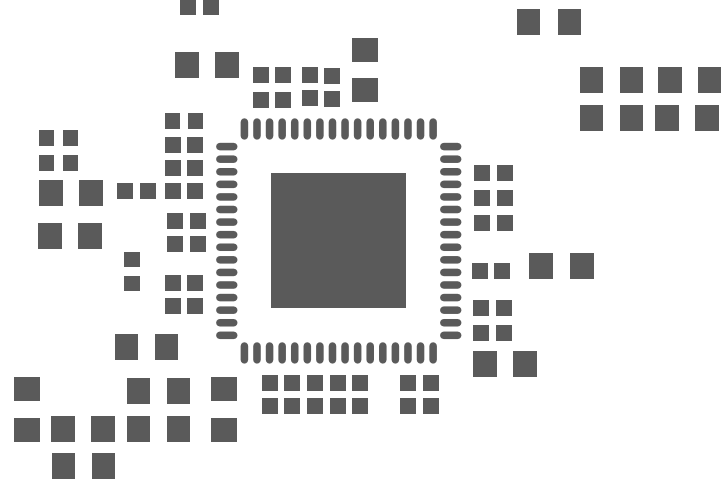
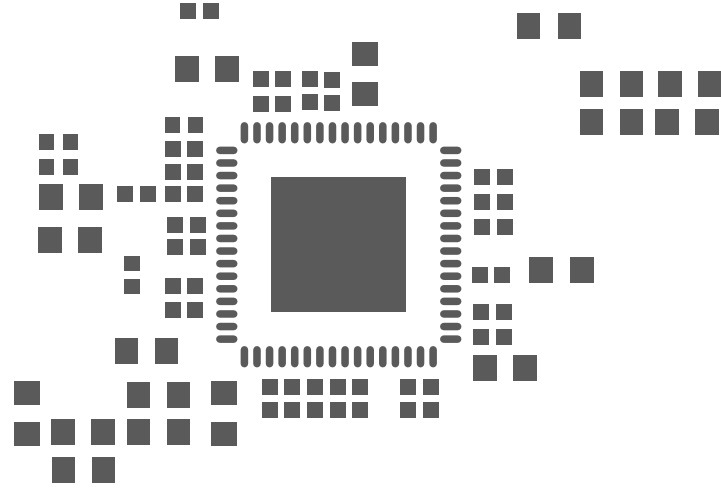
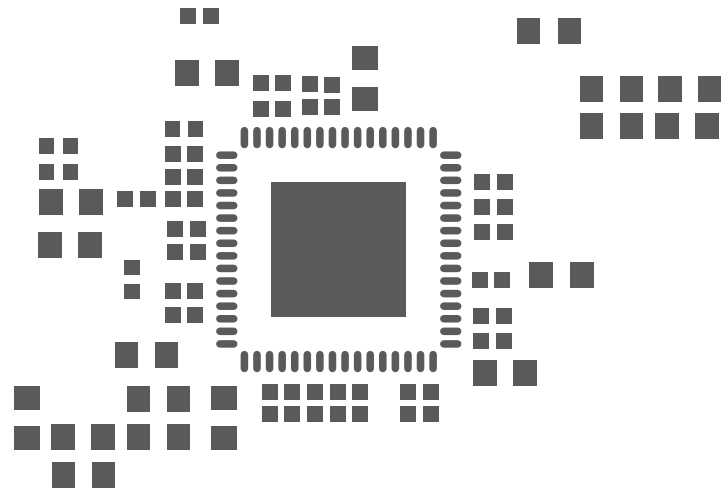
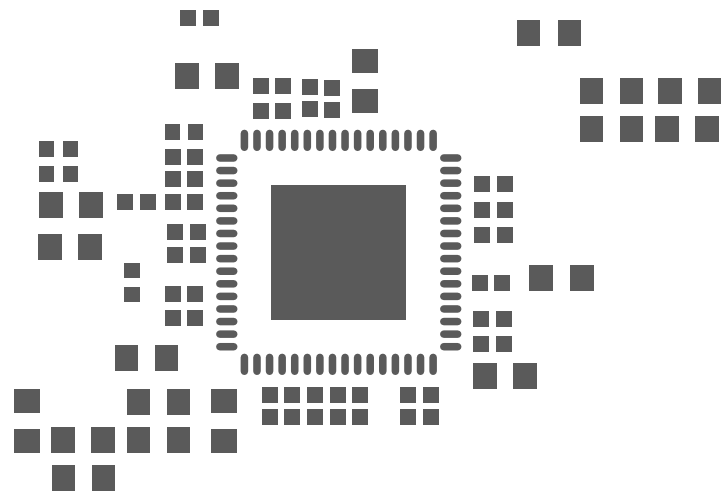
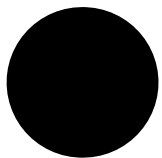
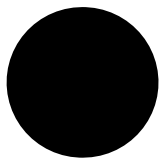
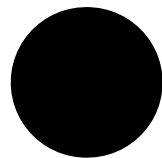
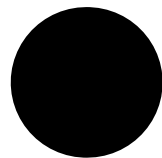
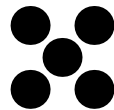
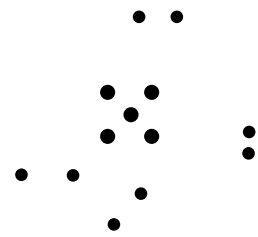
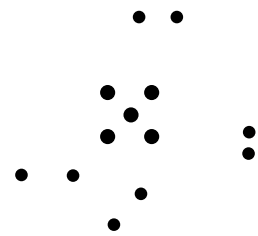
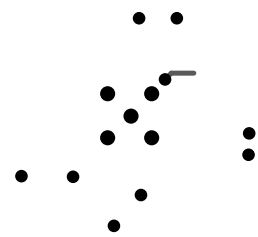
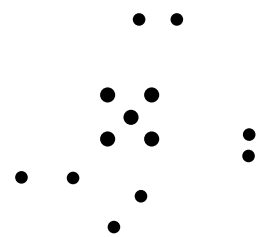
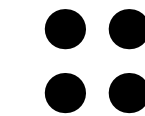
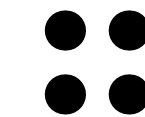
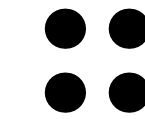
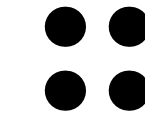
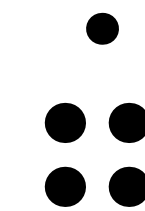


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