shield clips

CLIP1 CLIP2 CLIP3 CLIP4 CLIP5 CLIP30 CLIP31
CLIP6 CLIP7 CLIP8 CLIP9 CLIP10 CLIP27
CLIP11 CLIP12 CLIP13 CLIP14 CLIP15 CLIP28
CLIP16 CLIP17 CLIP18 CLIP19 CLIP20 CLIP29
CLIP21 CLIP22 CLIP23 CLIP24 CLIP25 CLIP26
(all GND)

Ext clock input

Internal clock input

Output SMAs

U_CLK_INPUT
CLK_INPUT.SchDoc
CK_SMA_IN, IN_SEL, CLK_DIV, INT_CLK_IN
DDS_CLKA0_P/N … DDS_CLKB3_P/N

U_CTRL_LOGIC
CTRL_LOGIC.SchDoc
RFSW_CTRL0..3, DDS_SDO/SDI/SCKI/CSN[3..0], IO_A1..A7, IO_B8_SCKI..IO_B15, DDS_UPDATE[3..0], DDS_SYNC_CLK0, DDS_PLL_LOCK[3..0], SYNC_SMP_ERR[3..0], DDS_Profile, Master_RESET, DDS_I/O_RESET, DDS_RESET[3..0], LED[7..0], ATT_CLK/LE/RSTn/S_IN/S_OUT, DDS_SYNC_CLKSEL, DDS_SYNC_OUTEN, DDS_SYNC_CLK_OUTEN
RE_DE[15..0] → RE_DE[15..01]

LVDS_IFC_DDS.SchDoc U_LVDS_IFCA
EEM 0
IO0..IO7, LVDS0_P/N, LVDS1_P/N, LVDS7_P/N, I2C_SDA, I2C_SCL, SDA, SCL
RE_DE0..RE_DE7

LVDS_IFC_DDS.SchDoc U_LVDS_IFCB
EEM 1
RE_DE8..RE_DE15

U_DDS_OUT_channel0..3
DDS_OUT_channel.SchDoc
DAC_OUT_P/N, ATT_CLK, ATT_LE, ATT_RSTn, ATT_S_IN, ATT_S_OUT, RFSW_CTRL
RF_OUT0..RF_OUT3, RFSW_CTRL0..3

U_DDS_channel0..3
DDS_channel.SchDoc
SDO, SDI, SCKI, CSN, IO_UPDATE, PLL_LOCK, SYNC_SMP_ERR, DDS_Profile, DDS_CLKA0_P/N, DDS_CLKB0_P/N, SYNC_IN_P/N, Master_RESET, I/O_RESET, RESET, SYNC_OUT_P/N, SYNC_CLK, DAC_OUT_P/N
DDS_SDO0..3, DDS_SDI0..3, DDS_SCKI0..3, DDS_CSn0..3, DDS_UPDATE0..3, DDS_PLL_LOCK0..3, SYNC_SMP_ERR0..3, DDS_CLKA0_P/N … DDS_CLKB3_P/N

IC4 FIN1101K8X (EN, GND, VCC)
IC9 Si53304-B-GM (CLK0/CLK0, CLK1/CLK1, CLK_SEL, SFOUTA0/1, SFOUTB0/1, OE0..OE5, VREF, VDD, VDDOA, VDDOB, Q0..Q5)
IC16 FIN1101K8X

DDS0_SYNC_IN_P/N, DDS1_SYNC_IN_P/N, DDS2_SYNC_IN_P/N, DDS3_SYNC_IN_P/N
DDS0_SYNC_OUT_P/N
FB_SYNC_P, FB_SYNC_N

U_Supply_DDS
Supply_DDS.SchDoc
SDA, SCL

LED0..LED7 (LD5A/B, LD6A/B, LD2A/B, LD8A/B; BOT/TOP; Green/Red)
DDS0 LEDs, DDS1 LEDs, DDS2 LEDs, DDS3 LEDs

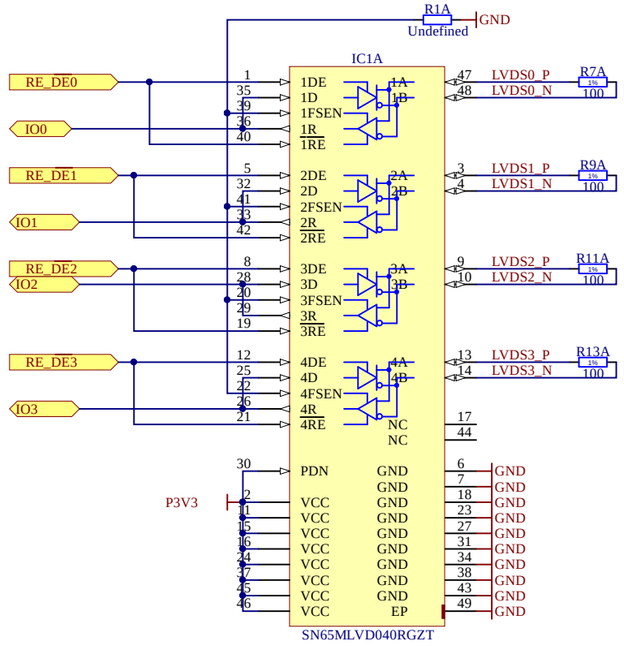
Trace lengths matched within each of DDS_SYNC_CLK[3:0], DDS_UDPATE[3:0], RF_SW_CTRL[3:0], IO[15:11] (RF_SW ctrl lines), DDS_SYNC_IN[3:0], DDS_RESET[3:0], DDS_CLK[3:0]

Project/Equipment: ARTIQ/SINARA
Document: **3U DDS (URUKUL)** *Top entity*

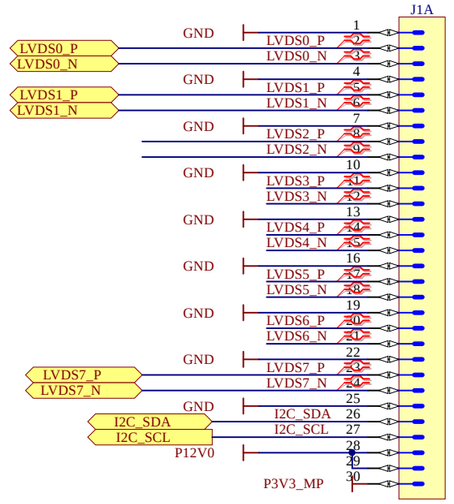
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.10.2017
File	PCB_3U_DDS.schdoc
Print Date	17.10.2017 23:26:08 Sheet 1 of 7

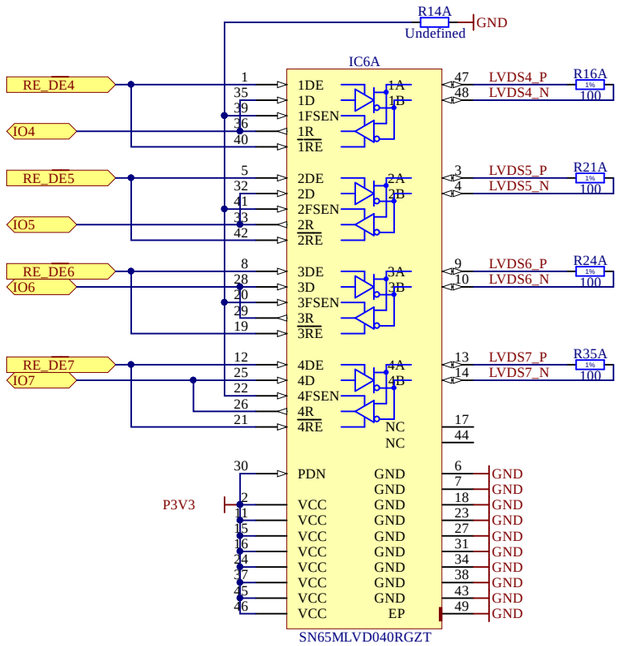
Warsaw Univeristy of Technology *Nowowiejska 15/19* *ISE*
ARTIQ — Size A3 — Rev -

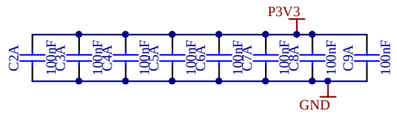
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

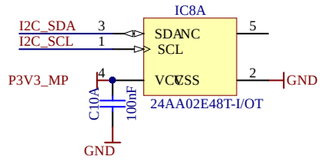


EEM Connector
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A



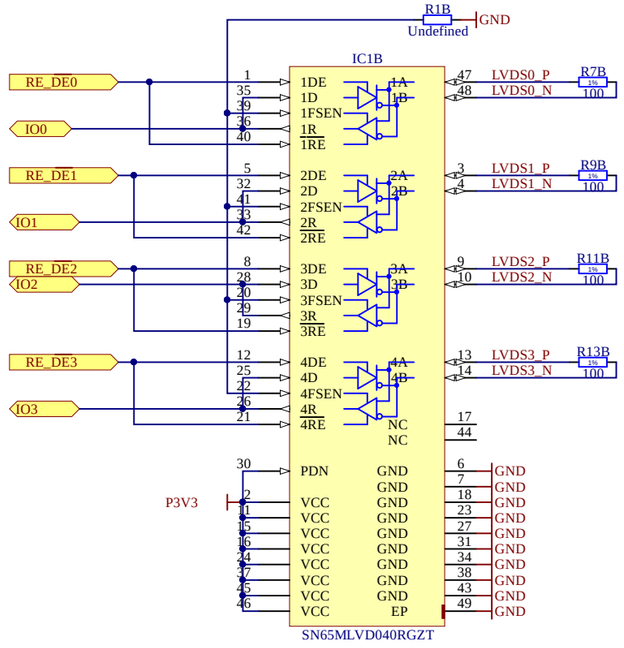






Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.10.2017
		File LVDS_IFC_DDS.SchDoc	
		Print Date 17.10.2017 23:26:08	Sheet 2 of 7
Warsaw Univeristy of Technology *Nowowiejska 15/19* *ISE*	ARTIQ	Size A3	Rev -

FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output



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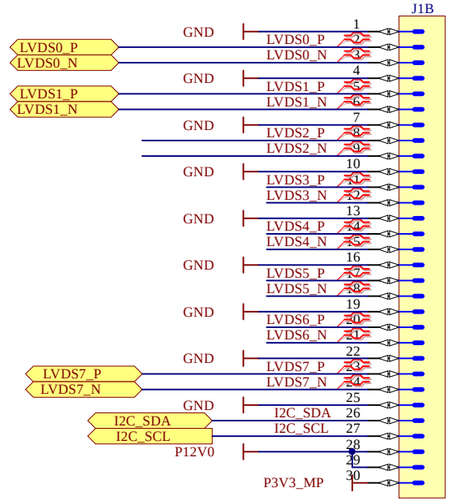
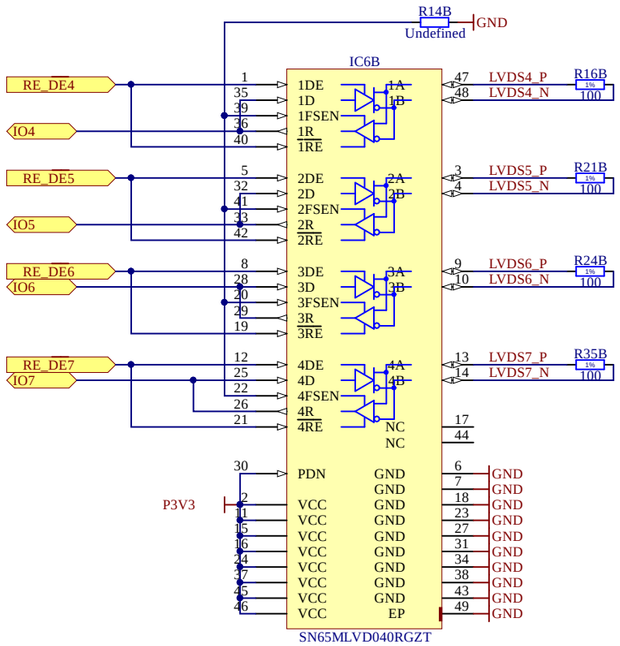
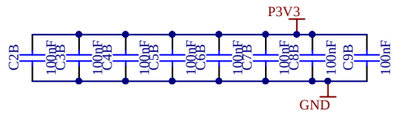
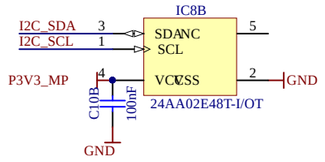
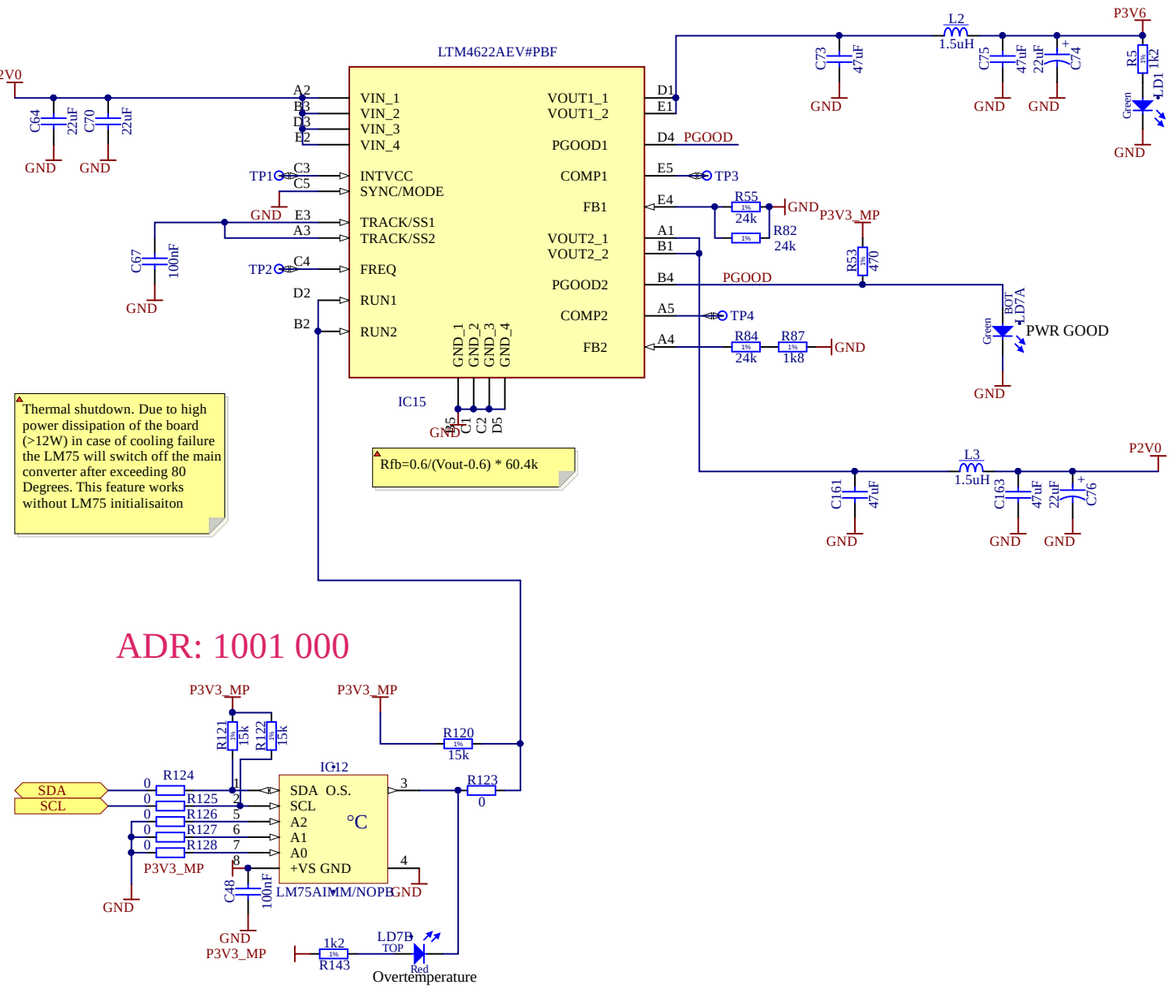


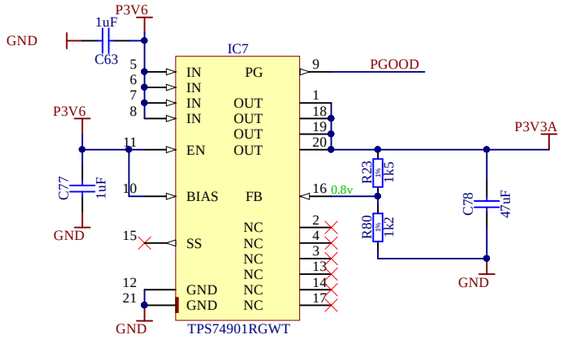


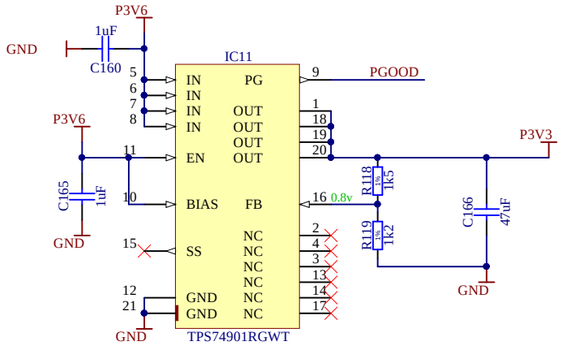


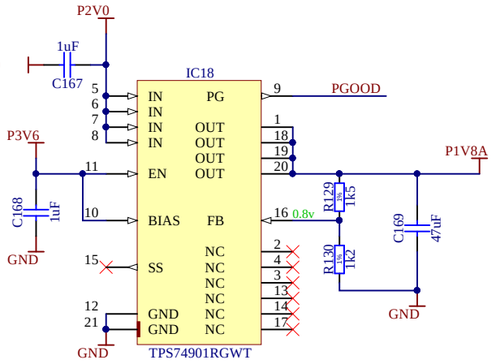


Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.10.2017
		File LVDS_IFC_DDS.SchDoc	
		Print Date 17.10.2017 23:26:08	Sheet 2 of 7
Warsaw Univeristy of Technology *Nowowiejska 15/19*	*ISE*	ARTIQ	Size A3 / Rev -

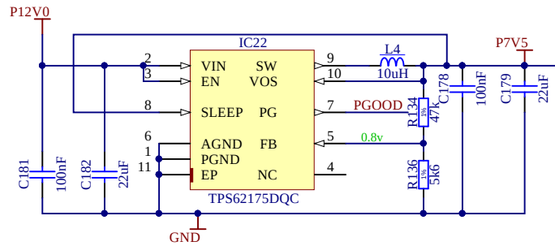


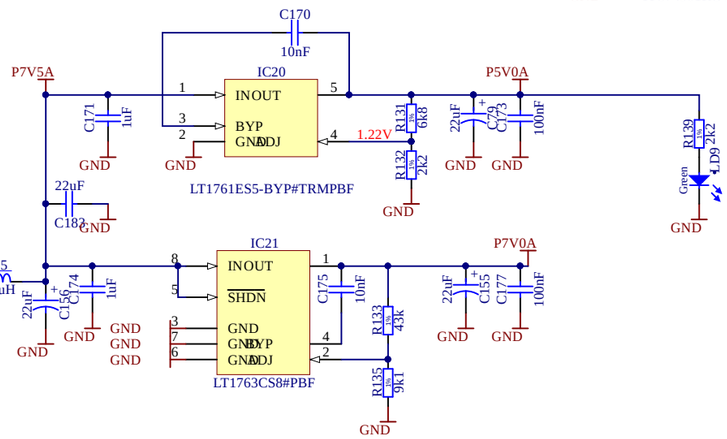


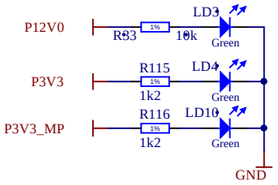




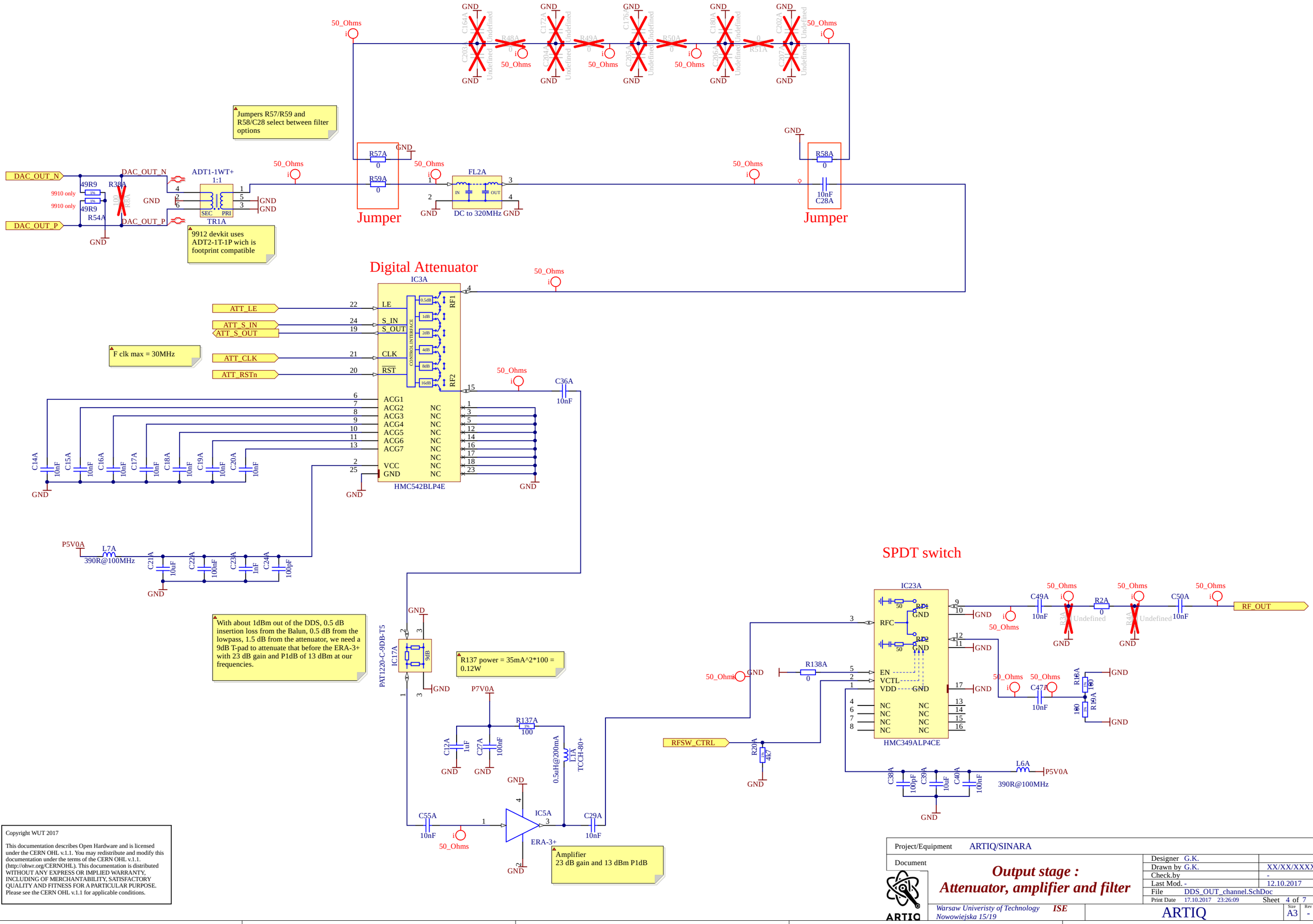
Power budget (max ratings):	AD9912 variant(mA)	AD9910 variant(mA)
P3V3:		
LVDS interface 4x	660	660
LVDS load 4x24mA	96	96
CPLD	100	100
Si53312-B-GM	240	240
Si453304	-	100
DDS AVDD3	4*(9,6+31)=133,6	4*29=116
DDS DVDDIO	4*3=12	4*11=44
TOTAL P3V3	1121	1246
TOTAL POWER	3.7	3.9
P1V8:		
DDS AVDD	4*(48+136)=736	4*110=440
DDS DVDD	4*246=984	4*222=888
TOTAL P1V8	1720	1328
TOTAL POWER	3,096	2.39
P5V0		
HMC542BLP4E	4*2.9=11.6	4*2.9=11.6
HMC349LP4C	4*3.5=14	4*3.5=14
TOTAL 5V0	25.6	25.6
TOTAL POWER	0,125	0,125
P7V0		
ERA-3XSM+	4*35=150	4*35=150
TOTAL POWER	1.05	1.05
DC/DC converter losses		
TPS62175 eff .95	0,05*(.27+0,026)*7,5=0.11	0,05*(.27+0,026)*7,5=0.11
LTM:3.6V eff .9	0.1*1,321*3,6=0,47	0,1*1,346*3,6=0,48
LTM:2V eff .87	0.13*1,721*2=0,44	0.13*1.328*2=0.34
LDO losses		
2V->1.8V	0.34	0,26
3.6V->3.3V	0.396	0.4
7.5V->7V	0,135	0,135
7.5V->5V	0,064	0,064
Total power from 12V	9.95W	9.05
Total current from 12V	0.83A	0.75A







Project/Equipment	ARTIQ/SINARA
Document	**Power supply DC/DC & LDOs**
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.10.2017
File	Supply_DDS.SchDoc
Print Date	17.10.2017 23:26:09 Sheet 3 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -


50_Ohms
GND
C164A
C203A
R48A
C172A
C204A
R49A
C176A
C205A
R50A
C180A
C206A
R51A
C207A
Jumpers R57/R59 and R58/C28 select between filter options
R57A
R59A
Jumper
FL2A
DC to 320MHz
R58A
10nF
C28A
Jumper
DAC_OUT_N
DAC_OUT_P
49R9
R38A
R54A
9910 only
ADT1-1WT+
1:1
SEC
PRI
TR1A
9912 devkit uses ADT2-1T-1P wich is footprint compatible
Digital Attenuator
IC3A
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
F clk max = 30MHz
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB
1dB
2dB
4dB
8dB
16dB
RF1
RF2
ACG1
ACG2
ACG3
ACG4
ACG5
ACG6
ACG7
NC
VCC
GND
HMC542BLP4E
C14A
C15A
C16A
C17A
C18A
C19A
C20A
10nF
C36A
P5V0A
L7A
390R@100MHz
C21A
C22A
C23A
C24A
10uF
100nF
1nF
100pF
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.
PAT1220-C-9DB-T5
IC17A
9dB
R137 power = 35mA^2*100 = 0.12W
P7V0A
R137A
100
C12A
1uF
C27A
100nF
0.5uH@200mA
L1A
TCCH-80+
C55A
C29A
IC5A
ERA-3+
Amplifier
23 dB gain and 13 dBm P1dB
SPDT switch
IC23A
RFC
RF1
RF2
EN
VCTL
VDD
HMC349ALP4CE
R138A
RFSW_CTRL
R20A
4k7
C49A
R2A
C50A
RF_OUT
C47A
R19A
C38A
C39A
C40A
L6A
Undefined
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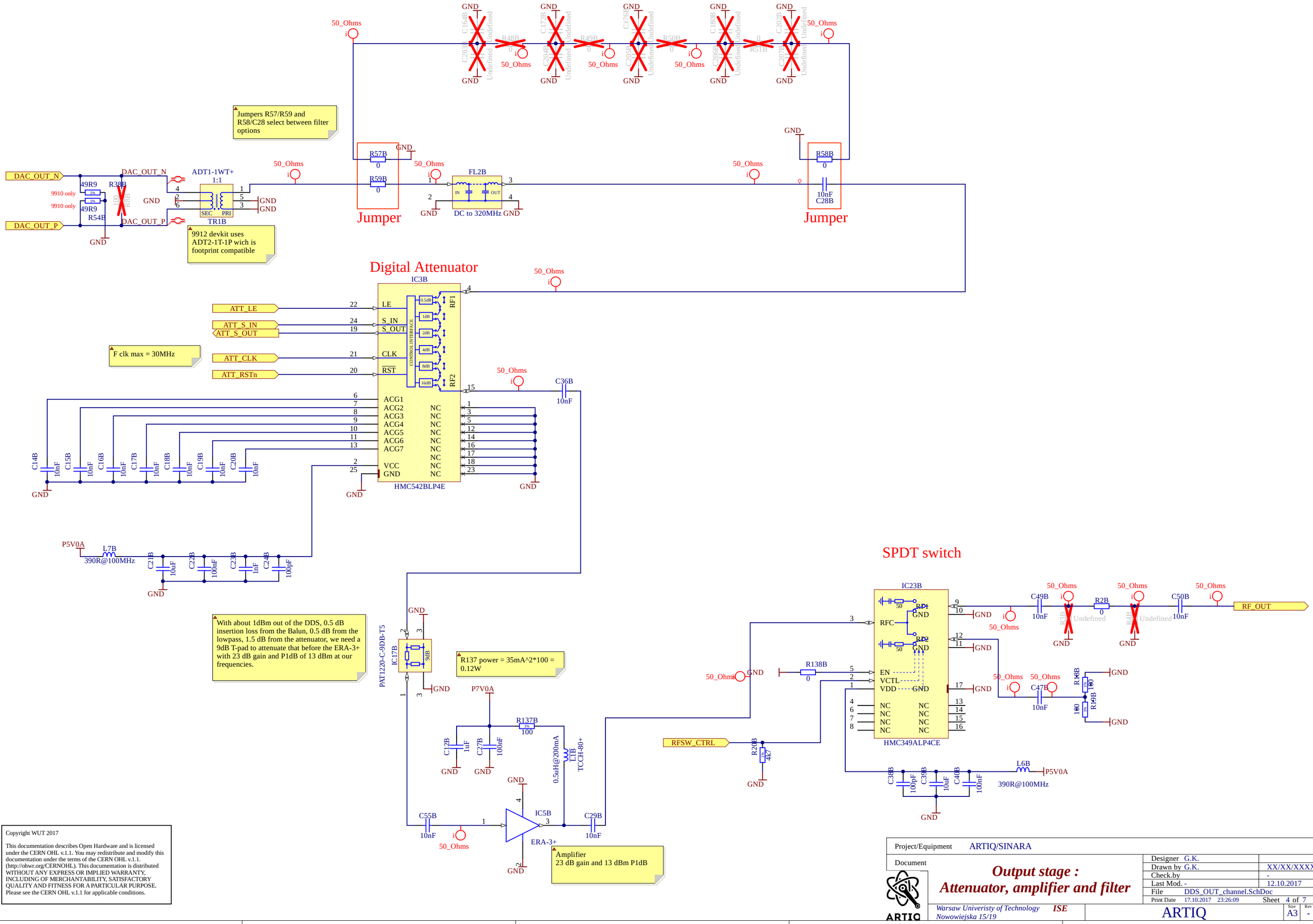
Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter
Designer G.K.
Drawn by G.K.
XX/XX/XXXX
Check.by -
Last Mod. -
12.10.2017
File DDS_OUT_channel.SchDoc
Print Date 17.10.2017 23:26:09
Sheet 4 of 7
Warsaw Univeristy of Technology
Nowowiejska 15/19
ISE
ARTIQ
Size A3
Rev -


50_Ohms
GND
C164B
C203B
R48B
C172B
C204B
R49B
C176B
C205B
R50B
C180B
C206B
R51B
C202B
C207B
Undefined
Jumpers R57/R59 and R58/C28 select between filter options
R57B
R59B
R58B
C28B
10nF
Jumper
FL2B
DC to 320MHz
DAC_OUT_N
DAC_OUT_P
49R9
R38B
R54B
9910 only
100
R58B
ADT1-1WT+
1:1
TR1B
SEC
PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible
Digital Attenuator
IC3B
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
F clk max = 30MHz
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB
1dB
2dB
4dB
8dB
16dB
RF1
RF2
ACG1
ACG2
ACG3
ACG4
ACG5
ACG6
ACG7
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VCC
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C16B
C17B
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L7B
390R@100MHz
C21B
C22B
C23B
C24B
10uF
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1nF
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With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.
IC17B
PAT1220-C-9DB-T5
9dB
R137 power = 35mA^2*100 = 0.12W
P7V0A
R137B
100
C12B
1uF
C27B
100nF
0.5uH@200mA
L1B
TCCH-80+
IC5B
ERA-3+
C55B
C29B
Amplifier
23 dB gain and 13 dBm P1dB
SPDT switch
IC23B
RFC
EN
VCTL
VDD
HMC349ALP4CE
R138B
RFSW_CTRL
R20B
4k7
C49B
R2B
C50B
RF_OUT
C47B
R46B
R45B
C38B
C39B
C40B
L6B
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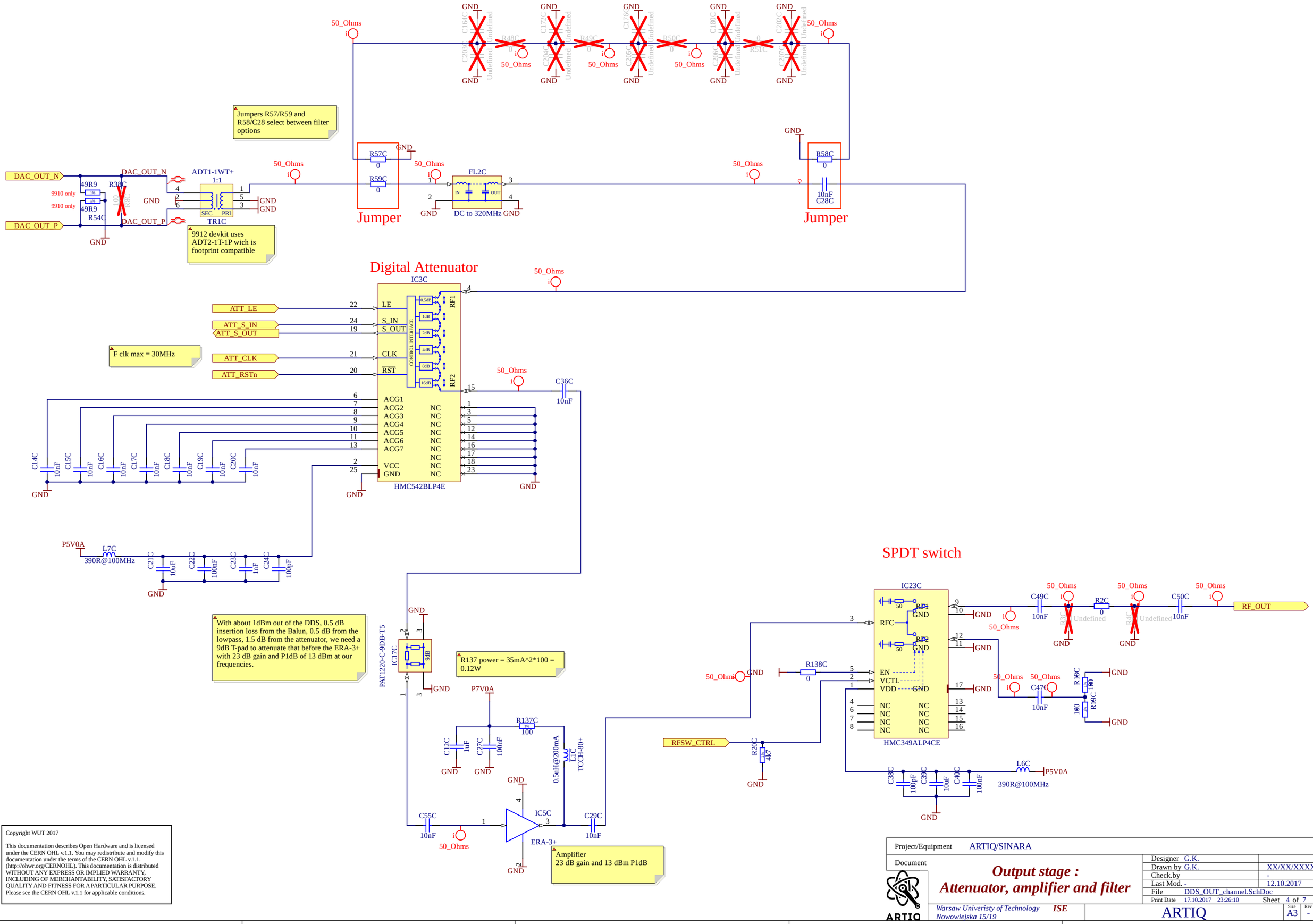
Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter
Designer G.K.
Drawn by G.K.
XX/XX/XXXX
Check.by -
Last Mod. -
12.10.2017
File DDS_OUT_channel.SchDoc
Print Date 17.10.2017 23:26:09
Sheet 4 of 7
Warsaw Univeristy of Technology
Nowowiejska 15/19
ISE
ARTIQ
Size A3
Rev -


50_Ohms
GND
C164C
C203C
R48C
C172C
C204C
R49C
C176C
C205C
R50C
C180C
C206C
R51C
C202C
C207C
Undefined
Jumpers R57/R59 and R58/C28 select between filter options
R57C
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DAC_OUT_N
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R54C
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9910 only
ADT1-1WT+
1:1
TR1C
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PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible
Digital Attenuator
IC3C
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
F clk max = 30MHz
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB
1dB
2dB
4dB
8dB
16dB
RF1
RF2
ACG1
ACG2
ACG3
ACG4
ACG5
ACG6
ACG7
NC
VCC
HMC542BLP4E
C36C
C14C
C15C
C16C
C17C
C18C
C19C
C20C
P5V0A
L7C
390R@100MHz
C21C
C22C
C23C
C24C
10uF
100nF
1nF
100pF
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.
PAT1220-C-9DB-T5
IC17C
9dB
R137 power = 35mA^2*100 = 0.12W
P7V0A
R137C
C12C
C27C
0.5uH@200mA
L1C
TCCH-80+
IC5C
ERA-3+
C55C
C29C
Amplifier
23 dB gain and 13 dBm P1dB
SPDT switch
IC23C
RFC
EN
VCTL
VDD
HMC349ALP4CE
R138C
RFSW_CTRL
R20C
4k7
C38C
C39C
C40C
L6C
C49C
R2C
C50C
RF_OUT
C47C
R46C
R47C
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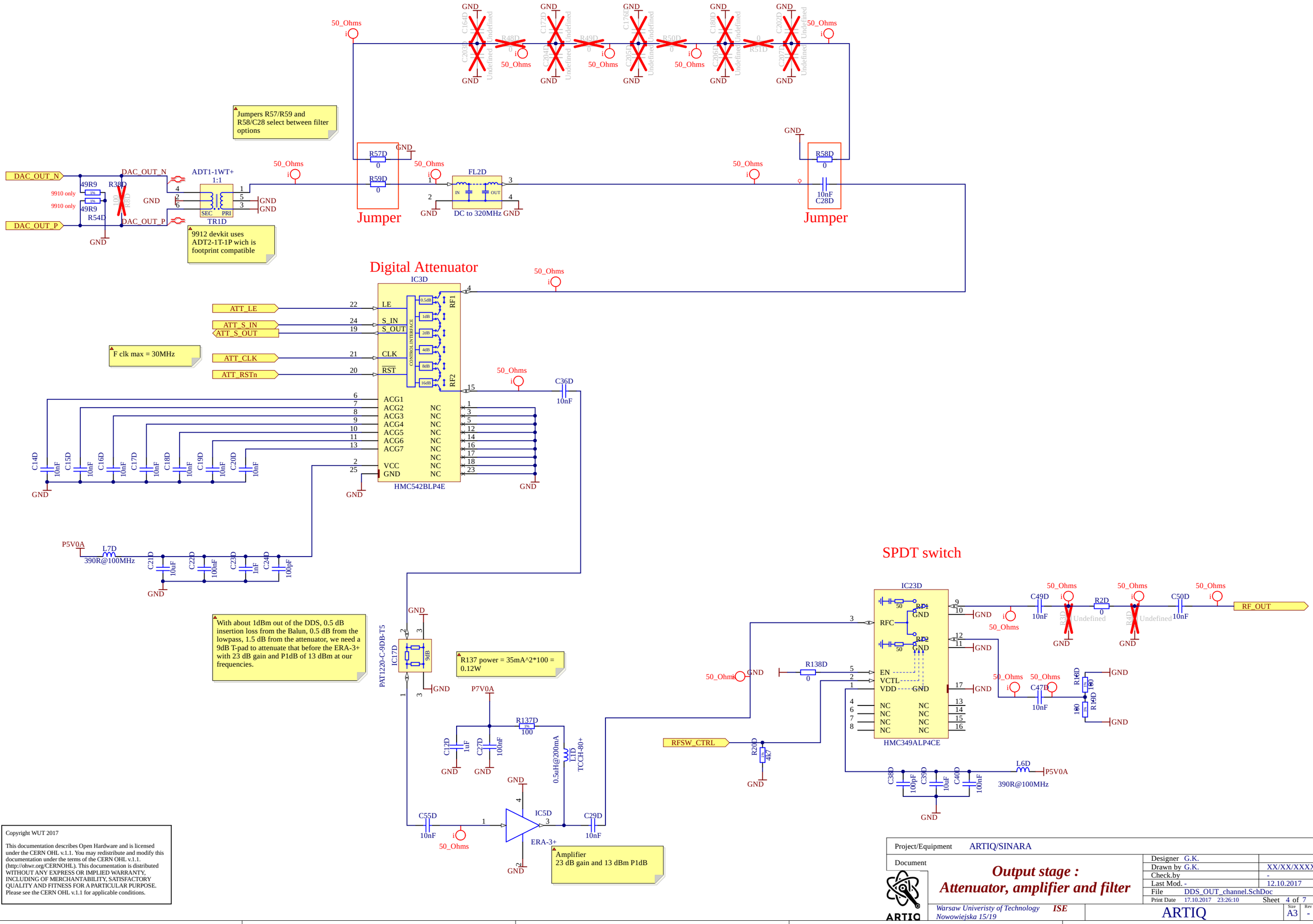
Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter
Designer G.K.
Drawn by G.K.
XX/XX/XXXX
Check.by -
Last Mod. -
12.10.2017
File DDS_OUT_channel.SchDoc
Print Date 17.10.2017 23:26:10
Sheet 4 of 7
Warsaw Univeristy of Technology
Nowowiejska 15/19
ISE
ARTIQ
Size A3
Rev -


50_Ohms
GND
C164D
C203D
R48D
C172D
C204D
R49D
C176D
C205D
R50D
C180D
C206D
R51D
C202D
C207D
Undefined
Jumpers R57/R59 and R58/C28 select between filter options
R57D
R59D
R58D
10nF
C28D
Jumper
DAC_OUT_N
DAC_OUT_P
49R9
R38D
R54D
9910 only
100
R8D
ADT1-1WT+
1:1
TR1D
SEC
PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible
FL2D
IN
OUT
DC to 320MHz
Digital Attenuator
IC3D
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB
1dB
2dB
4dB
8dB
16dB
RF1
RF2
ACG1
ACG2
ACG3
ACG4
ACG5
ACG6
ACG7
NC
VCC
GND
HMC542BLP4E
F clk max = 30MHz
C14D
C15D
C16D
C17D
C18D
C19D
C20D
10nF
C36D
P5V0A
L7D
390R@100MHz
C21D
C22D
C23D
C24D
10uF
100nF
1nF
100pF
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.
PAT1220-C-9DB-T5
IC17D
9dB
R137 power = 35mA^2*100 = 0.12W
P7V0A
R137D
100
C12D
1uF
C27D
100nF
0.5uH@200mA
L1D
TCCH-80+
C55D
IC5D
ERA-3+
C29D
Amplifier
23 dB gain and 13 dBm P1dB
SPDT switch
IC23D
RFC
RF1
RF2
EN
VCTL
VDD
HMC349ALP4CE
R138D
RFSW_CTRL
R20D
4k7
C49D
R2D
C50D
RF_OUT
C47D
R46D
R45D
C38D
C39D
C40D
L6D
390R@100MHz
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Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter
Designer G.K.
Drawn by G.K.
XX/XX/XXXX
Check.by -
Last Mod. -
12.10.2017
File DDS_OUT_channel.SchDoc
Print Date 17.10.2017 23:26:10
Sheet 4 of 7
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Nowowiejska 15/19
ISE
ARTIQ
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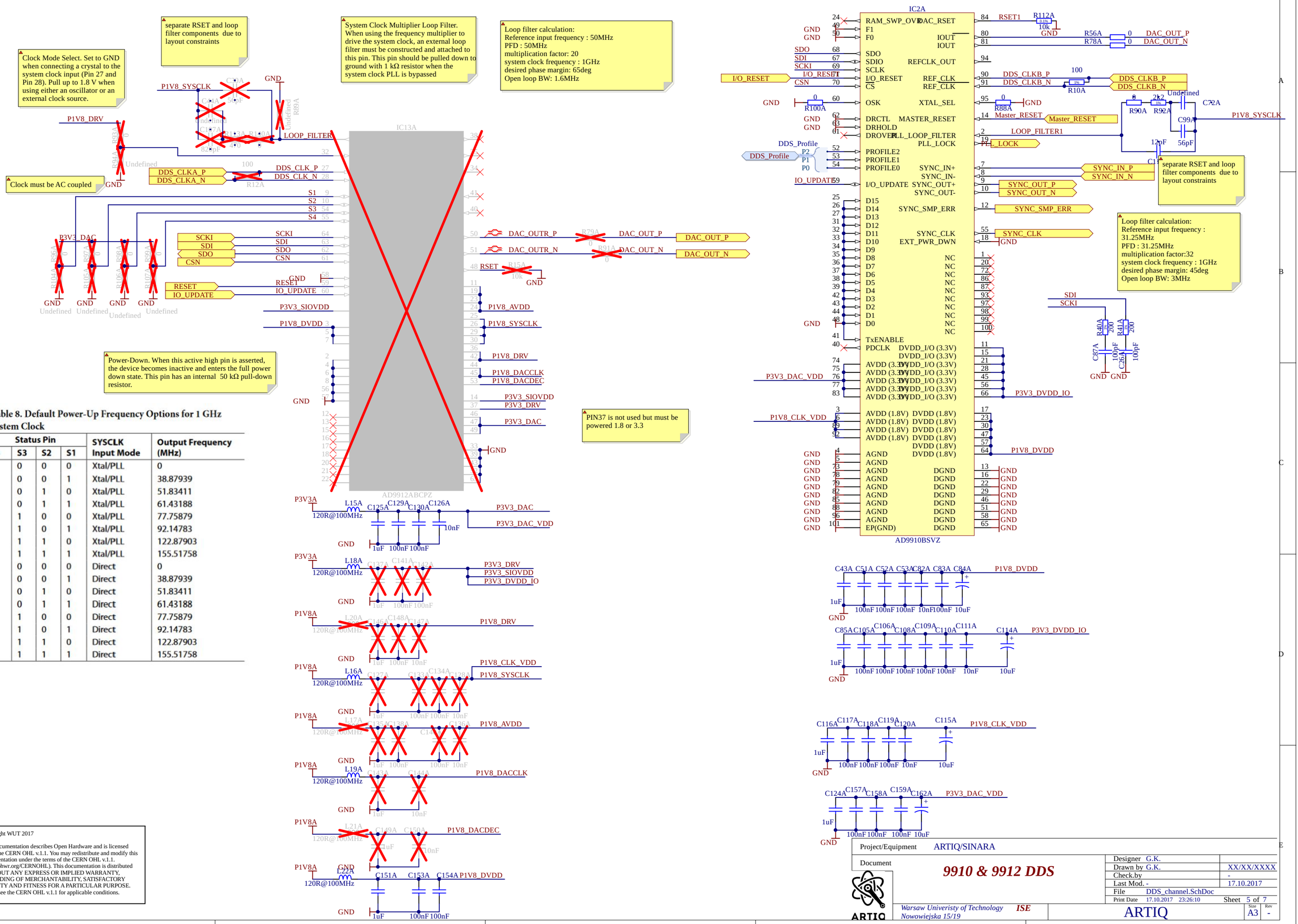

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK	Output Frequency
S4	S3	S2	S1	Input Mode	(MHz)
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.10.2017
File	DDS_channel.SchDoc
Print Date	17.10.2017 23:26:10 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

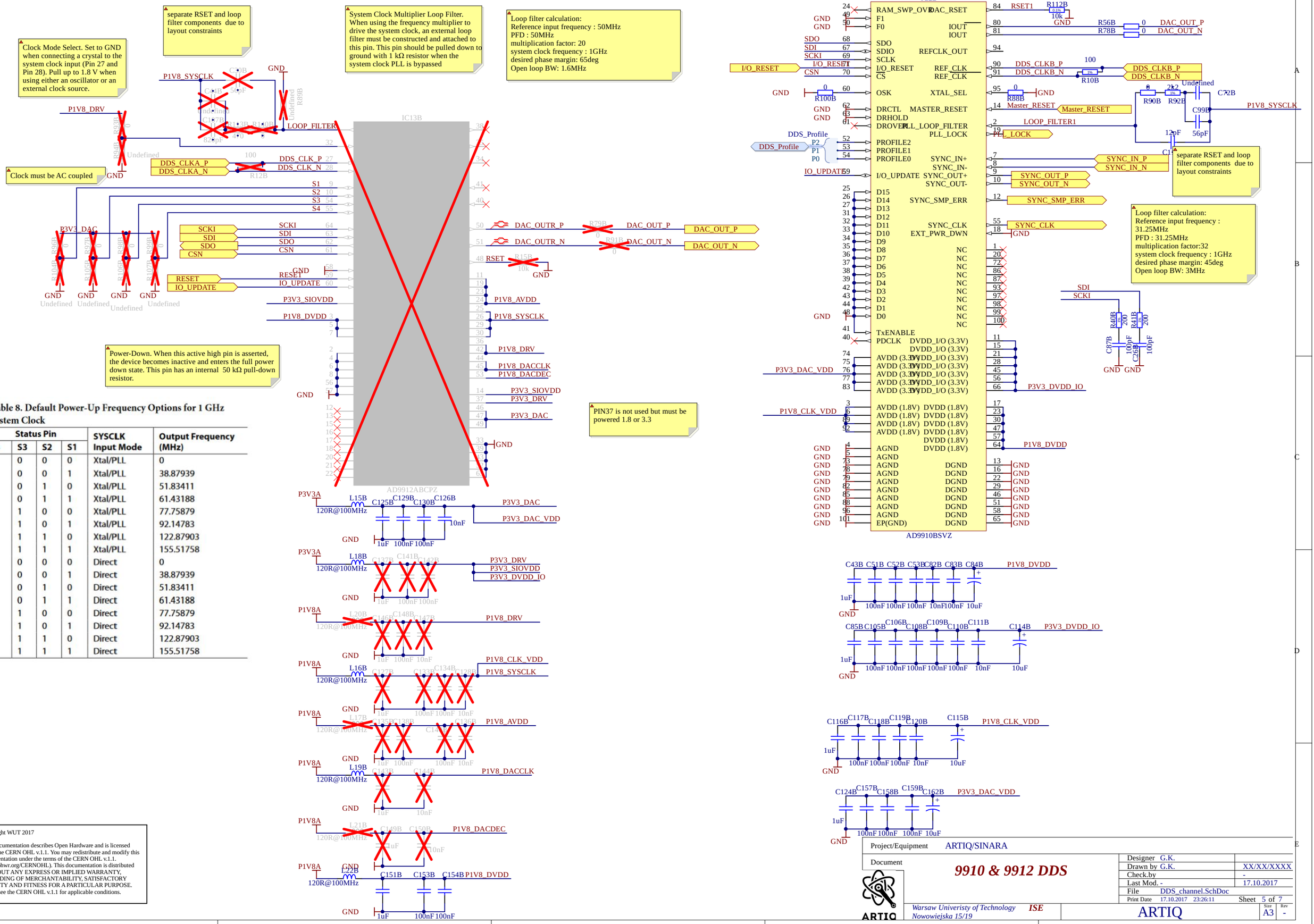

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK	Output Frequency
S4	S3	S2	S1	Input Mode	(MHz)
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K.
Check.by	-
Last Mod.	-
File	DDS_channel.SchDoc
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XX/XX/XXXX
17.10.2017

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ISE
ARTIQ

separate RSET and loop filter components due to layout constraints

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Loop filter calculation:
Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Project/Equipment ARTIQ/SINARA

Document **9910 & 9912 DDS**

Designer G.K.	
Drawn by G.K.	XX/XX/XXXX
Check.by	-
Last Mod. -	17.10.2017
File DDS_channel.SchDoc	
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Warsaw Univeristy of Technology ISE
Nowowiejska 15/19

ARTIQ

Size A3 | Rev -

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Loop filter calculation:
Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

Loop filter calculation:
Reference input frequency : 31.25MHz
PFD : 31.25MHz
multiplication factor:32
system clock frequency : 1GHz
desired phase margin: 45deg
Open loop BW: 3MHz

separate RSET and loop filter components due to layout constraints

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK	Output Frequency
S4	S3	S2	S1	Input Mode	(MHz)
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.10.2017
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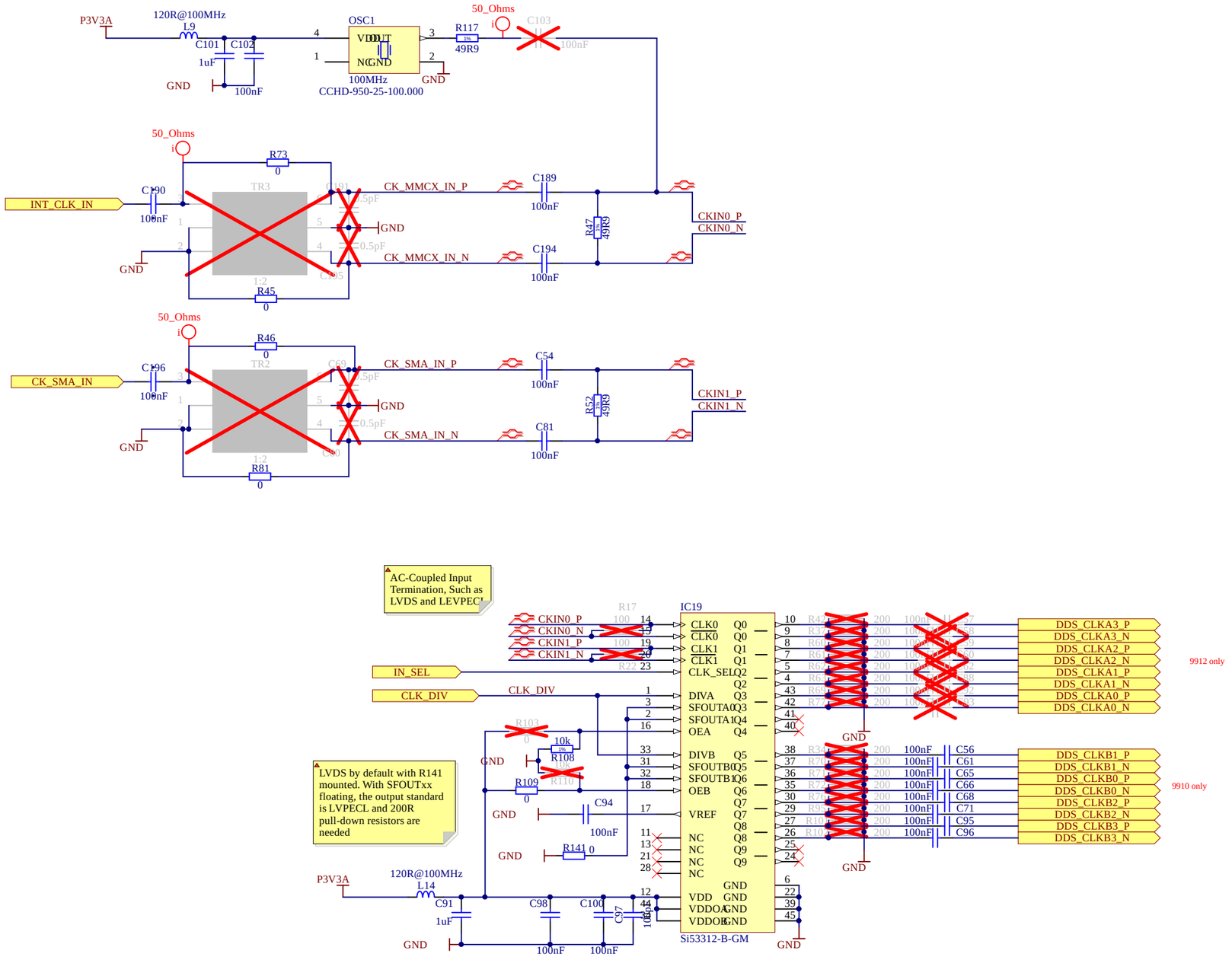
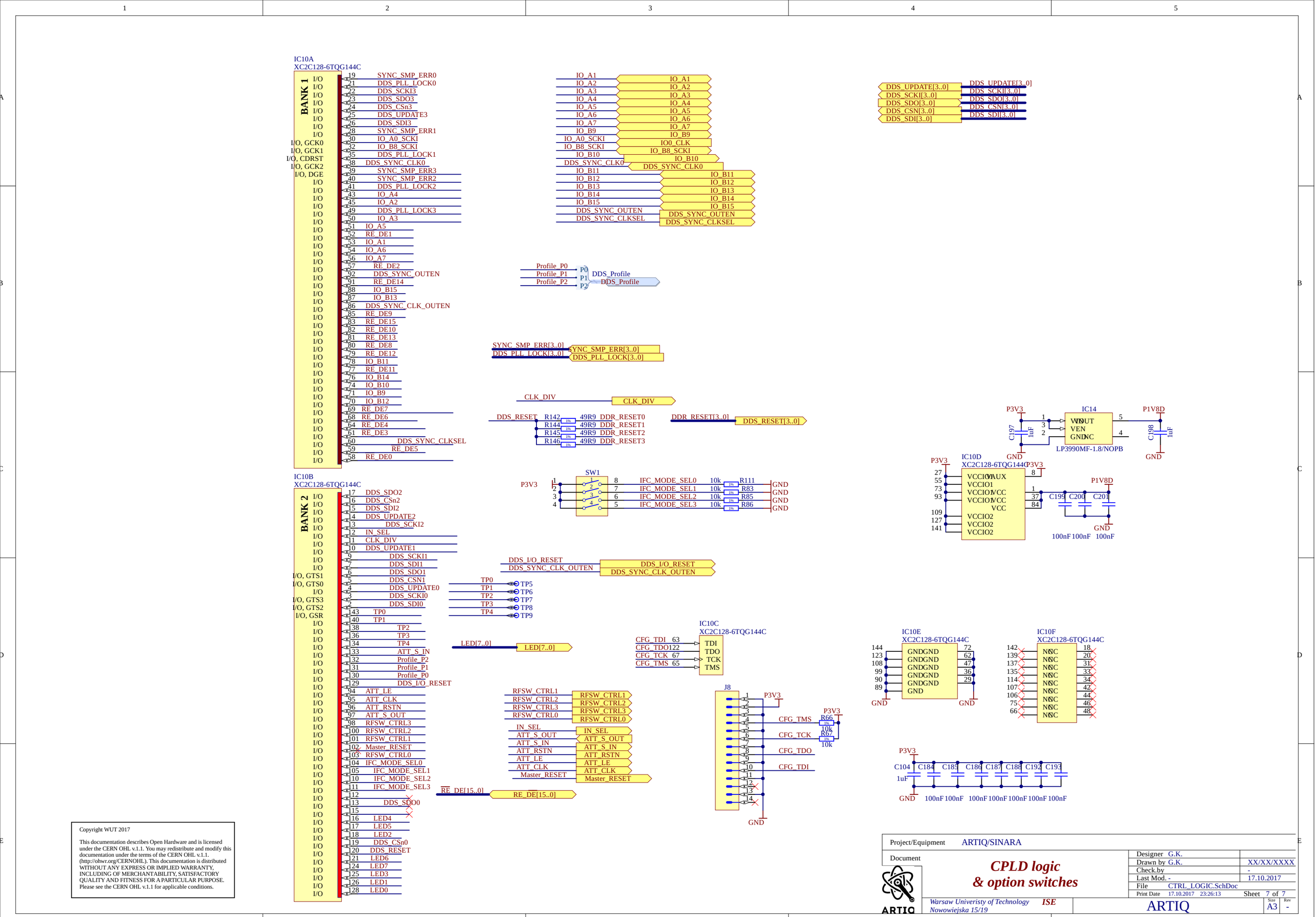
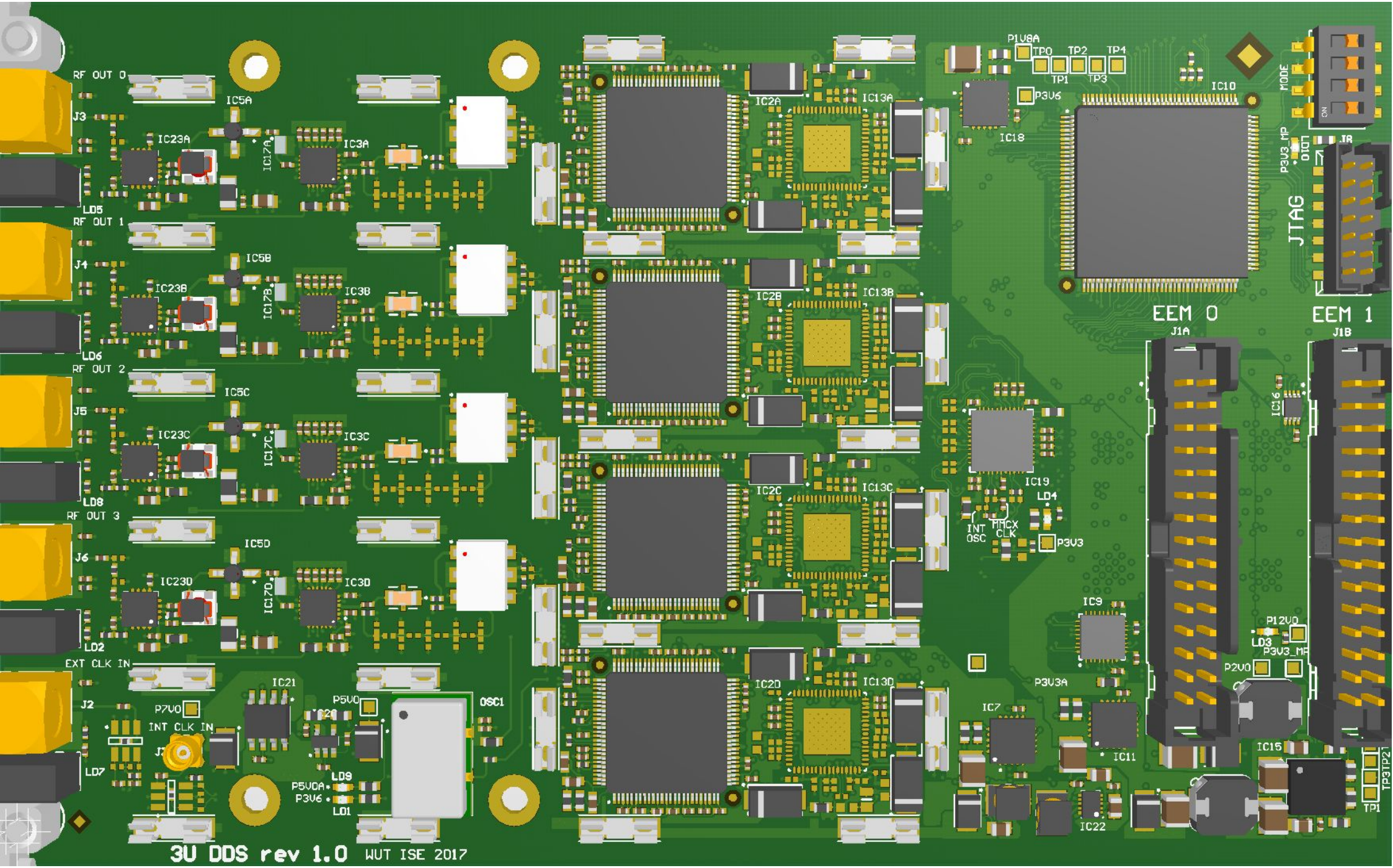
Print Date	17.10.2017 23:26:12 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

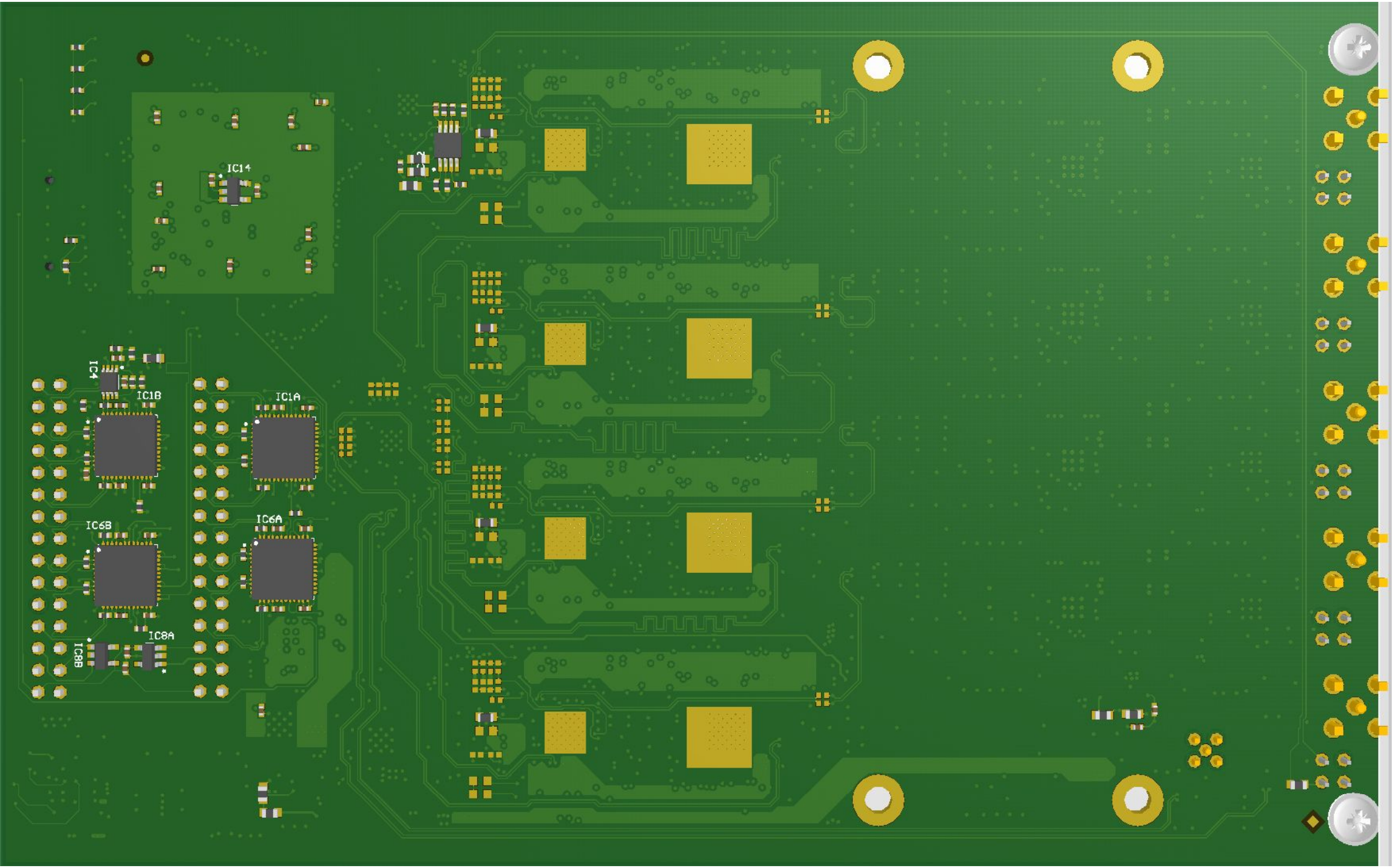


Project/Equipment	ARTIQ/SINARA		
Document	**Clock distribution and generation**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.10.2017
		File CLK_INPUT.SchDoc	
		Print Date 17.10.2017 23:26:12	Sheet 6 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19 ISE	ARTIQ	Size A3	Rev -



Project/Equipment	ARTIQ/SINARA		
Document	**CPLD logic & option switches**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.10.2017
		File CTRL_LOGIC.SchDoc	
		Print Date 17.10.2017 23:26:13	Sheet 7 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	*ISE*	ARTIQ	Size A3 / Rev -


RF OUT 0
RF OUT 1
RF OUT 2
RF OUT 3
EXT CLK IN
INT CLK IN
3U DDS rev 1.0
WUT ISE 2017
EEM 0
EEM 1
JTAG
MODE
P1V8A
P3V6
P3V3
P3V3A
P5V0
P7V0
P2V0
P12V0
P3V3_MP
INT OSC
MMCX CLK
OSC1
TP0
TP1
TP2
TP3
TP4
J1A
J1B
J3
J4
J5
J6
J2
IC2A
IC2B
IC2C
IC2D
IC3A
IC3B
IC3C
IC3D
IC5A
IC5B
IC5C
IC5D
IC7
IC9
IC10
IC11
IC13A
IC13B
IC13C
IC13D
IC15
IC16
IC18
IC19
IC21
IC22
IC23A
IC23B
IC23C
IC23D
LD1
LD2
LD3
LD4
LD5
LD6
LD7
LD8
LD9


IC14
IC4
IC1B
IC1A
IC6B
IC6A
IC8A
IC8B

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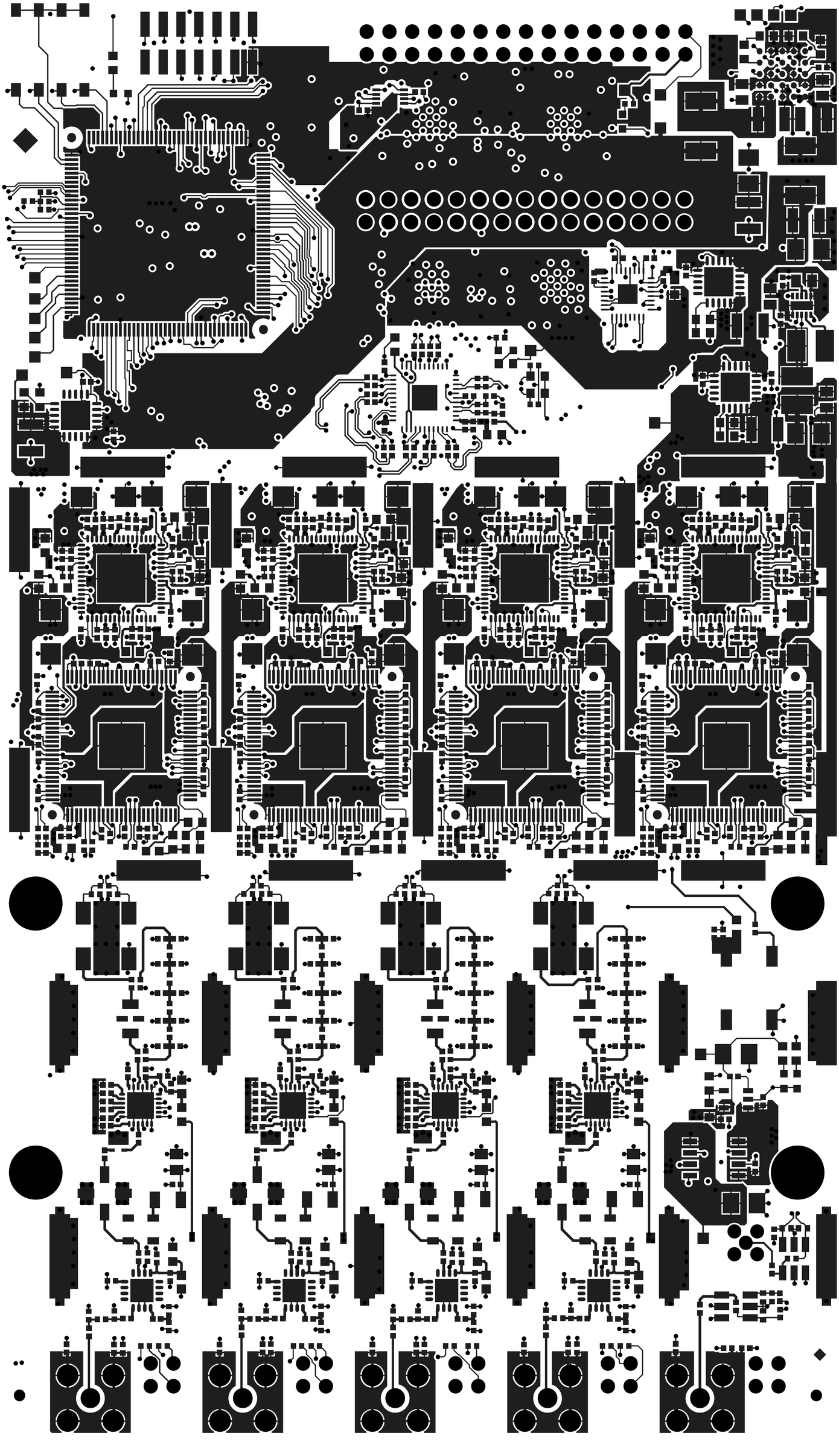
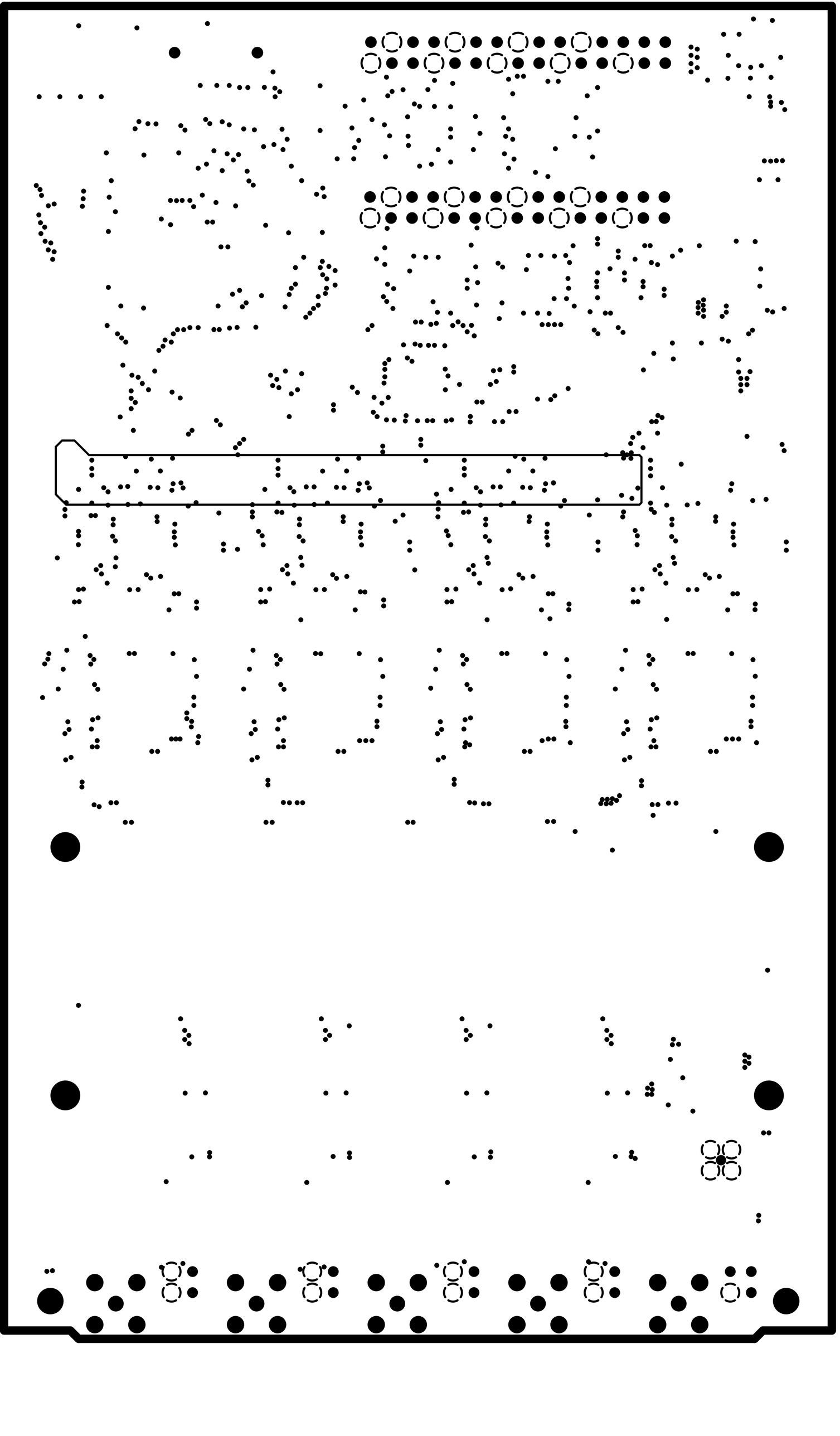
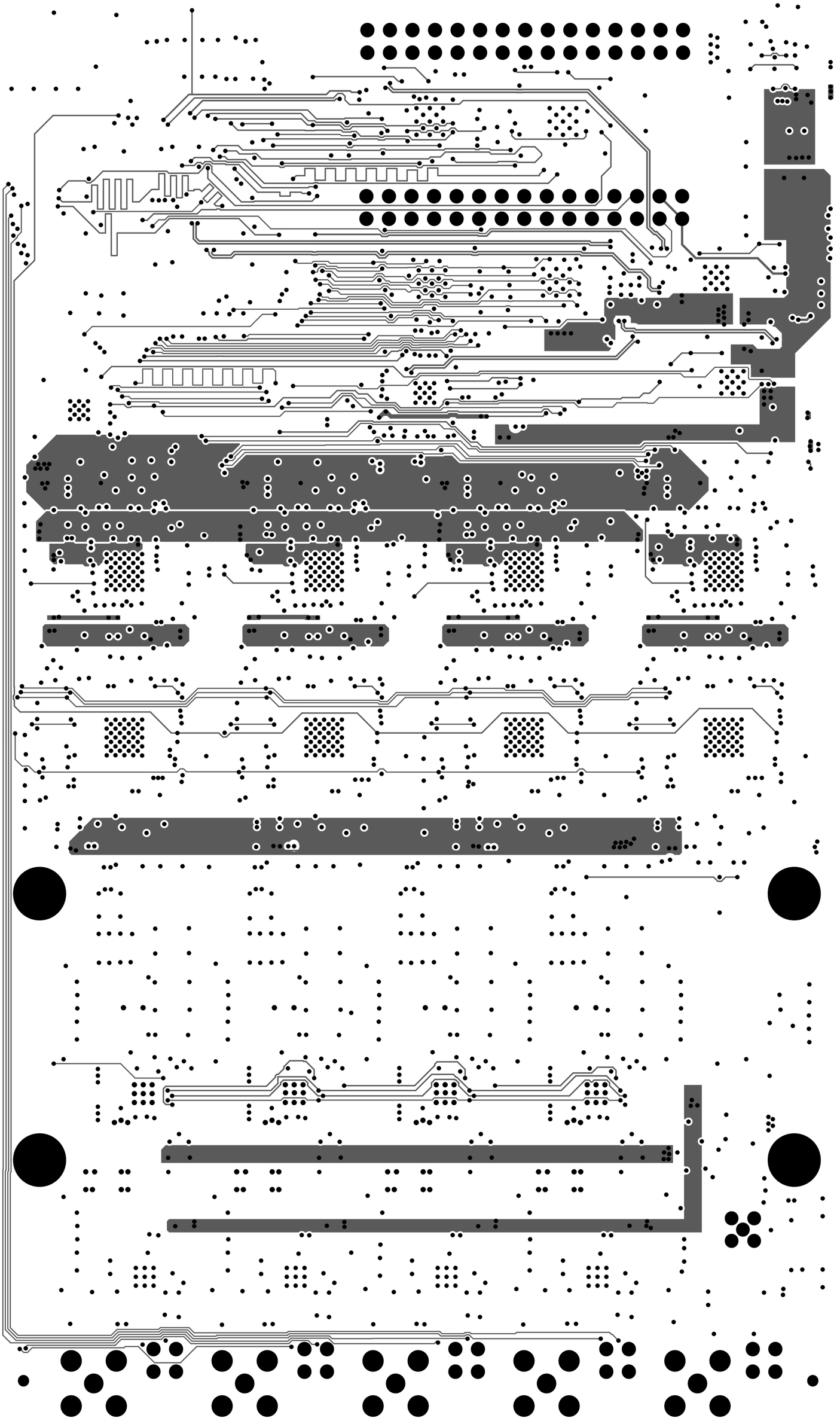
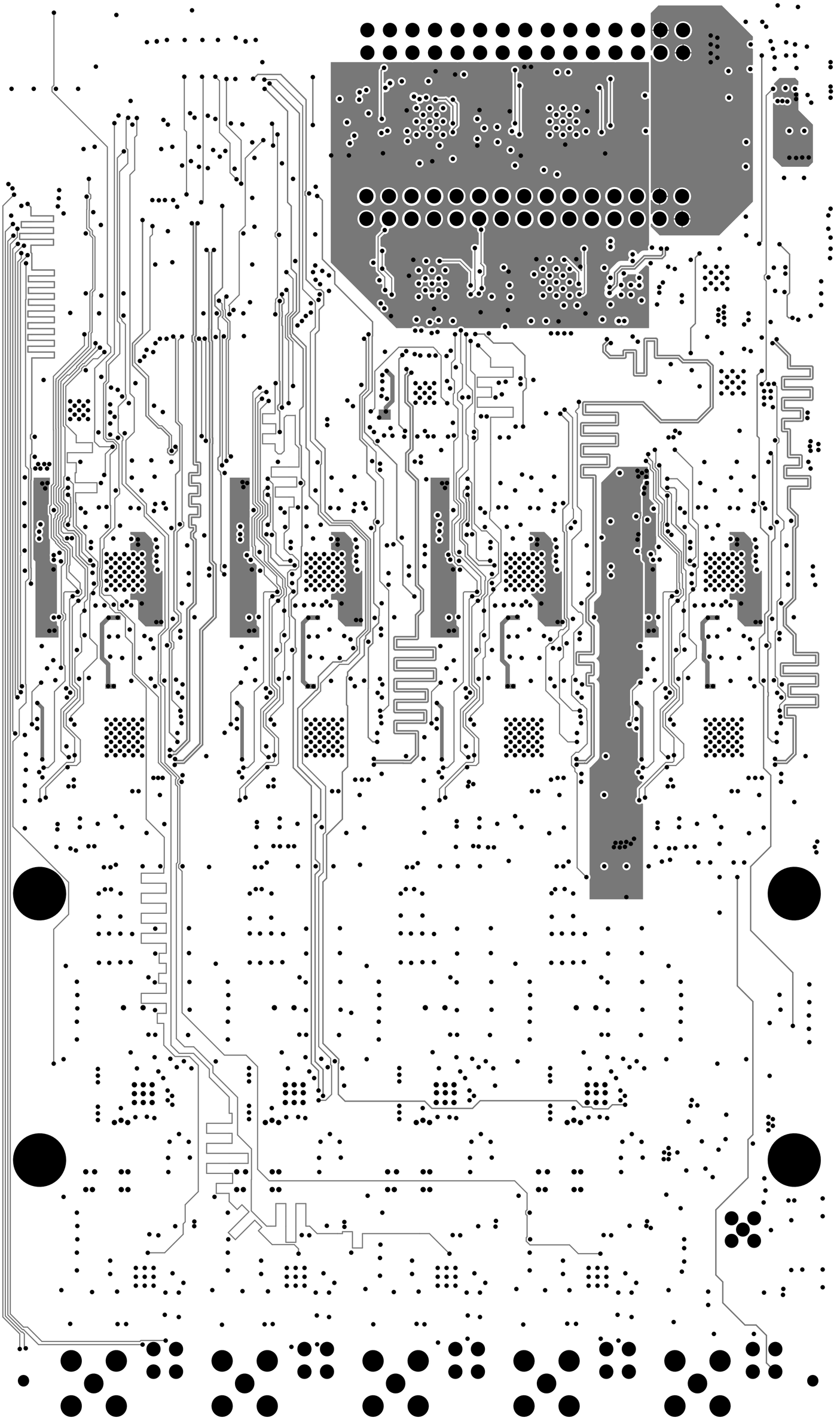
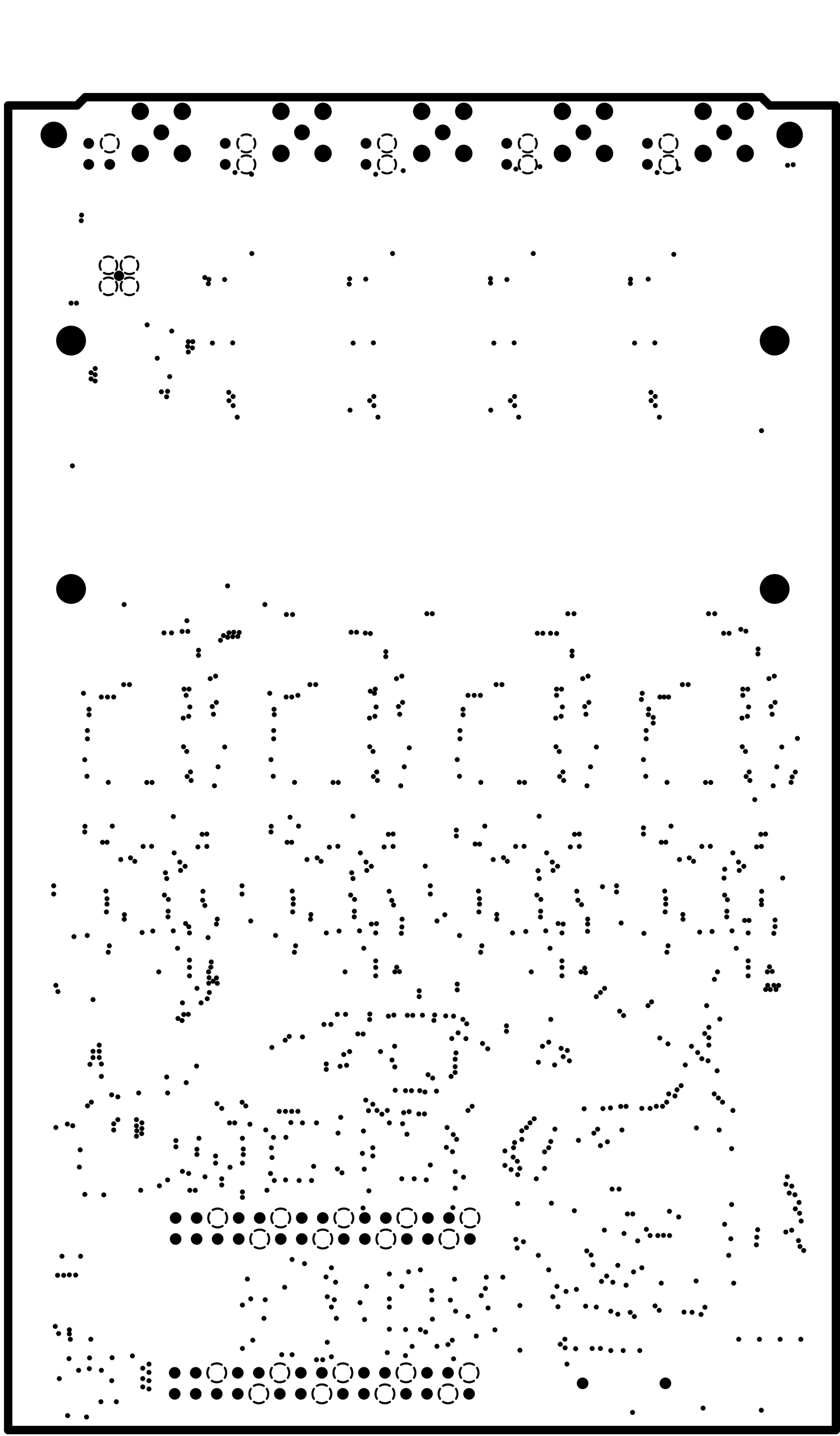
J3
LD5
RF OUT 1
J4
LD6
RF OUT 2
J5
LD8
RF OUT 3
J6
LD2
EXT CLK IN
J2
LD7
P7V0
INT CLK IN
J7
IC21
P5V0
IC20
OSC1
LD9
P5V0A
P3V6
LD1
IC5A
IC5B
IC5C
IC5D
IC23A
IC23B
IC23C
IC23D
IC17A
IC17B
IC17C
IC17D
IC3A
IC3B
IC3C
IC3D
IC2A
IC2B
IC2C
IC2D
IC13A
IC13B
IC13C
IC13D
P1V8A
TP0
TP1
TP2
TP3
TP4
P3V6
IC18
IC10
MODE
ON
1 2 3 4
J8
P3V3_MP
GND
JTAG
EEM 0
J1A
EEM 1
J1B
IC16
IC19
LD4
INT OSC
MMCX CLK
P3V3
IC9
P12V0
LD3
P3V3_MP
P2V0
P3V3A
IC7
IC11
IC15
30
30
TP3
TP2
TP4
TP1
IC22
3U DDS rev 1.0
WUT ISE 2017

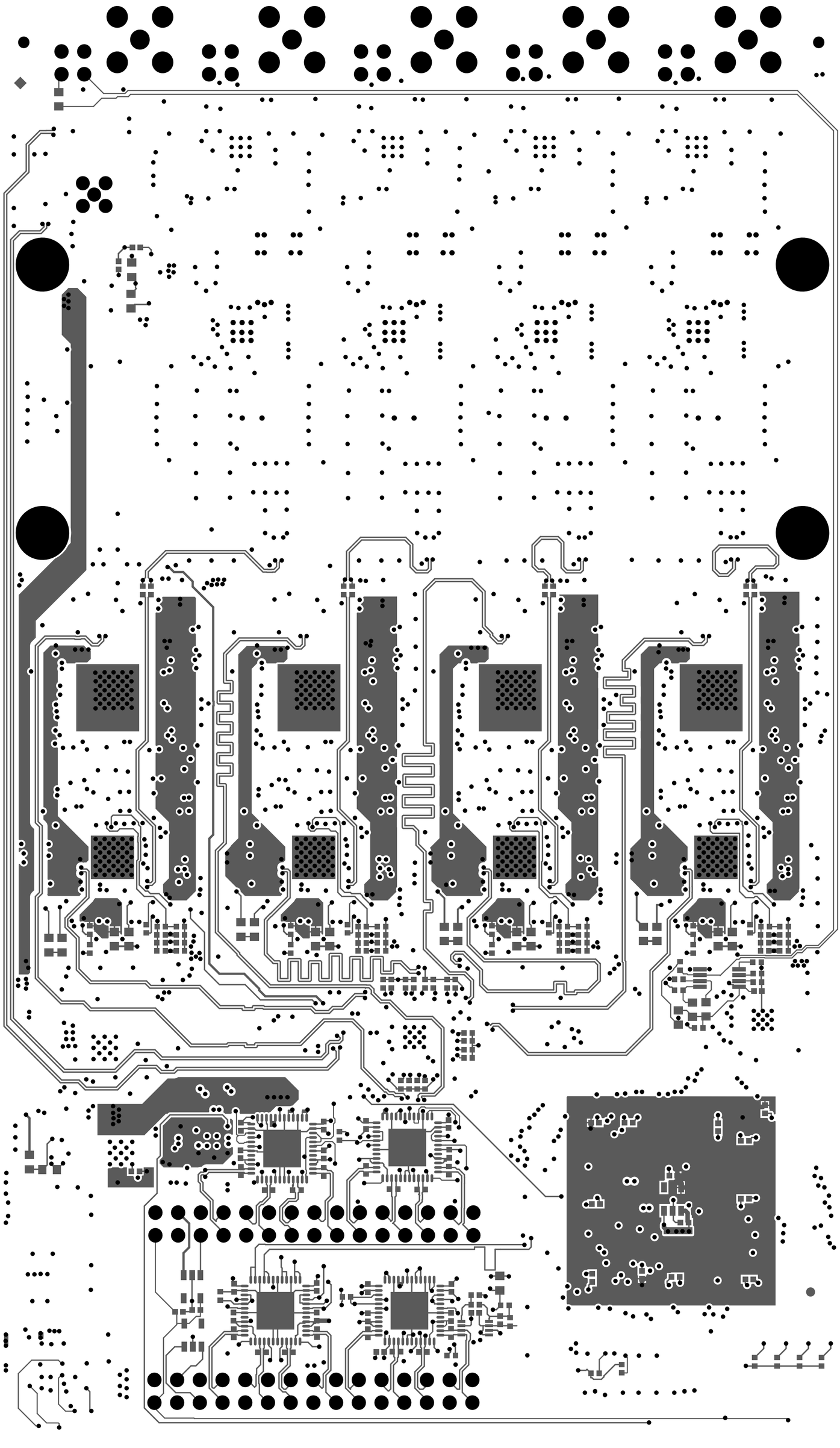












IC15

IC14

IC4

IC1A

IC1B

IC6A

IC6B

IC8A

IC8B