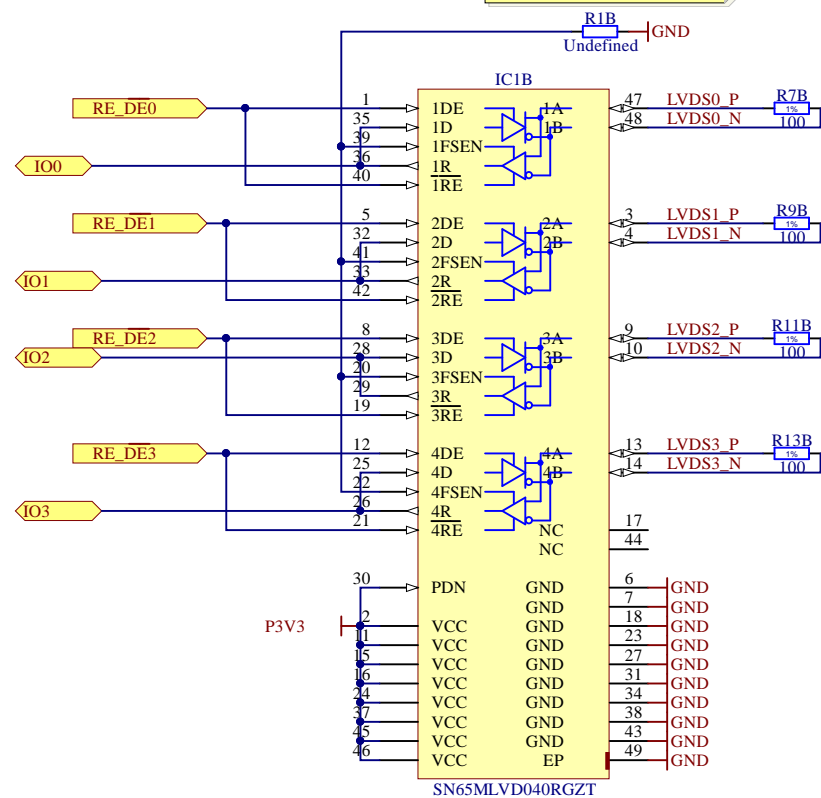
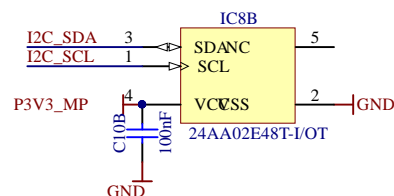
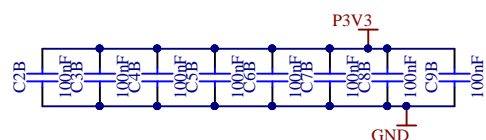
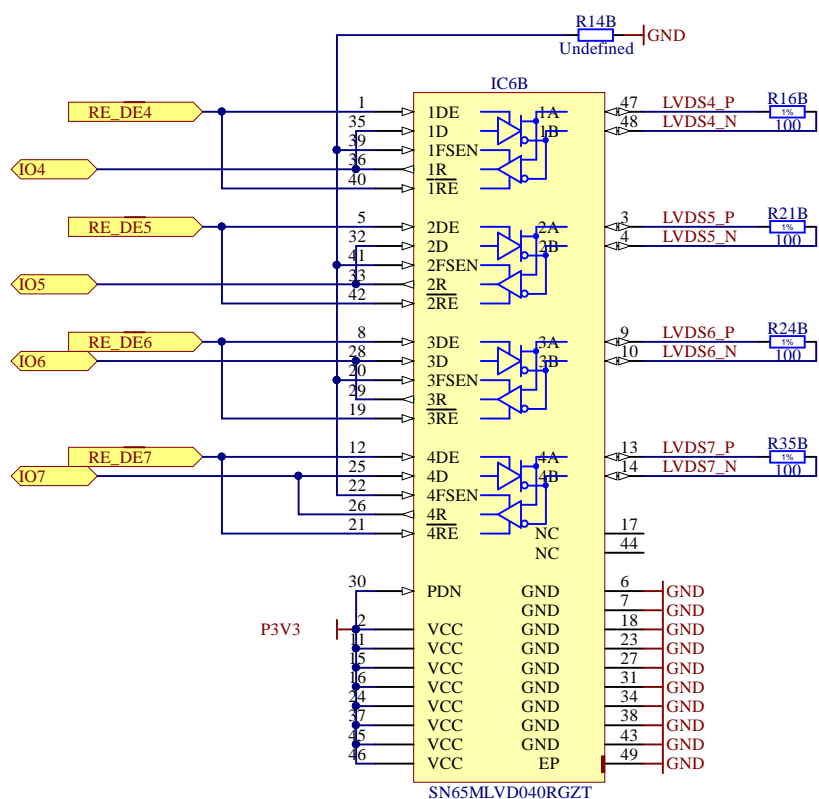
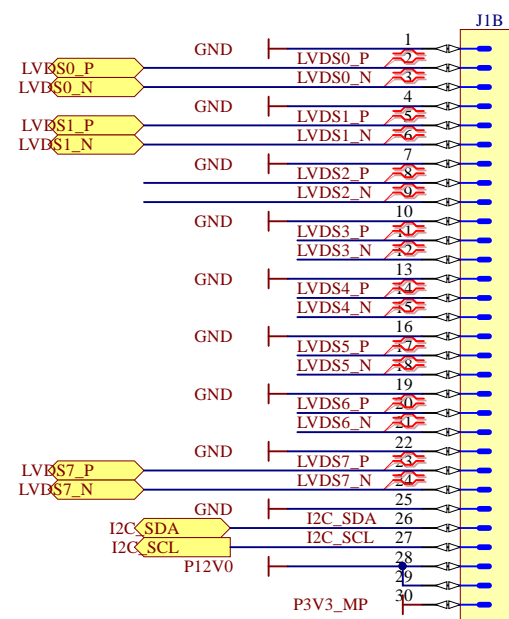


FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output



This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A



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Project/Equipment ARTIQ/SINARA

Document



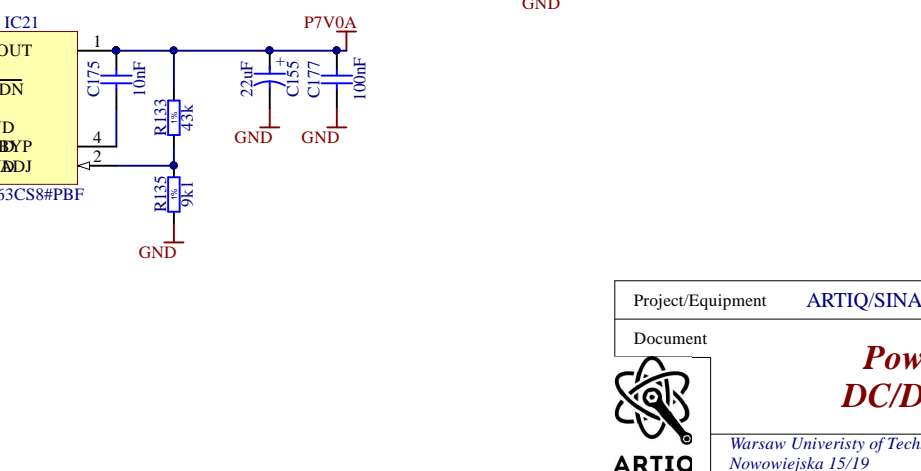
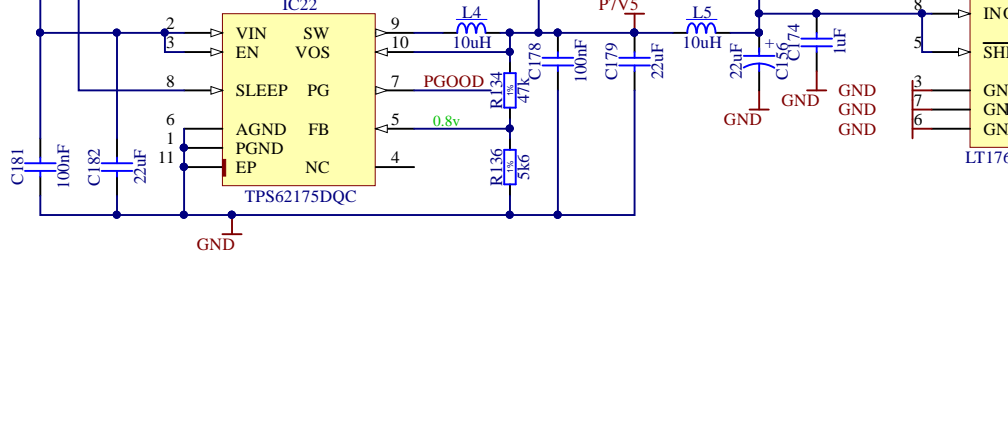
**LVDS to LVTTL
interface & EEM connector**

Warsaw University of Technology ISE
Nowowiejska 15/19

Designer	G.K.	
Drawn by	G.K.	XX/XX/XXXX
Check by	-	17.09.2017
Last Mod.	-	
File	LVDS_IFC_DDS.SchDoc	
Print Date	17.09.2017 23:10:14	Sheet 2 of 7

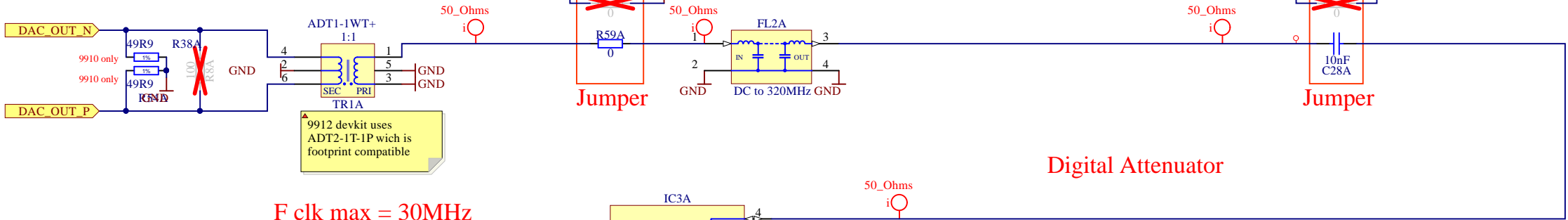
ARTIQ

Size A3 Rev -



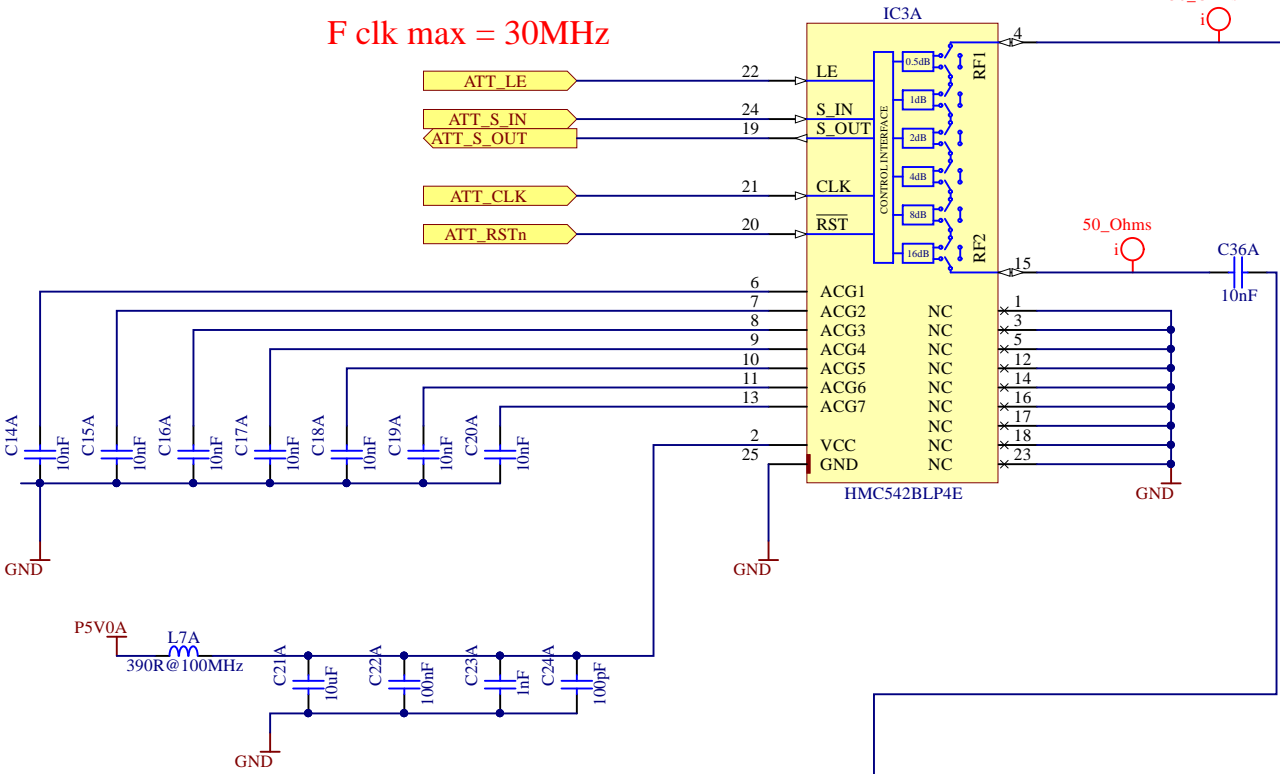
<p>er supply C & LDOs</p>		<p>Designer <u>G.K.</u></p> <p>Drawn by <u>G.K.</u></p> <p>Check by <u>-</u></p> <p>Last Mod. <u>-</u></p> <p>File <u>Supply_DDS.SchDoc</u></p> <p>Print Date <u>17.09.2017 23:10:14</u></p>	<p>Sheet <u>3</u> of <u>7</u></p>
<p>ology ISE</p>	<p>ARTIQ</p>	<p>Size A3</p>	<p>Re</p>

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28) for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom Filter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder



F clk max = 30MHz

Digital Attenuator

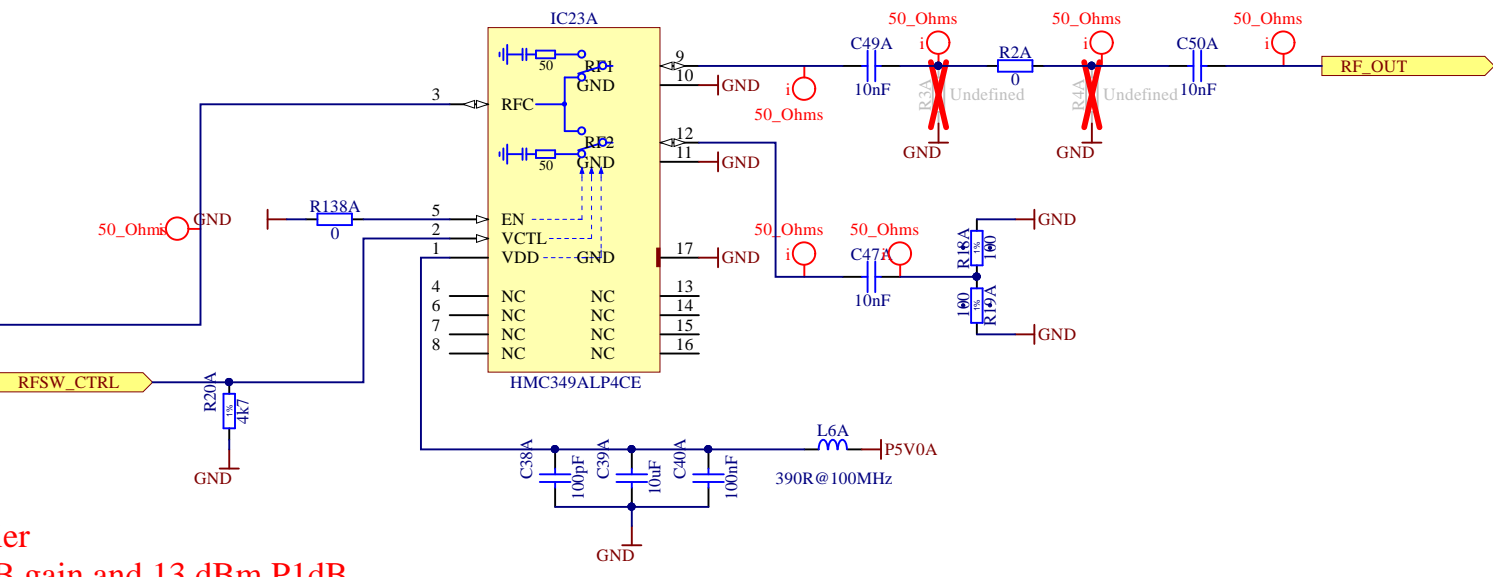


With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

$R5 \text{ power} = 65\text{mA}^2 \cdot 39 = 0.16\text{W}$

Amplifier
~23 dB gain and 13 dBm P1dB

SPDT switch



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Project/Equipment		ARTIQ/SINARA	
Document		Designer G.K.	
		Drawn by G.K.	
		Check by -	
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		Rev -	

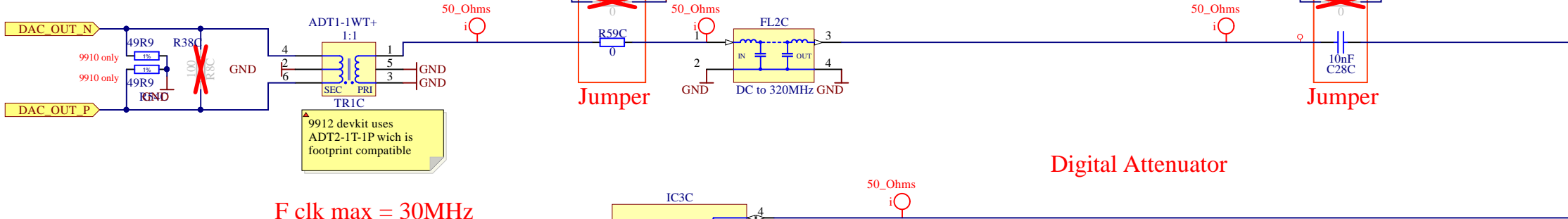
Output stage :
Attenuator, amplifier and filter



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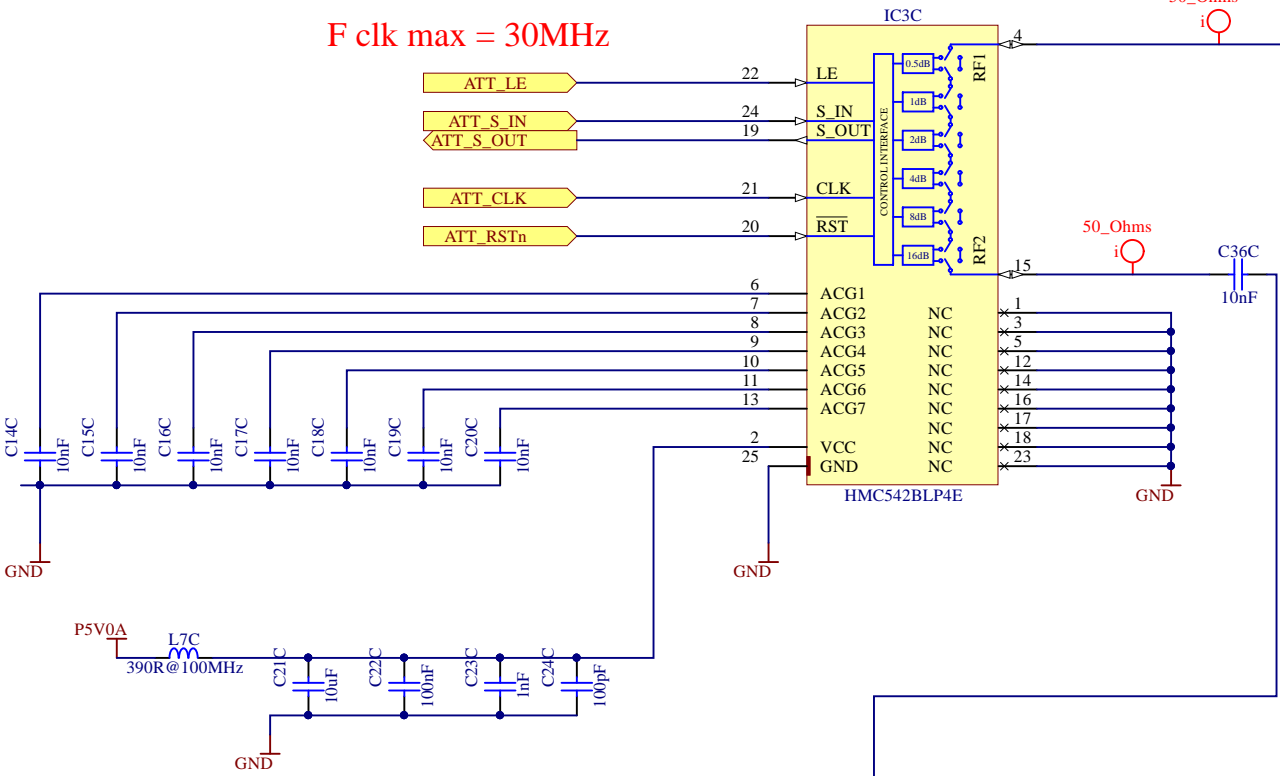
ARTIQ

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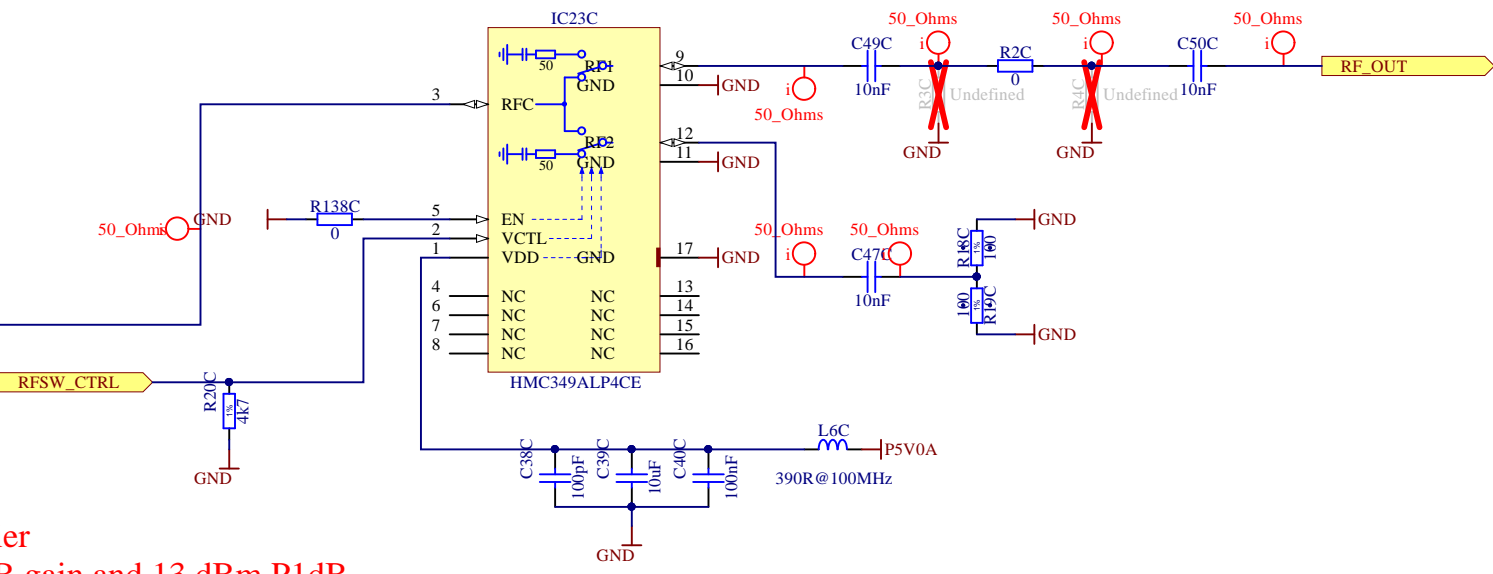
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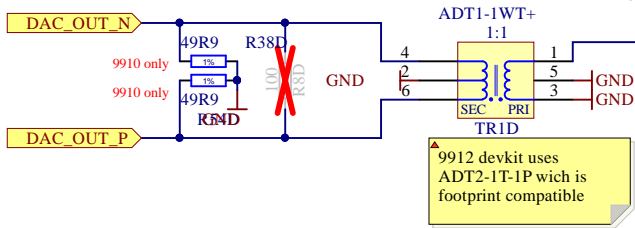
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Document		Drawn by	G.K.
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		Sheet	4 of 7
		Size	A3
		Rev	-

Output stage :
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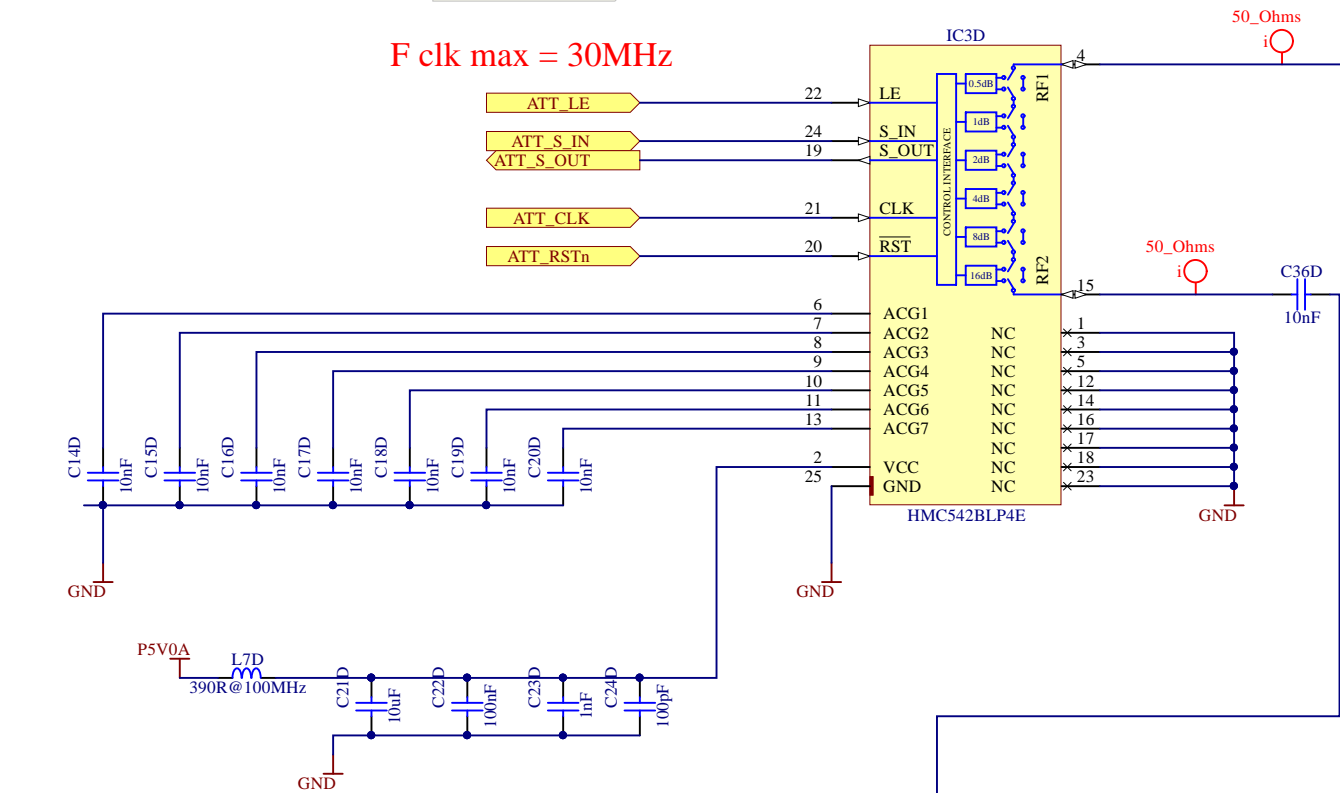
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ARTIQ

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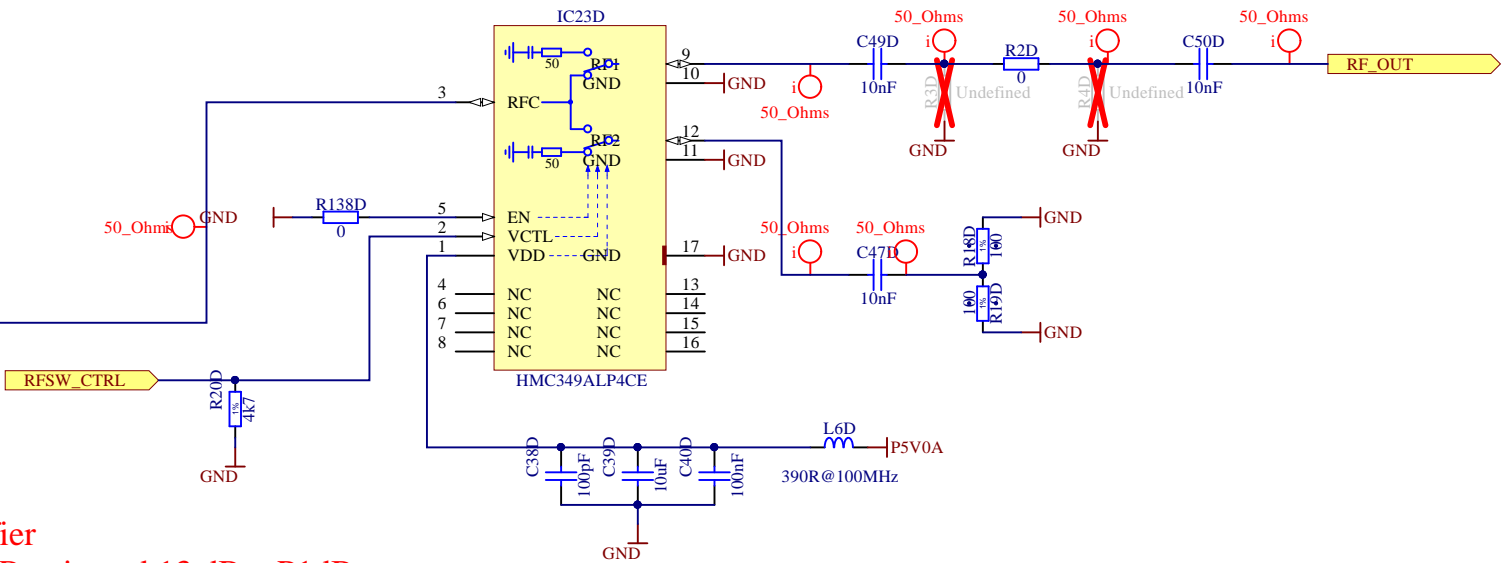


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Project/Equipment		ARTIQ/SINARA	
Document		Output stage : Attenuator, amplifier and filter	
Designer		G.K.	
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Check by		-	
Last Mod.		-	17.09.2017
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Rev		-	

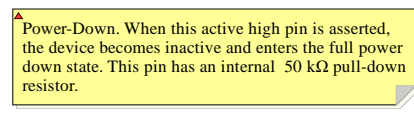


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

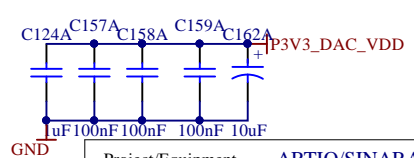
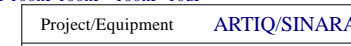
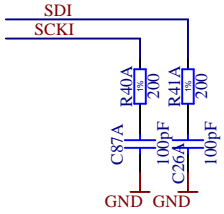
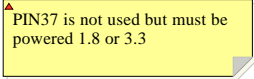


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1	0	1	0		Direct	51.83411
1	0	1	1		Direct	61.43188
1	1	0	0		Direct	77.75879
1	1	0	1		Direct	92.14783
1	1	1	0		Direct	122.87903
1	1	1	1		Direct	155.51758

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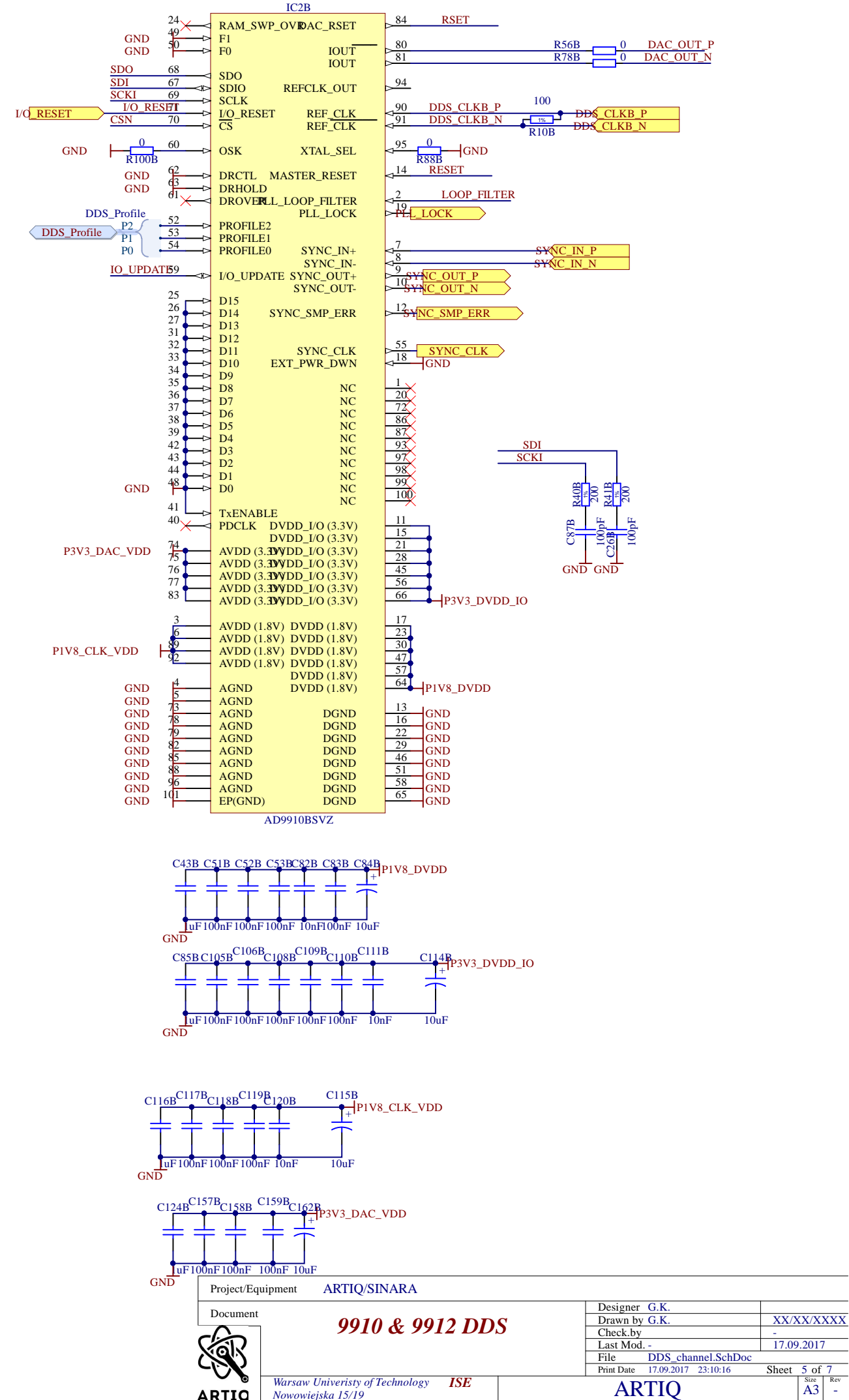
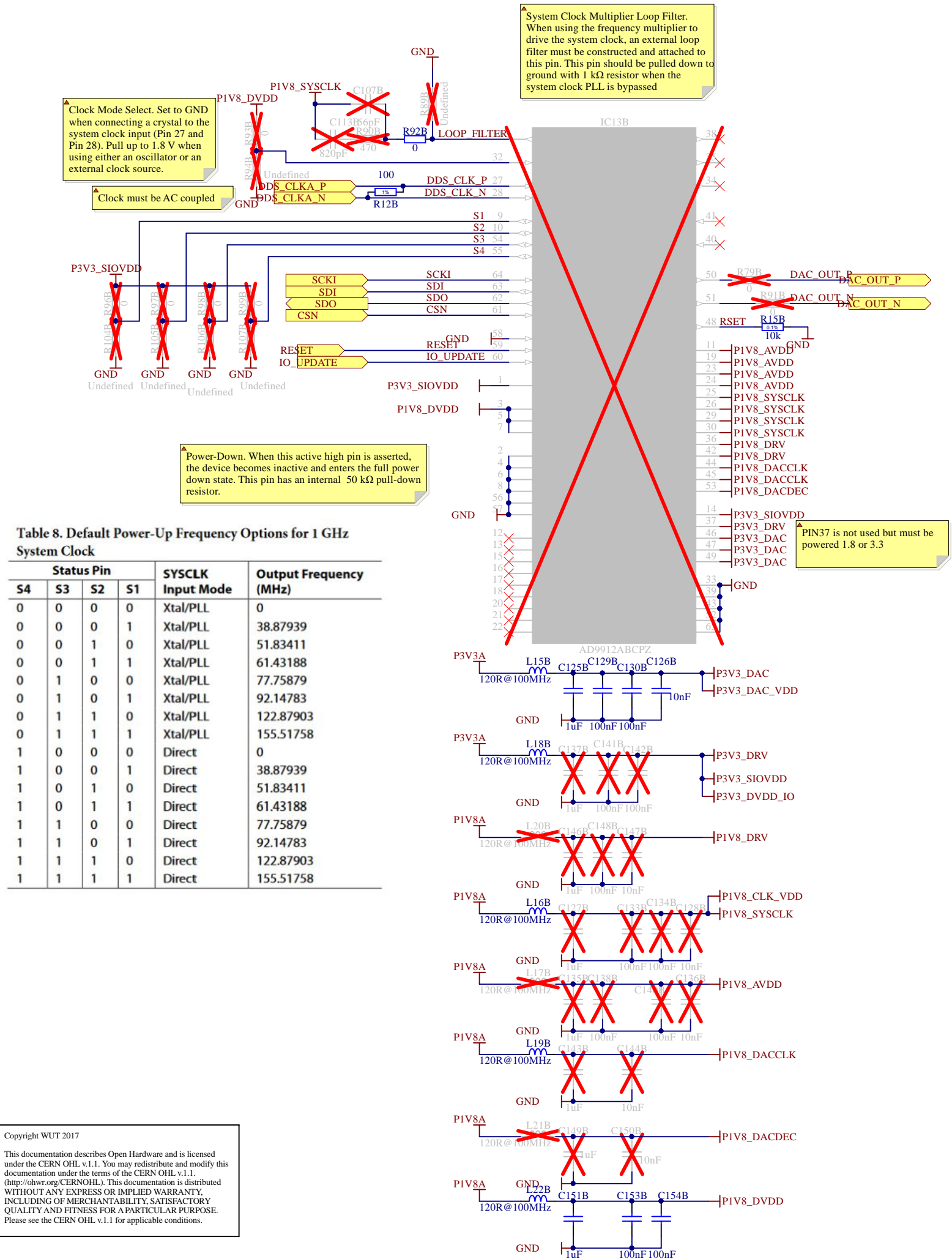


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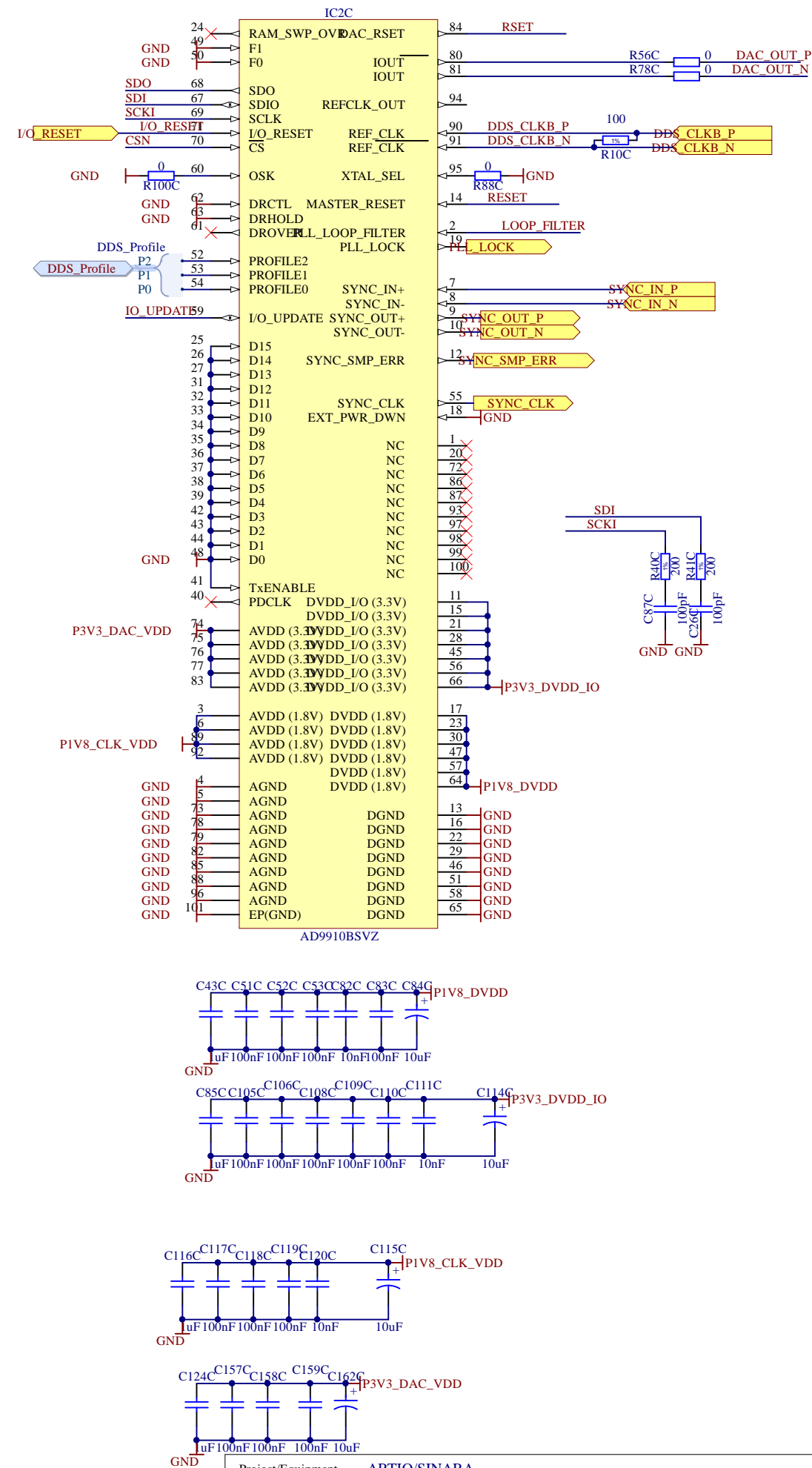
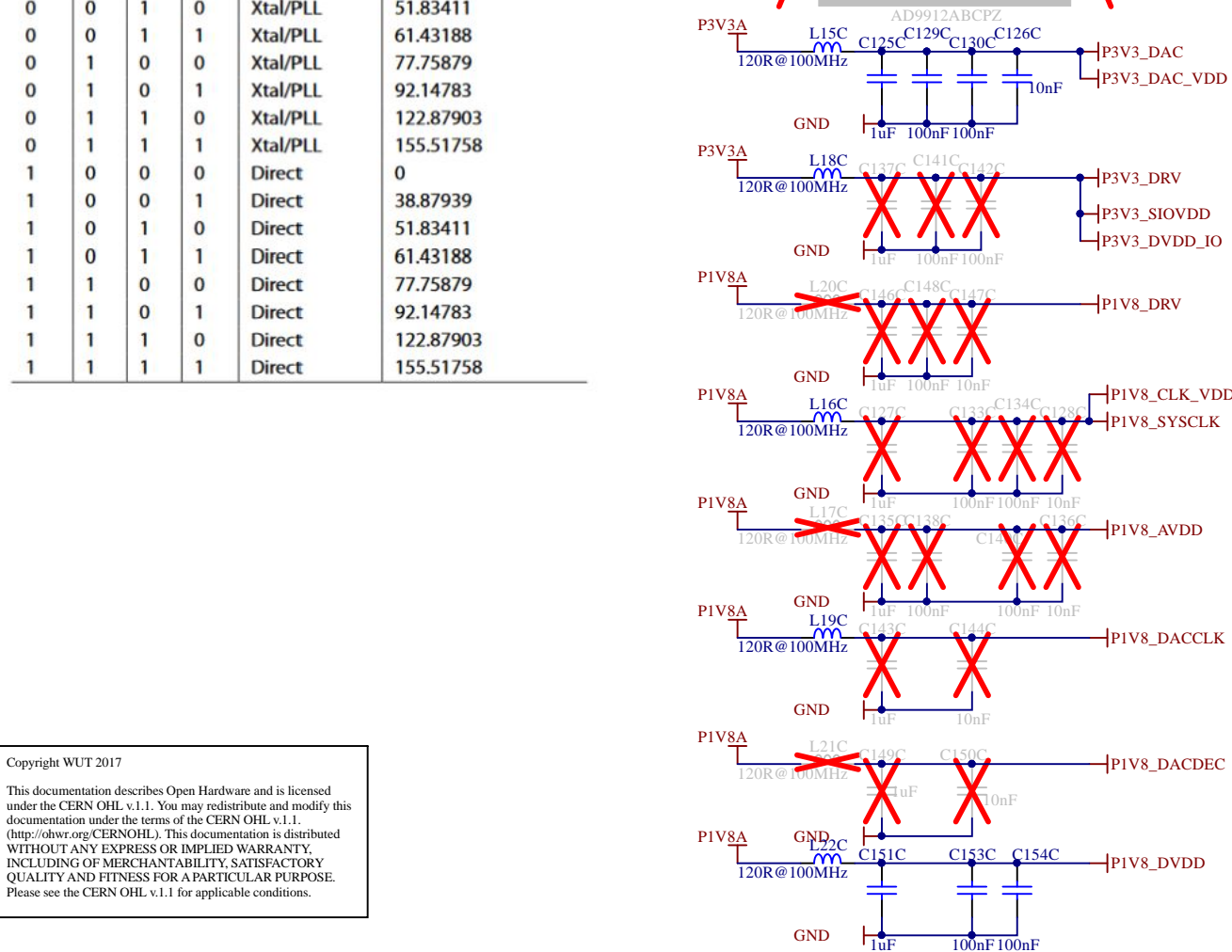
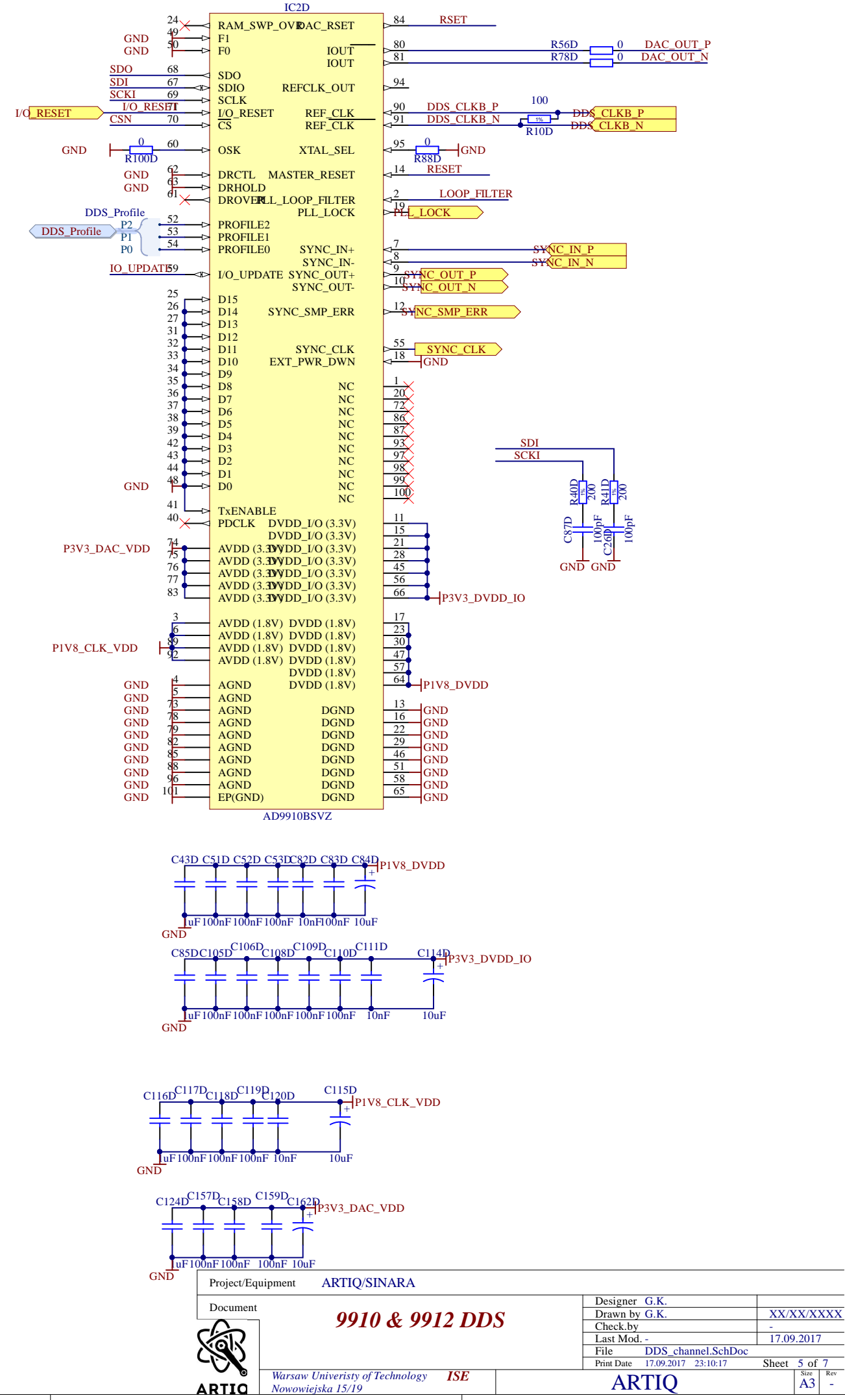
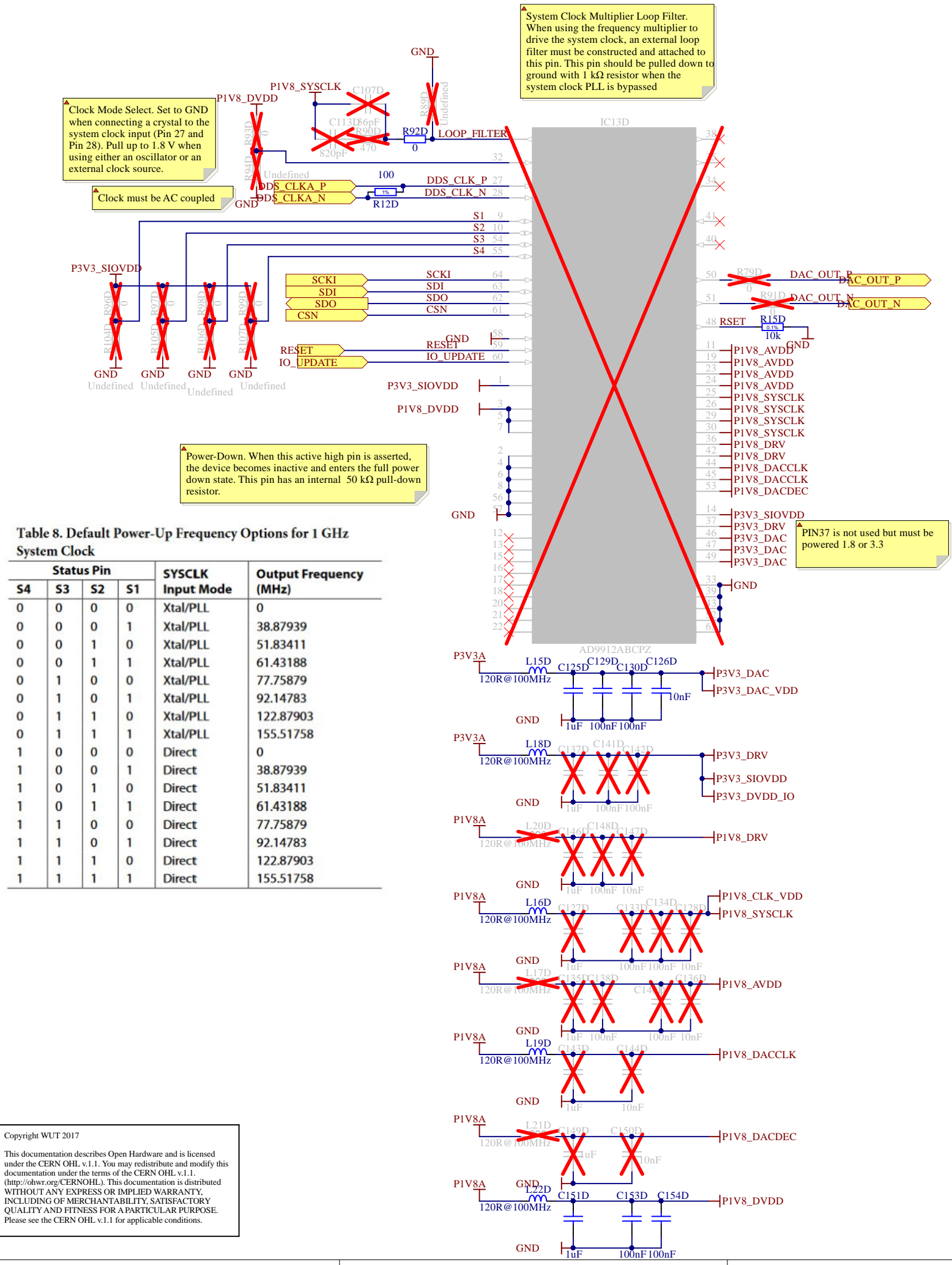


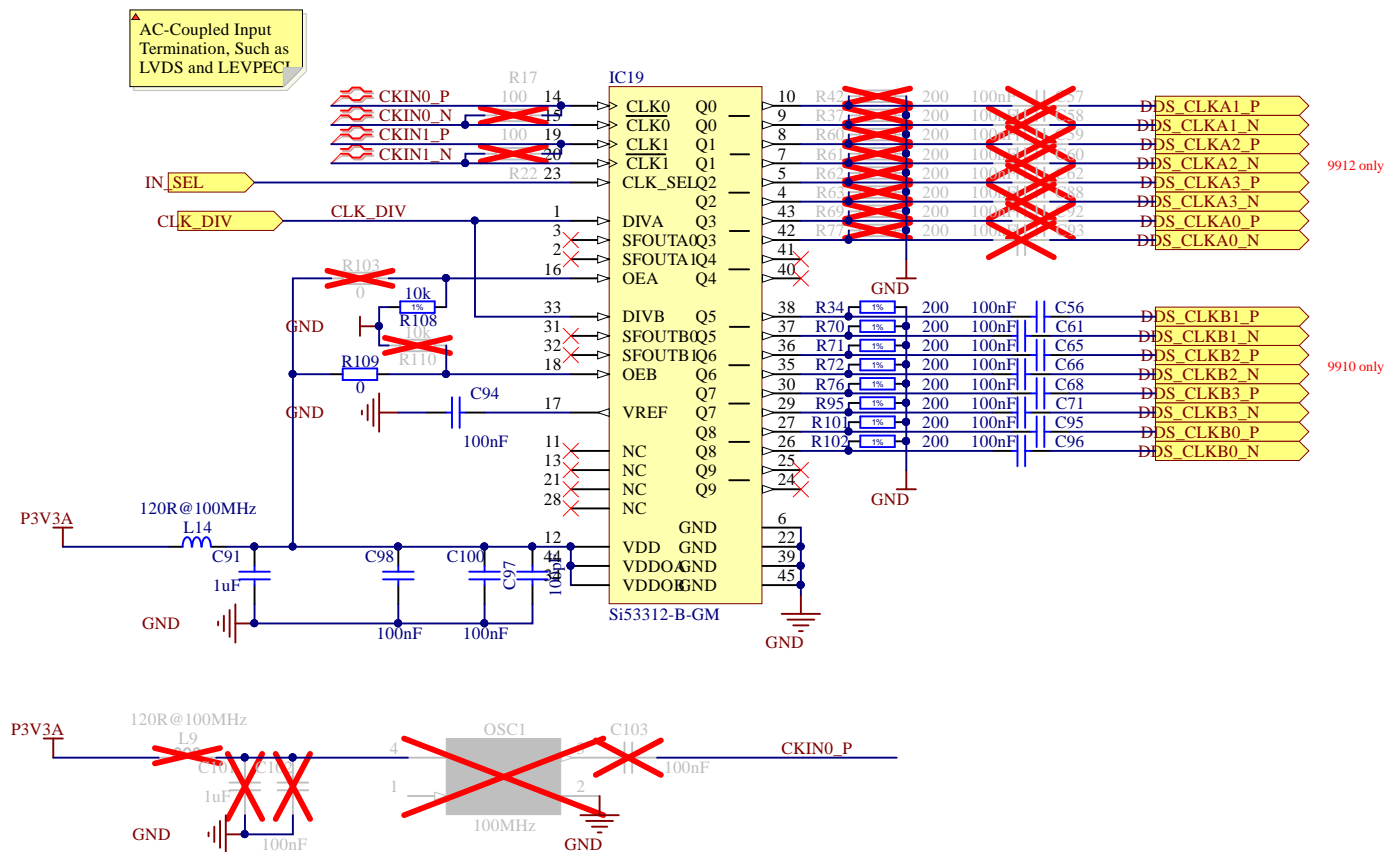
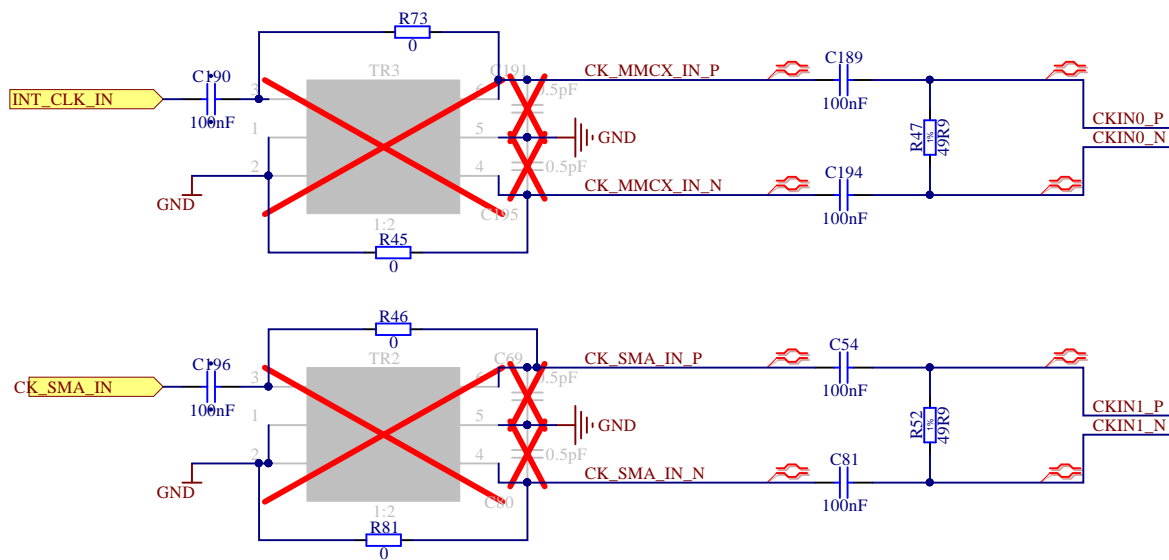
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1	1	0	0		Direct	77.75879
1	1	0	1		Direct	92.14783
1	1	1	0		Direct	122.87903
1	1	1	1		Direct	155.51758

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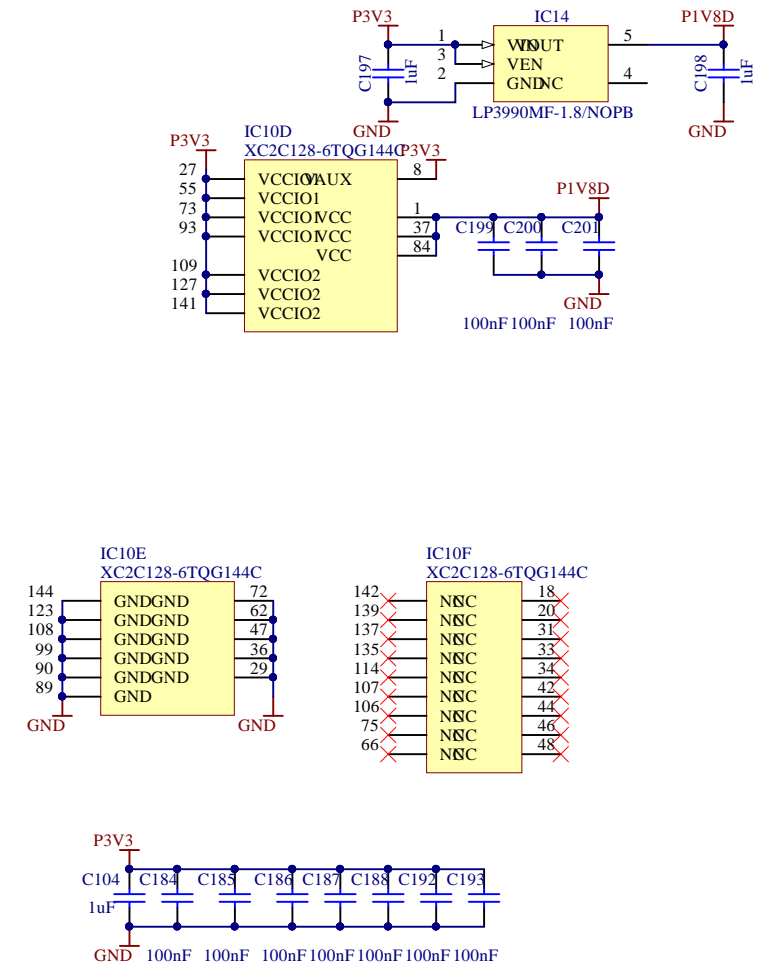
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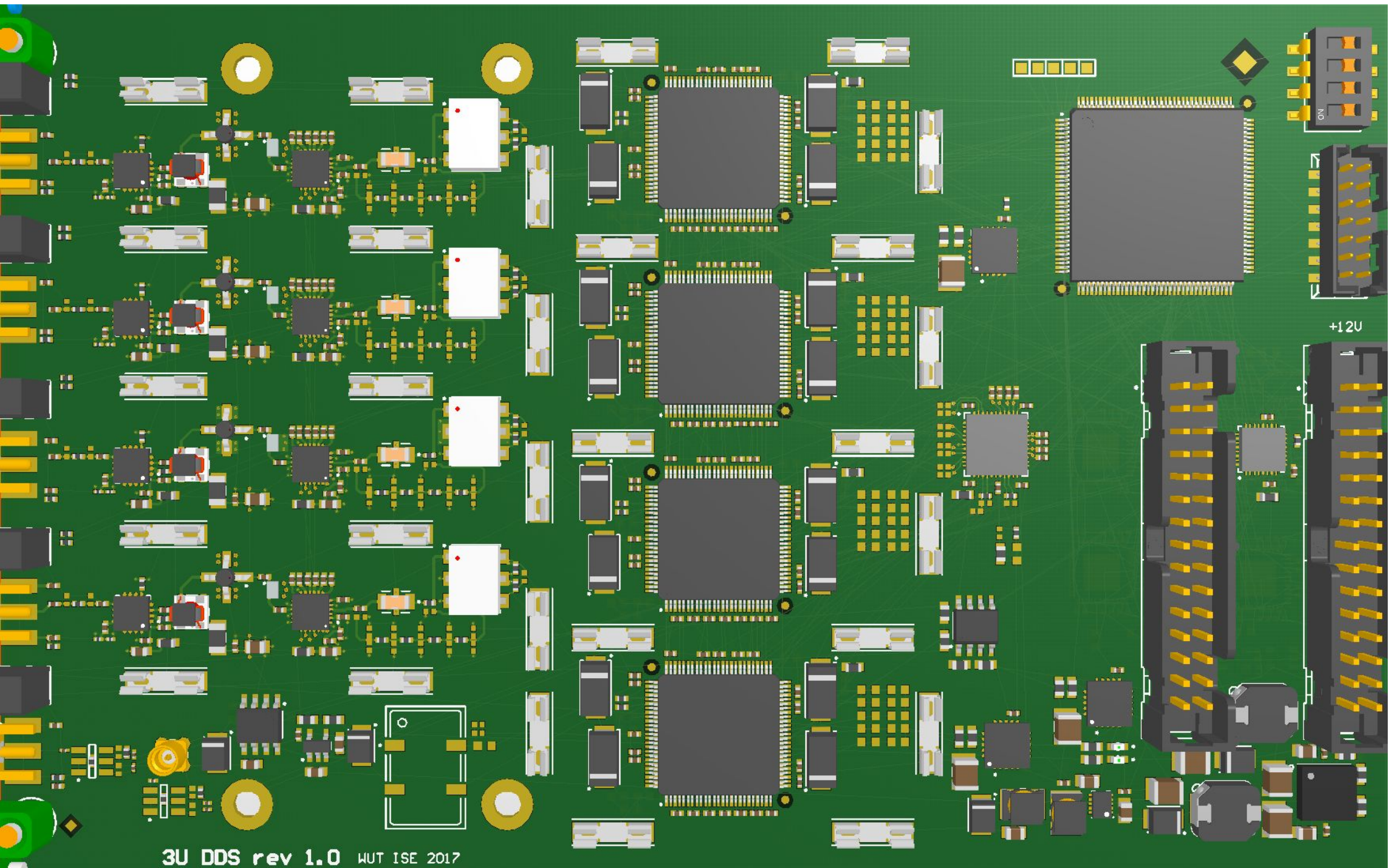




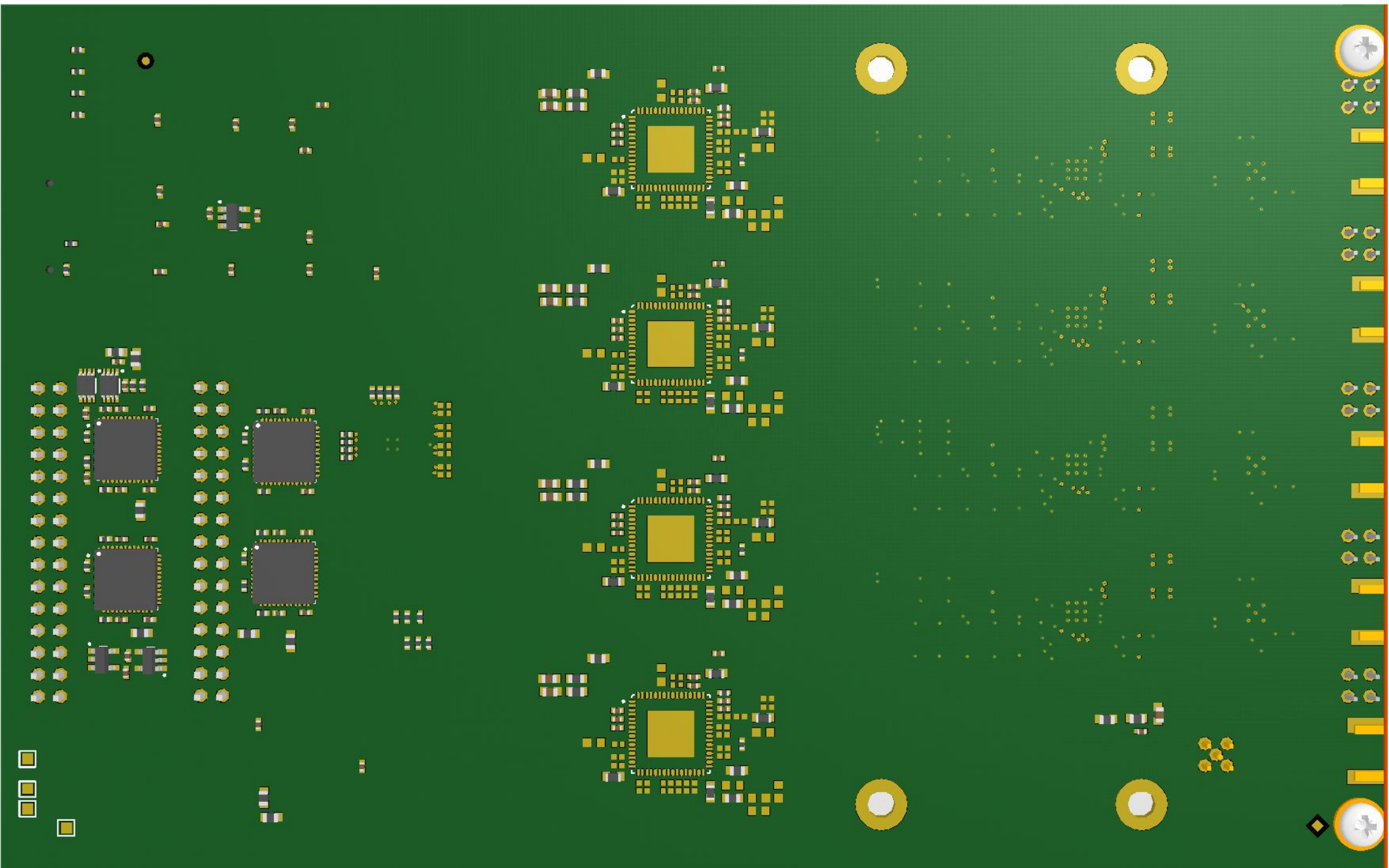
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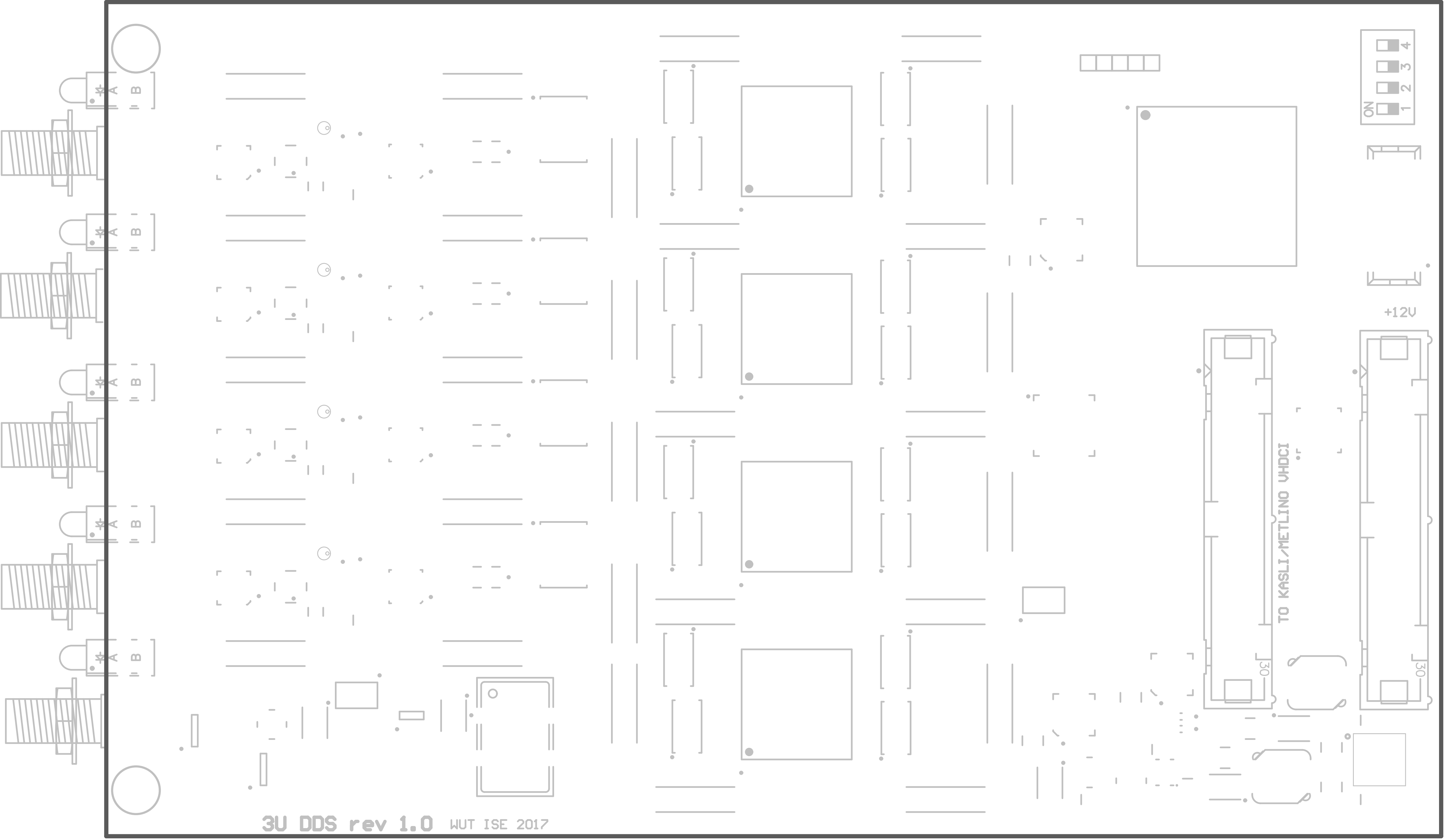
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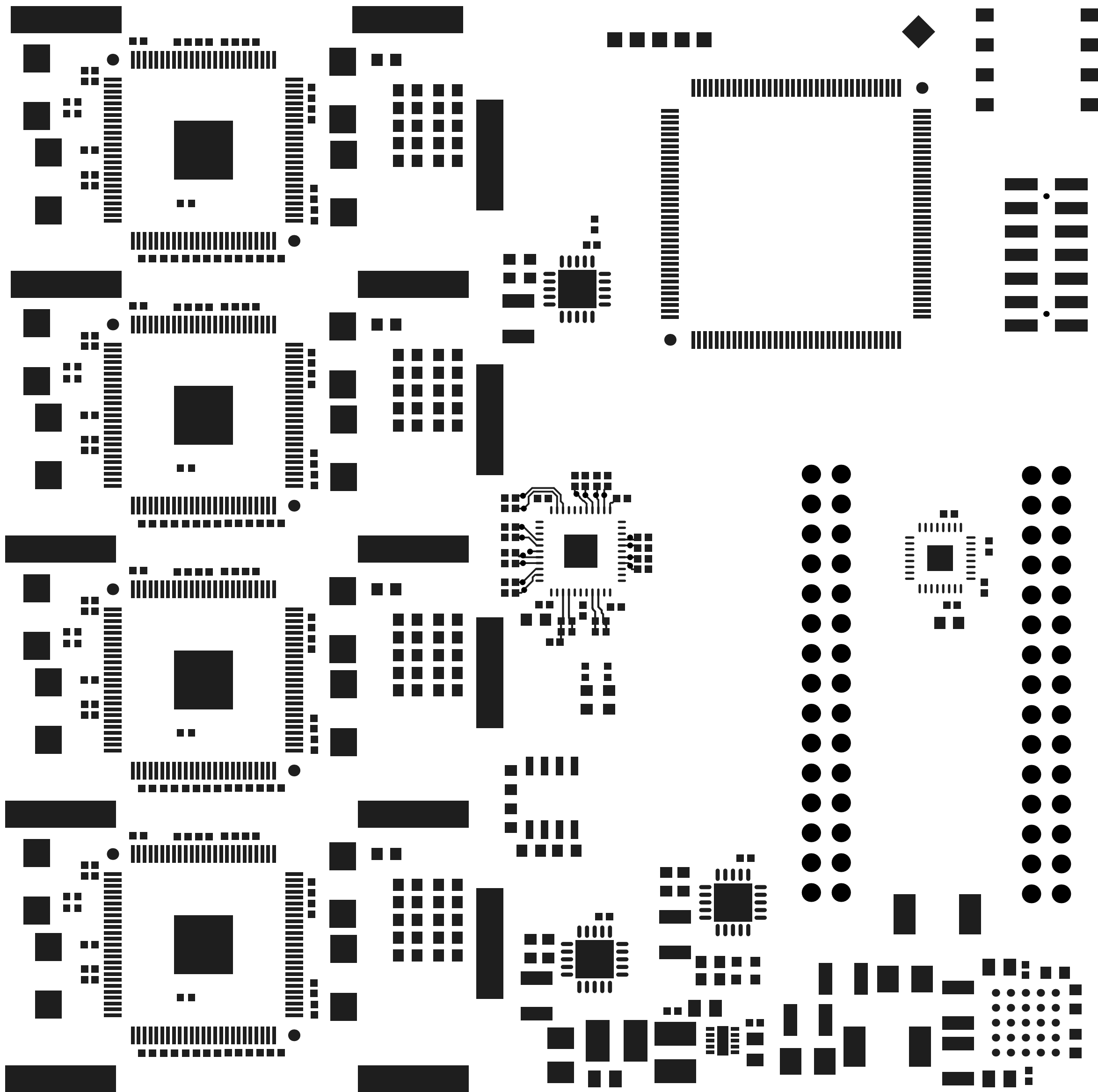
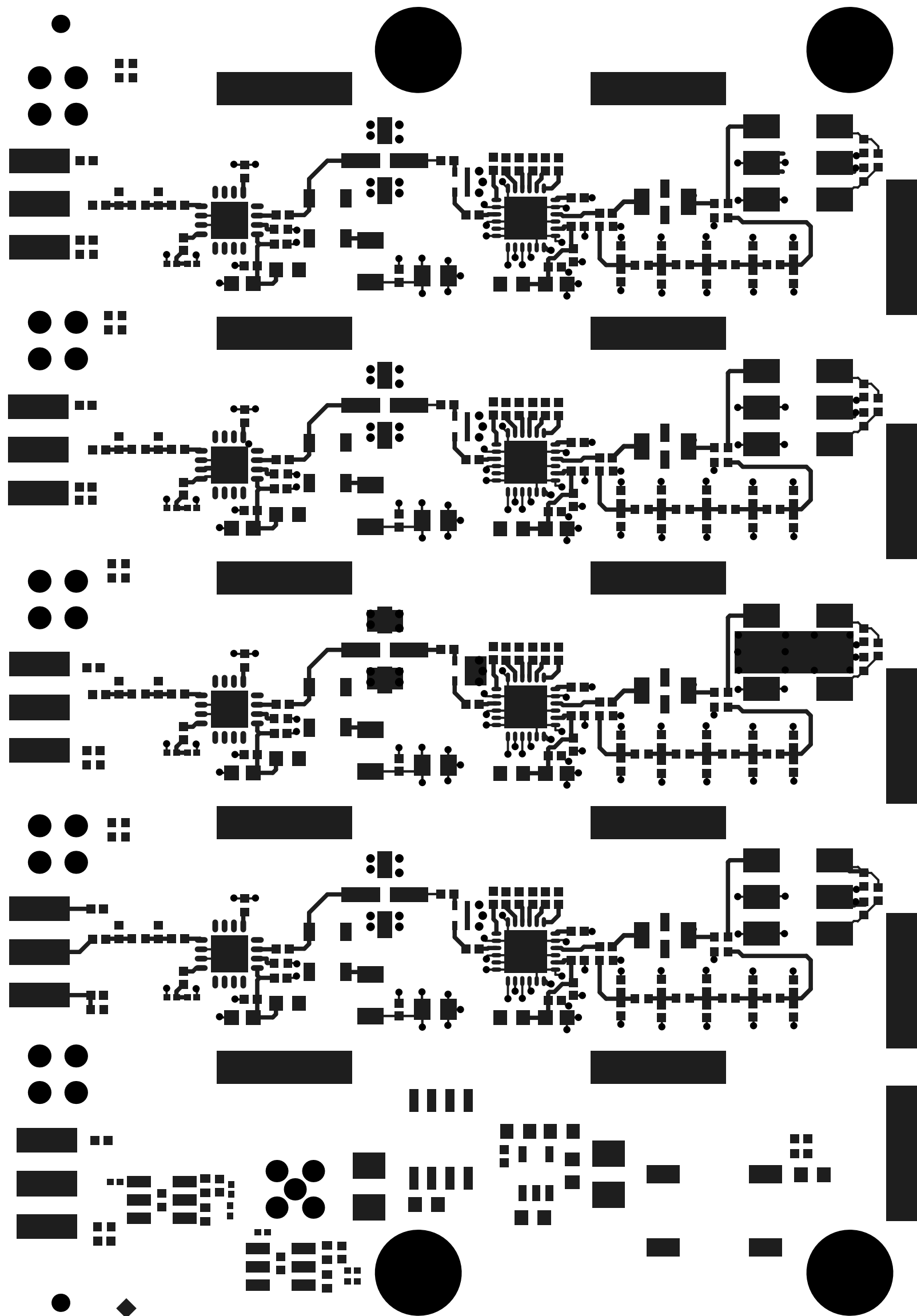


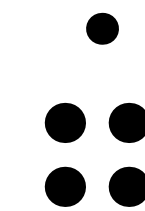


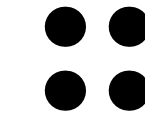
3U DDS rev 1.0 WUT ISE 2017

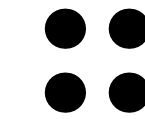


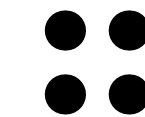


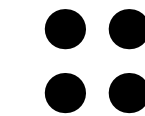




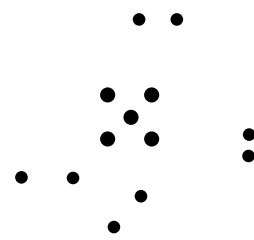
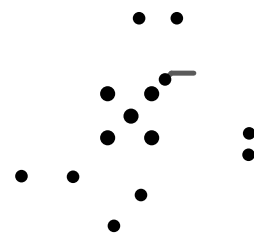
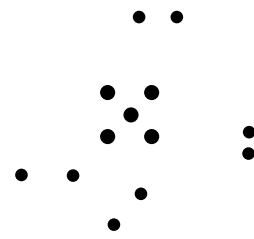
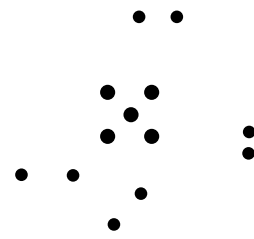
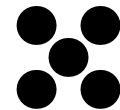
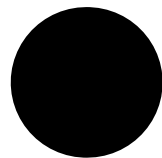
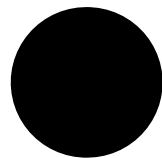
























































































































































































































































































































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