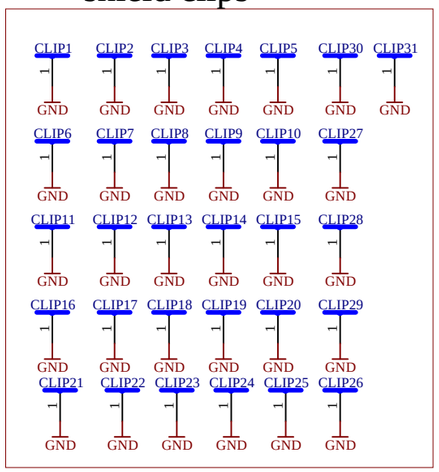
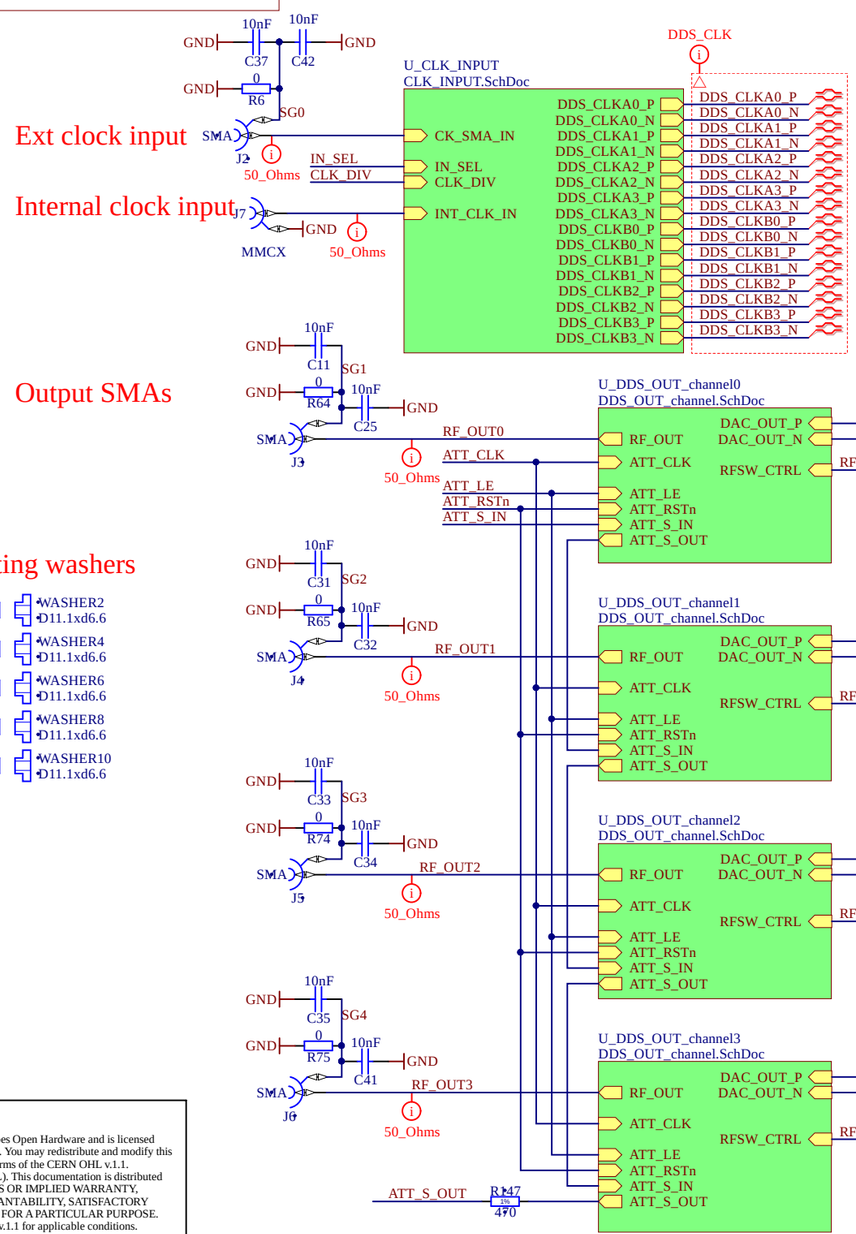
shield clips

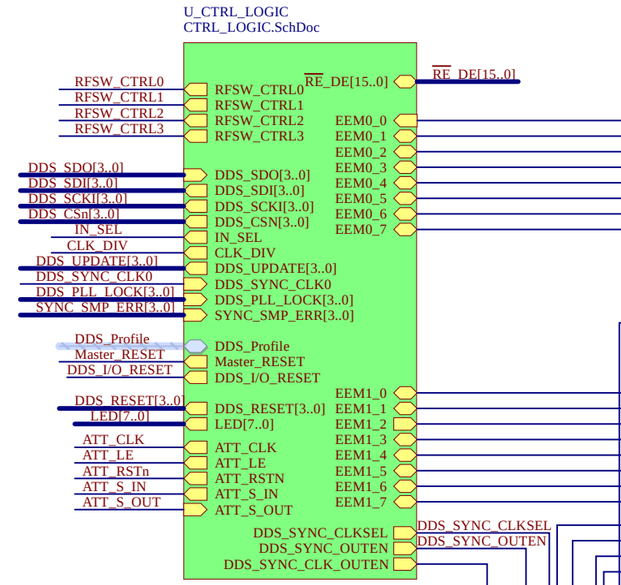


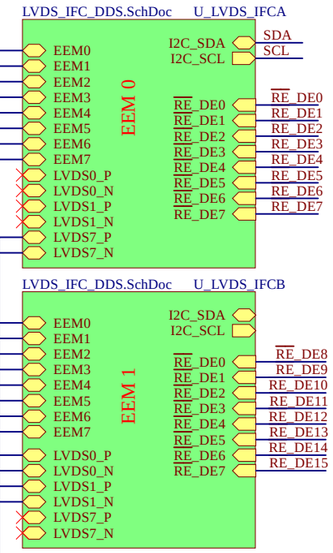
Output SMAs

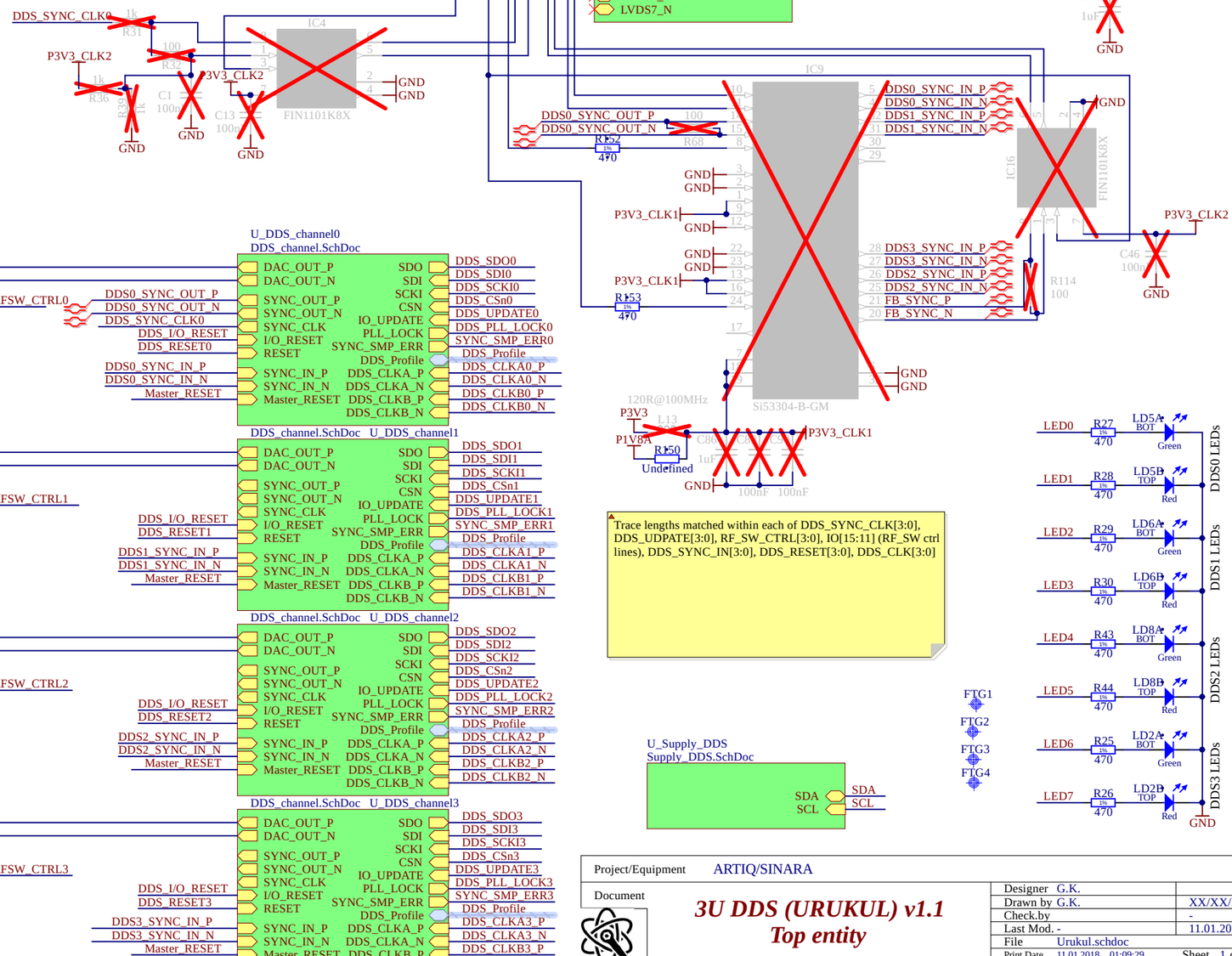
SMA Insulating washers

WASHER1 D11.1xd6.6 — WASHER2 D11.1xd6.6
WASHER3 D11.1xd6.6 — WASHER4 D11.1xd6.6
WASHER5 D11.1xd6.6 — WASHER6 D11.1xd6.6
WASHER7 D11.1xd6.6 — WASHER8 D11.1xd6.6
WASHER9 D11.1xd6.6 — WASHER10 D11.1xd6.6





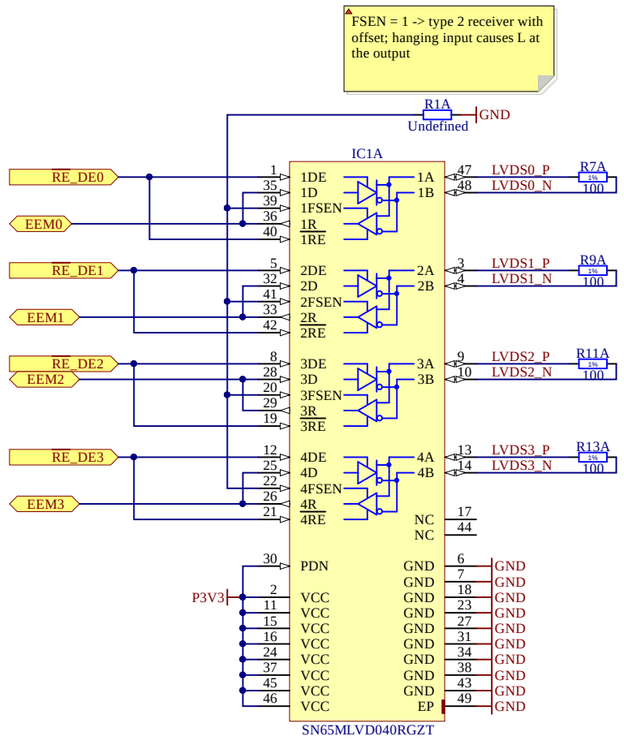




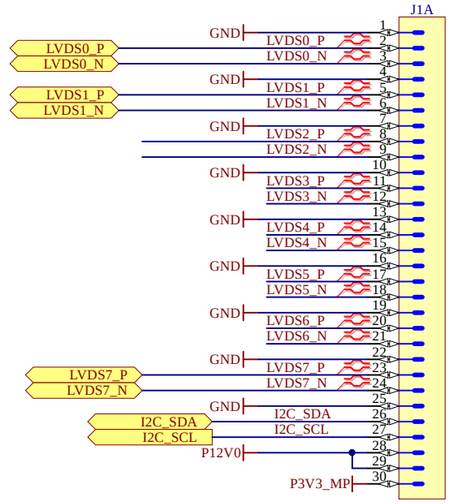
Project/Equipment	ARTIQ/SINARA
Document	3U DDS (URUKUL) v1.1 — Top entity
Designer	G.K.
Drawn by	G.K. — XX/XX/XXXX
Check.by	-
Last Mod.	- — 11.01.2018
File	Urukul.schdoc
Print Date	11.01.2018 01:09:29 — Sheet 1 of 7
Size	A3 — Rev -

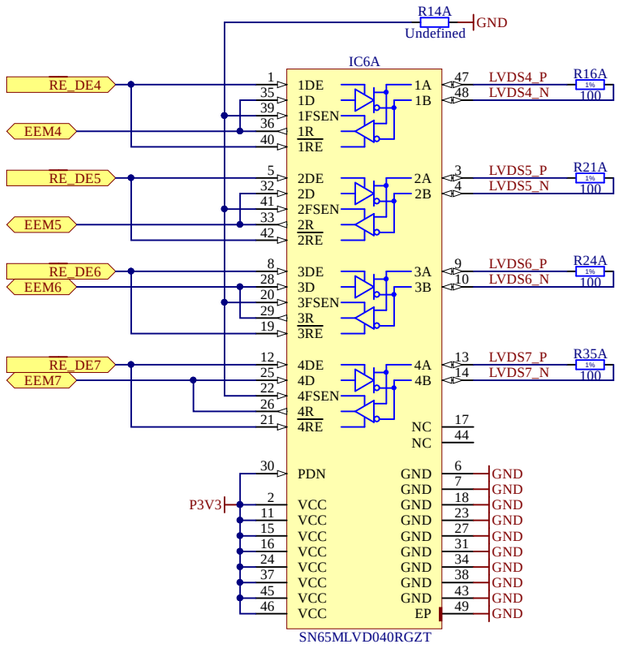
Warsaw Univeristy of Technology ISE
Nowowiejska 15/19

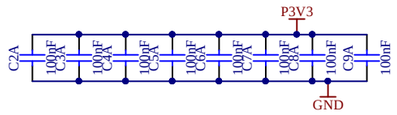
ARTIQ

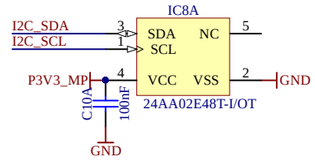


EEM Connector
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A



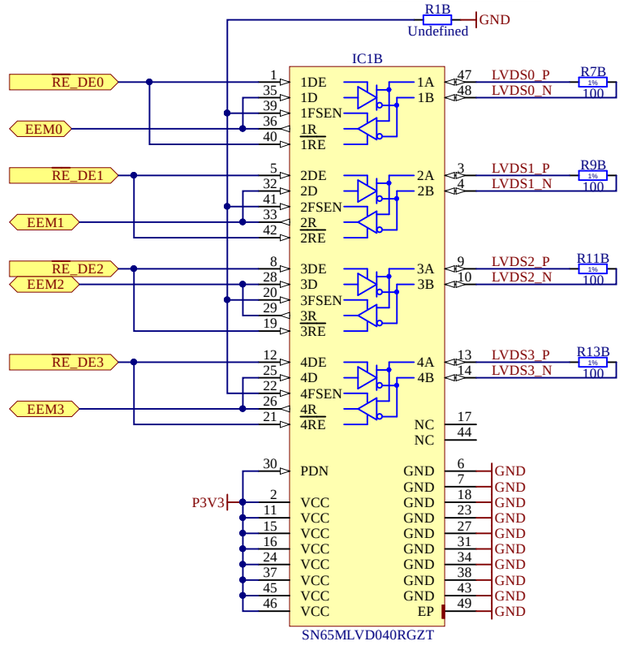




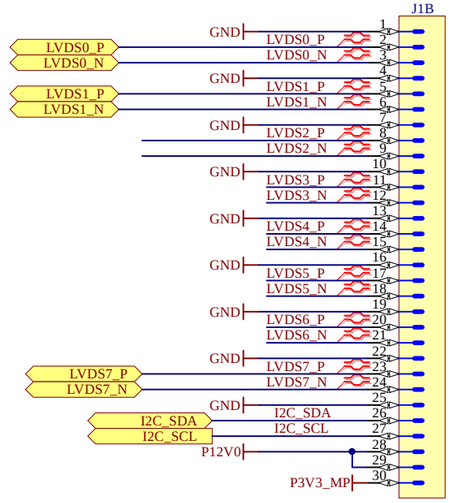


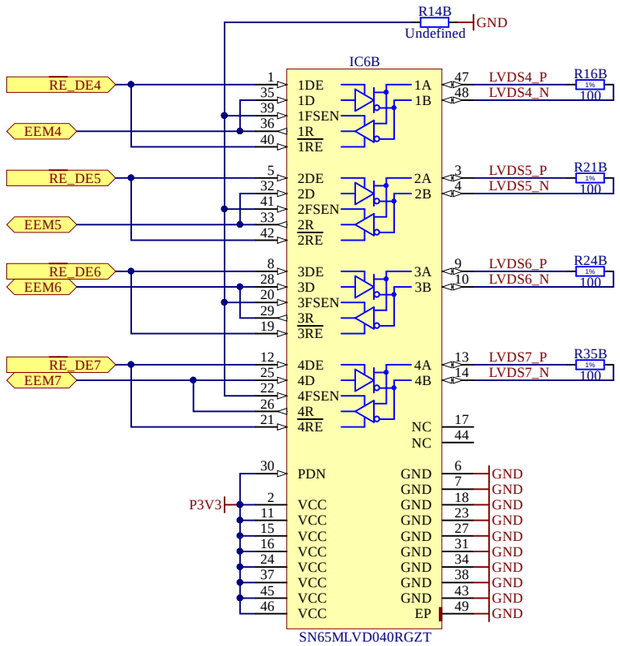
Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	11.01.2018
		File LVDS_IFC_DDS.SchDoc	
		Print Date 11.01.2018 01:09:30	Sheet 2 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	*ISE*	ARTIQ	Size A3 / Rev -

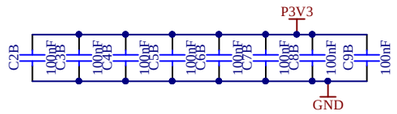
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

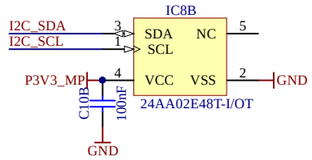


EEM Connector
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A

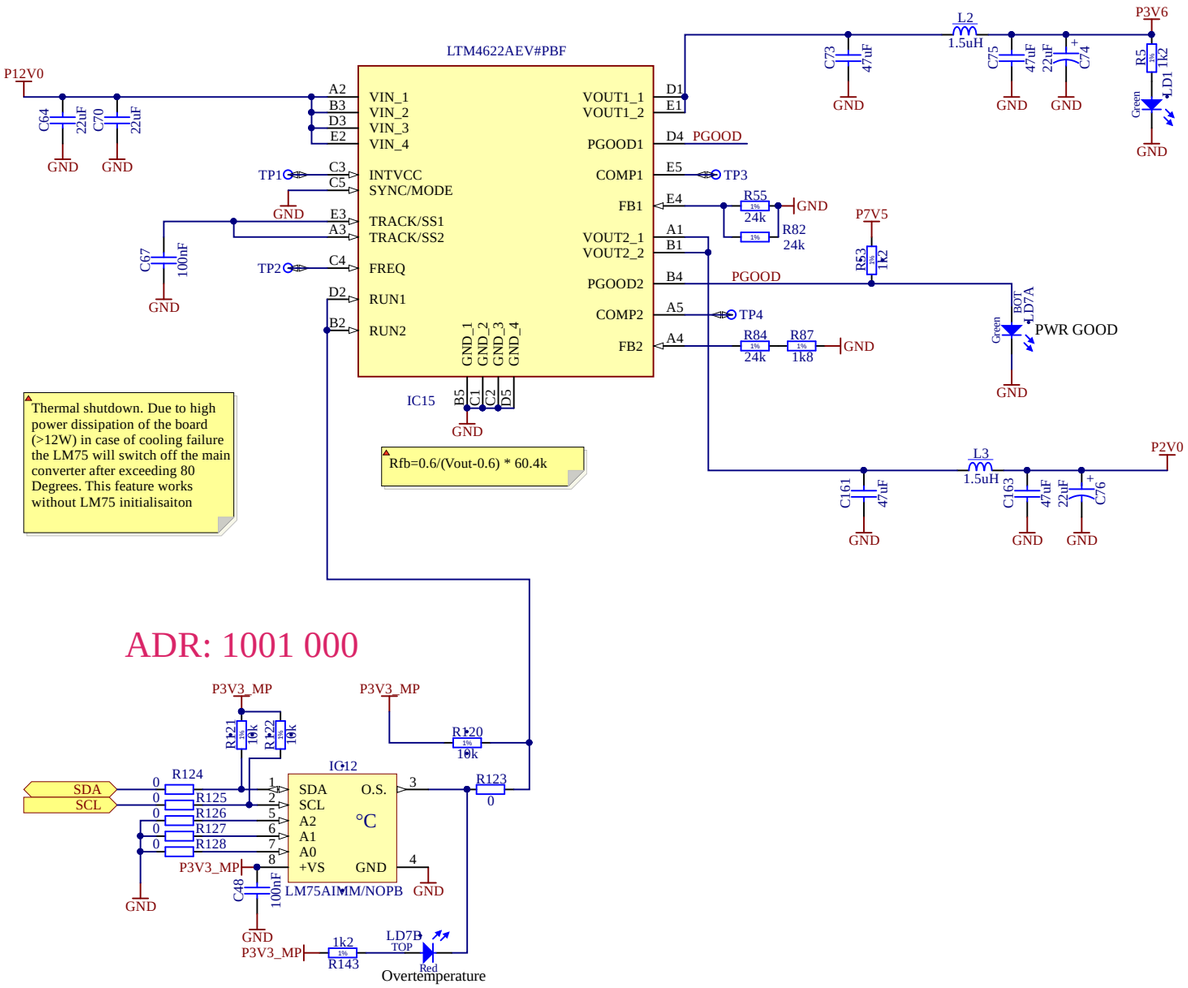


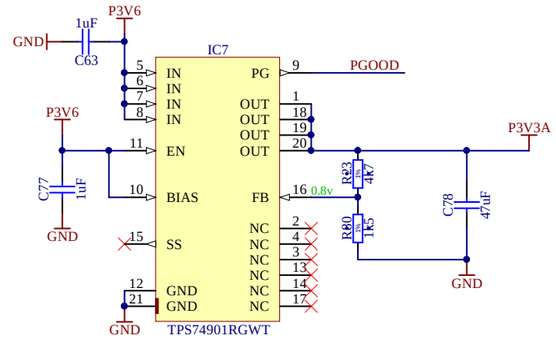


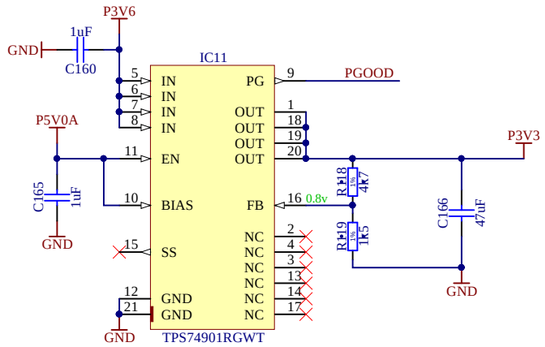


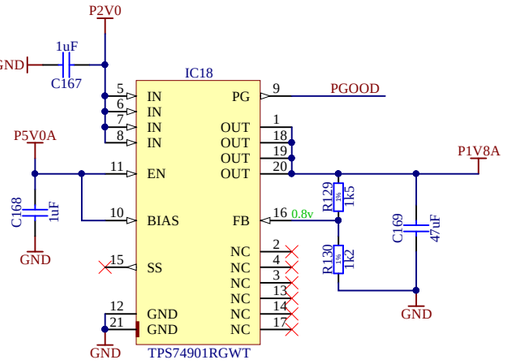


Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	11.01.2018
		File LVDS_IFC_DDS.SchDoc	
		Print Date 11.01.2018 01:09:30	Sheet 2 of 7
Warsaw Univeristy of Technology *Nowowiejska 15/19*	*ISE*	ARTIQ	Size A3 / Rev -



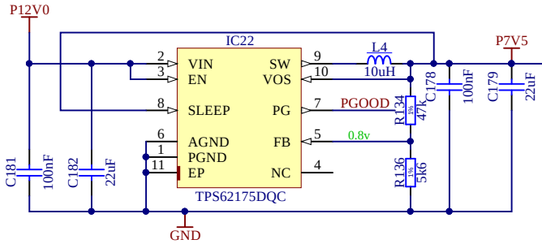


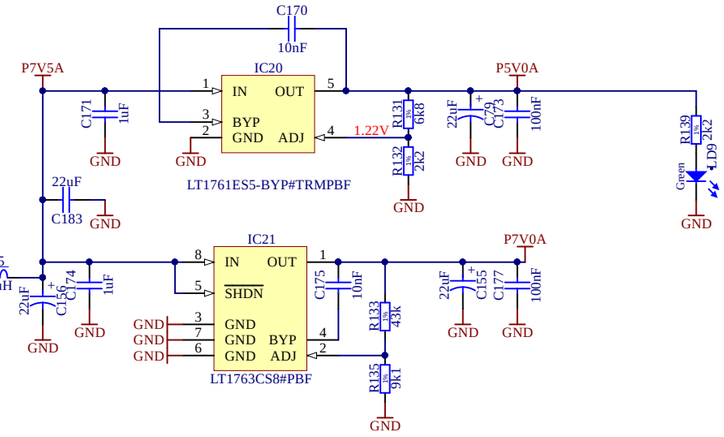


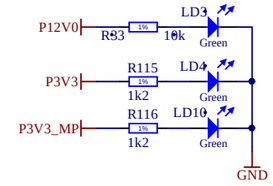


Power budget (max ratings):	AD9912 variant(mA)	AD9910 variant(mA)
P3V3:		
LVDS interface 4x	660	660
LVDS load 4x24mA	96	96
CPLD	100	100
Si53312-B-GM	240	240
Si53304	-	200
DDS AVDD3	4*(9,6+31)=133,6	4*29=116
DDS DVDDIO	4*3=12	4*11=44
TOTAL P3V3	1121	1346
TOTAL POWER	3.7	4.4
P1V8:		
DDS AVDD	4*(48+136)=736	4*110=440
DDS DVDD	4*246=984	4*222=888
TOTAL P1V8	1720	1328
TOTAL POWER	3,096	2.39
P5V0		
HMC542BLP4E	4*2.9=11.6	4*2.9=11.6
HMC349LP4C	4*3.5=14	4*3.5=14
TOTAL 5V0	25.6	25.6
TOTAL POWER	0,125	0,125
P7V0		
ERA-3XSM+	4*35=150	4*35=150
TOTAL POWER	1.05	1.05
DC/DC converter losses		
TPS62175 eff .95	0,05*(.27+0,026)*7,5=0.11	0,05*(.27+0,026)*7,5=0.11
LTM:3.6V eff .9	0.1*1,321*3,6=0,47	0,1*1,346*3,6=0,48
LTM:2V eff .87	0.13*1,721*2=0,44	0.13*1.328*2=0.34
LDO losses		
2V->1.8V	0.34	0,26
3.6V->3.3V	0.396	0.4
7.5V->7V	0,135	0,135
7.5V->5V	0,064	0,064
Total power from 12V 9.95W		9.45
Total current from 12V 0.83A		0.75A

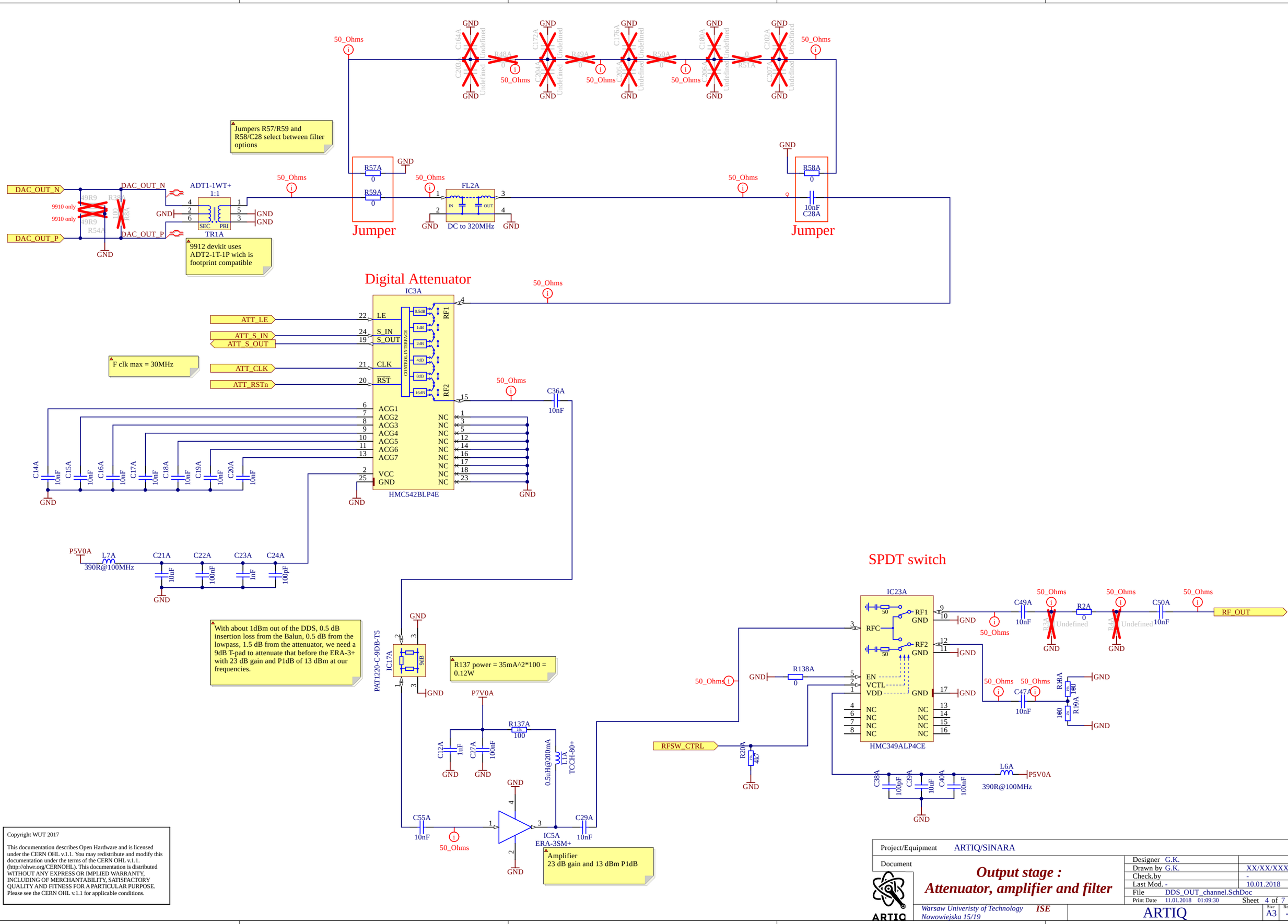
ADR: 1001 000

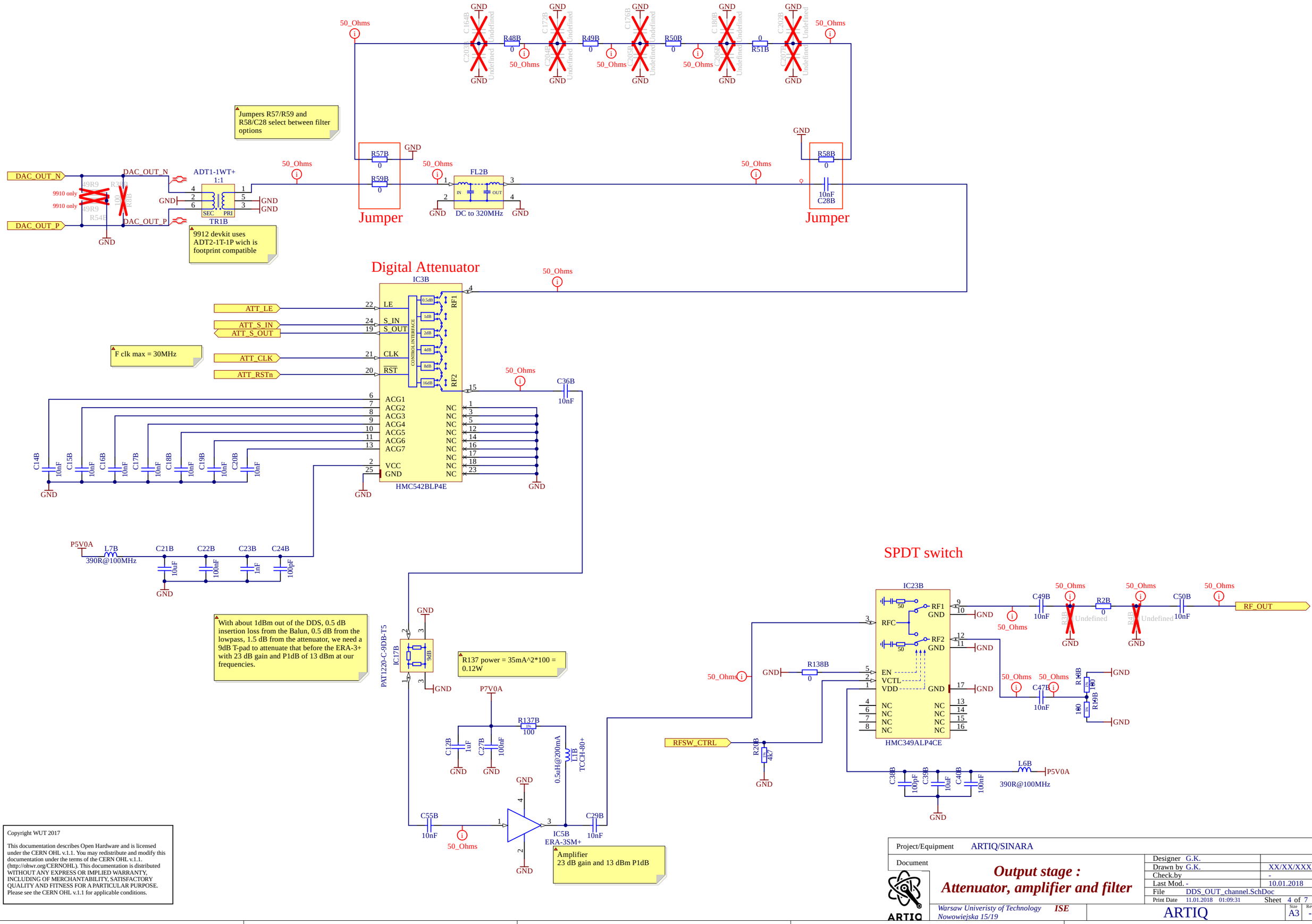


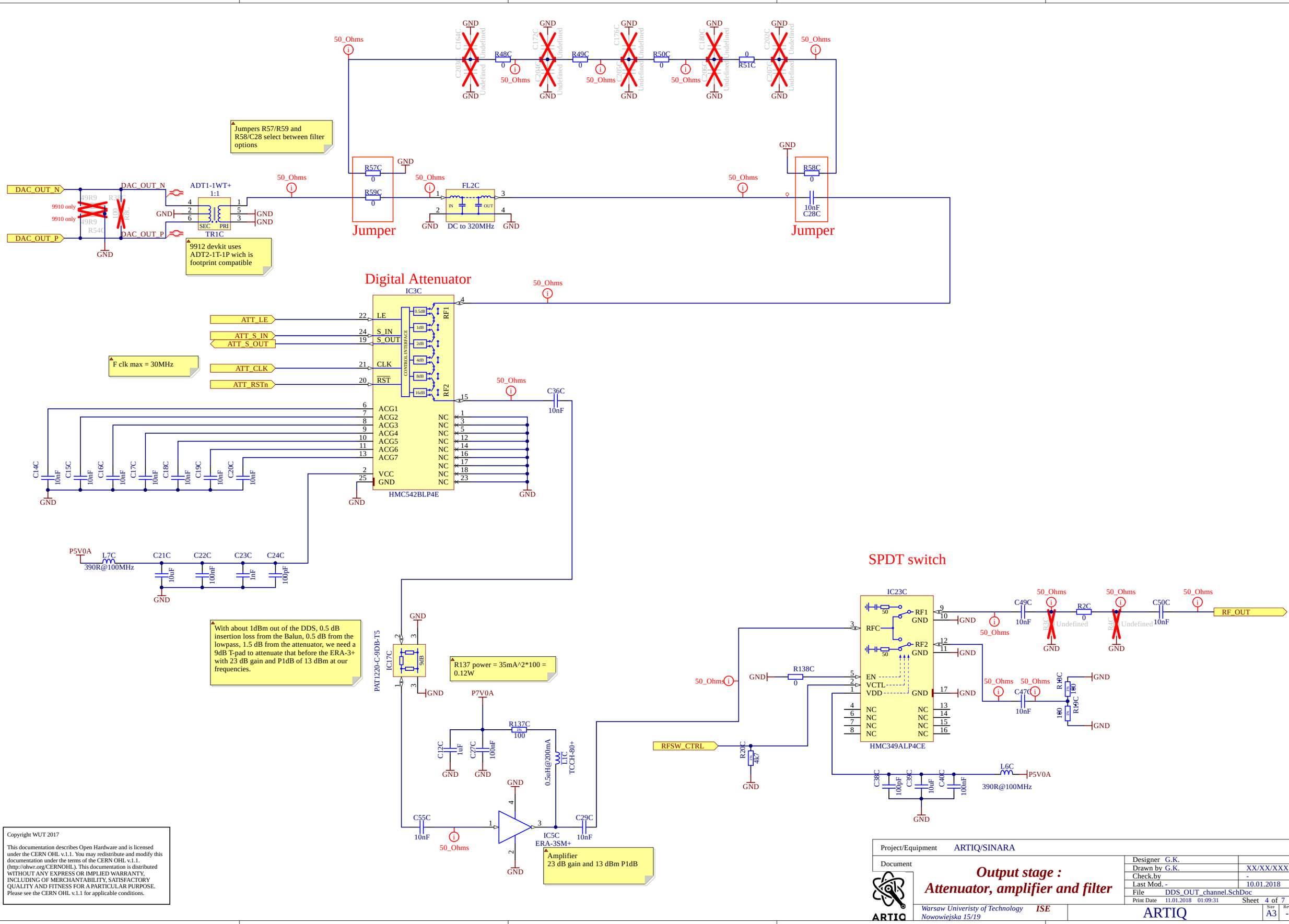


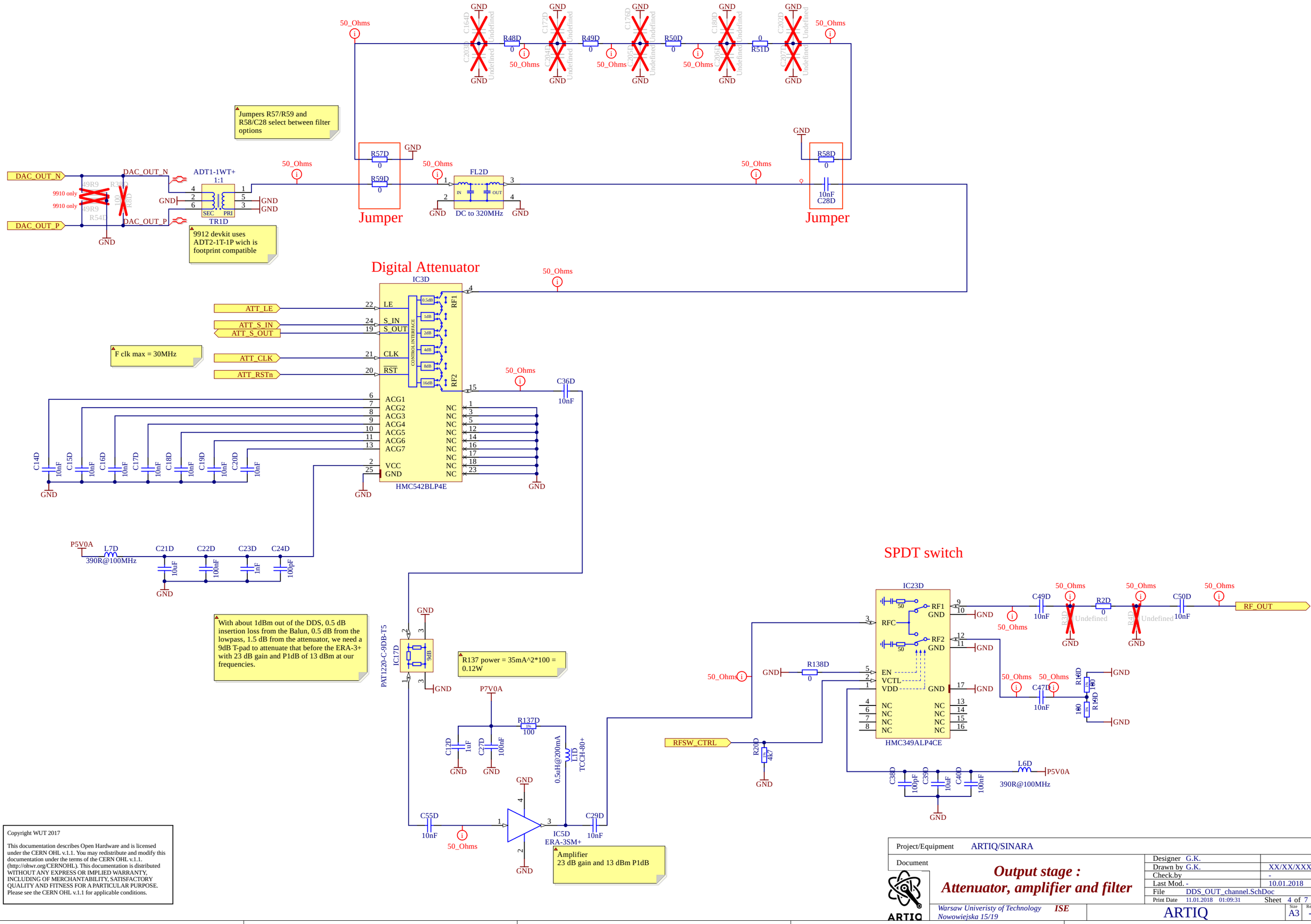


Project/Equipment	ARTIQ/SINARA		
Document	**Power supply DC/DC & LDOs**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	11.01.2018
		File Supply_DDS.SchDoc	
		Print Date 11.01.2018 01:09:30	Sheet 3 of 7
Warsaw Univeristy of Technology ISE *Nowowiejska 15/19*	ARTIQ	Size A3	Rev -


50_Ohms
GND
C164A
C203A
R48A
C172A
C204A
R49A
C176A
C205A
R50A
C180A
C206A
R51A
C202A
C207A
Undefined
Jumpers R57/R59 and R58/C28 select between filter options
R57A
R59A
Jumper
FL2A
DC to 320MHz
R58A
10nF
C28A
Jumper
DAC_OUT_N
DAC_OUT_P
9910 only
49R9
R54A
R38A
100
R8A
ADT1-1WT+
1:1
SEC
PRI
TR1A
9912 devkit uses ADT2-1T-1P wich is footprint compatible
Digital Attenuator
IC3A
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
F clk max = 30MHz
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB
1dB
2dB
4dB
8dB
16dB
RF1
RF2
ACG1
ACG2
ACG3
ACG4
ACG5
ACG6
ACG7
NC
VCC
HMC542BLP4E
C36A
10nF
C14A
C15A
C16A
C17A
C18A
C19A
C20A
P5V0A
L7A
390R@100MHz
C21A
C22A
C23A
C24A
10uF
100nF
1nF
100pF
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.
PAT1220-C-9DB-T5
IC17A
9dB
R137 power = 35mA^2*100 = 0.12W
P7V0A
R137A
100
C12A
1uF
C27A
100nF
0.5uH@200mA
L1A
TCCH-80+
C55A
10nF
IC5A
ERA-3SM+
C29A
10nF
Amplifier
23 dB gain and 13 dBm P1dB
SPDT switch
IC23A
RF1
RFC
RF2
EN
VCTL
VDD
HMC349ALP4CE
R138A
RFSW_CTRL
R20A
4k7
C49A
R2A
C50A
RF_OUT
C47A
R19A
C38A
100pF
C39A
10uF
C40A
L6A
390R@100MHz
Copyright WUT 2017
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter
Designer G.K.
Drawn by G.K. XX/XX/XXXX
Check.by -
Last Mod. - 10.01.2018
File DDS_OUT_channel.SchDoc
Print Date 11.01.2018 01:09:30 Sheet 4 of 7
Warsaw Univeristy of Technology ISE
Nowowiejska 15/19
ARTIQ
Size A3 Rev -


50_Ohms
GND
C164B
C172B
C176B
C180B
C202B
C203B
C204B
C205B
C206B
C207B
Undefined
R48B
R49B
R50B
R51B
0
Jumpers R57/R59 and R58/C28 select between filter options
R57B
R59B
R58B
Jumper
Jumper
DAC_OUT_N
DAC_OUT_P
9910 only
49R9
R54B
R8B
100
ADT1-1WT+
1:1
SEC
PRI
TR1B
9912 devkit uses ADT2-1T-1P wich is footprint compatible
FL2B
IN
OUT
DC to 320MHz
10nF
C28B
Digital Attenuator
IC3B
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
F clk max = 30MHz
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB
1dB
2dB
4dB
8dB
16dB
RF1
RF2
ACG1
ACG2
ACG3
ACG4
ACG5
ACG6
ACG7
NC
VCC
GND
HMC542BLP4E
C36B
10nF
C14B
C15B
C16B
C17B
C18B
C19B
C20B
P5V0A
L7B
390R@100MHz
C21B
C22B
C23B
C24B
10uF
100nF
1nF
100pF
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.
PAT1220-C-9DB-T5
IC17B
9dB
R137 power = 35mA^2*100 = 0.12W
P7V0A
R137B
100
C12B
1uF
C27B
100nF
0.5uH@200mA
L1B
TCCH-80+
C55B
10nF
IC5B
ERA-3SM+
C29B
10nF
Amplifier
23 dB gain and 13 dBm P1dB
SPDT switch
IC23B
RF1
RF2
RFC
EN
VCTL
VDD
HMC349ALP4CE
R138B
RFSW_CTRL
R20B
4k7
C49B
R2B
C50B
RF_OUT
R3B
R4B
C47B
R46B
R45B
C38B
C39B
C40B
L6B
390R@100MHz
Copyright WUT 2017
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter
Designer G.K.
Drawn by G.K. XX/XX/XXXX
Check.by -
Last Mod. - 10.01.2018
File DDS_OUT_channel.SchDoc
Print Date 11.01.2018 01:09:31 Sheet 4 of 7
Warsaw Univeristy of Technology ISE
Nowowiejska 15/19
ARTIQ
Size A3
Rev -


50_Ohms
GND
R48C
R49C
R50C
R51C
C164C
C172C
C176C
C180C
C202C
C203C
C204C
C205C
C206C
C207C
Undefined
Jumpers R57/R59 and R58/C28 select between filter options
R57C
R59C
R58C
Jumper
Jumper
DAC_OUT_N
DAC_OUT_P
9910 only
49R9
R54C
R8C
100
ADT1-1WT+
1:1
TR1C
SEC
PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible
FL2C
DC to 320MHz
10nF
C28C
Digital Attenuator
IC3C
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB
1dB
2dB
4dB
8dB
16dB
RF1
RF2
F clk max = 30MHz
ACG1
ACG2
ACG3
ACG4
ACG5
ACG6
ACG7
VCC
NC
C14C
C15C
C16C
C17C
C18C
C19C
C20C
C36C
HMC542BLP4E
P5V0A
L7C
390R@100MHz
C21C
C22C
C23C
C24C
10uF
100nF
1nF
100pF
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.
PAT1220-C-9DB-T5
IC17C
9dB
R137 power = 35mA^2*100 = 0.12W
P7V0A
R137C
C12C
C27C
0.5uH@200mA
L1C
TCCH-80+
C55C
C29C
IC5C
ERA-3SM+
Amplifier
23 dB gain and 13 dBm P1dB
SPDT switch
IC23C
RF1
RF2
RFC
EN
VCTL
VDD
HMC349ALP4CE
RFSW_CTRL
R20C
4k7
R138C
C49C
R2C
C50C
RF_OUT
C47C
C38C
C39C
C40C
L6C
390R@100MHz
Copyright WUT 2017
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter
Designer G.K.
Drawn by G.K.
XX/XX/XXXX
Check.by -
Last Mod. -
10.01.2018
File DDS_OUT_channel.SchDoc
Print Date 11.01.2018 01:09:31
Sheet 4 of 7
Warsaw Univeristy of Technology
Nowowiejska 15/19
ISE
ARTIQ
Size A3
Rev -


50_Ohms
GND
C164D
C172D
C176D
C180D
C202D
R48D
R49D
R50D
R51D
C203D
C204D
C205D
C206D
C207D
Undefined
Jumpers R57/R59 and R58/C28 select between filter options
R57D
R59D
R58D
Jumper
Jumper
DAC_OUT_N
DAC_OUT_P
9910 only
49R9
R53D
R54D
100
R8D
ADT1-1WT+
1:1
TR1D
SEC
PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible
FL2D
IN
OUT
DC to 320MHz
10nF
C28D
Digital Attenuator
IC3D
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
F clk max = 30MHz
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB
1dB
2dB
4dB
8dB
16dB
RF1
RF2
ACG1
ACG2
ACG3
ACG4
ACG5
ACG6
ACG7
NC
VCC
GND
HMC542BLP4E
C36D
10nF
C14D
C15D
C16D
C17D
C18D
C19D
C20D
P5V0A
L7D
390R@100MHz
C21D
C22D
C23D
C24D
10uF
100nF
1nF
100pF
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.
PAT1220-C-9DB-T5
IC17D
9dB
R137 power = 35mA^2*100 = 0.12W
P7V0A
R137D
100
C12D
1uF
C27D
100nF
0.5uH@200mA
L1D
TCCH-80+
C55D
10nF
IC5D
ERA-3SM+
C29D
10nF
Amplifier
23 dB gain and 13 dBm P1dB
SPDT switch
IC23D
RF1
RFC
RF2
EN
VCTL
VDD
HMC349ALP4CE
R138D
RFSW_CTRL
R20D
4k7
C49D
R2D
C50D
RF_OUT
R3D Undefined
R4D Undefined
C47D
R46D
R45D
C38D
100pF
C39D
10uF
C40D
100nF
L6D
390R@100MHz
Copyright WUT 2017
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter
Designer G.K.
Drawn by G.K. XX/XX/XXXX
Check.by -
Last Mod. - 10.01.2018
File DDS_OUT_channel.SchDoc
Print Date 11.01.2018 01:09:31 Sheet 4 of 7
Warsaw Univeristy of Technology ISE
Nowowiejska 15/19
ARTIQ
Size A3
Rev -

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Loop filter calculation:
Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

Cannot open file
D:\Dropbox\DESIGNS\MTCA_projects\SINARA\ARTIQ_ALTIUM\Kasli\3U\PCB_3U_DDS\Sx_table.PNG

IC13A
AD9912ABCPZ

IC2A
AD9910BSVZ

separate RSET and loop filter components due to layout constraints

Loop filter calculation:
Reference input frequency : 31.25MHz
PFD : 31.25MHz
multiplication factor:32
system clock frequency : 1GHz
desired phase margin: 45deg
Open loop BW: 3MHz

Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 11.12.2017
File	DDS_channel.SchDoc
Print Date	11.01.2018 01:09:32 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Loop filter calculation:
Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

Cannot open file
D:\Dropbox\DESIGNS\MTCA_projects\SINARA\ARTIQ_ALTIUM\Kasli\3U\PCB_3U_DDS\Sx_table.PNG

IC13B
AD9912ABCPZ

IC2B
AD9910BSVZ

Loop filter calculation:
Reference input frequency : 31.25MHz
PFD : 31.25MHz
multiplication factor:32
system clock frequency : 1GHz
desired phase margin: 45deg
Open loop BW: 3MHz

Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 11.12.2017
File	DDS_channel.SchDoc
Print Date	11.01.2018 01:09:32 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Loop filter calculation:
Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

Cannot open file
D:\Dropbox\DESIGNS\MTCA_projects\SINARA\ARTIQ_ALTIUM\Kasli\3U\PCB_3U_DDS\Sx_table.PNG

IC13C
AD9912ABCPZ

IC2C
AD9910BSVZ

Loop filter calculation:
Reference input frequency : 31.25MHz
PFD : 31.25MHz
multiplication factor:32
system clock frequency : 1GHz
desired phase margin: 45deg
Open loop BW: 3MHz

Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K.
Check.by	
Last Mod.	-
File	DDS_channel.SchDoc
Print Date	11.01.2018 01:09:33
Sheet	5 of 7
Size	A3
Rev	-

Warsaw Univeristy of Technology ISE
Nowowiejska 15/19

ARTIQ

separate RSET and loop filter components due to layout constraints

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Loop filter calculation:
Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

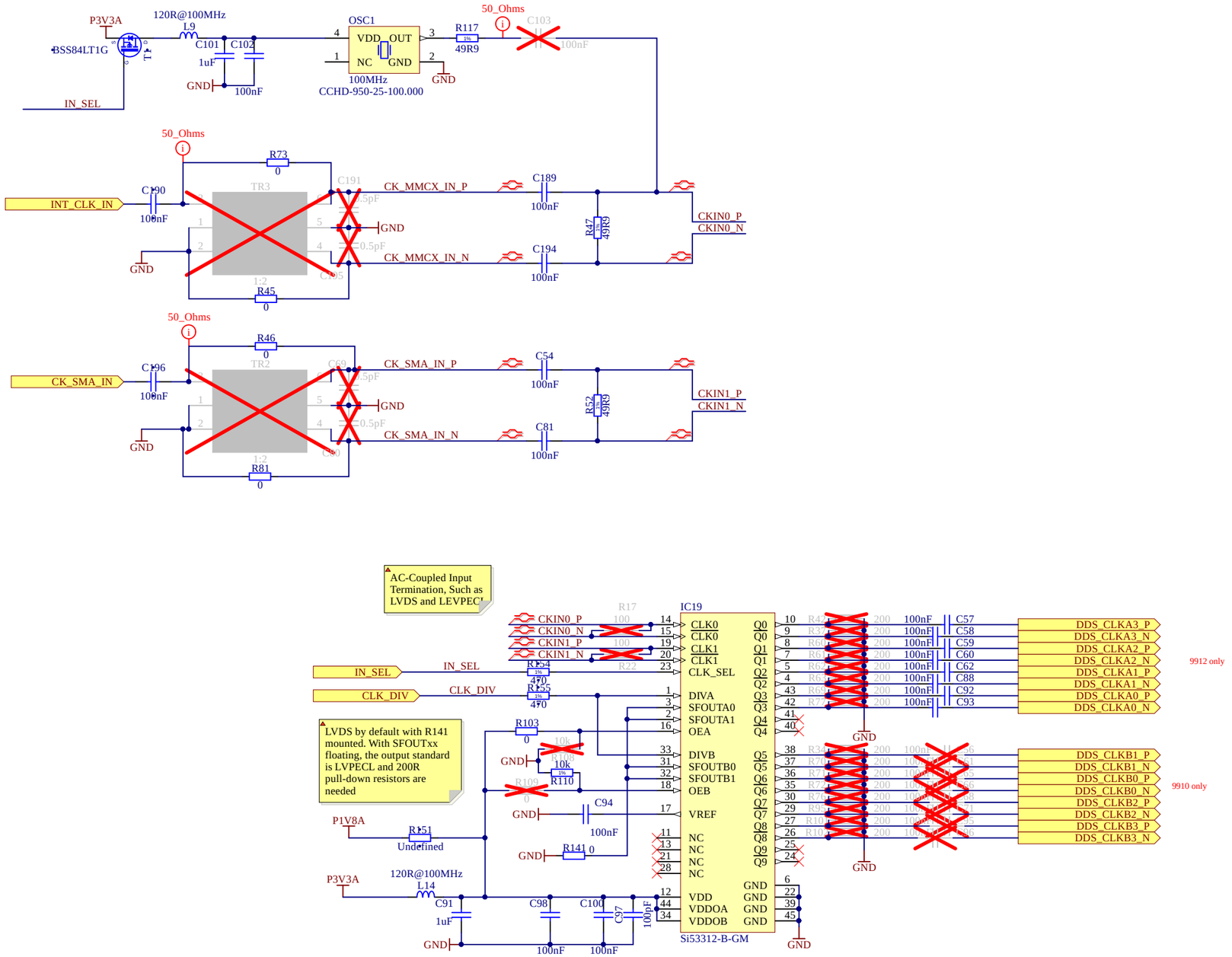
Cannot open file
D:\Dropbox\DESIGNS\MTCA_projects\SINARA\ARTIQ_ALTIUM\Kasli\3U\PCB_3U_DDS\Sx_table.PNG

IC13D
AD9912ABCPZ

IC2D
AD9910BSVZ

Loop filter calculation:
Reference input frequency : 31.25MHz
PFD : 31.25MHz
multiplication factor:32
system clock frequency : 1GHz
desired phase margin: 45deg
Open loop BW: 3MHz

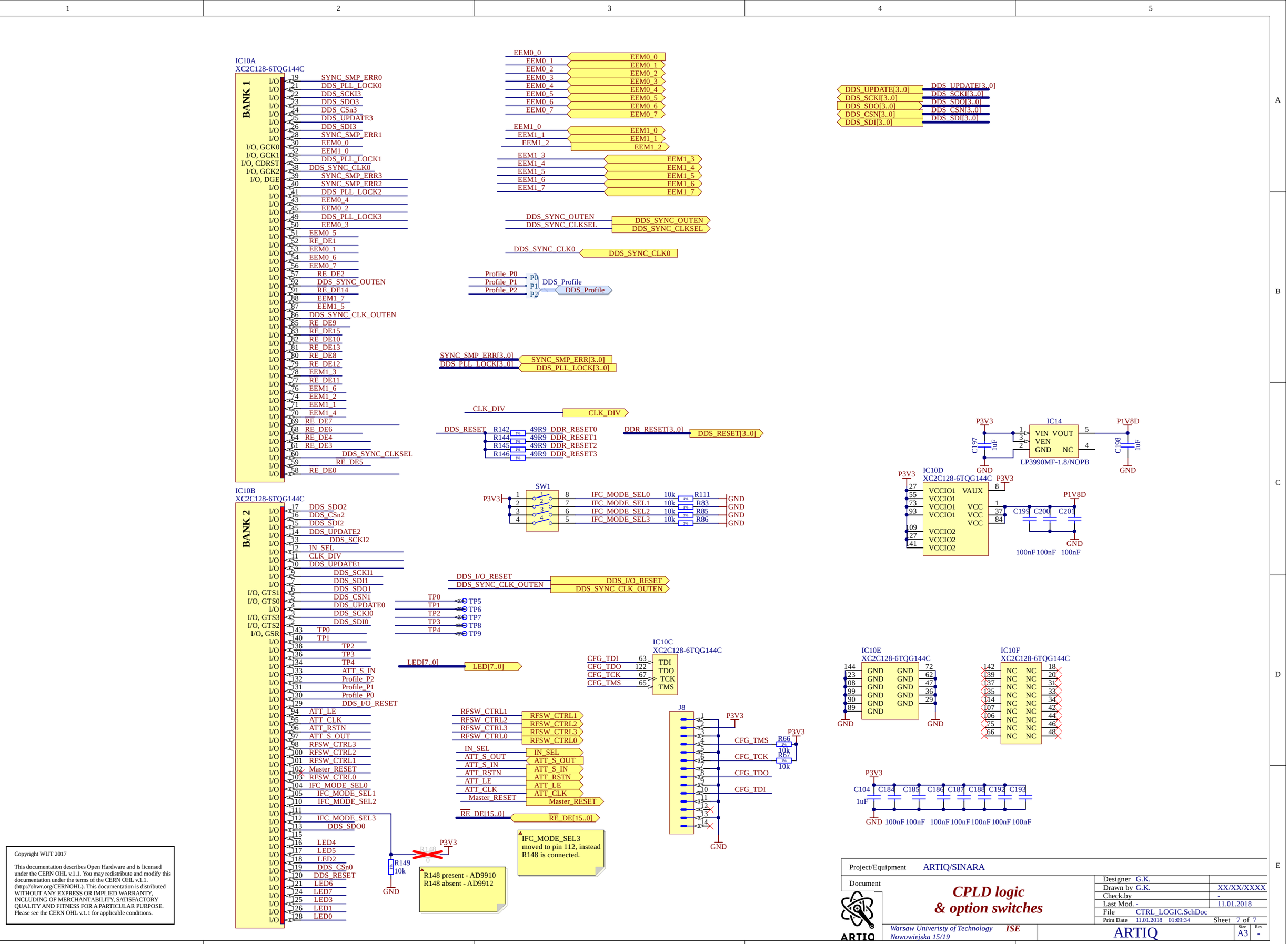
Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 11.12.2017
File	DDS_channel.SchDoc
Print Date	11.01.2018 01:09:33 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -



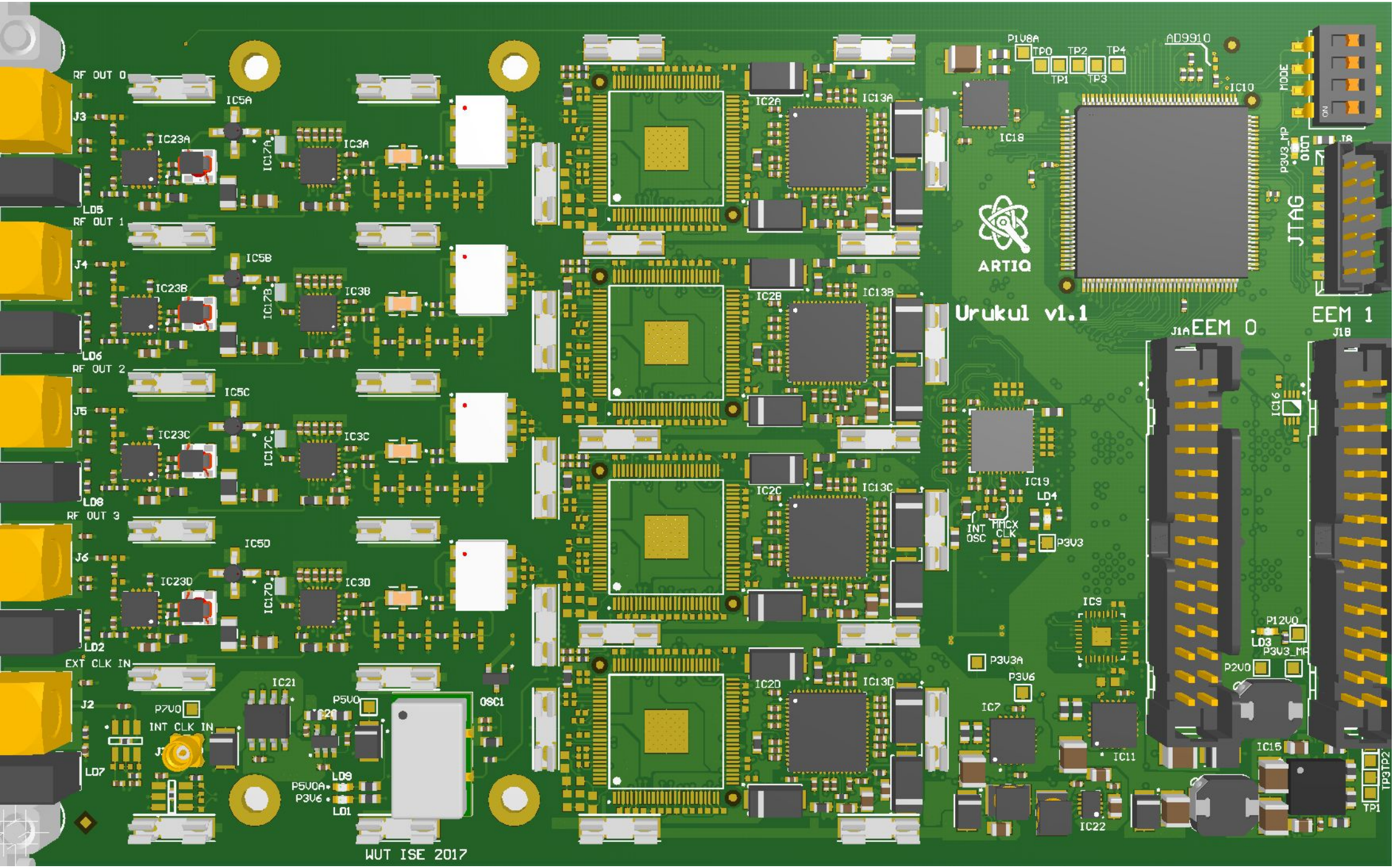
Project/Equipment	ARTIQ/SINARA		
Document	**Clock distribution and generation**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	10.01.2018
		File CLK_INPUT.SchDoc	
		Print Date 11.01.2018 01:09:33	Sheet 6 of 7

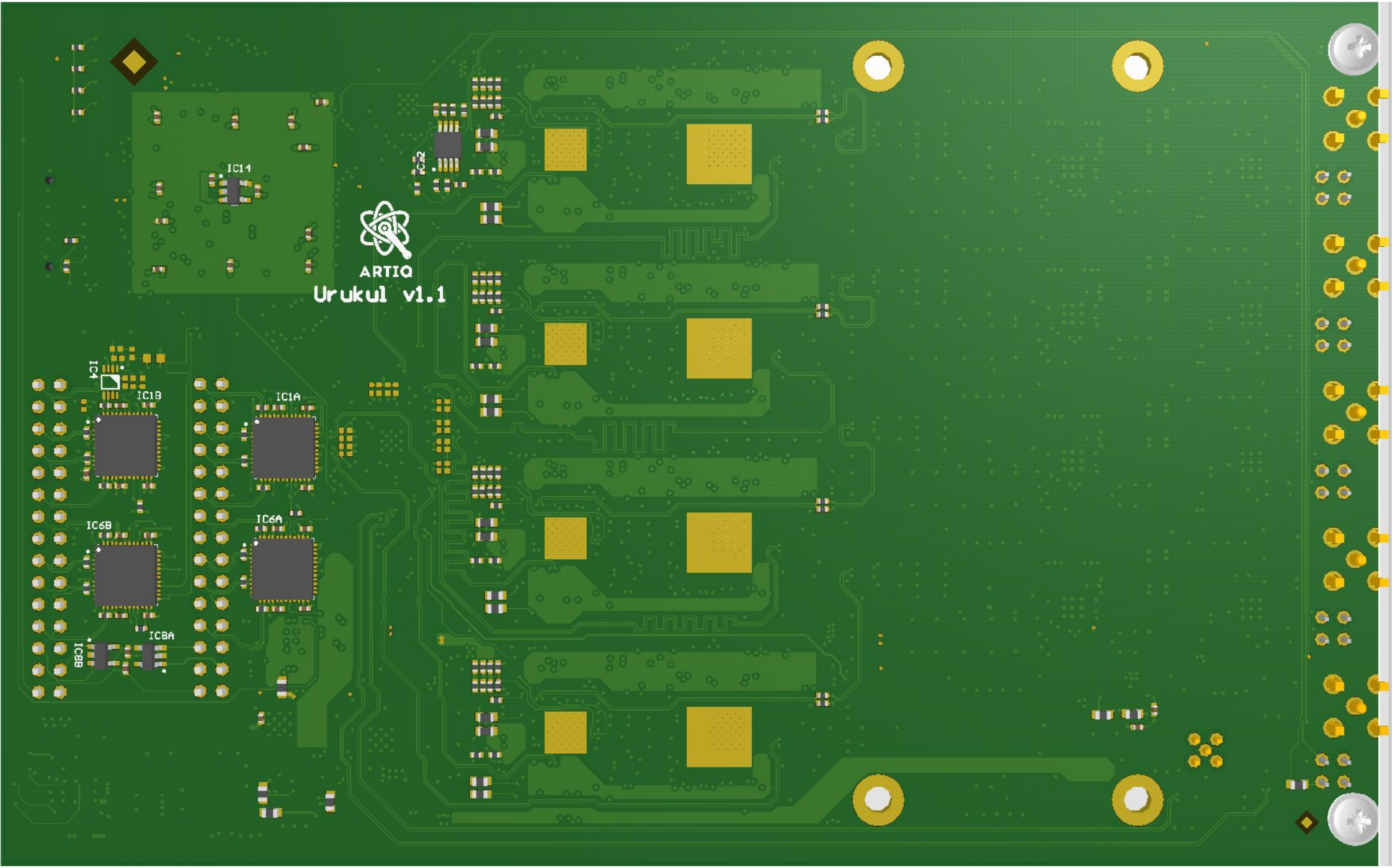
Warsaw Univeristy of Technology *ISE*
Nowowiejska 15/19

ARTIQ | Size A3 | Rev -

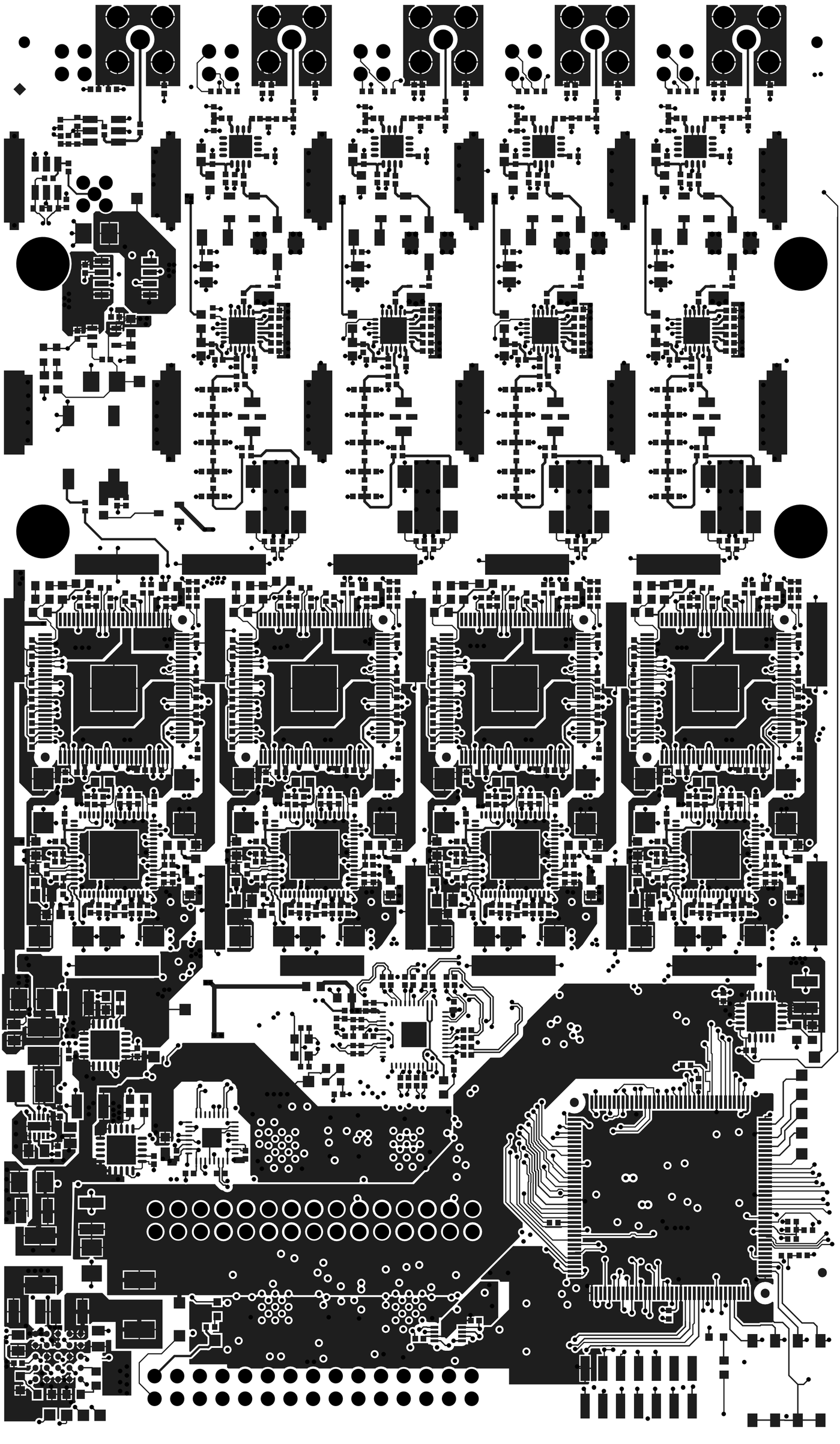


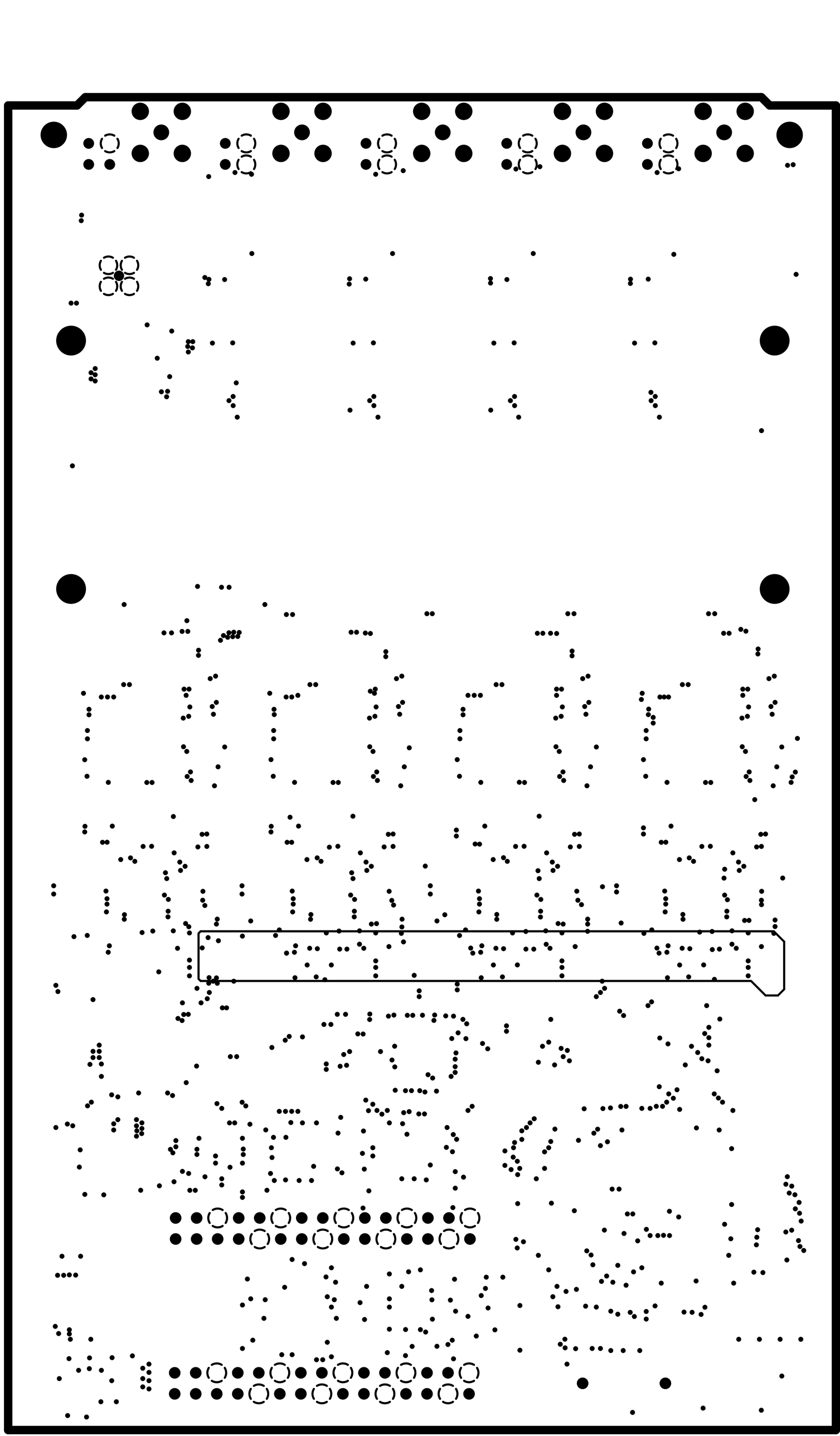
Project/Equipment	ARTIQ/SINARA
Document	**CPLD logic & option switches**
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 11.01.2018
File	CTRL_LOGIC.SchDoc
Print Date	11.01.2018 01:09:34 Sheet 7 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

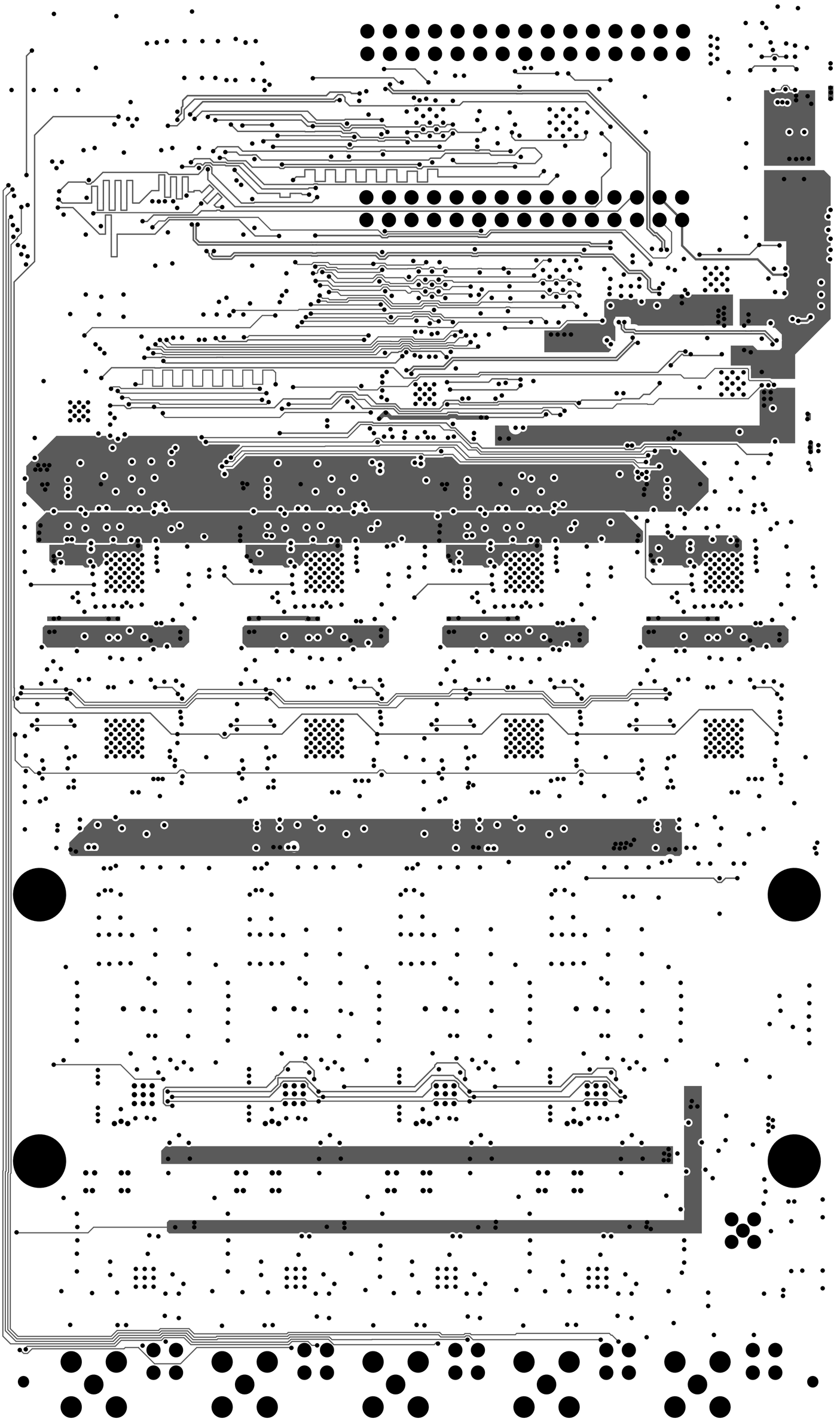

RF OUT 0
RF OUT 1
RF OUT 2
RF OUT 3
EXT CLK IN
INT CLK IN
WUT ISE 2017
Urukul v1.1
ARTIQ
EEM 0
EEM 1
JTAG
AD9910
MODE
P3V3_MP
P1V8A
P2V0
P5V0
P5V0A
P3V6
P3V3
P3V3A
P12V0
INT OSC
MMCX CLK
OSC1
IC10
IC18
IC19
IC9
IC7
IC11
IC15
IC22
IC16
IC21
IC2A
IC2B
IC2C
IC2D
IC13A
IC13B
IC13C
IC13D
IC5A
IC5B
IC5C
IC5D
IC3A
IC3B
IC3C
IC3D
IC17A
IC17B
IC17C
IC17D
IC23A
IC23B
IC23C
IC23D
J1A
J1B
J2
J3
J4
J5
J6
LD1
LD2
LD3
LD4
LD5
LD6
LD7
LD8
LD9
TP0
TP1
TP2
TP3
TP4
TP1
TP2
TP3

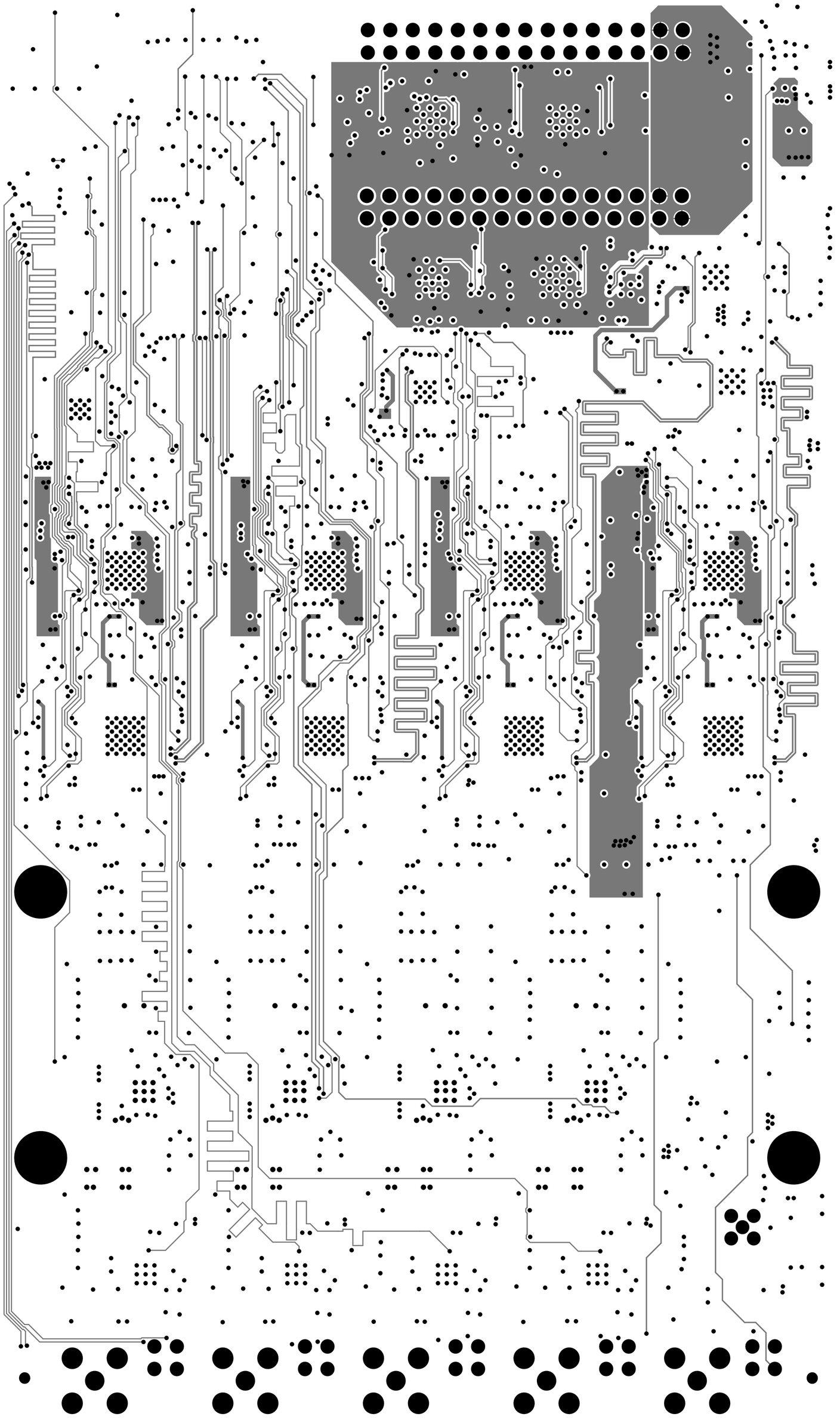

IC14
IC2
ARTIQ
Urukul v1.1
IC4
IC1B
IC1A
IC6B
IC6A
IC8A
IC8B

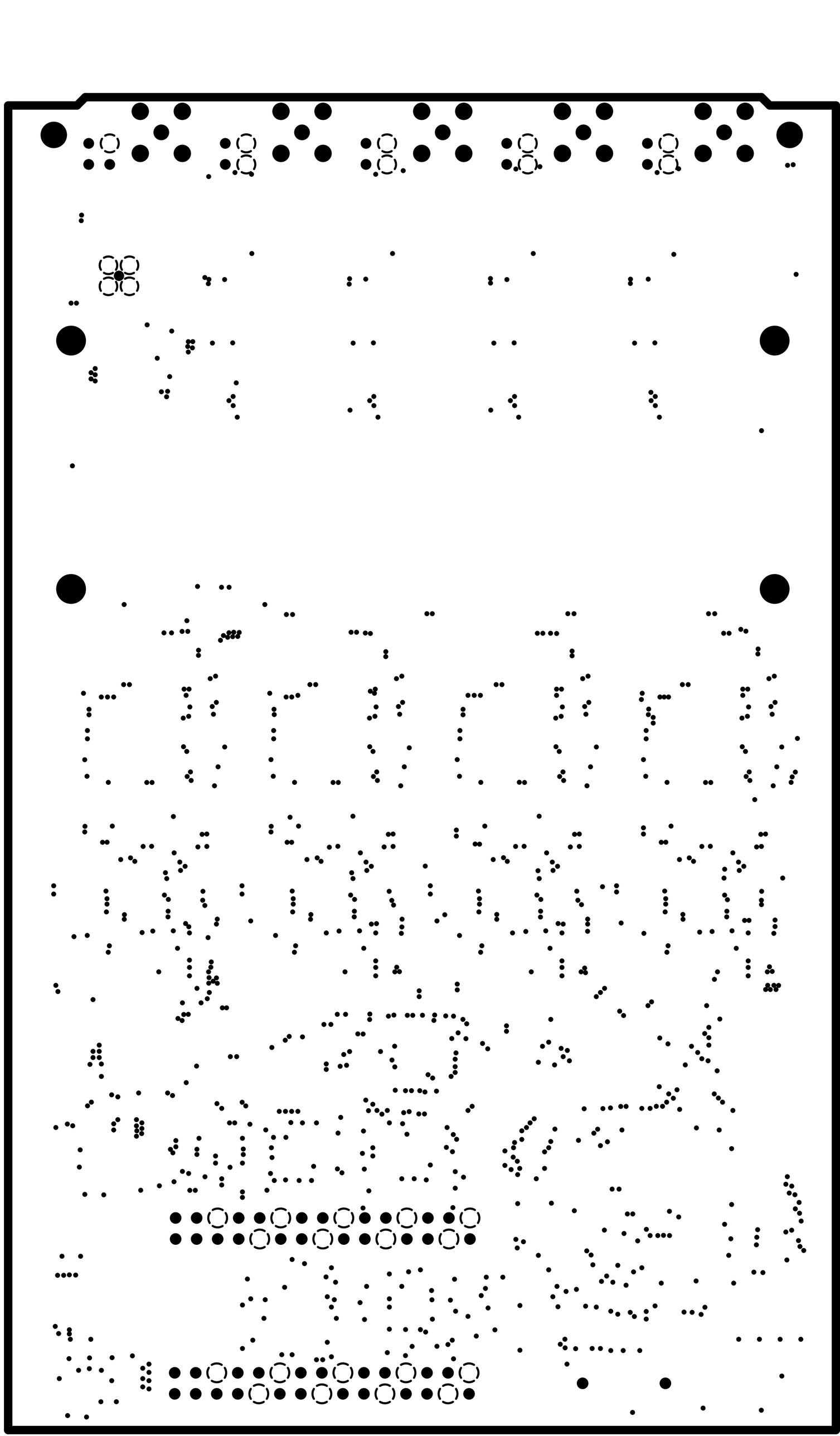
RF OUT 0
RF OUT 1
RF OUT 2
RF OUT 3
EXT CLK IN
INT CLK IN
J1A
EEM 0
J1B
EEM 1
Urukul v1.1
ARTIQ
WUT ISE 2017

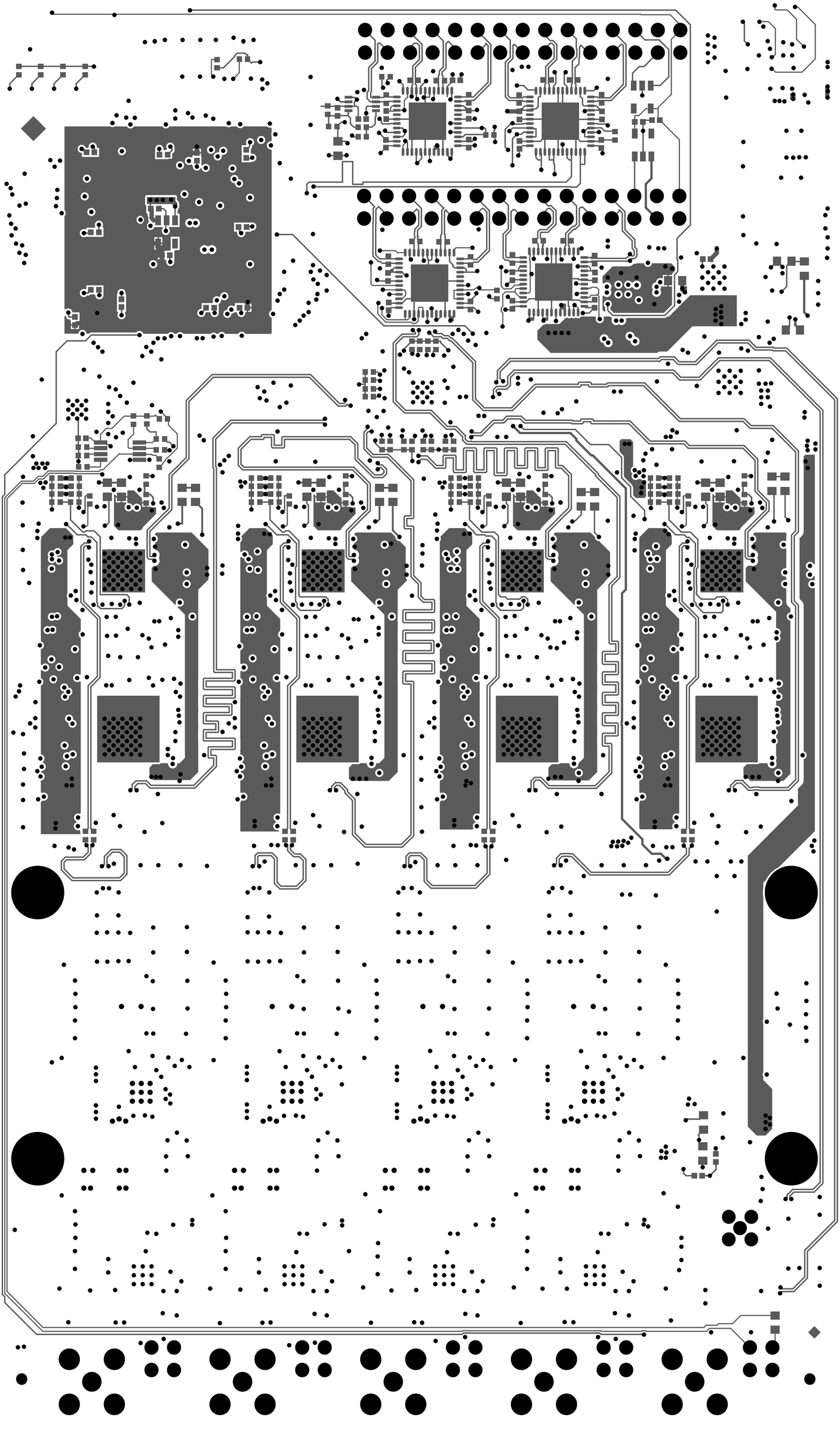












IC15
IC14
ARTIQ
Urukul v1.1
IC4
IC1A
IC1B
IC6A
IC6B
IC8A
IC8B