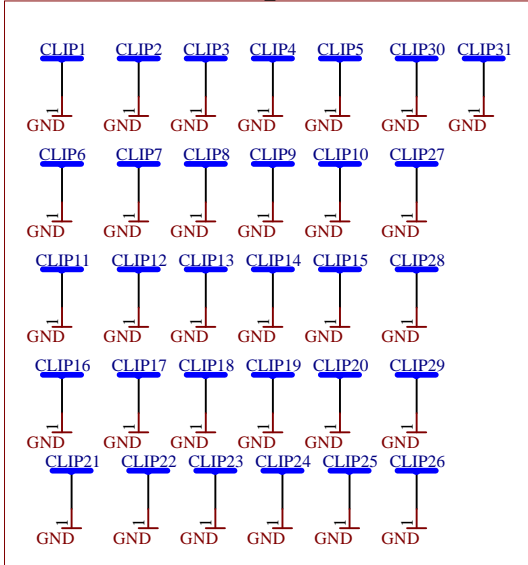


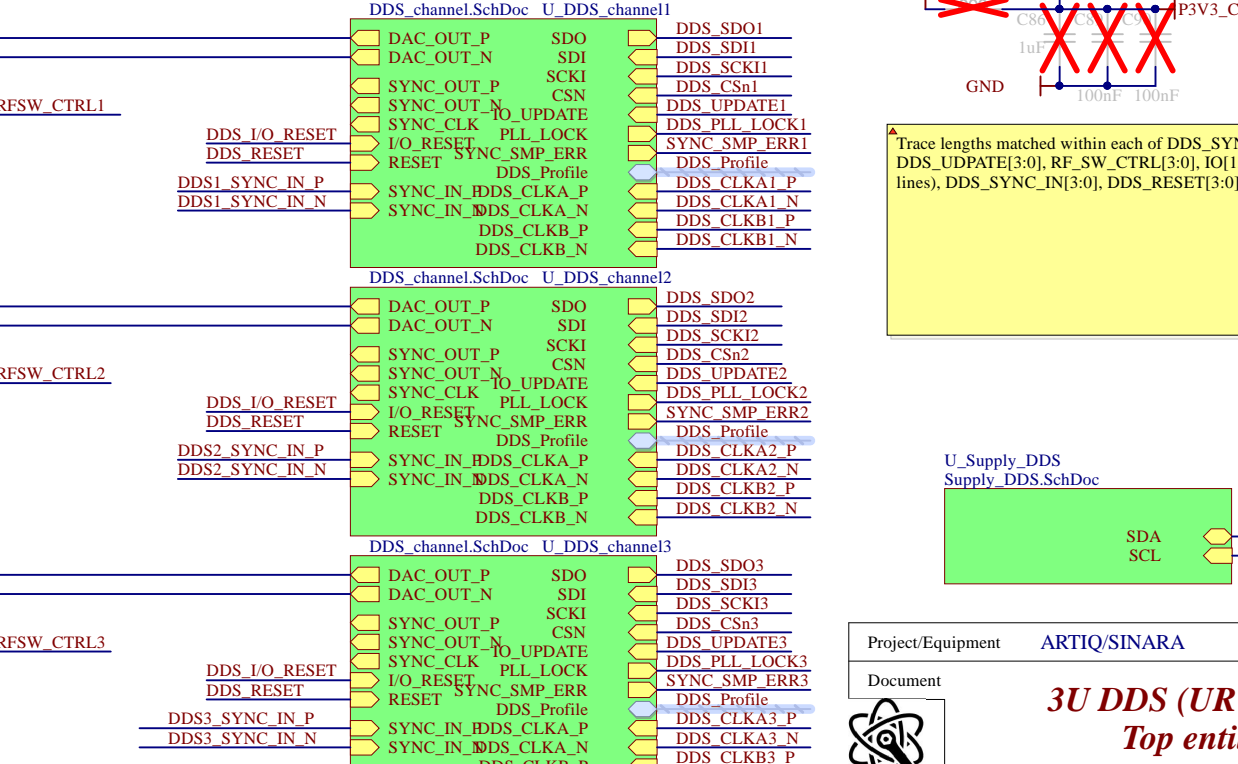
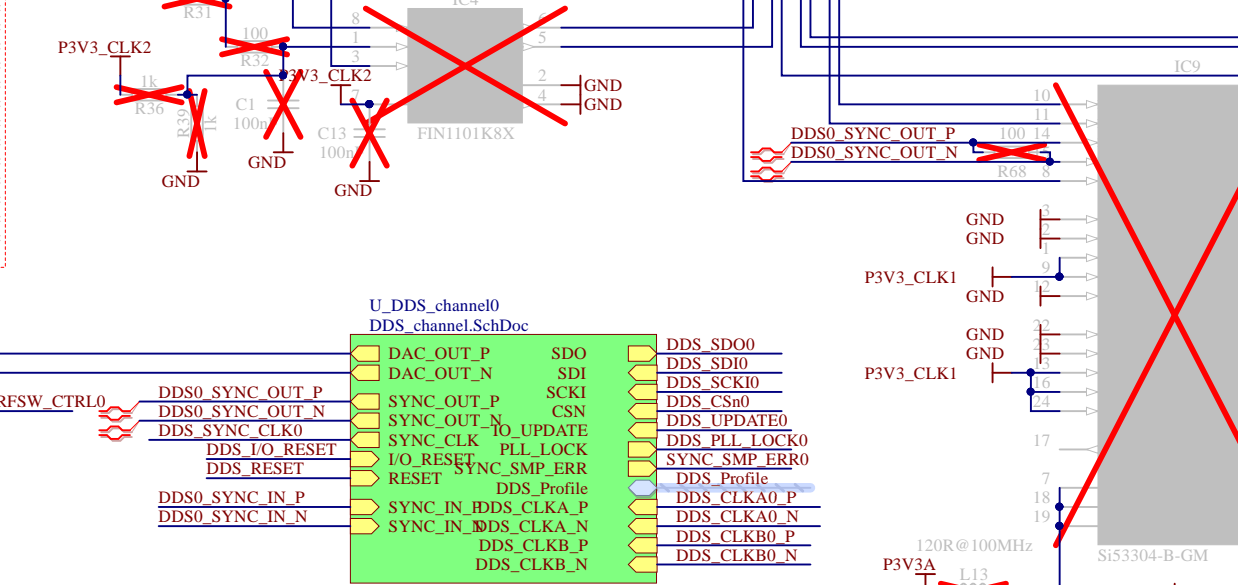
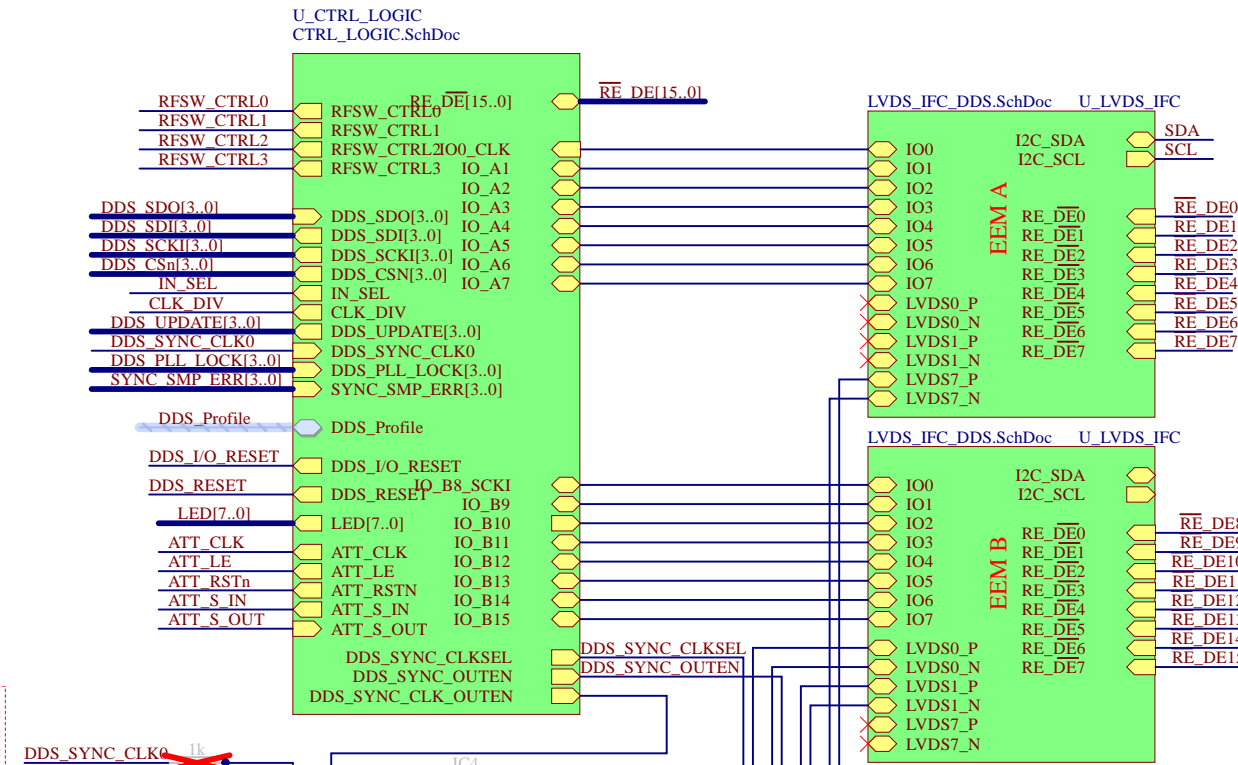
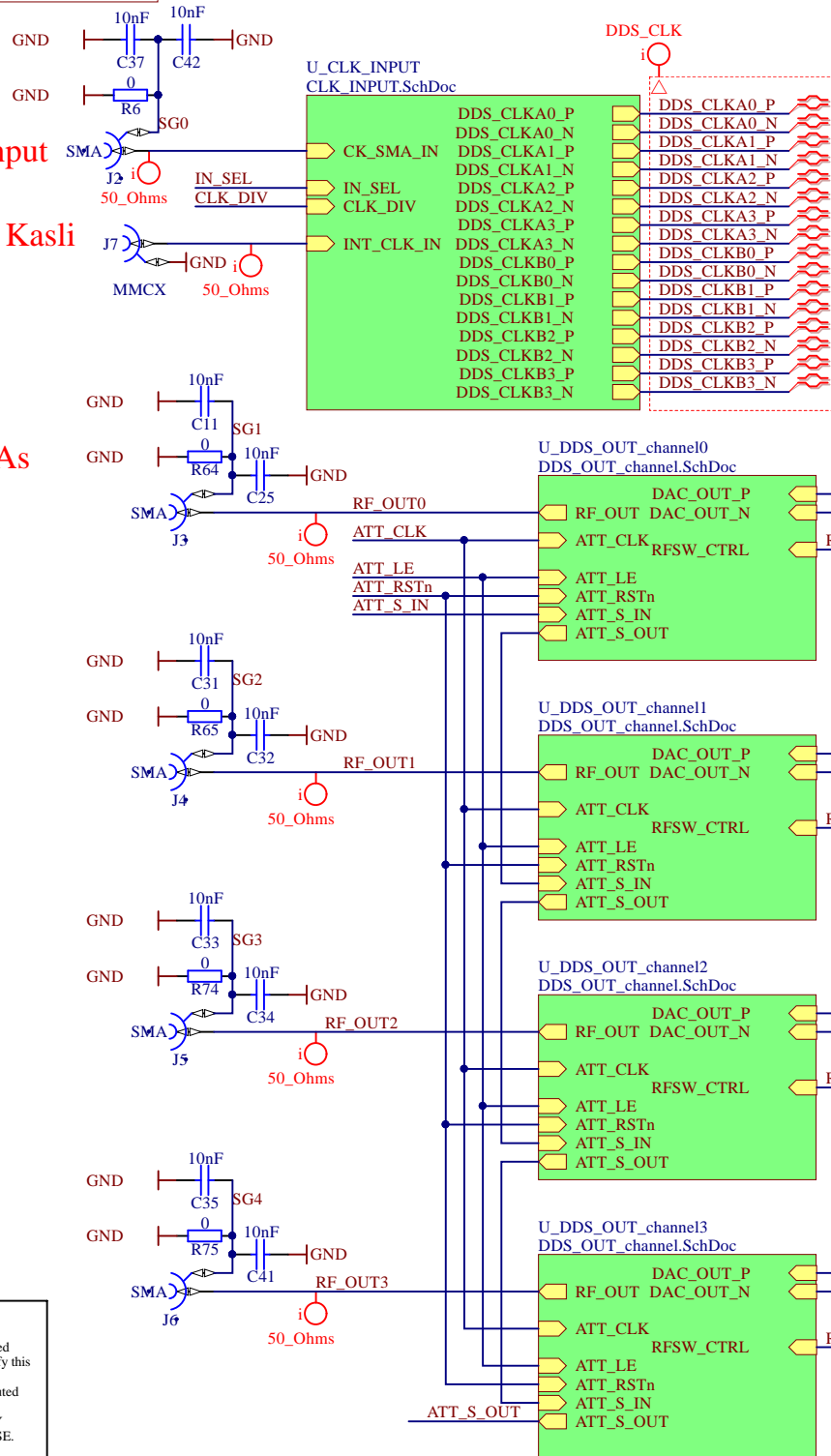
shield clips



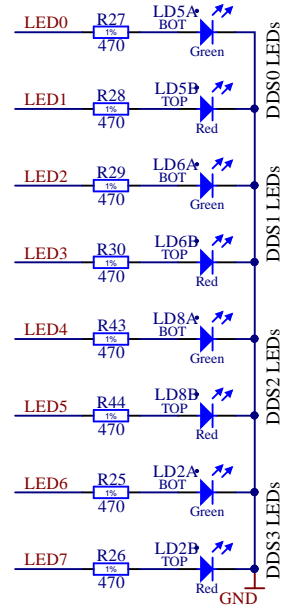
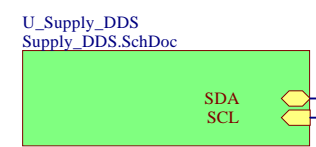
Ext clock input

Clock from Kasli

Output SMAs

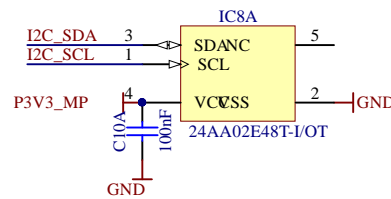
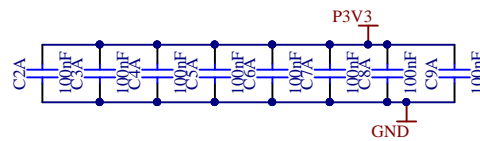
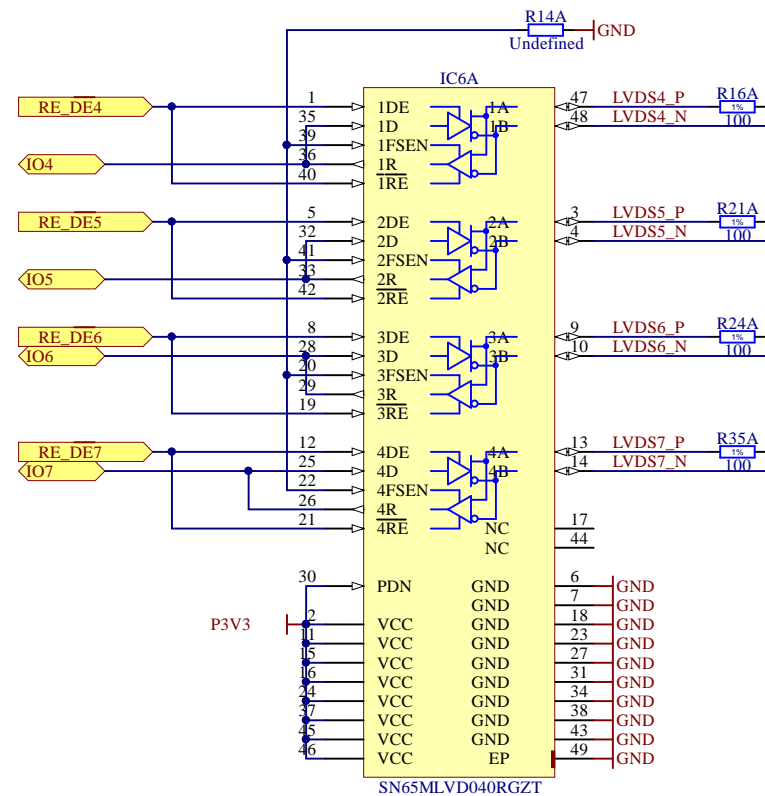
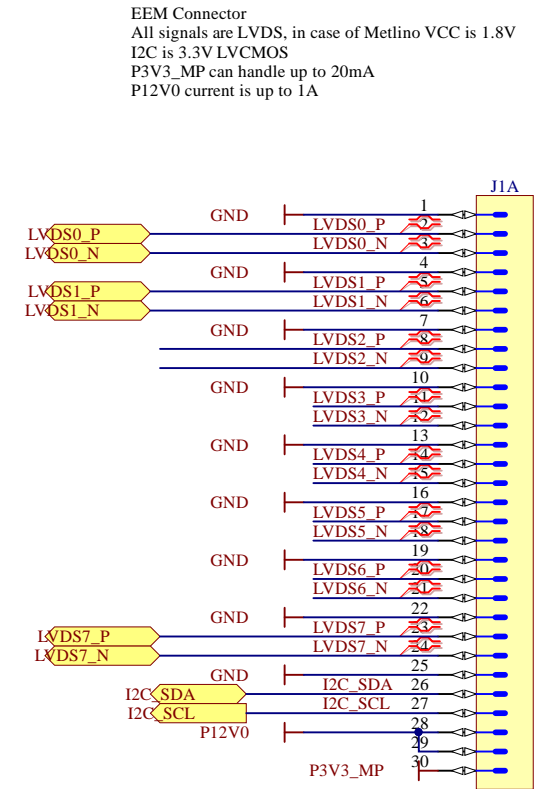
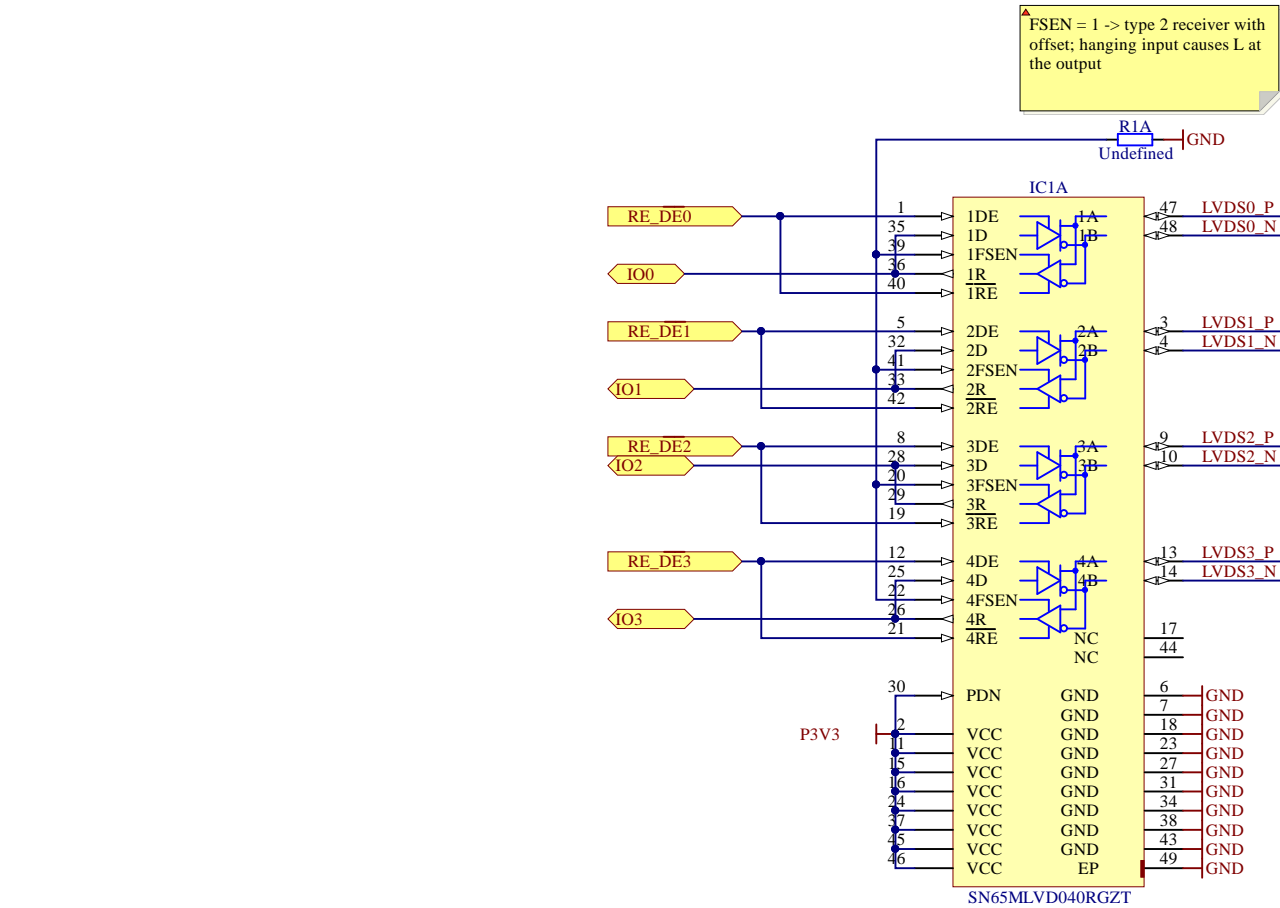


Trace lengths matched within each of DDS_SYNC_CLK[3:0], DDS_UPDATE[3:0], RF_SW_CTRL[3:0], IO[15:11] (RF_SW ctrl lines), DDS_SYNC_IN[3:0], DDS_RESET[3:0], DDS_CLK[3:0]




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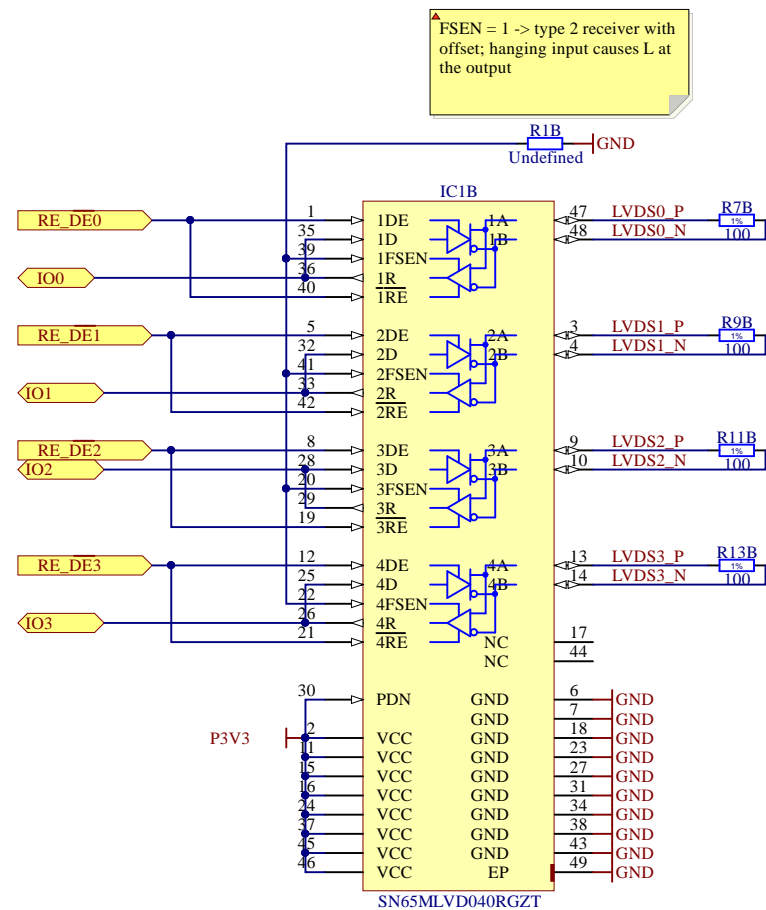
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Document		3U DDS (URUKUL) Top entity	
Designer		G.K.	XX/XX/XXXX
Drawn by		G.K.	-
Check by		-	10.10.2017
Last Mod. -		-	-
File		PCB_3U_DDS.schdoc	Sheet 1 of 7
Print Date		10.10.2017 01:06:16	Size A3
Warsaw University of Technology		ISE	Rev -
Nowowiejska 15/19		ARTIQ	-



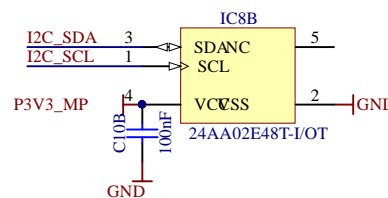
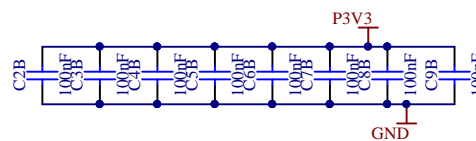
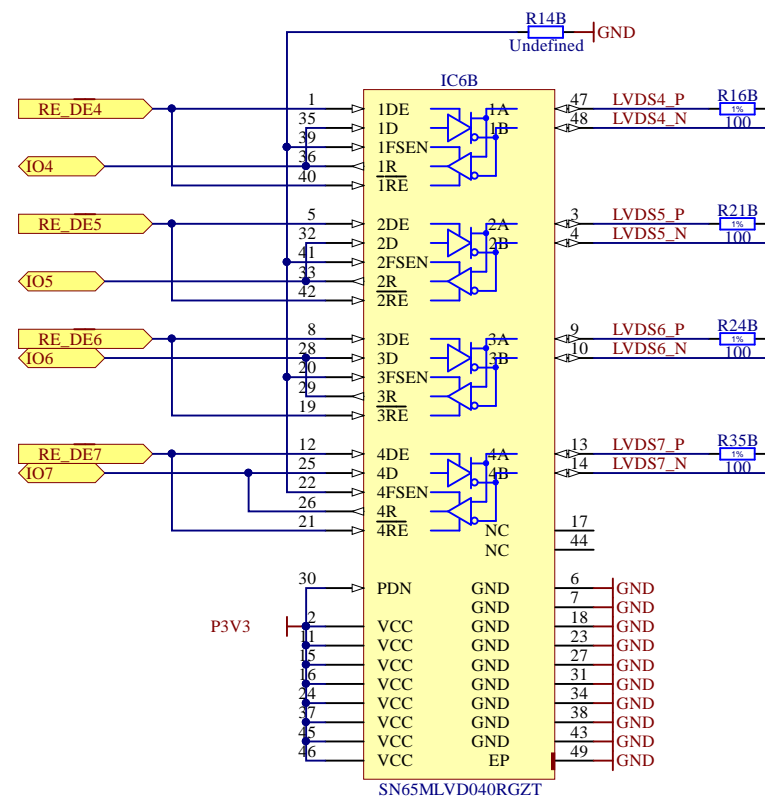
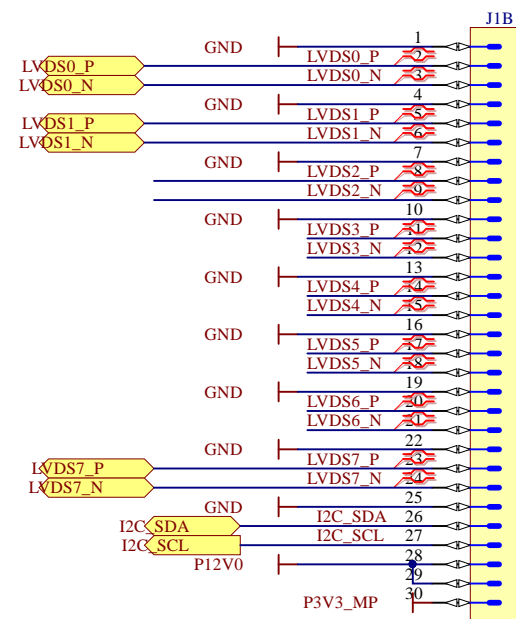
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Project/Equipment	ARTIQ/SINARA		
Document	<div><div></div><div>LVDS to LVTTL interface & EEM connector</div><div>Warsaw Univeristy of Technology ISE Nowowiejska 15/19</div></div>		
Designer	G.K.	XX/XX/XXXX	
Drawn by	G.K.	-	
Check by	-	10.10.2017	
Last Mod.	-		
File	LVDS_IFC_DDS.SchDoc	Sheet	2 of 7
Print Date	10.10.2017 01:06:16	Size	A3
		Rev	-



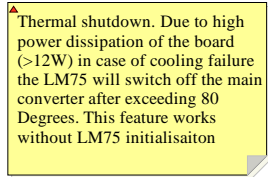
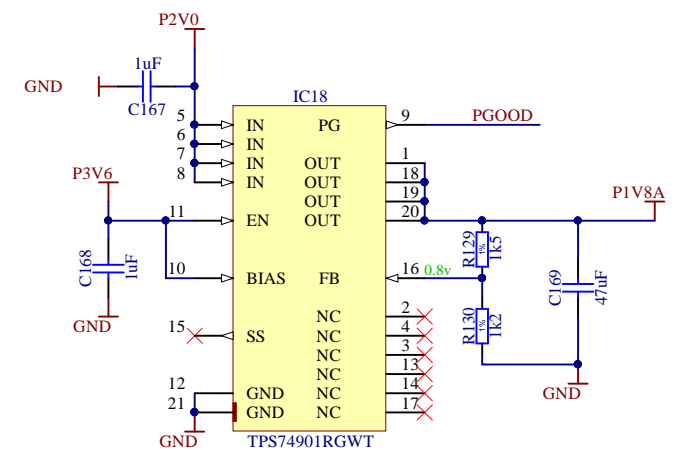
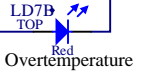
EEM Connector
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A












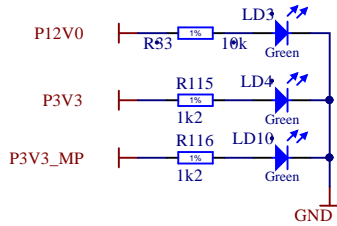
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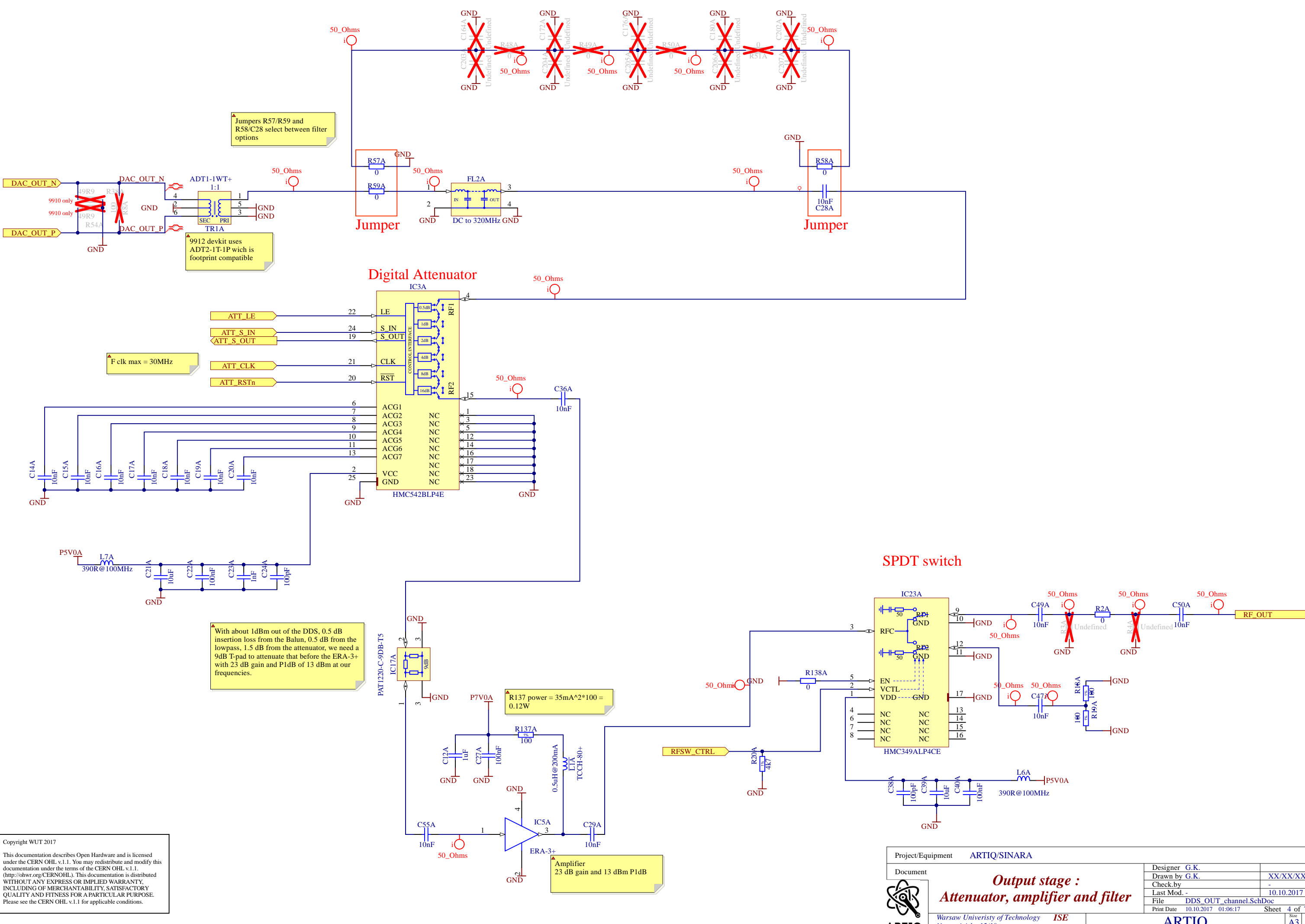
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	<div><div>LVDS to LVTTL</div><div>interface & EEM connector</div></div>		
	<div><div>Warsaw University of Technology ISE</div><div>Nowowiejska 15/19</div></div>		
	<div>ARTIQ</div>		


$$R_{fb} = 0.6 / (V_{out} - 0.6) * 60.4k$$


P1V8A		TP10
P2V0		TP11
P3V3		TP12
P3V3A		TP13
3V3_MP		TP14
P3V6		TP15
P5V0A		TP16
P7V0A		TP17
P12V0		TP18

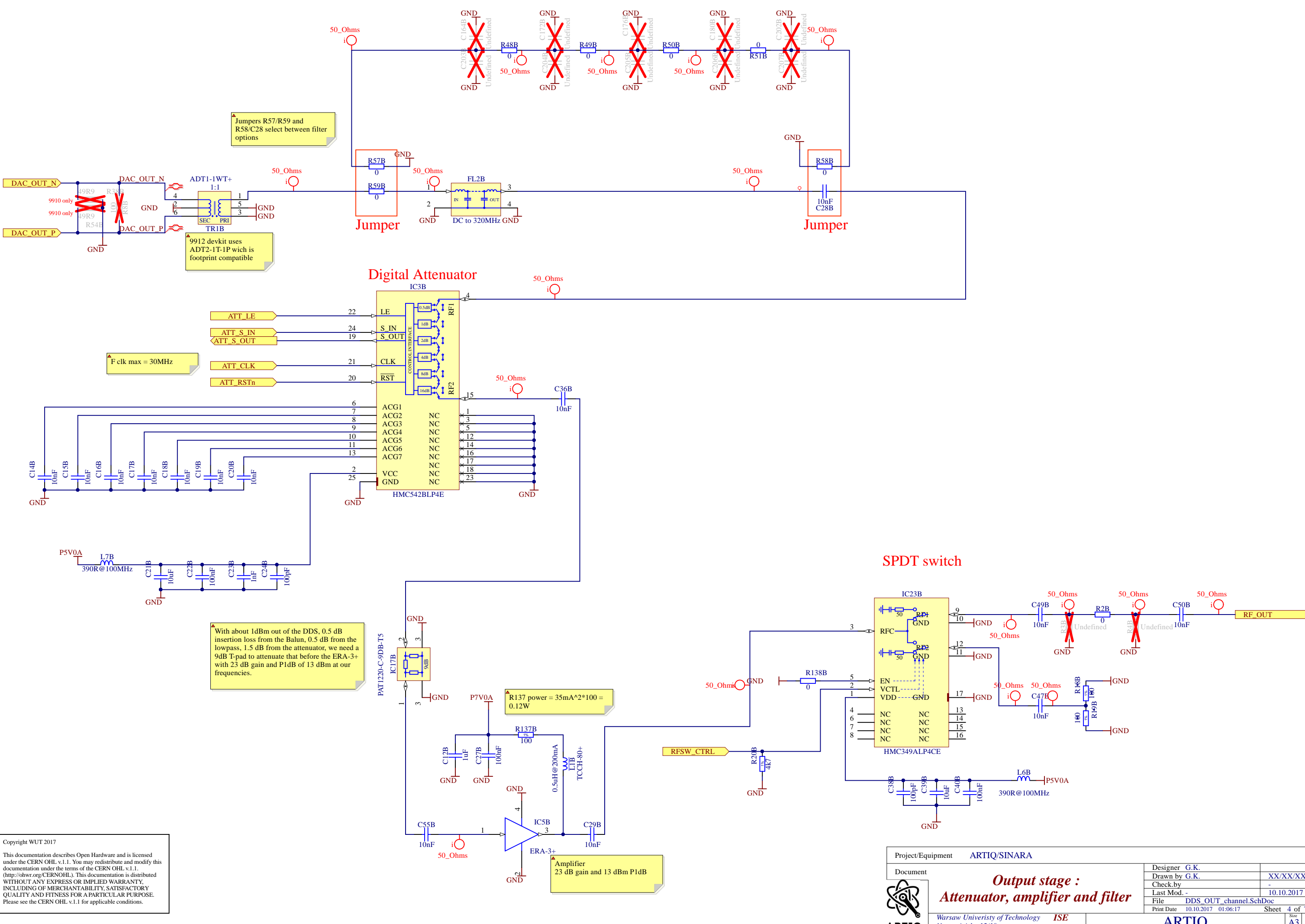


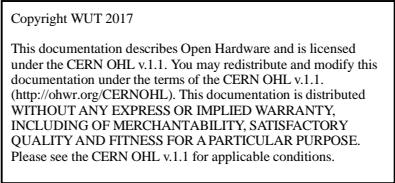
Project/Equipment		ARTIQ/SINARA	
Document		Designer	G.K.
 <div style="text-align: center;"> <p>Power supply</p> <p>DC/DC & LDOs</p> </div>		Drawn by	G.K.
		Check by	-
		Last Mod. -	10.10.2017
		File	Supply_DDS.SchDoc
		Print Date	10.10.2017 01:06:17
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		Sheet	3 of 7
		Size	A3
		Rev	-

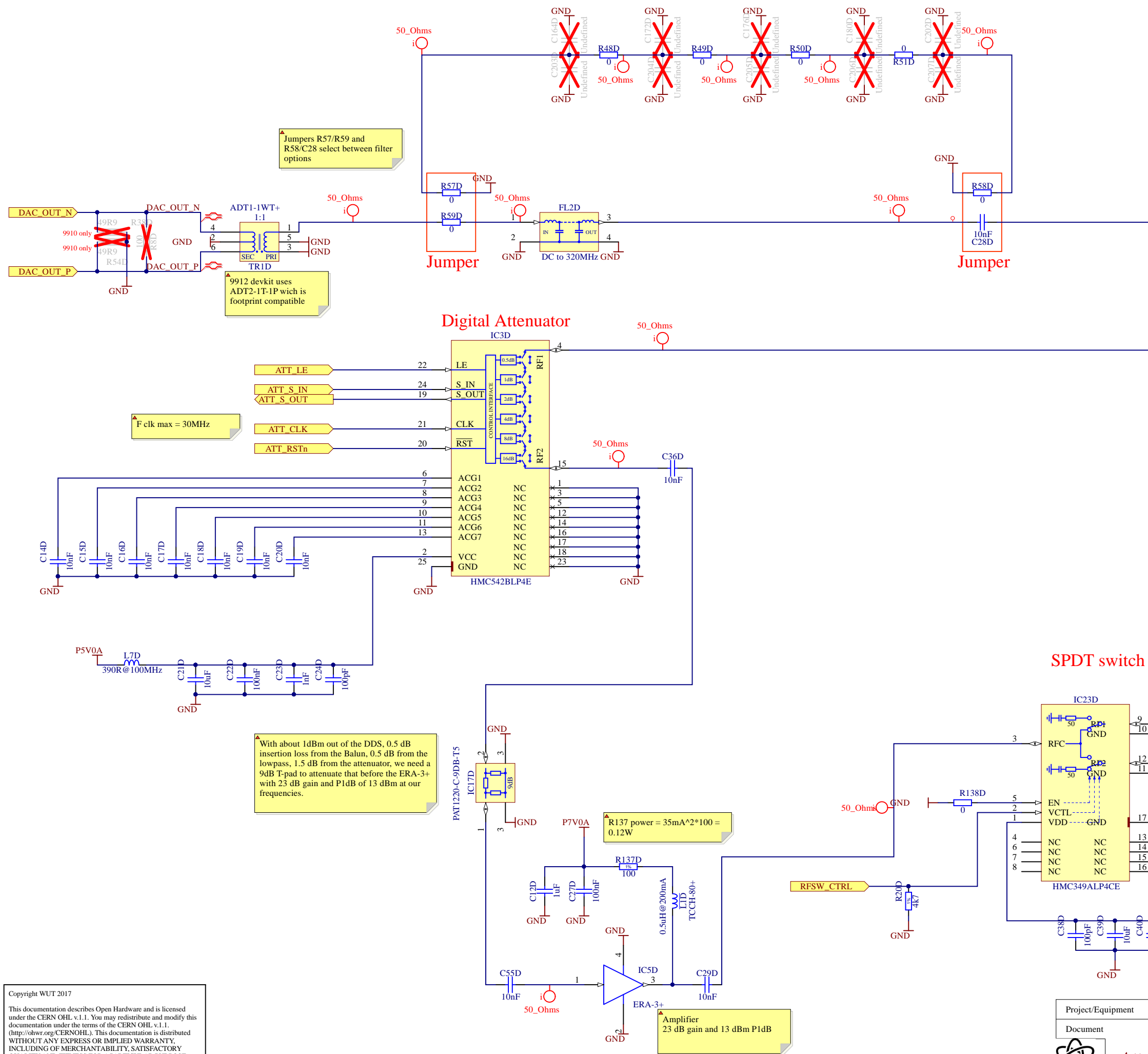


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Project/Equipment ARTIQ/SINARA

Document



Warsaw University of Technology ISE

Output stage :
Attenuator, amplifier and filter

Nowowiejska 15/19

Designer	G.K.	
Drawn by	G.K.	XX/XX/XXXX
Check by	-	
Last Mod.	-	10.10.2017
File	DDS_OUT_channel.SchDoc	
Print Date	10.10.2017 01:06:18	Sheet 4 of 7

ARTIQ

Size A3 Rev -

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Loop filter calculation:
Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20MHz
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

R=859R
Cs=522p
Cp=27p

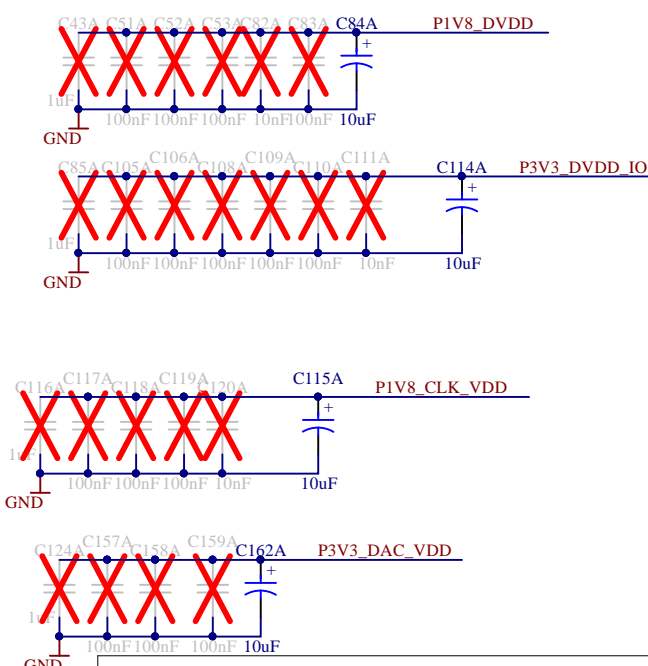
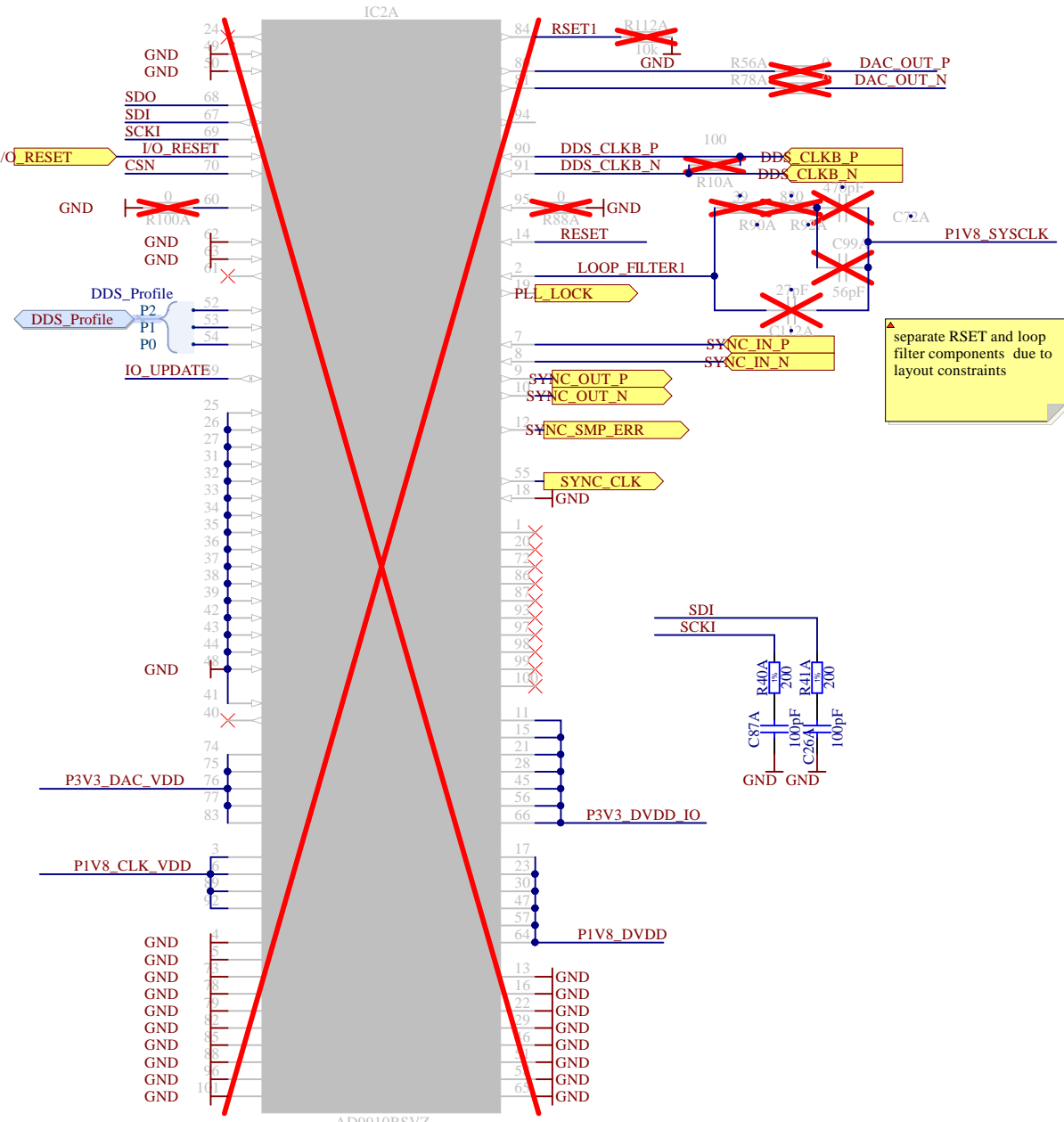
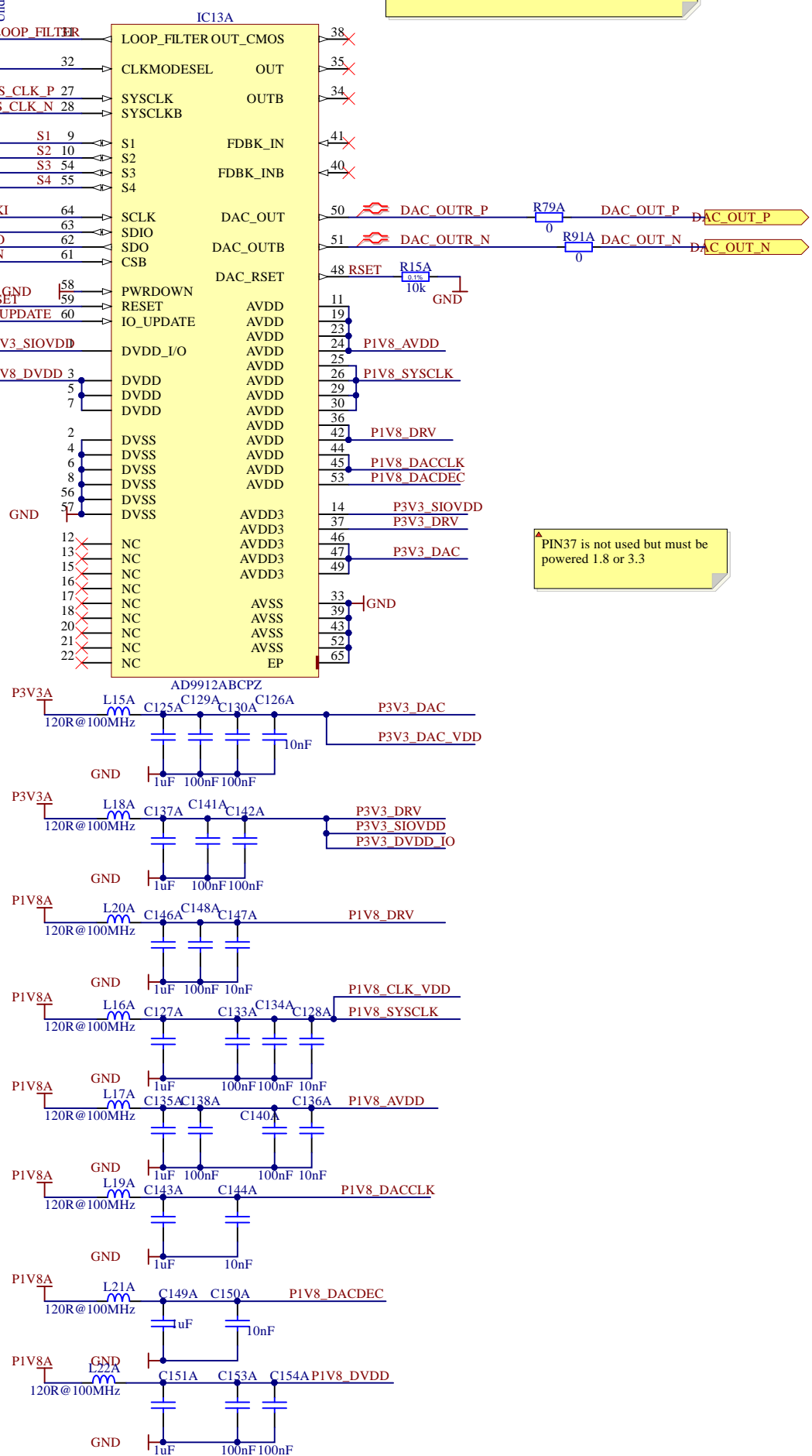
Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

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Project/Equipment		ARTIQ/SINARA	
Document		9910 & 9912 DDS	
Designer	G.K.	Check by	XX/XX/XXXX
Last Mod.	-	File	DDS_channel.SchDoc
Print Date	10.10.2017 01:06:19	Sheet	5 of 7
Warsaw University of Technology ISE		ARTIQ	
Nowowiejska 15/19		A3	

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Loop filter calculation:
Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20MHz
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

R=859R
Cs=522p
Cp=27p

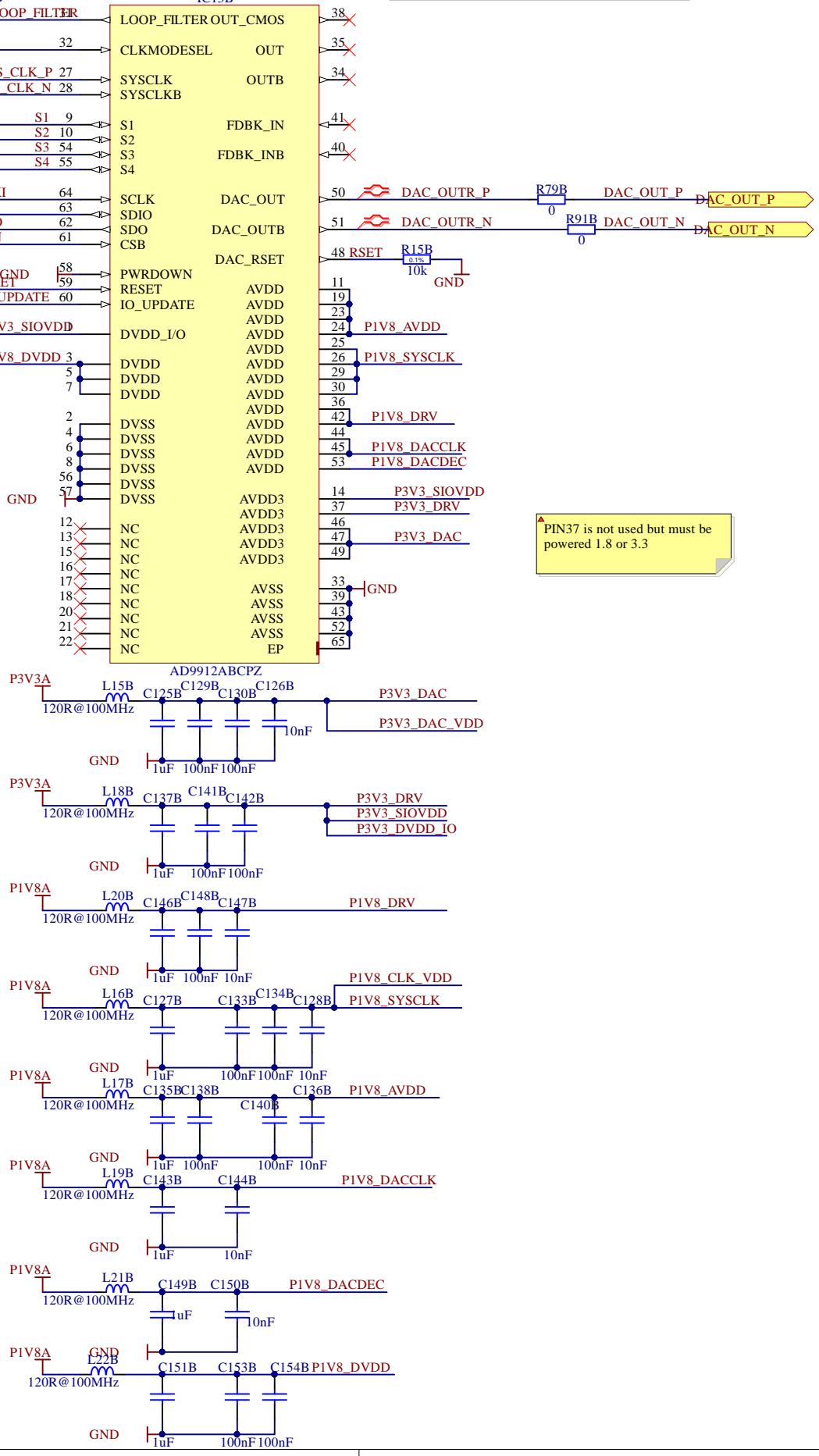
Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

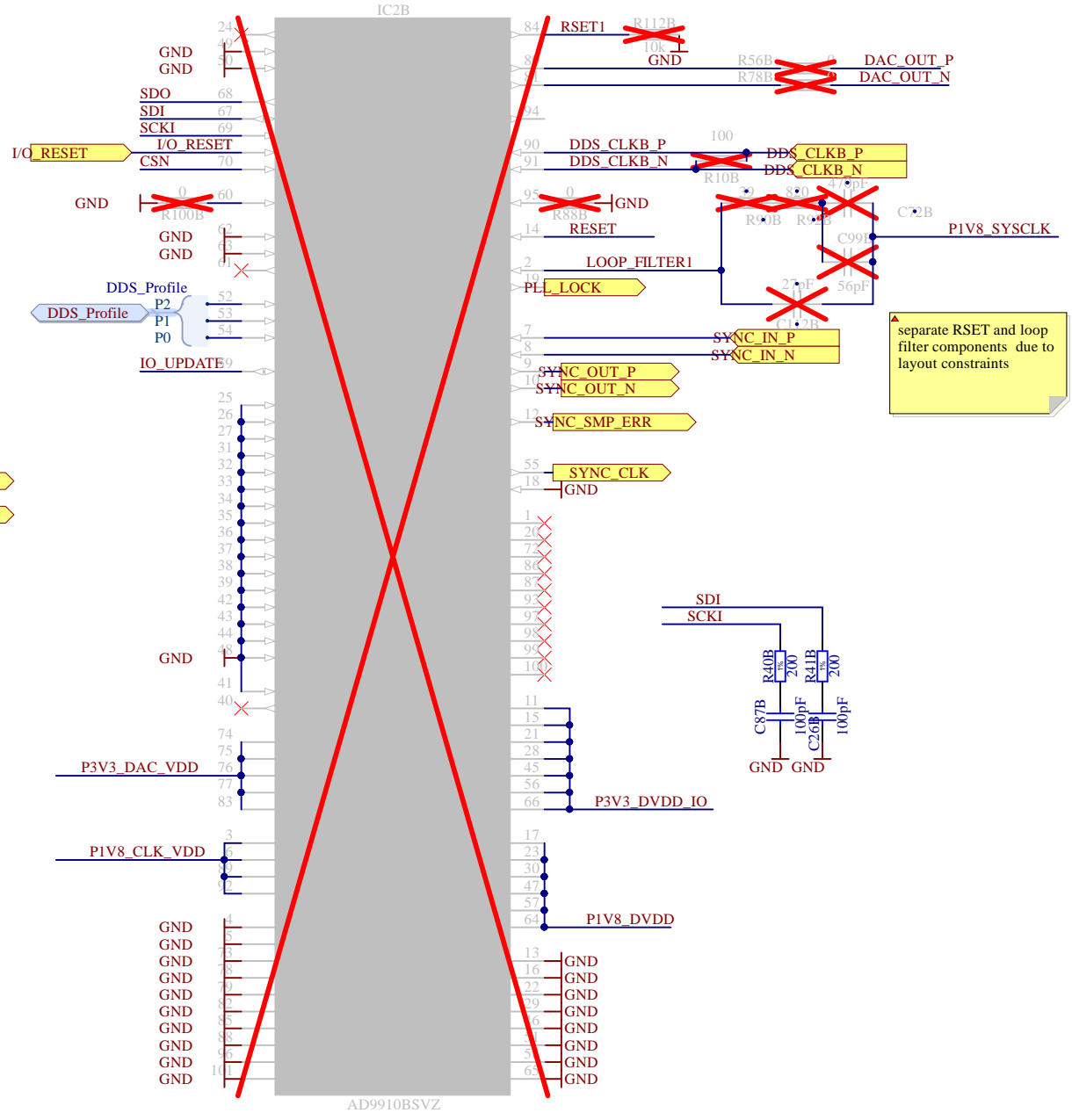
Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
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0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

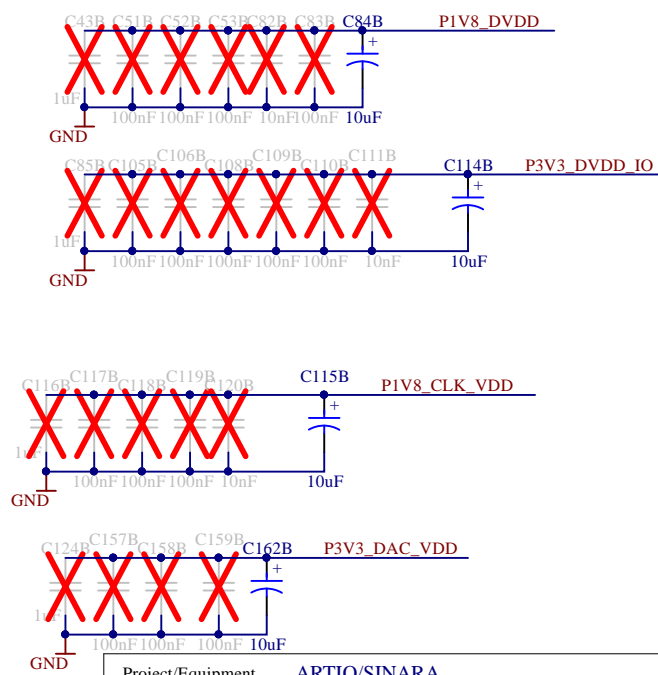
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PIN37 is not used but must be powered 1.8 or 3.3



separate RSET and loop filter components due to layout constraints



Project/EquipmentARTIQ/SINARA

Document

9910 & 9912 DDS

DesignerG.K.

Drawn byG.K.

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FileDDS_channel.SchDoc

Print Date10.10.2017 01:06:19

Sheet5 of 7

SizeA3

Rev-

Warsaw University of TechnologyISE

Nowowiejska 15/19

ARTIQ

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

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multiplication factor: 20MHz
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

R=859R
Cs=522p
Cp=27p

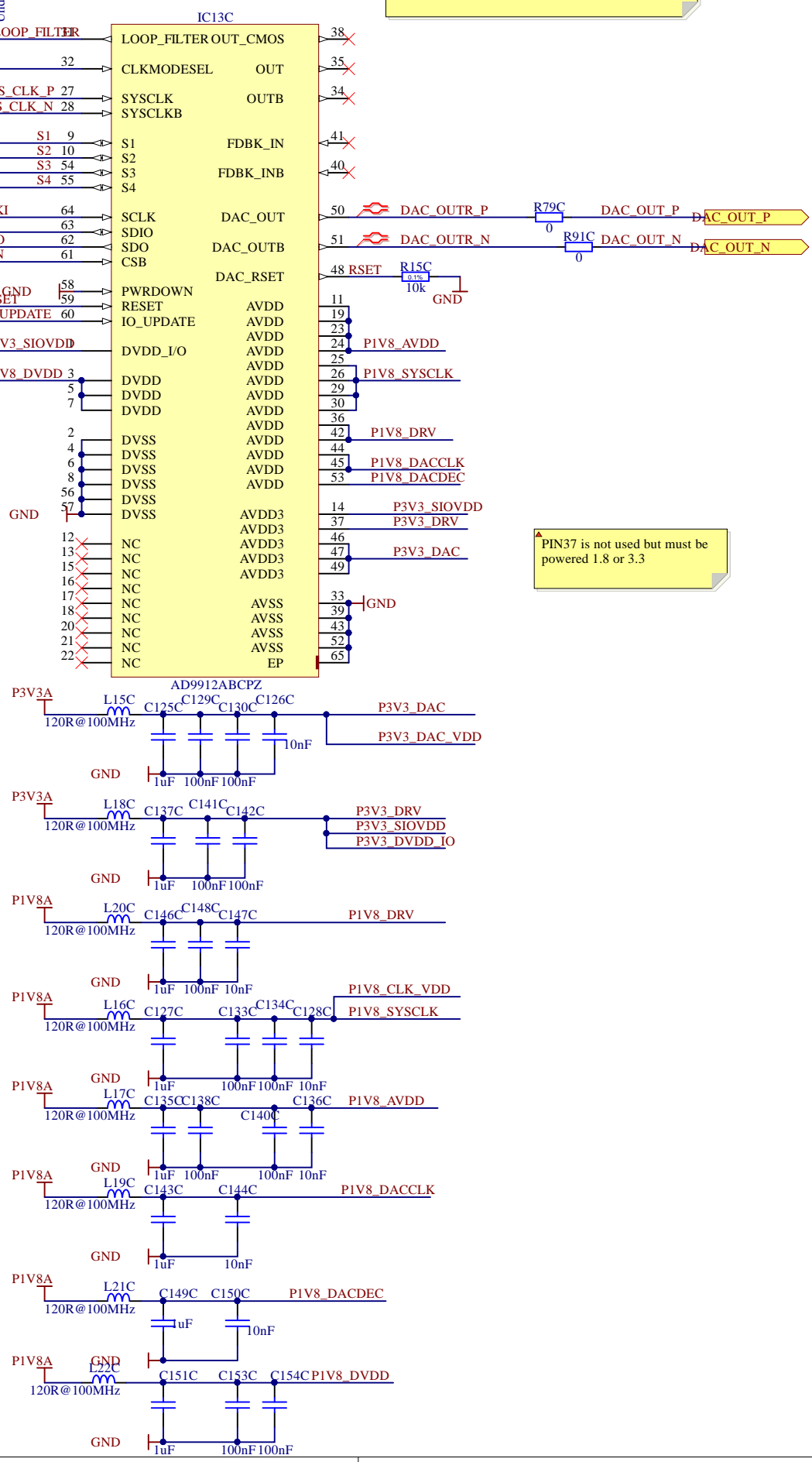
Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

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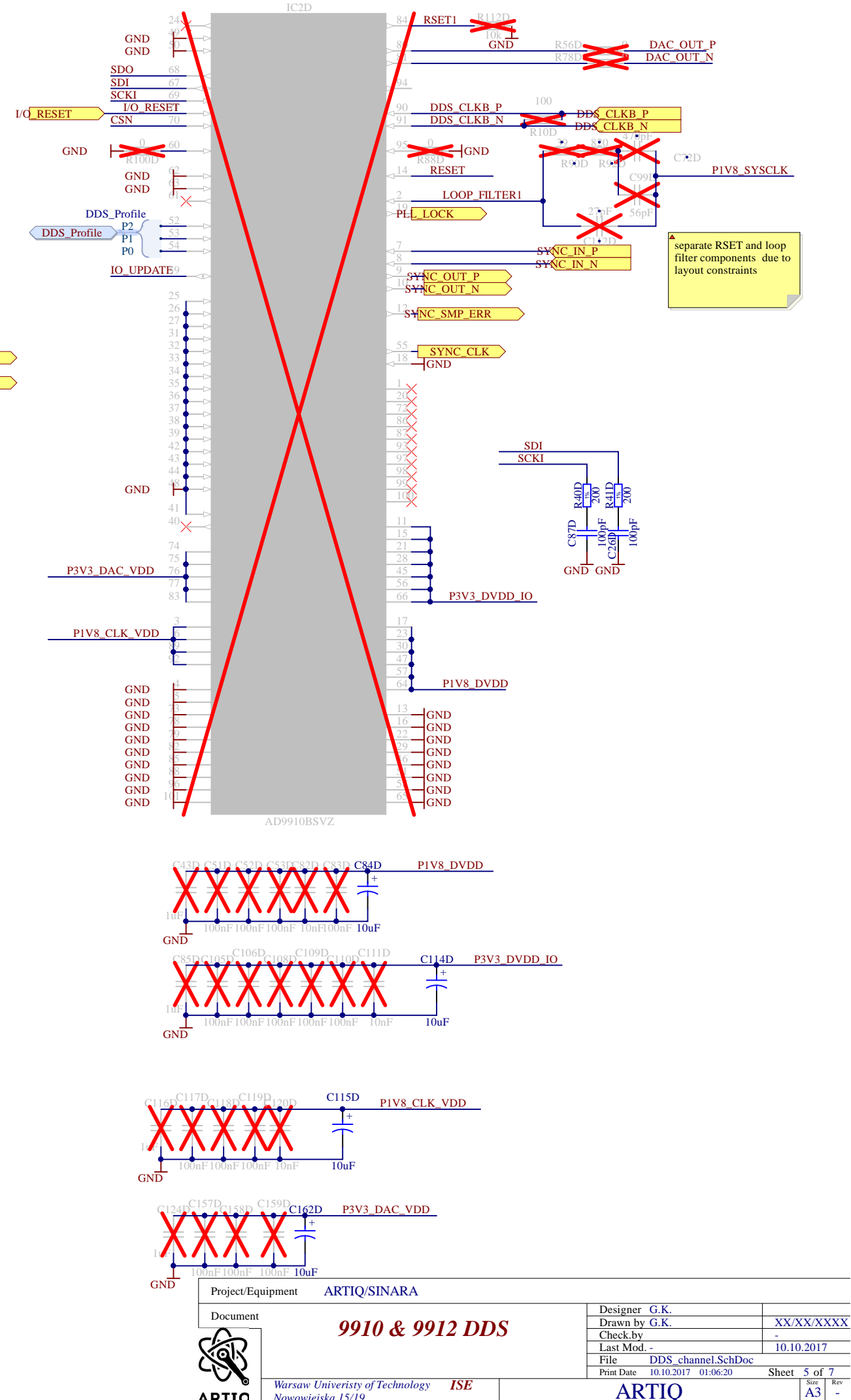
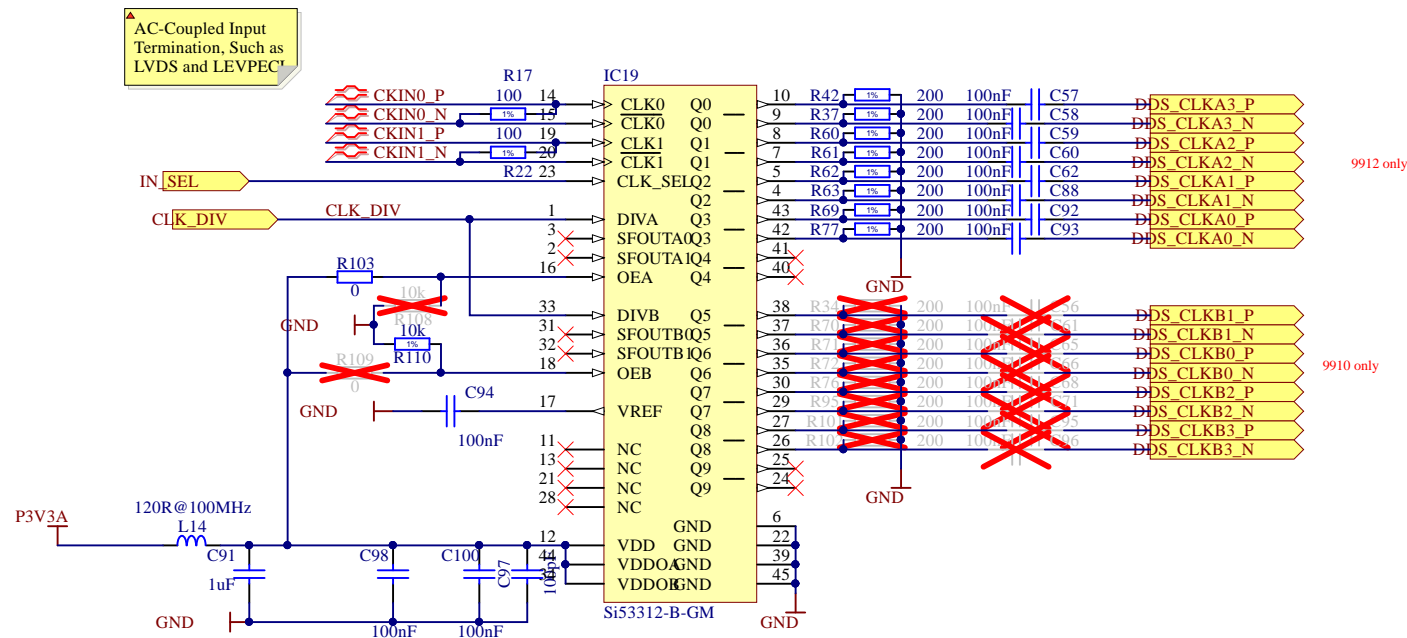
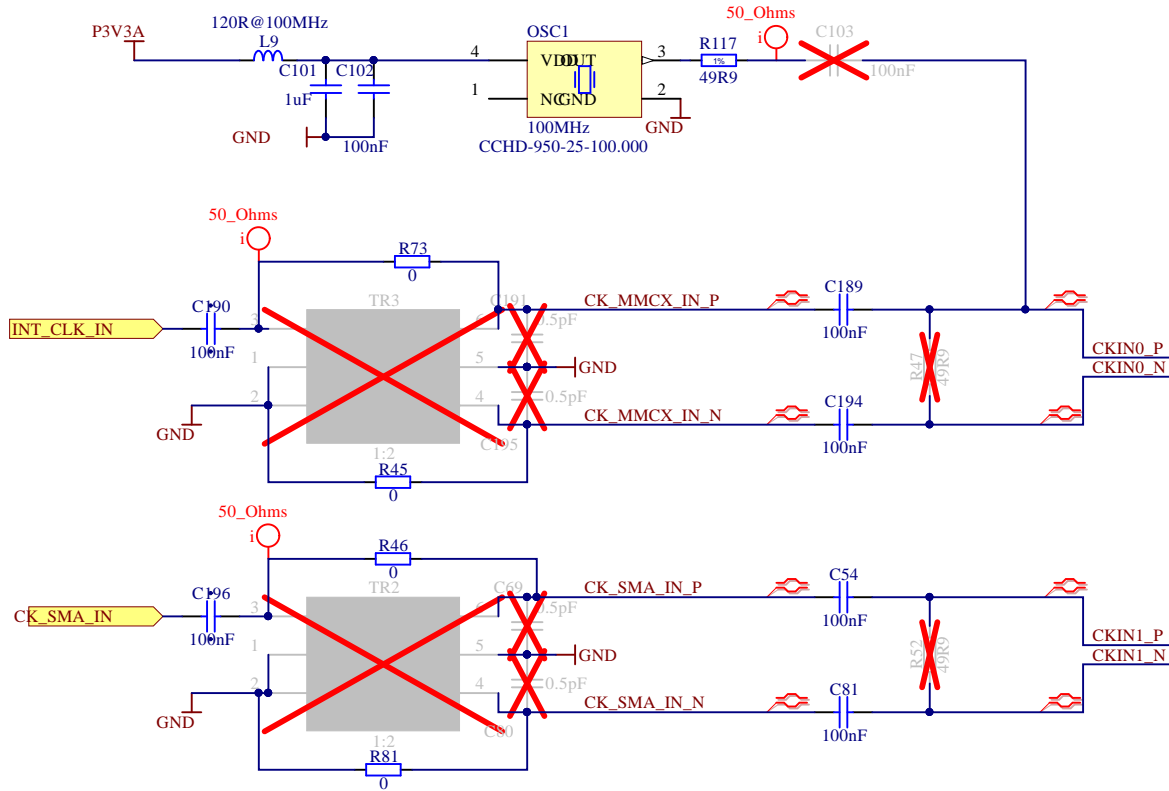


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSClk Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758


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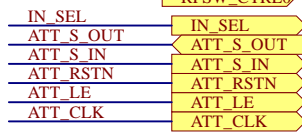
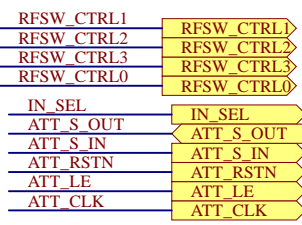
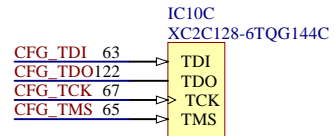
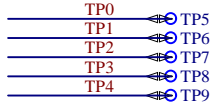
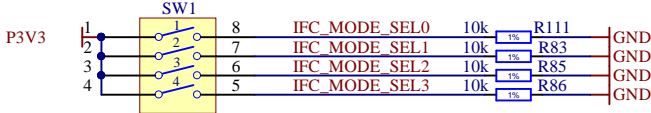
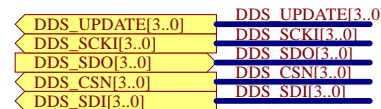
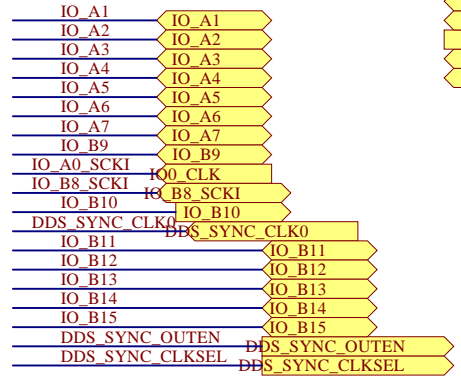
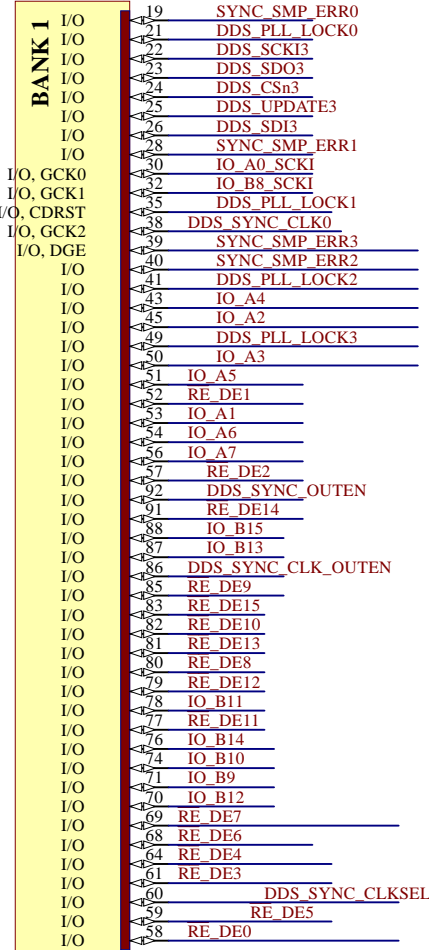


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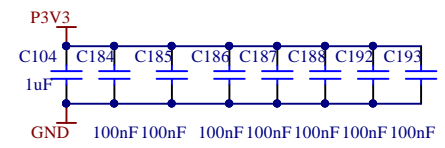
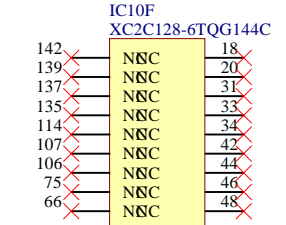
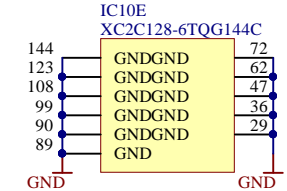
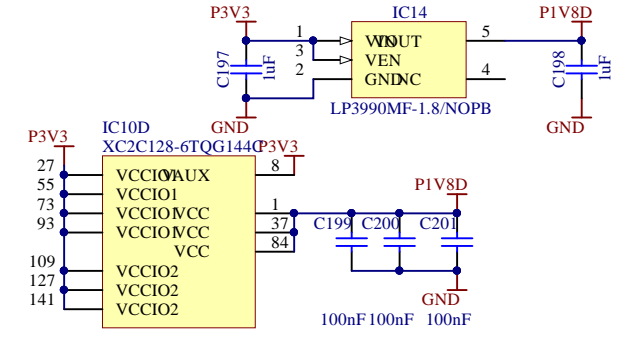
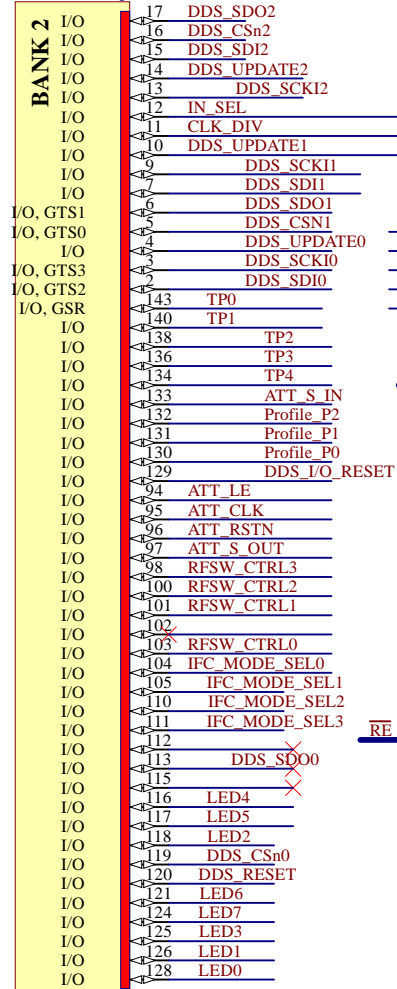
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Warsaw University of Technology ISE		ARTIQ	Size A3 Rev -

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IC10B
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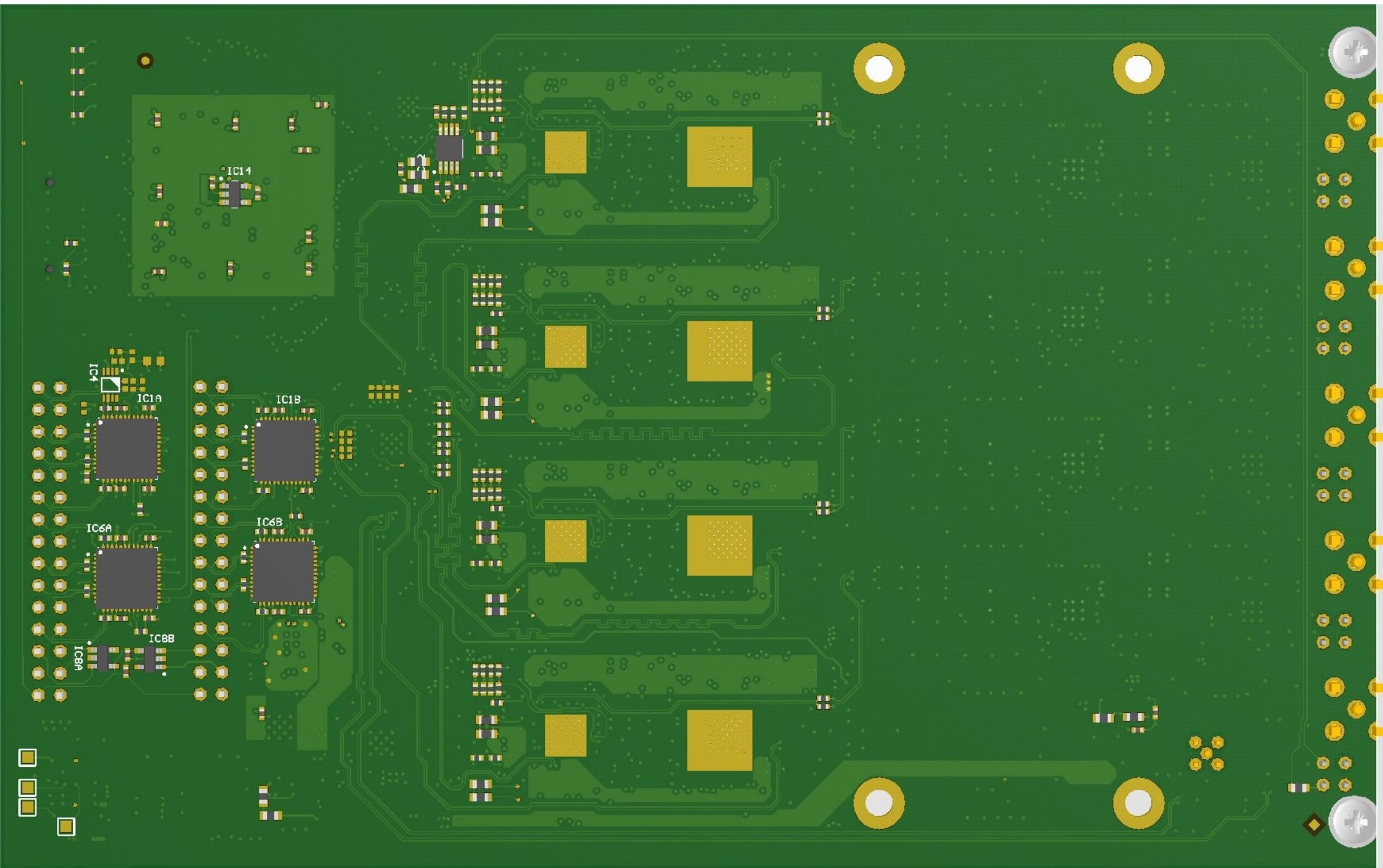


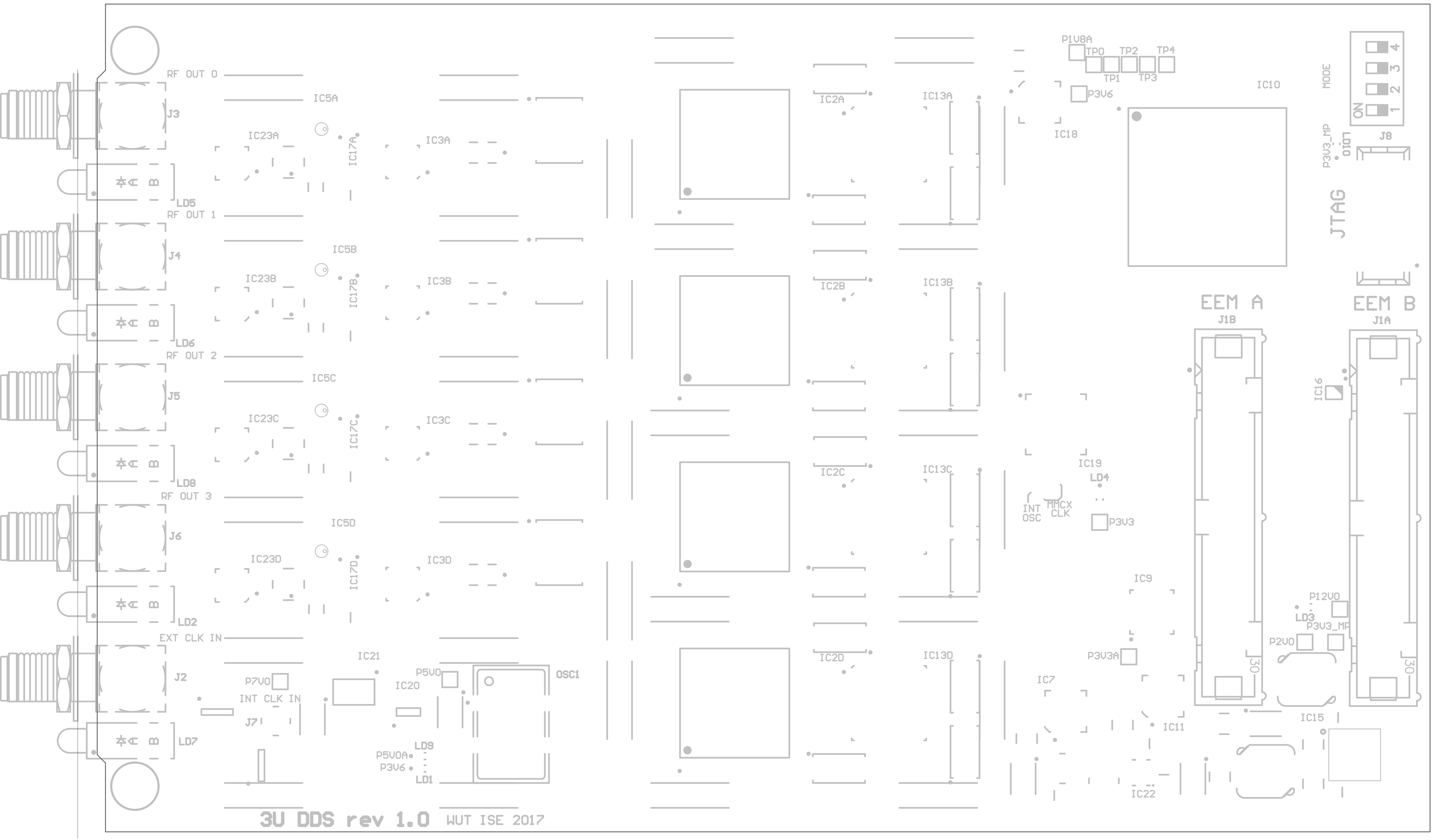
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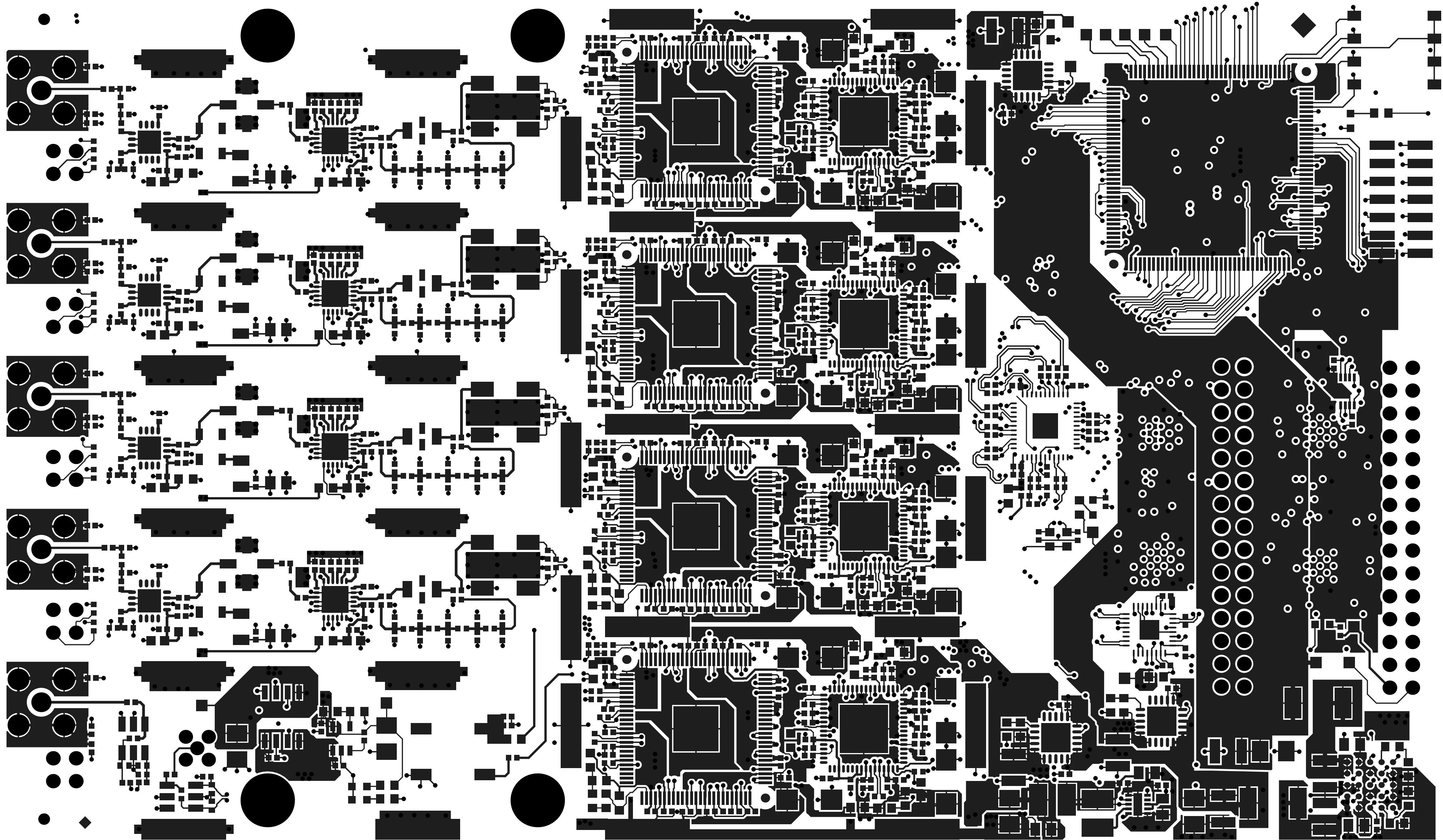
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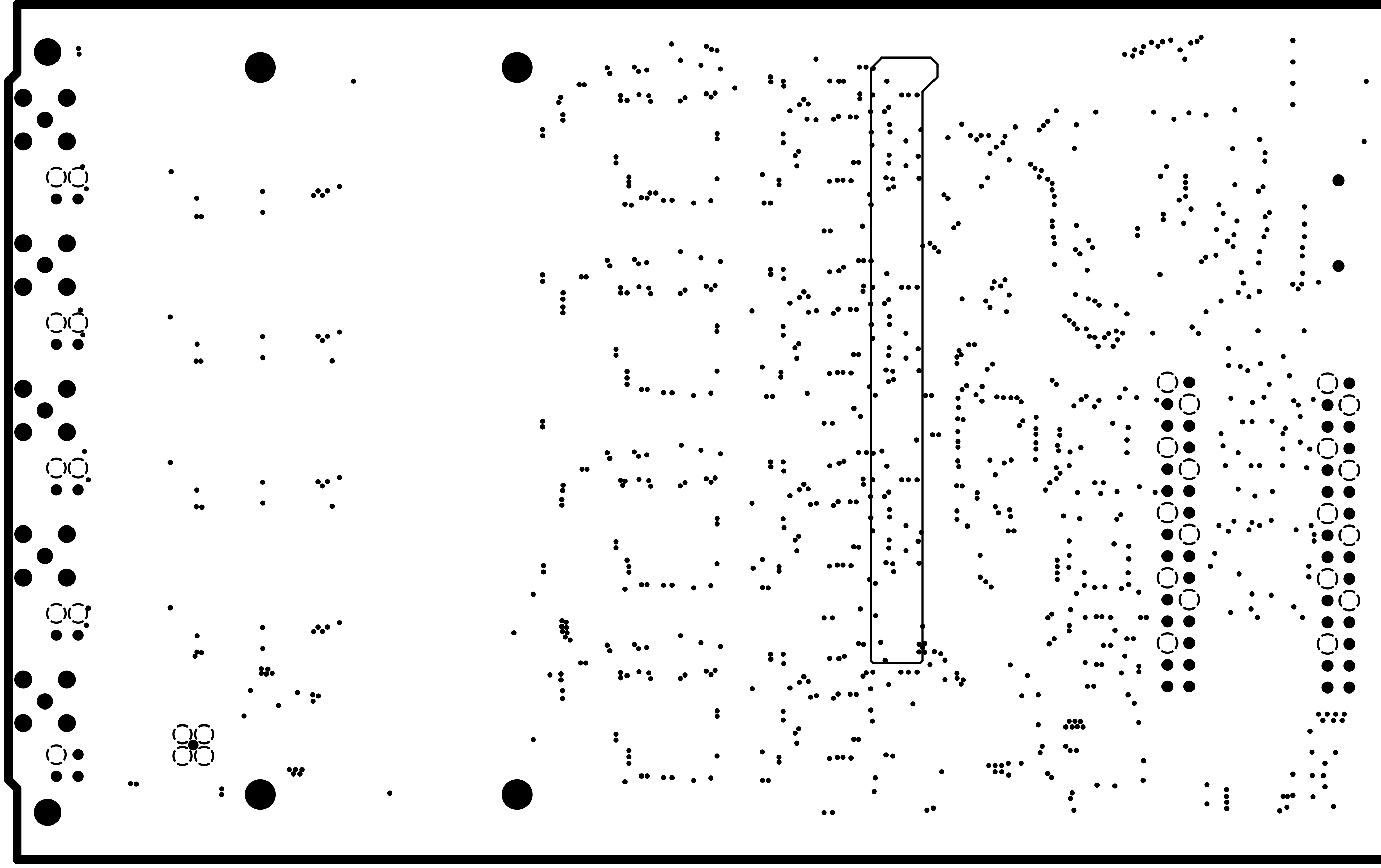
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Warsaw University of Technology		ISE	Rev
Nowowiejska 15/19		ARTIQ	
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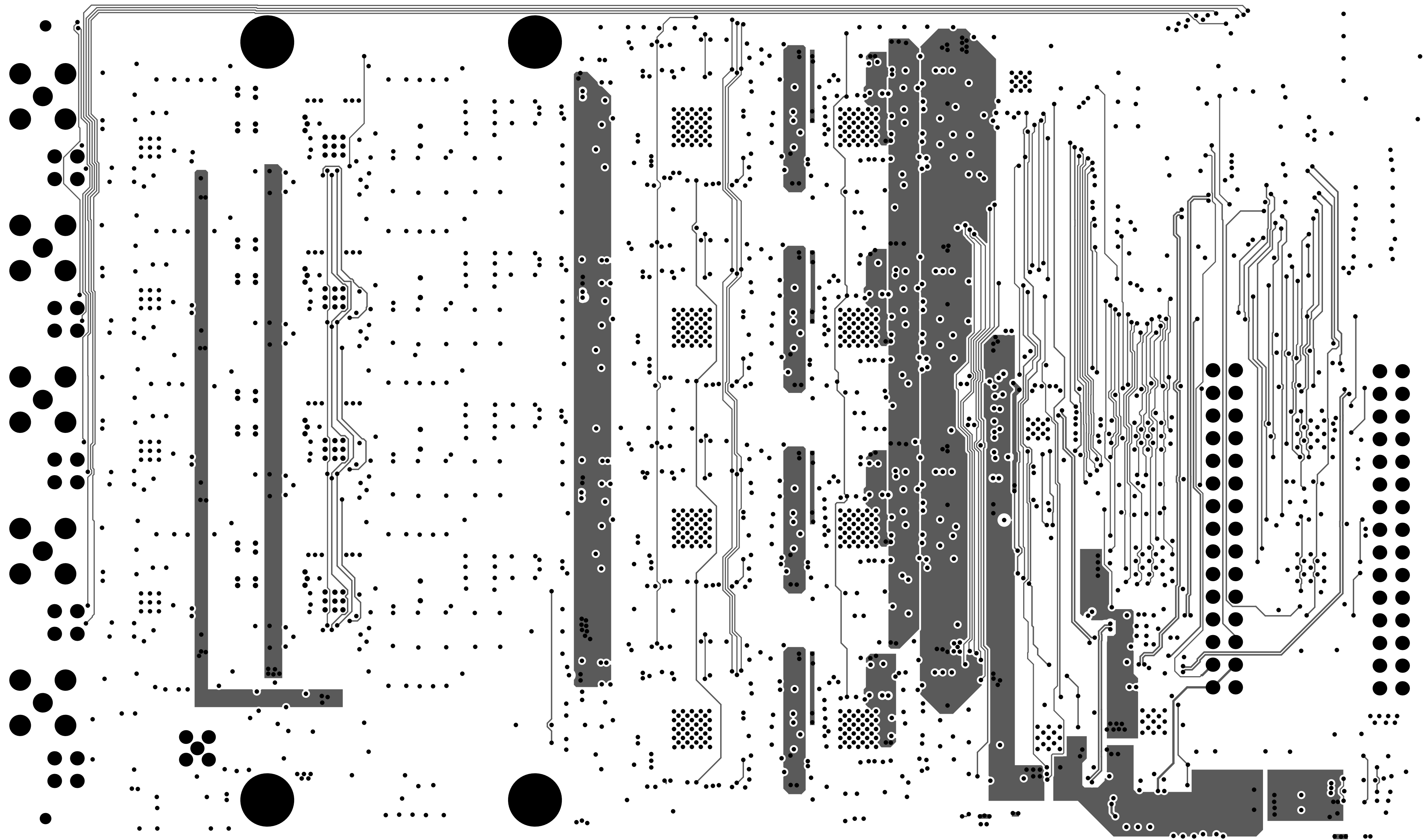


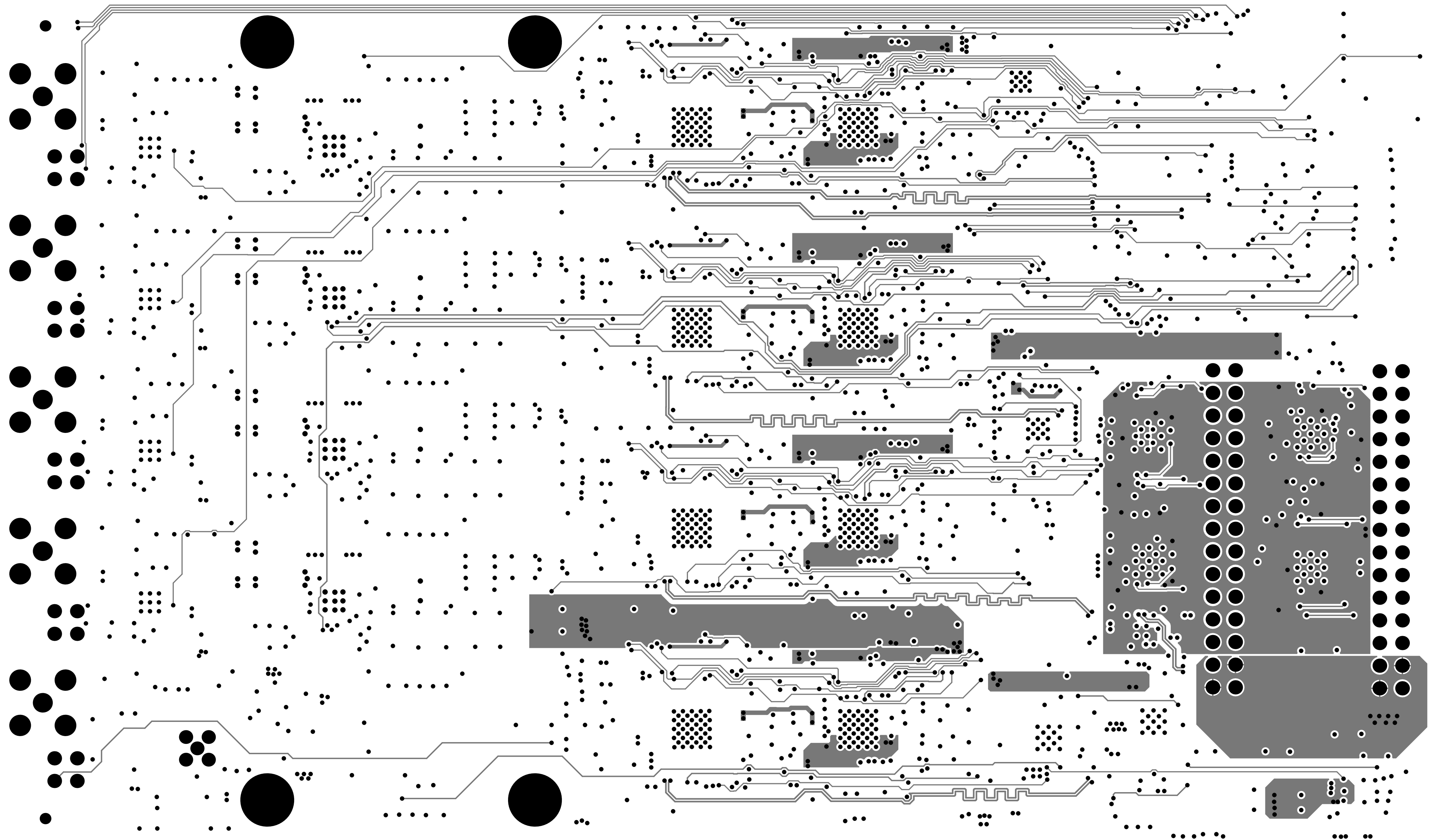


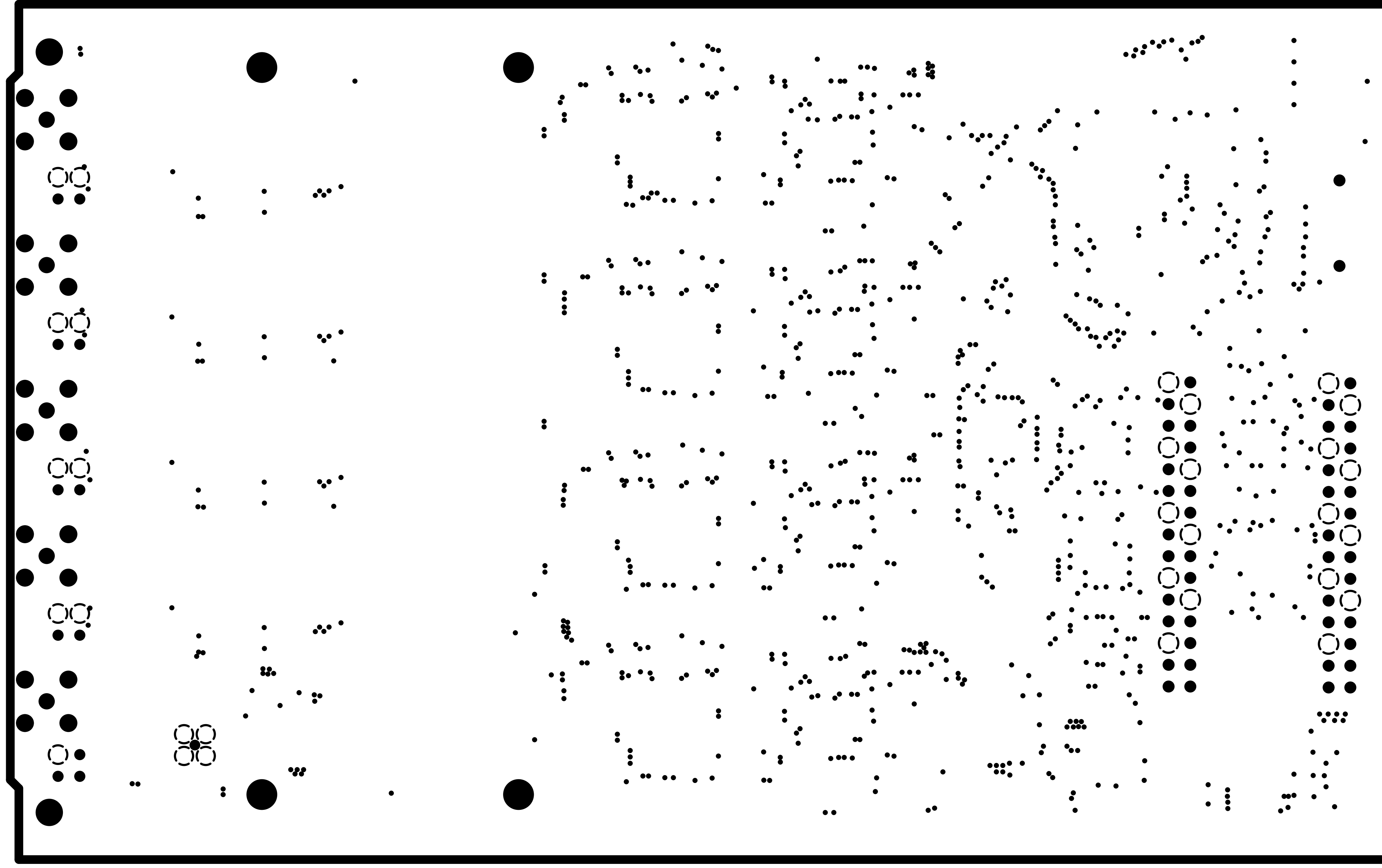


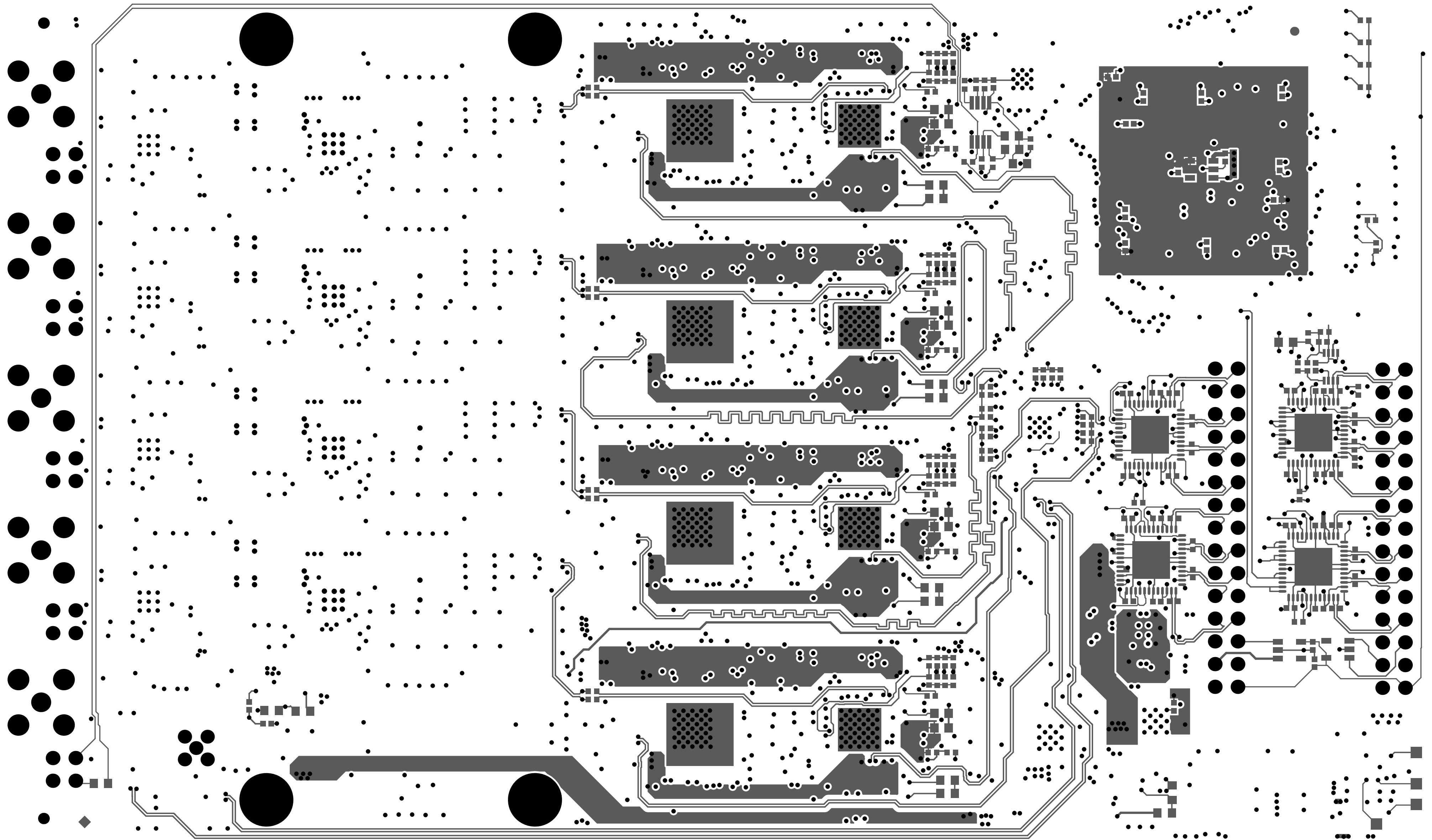














ICI⁴

IC9A

ICI⁸

ICI⁸



ICI^{8B}

ICI⁴



ICI⁸

IC9B



ICI⁵