shield clips

CLIP1 CLIP2 CLIP3 CLIP4 CLIP5
CLIP6 CLIP7 CLIP8 CLIP9 CLIP10 CLIP27
CLIP11 CLIP12 CLIP13 CLIP14 CLIP15 CLIP28
CLIP16 CLIP17 CLIP18 CLIP19 CLIP20 CLIP29
CLIP21 CLIP22 CLIP23 CLIP24 CLIP25 CLIP26
(all GND)

Ext clock input

Clock from Kasli

Output SMAs

GND — 10nF C37 — 10nF C42 — GND
GND — 0 R6
J2 SMA — 50_Ohms
J7 MMCX — GND

U_CLK_INPUT
CLK_INPUT.SchDoc

IN_SEL
CLK_DIV

CK_SMA_IN
IN_SEL
CLK_DIV
INT_CLK_IN

DDS_CLKA0_P DDS_CLKA0_N DDS_CLKA1_P DDS_CLKA1_N DDS_CLKA2_P DDS_CLKA2_N DDS_CLKA3_P DDS_CLKA3_N DDS_CLKB0_P DDS_CLKB0_N DDS_CLKB1_P DDS_CLKB1_N DDS_CLKB2_P DDS_CLKB2_N DDS_CLKB3_P DDS_CLKB3_N

GND — 10nF C11 — 0 R64 — 10nF C25 — GND
J3 SMA — RF_OUT0 — 50_Ohms
GND — 10nF C31 — 0 R65 — 10nF C32 — GND
J4 SMA — RF_OUT1 — 50_Ohms
GND — 10nF C33 — 0 R74 — 10nF C34 — GND
J5 SMA — RF_OUT2 — 50_Ohms
GND — 10nF C35 — 0 R75 — 10nF C41 — GND
J6 SMA — RF_OUT3 — 50_Ohms

ATT_CLK
ATT_LE
ATT_RSTn
ATT_S_IN
ATT_S_OUT

U_DDS_OUT_channel0
DDS_OUT_channel.SchDoc
U_DDS_OUT_channel1
DDS_OUT_channel.SchDoc
U_DDS_OUT_channel2
DDS_OUT_channel.SchDoc
U_DDS_OUT_channel3
DDS_OUT_channel.SchDoc

DAC_OUT_P DAC_OUT_N RF_OUT ATT_CLK RFSW_CTRL ATT_LE ATT_RSTn ATT_S_IN ATT_S_OUT

RFSW_CTRL0
RFSW_CTRL1
RFSW_CTRL2
RFSW_CTRL3

U_CTRL_LOGIC
CTRL_LOGIC.SchDoc

RFSW_CTRL0 RFSW_CTRL1 RFSW_CTRL2 RFSW_CTRL3
DDS_SDO[3..0] DDS_SDI[3..0] DDS_SCKI[3..0] DDS_CSn[3..0] IN_SEL CLK_DIV DDS_UPDATE[3..0] DDS_SYNC_CLK0 DDS_PLL_LOCK[3..0] SYNC_SMP_ERR[3..0] DDS_Profile DDS_I/O_RESET DDS_RESET LED[7..0] ATT_CLK ATT_LE ATT_RSTn ATT_S_IN ATT_S_OUT
RE_DE[15..0]
IO0_SCKI IO1 IO2 IO3 IO4 IO5 IO6 IO7 IO8_CLK IO9 IO10 IO11 IO12 IO13 IO14 IO15
DDS_SYNC_CLKSEL DDS_SYNC_OUTEN DDS_SYNC_CLK_OUTEN

RE_DE[15..0]

LVDS_IFC_DDS.SchDoc U_LVDS_IFC
EEM A
IO0 IO1 IO2 IO3 IO4 IO5 IO6 IO7 LVDS0_P LVDS0_N LVDS1_P LVDS1_N LVDS7_P LVDS7_N
I2C_SDA I2C_SCL
RE_DE0 RE_DE1 RE_DE2 RE_DE3 RE_DE4 RE_DE5 RE_DE6 RE_DE7

LVDS_IFC_DDS.SchDoc U_LVDS_IFC
EEM B
IO0 IO1 IO2 IO3 IO4 IO5 IO6 IO7 LVDS0_P LVDS0_N LVDS1_P LVDS1_N LVDS7_P LVDS7_N
I2C_SDA I2C_SCL
RE_DE0 RE_DE1 RE_DE2 RE_DE3 RE_DE4 RE_DE5 RE_DE6 RE_DE7
RE_DE8 RE_DE9 RE_DE10 RE_DE11 RE_DE12 RE_DE13 RE_DE14 RE_DE15

DDS_SYNC_CLKSEL
DDS_SYNC_OUTEN

PLACE IT CLOSE TO LVDS Rx/Tx

DDS_SYNC_CLK0 — 1k R31 — 100 R32 — P3V3_CLK1
P3V3_CLK1 — 220 R36 — 220 R39 — GND
C1 100n — GND
C13 100n — GND
IC4 FIN1101K8X
GND GND

PLACE IT CLOSE TO LVDS Rx/Tx

DDS0_SYNC_OUT_P — 100 R68 — DDS0_SYNC_OUT_N
IC9
DDS0_SYNC_IN_P DDS0_SYNC_IN_N DDS1_SYNC_IN_P DDS1_SYNC_IN_N DDS2_SYNC_IN_P DDS2_SYNC_IN_N DDS3_SYNC_IN_P DDS3_SYNC_IN_N
GND GND P3V3_CLK1 GND GND P3V3_CLK1 GND GND
Si53304-B-GM
120R@100MHz L13 — P3V3 — P3V3_CLK1
C86 1uF C87 100nF C88 100nF
GND

IC16 FIN1101K8X
P3V3_CLK1 — C46 100n — GND

LED0 R25 1% 470 LD2A BOT Green
LED1 R26 1% 470 LD2B TOP Green
LED2 R27 1% 470 LD5A BOT Green
LED3 R28 1% 470 LD5B TOP Green
LED4 R29 1% 470 LD6A BOT Green
LED5 R30 1% 470 LD6B TOP Green
LED6 R43 1% 470 LD8A BOT Green
LED7 R44 1% 470 LD8B TOP Green
GND

When routing please do a reasonable (100ps) length match within each of DDS_SYNC_CLK[3:0], DDS_UPDATE[3:0], RFSW_CTRL[3:0], IO[15:11] (nominally the RFSW_CTRL lines), DDS[3:0]_SYNC_IN, DDS_RESET and a really good one on DDS_CLK[3:0]_[PN].

U_DDS_channel0
DDS_channel.SchDoc
U_DDS_channel1
DDS_channel.SchDoc
U_DDS_channel2
DDS_channel.SchDoc
U_DDS_channel3
DDS_channel.SchDoc

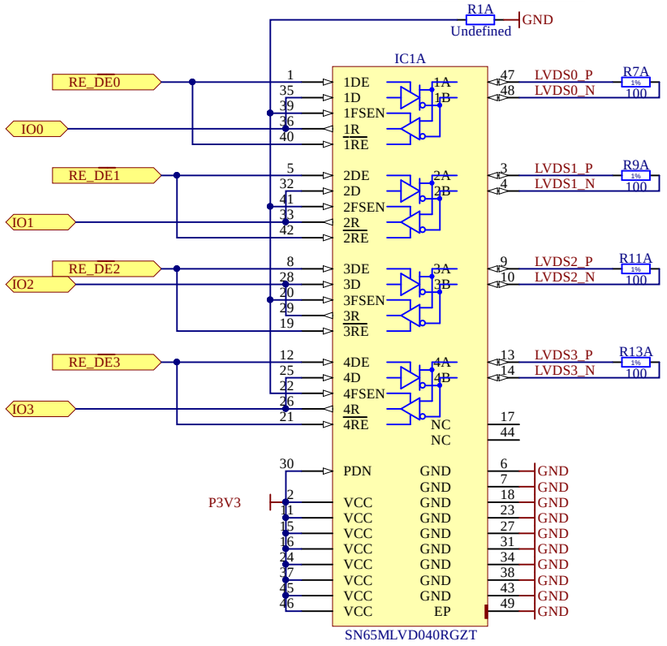
DAC_OUT_P DAC_OUT_N SYNC_OUT_P SYNC_OUT_N SYNC_CLK I/O_RESET RESET SYNC_IN_P SYNC_IN_N
SDO SDI SCKI CSN IO_UPDATE PLL_LOCK SYNC_SMP_ERR DDS_Profile DDS_CLKA_P DDS_CLKA_N DDS_CLKB_P DDS_CLKB_N

DDS_SDO0 DDS_SDI0 DDS_SCKI0 DDS_CSn0 DDS_UPDATE0 DDS_PLL_LOCK0 SYNC_SMP_ERR0 DDS_Profile DDS_CLKA0_P DDS_CLKA0_N DDS_CLKB0_P DDS_CLKB0_N
DDS_SDO1 DDS_SDI1 DDS_SCKI1 DDS_CSn1 DDS_UPDATE1 DDS_PLL_LOCK1 SYNC_SMP_ERR1 DDS_Profile DDS_CLKA1_P DDS_CLKA1_N DDS_CLKB1_P DDS_CLKB1_N
DDS_SDO2 DDS_SDI2 DDS_SCKI2 DDS_CSn2 DDS_UPDATE2 DDS_PLL_LOCK2 SYNC_SMP_ERR2 DDS_Profile DDS_CLKA2_P DDS_CLKA2_N DDS_CLKB2_P DDS_CLKB2_N
DDS_SDO3 DDS_SDI3 DDS_SCKI3 DDS_CSn3 DDS_UPDATE3 DDS_PLL_LOCK3 SYNC_SMP_ERR3 DDS_Profile DDS_CLKA3_P DDS_CLKA3_N DDS_CLKB3_P DDS_CLKB3_N

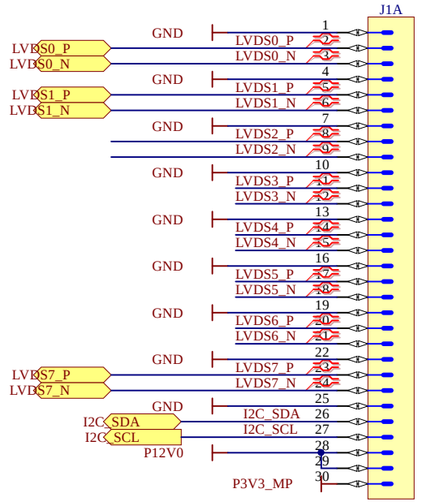
U_Supply_DDS
Supply_DDS.SchDoc
FTG1 FTG2 FTG3 FTG4

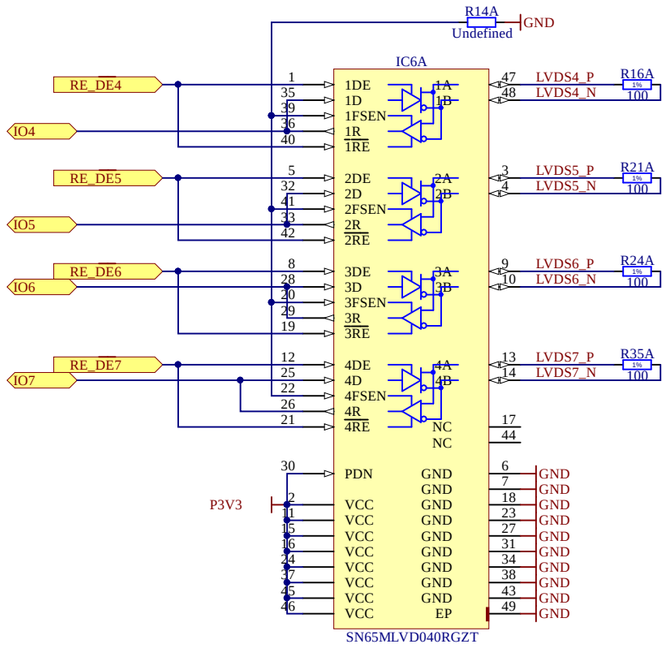
Project/Equipment	ARTIQ/SINARA		
Document	3U DDS (URUKUL) Top entity	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File PCB_3U_DDS.schdoc	
		Print Date 17.09.2017 22:43:33	Sheet 1 of 7
Warsaw Univeristy of Technology ISE Nowowiejska 15/19	ARTIQ	Size A3	Rev -

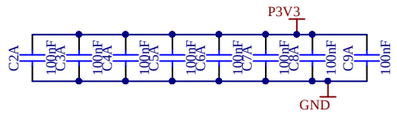
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

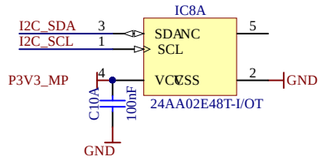


This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A



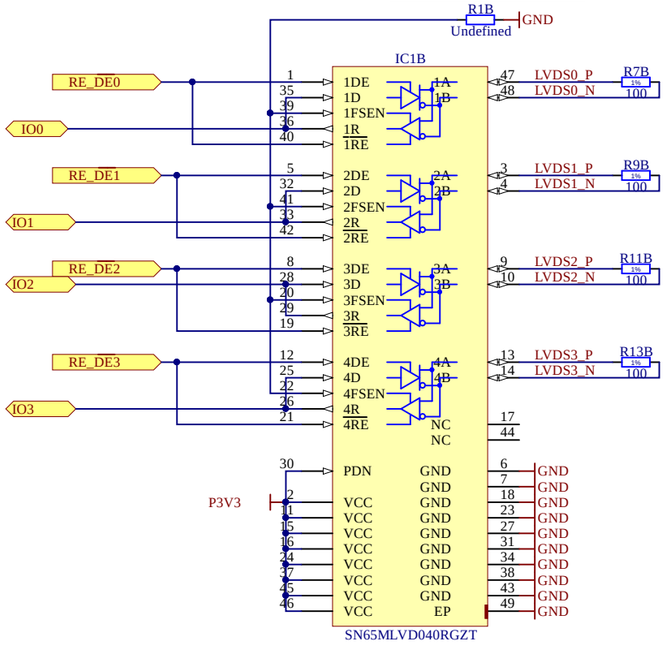




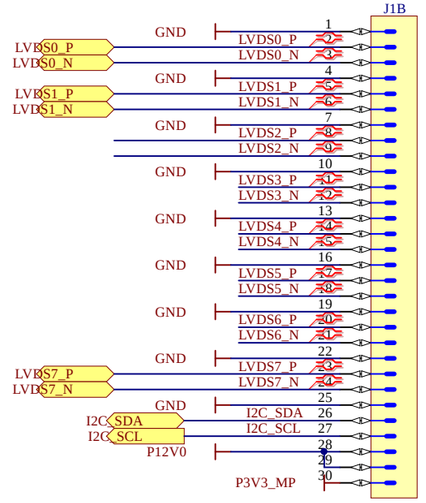


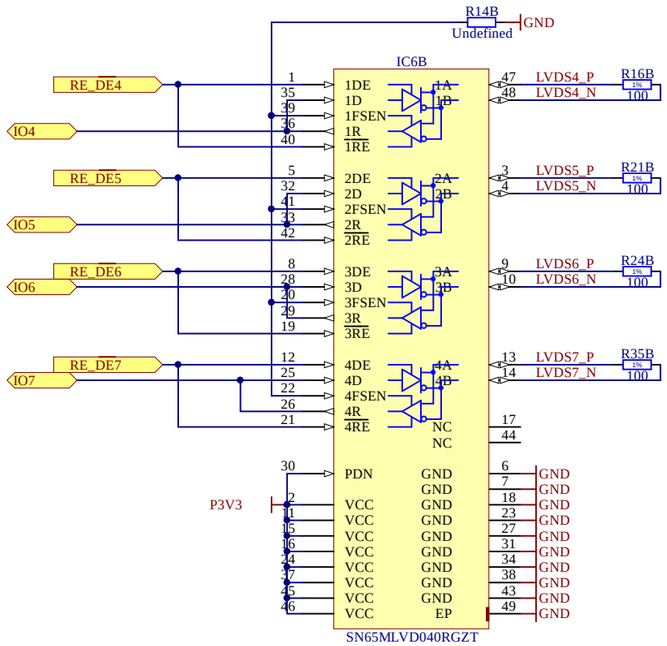
Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File LVDS_IFC_DDS.SchDoc	
		Print Date 17.09.2017 22:43:33	Sheet 2 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	*ISE*	ARTIQ	Size A3 / Rev -

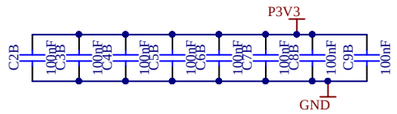
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

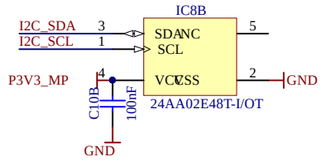


This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A

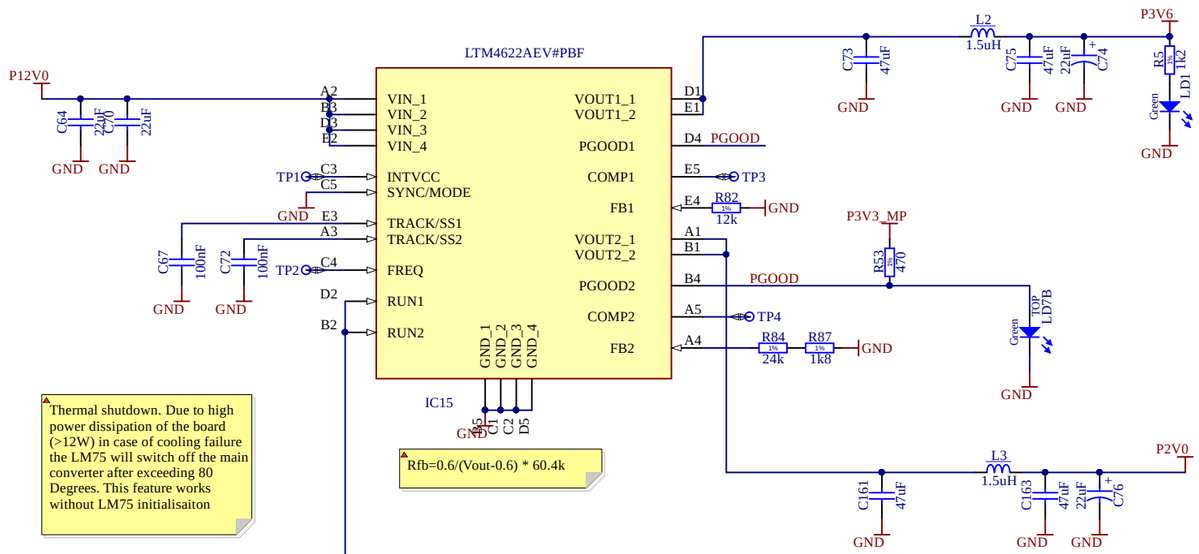


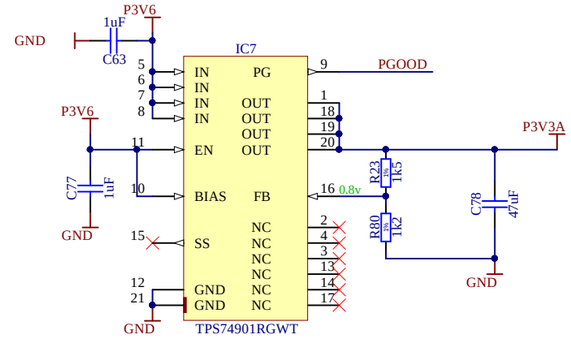


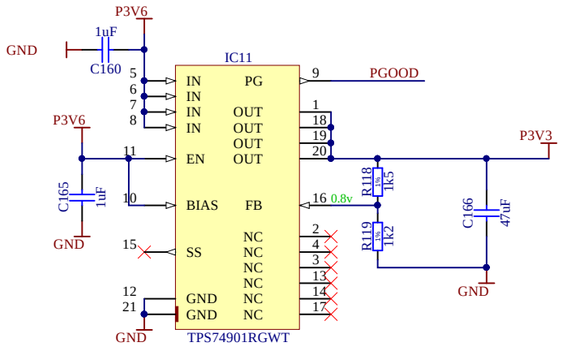


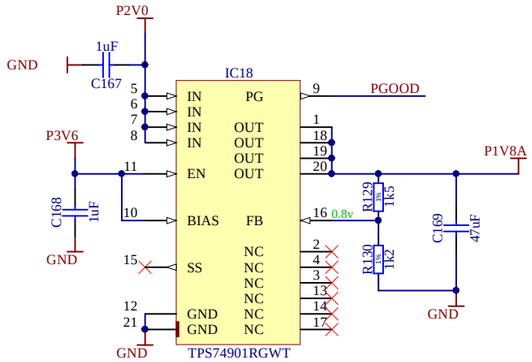


Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File LVDS_IFC_DDS.SchDoc	
		Print Date 17.09.2017 22:43:33	Sheet 2 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19 *ISE*	ARTIQ	Size A3	Rev -

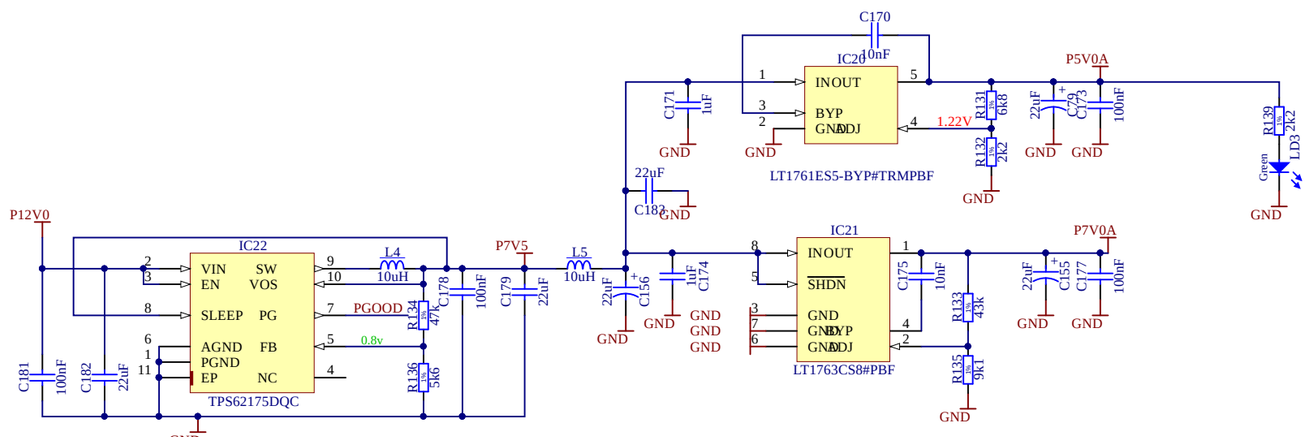








Power budget (max ratings):	AD9912 variant(mA)	AD9910 variant(mA)
P3V3:		
LVDS interface 4x	660	660
LVDS load 4x24mA	96	96
CPLD	100	100
ADCLK948	230	230
DDS AVDD3	4*(9,6+31)=133,6	4*29=116
DDS DVDDIO	4*3=12	4*11=44
TOTAL P3V3	1121	1146
TOTAL POWER	3.7	3.7
P1V8:		
DDS AVDD	4*(48+136)=736	4*110=440
DDS DVDD	4*246=984	4*222=888
TOTAL P1V8	1720	1328
TOTAL POWER	3,096	2.39
P5V0		
HMC542BLP4E	4*2.9=11.6	4*2.9=11.6
HMC349LP4C	4*3.5=14	4*3.5=14
TOTAL 5V0	25.6	25.6
TOTAL POWER	0,125	0,125
P7V0		
ERA-3XSM+	4*35=150	4*35=150
TOTAL POWER	1.05	1.05
DC/DC converter losses		
TPS62175 eff .95	0,05*(.27+0,026)*7,5=0.11	0,05*(.27+0,026)*7,5=0.11
LTM:3.6V eff .9	0.1*1,321*3,6=0,47	0,1*1,346*3,6=0,48
LTM:2V eff .87	0.13*1,721*2=0,44	0.13*1.328*2=0.34
LDO losses		
2V->1.8V	0.34	0,26
3.6V->3.3V	0.396	0.4
7.5V->7V	0,135	0,135
7.5V->5V	0,064	0,064
Total power from 12V	9.95W	9.05
Total current from 12V	0.83A	0.75A



Project/Equipment	ARTIQ/SINARA		
Document	**Power supply DC/DC & LDOs**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File Supply_DDS.SchDoc	
		Print Date 17.09.2017 22:43:34	Sheet 3 of 7
Warsaw Univeristy of Technology *Nowowiejska 15/19* *ISE*	ARTIQ	Size A3	Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

50_Ohms
C164A C203A R48A C172A C204A R49A C176A C205A R50A C180A C206A R51A C207A C209A 50_Ohms
0 0 0 0 0
Undefined

DAC_OUT_N
DAC_OUT_P
49R9 9910 only
R38A
R39A
GND
ADT1-1WT+ 1:1
TR1A
SEC PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible
50_Ohms
R57A R59A
Jumper
FL2A
IN OUT
DC to 320MHz
R58A C28A 10nF
Jumper
Digital Attenuator

F clk max = 30MHz
IC3A
ATT_LE ATT_S_IN ATT_S_OUT ATT_CLK ATT_RSTn
LE S_IN S_OUT CLK RST
CONTROL INTERFACE
0.5dB 1dB 2dB 4dB 8dB 16dB
RF1 RF2
ACG1 ACG2 ACG3 ACG4 ACG5 ACG6 ACG7
NC
VCC GND
HMC542BLP4E
C14A C15A C16A C17A C18A C19A C20A 10nF
C36A 10nF
GND

P5V0A L7A 390R@100MHz
C21A 10uF C22A 100nF C23A 1nF C24A 100pF

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

PAT1220-C-9DB-T5 IC17A 9dB
R5 power = 65mA^2*39 = 0.16W

P7V0A
R137A 100
C12A 1uF C27A 100nF
0.5uH@200mA L1A TCCH-80+
C55A 10nF
IC5A ERA-3+
C29A 10nF
R61A Undefined

SPDT switch
IC23A
RFC RD1 RD2 EN VCTL VDD
GND NC
HMC349ALP4CE
RFSW_CTRL
R20A 4k7
R138A 0
C49A C50A 10nF
R23A R24A Undefined
R2A 0
RF_OUT
C47A 10nF
R18A R19A 100
C38A 100pF C39A 10uF C40A 100nF
L6A 390R@100MHz

Amplifier
~23 gain and 13 dBm P1dB

Project/Equipment	ARTIQ/SINARA
Document	**Output stage : Attenuator, amplifier and filter**
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	DDS_OUT_channel.SchDoc
Print Date	17.09.2017 22:43:34 Sheet 4 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

50_Ohms
C164B Undefined
C203B Undefined
R48B 0
C172B Undefined
C204B Undefined
R49B 0
C176B Undefined
C205B Undefined
R50B 0
C180B Undefined
C206B Undefined
R51B 0
C202B Undefined
C207B Undefined
GND

DAC_OUT_N
DAC_OUT_P
49R9 9910 only
R38B 49R9
R39B 49R9
ADT1-1WT+ 1:1
TR1B
SEC PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible

R57B 0
R59B 0
Jumper
FL2B
DC to 320MHz
R58B 0
10nF C28B
Jumper

Digital Attenuator
F clk max = 30MHz

IC3B HMC542BLP4E
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB 1dB 2dB 4dB 8dB 16dB
RF1
RF2
ACG1 ACG2 ACG3 ACG4 ACG5 ACG6 ACG7
NC
VCC GND
C14B 10nF
C15B 10nF
C16B 10nF
C17B 10nF
C18B 10nF
C19B 10nF
C20B 10nF
C36B 10nF

P5V0A
L7B 390R@100MHz
C21B 10uF
C22B 100nF
C23B 1nF
C24B 100pF

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

PAT1220-C-9DB-T5
IC17B 9dB

R5 power = 65mA^2*39 = 0.16W

P7V0A
R137B 100
C12B 1uF
C27B 100nF
L1B 0.5uH@200mA TCCH-80+
C55B 10nF
IC5B ERA-3+
C29B 10nF
R54B Undefined

Amplifier
~23 dB gain and 13 dBm P1dB

SPDT switch
RFSW_CTRL
R20B 4k7
R138B 0
IC23B HMC349ALP4CE
RFC RD1 RD2 EN VCTL VDD GND NC
C38B 100pF
C39B 10uF
C40B 100nF
L6B 390R@100MHz
P5V0A

C49B 10nF
R2B 0
C50B 10nF
R2B Undefined
R4B Undefined
RF_OUT
C47B 10nF
R18B 100
R19B 100

Project/Equipment	ARTIQ/SINARA		
Document	**Output stage : Attenuator, amplifier and filter**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File DDS_OUT_channel.SchDoc	
		Print Date 17.09.2017 22:43:34	Sheet 4 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19 *ISE*	ARTIQ	Size A3	Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
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50_Ohms
C164C Undefined
R48C 0
C172C Undefined
R49C 0
C176C Undefined
R50C 0
C180C Undefined
R51C 0
C202C Undefined
C203C Undefined
C204C Undefined
C205C Undefined
C206C Undefined
C207C Undefined
GND

DAC_OUT_N
DAC_OUT_P
49R9 1% 9910 only
R38C 100
ADT1-1WT+ 1:1
TR1C
SEC PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible

R57C 0
R59C 0
Jumper
FL2C
IN OUT
DC to 320MHz
R58C 0
10nF C28C
Jumper

Digital Attenuator

F clk max = 30MHz

IC3C
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB 1dB 2dB 4dB 8dB 16dB
RF1
RF2
ACG1 ACG2 ACG3 ACG4 ACG5 ACG6 ACG7
NC
VCC GND
HMC542BLP4E
C14C 10nF
C15C 10nF
C16C 10nF
C17C 10nF
C18C 10nF
C19C 10nF
C20C 10nF
C36C 10nF

P5V0A
L7C 390R@100MHz
C21C 10uF
C22C 100nF
C23C 1nF
C24C 100pF

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

PAT1220-C-9DB-T5
IC17C 9dB

R5 power = 65mA^2*39 = 0.16W

P7V0A
R137C 100
C12C 1uF
C27C 100nF
L1TC TCCH-80+ 0.5uH@200mA
C55C 10nF
IC5C
ERA-3+
C29C 10nF
R39C Undefined

Amplifier
~23 dB gain and 13 dBm P1dB

SPDT switch

IC23C
RFC
RD1 RD2
EN VCTL VDD
NC
HMC349ALP4CE
RFSW_CTRL
R20C 4k7
R138C 0
C49C 10nF
R2C 0
C50C 10nF
RF_OUT
R2C Undefined
R4C Undefined
C47C 10nF
R18C 100
R19C 100
C38C 100pF
C39C 10uF
C40C 100nF
L6C 390R@100MHz

Project/Equipment	ARTIQ/SINARA		
Document	**Output stage : Attenuator, amplifier and filter**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File DDS_OUT_channel.SchDoc	
		Print Date 17.09.2017 22:43:34	Sheet 4 of 7
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One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

Digital Attenuator

F clk max = 30MHz

Jumper

Jumper

9912 devkit uses ADT2-1T-1P wich is footprint compatible

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R5 power = 65mA^2*39 = 0.16W

SPDT switch

Amplifier
~23 dB gain and 13 dBm P1dB

Project/Equipment	ARTIQ/SINARA		
Document	**Output stage : Attenuator, amplifier and filter**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
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		File DDS_OUT_channel.SchDoc	
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Warsaw Univeristy of Technology ISE *Nowowiejska 15/19*	ARTIQ	Size A3	Rev -

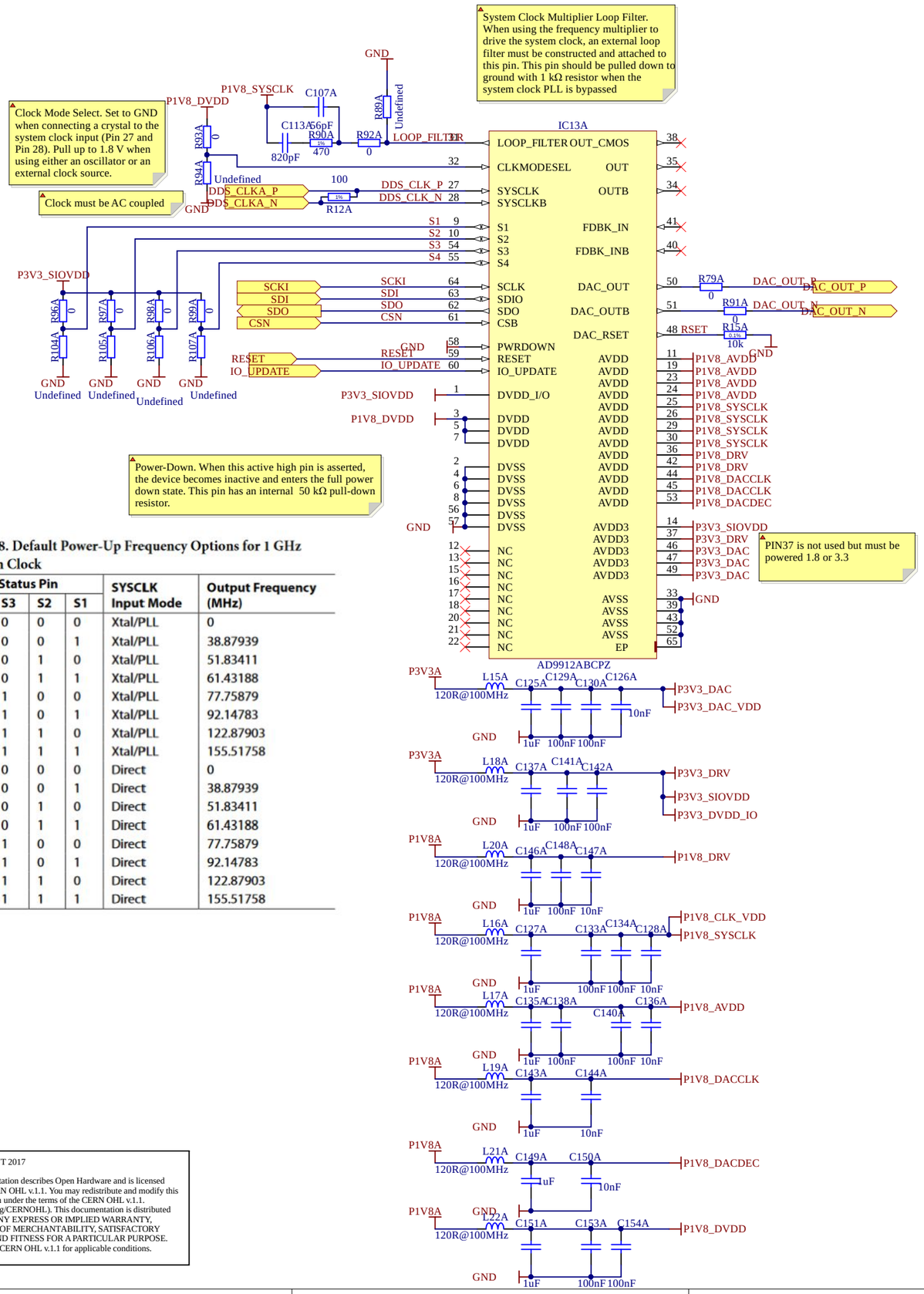
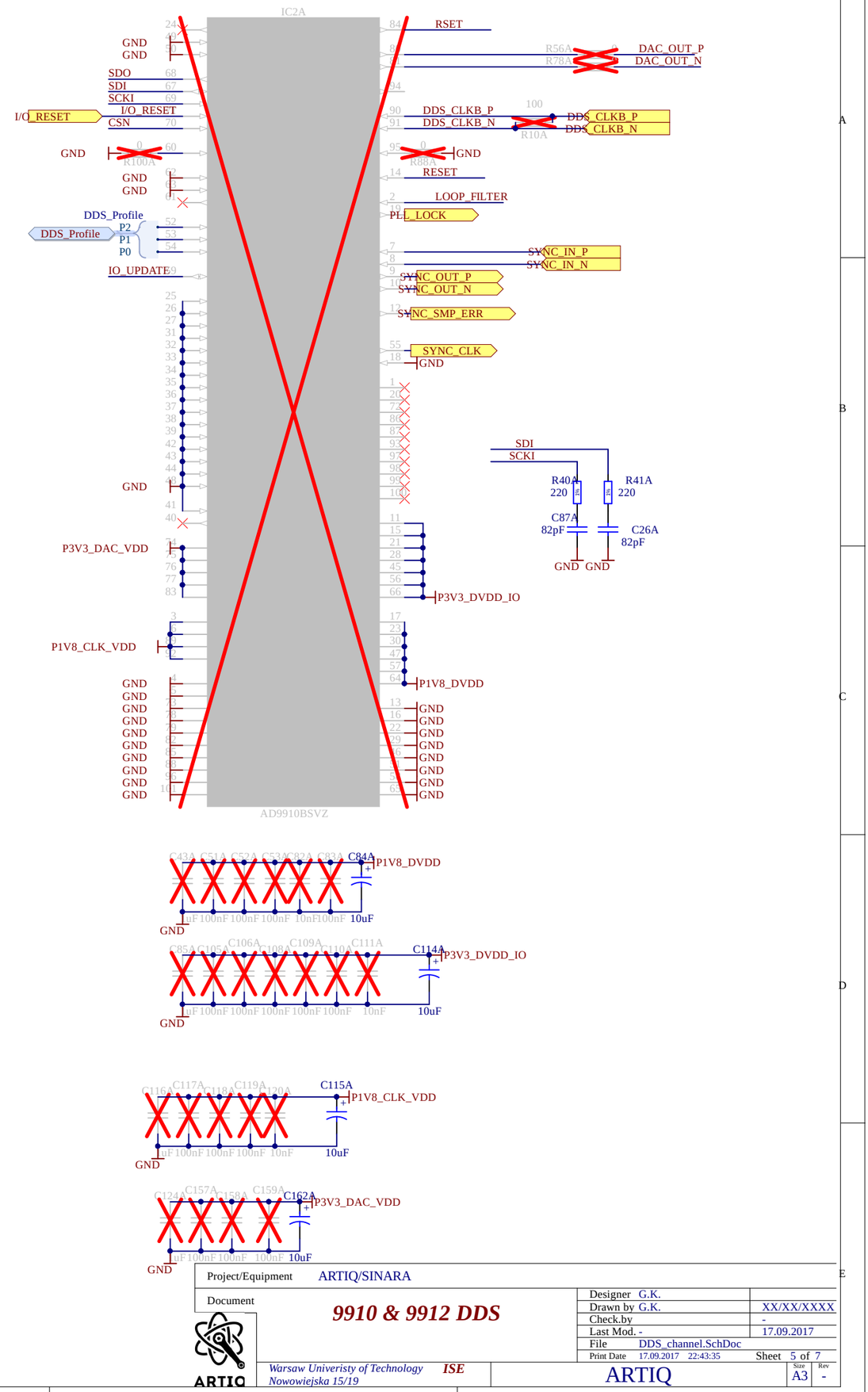


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758



Project/Equipment	ARTIQ/SINARA		
Document	9910 & 9912 DDS	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
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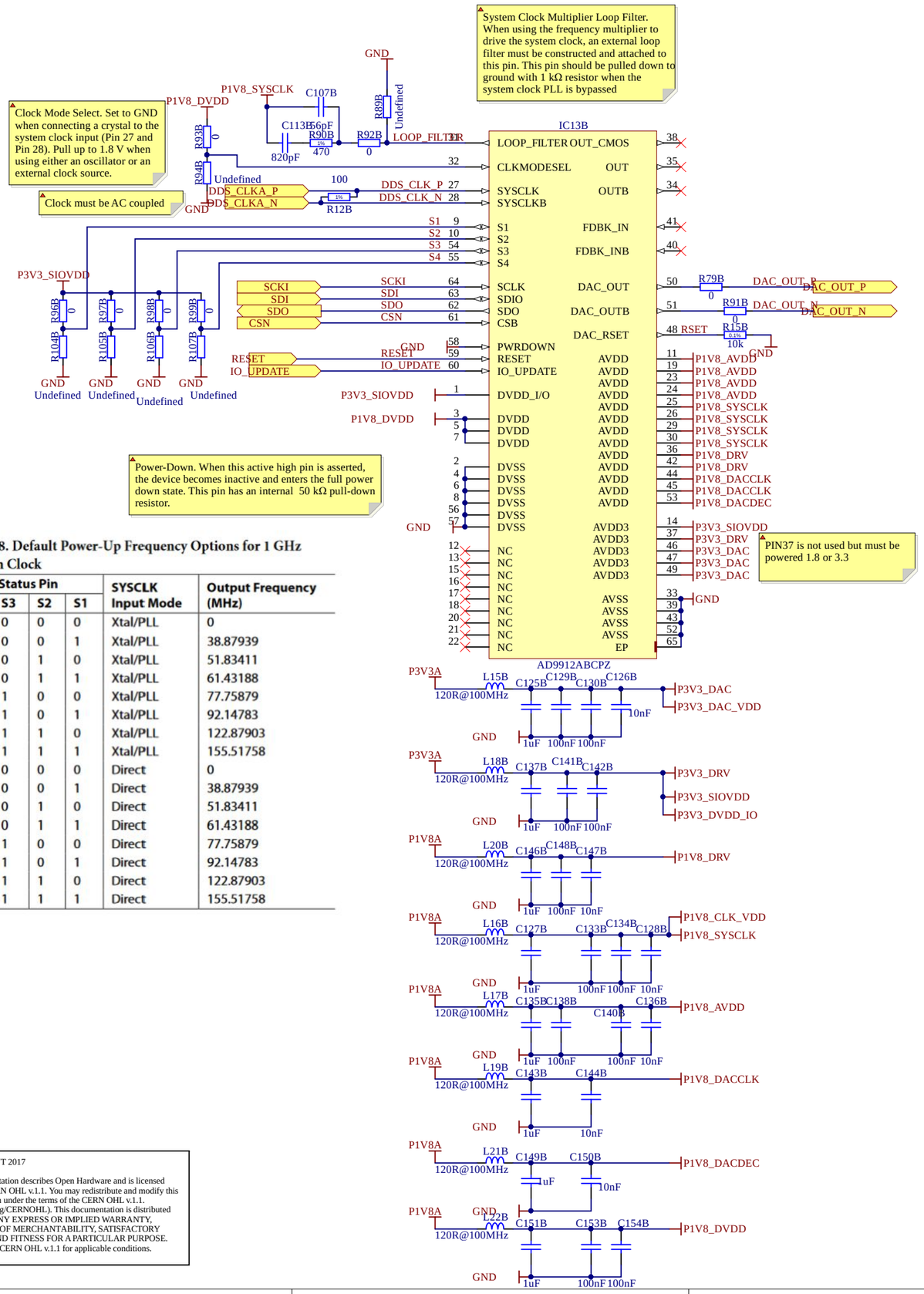
Warsaw Univeristy of Technology ISE Nowowiejska 15/19	ARTIQ	Size A3	Rev -



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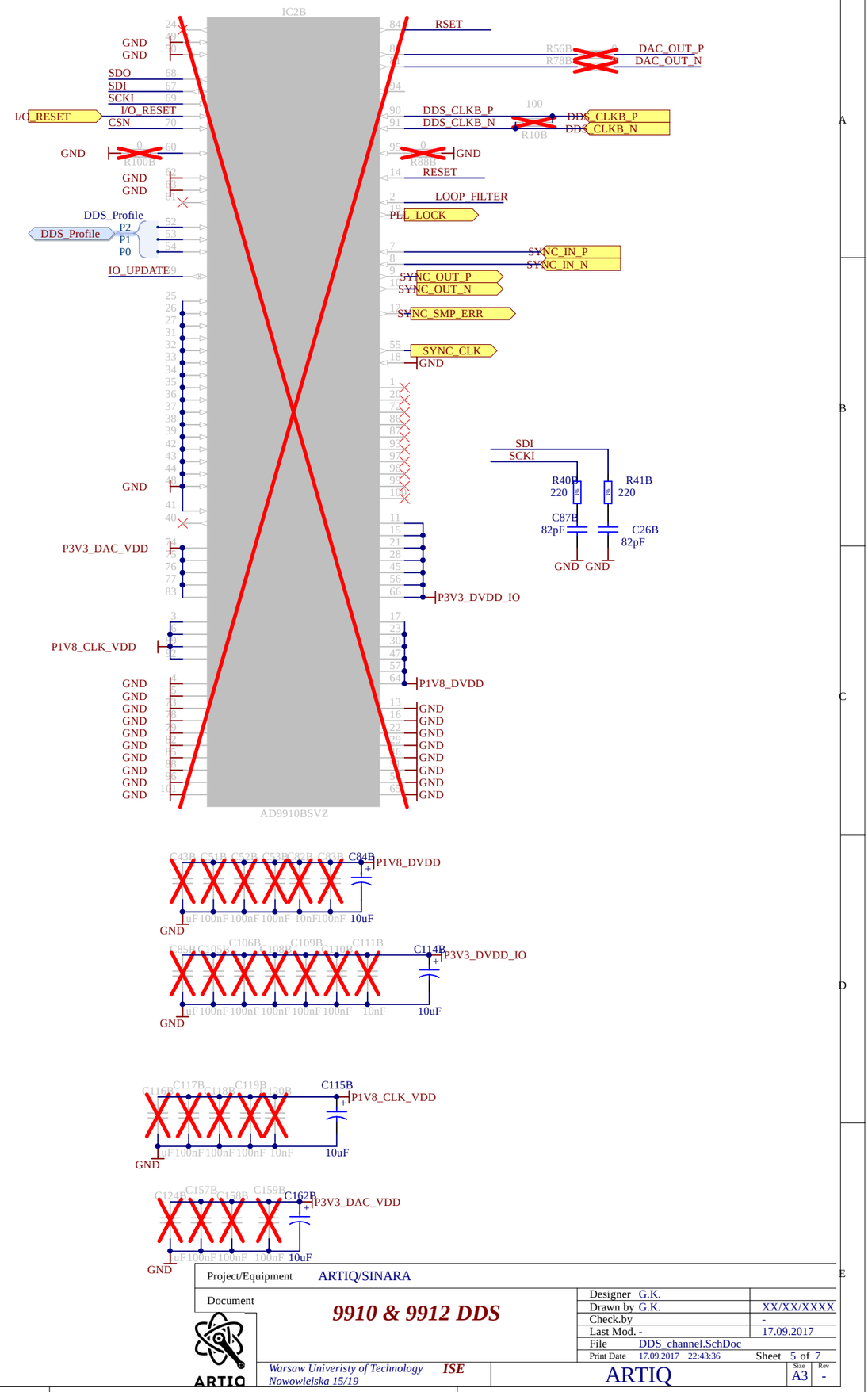
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758



Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
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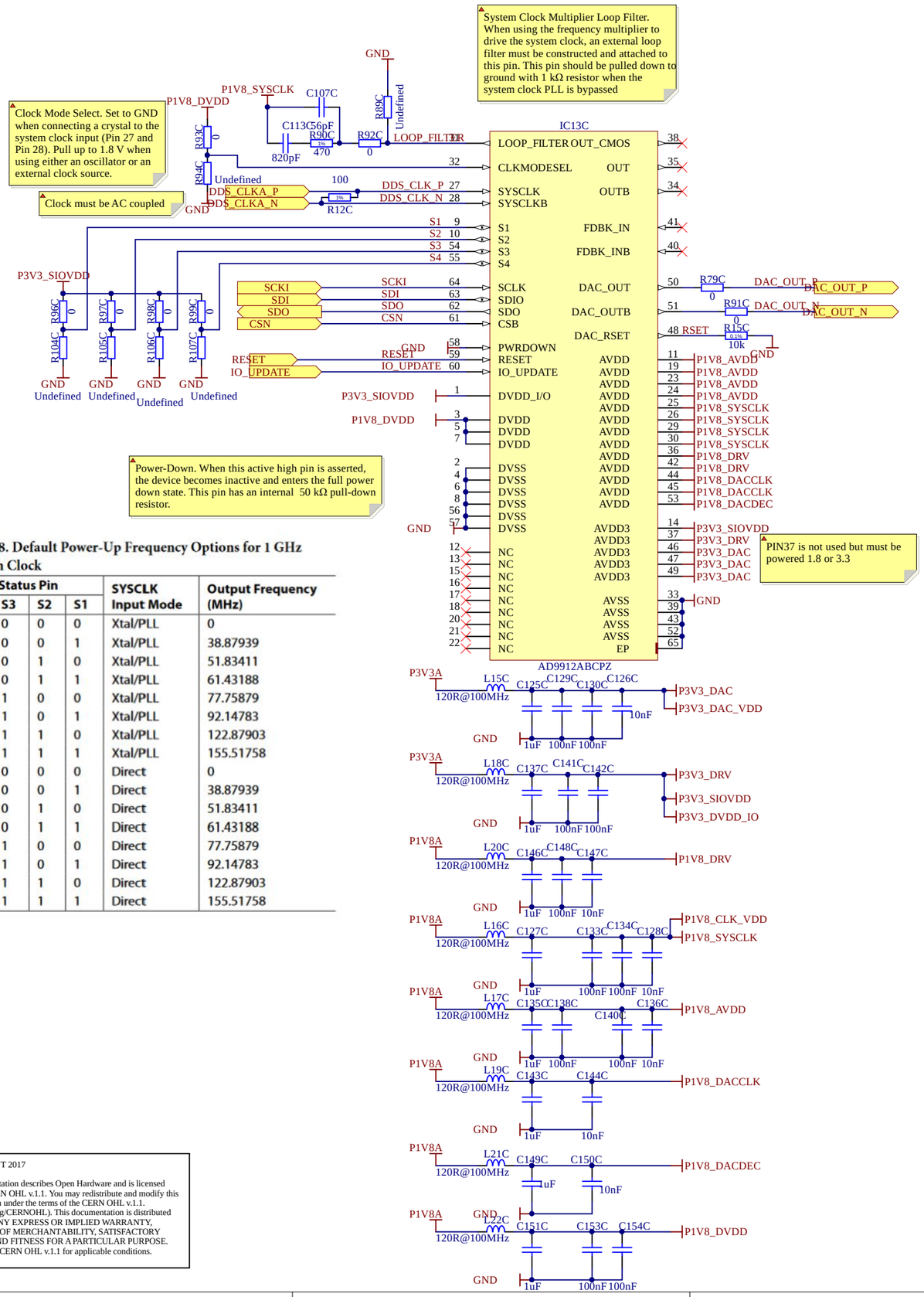

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0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
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0	1	1	0	Xtal/PLL	122.87903
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1	1	1	0	Direct	122.87903
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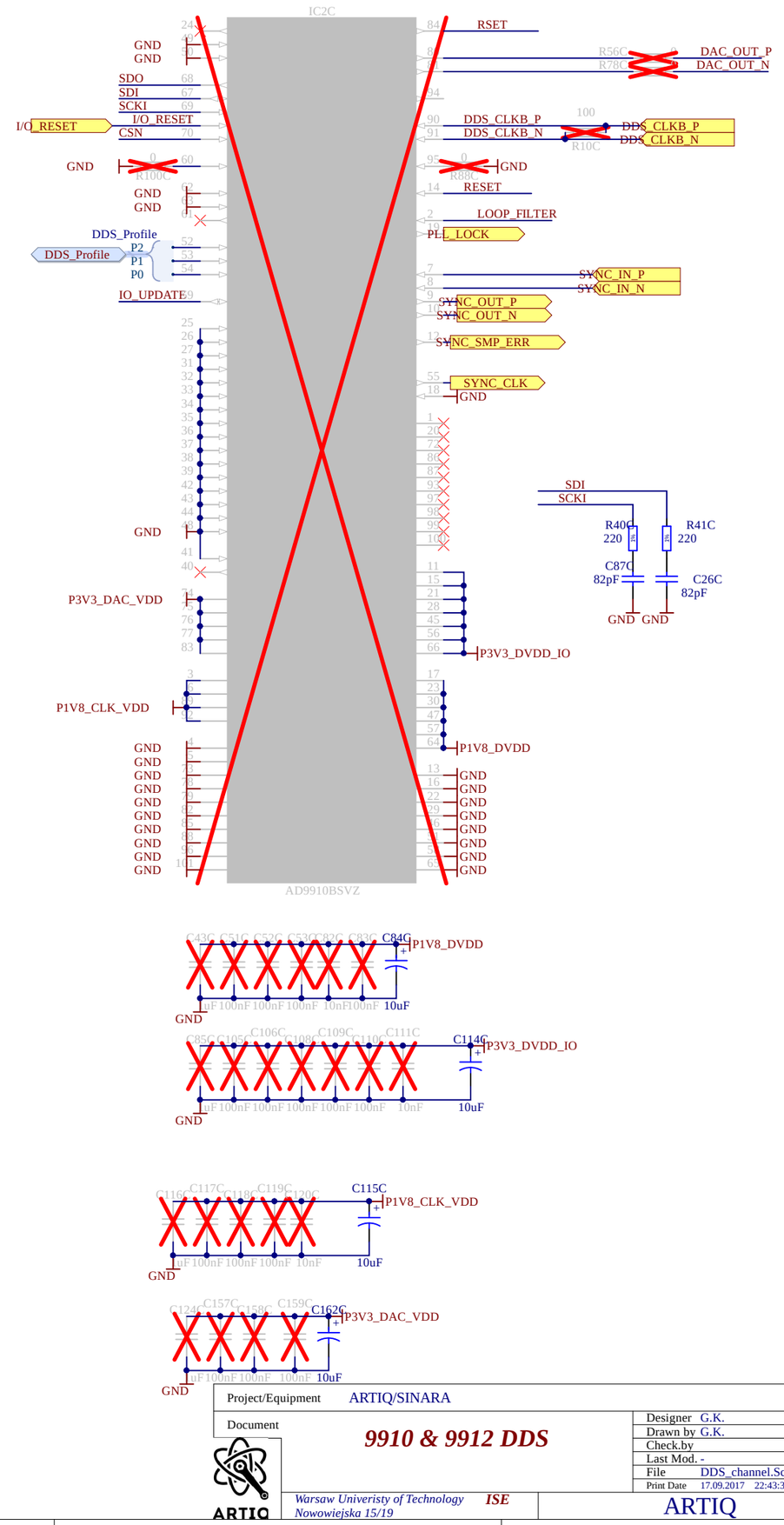

Project/Equipment	ARTIQ/SINARA		
Document	9910 & 9912 DDS	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
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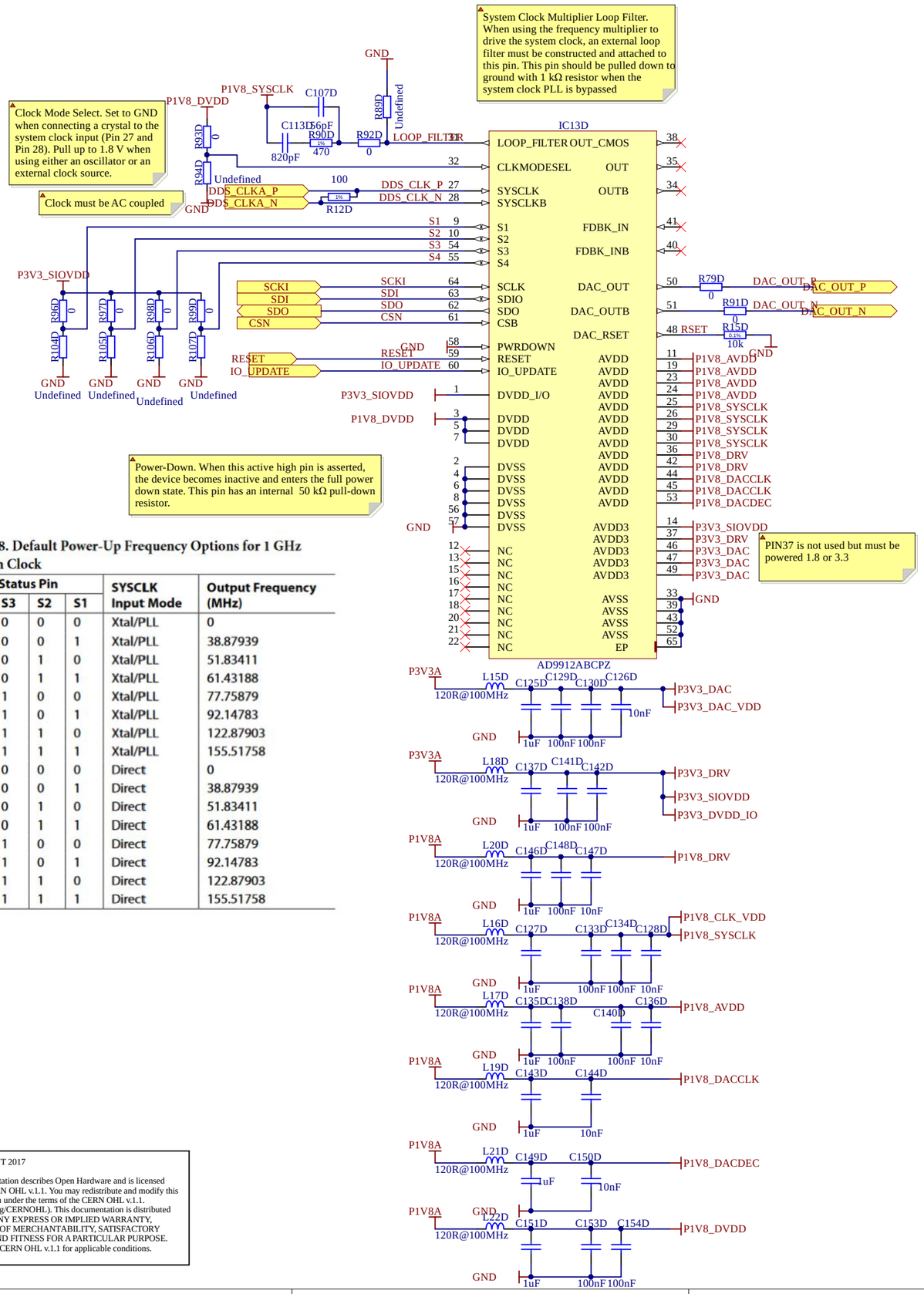
Warsaw Univeristy of Technology ISE Nowowiejska 15/19	ARTIQ	Size A3	Rev -



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1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
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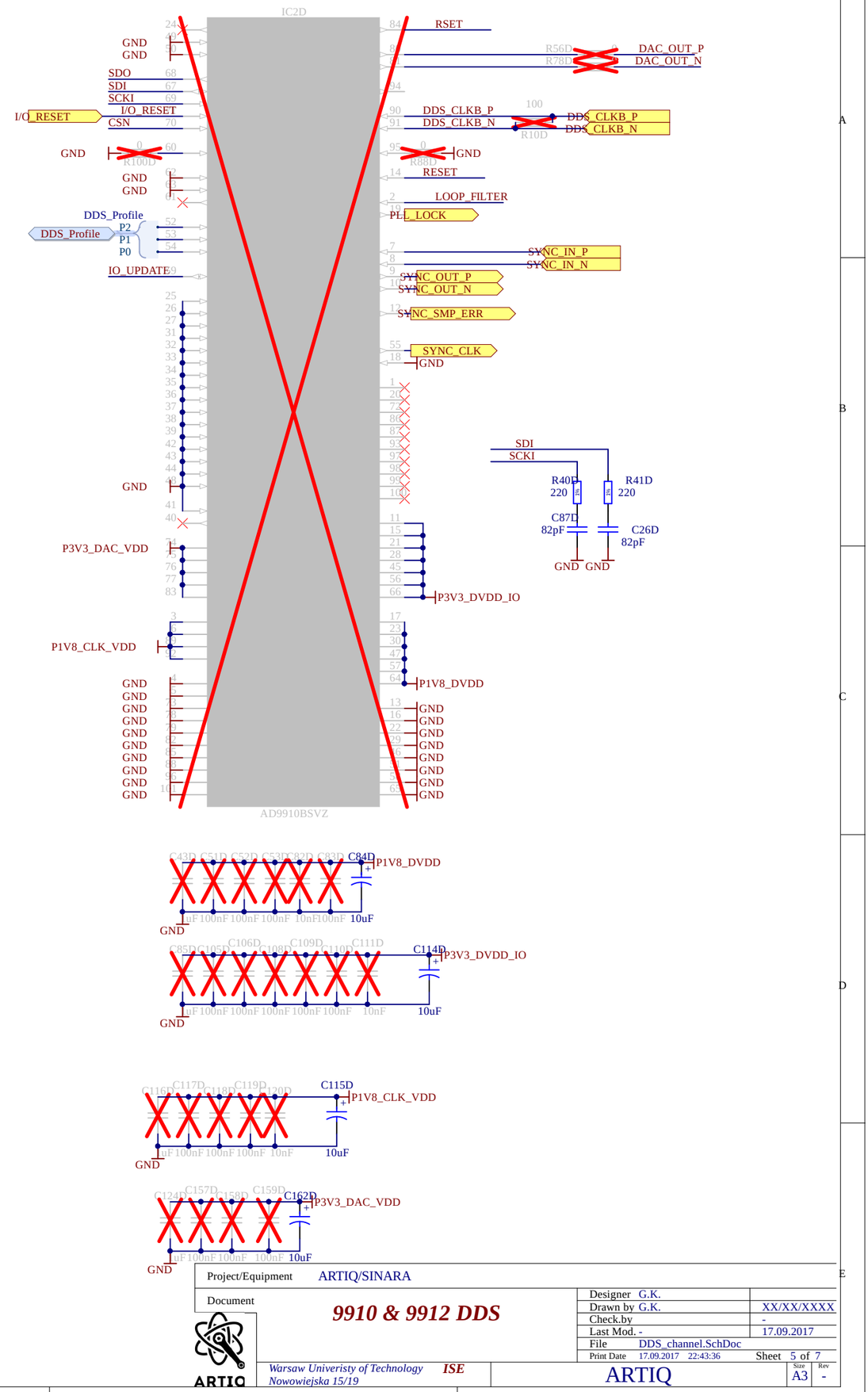

Project/Equipment	ARTIQ/SINARA		
Document	9910 & 9912 DDS	Designer G.K.	
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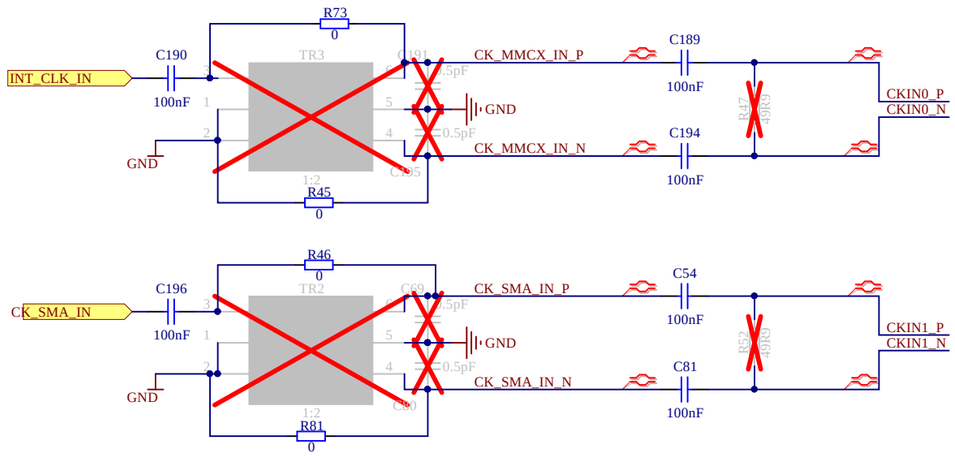
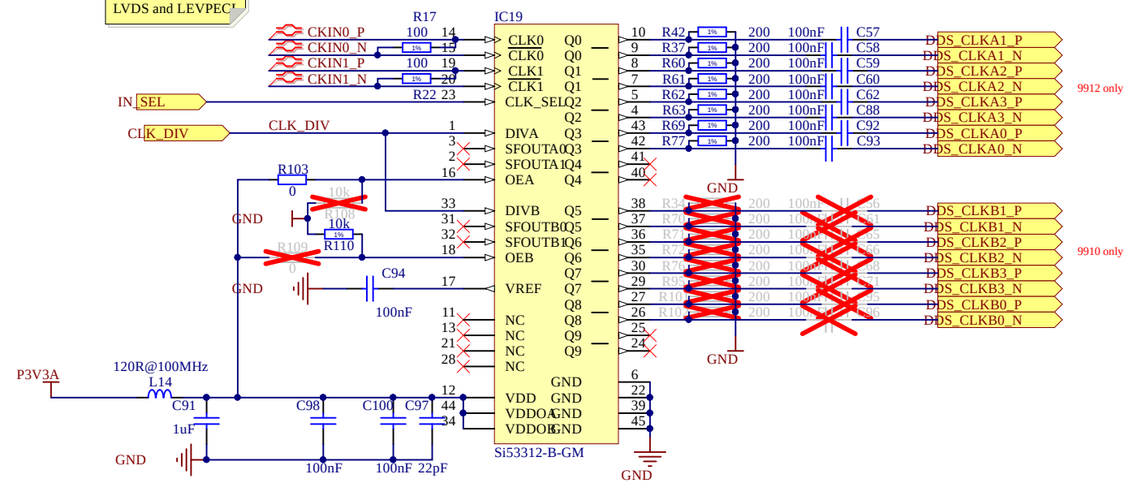
Warsaw Univeristy of Technology ISE Nowowiejska 15/19	ARTIQ	Size A3	Rev -



AC-Coupled Input Termination, Such as LVDS and LEVPECL



Project/Equipment	ARTIQ/SINARA		
Document	**Clock distribution and generation**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File CLK_INPUT.SchDoc	
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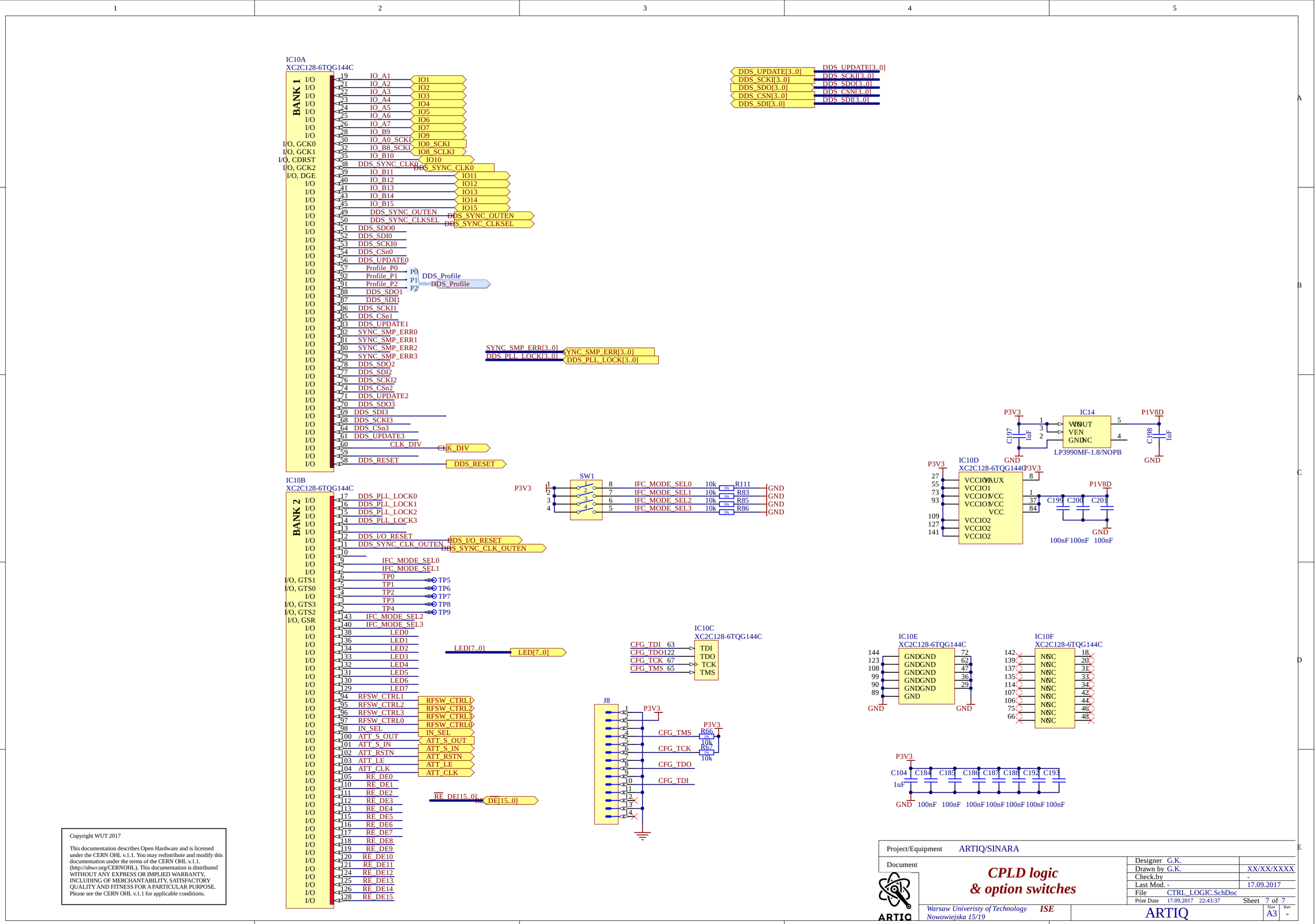
Warsaw Univeristy of Technology ISE *Nowowiejska 15/19*	ARTIQ	Size A3	Rev -



Project/Equipment	ARTIQ/SINARA
Document	**CPLD logic & option switches**
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	CTRL_LOGIC.SchDoc
Print Date	17.09.2017 22:43:37 Sheet 7 of 7

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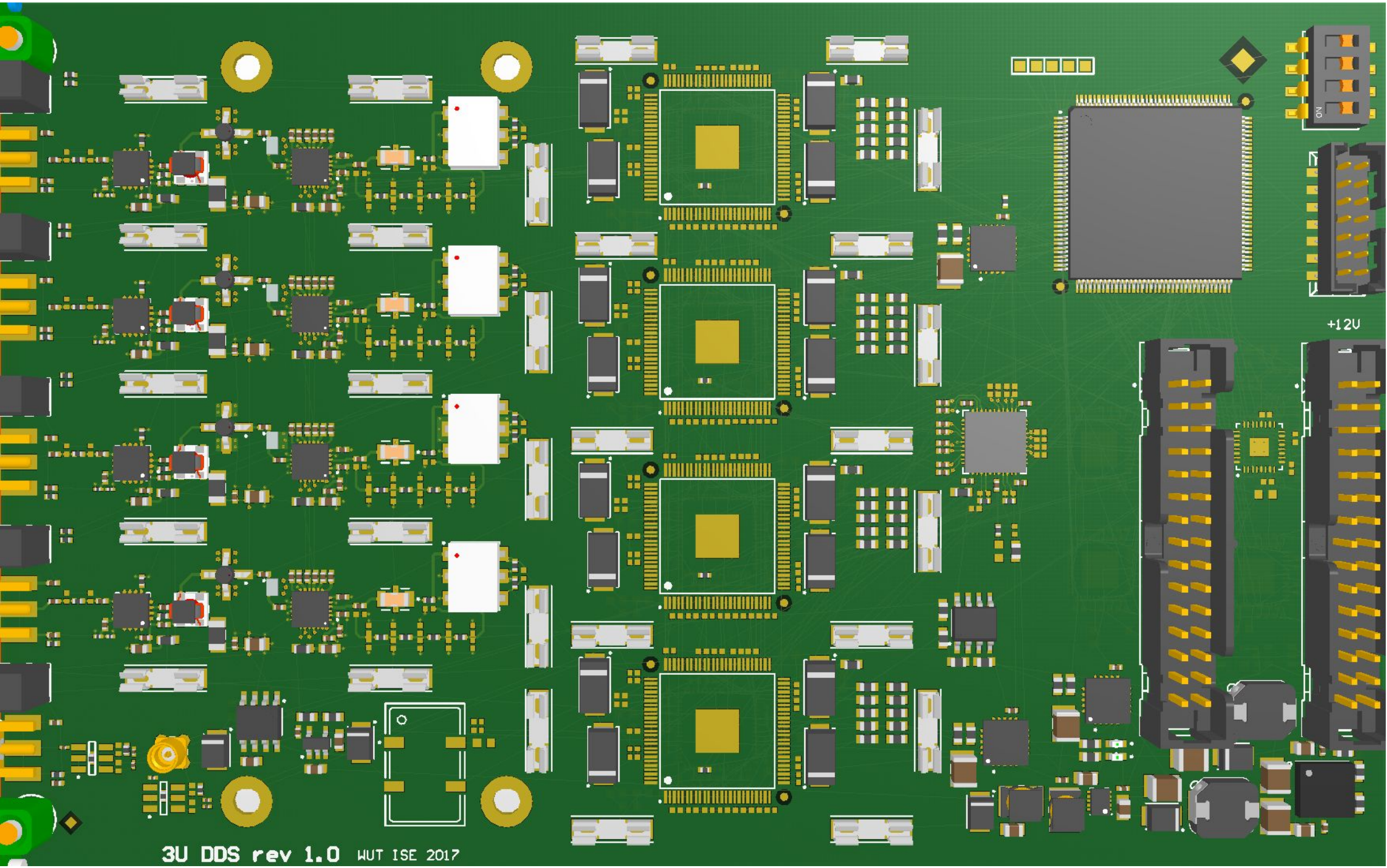
ARTIQ | Size A3 | Rev -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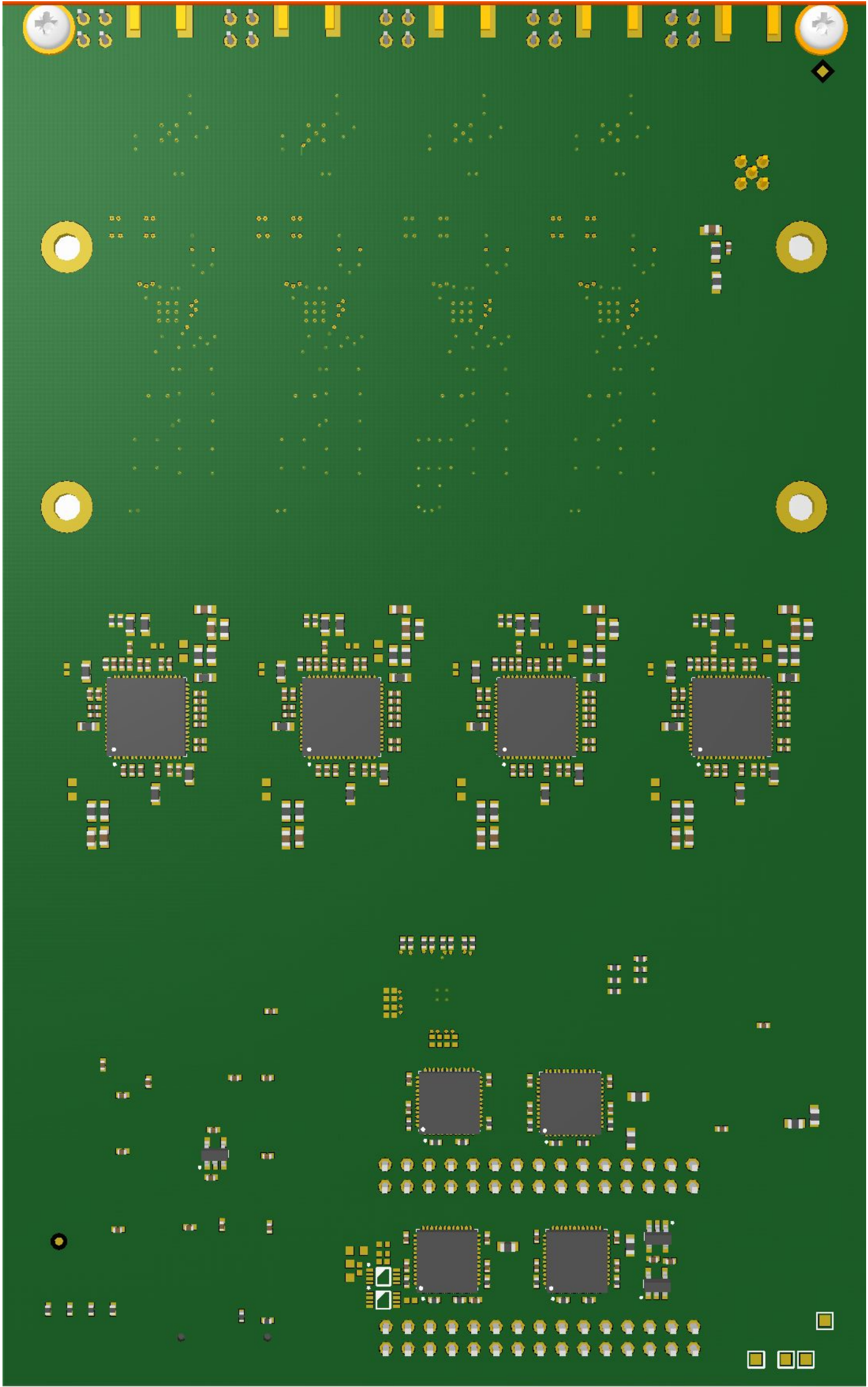

ON
1 2 3 4

+12V

TO KASLI/METLINO VHDCI

30

30

A B

A B

A B

A B

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