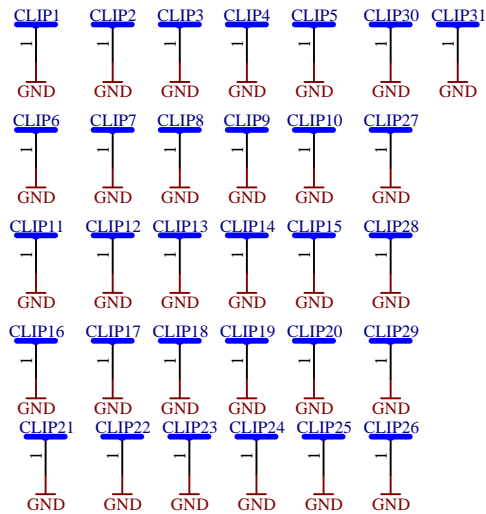


shield clips



Ext clock input

Internal clock input

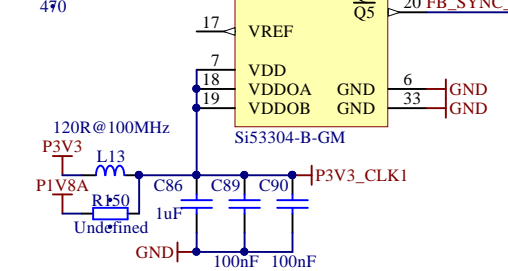
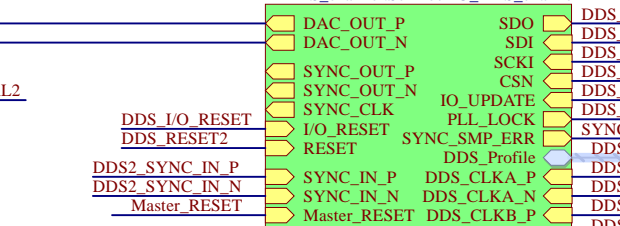
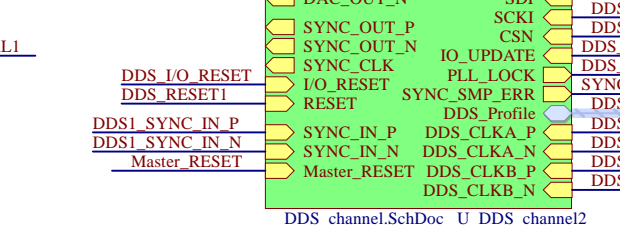
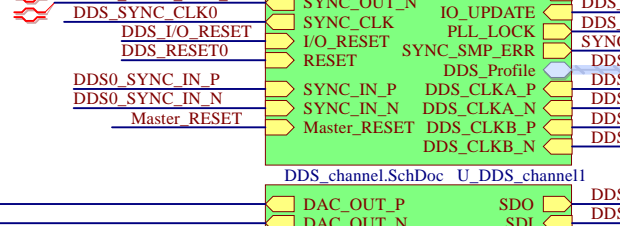
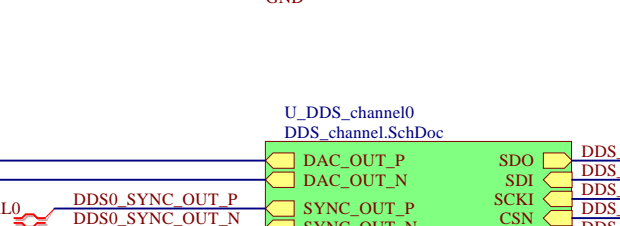
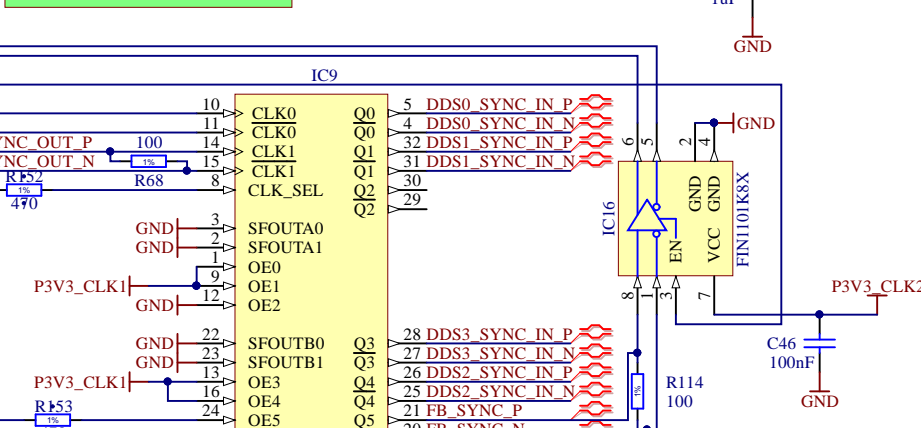
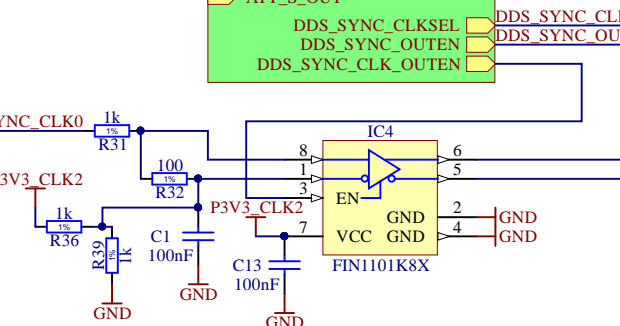
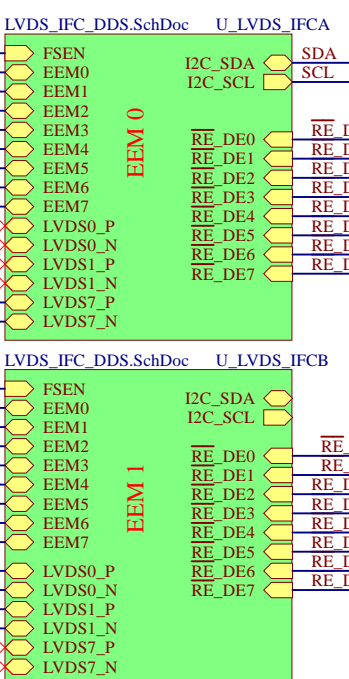
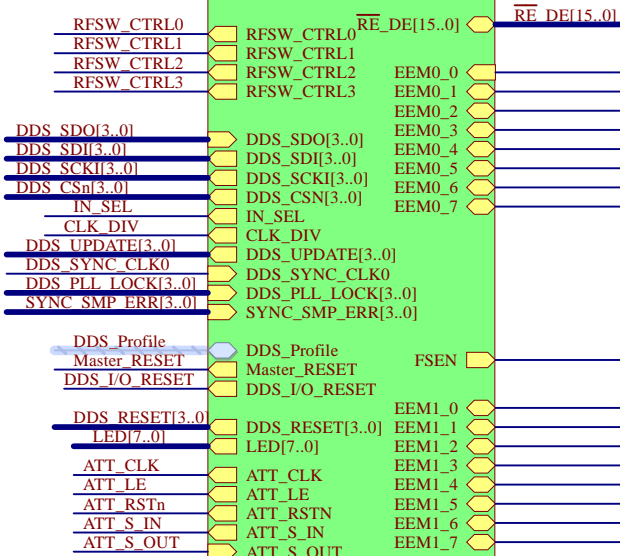
Output SMAs

SMA Insulating washers

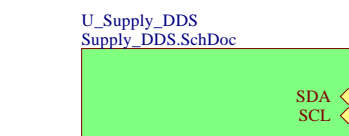
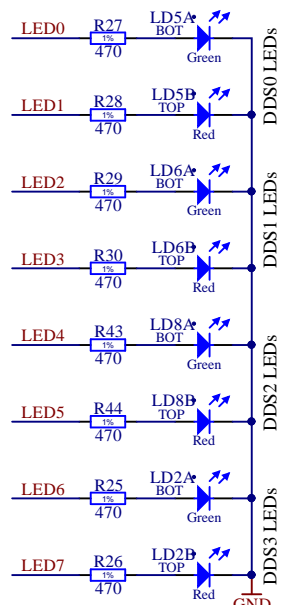
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D11.1xd6.6	D11.1xd6.6
WASHER3	WASHER4
D11.1xd6.6	D11.1xd6.6
WASHER5	WASHER6
D11.1xd6.6	D11.1xd6.6
WASHER7	WASHER8
D11.1xd6.6	D11.1xd6.6
WASHER9	WASHER10
D11.1xd6.6	D11.1xd6.6

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U_CTRL_LOGIC
CTRL_LOGIC.SchDoc



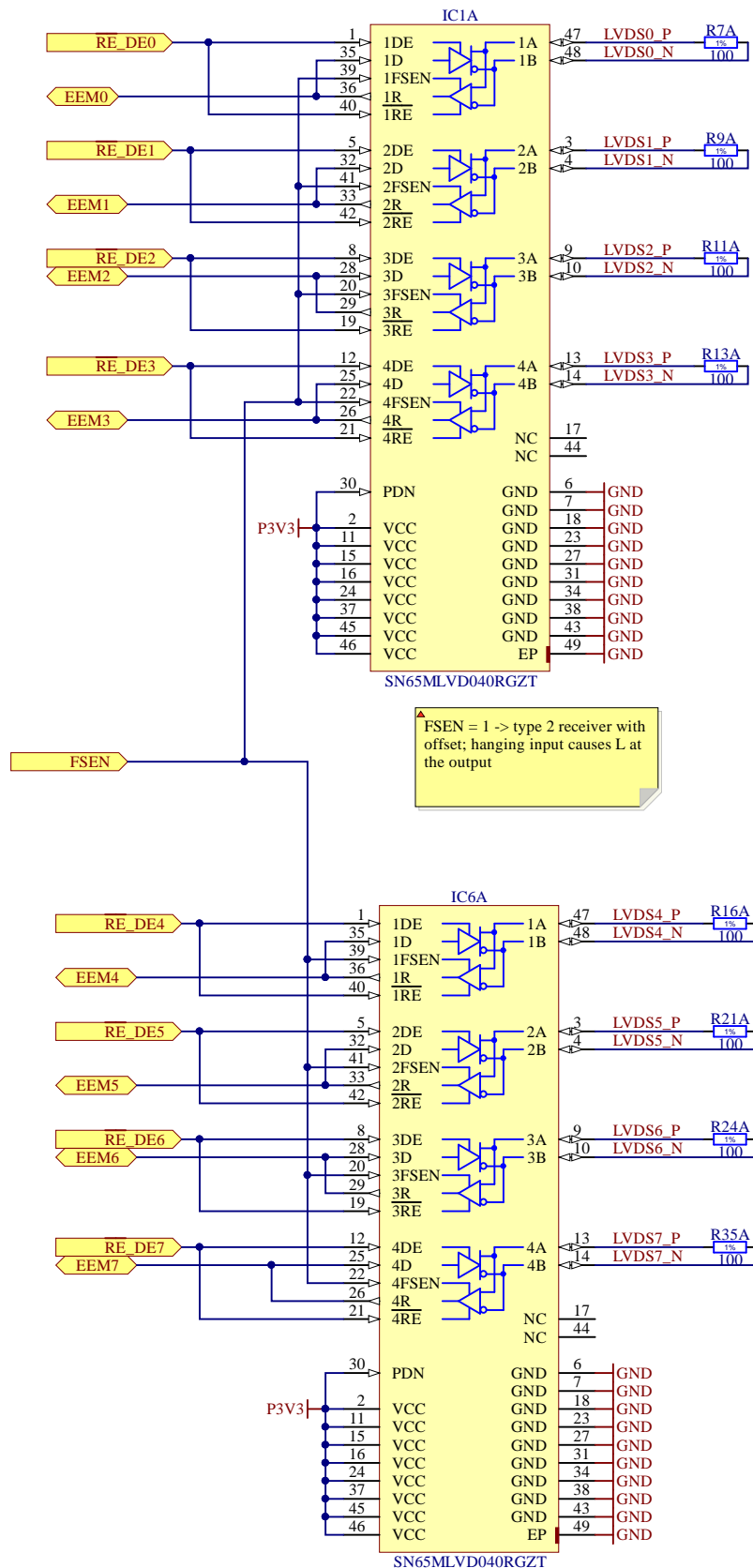
Trace lengths matched within each of DDS_SYNC_CLK[3:0], DDS_UPDATE[3:0], RF_SW_CTRL[3:0], IO[15:11] (RF_SW ctrl lines), DDS_SYNC_IN[3:0], DDS_RESET[3:0], DDS_CLK[3:0]



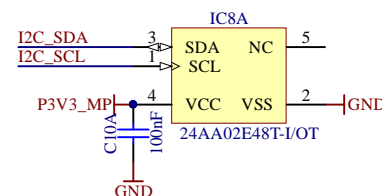
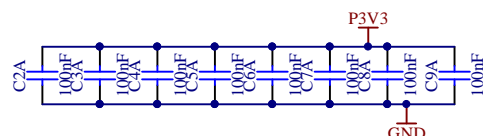
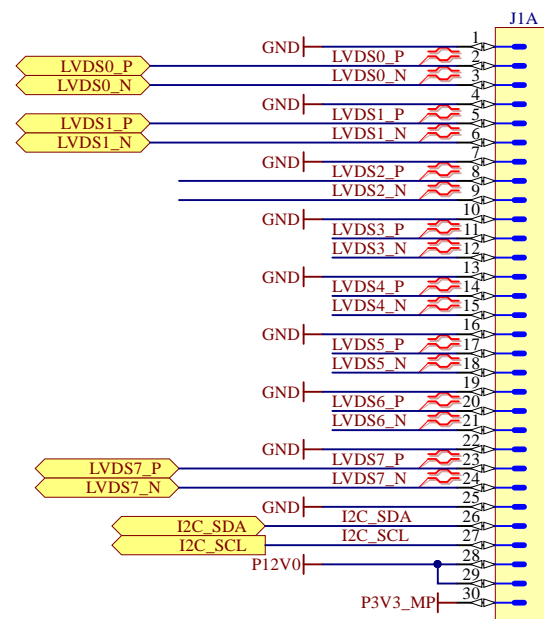
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Document	3U DDS (URUKUL) v1.1 Top entity	Warsaw University of Technology	ISE	Nowowiejska 15/19	ARTIQ	Size	A3	Rev	-						

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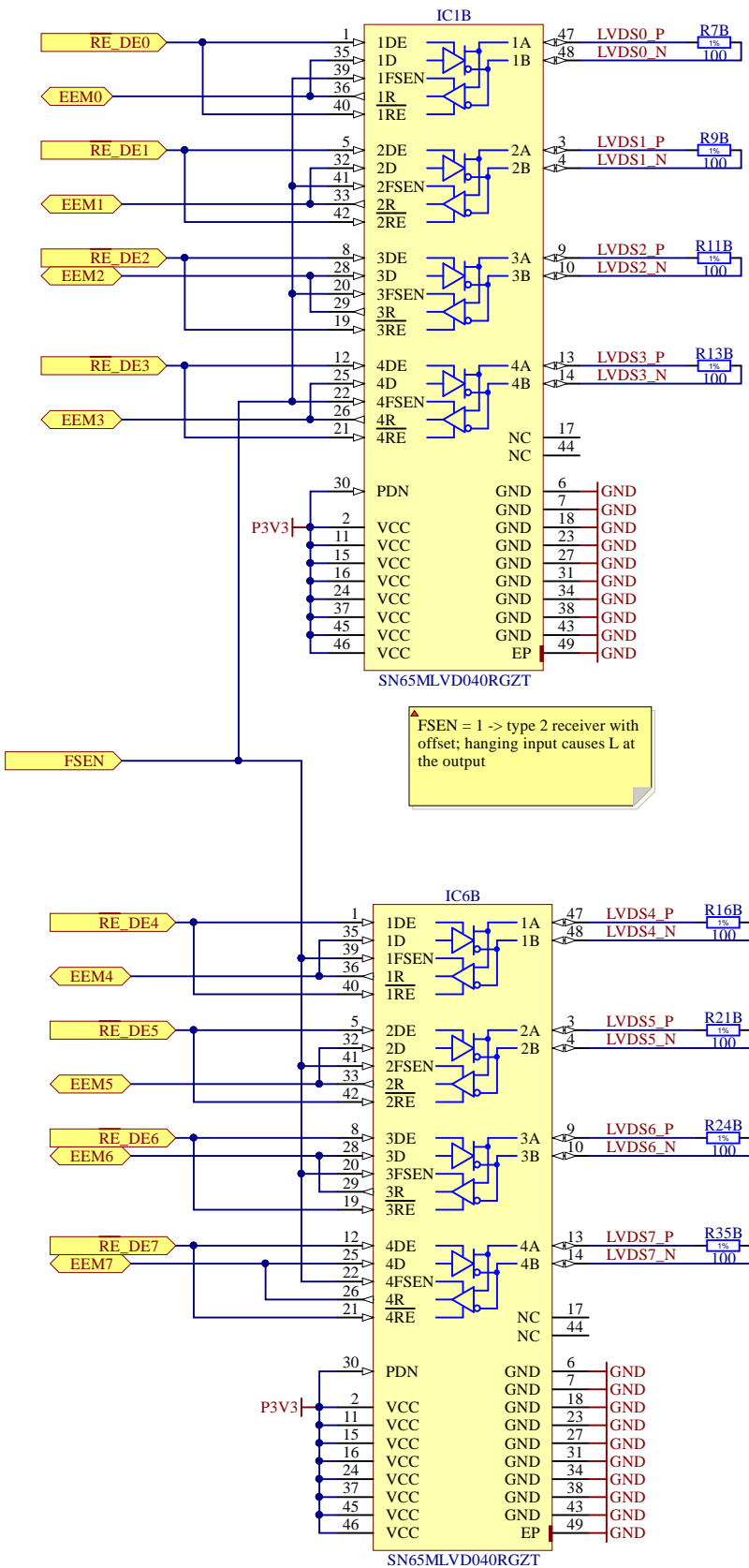


EEM connector: IO are LVDS, I2C is 3V3 LVCMOS, P3V3_MP up to 20mA, P12V up to 1A



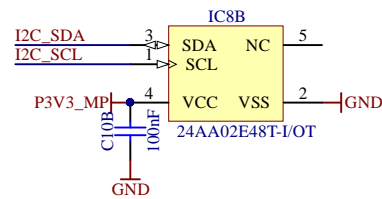
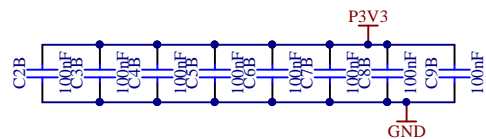
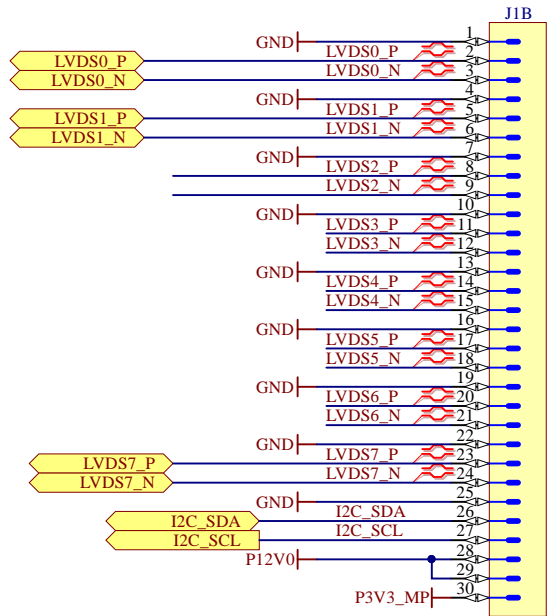
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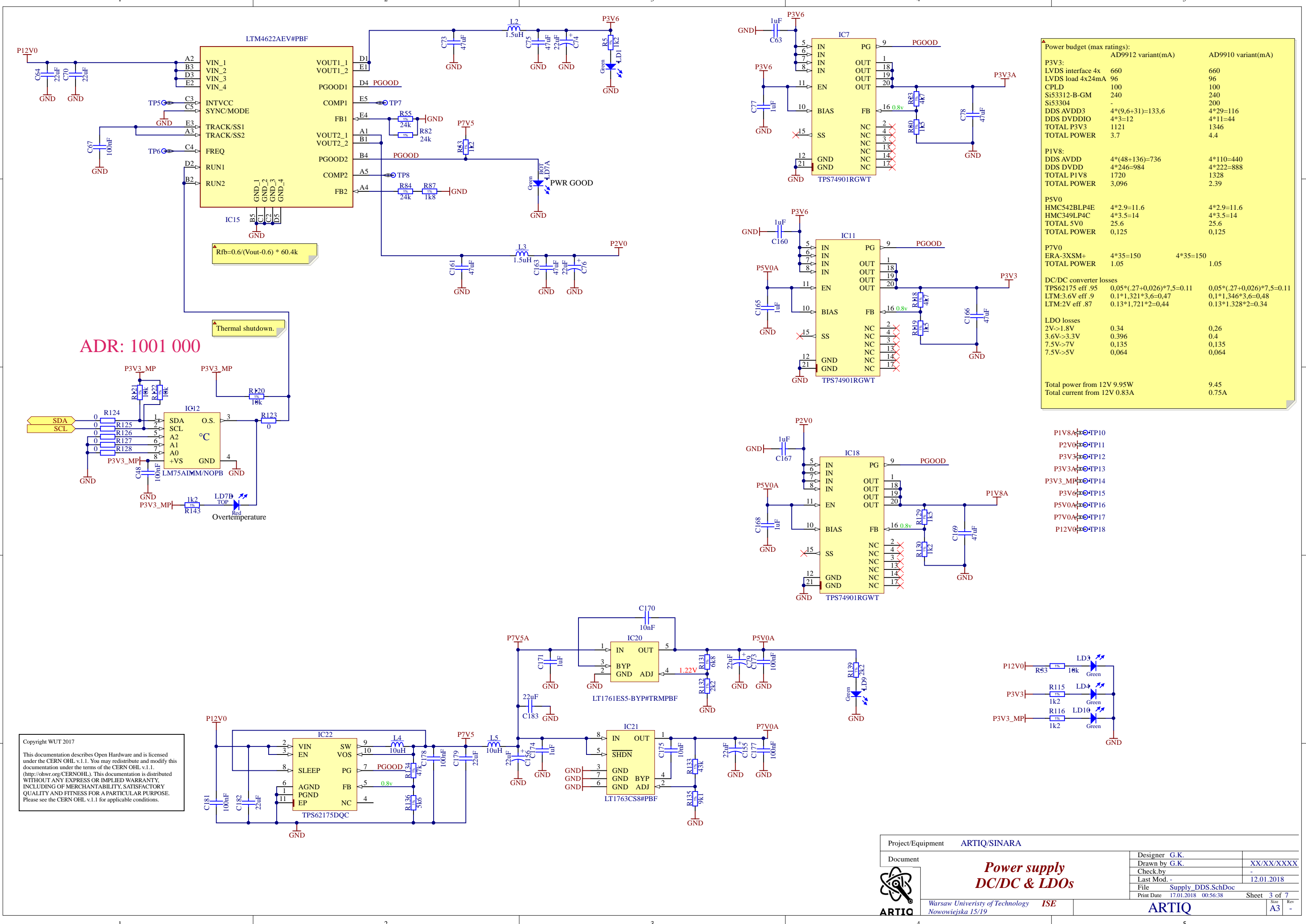
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FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

EEM connector: IO are LVDS, I2C is 3V3 LVCMOS, P3V3_MP up to 20mA, P12V up to 1A





Power budget (max ratings):		
	AD9912 variant(mA)	AD9910 variant(mA)
P3V3:		
LVDS interface 4x	660	660
LVDS load 4x24mA	96	96
CPLD	100	100
Si53312-B-GM	240	240
Si53304	-	200
DDS AVDD3	4*(9,6+31)=133,6	4*29=116
DDS DVDDIO	4*3=12	4*11=44
TOTAL P3V3	1121	1346
TOTAL POWER	3,7	4,4
P1V8:		
DDS AVDD	4*(48+136)=736	4*110=440
DDS DVDD	4*246=984	4*222=888
TOTAL P1V8	1720	1328
TOTAL POWER	3,096	2,39
P5V0		
HMC542BLP4E	4*2,9=11,6	4*2,9=11,6
HMC349LP4C	4*3,5=14	4*3,5=14
TOTAL 5V0	25,6	25,6
TOTAL POWER	0,125	0,125
P7V0		
ERA-3XSM+	4*35=150	4*35=150
TOTAL POWER	1,05	1,05
DC/DC converter losses		
TPS62175 eff .95	0,05*(,27+0,026)*7,5=0,11	0,05*(,27+0,026)*7,5=0,11
LTM:3.6V eff .9	0,1*1,321*3,6=0,47	0,1*1,346*3,6=0,48
LTM:2V eff .87	0,13*1,721*2=0,44	0,13*1,328*2=0,34
LDO losses		
2V->1.8V	0,34	0,26
3.6V->3.3V	0,396	0,4
7.5V->7V	0,135	0,135
7.5V->5V	0,064	0,064
Total power from 12V 9.95W		9.45
Total current from 12V 0.83A		0.75A

- P1V8A TP10
- P2V0 TP11
- P3V3 TP12
- P3V3A TP13
- P3V3_MP TP14
- P3V6 TP15
- P5V0A TP16
- P7V0A TP17
- P12V0 TP18

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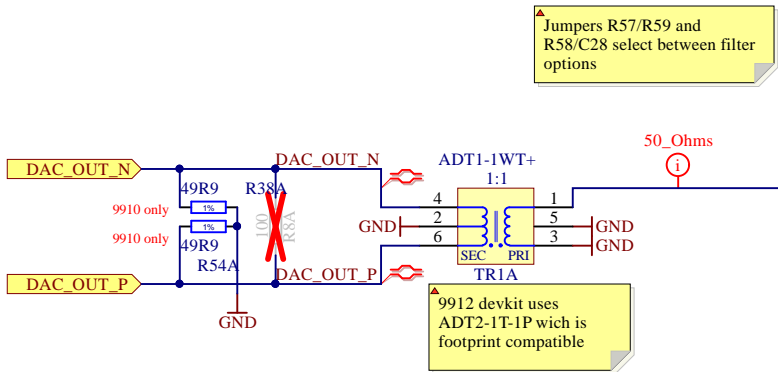
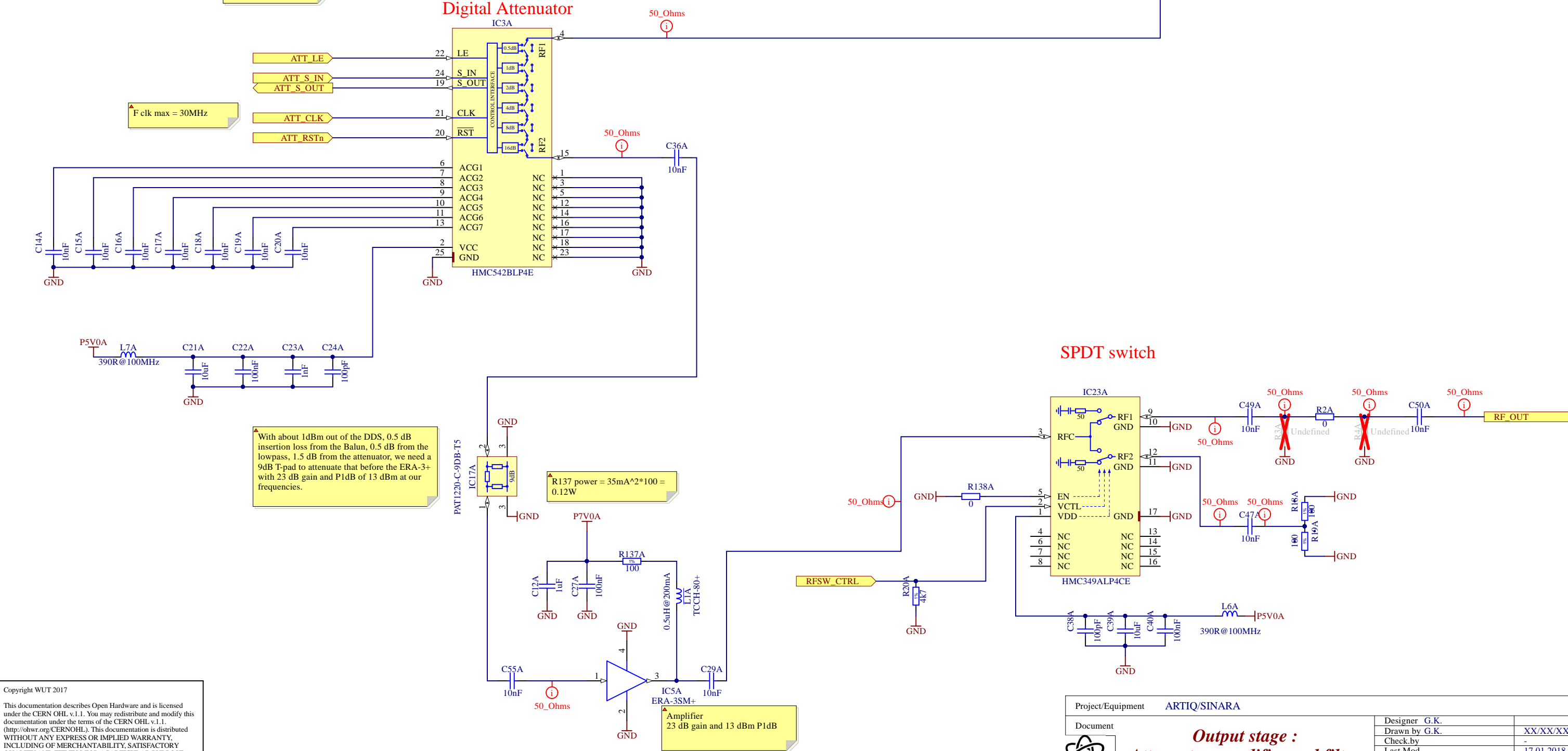
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		Sheet 4 of 7	
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Output stage :
Attenuator, amplifier and filter

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ARTIQ



Digital Attenuator

SPDT switch

Jumpers R57/R59 and R58/C28 select between filter options

9912 devkit uses ADT2-1T-1P which is footprint compatible

F clk max = 30MHz

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

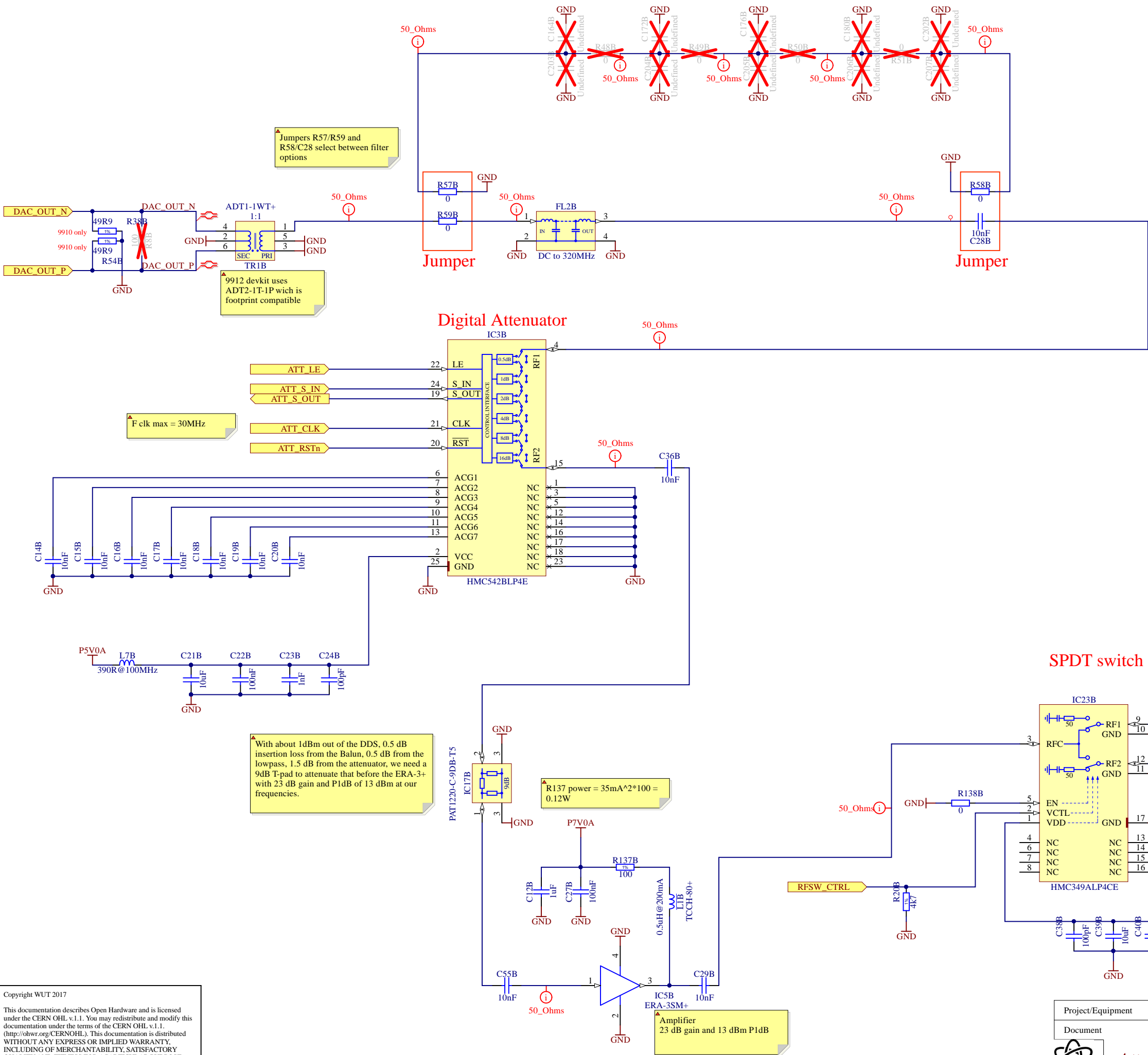
R137 power = $35\text{mA}^2 \times 100 = 0.12\text{W}$

Amplifier 23 dB gain and 13 dBm P1dB

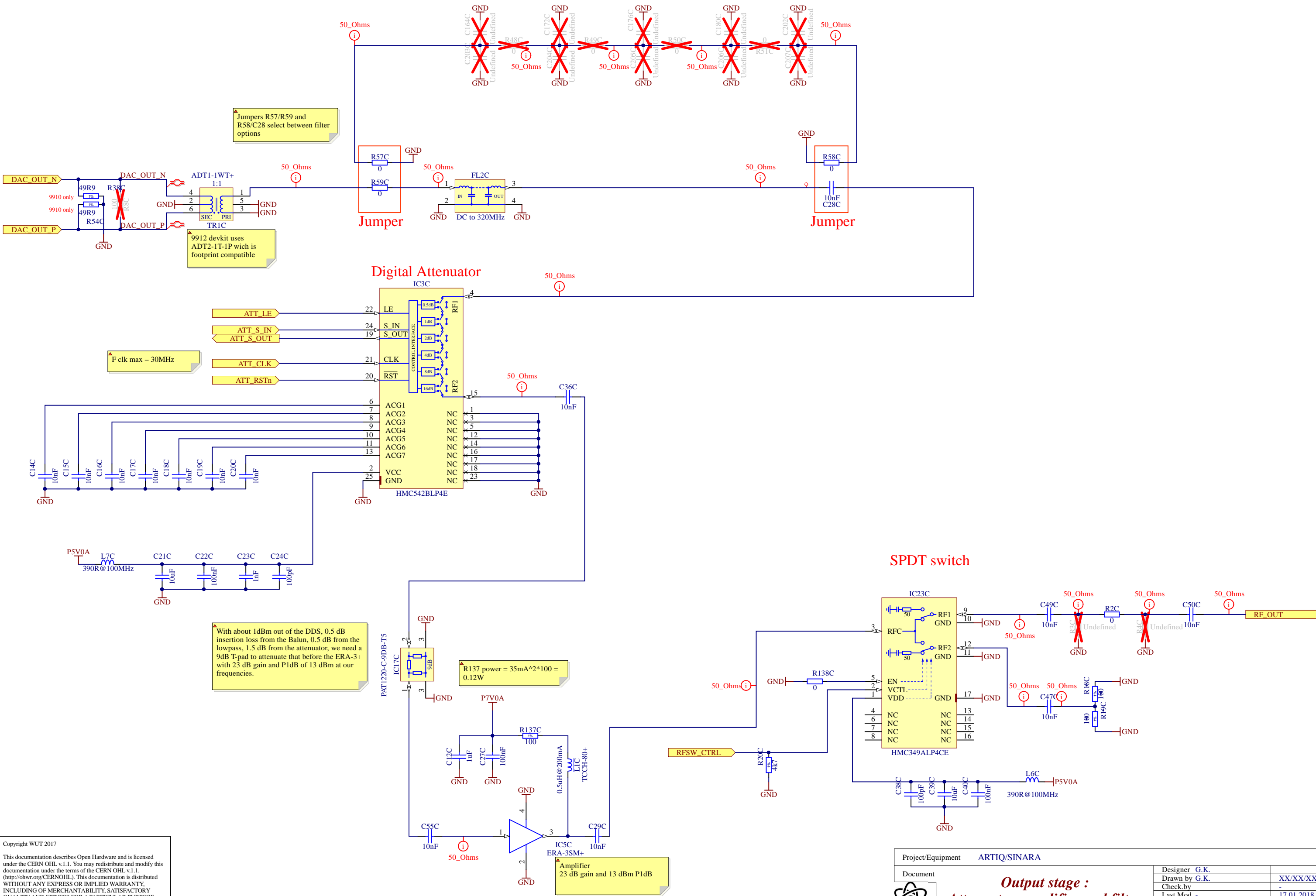
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Output stage :
Attenuator, amplifier and filter



Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Loop filter calculation:
Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

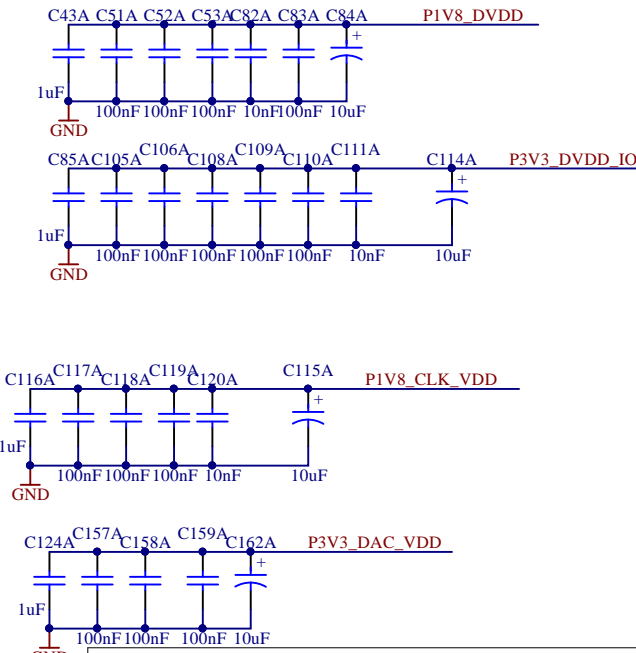
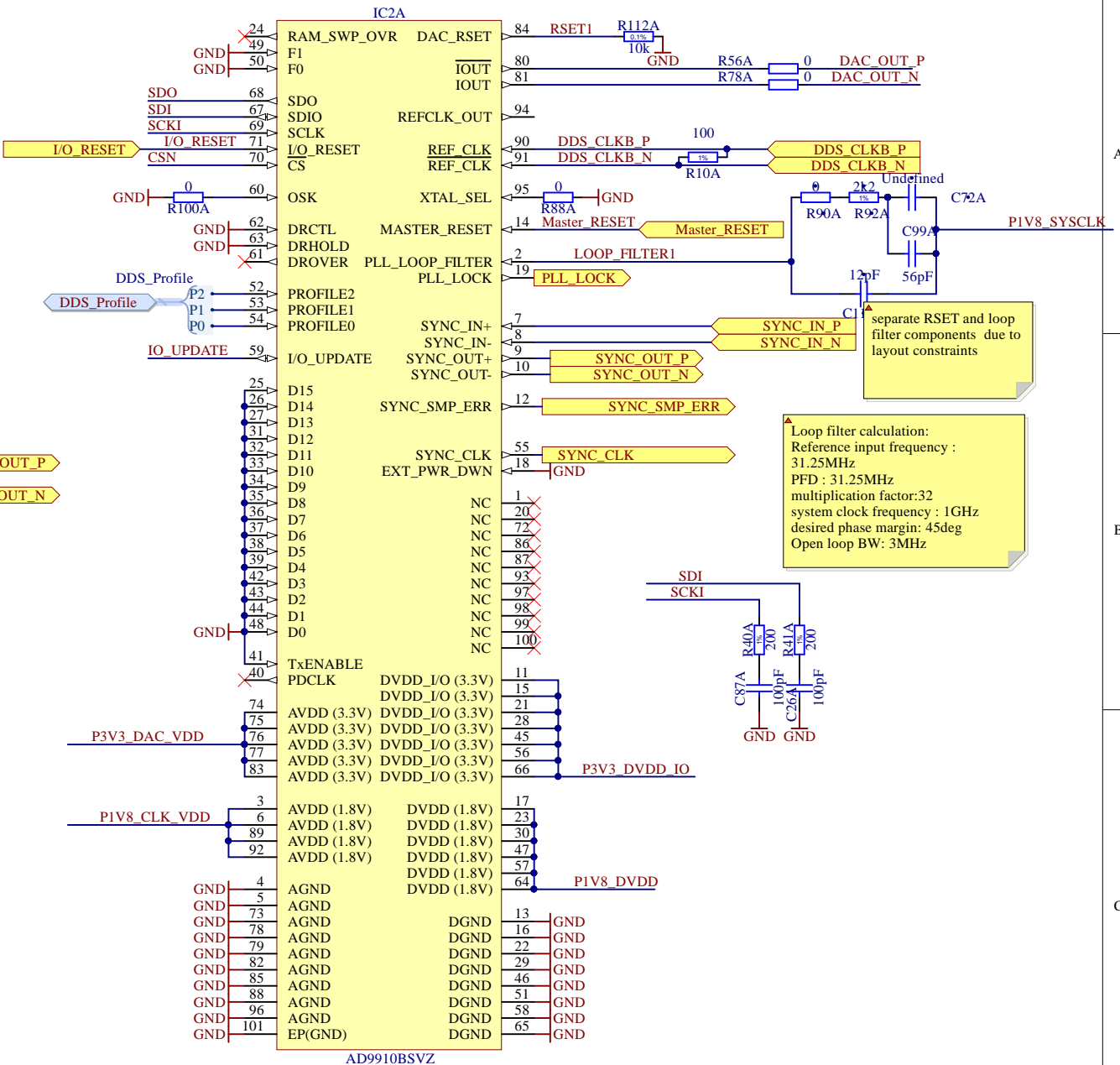
Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

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DS\Sx_table.PNG

PIN37 is not used but must be powered 1.8 or 3.3

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Warsaw University of Technology		ISE	ARTIQ
Nowowiejska 15/19		Size A3	Rev -

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

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Loop filter calculation:
Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

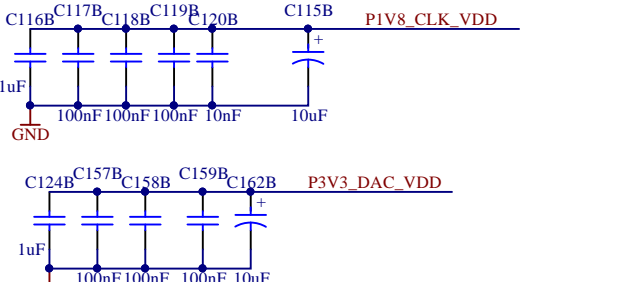
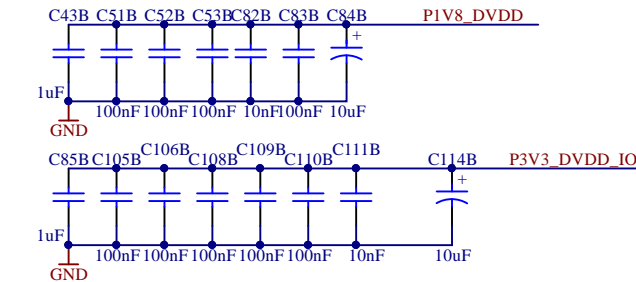
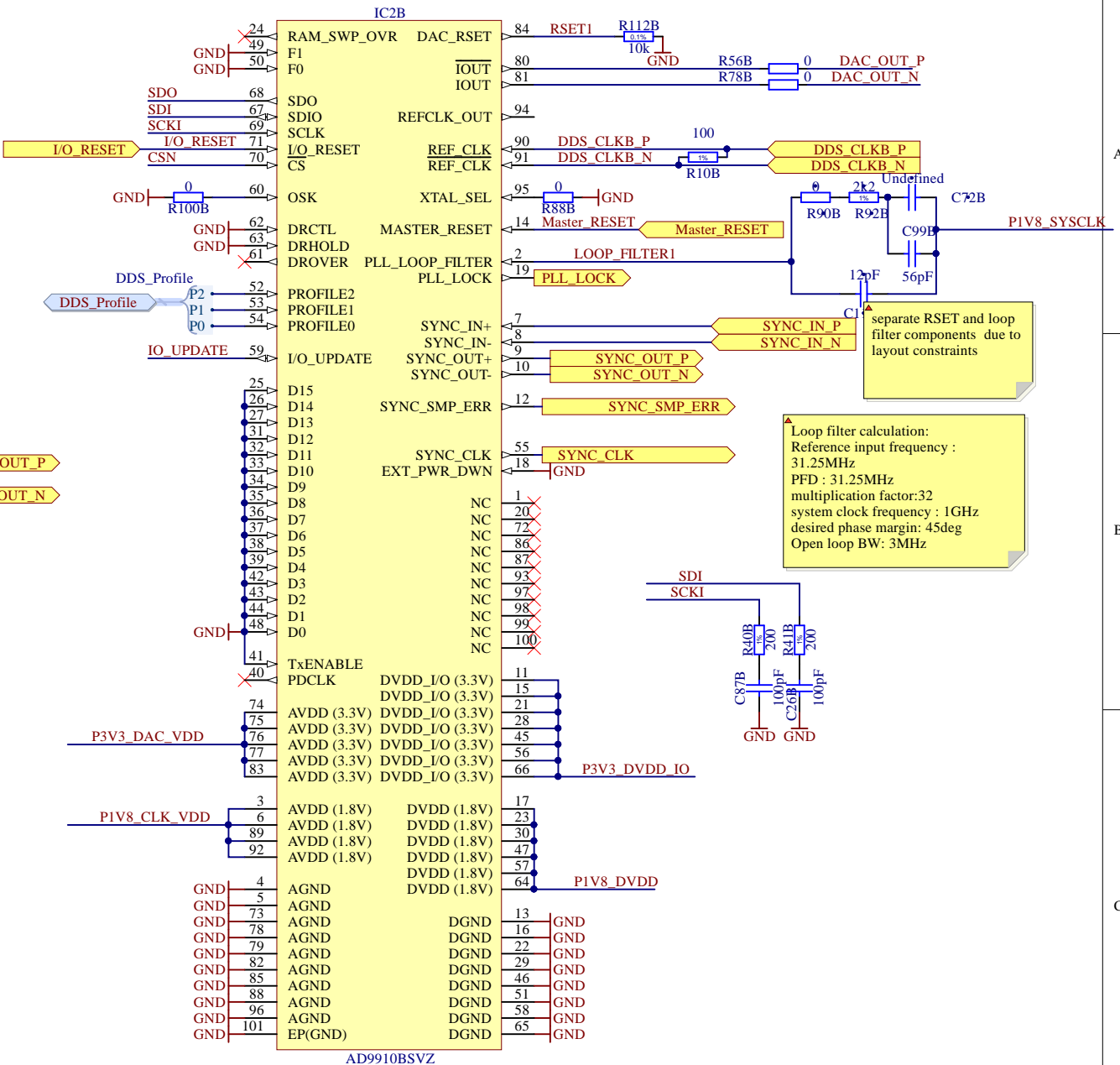
Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

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PIN37 is not used but must be powered 1.8 or 3.3

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multiplication factor: 20
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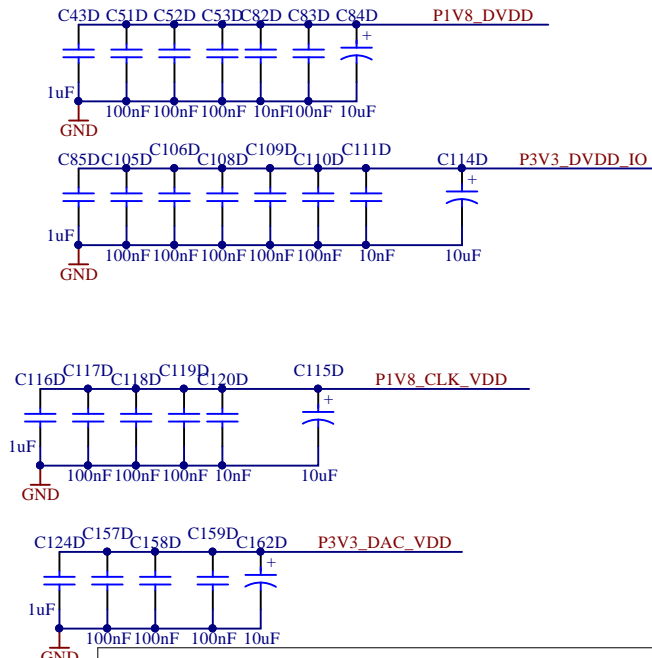
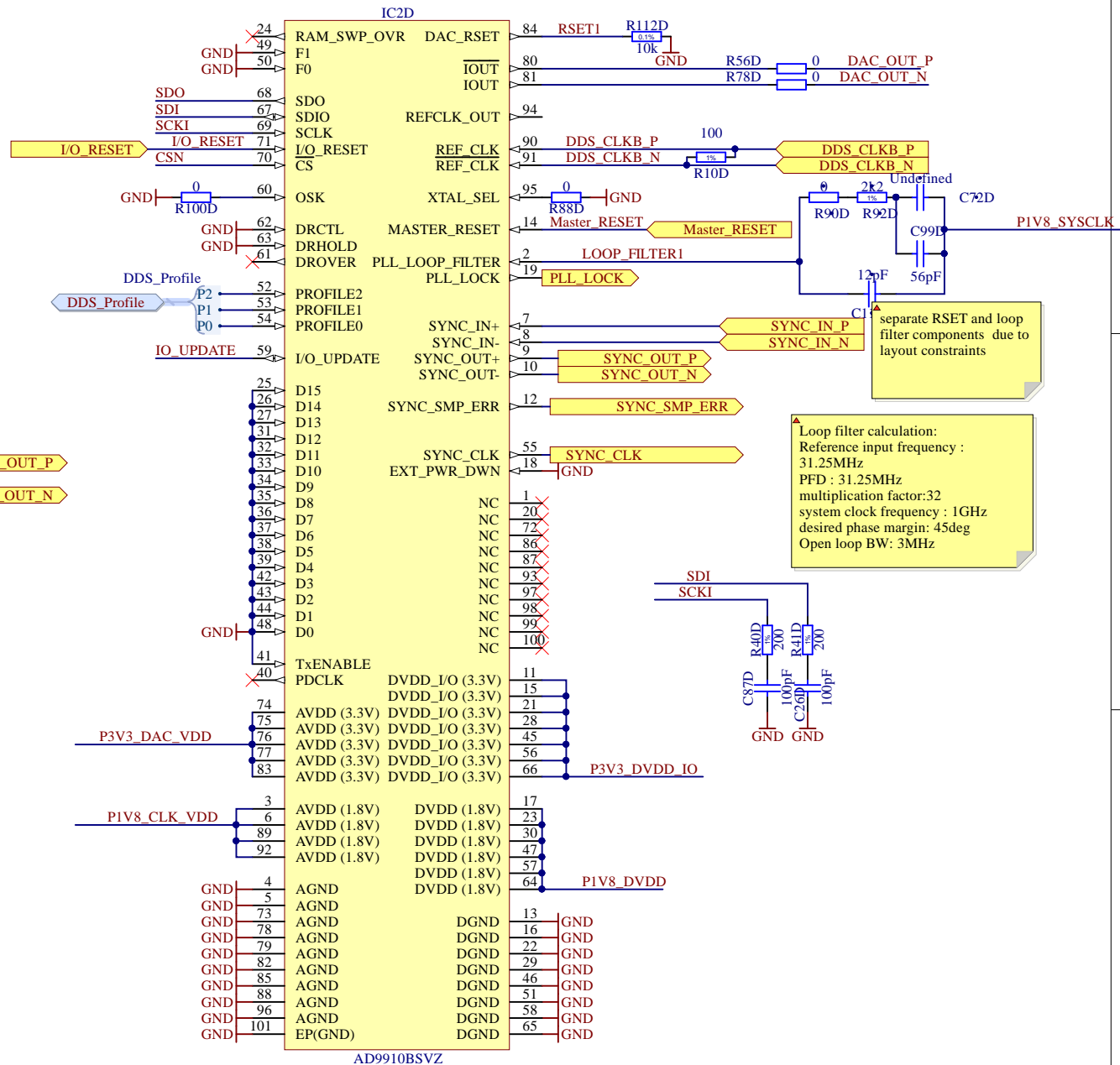
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Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

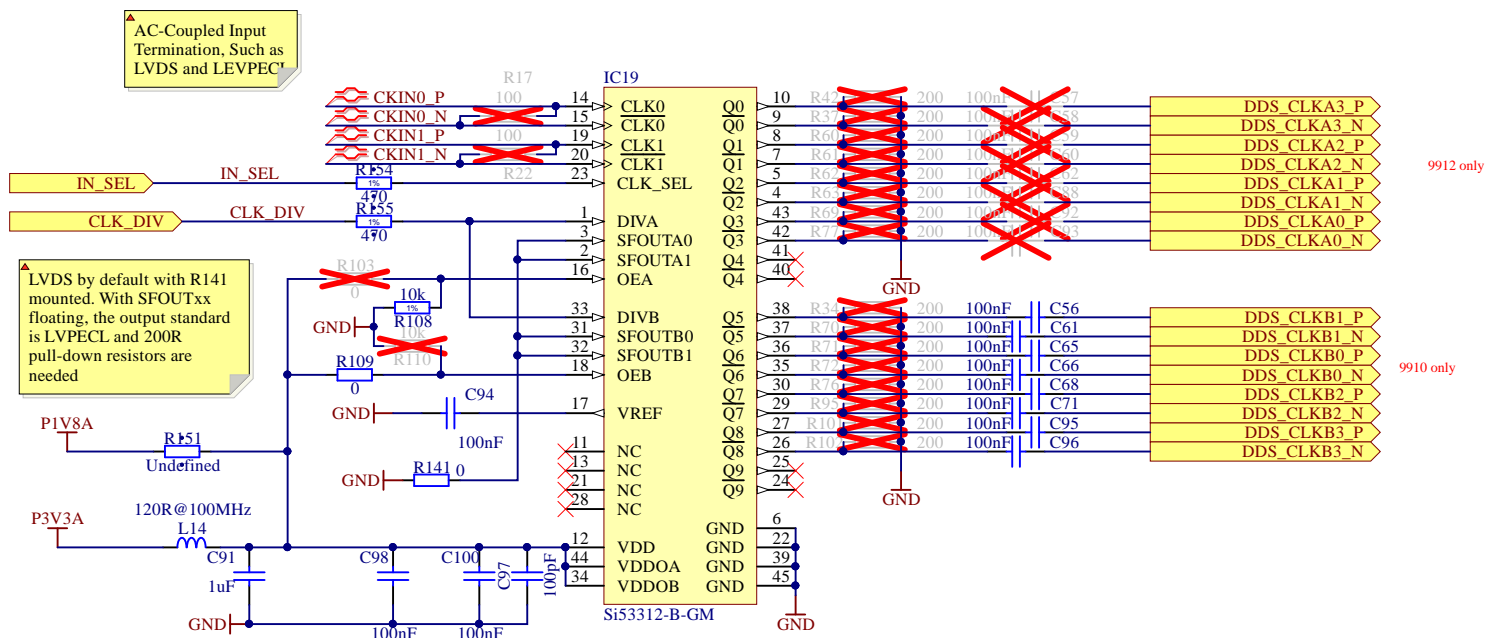
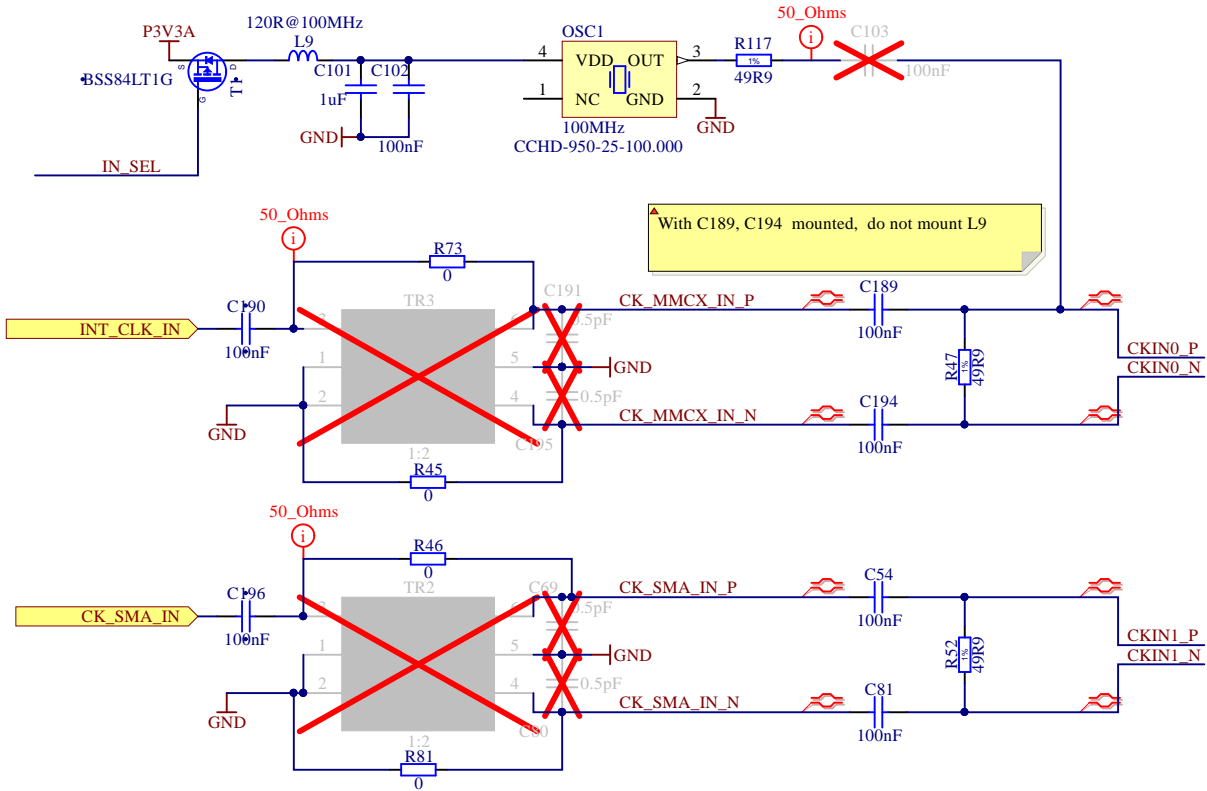
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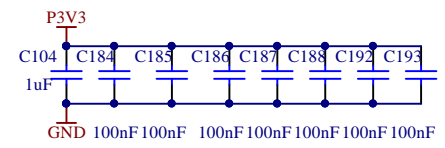
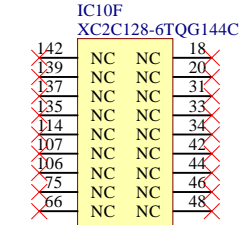
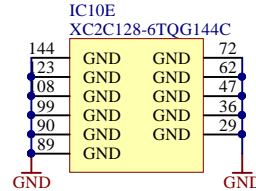
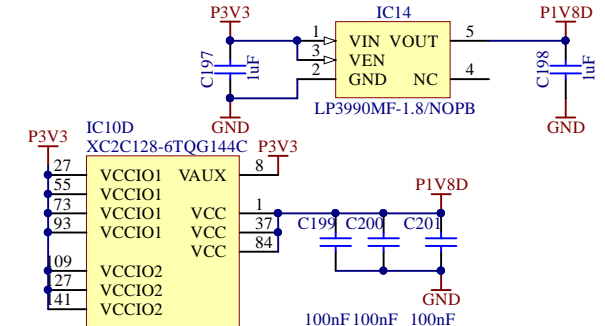
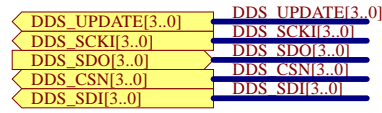
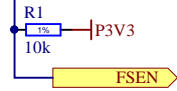
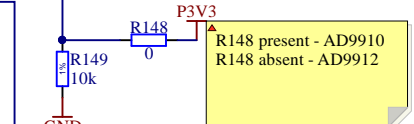
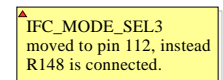
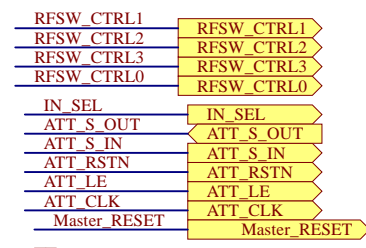
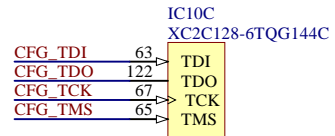
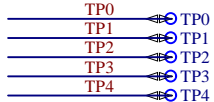
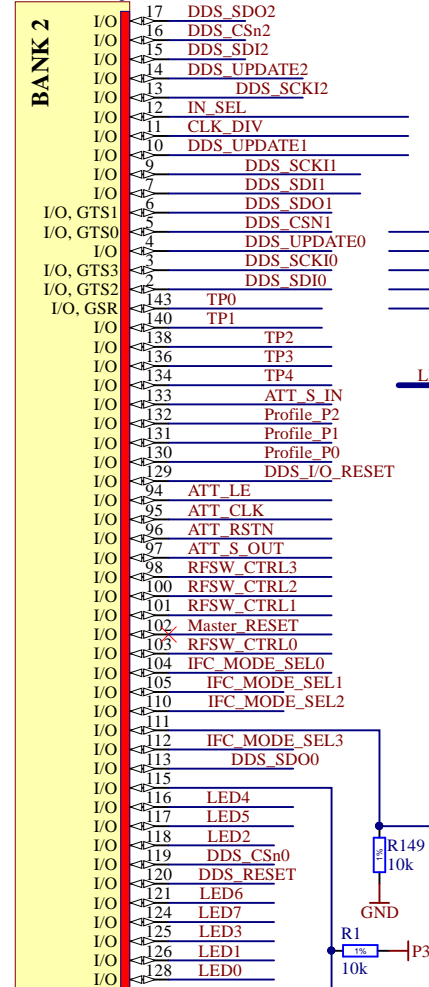
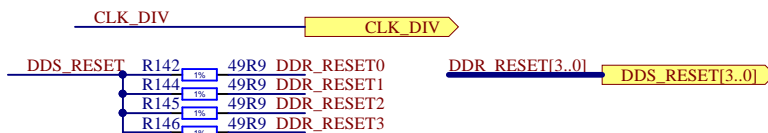
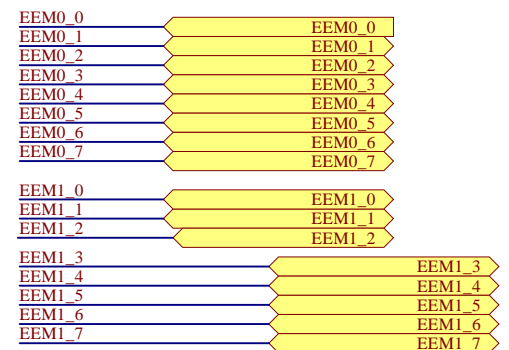
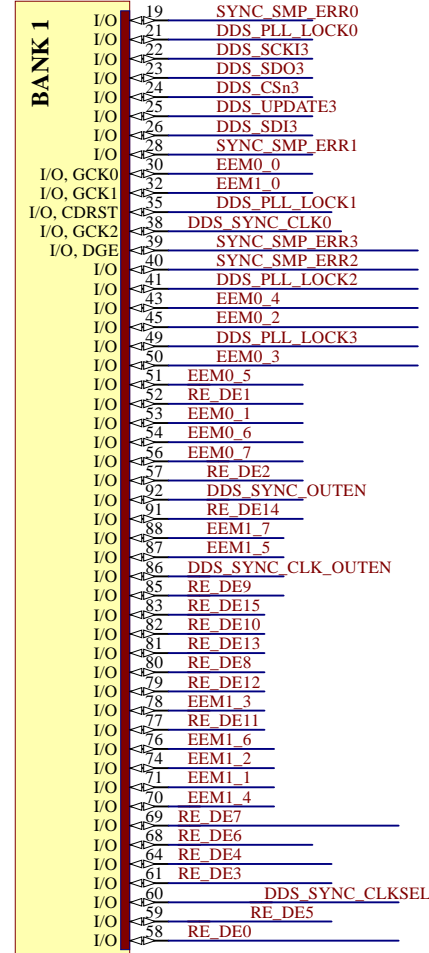


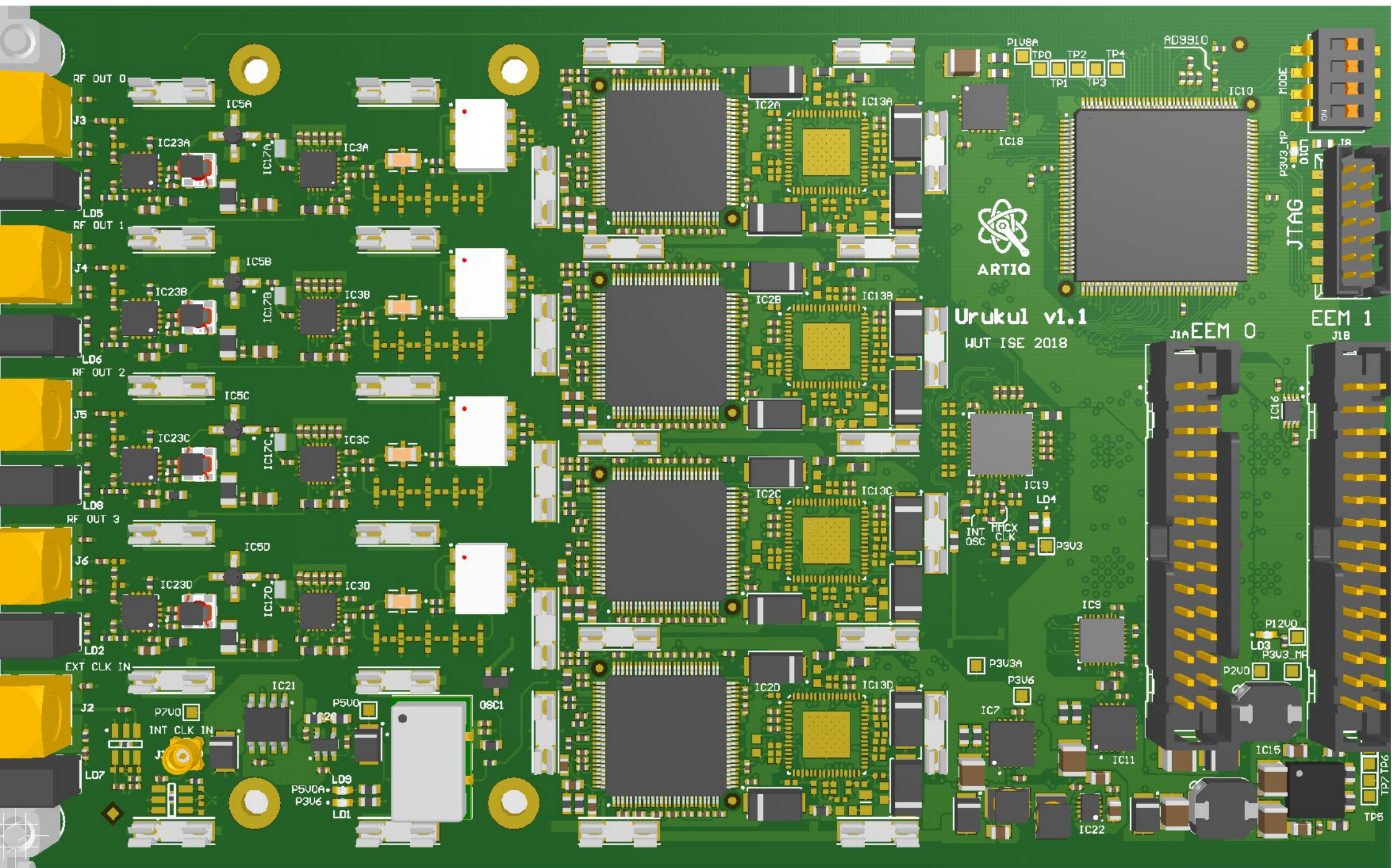
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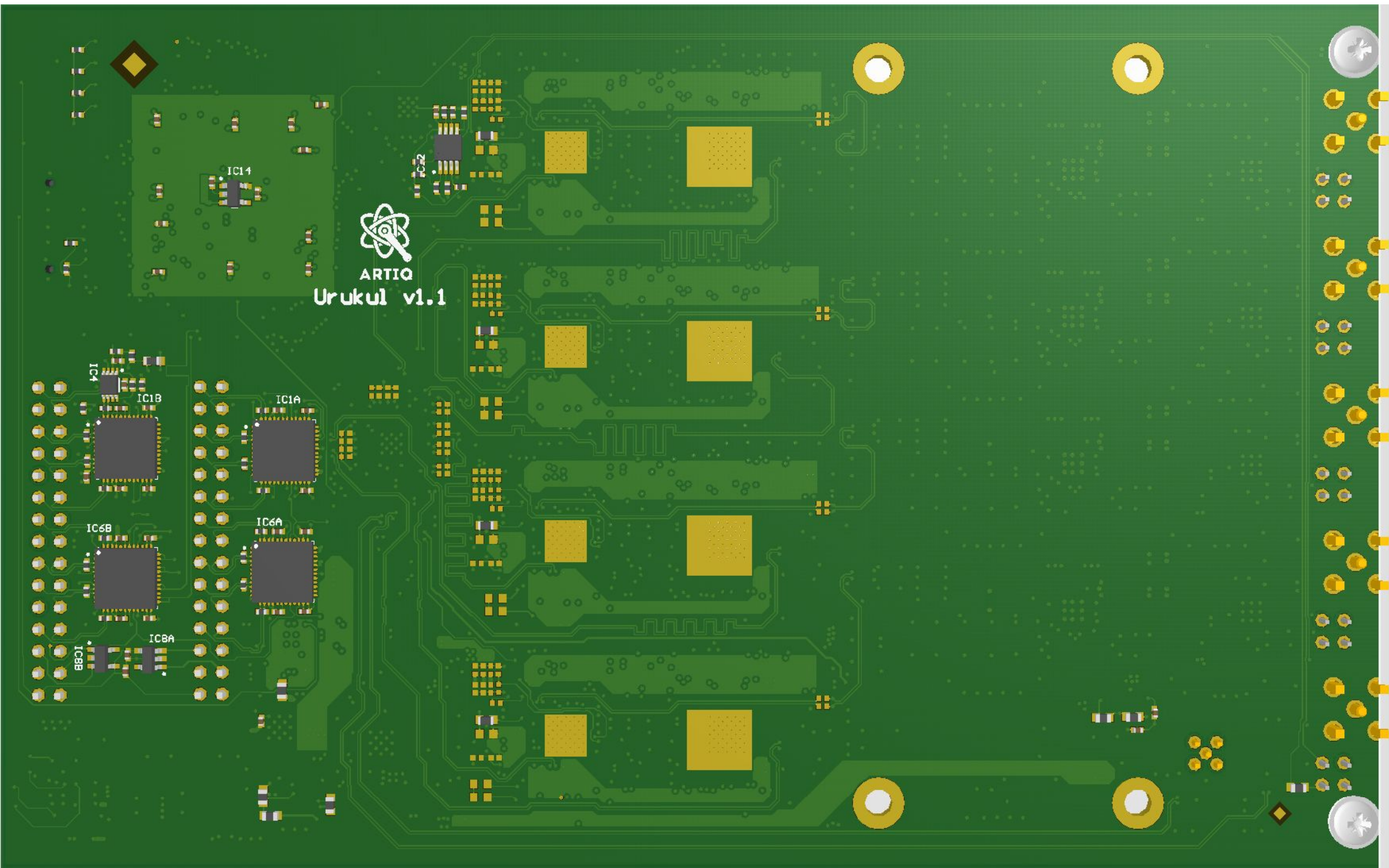


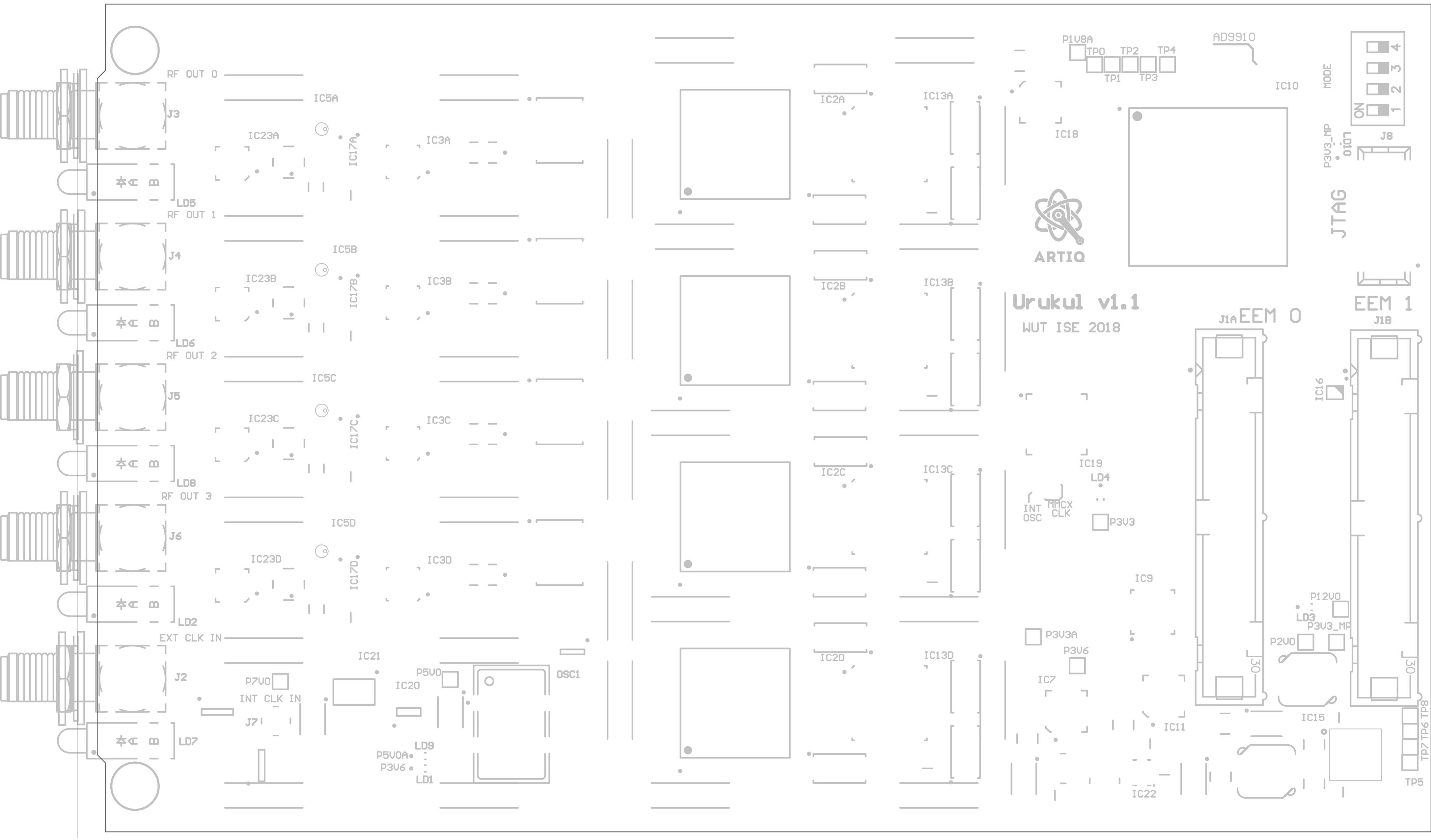
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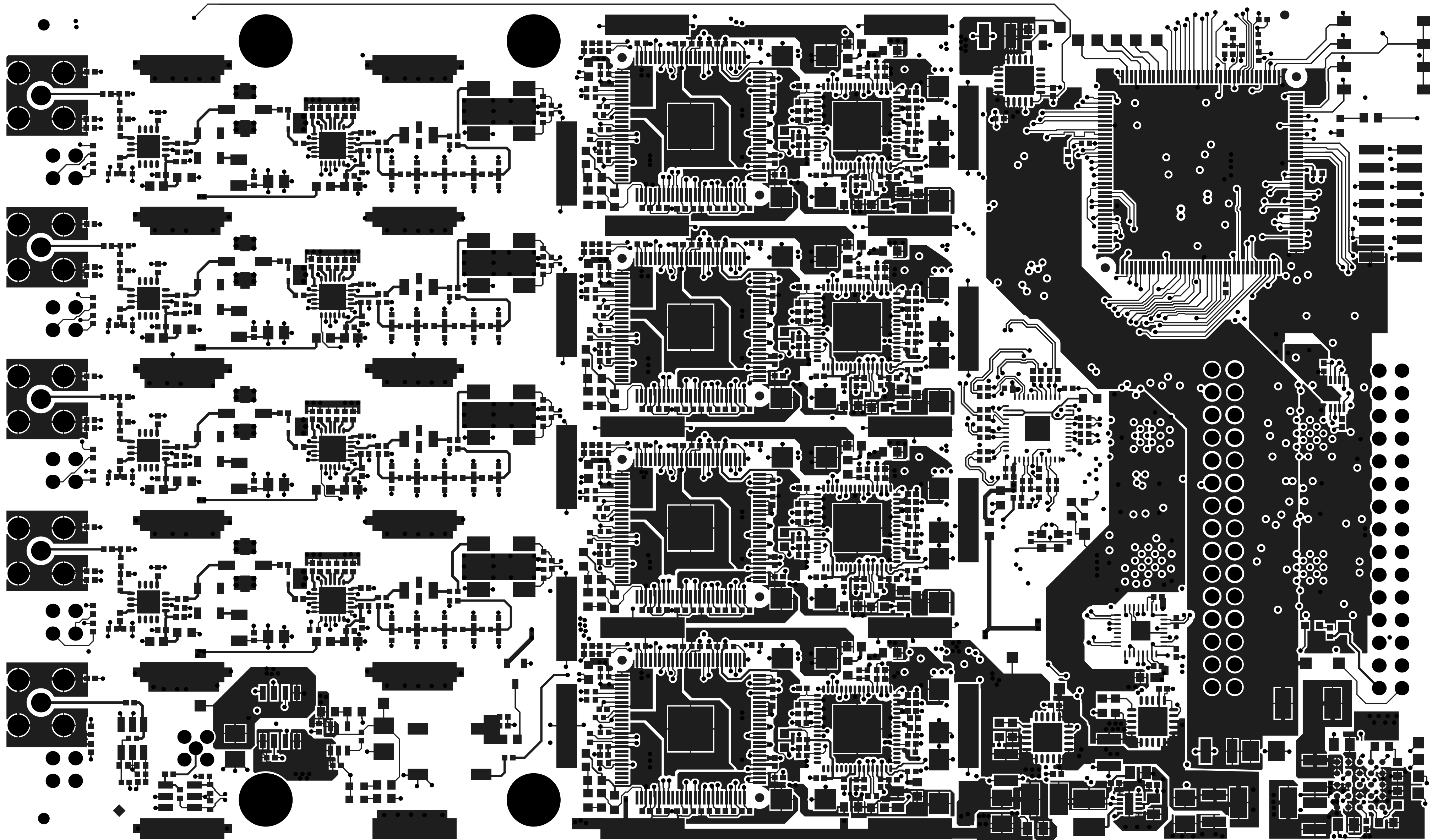
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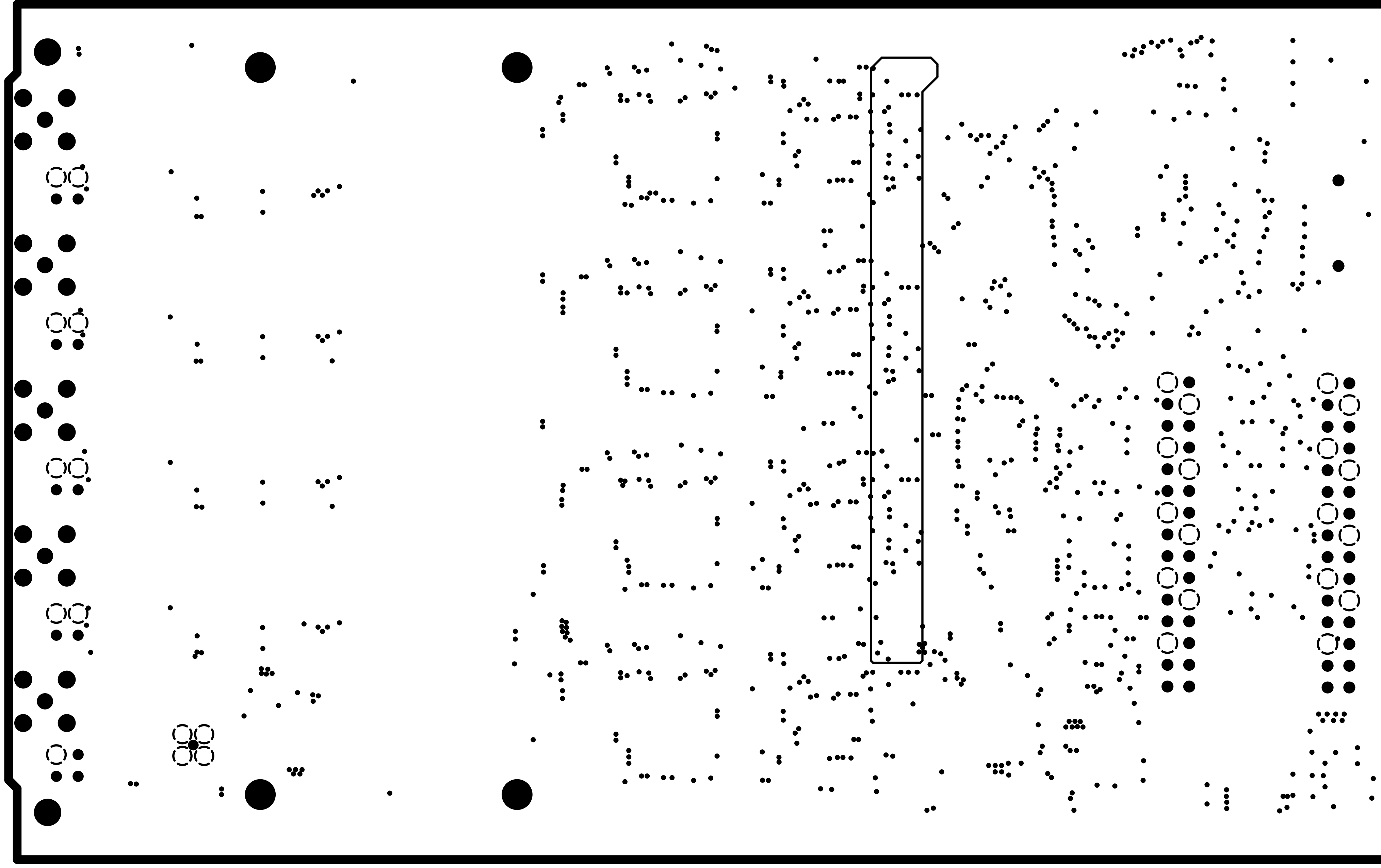


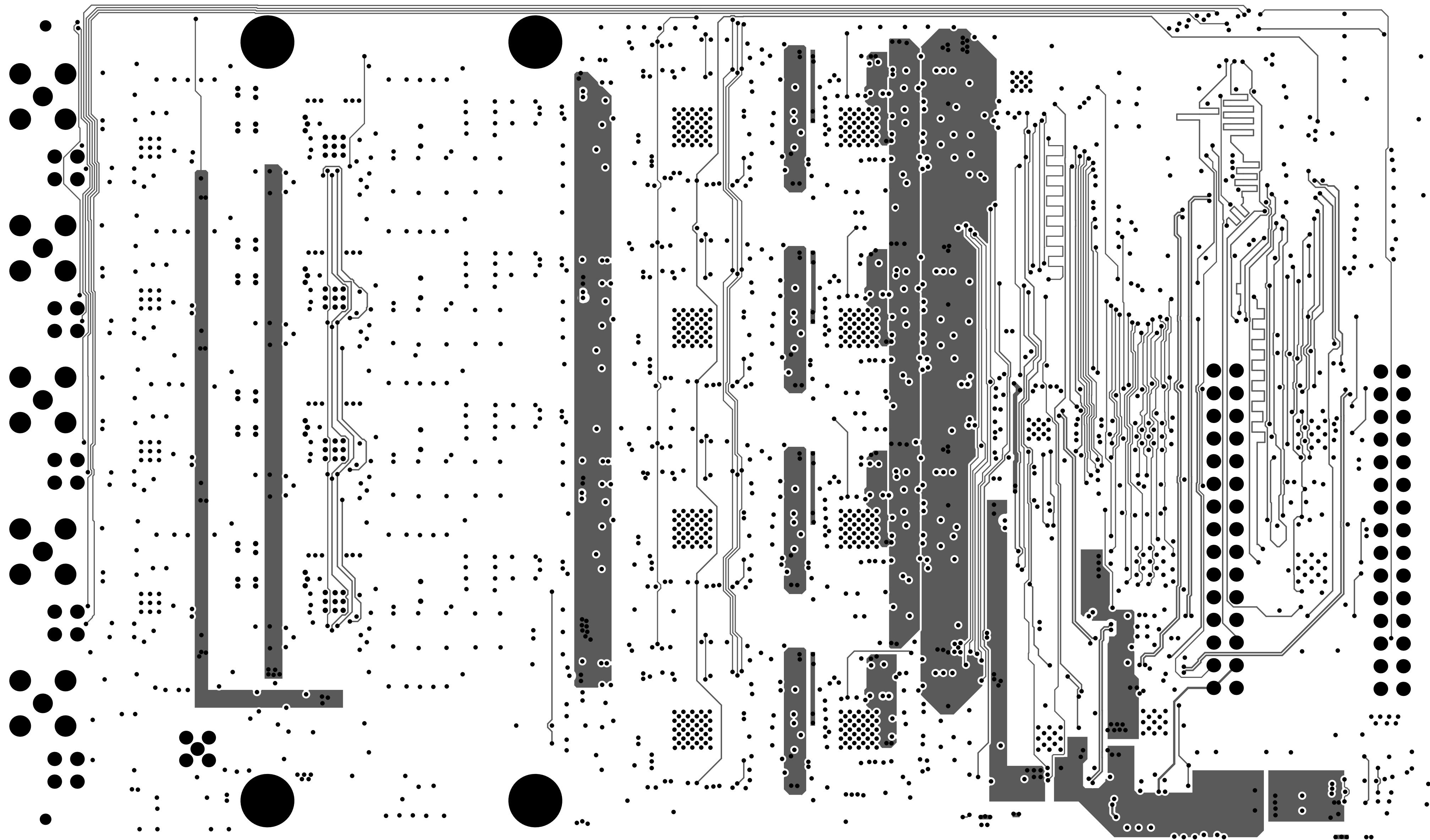


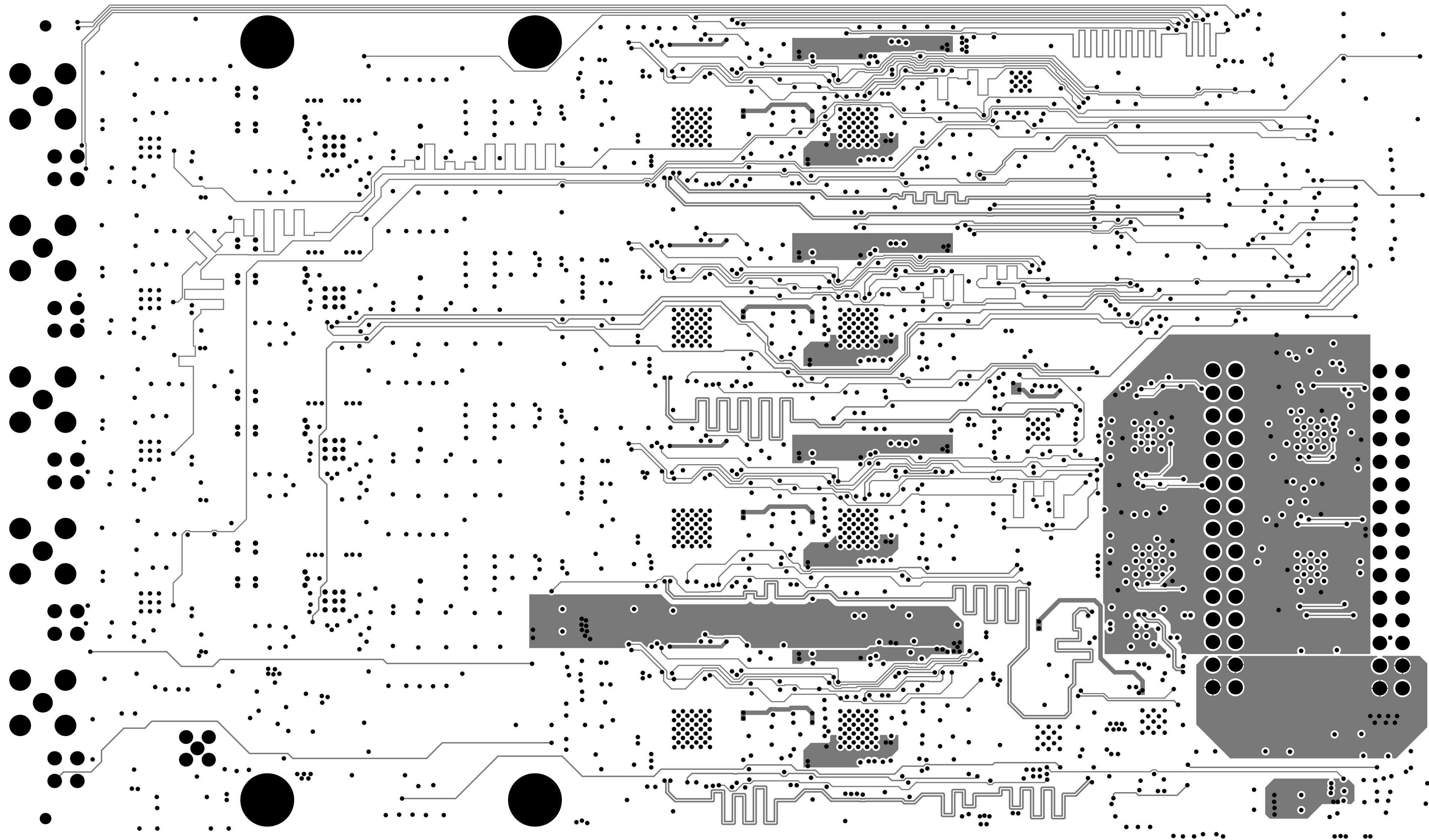


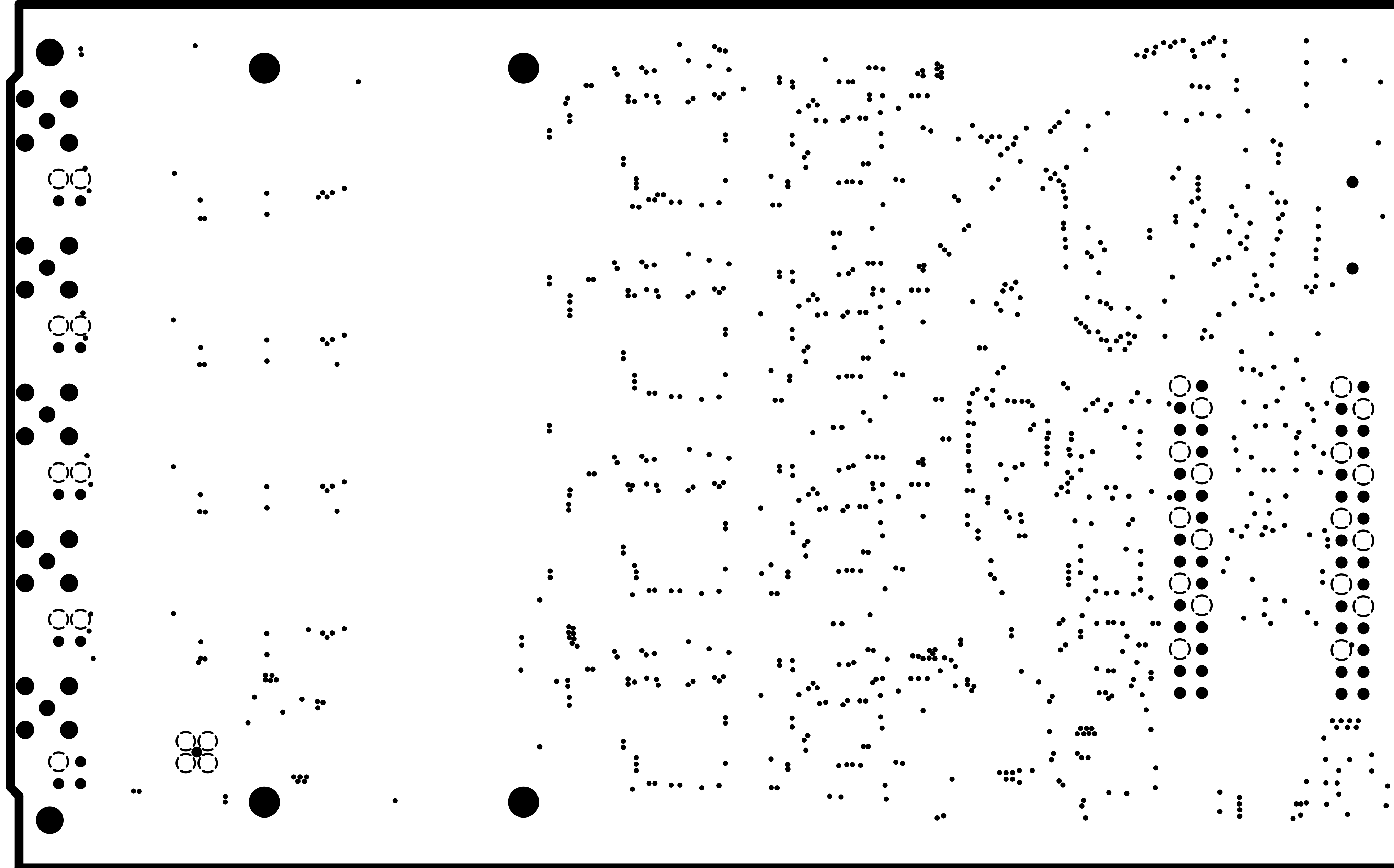


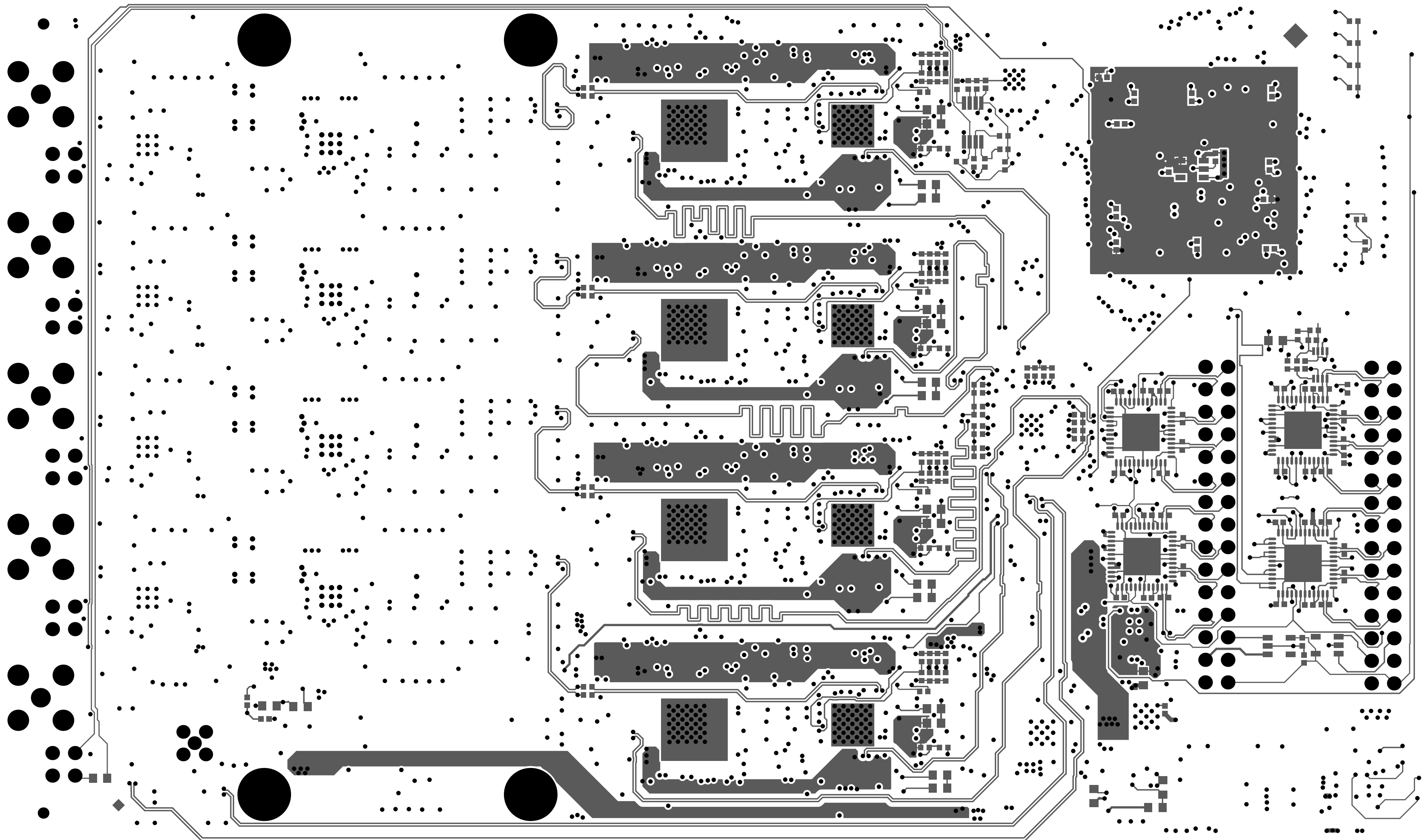














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