shield clips

CLIP1 CLIP2 CLIP3 CLIP4 CLIP5
CLIP6 CLIP7 CLIP8 CLIP9 CLIP10 CLIP27
CLIP11 CLIP12 CLIP13 CLIP14 CLIP15 CLIP28
CLIP16 CLIP17 CLIP18 CLIP19 CLIP20 CLIP29
CLIP21 CLIP22 CLIP23 CLIP24 CLIP25 CLIP26
(all GND)

Ext clock input

Clock from Kasli

Output SMAs

U_CLK_INPUT
CLK_INPUT.SchDoc

U_CTRL_LOGIC
CTRL_LOGIC.SchDoc

PLACE IT CLOSE TO LVDS Rx/Tx

PLACE IT CLOSE TO LVDS Rx/Tx

U_DDS_OUT_channel0
DDS_OUT_channel.SchDoc

U_DDS_OUT_channel1
DDS_OUT_channel.SchDoc

U_DDS_OUT_channel2
DDS_OUT_channel.SchDoc

U_DDS_OUT_channel3
DDS_OUT_channel.SchDoc

U_DDS_channel0
DDS_channel.SchDoc

U_DDS_channel1
DDS_channel.SchDoc

U_DDS_channel2
DDS_channel.SchDoc

U_DDS_channel3
DDS_channel.SchDoc

U_LVDS_IFC
LVDS_IFC_DDS.SchDoc
EEM A

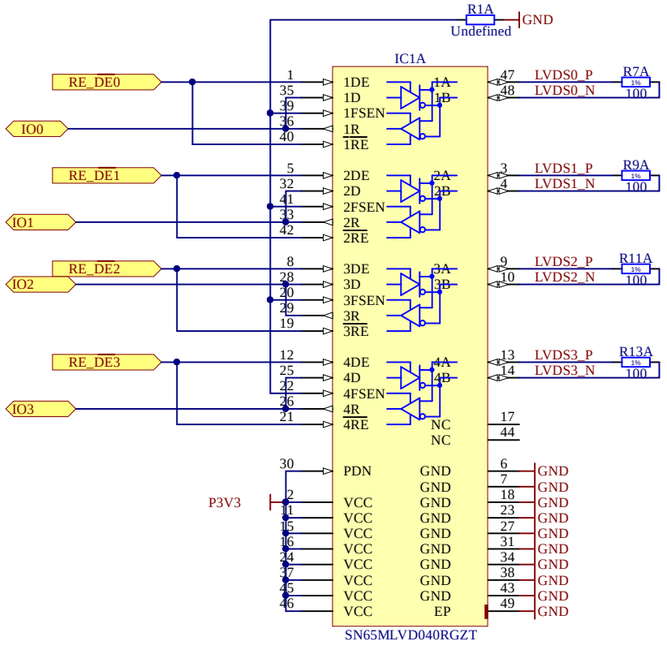
U_LVDS_IFC
LVDS_IFC_DDS.SchDoc
EEM B

U_Supply_DDS
Supply_DDS.SchDoc

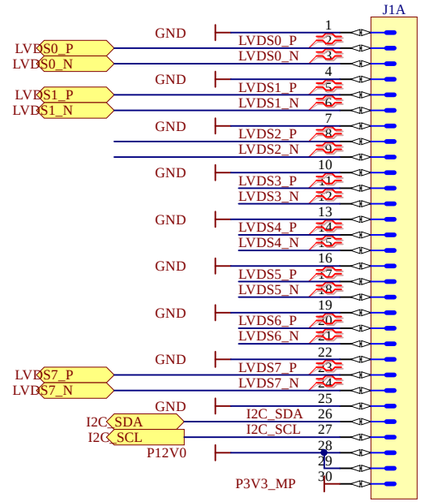
When routing please do a reasonable (100ps) length match within each of DDS_SYNC_CLK[3:0], DDS_UPDATE[3:0], RFSW_CTRL[3:0], IO[15:11] (nominally the RFSW_CTRL lines), DDS[3:0]_SYNC_IN, DDS_RESET and a really good one on DDS_CLK[3:0]_[PN].

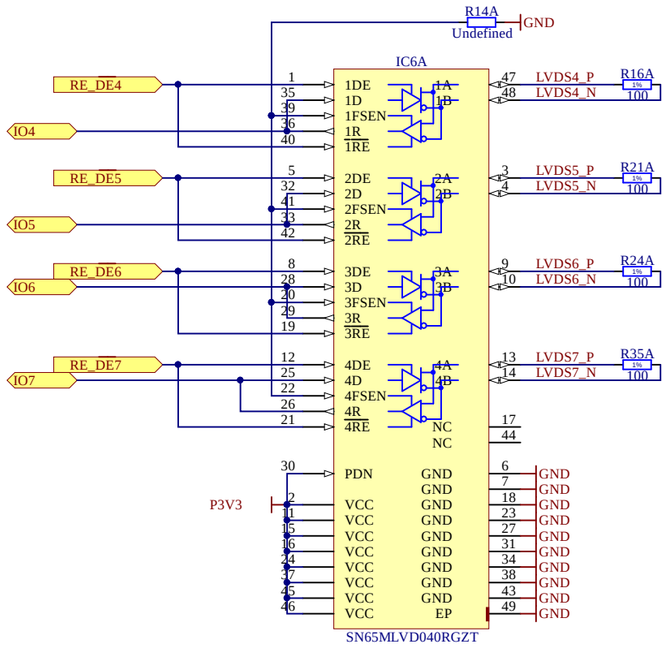
Project/Equipment	ARTIQ/SINARA
Document	3U DDS (URUKUL) Top entity
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	PCB_3U_DDS.schdoc
Print Date	17.09.2017 22:39:57 Sheet 1 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

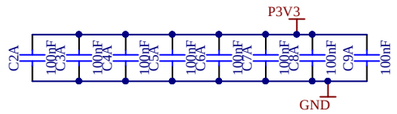
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

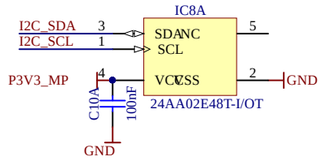


This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A



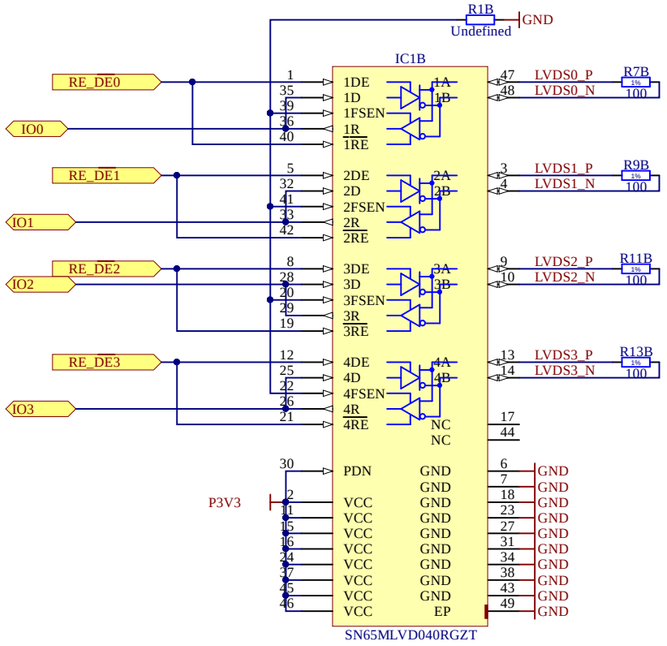




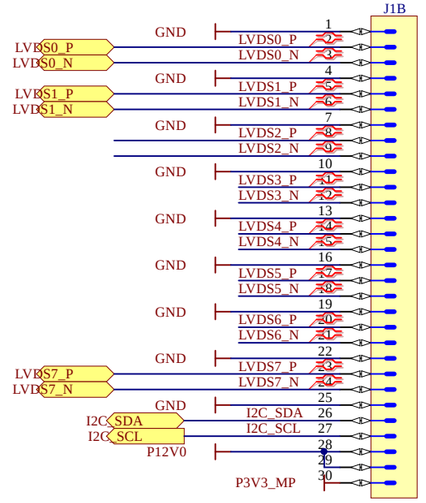


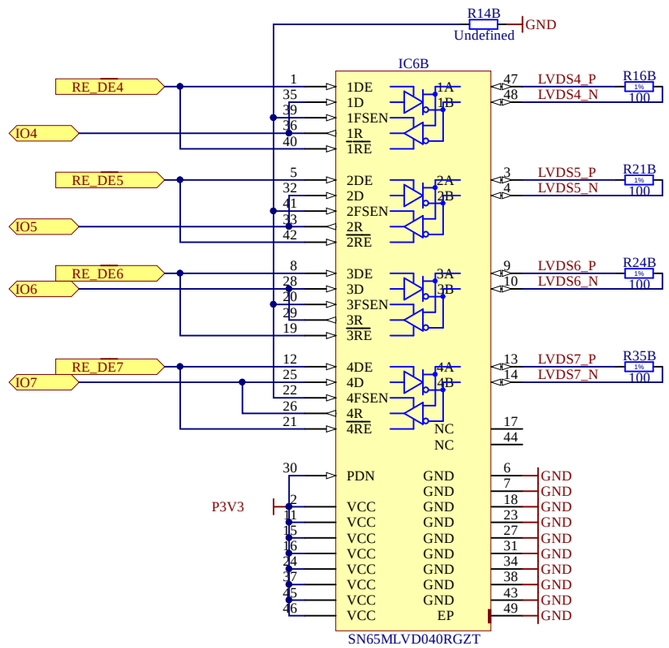
Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File LVDS_IFC_DDS.SchDoc	
		Print Date 17.09.2017 22:39:57	Sheet 2 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	*ISE*	ARTIQ	Size A3 / Rev -

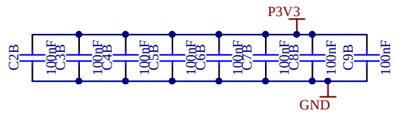
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

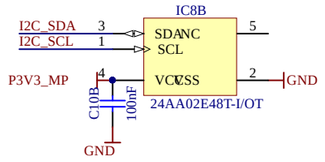


This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A

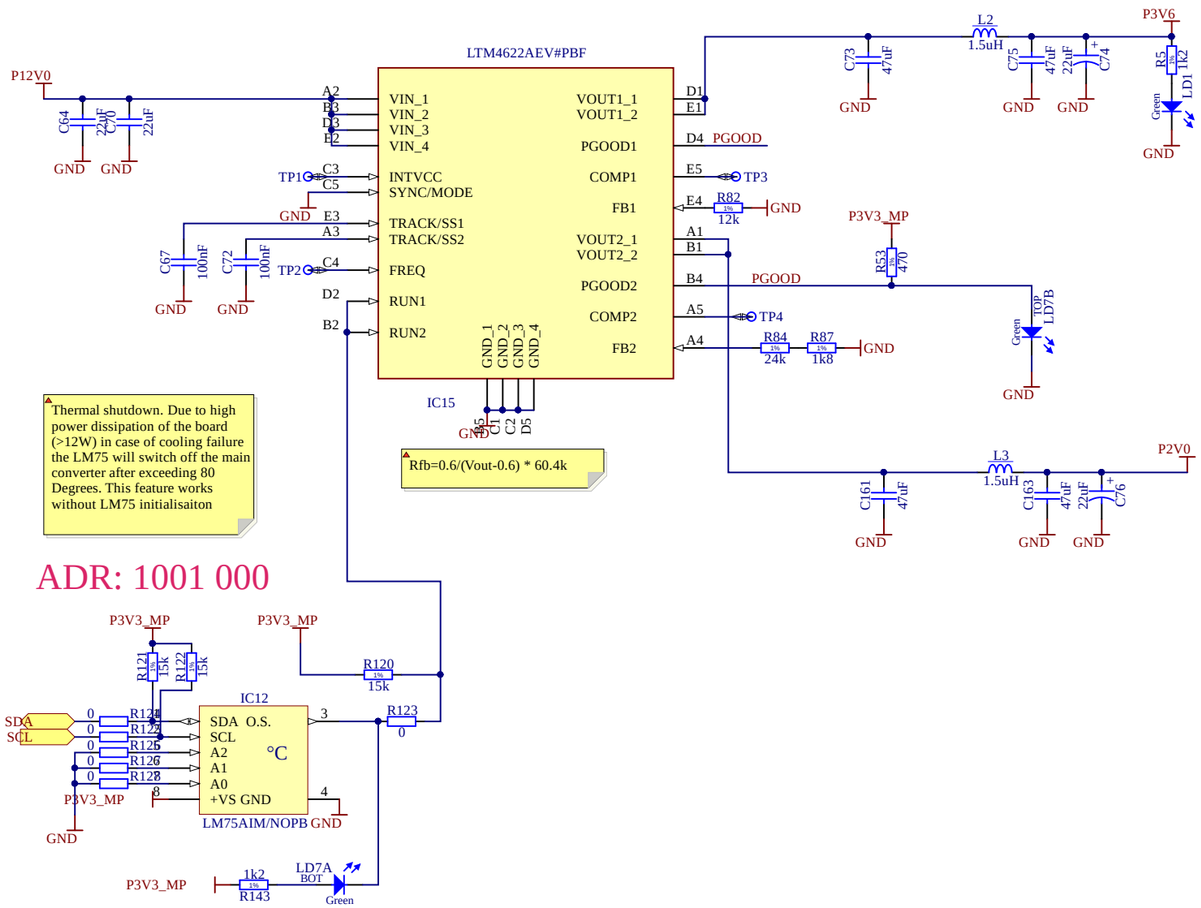








Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File LVDS_IFC_DDS.SchDoc	
		Print Date 17.09.2017 22:39:57	Sheet 2 of 7
Warsaw Univeristy of Technology *Nowowiejska 15/19*	*ISE*	ARTIQ	Size A3 / Rev -



Project/Equipment	ARTIQ/SINARA
Document	**Power supply DC/DC & LDOs**
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	Supply_DDS.SchDoc
Print Date	17.09.2017 22:39:58 Sheet 3 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

50_Ohms
C164A C203A R48A C172A C204A R49A C176A C205A R50A C180A C206A R51A C207A C202A 50_Ohms
0
Undefined
GND

DAC_OUT_N
DAC_OUT_P
49R9 9910 only
R38A
R39A
ADT1-1WT+ 1:1
TR1A
SEC PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible
R57A R59A Jumper
FL2A
IN OUT
DC to 320MHz
R58A C28A Jumper
Digital Attenuator

F clk max = 30MHz
IC3A
ATT_LE ATT_S_IN ATT_S_OUT ATT_CLK ATT_RSTn
LE S_IN S_OUT CLK RST
CONTROL INTERFACE
0.5dB 1dB 2dB 4dB 8dB 16dB
RF1 RF2
ACG1 ACG2 ACG3 ACG4 ACG5 ACG6 ACG7 VCC GND
NC
HMC542BLP4E
C14A C15A C16A C17A C18A C19A C20A 10nF
C36A 10nF

P5V0A L7A 390R@100MHz C21A 10uF C22A 100nF C23A 1nF C24A 100pF

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

PAT1220-C-9DB-T5 IC17A 9dB

R5 power = 65mA^2*39 = 0.16W

P7V0A R137A 100 C12A 1uF C27A 100nF L1TA TCCH-80+ 0.5uH@200mA
C55A 10nF
IC5A ERA-3+
C29A 10nF
R60A Undefined

SPDT switch
IC23A
RFC RF1 RF2 GND EN VCTL VDD NC
HMC349ALP4CE
RFSW_CTRL R20A 4k7
R138A 0
C49A C50A C47A 10nF
R2A R24A R44A Undefined
R18A R19A 100
RF_OUT
C38A 100pF C39A 10uF C40A 100nF L6A 390R@100MHz P5V0A

Amplifier
~23 dB gain and 13 dBm P1dB

Project/Equipment	ARTIQ/SINARA		
Document	**Output stage : Attenuator, amplifier and filter**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File DDS_OUT_channel.SchDoc	
		Print Date 17.09.2017 22:39:58	Sheet 4 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19 *ISE*	ARTIQ	Size A3	Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

50_Ohms
R48B 0
R49B 0
R50B 0
R51B 0
C164B C203B C172B C204B C176B C205B C180B C206B C202B C207B
Undefined

DAC_OUT_N
DAC_OUT_P
49R9 9910 only
R38B
R39B
ADT1-1WT+ 1:1
TR1B
9912 devkit uses ADT2-1T-1P wich is footprint compatible
R57B 0
R59B 0
Jumper
FL2B
DC to 320MHz
R58B 0
10nF C28B
Jumper

Digital Attenuator

F clk max = 30MHz

IC3B
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB 1dB 2dB 4dB 8dB 16dB
RF1
RF2
ACG1 ACG2 ACG3 ACG4 ACG5 ACG6 ACG7
NC
VCC GND
HMC542BLP4E
C14B C15B C16B C17B C18B C19B C20B 10nF
C36B 10nF
P5V0A
L7B 390R@100MHz
C21B 10uF
C22B 100nF
C23B 1nF
C24B 100pF

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

PAT1220-C-9DB-T5
IC17B 9dB

R5 power = 65mA^2*39 = 0.16W

P7V0A
R137B 100
C12B 1uF
C27B 100nF
L1B TCCH-80+ 0.5uH@200mA
C55B 10nF
IC5B
ERA-3+
C29B 10nF
R54B Undefined

Amplifier
~23 dB gain and 13 dBm P1dB

SPDT switch

IC23B
RFSW_CTRL
R200B 4k7
R138B 0
RFC
RF1 RF2
EN VCTL VDD
NC
HMC349ALP4E
C49B 10nF
R2B 0
C50B 10nF
RF_OUT
C47B 10nF
R18B 100
R19B 100
L6B 390R@100MHz
C38B 100pF
C39B 10uF
C40B 100nF

Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter

Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	DDS_OUT_channel.SchDoc
Print Date	17.09.2017 22:39:58 Sheet 4 of 7

Warsaw Univeristy of Technology ISE
Nowowiejska 15/19

ARTIQ Size A3 Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

50_Ohms
C164C Undefined
R48C 0
C172C Undefined
R49C 0
C176C Undefined
R50C 0
C180C Undefined
R51C 0
C202C Undefined
C203C Undefined
C204C Undefined
C205C Undefined
C206C Undefined
C207C Undefined
GND

DAC_OUT_N
DAC_OUT_P
49R9 1% 9910 only
R38C 100
ADT1-1WT+ 1:1
TR1C SEC PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible

R57C 0
R59C 0
Jumper
FL2C IN OUT
DC to 320MHz
R58C 0
10nF C28C
Jumper

Digital Attenuator

F clk max = 30MHz

IC3C HMC542BLP4E
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB 1dB 2dB 4dB 8dB 16dB
RF1
RF2
ACG1 ACG2 ACG3 ACG4 ACG5 ACG6 ACG7
NC
VCC GND
C14C 10nF
C15C 10nF
C16C 10nF
C17C 10nF
C18C 10nF
C19C 10nF
C20C 10nF
C36C 10nF

P5V0A
L7C 390R@100MHz
C21C 10uF
C22C 100nF
C23C 1nF
C24C 100pF

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

PAT1220-C-9DB-T5 IC17C 9dB

R5 power = 65mA^2*39 = 0.16W

P7V0A
R137C 100
C12C 1uF
C27C 100nF
L1TC TCCH-80+ 0.5uH@200mA
C55C 10nF
IC5C ERA-3+
C29C 10nF
R52C Undefined

Amplifier
~23 dB gain and 13 dBm P1dB

SPDT switch

IC23C HMC349ALP4CE
RFC RF1 RF2 GND
EN VCTL VDD
NC
RFSW_CTRL
R20C 4k7
R138C 0
C49C 10nF
R2C 0
C50C 10nF
RF_OUT
C47C 10nF
R18C 100
R19C 100
L6C 390R@100MHz
C38C 100pF
C39C 10uF
C40C 100nF

Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter

Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	DDS_OUT_channel.SchDoc
Print Date	17.09.2017 22:39:59 Sheet 4 of 7

Warsaw Univeristy of Technology ISE
Nowowiejska 15/19

ARTIQ Size A3 Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

Jumper

Jumper

Digital Attenuator

F clk max = 30MHz

HMC542BLP4E

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R5 power = 65mA^2*39 = 0.16W

SPDT switch

HMC349ALP4CE

Amplifier
~23 dB gain and 13 dBm P1dB

Project/Equipment	ARTIQ/SINARA		
Document	**Output stage : Attenuator, amplifier and filter**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File	DDS_OUT_channel.SchDoc
		Print Date 17.09.2017 22:39:59	Sheet 4 of 7
Warsaw Univeristy of Technology ISE *Nowowiejska 15/19*	ARTIQ	Size A3	Rev -

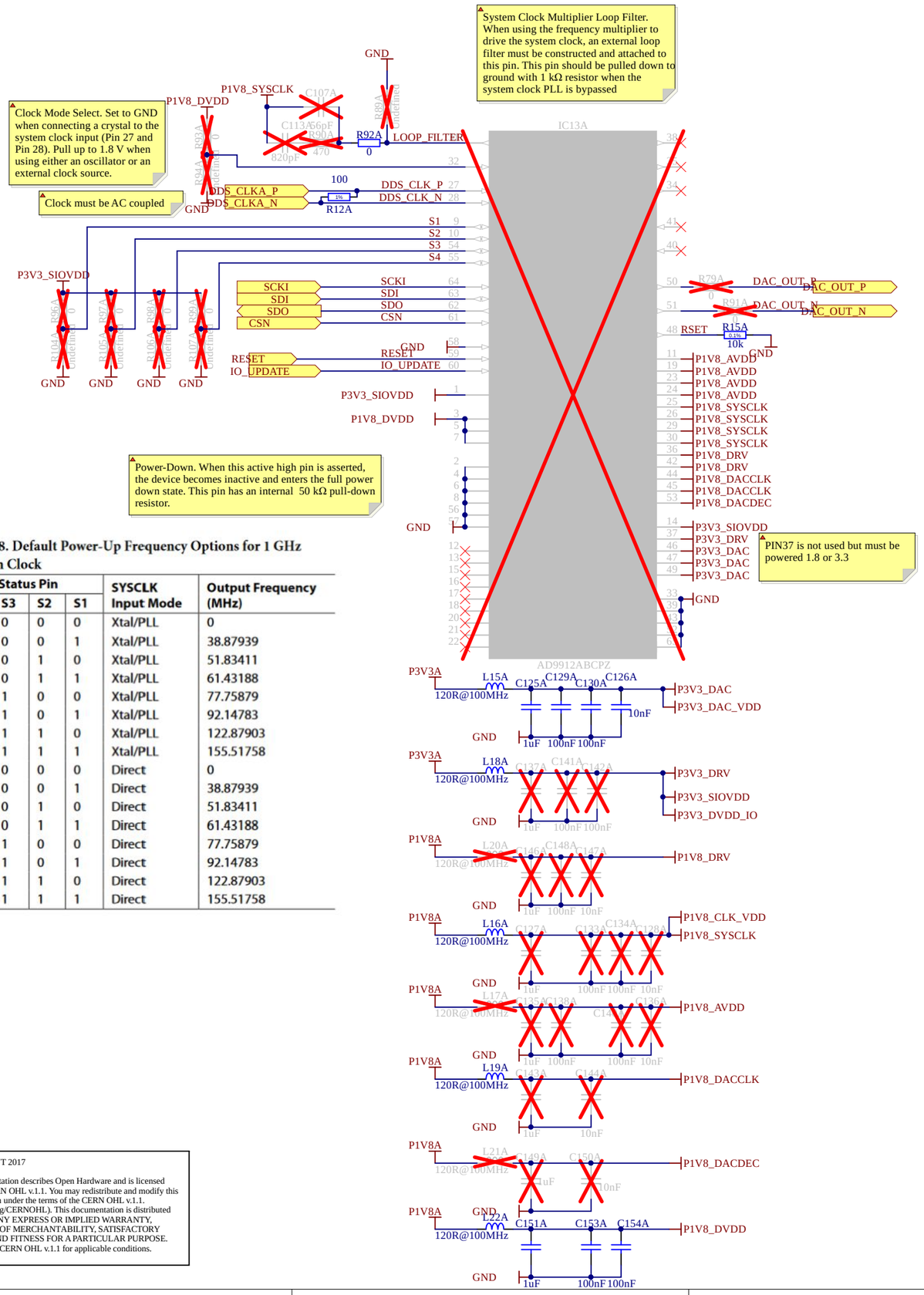
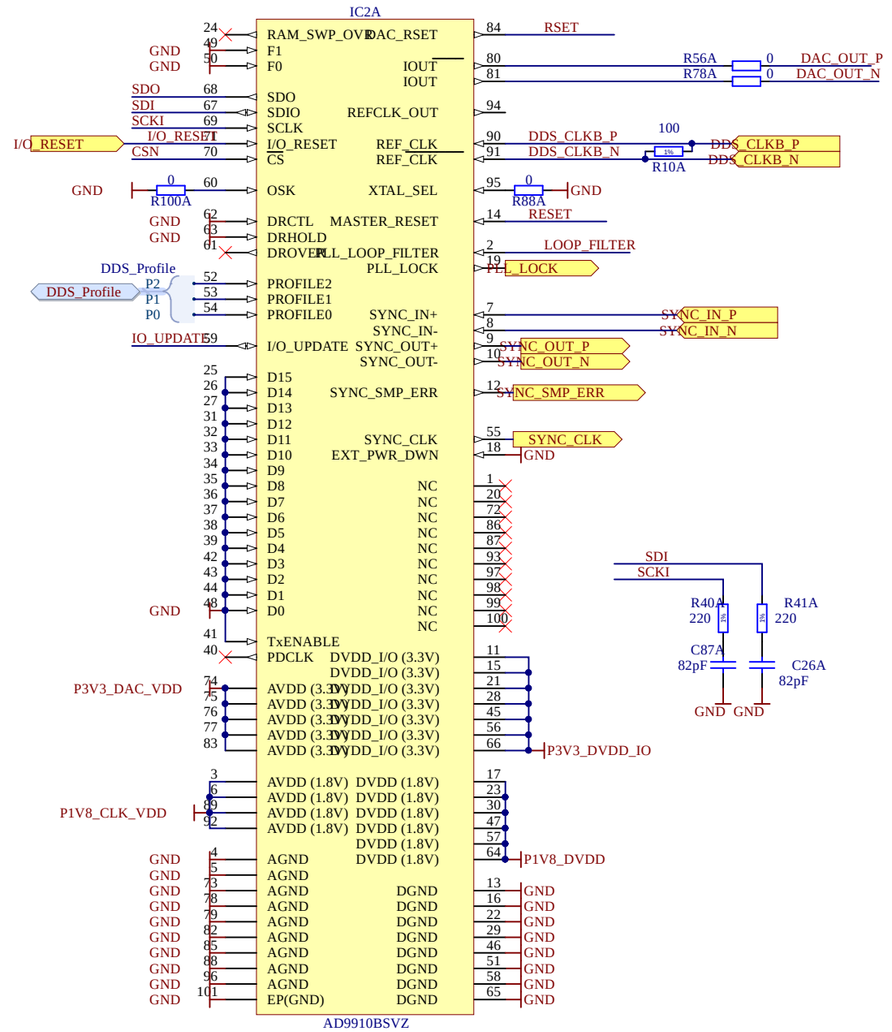
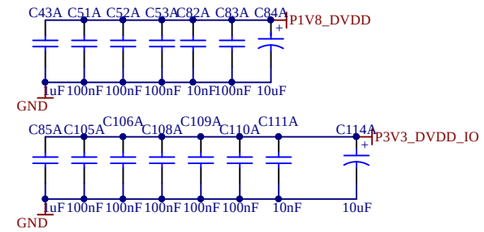
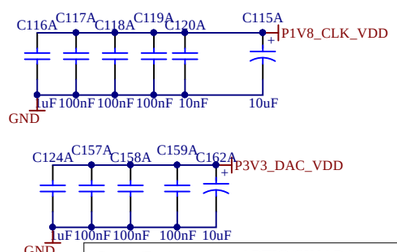


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758







Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	DDS_channel.SchDoc
Print Date	17.09.2017 22:39:59 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

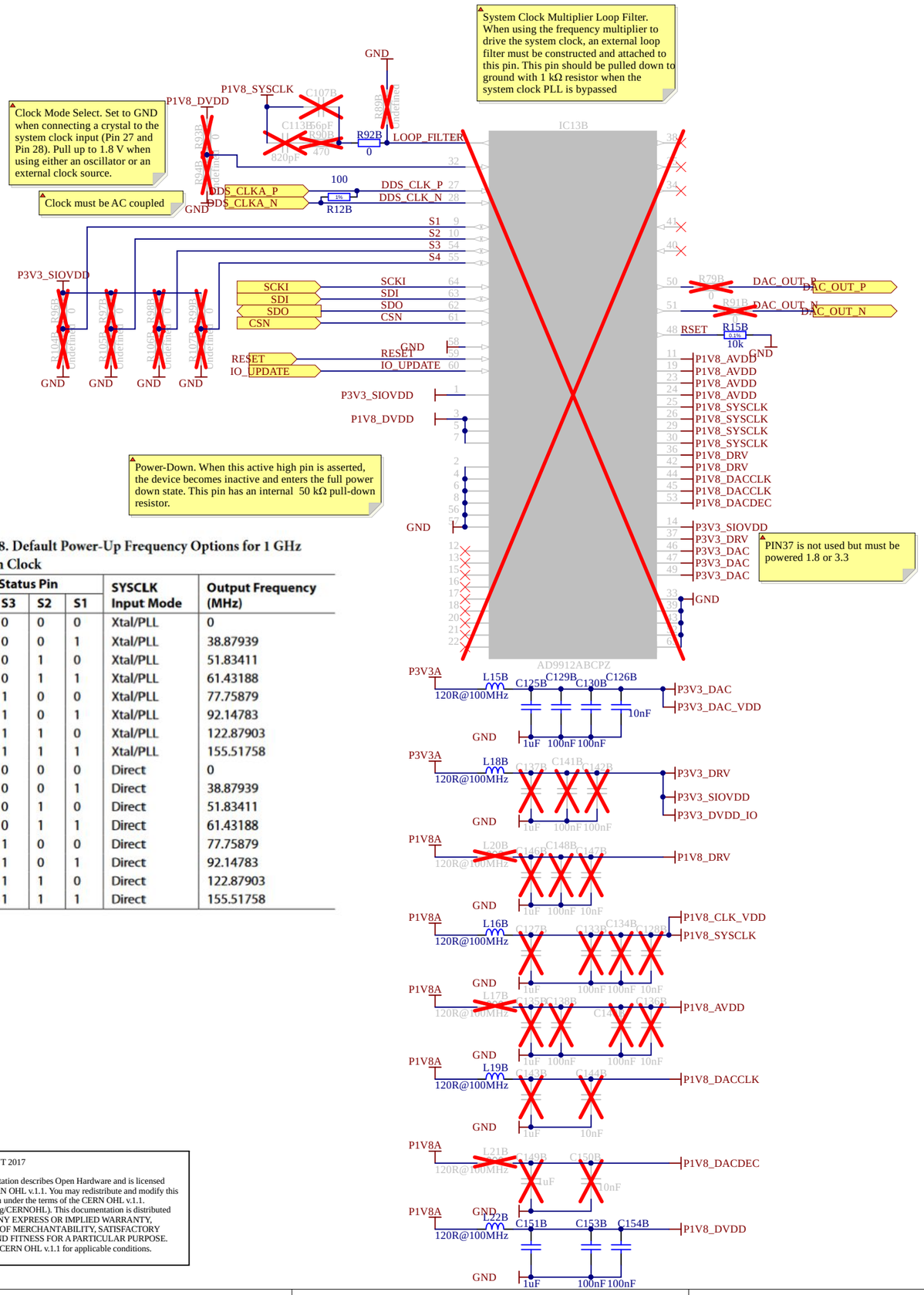
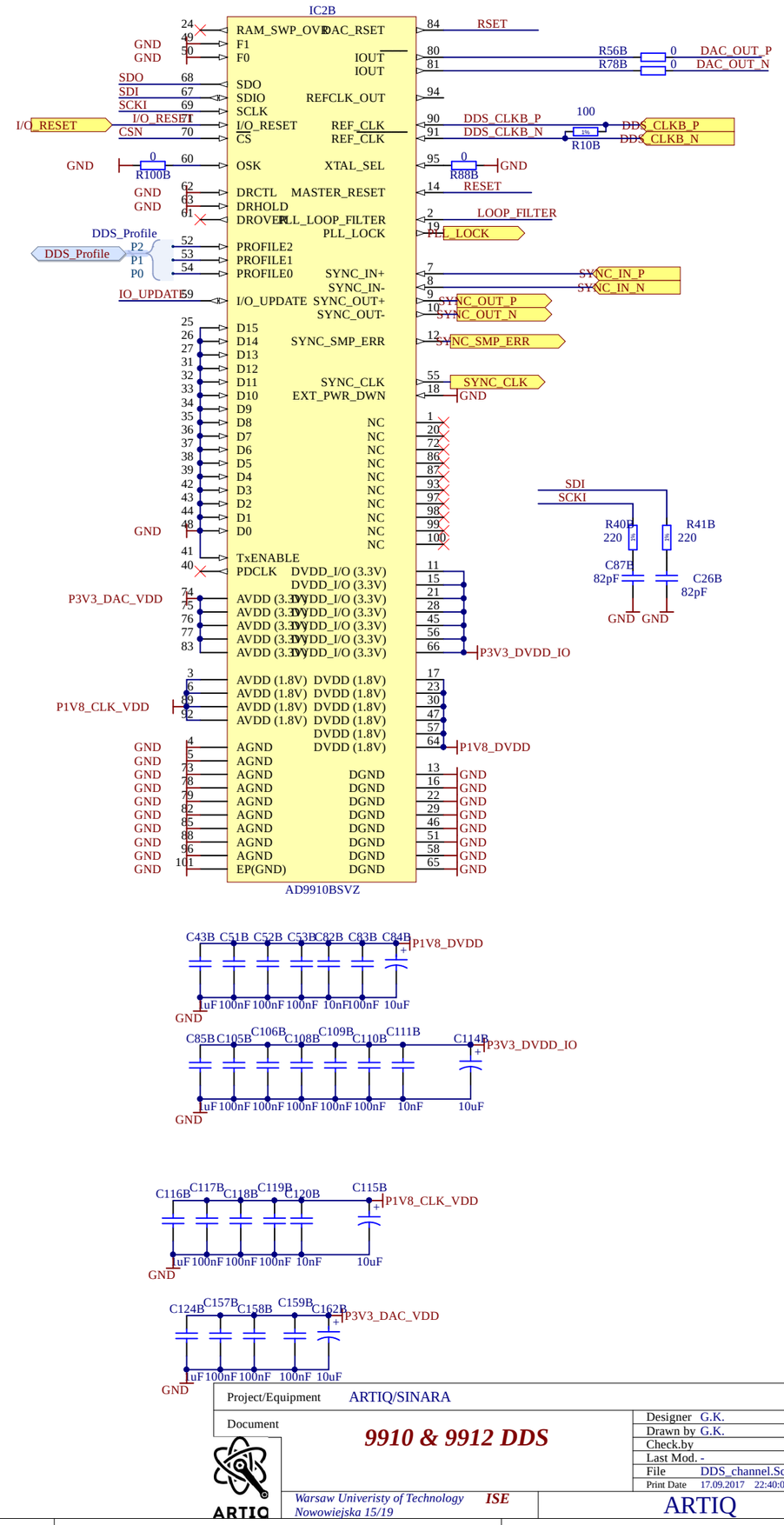


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK	Output Frequency
S4	S3	S2	S1	Input Mode	(MHz)
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758



Project/Equipment: ARTIQ/SINARA

Document: **9910 & 9912 DDS**

Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	DDS_channel.SchDoc
Print Date	17.09.2017 22:40:00 Sheet 5 of 7

Warsaw Univeristy of Technology *ISE*
Nowowiejska 15/19

ARTIQ

Size A3 | Rev -

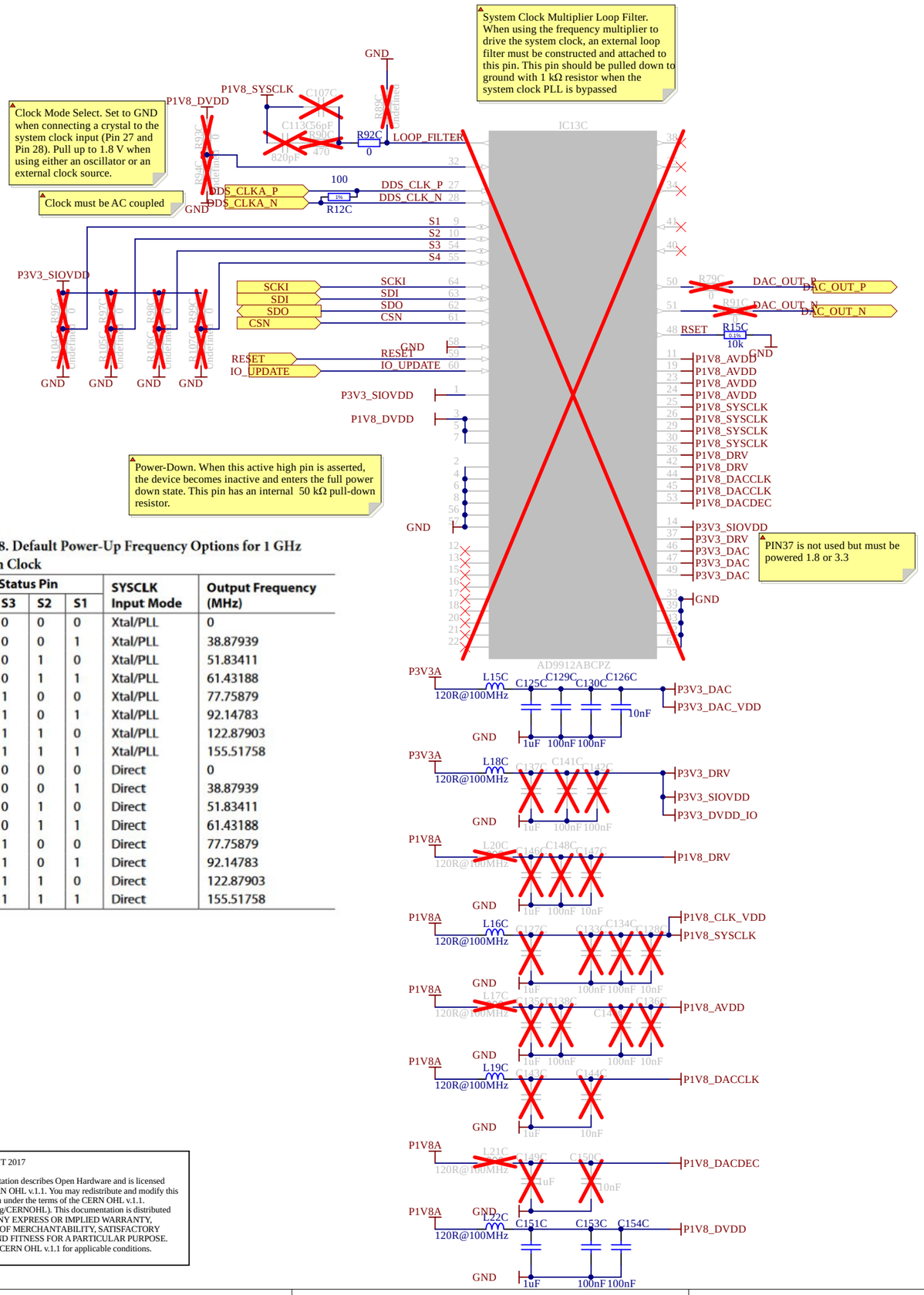
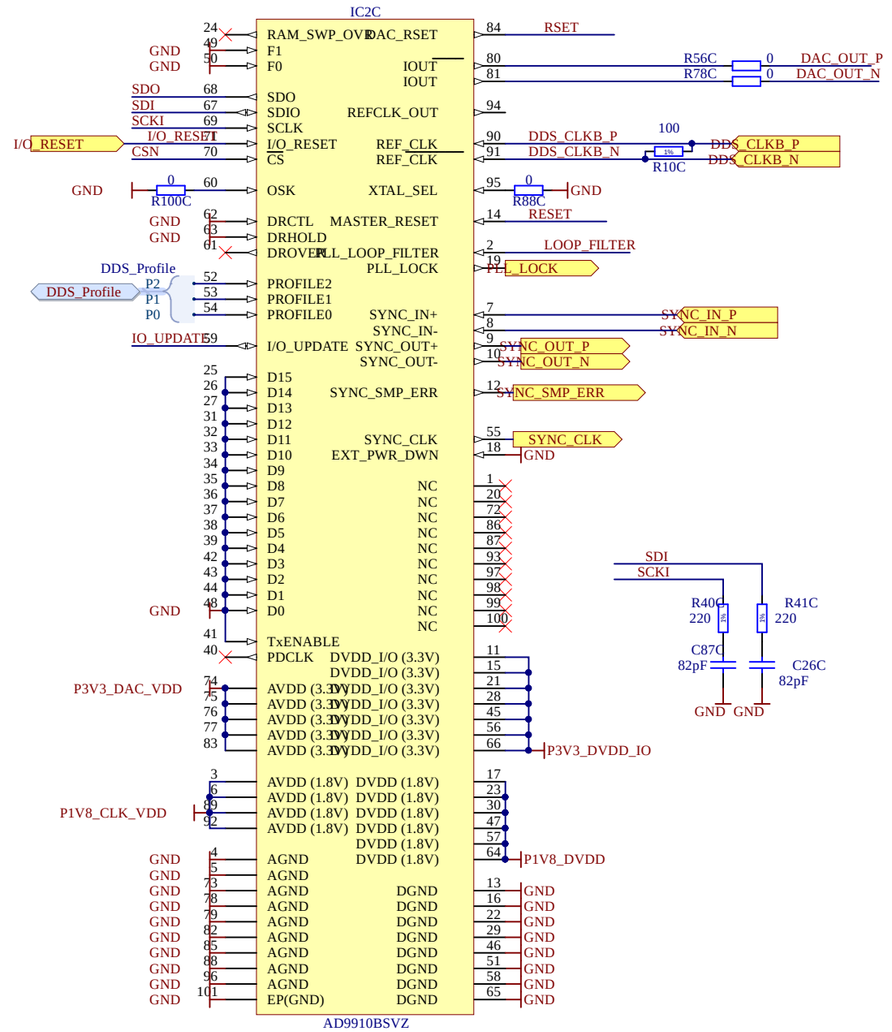
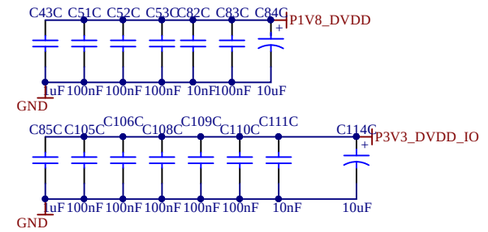


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK	Output Frequency
S4	S3	S2	S1	Input Mode	(MHz)
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758





Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	DDS_channel.SchDoc
Print Date	17.09.2017 22:40:00 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

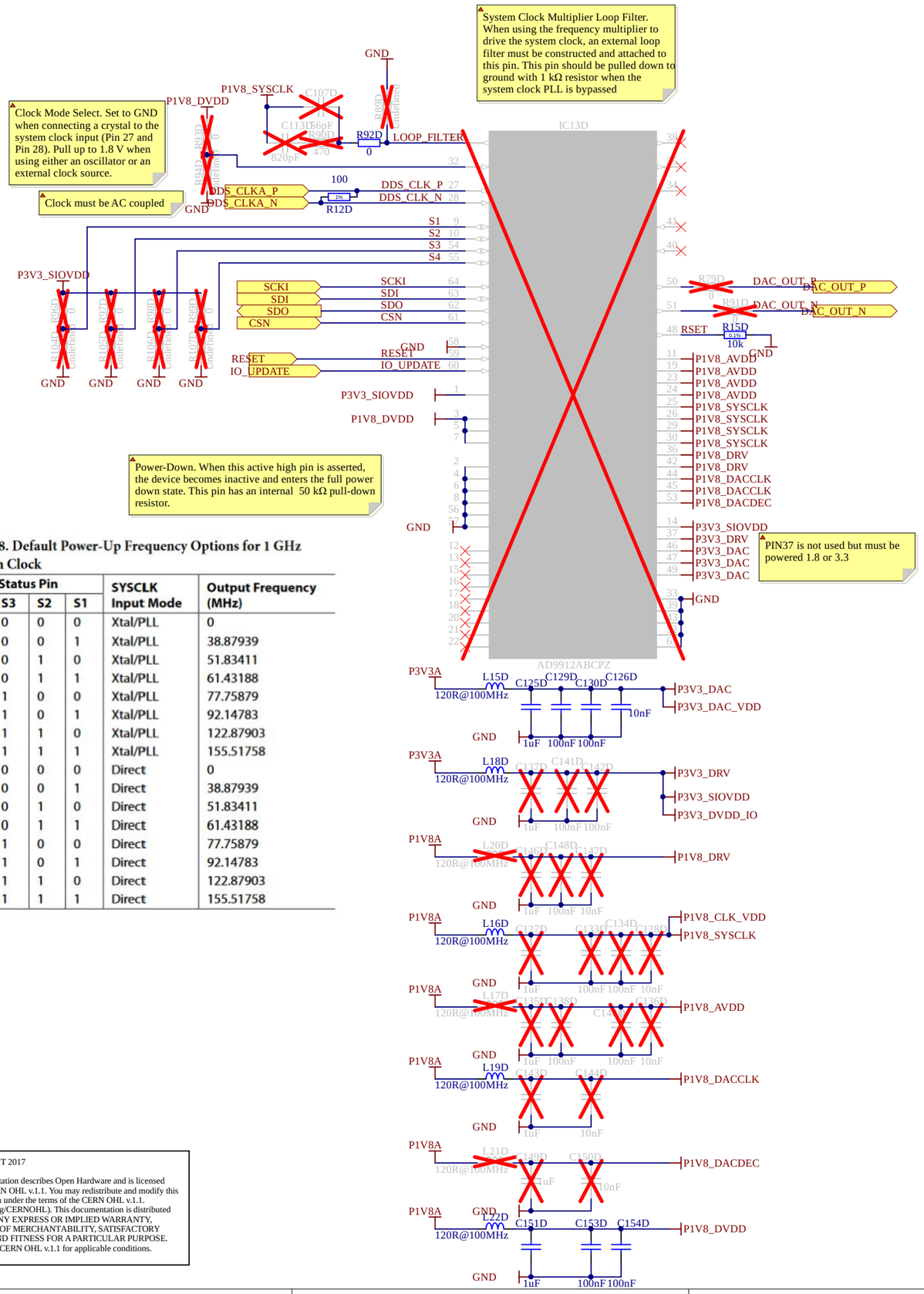


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
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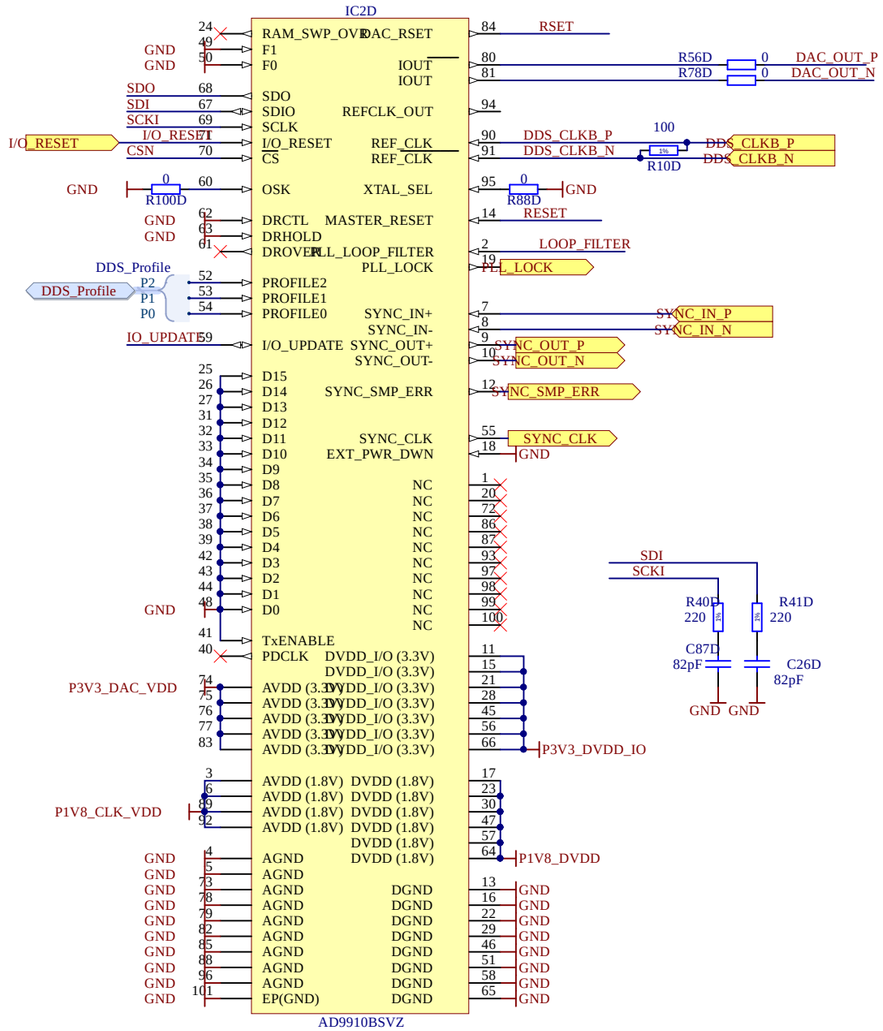
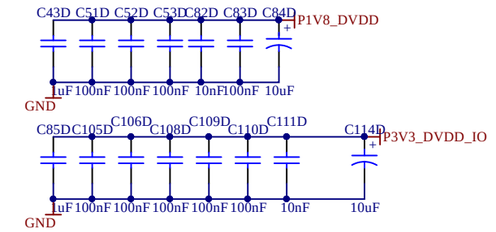
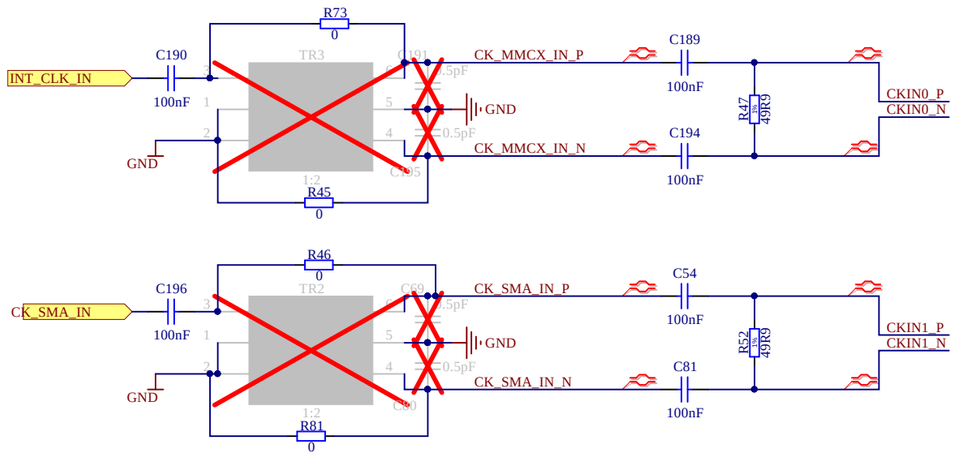
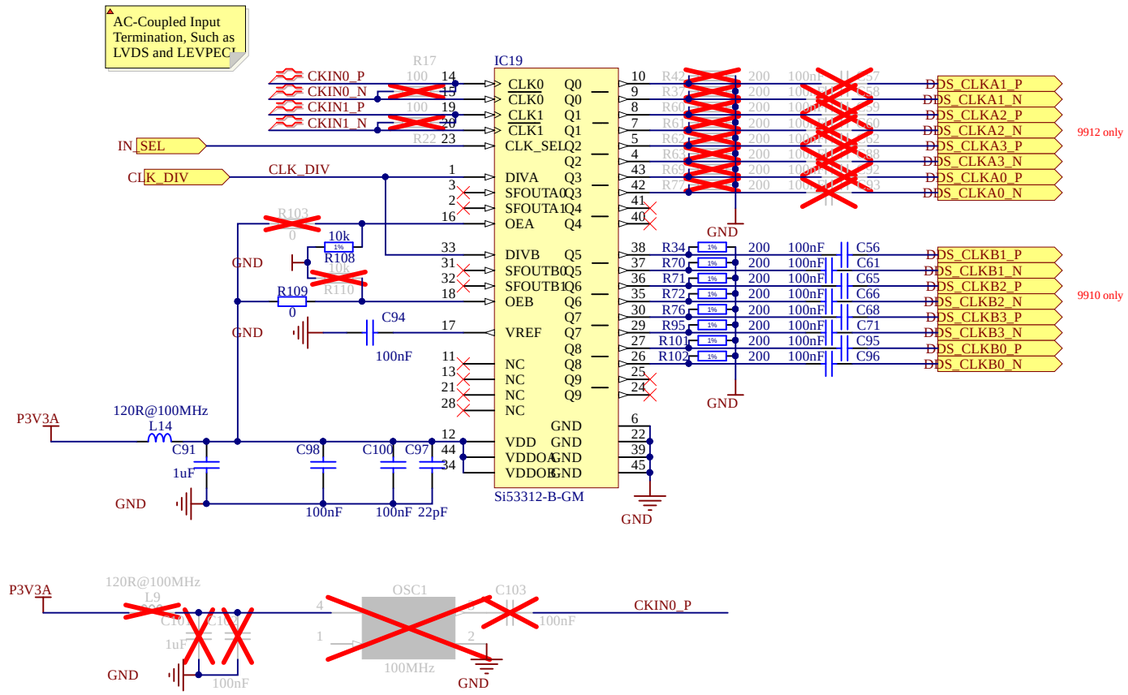
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758



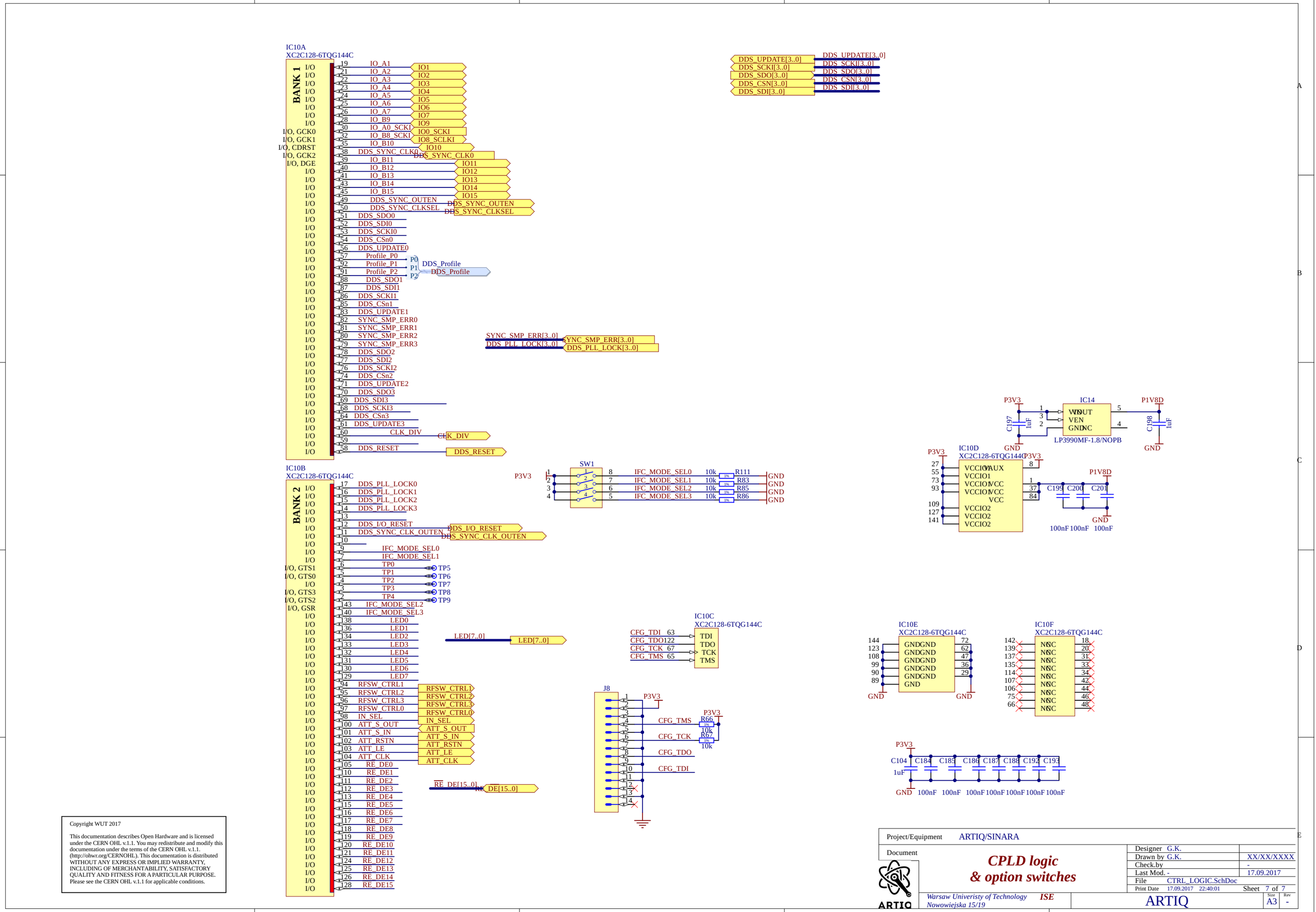


Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	DDS_channel.SchDoc
Print Date	17.09.2017 22:40:01 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

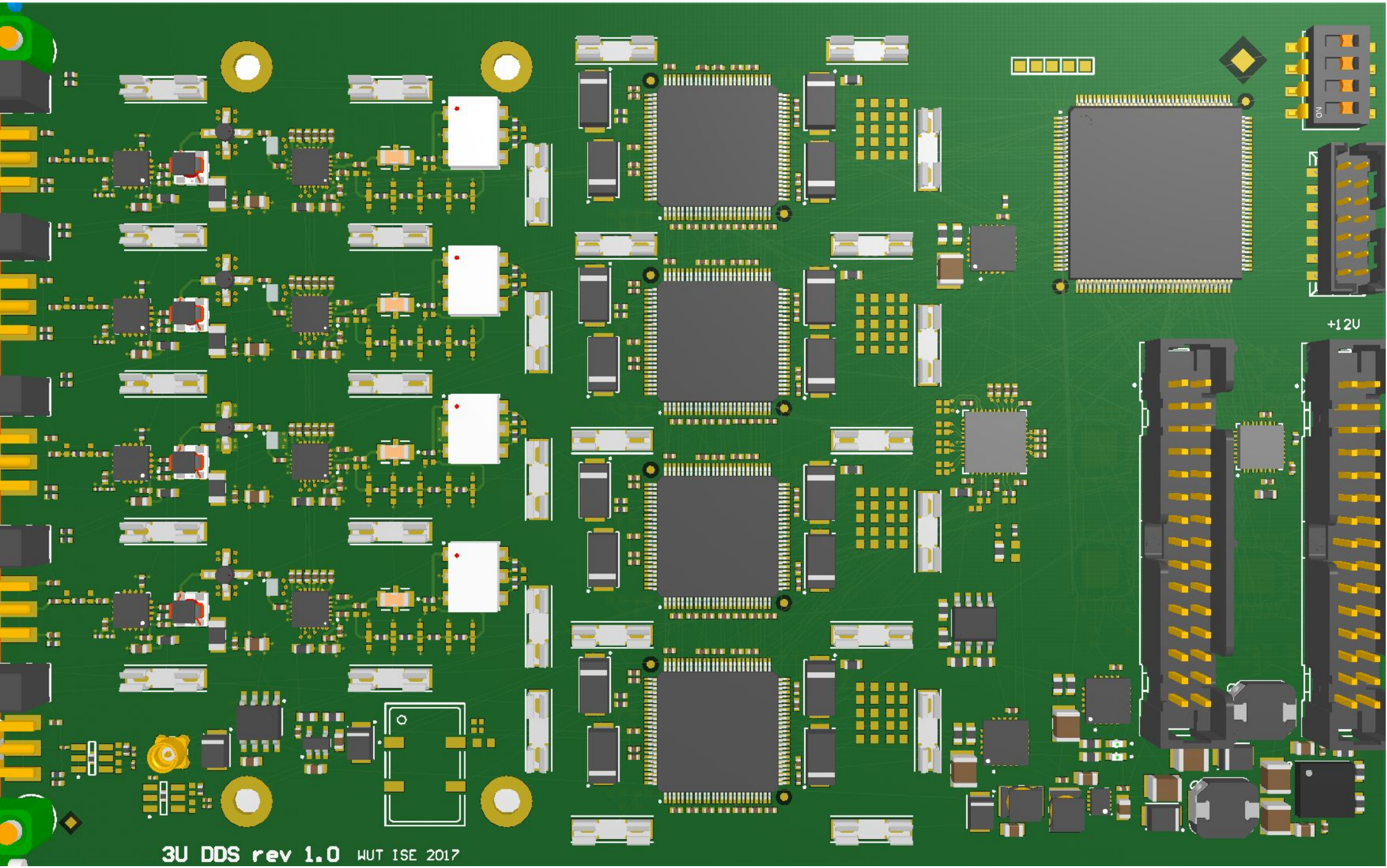




Project/Equipment	ARTIQ/SINARA		
Document	**Clock distribution and generation**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File CLK_INPUT.SchDoc	
		Print Date 17.09.2017 22:40:01	Sheet 6 of 7
Warsaw Univeristy of Technology *Nowowiejska 15/19*	*ISE*	ARTIQ	Size A3 / Rev -



Project/Equipment	ARTIQ/SINARA		
Document	**CPLD logic & option switches**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File CTRL_LOGIC.SchDoc	
		Print Date 17.09.2017 22:40:01	Sheet 7 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	*ISE*	ARTIQ	Size A3 / Rev -


+12V
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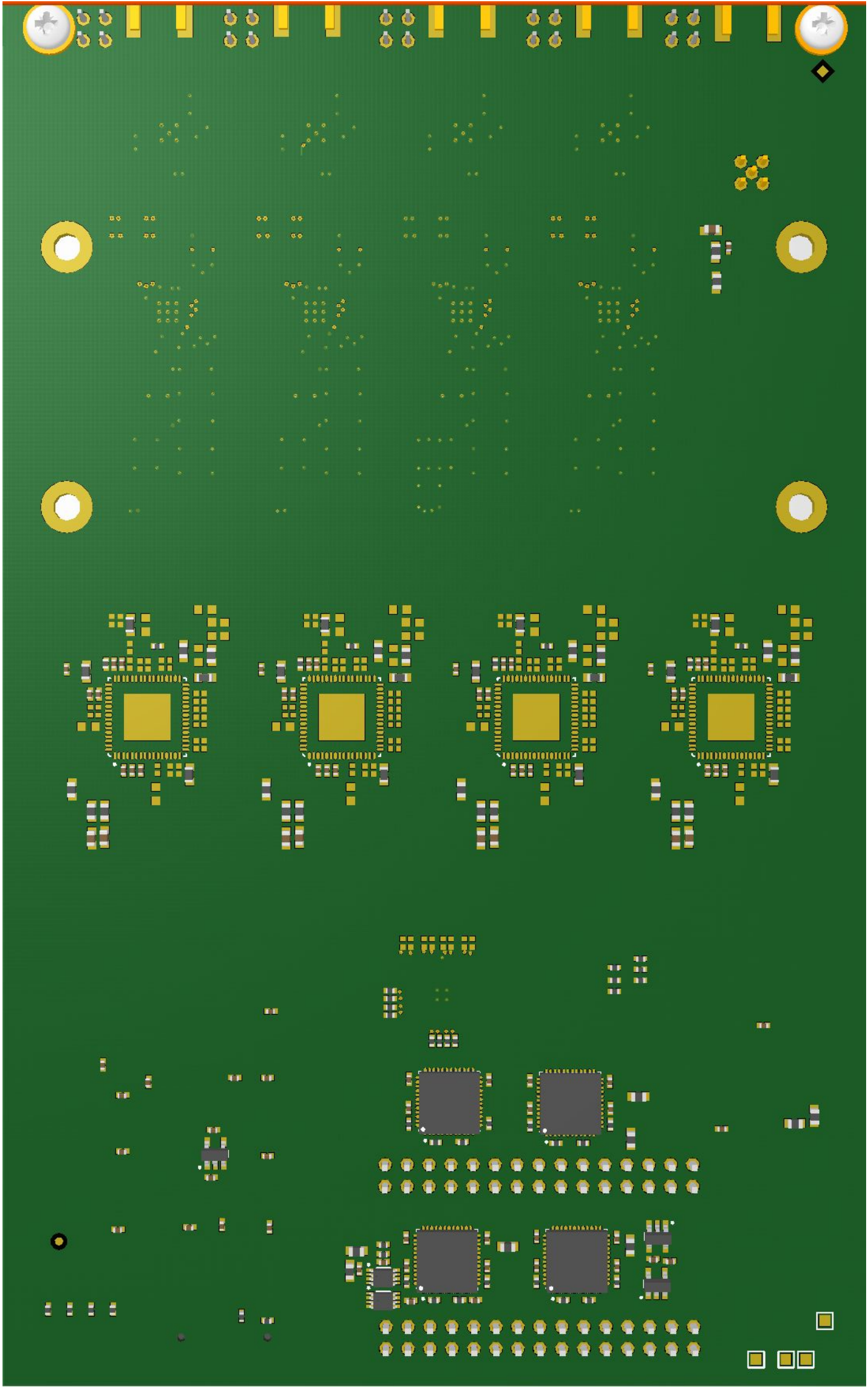

ON
1 2 3 4

+12V

TO KASLI/METLINO VHDCI

30

30

A B

A B

A B

A B

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