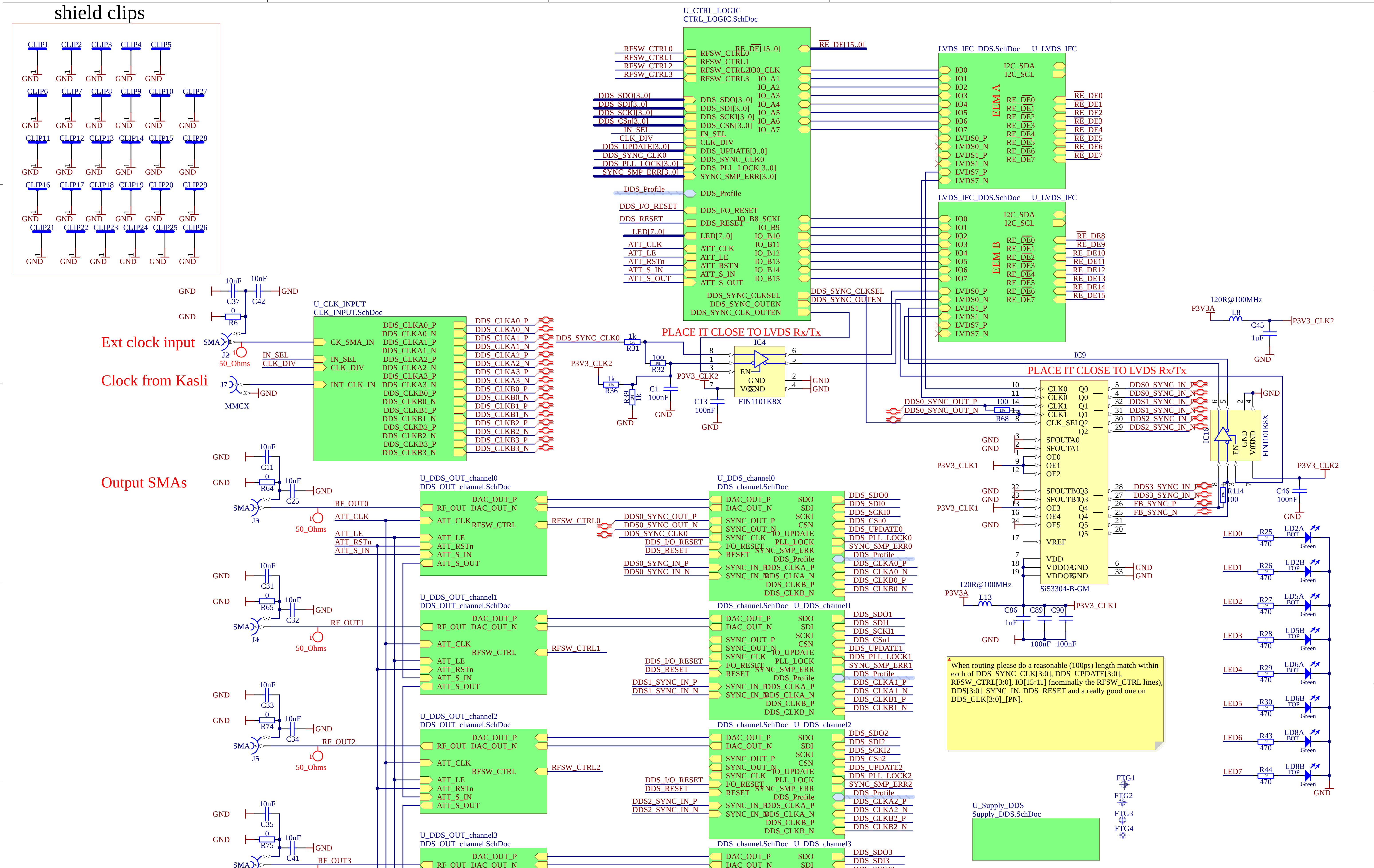
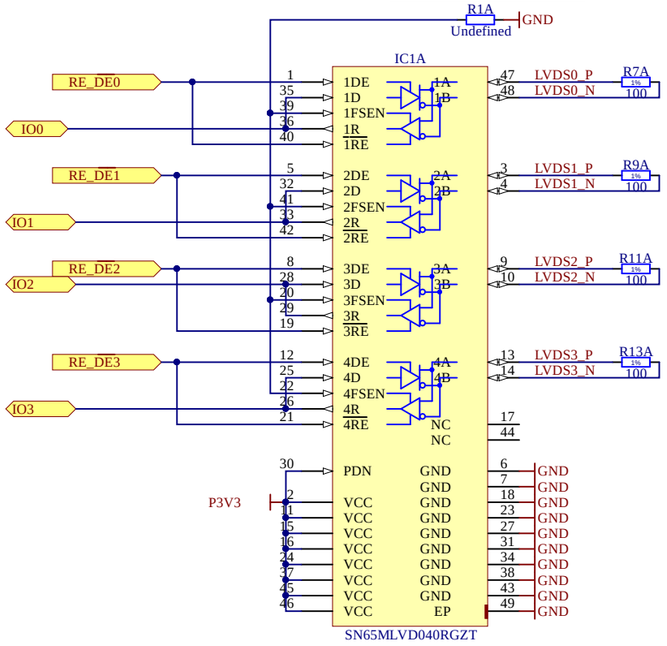

shield clips
CLIP1 CLIP2 CLIP3 CLIP4 CLIP5
CLIP6 CLIP7 CLIP8 CLIP9 CLIP10 CLIP27
CLIP11 CLIP12 CLIP13 CLIP14 CLIP15 CLIP28
CLIP16 CLIP17 CLIP18 CLIP19 CLIP20 CLIP29
CLIP21 CLIP22 CLIP23 CLIP24 CLIP25 CLIP26
GND
U_CTRL_LOGIC
CTRL_LOGIC.SchDoc
RFSW_CTRL0 RFSW_CTRL1 RFSW_CTRL2 RFSW_CTRL3
DDS_SDO[3..0] DDS_SDI[3..0] DDS_SCKI[3..0] DDS_CSn[3..0]
IN_SEL CLK_DIV DDS_UPDATE[3..0] DDS_SYNC_CLK0 DDS_PLL_LOCK[3..0] SYNC_SMP_ERR[3..0]
DDS_Profile DDS_I/O_RESET DDS_RESET LED[7..0]
ATT_CLK ATT_LE ATT_RSTn ATT_S_IN ATT_S_OUT
RE_DE[15..0] IO0_CLK IO_A1 IO_A2 IO_A3 IO_A4 IO_A5 IO_A6 IO_A7
IO_B8_SCKI IO_B9 IO_B10 IO_B11 IO_B12 IO_B13 IO_B14 IO_B15
DDS_SYNC_CLKSEL DDS_SYNC_OUTEN DDS_SYNC_CLK_OUTEN
LVDS_IFC_DDS.SchDoc U_LVDS_IFC
EEM A
EEM B
I2C_SDA I2C_SCL
IO0 IO1 IO2 IO3 IO4 IO5 IO6 IO7
LVDS0_P LVDS0_N LVDS1_P LVDS1_N LVDS7_P LVDS7_N
RE_DE0 RE_DE1 RE_DE2 RE_DE3 RE_DE4 RE_DE5 RE_DE6 RE_DE7
RE_DE8 RE_DE9 RE_DE10 RE_DE11 RE_DE12 RE_DE13 RE_DE14 RE_DE15
U_CLK_INPUT
CLK_INPUT.SchDoc
CK_SMA_IN IN_SEL CLK_DIV INT_CLK_IN
DDS_CLKA0_P DDS_CLKA0_N DDS_CLKA1_P DDS_CLKA1_N DDS_CLKA2_P DDS_CLKA2_N DDS_CLKA3_P DDS_CLKA3_N
DDS_CLKB0_P DDS_CLKB0_N DDS_CLKB1_P DDS_CLKB1_N DDS_CLKB2_P DDS_CLKB2_N DDS_CLKB3_P DDS_CLKB3_N
Ext clock input
Clock from Kasli
Output SMAs
SMA J2 J7 MMCX 50_Ohms
PLACE IT CLOSE TO LVDS Rx/Tx
IC4 FIN1101K8X
IC9 Si53304-B-GM
IC16 FIN1101K8X
120R@100MHz P3V3A L8 C45 1uF P3V3_CLK2
P3V3_CLK1 L13 C86 C89 C90 100nF
DDS0_SYNC_IN_P DDS0_SYNC_IN_N DDS1_SYNC_IN_P DDS1_SYNC_IN_N DDS2_SYNC_IN_P DDS2_SYNC_IN_N DDS3_SYNC_IN_P DDS3_SYNC_IN_N
FB_SYNC_P FB_SYNC_N
DDS0_SYNC_OUT_P DDS0_SYNC_OUT_N
U_DDS_OUT_channel0 DDS_OUT_channel.SchDoc
U_DDS_OUT_channel1
U_DDS_OUT_channel2
U_DDS_OUT_channel3
DAC_OUT_P DAC_OUT_N RF_OUT ATT_CLK RFSW_CTRL ATT_LE ATT_RSTn ATT_S_IN ATT_S_OUT
RF_OUT0 RF_OUT1 RF_OUT2 RF_OUT3
U_DDS_channel0 DDS_channel.SchDoc
U_DDS_channel1 U_DDS_channel2 U_DDS_channel3
SDO SDI SCKI CSN IO_UPDATE PLL_LOCK SYNC_SMP_ERR DDS_Profile DDS_CLKA_P DDS_CLKA_N DDS_CLKB_P DDS_CLKB_N
SYNC_OUT_P SYNC_OUT_N SYNC_CLK I/O_RESET RESET SYNC_IN_P SYNC_IN_N
LED0 LED1 LED2 LED3 LED4 LED5 LED6 LED7
R25 R26 R27 R28 R29 R30 R43 R44 470
LD2A LD2B LD5A LD5B LD6A LD6B LD8A LD8B Green
FTG1 FTG2 FTG3 FTG4
U_Supply_DDS
Supply_DDS.SchDoc
When routing please do a reasonable (100ps) length match within each of DDS_SYNC_CLK[3:0], DDS_UPDATE[3:0], RFSW_CTRL[3:0], IO[15:11] (nominally the RFSW_CTRL lines), DDS[3:0]_SYNC_IN, DDS_RESET and a really good one on DDS_CLK[3:0]_[P,N].

Project/Equipment	ARTIQ/SINARA
Document	3U DDS (URUKUL) Top entity
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 21.09.2017
File	PCB_3U_DDS.schdoc
Print Date	21.09.2017 20:30:55
Sheet	1 of 7
Size	A3
Rev	-

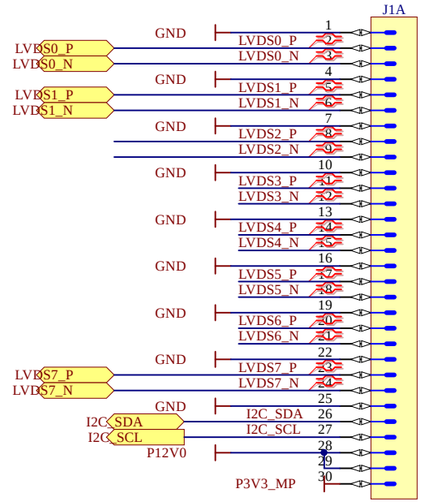
Warsaw Univeristy of Technology ISE
Nowowiejska 15/19

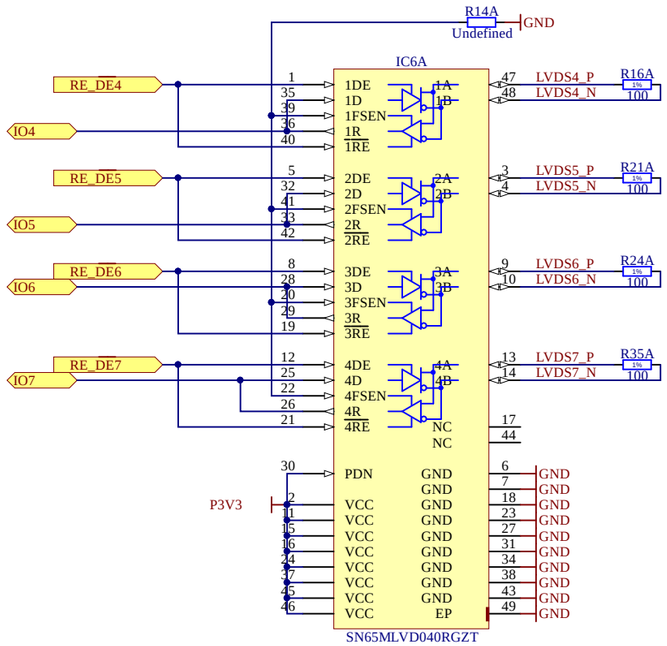
ARTIQ

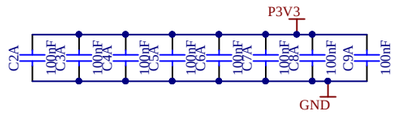
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

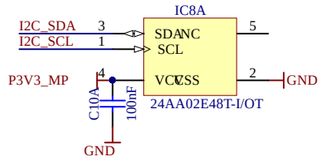


This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A



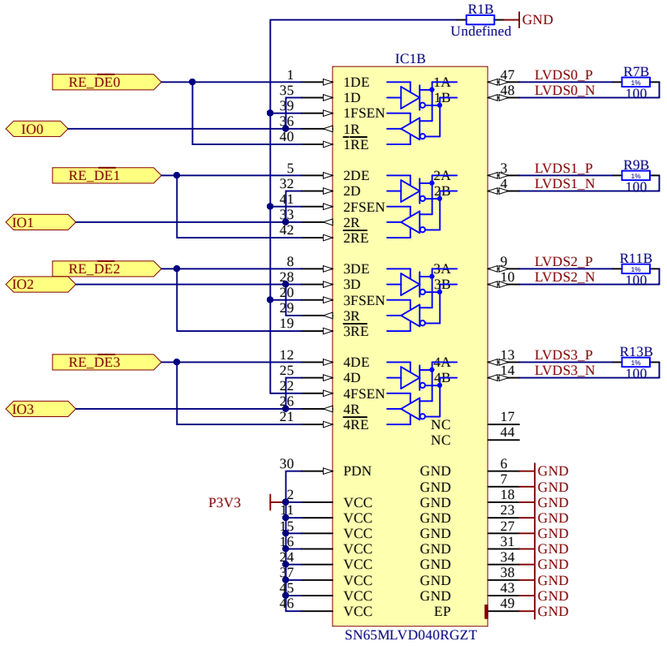




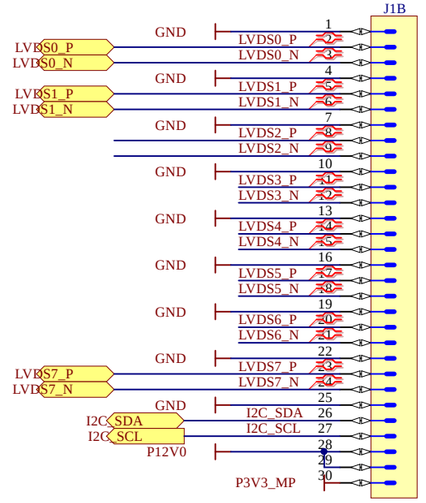


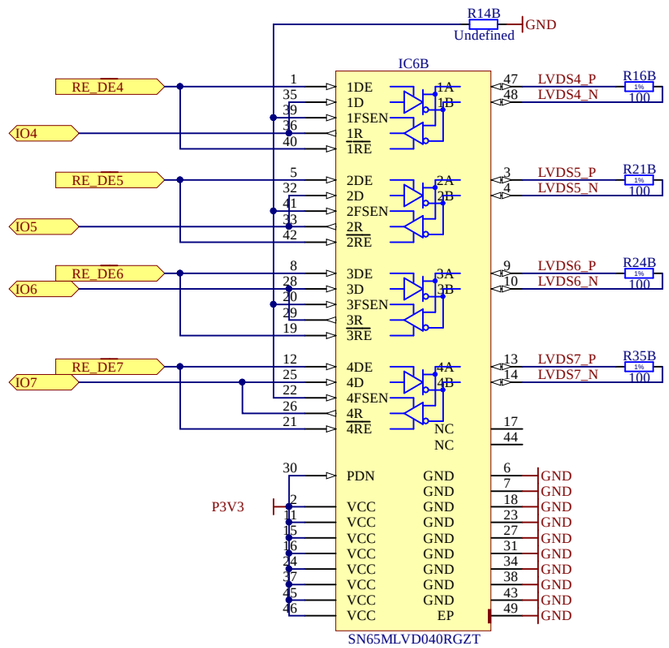
Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File LVDS_IFC_DDS.SchDoc	
		Print Date 21.09.2017 20:30:55	Sheet 2 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19 *ISE*	ARTIQ	Size A3	Rev -

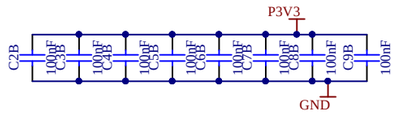
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

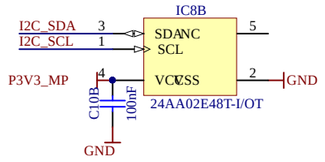


This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A

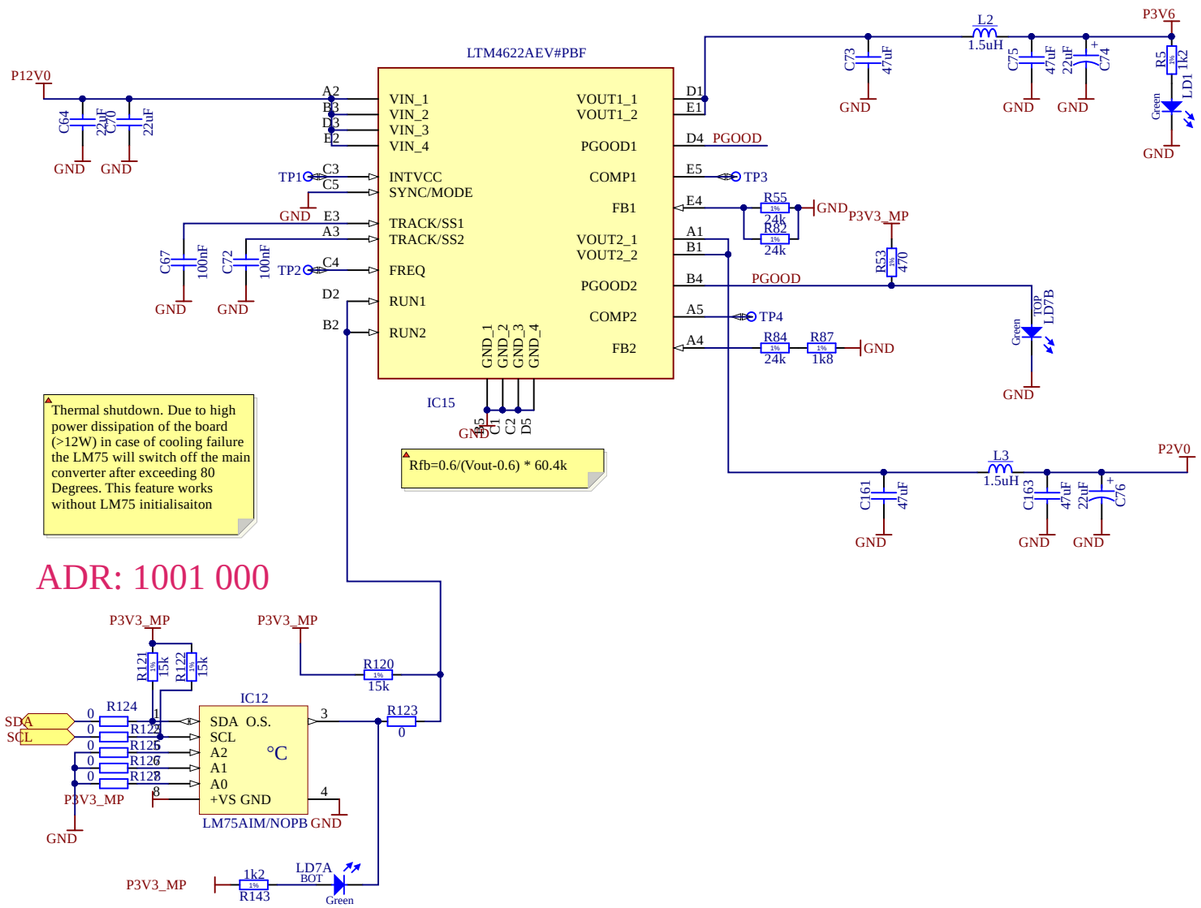








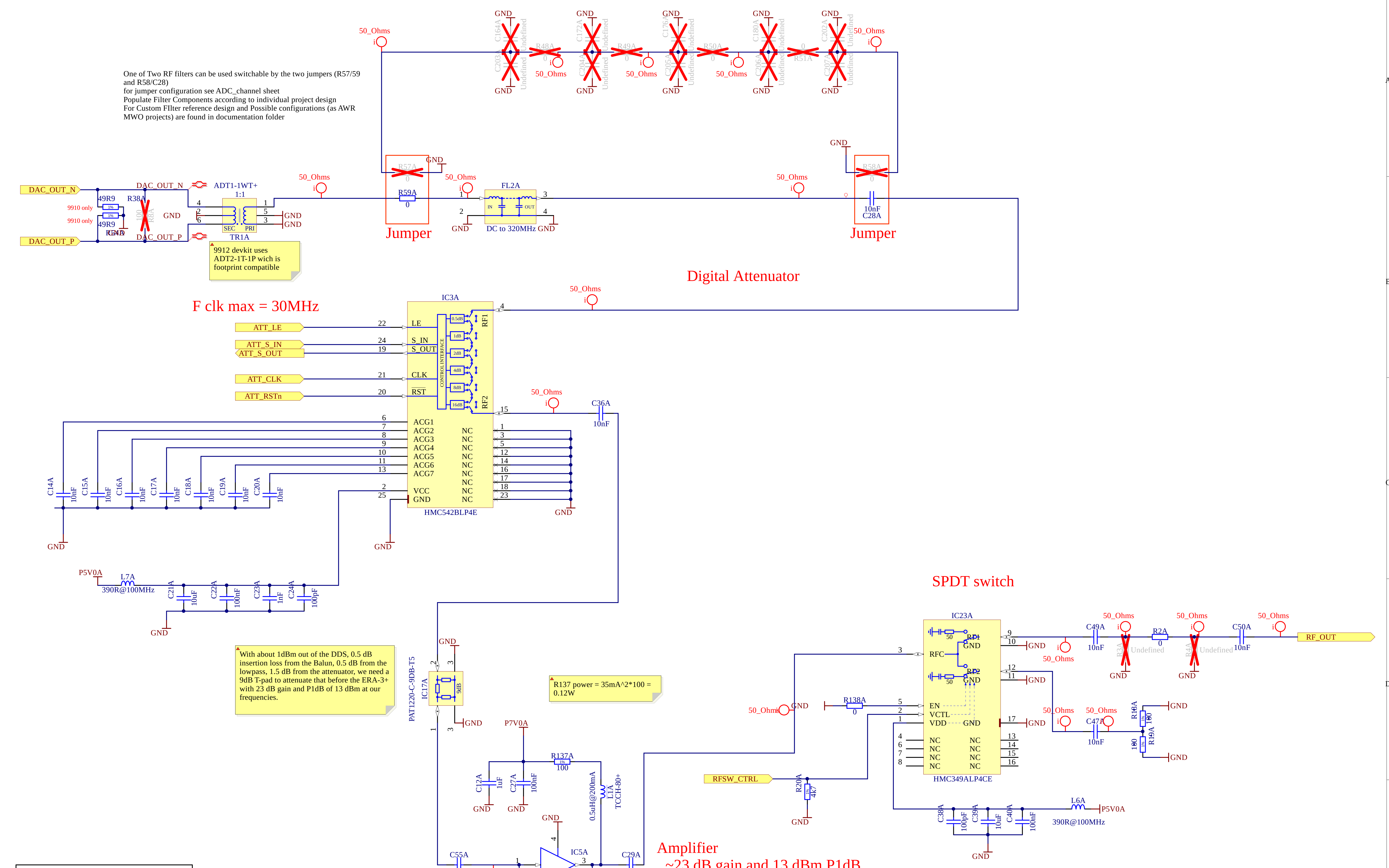
Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File LVDS_IFC_DDS.SchDoc	
		Print Date 21.09.2017 20:30:55	Sheet 2 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	*ISE*	ARTIQ	Size A3 / Rev -



Power budget (max ratings):

	AD9912 variant(mA)	AD9910 variant(mA)
P3V3:		
LVDS interface 4x	660	660
LVDS load 4x24mA	96	96
CPLD	100	100
ADCLK948	230	230
DDS AVDD3	4*(9,6+31)=133,6	4*29=116
DDS DVDDIO	4*3=12	4*11=44
TOTAL P3V3	1121	1146
TOTAL POWER	3.7	3.7
P1V8:		
DDS AVDD	4*(48+136)=736	4*110=440
DDS DVDD	4*246=984	4*222=888
TOTAL P1V8	1720	1328
TOTAL POWER	3,096	2.39
P5V0		
HMC542BLP4E	4*2.9=11.6	4*2.9=11.6
HMC349LP4C	4*3.5=14	4*3.5=14
TOTAL 5V0	25.6	25.6
TOTAL POWER	0,125	0,125
P7V0		
ERA-3XSM+	4*35=150	4*35=150
TOTAL POWER	1.05	1.05
DC/DC converter losses		
TPS62175 eff .95	0,05*(.27+0,026)*7,5=0.11	0,05*(.27+0,026)*7,5=0.11
LTM:3.6V eff .9	0.1*1,321*3,6=0,47	0,1*1,346*3,6=0,48
LTM:2V eff .87	0.13*1,721*2=0,44	0.13*1.328*2=0.34
LDO losses		
2V->1.8V	0.34	0,26
3.6V->3.3V	0.396	0.4
7.5V->7V	0,135	0,135
7.5V->5V	0,064	0,064
Total power from 12V	9.95W	9.05
Total current from 12V	0.83A	0.75A

Project/Equipment	ARTIQ/SINARA		
Document	**Power supply DC/DC & LDOs**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	21.09.2017
		File Supply_DDS.SchDoc	
		Print Date 21.09.2017 20:30:55	Sheet 3 of 7
Warsaw Univeristy of Technology *Nowowiejska 15/19* *ISE*	ARTIQ	Size A3	Rev -



One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder
DAC_OUT_N
DAC_OUT_P
49R9
49R9
9910 only
9910 only
R38A
ADT1-1WT+
1:1
TR1A
9912 devkit uses ADT2-1T-1P wich is footprint compatible
Jumper
Jumper
R57A
R59A
R58A
FL2A
DC to 320MHz
10nF
C28A
50_Ohms
GND
Digital Attenuator
F clk max = 30MHz
IC3A
HMC542BLP4E
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
LE
S_IN
S_OUT
CLK
RST
ACG1
ACG2
ACG3
ACG4
ACG5
ACG6
ACG7
VCC
NC
RF1
RF2
C36A
10nF
C14A
C15A
C16A
C17A
C18A
C19A
C20A
P5V0A
L7A
390R@100MHz
C21A
10uF
C22A
100nF
C23A
1nF
C24A
100pF
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.
IC17A
PAT1220-C-9DB-T5
9dB
R137 power = 35mA^2*100 = 0.12W
P7V0A
R137A
100
C12A
1uF
C27A
100nF
0.5uH@200mA
L1A
TCCH-80+
C55A
10nF
IC5A
ERA-3+
C29A
10nF
R33A
Undefined
Amplifier
~23 dB gain and 13 dBm P1dB
SPDT switch
IC23A
HMC349ALP4CE
RFC
RF1
RF2
EN
VCTL
VDD
R138A
RFSW_CTRL
R20A
4K7
C38A
100pF
C39A
10uF
C40A
100nF
L6A
390R@100MHz
C49A
10nF
R2A
C50A
10nF
RF_OUT
C47A
10nF
R16A
R19A
180

Project/Equipment	ARTIQ/SINARA
Document	*Output stage : Attenuator, amplifier and filter*
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 21.09.2017
File	DDS_OUT_channel.SchDoc
Print Date	21.09.2017 20:30:56
Sheet	4 of 7
Size	A3
Rev	-

Warsaw Univeristy of Technology *ISE*
Nowowiejska 15/19

ARTIQ

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

Jumper

Jumper

Digital Attenuator

F clk max = 30MHz

IC3B
HMC542BLP4E

ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R137 power = 35mA^2*100 = 0.12W

SPDT switch

IC23B
HMC349ALP4CE

RFSW_CTRL

Amplifier
~23 dB gain and 13 dBm P1dB

IC5B
ERA-3+

Project/Equipment	ARTIQ/SINARA
Document	**Output stage : Attenuator, amplifier and filter**
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 21.09.2017
File	DDS_OUT_channel.SchDoc
Print Date	21.09.2017 20:30:56 Sheet 4 of 7
Warsaw Univeristy of Technology ISE Nowowiejska 15/19	ARTIQ Size A3 Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

Jumper

Jumper

Digital Attenuator

F clk max = 30MHz

IC3C

HMC542BLP4E

ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R137 power = 35mA^2*100 = 0.12W

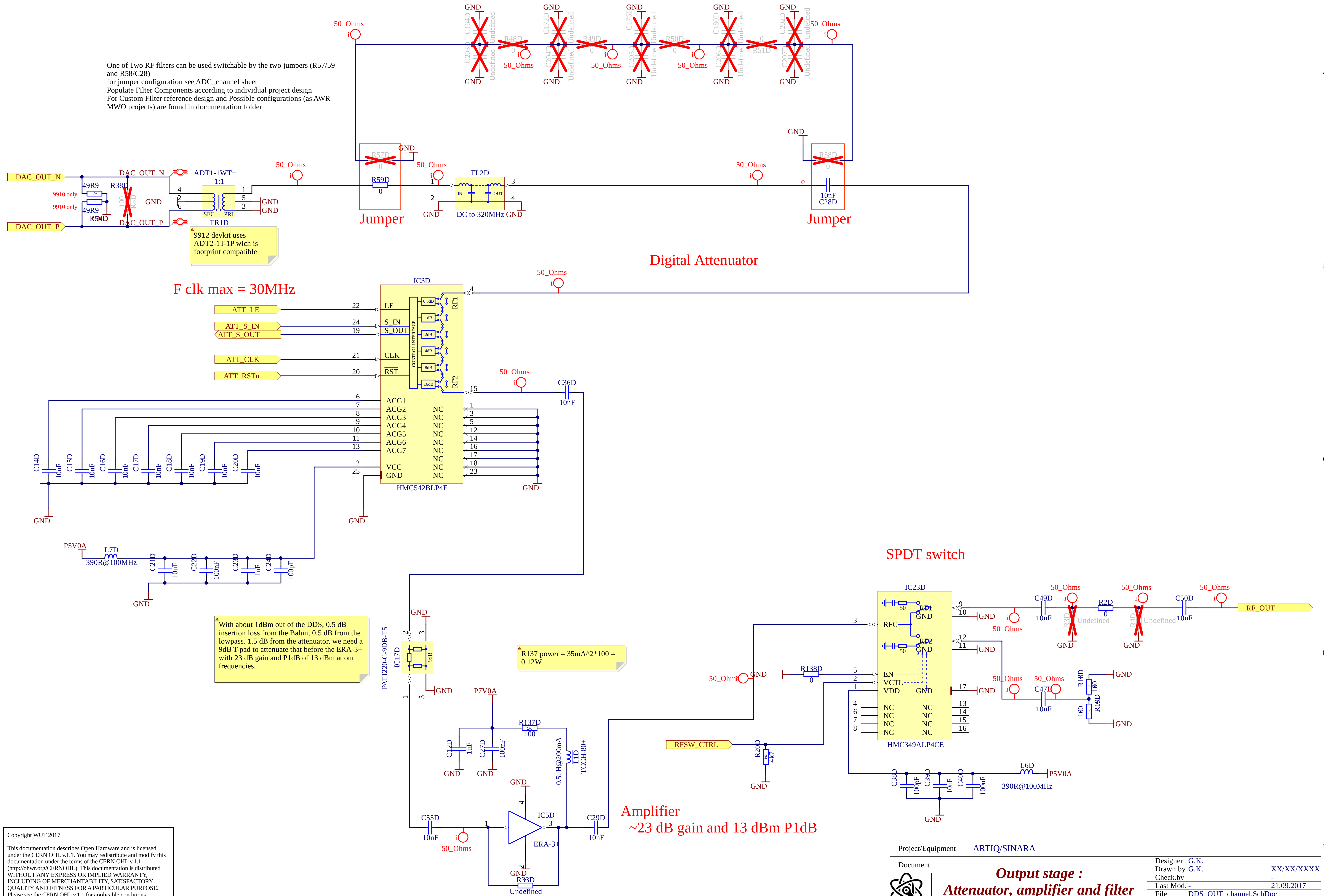
SPDT switch

IC23C

HMC349ALP4CE

Amplifier
~23 dB gain and 13 dBm P1dB

Project/Equipment	ARTIQ/SINARA
Document	**Output stage : Attenuator, amplifier and filter**
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 21.09.2017
File	DDS_OUT_channel.SchDoc
Print Date	21.09.2017 20:30:56 Sheet 4 of 7
Warsaw Univeristy of Technology ISE Nowowiejska 15/19	ARTIQ Size A3 Rev -


One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
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DAC_OUT_N
DAC_OUT_P
ADT1-1WT+
1:1
TR1D
9912 devkit uses ADT2-1T-1P wich is footprint compatible
Jumper
FL2D
DC to 320MHz
Jumper
Digital Attenuator
F clk max = 30MHz
IC3D
HMC542BLP4E
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
P5V0A
L7D
390R@100MHz
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.
PAT1220-C-9DB-T5
IC17D
R137 power = 35mA^2*100 = 0.12W
P7V0A
R137D
100
L1D
TCCH-80+
0.5uH@200mA
IC5D
ERA-3+
Amplifier
~23 dB gain and 13 dBm P1dB
SPDT switch
IC23D
HMC349ALP4CE
RF_OUT
RFSW_CTRL
L6D
390R@100MHz
P5V0A

Project/Equipment	ARTIQ/SINARA
Document	*Output stage : Attenuator, amplifier and filter*
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 21.09.2017
File	DDS_OUT_channel.SchDoc
Print Date	21.09.2017 20:30:57
Sheet	4 of 7
Size	A3
Rev	-

Warsaw Univeristy of Technology ISE
Nowowiejska 15/19

ARTIQ

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Project/Equipment ARTIQ/SINARA

Document **9910 & 9912 DDS**

Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 21.09.2017
File	DDS_channel.SchDoc
Print Date	21.09.2017 20:30:57 Sheet 5 of 7

Warsaw Univeristy of Technology ISE
Nowowiejska 15/19

ARTIQ Size A3 Rev -

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

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0	0	0	1	Xtal/PLL	38.87939
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0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Project/Equipment ARTIQ/SINARA

Document **9910 & 9912 DDS**

Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 21.09.2017
File	DDS_channel.SchDoc
Print Date	21.09.2017 20:30:58 Sheet 5 of 7

Warsaw Univeristy of Technology ISE
Nowowiejska 15/19

ARTIQ Size A3 Rev -

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Project/Equipment: ARTIQ/SINARA

Document: 9910 & 9912 DDS

Designer	G.K.
Drawn by	G.K.
Check.by	-
Last Mod.	-
File	DDS_channel.SchDoc
Print Date	21.09.2017 20:30:58
	XX/XX/XXXX
	21.09.2017
Sheet	5 of 7

Warsaw Univeristy of Technology ISE
Nowowiejska 15/19

ARTIQ

Size A3 | Rev -

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0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
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0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
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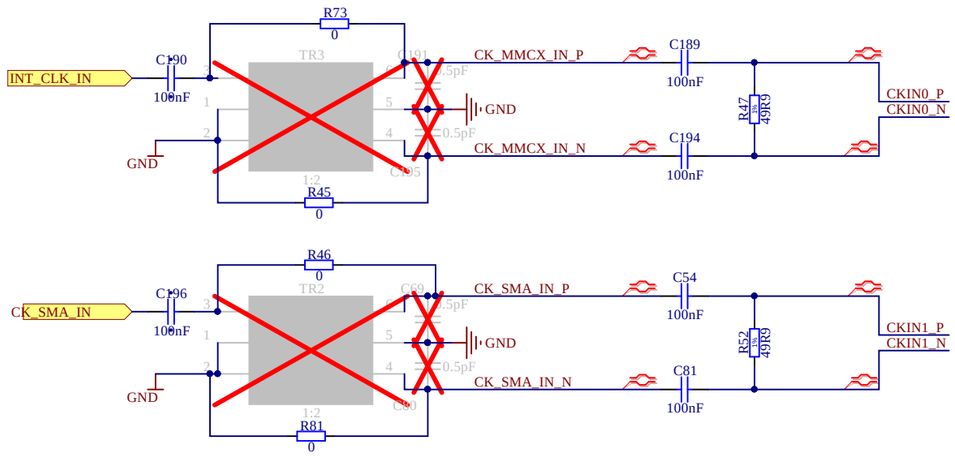
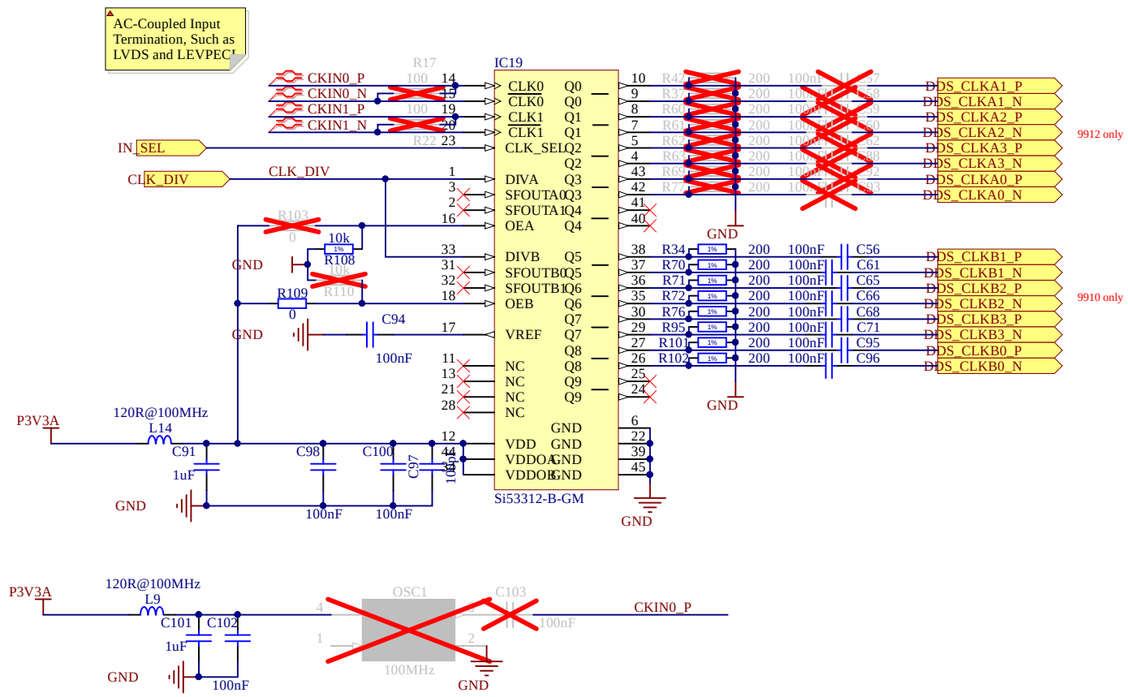
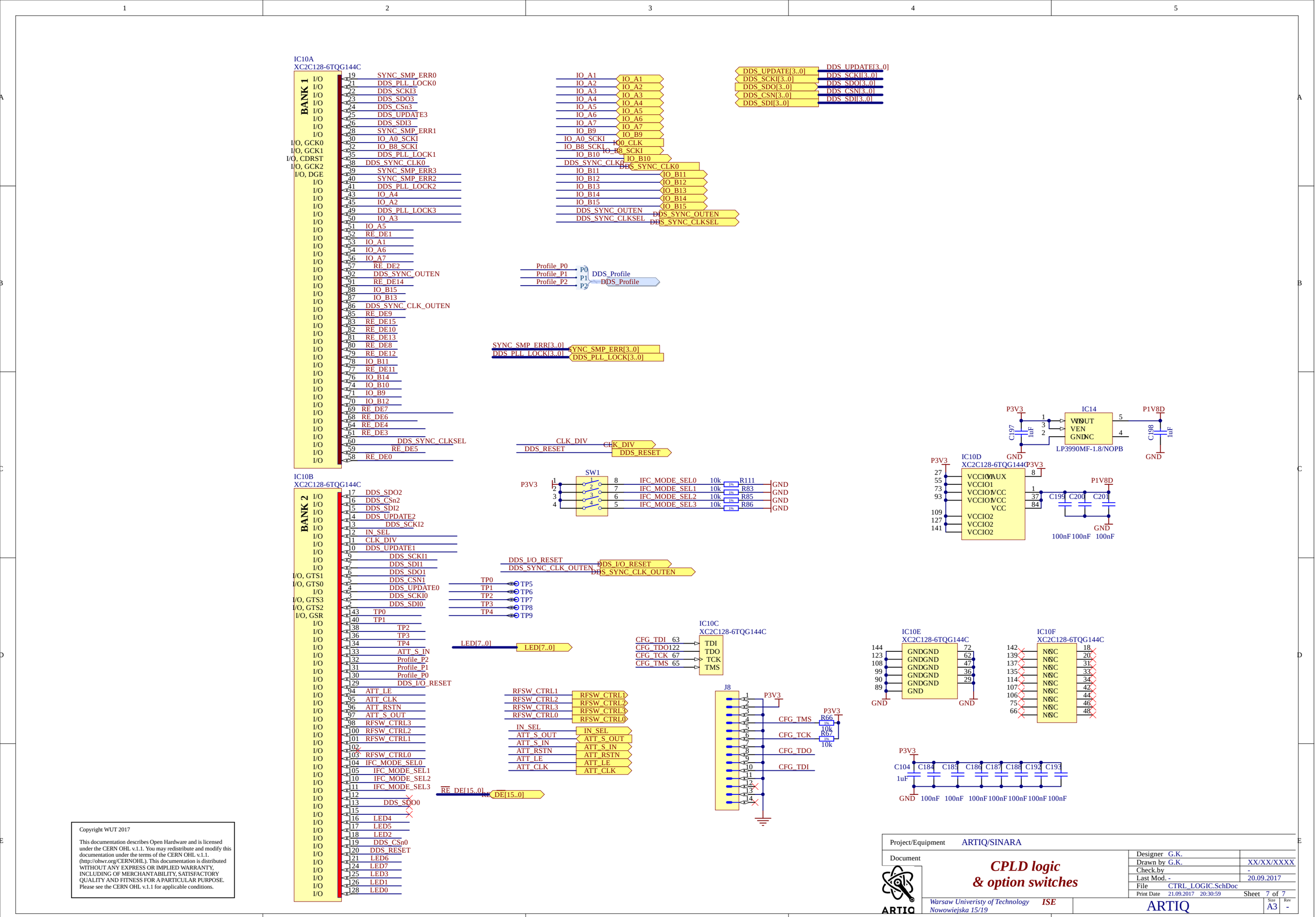
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 21.09.2017
File	DDS_channel.SchDoc
Print Date	21.09.2017 20:30:59 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE ARTIQ Size A3 Rev -





Project/Equipment	ARTIQ/SINARA		
Document	**Clock distribution and generation**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File CLK_INPUT.SchDoc	
		Print Date 21.09.2017 20:30:59	Sheet 6 of 7
Warsaw Univeristy of Technology *Nowowiejska 15/19*	*ISE*	ARTIQ	Size A3 / Rev -


IC10A
XC2C128-6TQG144C
BANK 1
SYNC_SMP_ERR0
DDS_PLL_LOCK0
DDS_SCKI3
DDS_SDO3
DDS_CSn3
DDS_UPDATE3
DDS_SDI3
SYNC_SMP_ERR1
IO_A0_SCKI
IO_B8_SCKI
DDS_PLL_LOCK1
DDS_SYNC_CLK0
SYNC_SMP_ERR3
SYNC_SMP_ERR2
DDS_PLL_LOCK2
IO_A4
IO_A2
DDS_PLL_LOCK3
IO_A3
IO_A5
RE_DE1
IO_A1
IO_A6
IO_A7
RE_DE2
DDS_SYNC_OUTEN
RE_DE14
IO_B15
IO_B13
DDS_SYNC_CLK_OUTEN
RE_DE9
RE_DE15
RE_DE10
RE_DE13
RE_DE8
RE_DE12
IO_B11
RE_DE11
IO_B14
IO_B10
IO_B9
IO_B12
RE_DE7
RE_DE6
RE_DE4
RE_DE3
DDS_SYNC_CLKSEL
RE_DE5
RE_DE0
IO_A1
IO_A2
IO_A3
IO_A4
IO_A5
IO_A6
IO_A7
IO_B9
IO_A0_SCKI
IO0_CLK
IO_B8_SCKI
IO_B10
DDS_SYNC_CLK0
IO_B11
IO_B12
IO_B13
IO_B14
IO_B15
DDS_SYNC_OUTEN
DDS_SYNC_CLKSEL
DDS_UPDATE[3..0]
DDS_SCKI[3..0]
DDS_SDO[3..0]
DDS_CSN[3..0]
DDS_SDI[3..0]
Profile_P0
Profile_P1
Profile_P2
P0
P1
P2
DDS_Profile
SYNC_SMP_ERR[3..0]
DDS_PLL_LOCK[3..0]
CLK_DIV
DDS_RESET
SW1
P3V3
IFC_MODE_SEL0
IFC_MODE_SEL1
IFC_MODE_SEL2
IFC_MODE_SEL3
10k
R111
R83
R85
R86
GND
IC10B
XC2C128-6TQG144C
BANK 2
DDS_SDO2
DDS_CSn2
DDS_SDI2
DDS_UPDATE2
DDS_SCKI2
IN_SEL
CLK_DIV
DDS_UPDATE1
DDS_SCKI1
DDS_SDI1
DDS_SDO1
DDS_CSN1
DDS_UPDATE0
DDS_SCKI0
DDS_SDI0
TP0
TP1
TP2
TP3
TP4
ATT_S_IN
Profile_P2
Profile_P1
Profile_P0
DDS_I/O_RESET
ATT_LE
ATT_CLK
ATT_RSTN
ATT_S_OUT
RFSW_CTRL3
RFSW_CTRL2
RFSW_CTRL1
RFSW_CTRL0
IFC_MODE_SEL0
IFC_MODE_SEL1
IFC_MODE_SEL2
IFC_MODE_SEL3
DDS_SDO0
LED4
LED5
LED2
DDS_CSn0
DDS_RESET
LED6
LED7
LED3
LED1
LED0
DDS_I/O_RESET
DDS_SYNC_CLK_OUTEN
TP5
TP6
TP7
TP8
TP9
LED[7..0]
RE_DE[15..0]
DE[15..0]
IC10C
XC2C128-6TQG144C
TDI
TDO
TCK
TMS
CFG_TDI
CFG_TDO
CFG_TCK
CFG_TMS
RFSW_CTRL1
RFSW_CTRL2
RFSW_CTRL3
RFSW_CTRL0
IN_SEL
ATT_S_OUT
ATT_S_IN
ATT_RSTN
ATT_LE
ATT_CLK
J8
R66
R67
IC14
LP3990MF-1.8/NOPB
P1V8D
C197
C198
1uF
IC10D
XC2C128-6TQG144C
VCCIO3
VCCIO1
VCCIO0
VCCIO2
VCCAUX
VCC
C199
C200
C201
100nF
IC10E
XC2C128-6TQG144C
GNDGND
GND
IC10F
XC2C128-6TQG144C
NC
C104
C184
C185
C186
C187
C188
C192
C193
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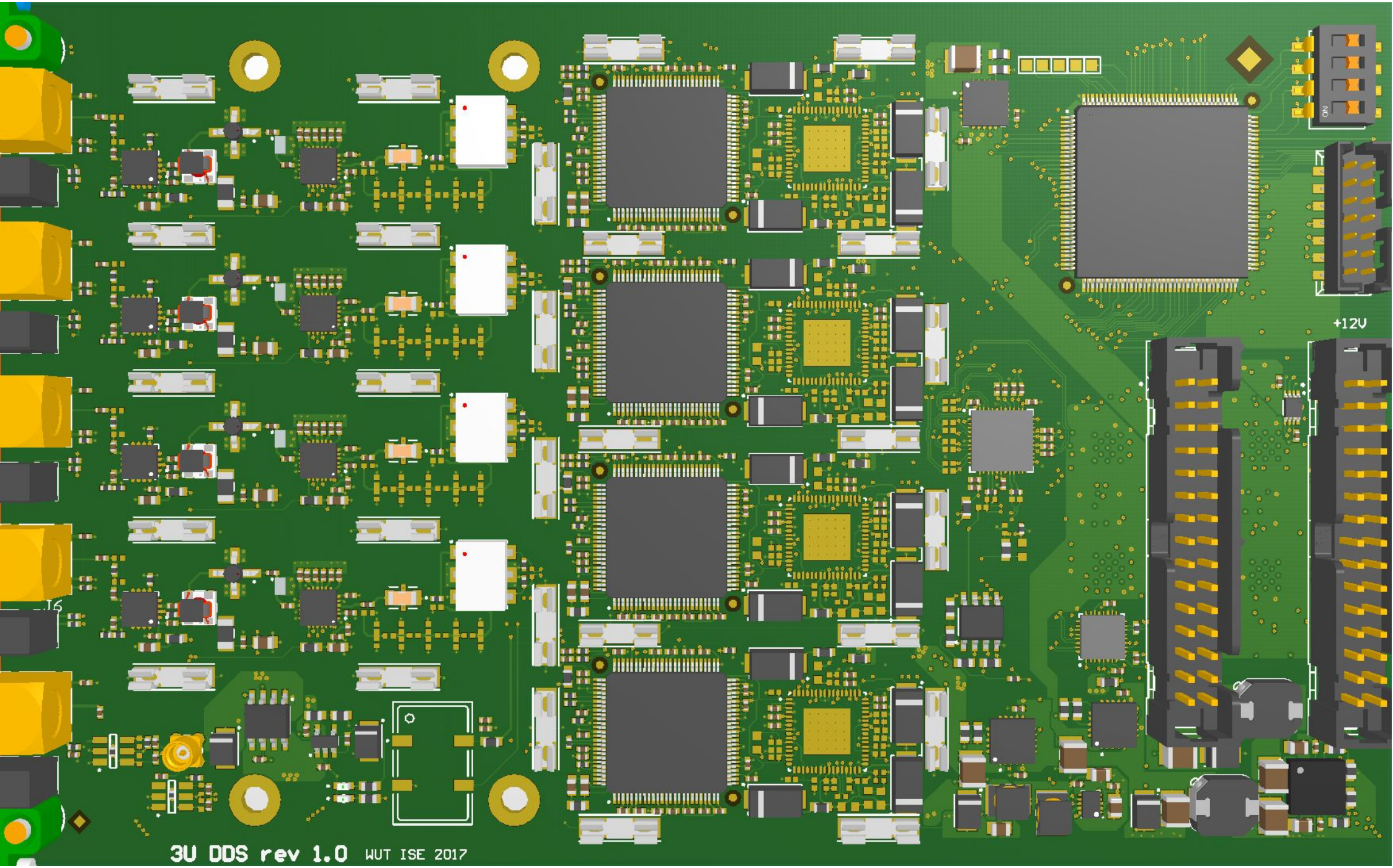
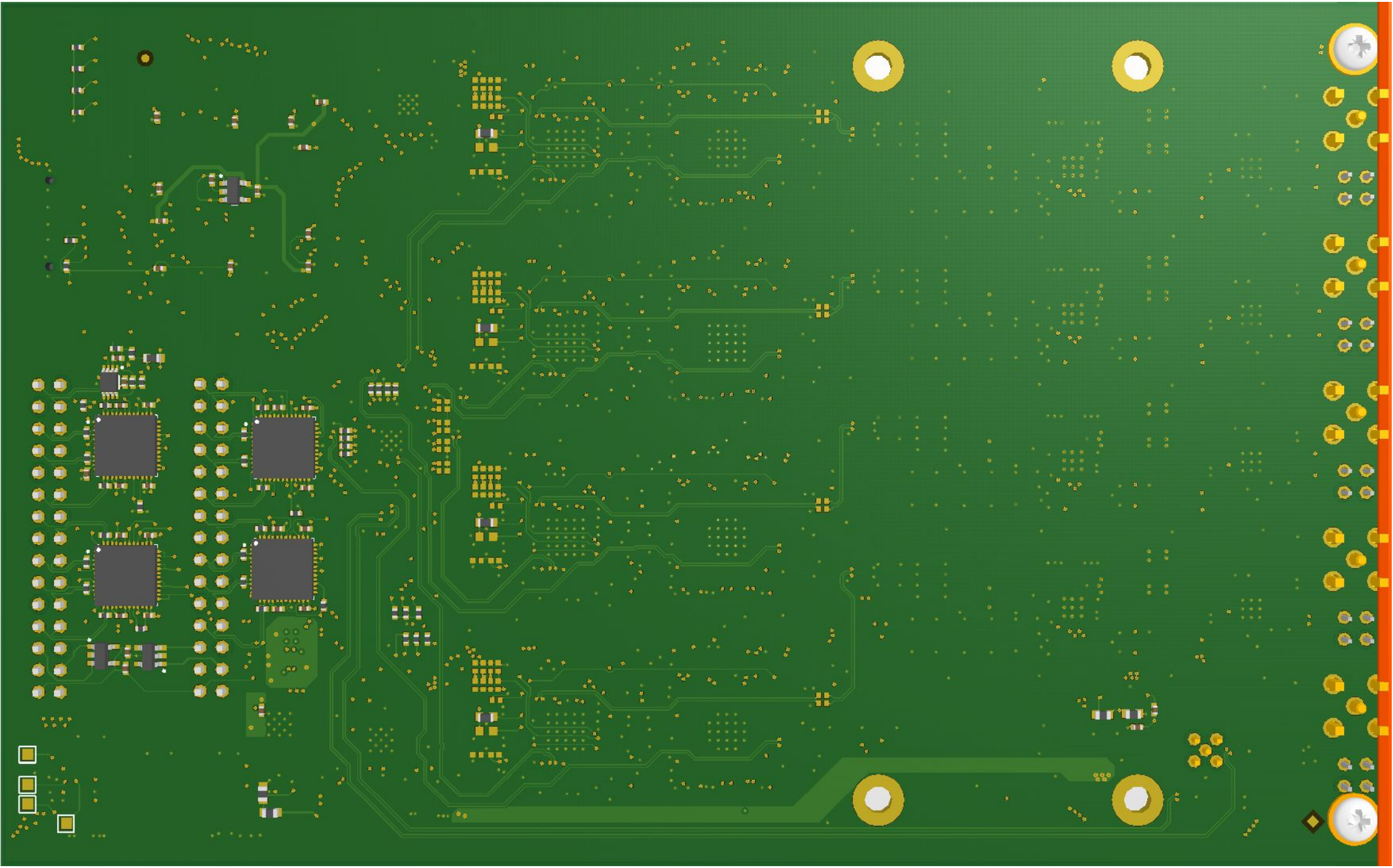
Project/Equipment ARTIQ/SINARA
Document
CPLD logic & option switches
Designer G.K.
Drawn by G.K. XX/XX/XXXX
Check.by -
Last Mod. - 20.09.2017
File CTRL_LOGIC.SchDoc
Print Date 21.09.2017 20:30:59 Sheet 7 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19
ISE
ARTIQ
Size A3
Rev -


+12V
3U DDS rev 1.0
WUT ISE 2017



ON
1 2 3 4

+12V

TO KASLI/METLINO VHDCI

30

30

J6

3U DDS rev 1.0 WUT ISE 2017