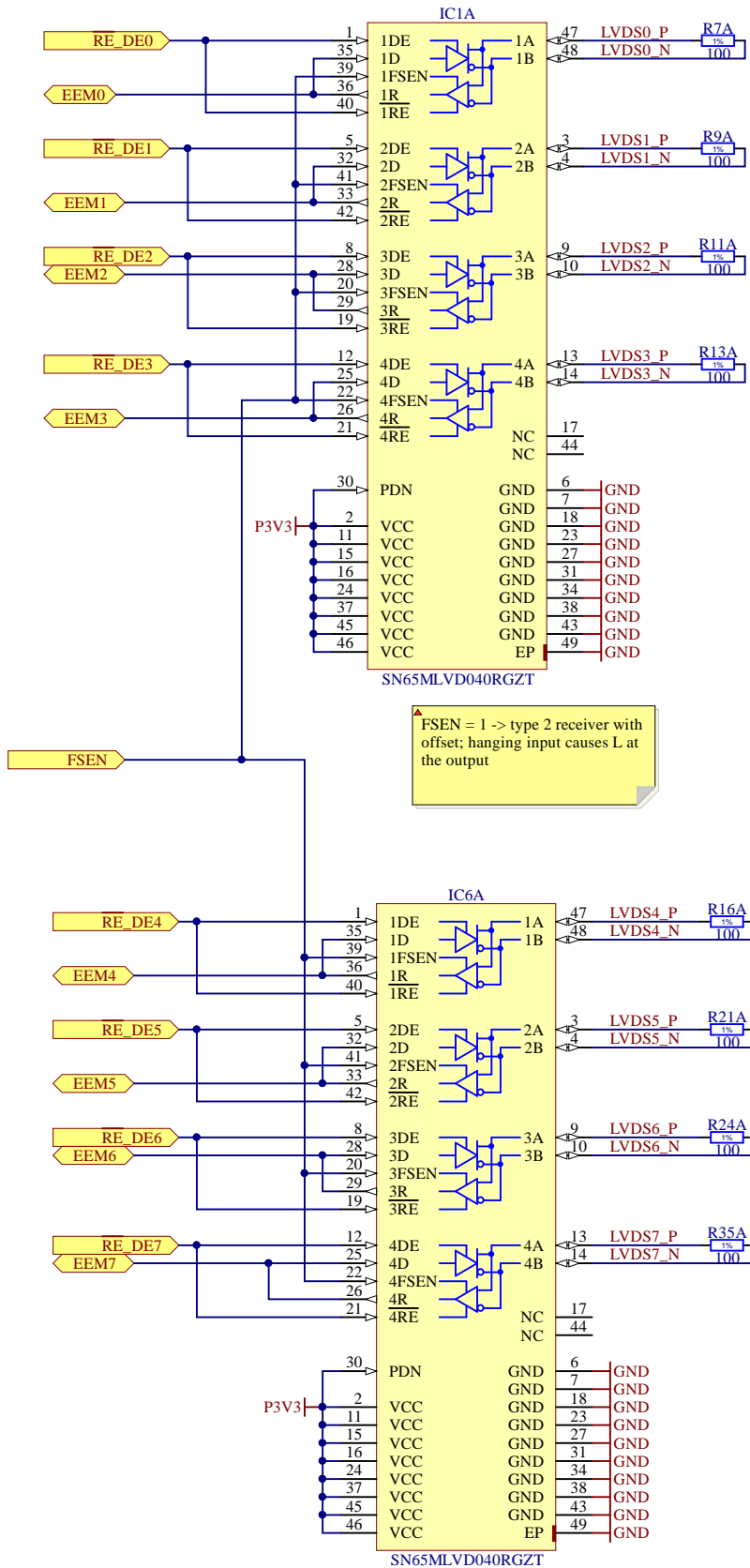
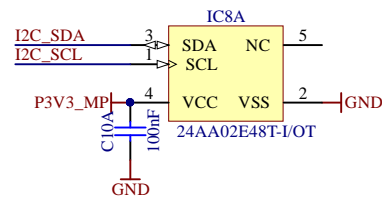
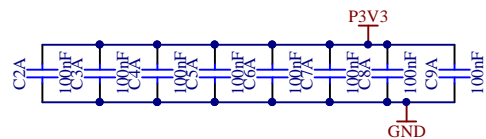
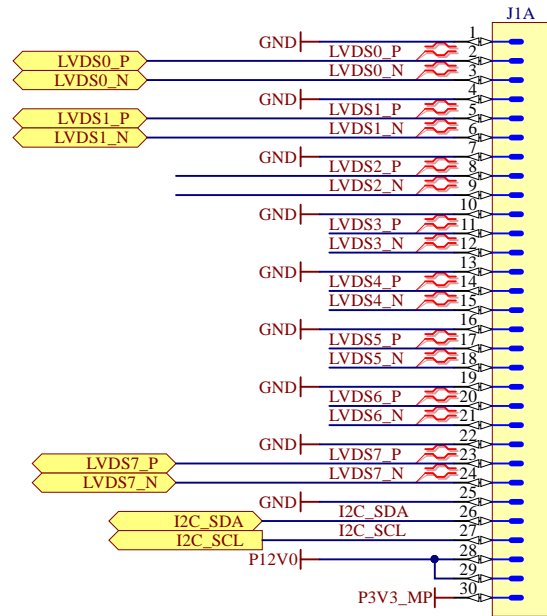


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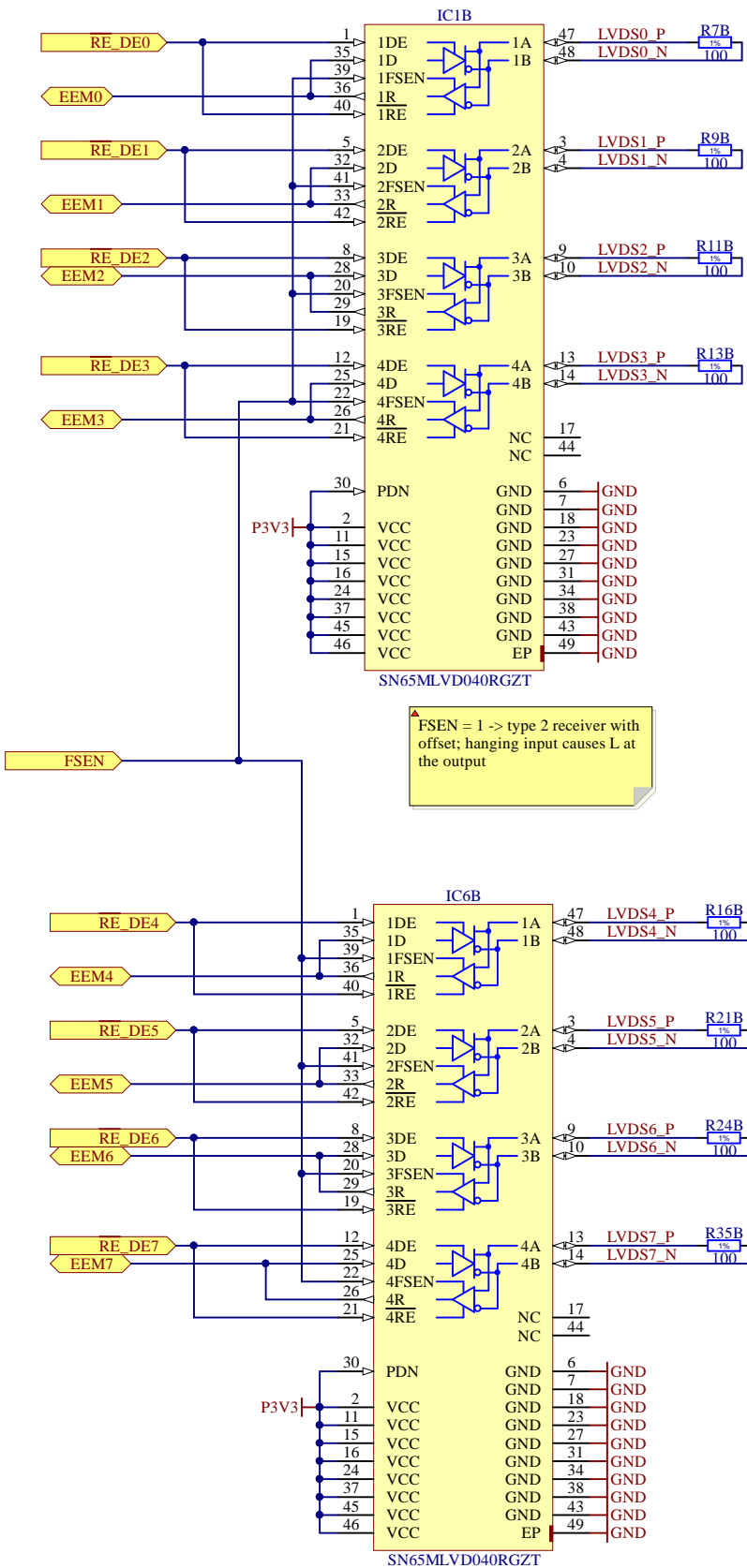
EEM connector: IO are LVDS, I2C is 3V3 LVCMOS, P3V3_MP up to 20mA, P12V up to 1A



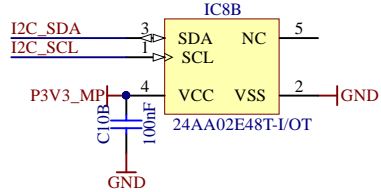
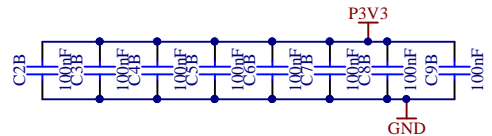
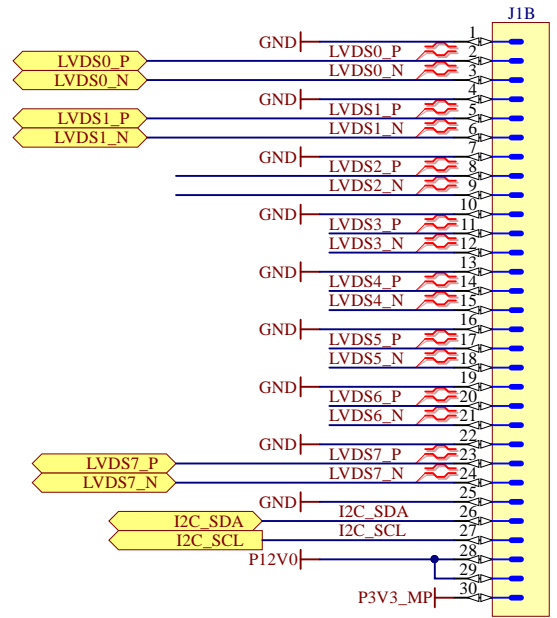
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| Project/Equipment | ARTIQ/SINARA | |
| Document | LVDS to LVTTL interface & EEM connector | |
| Designer | G.K. | XX/XX/XXXX |
| Drawn by | G.K. | - |
| Check by | - | 17.01.2018 |
| Last Mod. | - | - |
| File | LVDS_IFC_DDS.SchDoc | Sheet 2 of 7 |
| Print Date | 17.01.2018 00:55:52 | Size A3 Rev - |

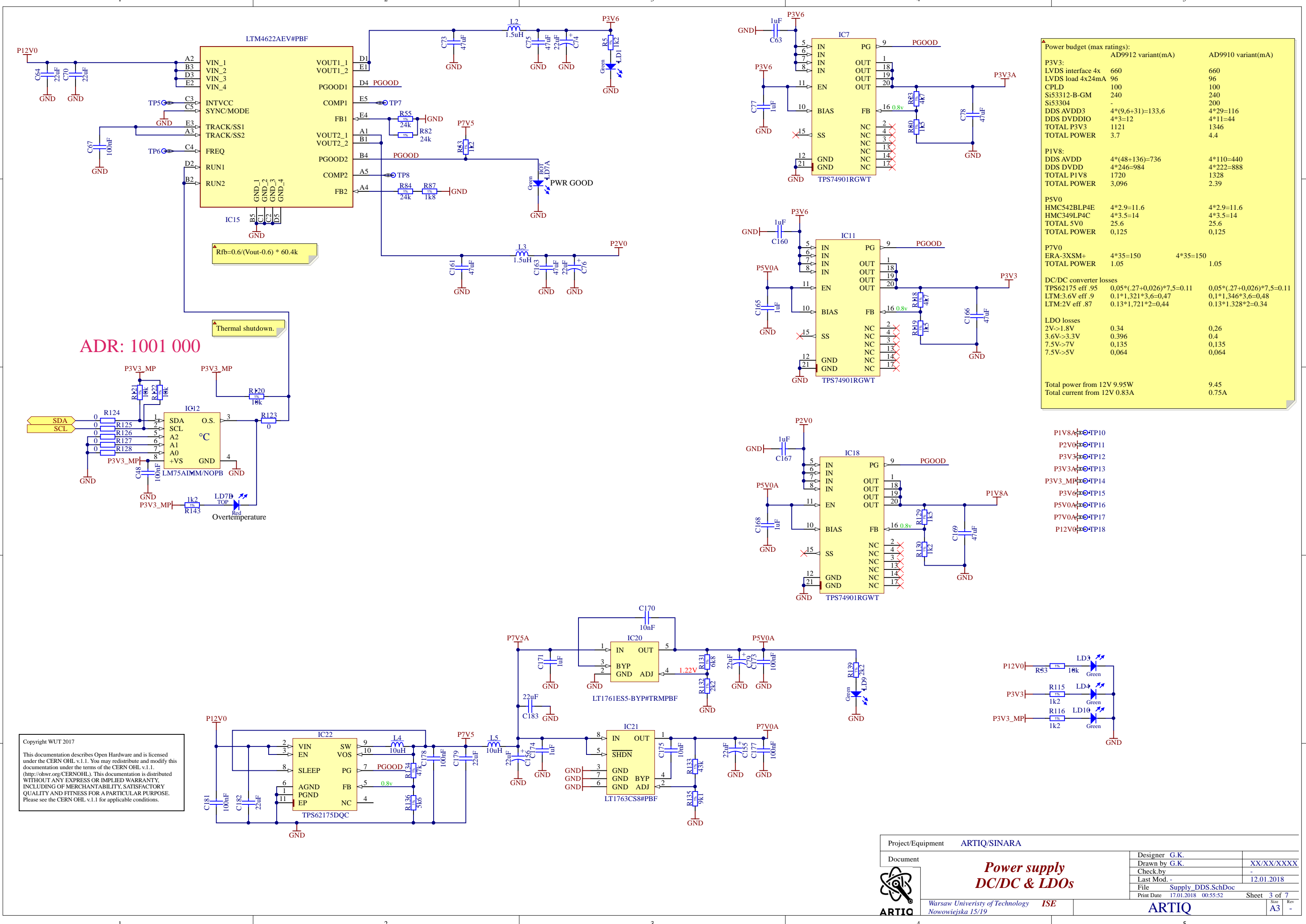
Warsaw Univeristy of Technology **ISE**
Nowowiejska 15/19

ARTIQ



EEM connector: IO are LVDS, I2C is 3V3 LVCMOS, P3V3_MP up to 20mA, P12V up to 1A





| Power budget (max ratings): | | |
|------------------------------|---------------------------|---------------------------|
| | AD9912 variant(mA) | AD9910 variant(mA) |
| P3V3: | | |
| LVDS interface 4x | 660 | 660 |
| LVDS load 4x24mA | 96 | 96 |
| CPLD | 100 | 100 |
| Si53312-B-GM | 240 | 240 |
| Si53304 | - | 200 |
| DDS AVDD3 | 4*(9,6+31)=133,6 | 4*29=116 |
| DDS DVDDIO | 4*3=12 | 4*11=44 |
| TOTAL P3V3 | 1121 | 1346 |
| TOTAL POWER | 3,7 | 4,4 |
| P1V8: | | |
| DDS AVDD | 4*(48+136)=736 | 4*110=440 |
| DDS DVDD | 4*246=984 | 4*222=888 |
| TOTAL P1V8 | 1720 | 1328 |
| TOTAL POWER | 3,096 | 2,39 |
| P5V0 | | |
| HMC542BLP4E | 4*2,9=11,6 | 4*2,9=11,6 |
| HMC349LP4C | 4*3,5=14 | 4*3,5=14 |
| TOTAL 5V0 | 25,6 | 25,6 |
| TOTAL POWER | 0,125 | 0,125 |
| P7V0 | | |
| ERA-3XSM+ | 4*35=150 | 4*35=150 |
| TOTAL POWER | 1,05 | 1,05 |
| DC/DC converter losses | | |
| TPS62175 eff. 95 | 0,05*(,27+0,026)*7,5=0,11 | 0,05*(,27+0,026)*7,5=0,11 |
| LTM:3.6V eff. 9 | 0,1*1,321*3,6=0,47 | 0,1*1,346*3,6=0,48 |
| LTM:2V eff. 87 | 0,13*1,721*2=0,44 | 0,13*1,328*2=0,34 |
| LDO losses | | |
| 2V->1.8V | 0,34 | 0,26 |
| 3.6V->3.3V | 0,396 | 0,4 |
| 7.5V->7V | 0,135 | 0,135 |
| 7.5V->5V | 0,064 | 0,064 |
| Total power from 12V 9.95W | | 9.45 |
| Total current from 12V 0.83A | | 0.75A |

- P1V8A1-TP10
- P2V0A1-TP11
- P3V3A1-TP12
- P3V3A2-TP13
- P3V3_MP1-TP14
- P3V3_MP2-TP15
- P5V0A1-TP16
- P7V0A1-TP17
- P12V0A1-TP18

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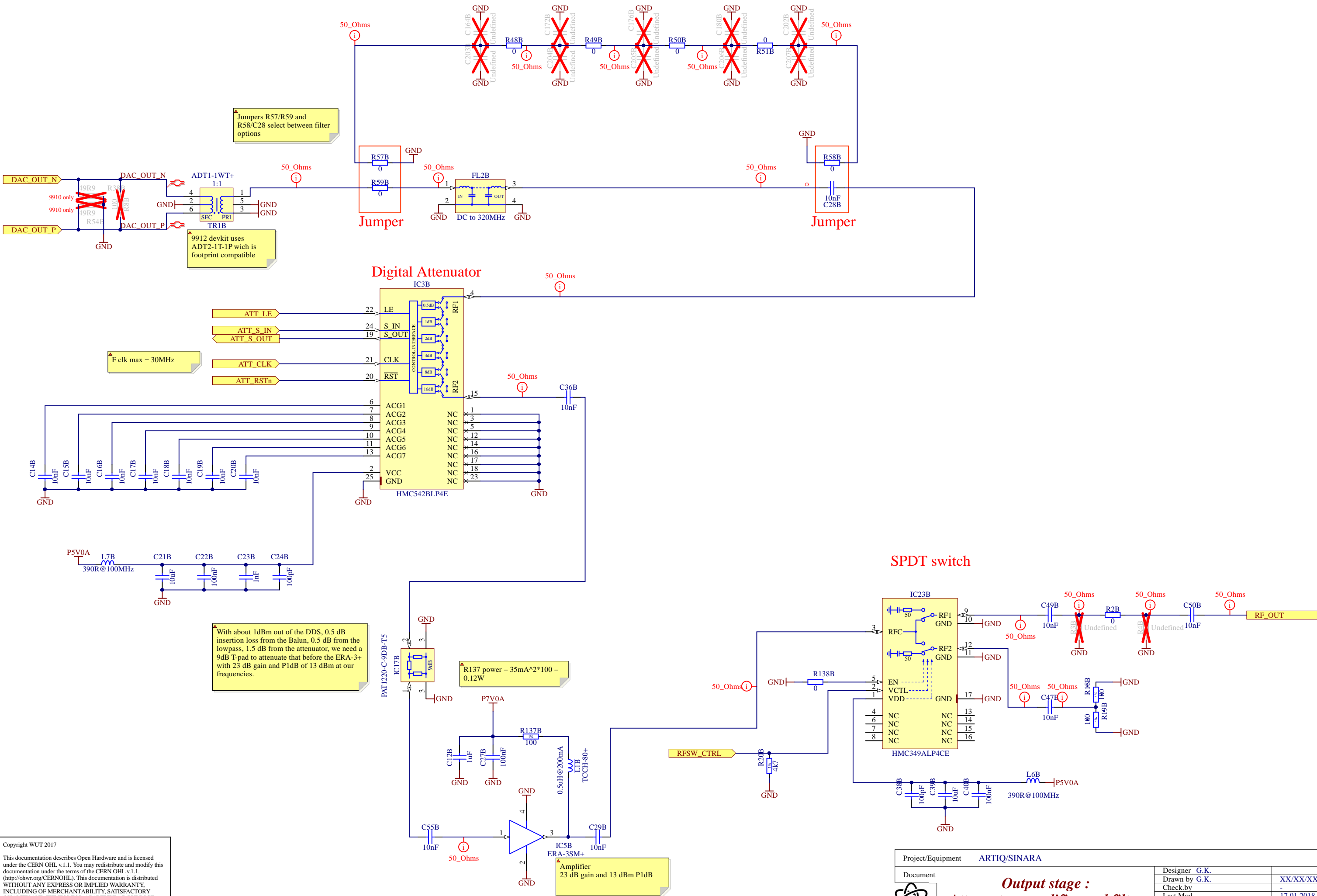
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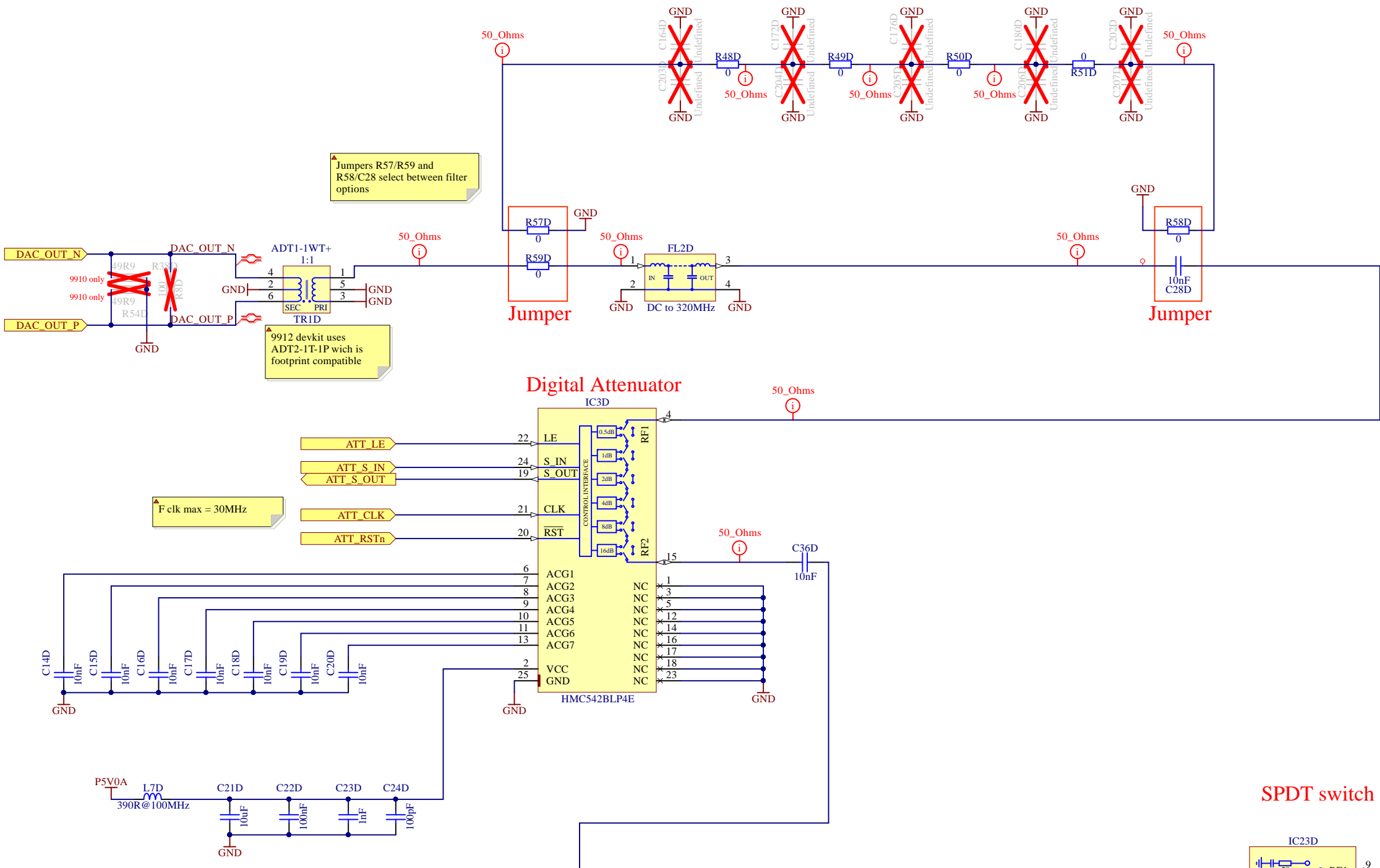
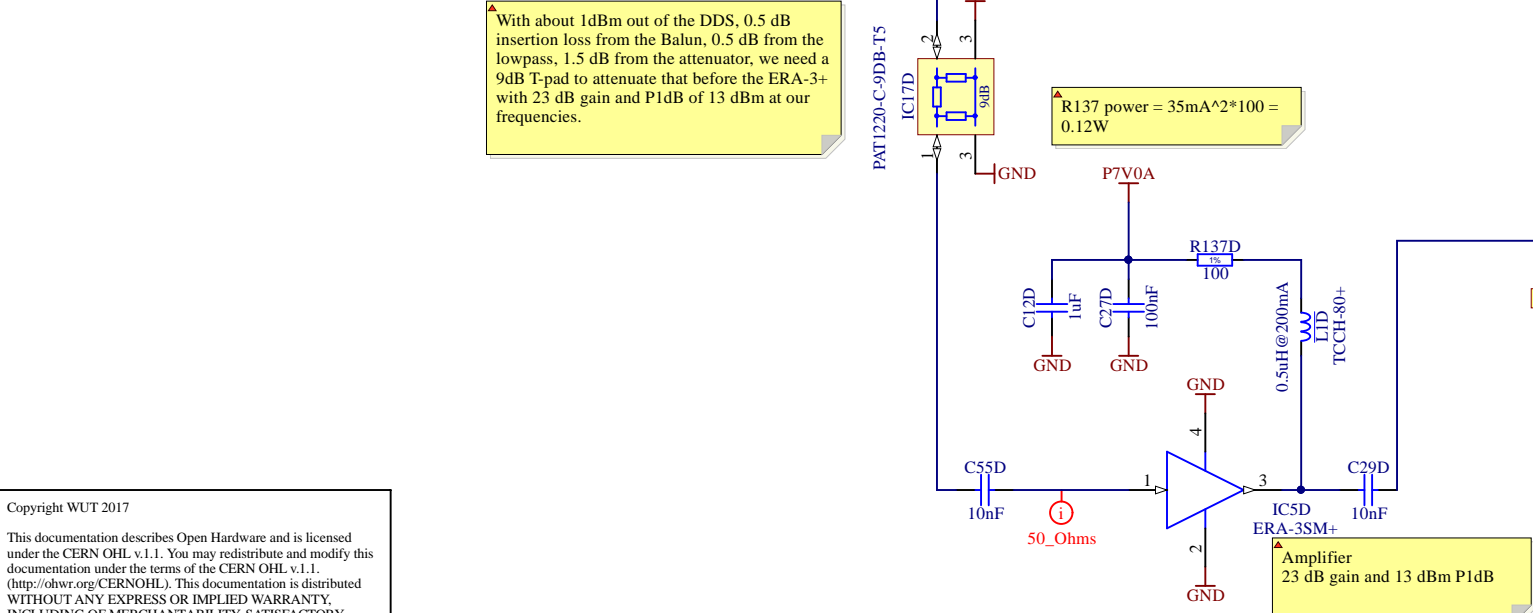
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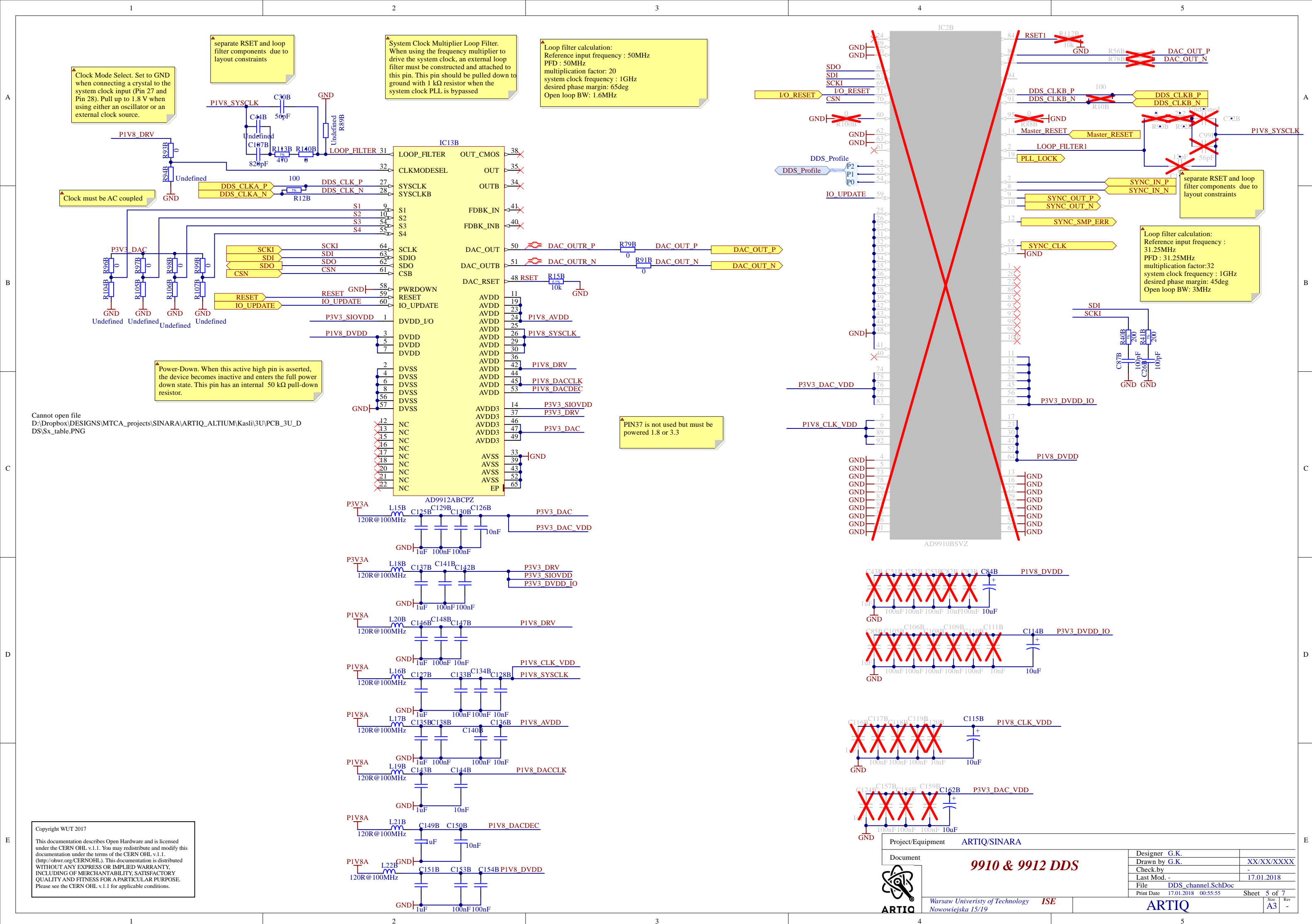
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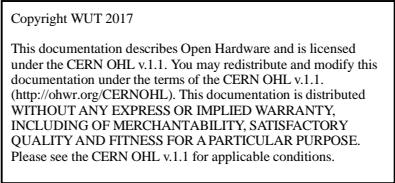
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|--|--|------------------------|--------------|
| Project/Equipment | | ARTIQ/SINARA | |
| Document | | Designer | G.K. |
| <div>ARTIQ</div> <div>Warsaw University of Technology</div> <div>Nowowiejska 15/19</div> | | Drawn by | G.K. |
| | | Check by | - |
| | | Last Mod. | 17.01.2018 |
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| Print Date | | 17.01.2018 00:55:53 | Sheet 4 of 7 |
| | | Size | A3 |
| | | Rev | - |

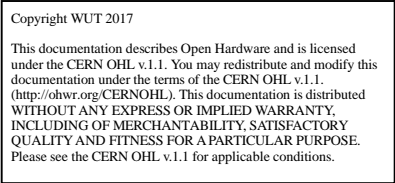
Output stage :
Attenuator, amplifier and filter

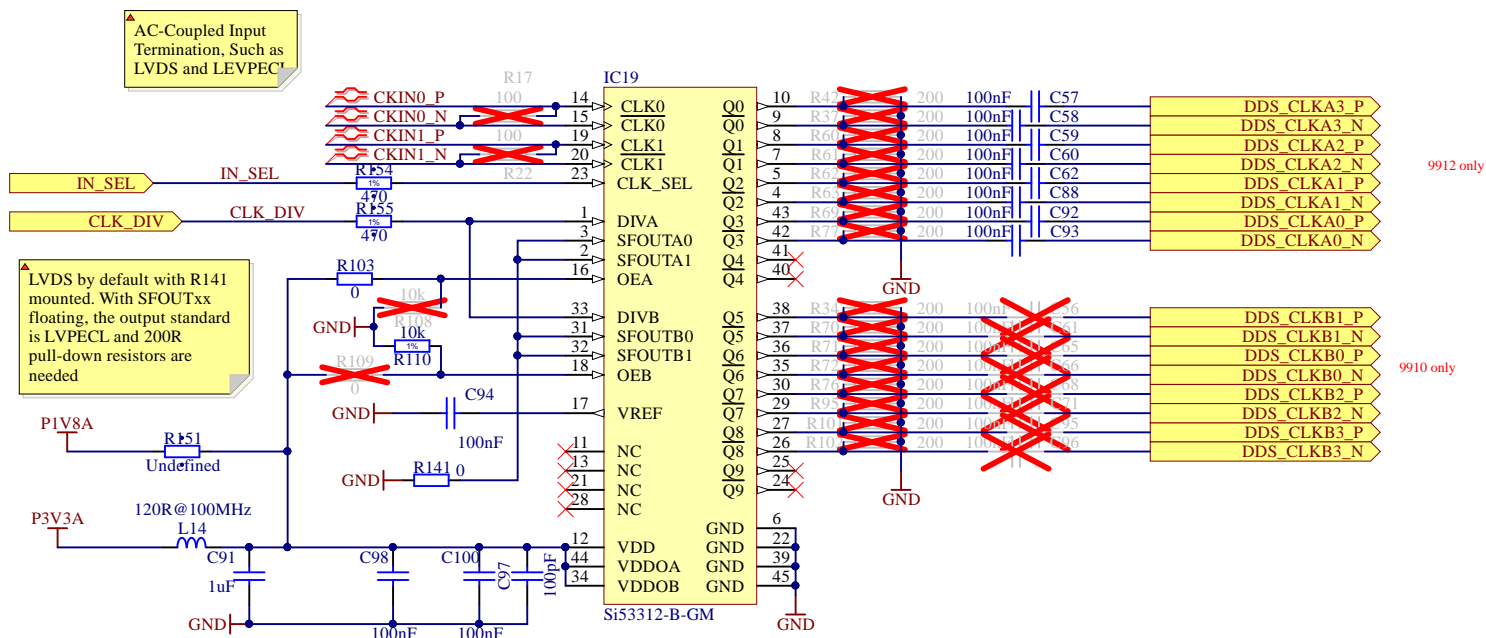
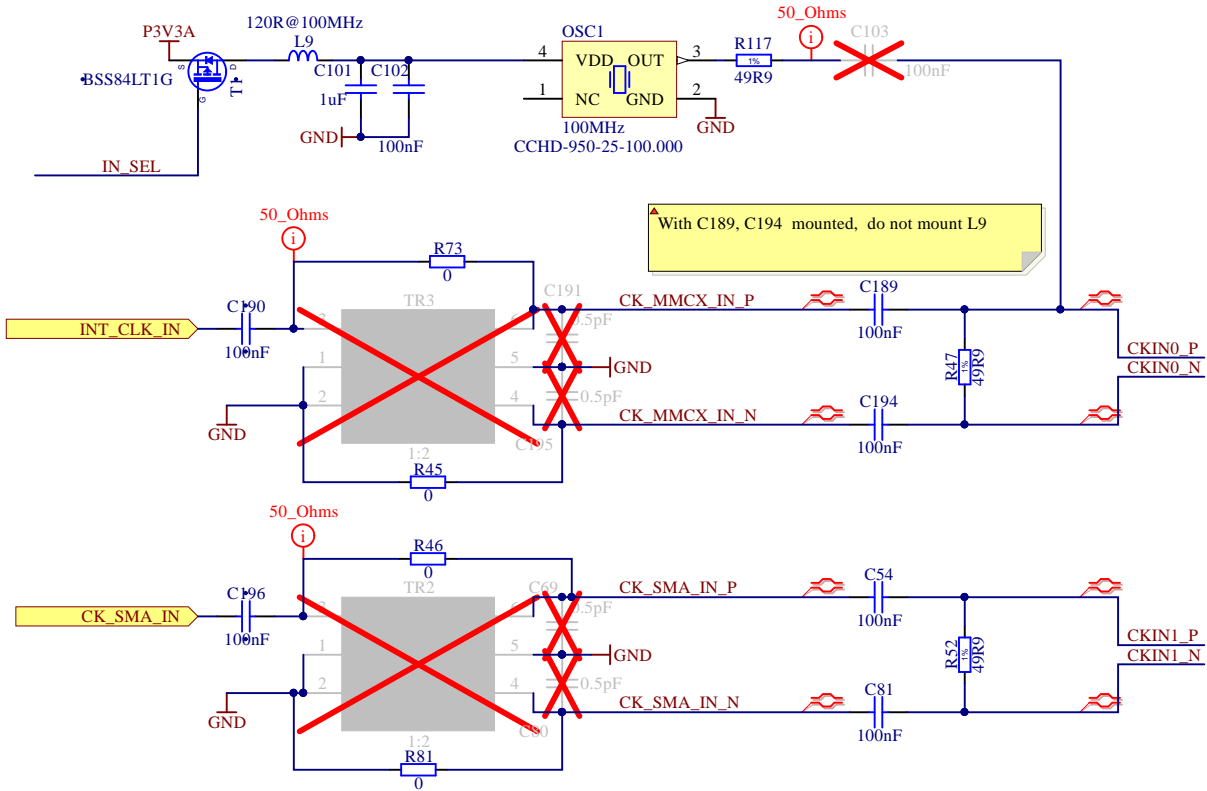








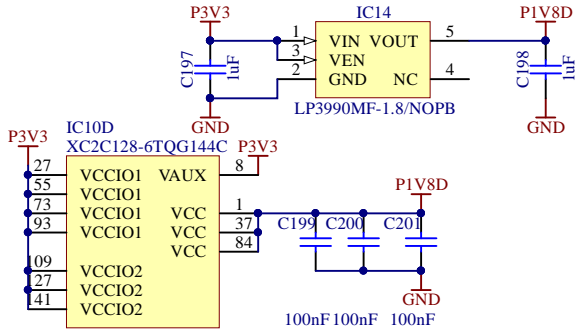
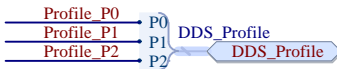
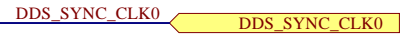
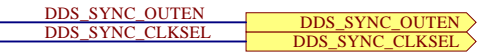
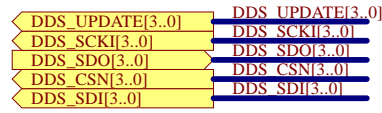
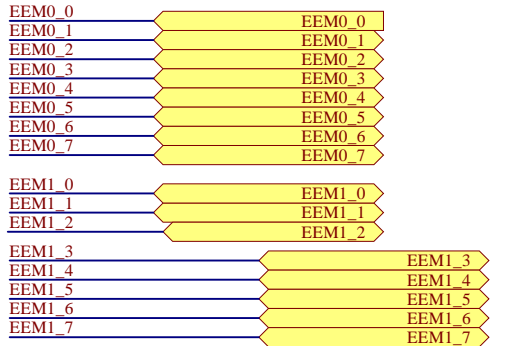
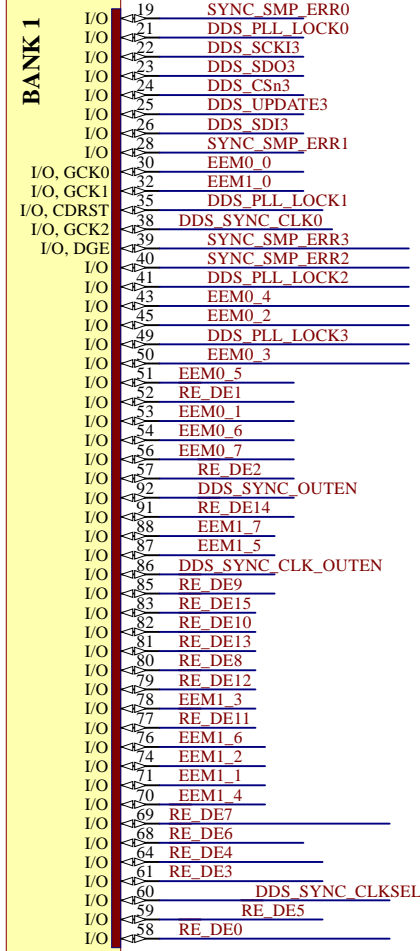




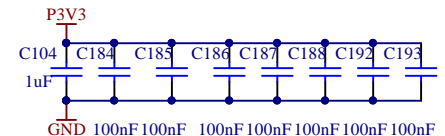
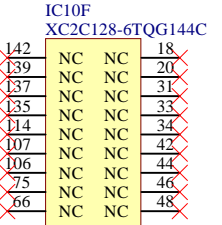
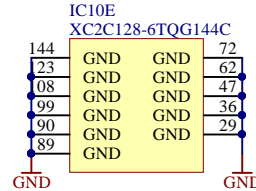
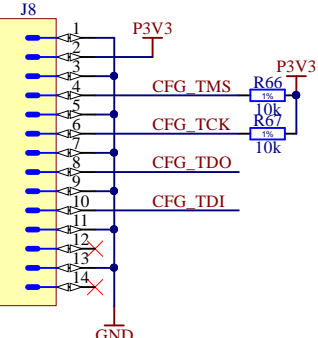
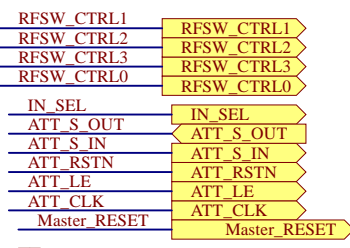
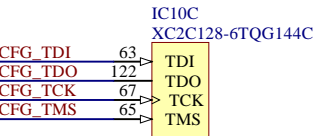
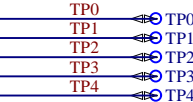
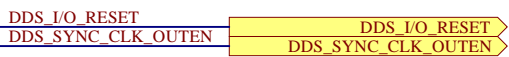
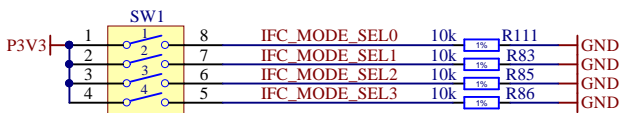
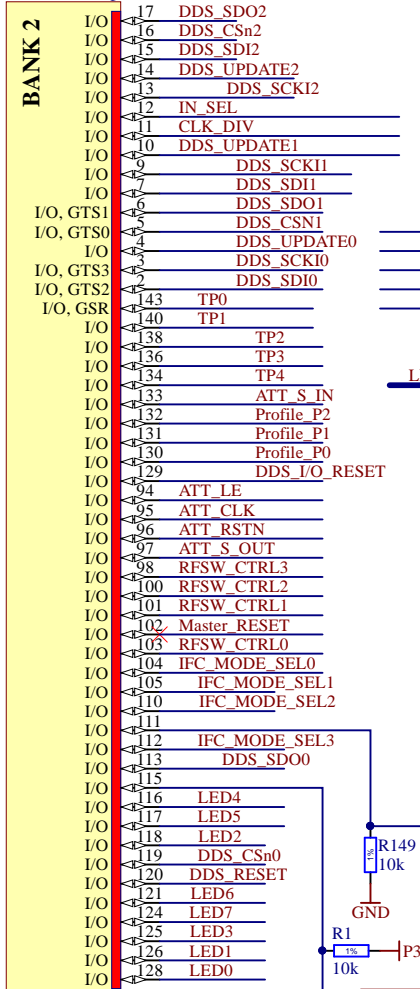
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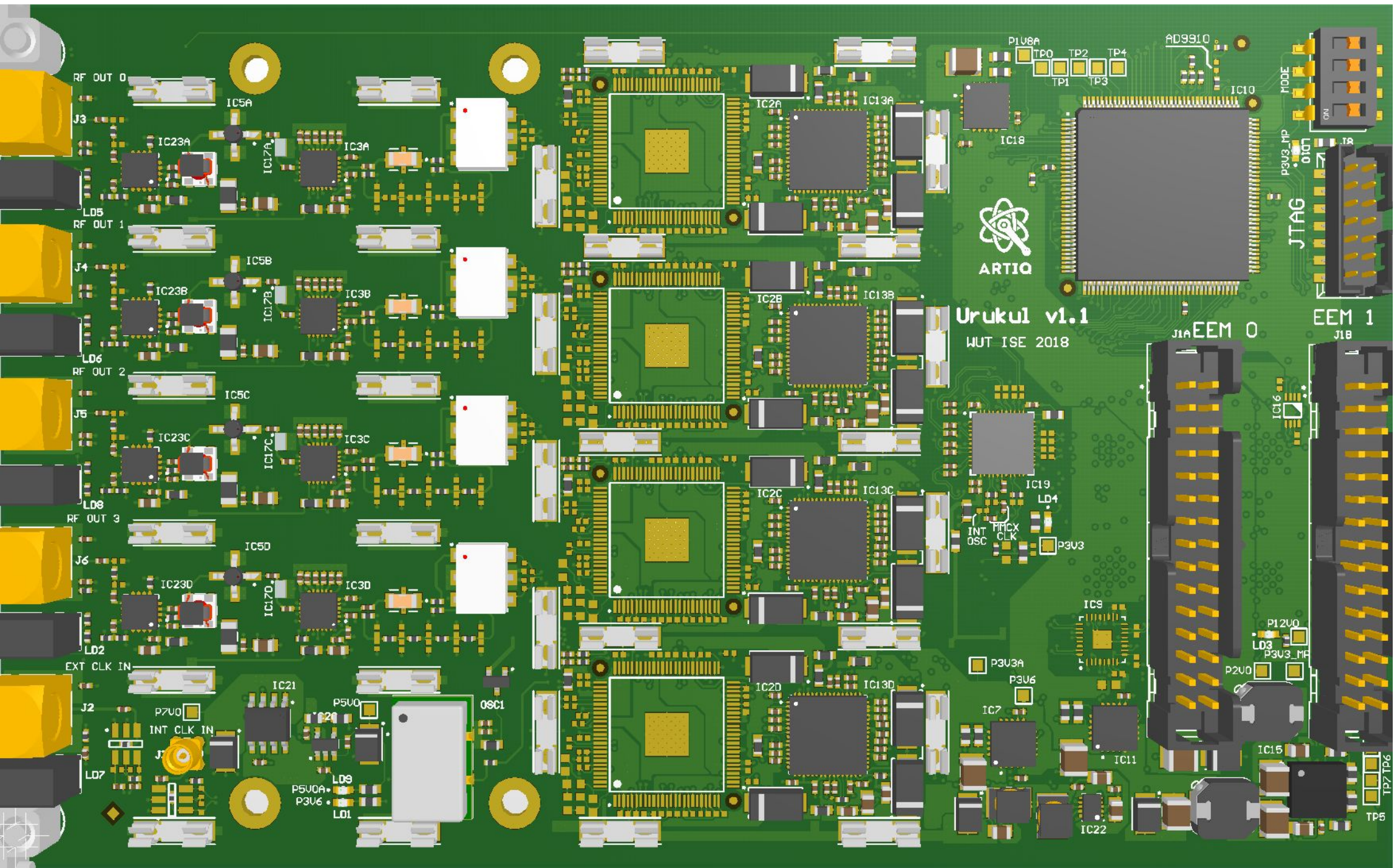
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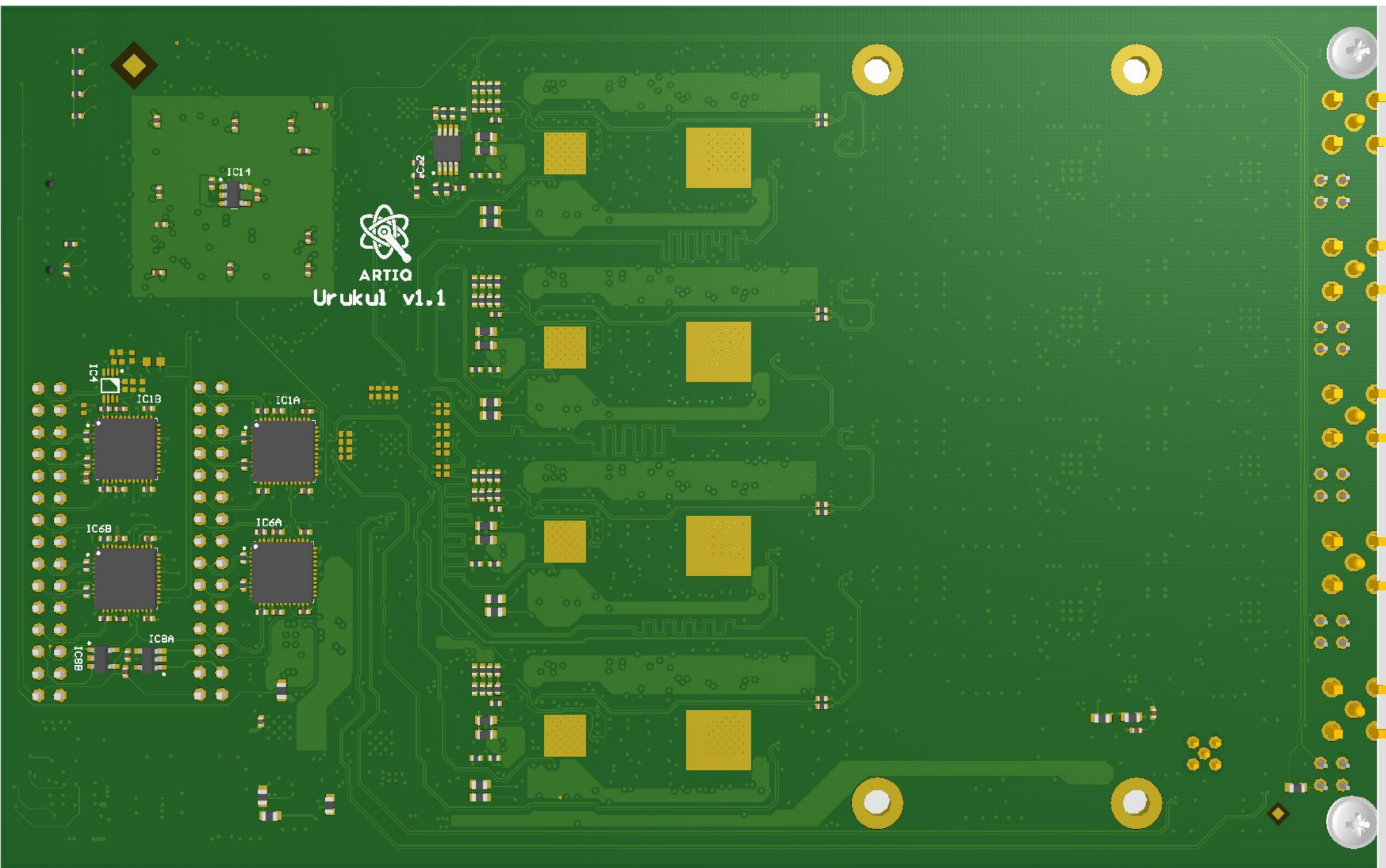


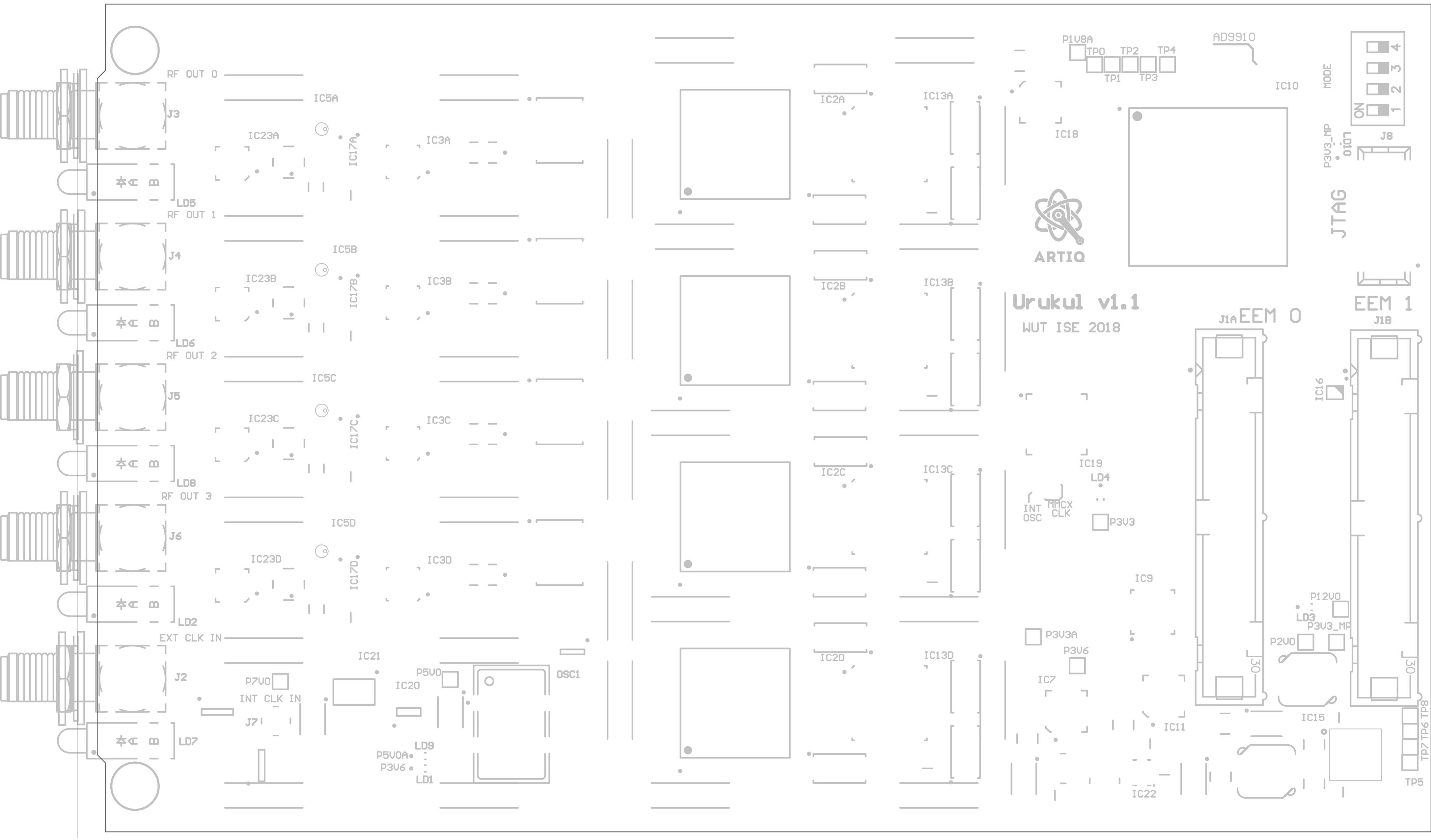
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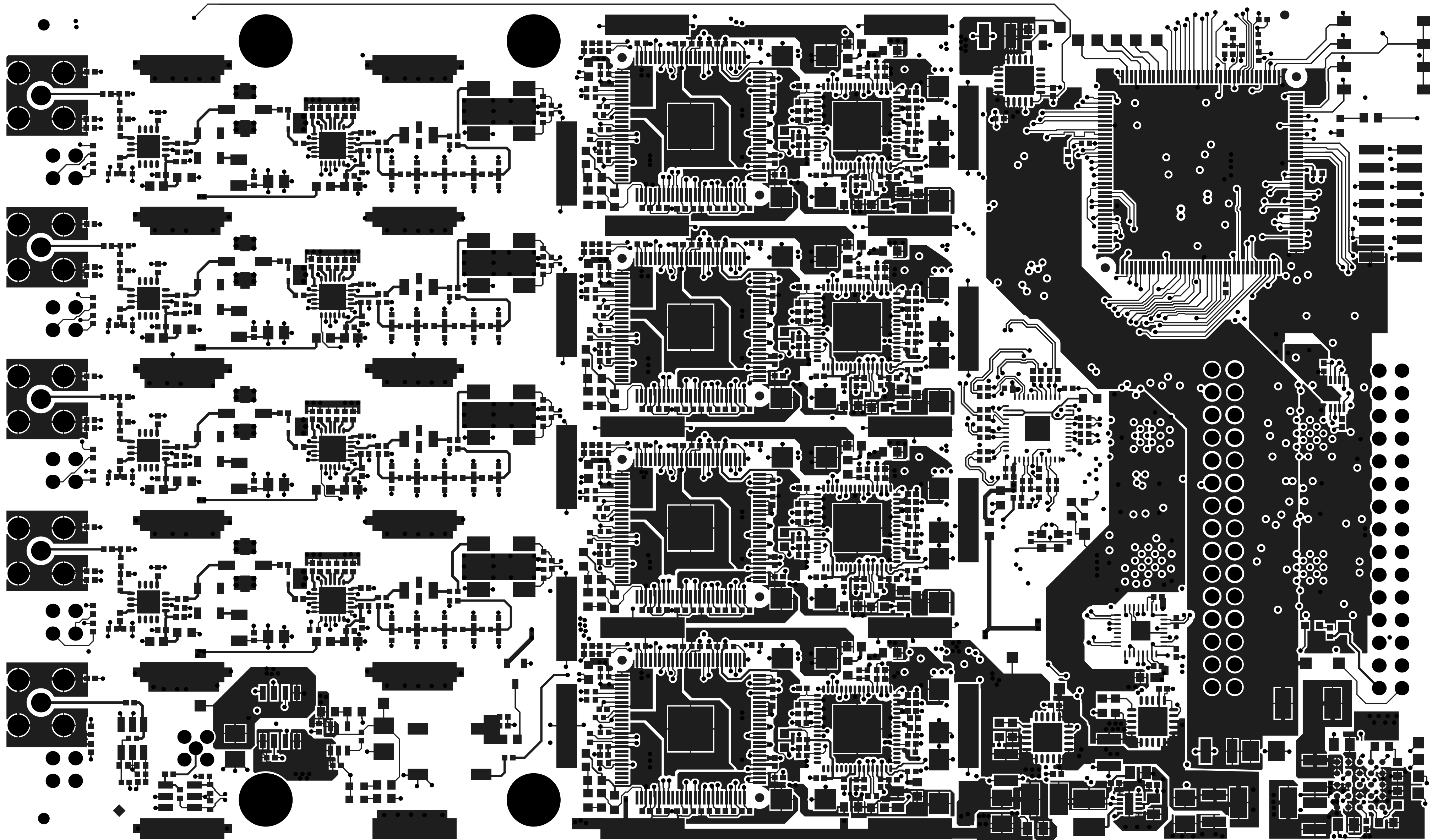
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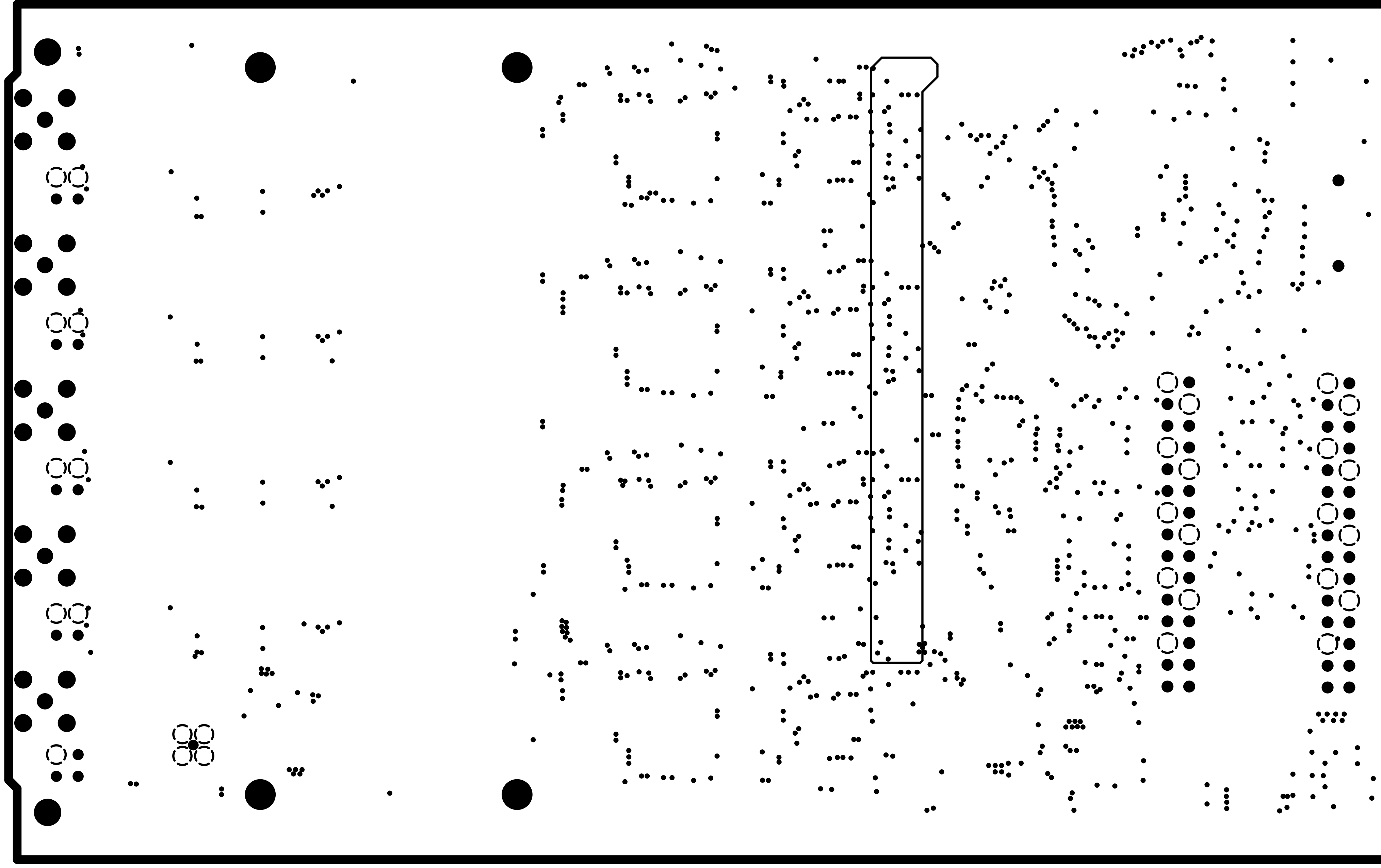
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| Project/Equipment | | ARTIQ/SINARA | |
| Document | | Designer | G.K. |
| CPLD logic & option switches | | Drawn by | G.K. |
| | | Check by | - |
| | | Last Mod. | 17.01.2018 |
| File | | CTRL_LOGIC.SchDoc | |
| Print Date | | 17.01.2018 00:55:57 | Sheet 7 of 7 |
| Warsaw University of Technology | | ISE | ARTIQ |
| Nowowiejska 15/19 | | Size | A3 |
| | | Rev | - |

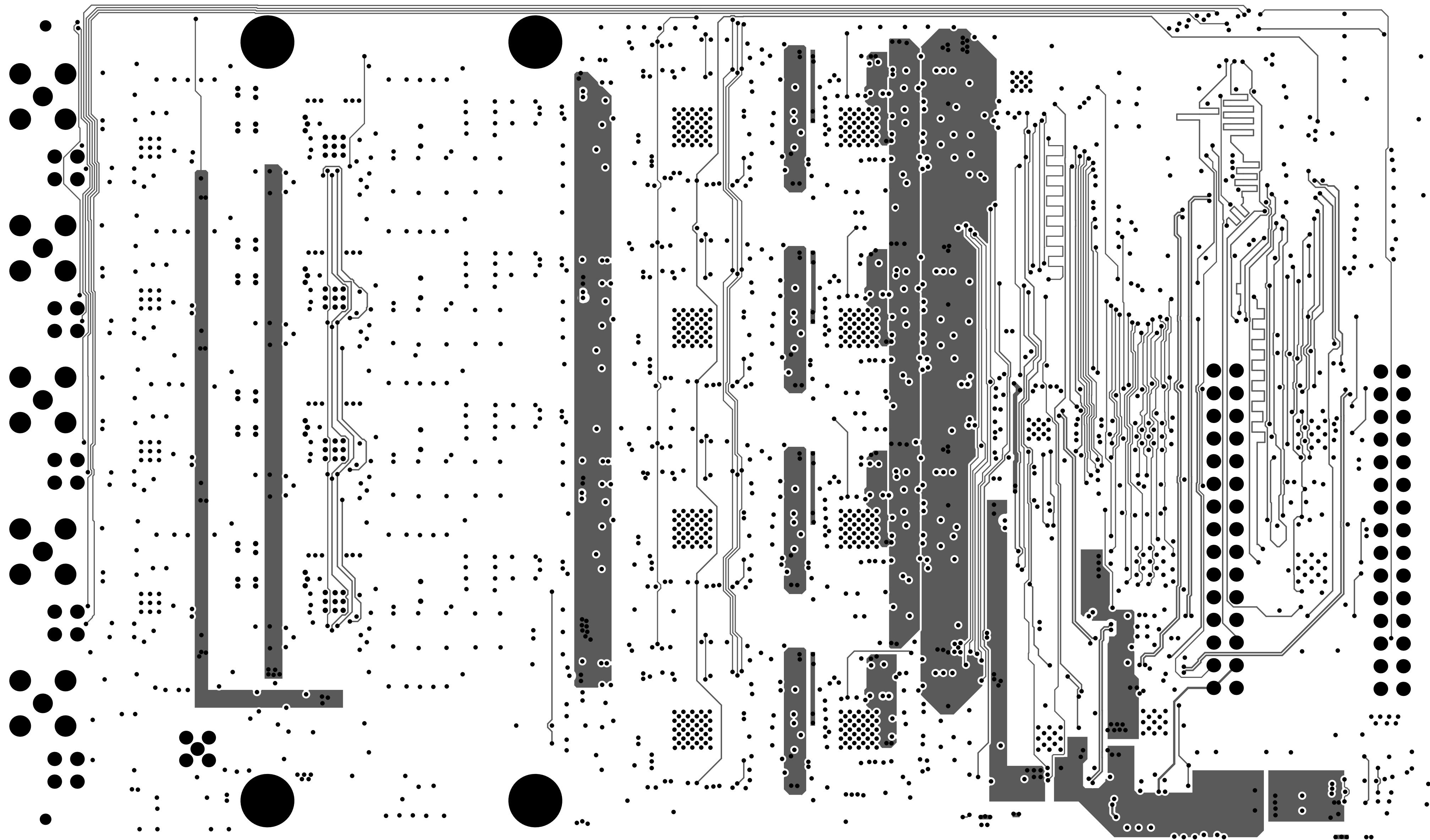


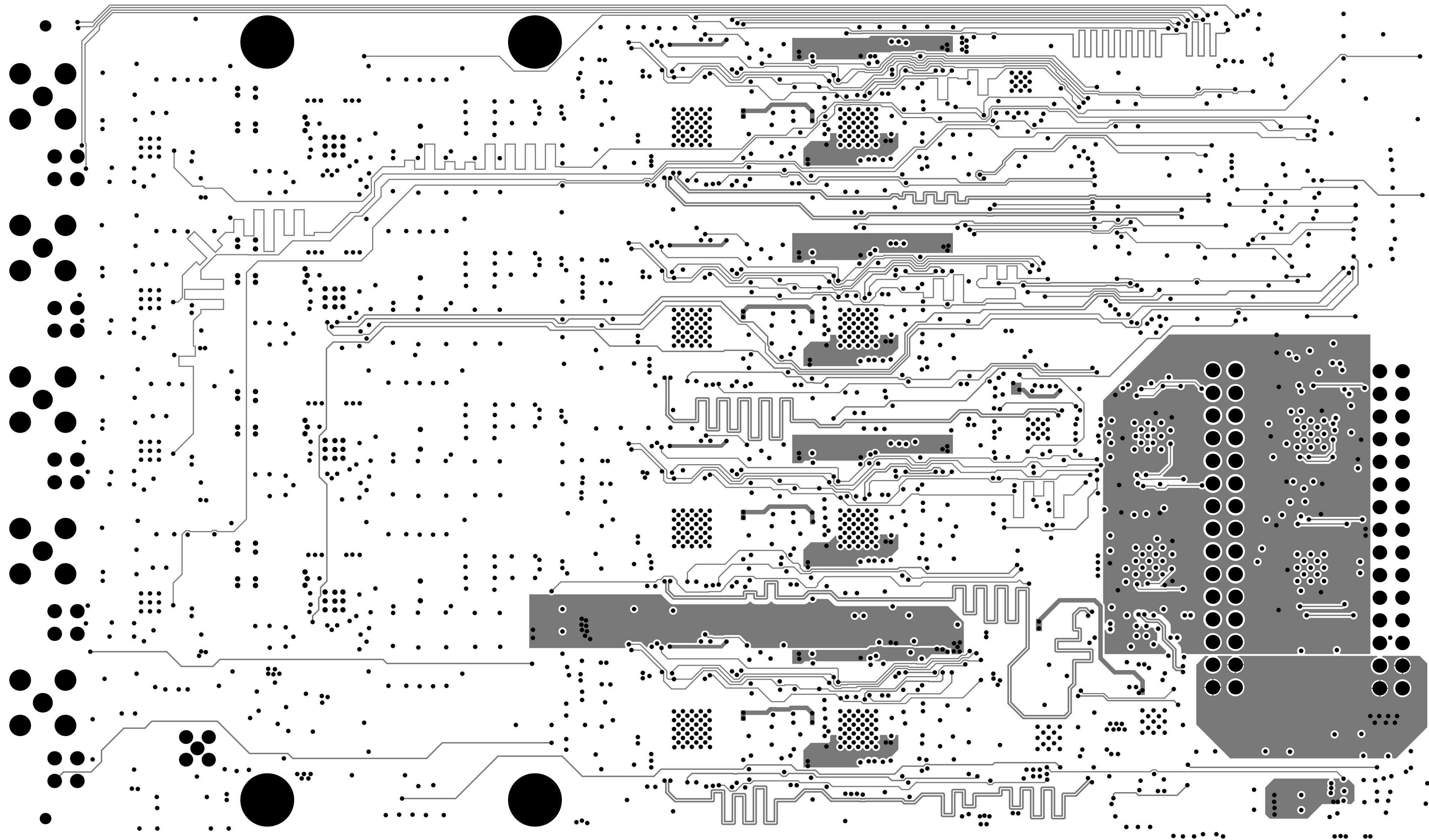


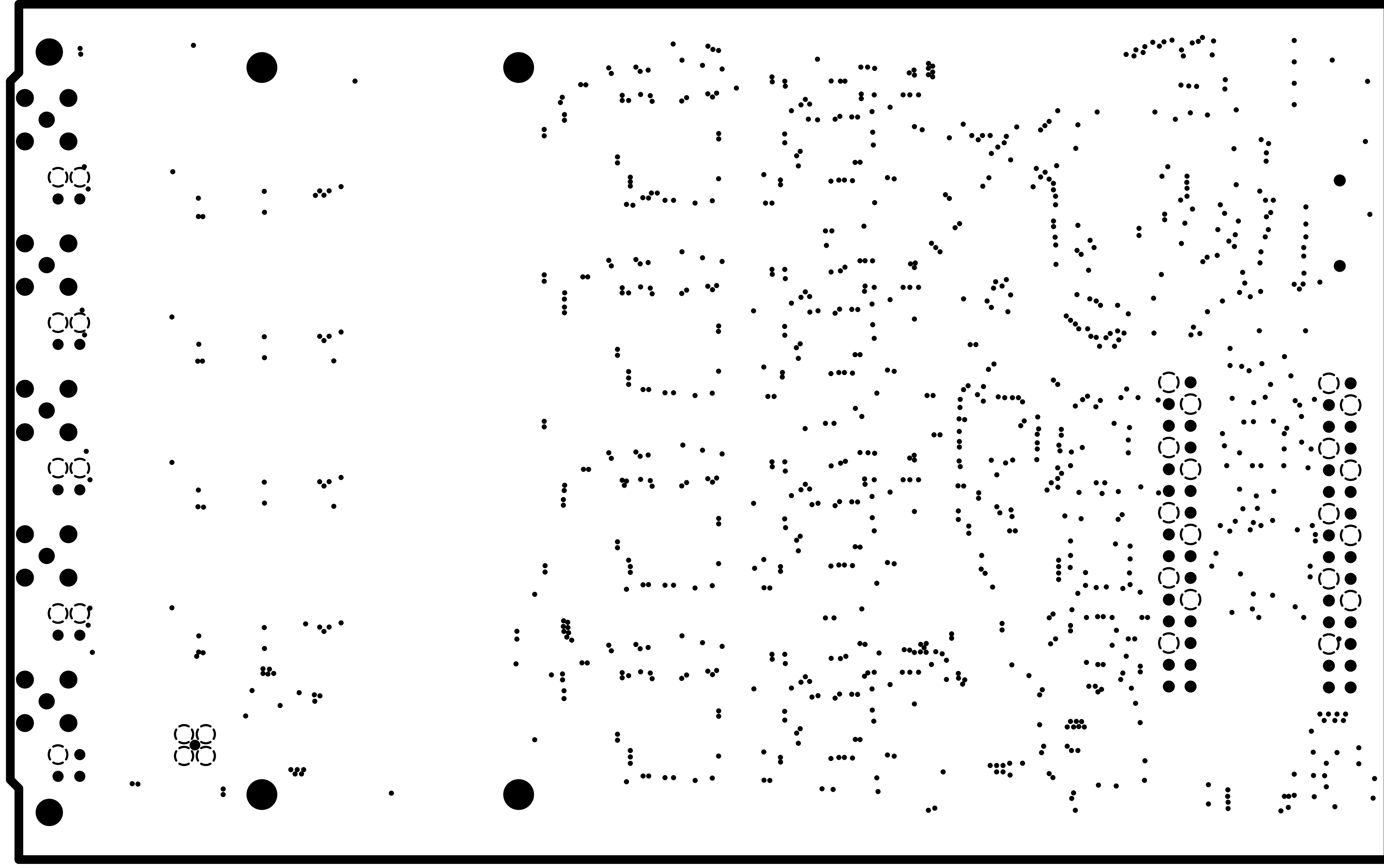


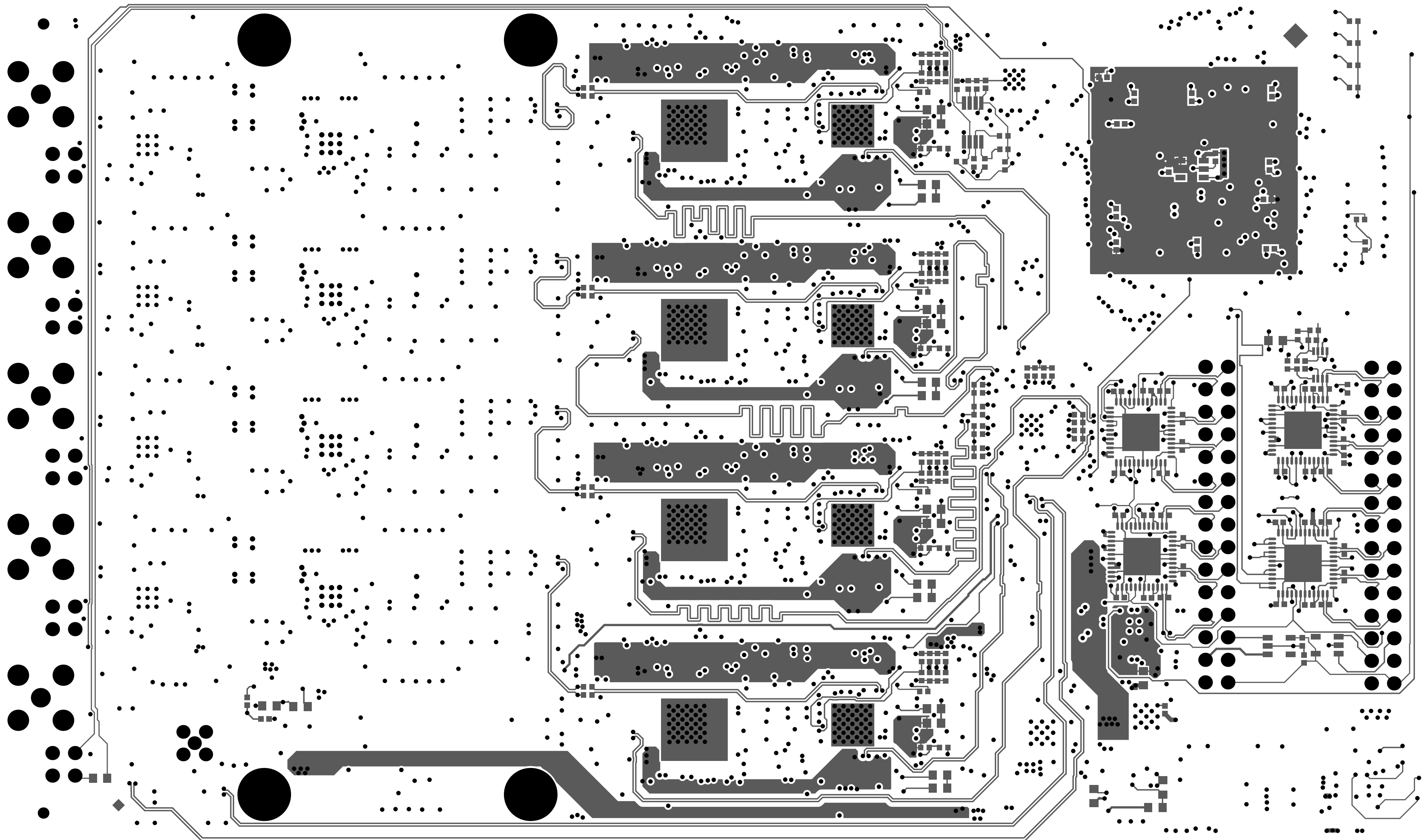














Urknul v1.1
ARTIO



IC1B

IC1B

IC9A

IC9B

IC8A

IC8B