shield clips

CLIP1 CLIP2 CLIP3 CLIP4 CLIP5 CLIP30 CLIP31 — GND
CLIP6 CLIP7 CLIP8 CLIP9 CLIP10 CLIP27 — GND
CLIP11 CLIP12 CLIP13 CLIP14 CLIP15 CLIP28 — GND
CLIP16 CLIP17 CLIP18 CLIP19 CLIP20 CLIP29 — GND
CLIP21 CLIP22 CLIP23 CLIP24 CLIP25 CLIP26 — GND

Ext clock input

GND — 10nF C37 — 10nF C42 — GND
GND — 0 R6 — SG0
SMA J2 — 50_Ohms
IN_SEL
CLK_DIV

Clock from Kasli

J7 MMCX — GND — 50_Ohms

DDS_CLK

U_CLK_INPUT
CLK_INPUT.SchDoc

CK_SMA_IN
IN_SEL
CLK_DIV
INT_CLK_IN

DDS_CLKA0_P DDS_CLKA0_N DDS_CLKA1_P DDS_CLKA1_N DDS_CLKA2_P DDS_CLKA2_N DDS_CLKA3_P DDS_CLKA3_N DDS_CLKB0_P DDS_CLKB0_N DDS_CLKB1_P DDS_CLKB1_N DDS_CLKB2_P DDS_CLKB2_N DDS_CLKB3_P DDS_CLKB3_N

Output SMAs

GND — 10nF C11 — SG1
GND — 0 R64 — 10nF C25 — GND
SMA J3 — RF_OUT0 — 50_Ohms
GND — 10nF C31 — SG2
GND — 0 R65 — 10nF C32 — GND
SMA J4 — RF_OUT1 — 50_Ohms
GND — 10nF C33 — SG3
GND — 0 R74 — 10nF C34 — GND
SMA J5 — RF_OUT2 — 50_Ohms
GND — 10nF C35 — SG4
GND — 0 R75 — 10nF C41 — GND
SMA J6 — RF_OUT3 — 50_Ohms

ATT_CLK
ATT_LE
ATT_RSTn
ATT_S_IN
ATT_S_OUT

U_DDS_OUT_channel0
DDS_OUT_channel.SchDoc
U_DDS_OUT_channel1
DDS_OUT_channel.SchDoc
U_DDS_OUT_channel2
DDS_OUT_channel.SchDoc
U_DDS_OUT_channel3
DDS_OUT_channel.SchDoc

DAC_OUT_P DAC_OUT_N ATT_CLK RFSW_CTRL ATT_LE ATT_RSTn ATT_S_IN ATT_S_OUT

RFSW_CTRL0
RFSW_CTRL1
RFSW_CTRL2
RFSW_CTRL3

U_CTRL_LOGIC
CTRL_LOGIC.SchDoc

RFSW_CTRL0 RFSW_CTRL1 RFSW_CTRL2 RFSW_CTRL3
DDS_SDO[3..0] DDS_SDI[3..0] DDS_SCKI[3..0] DDS_CSn[3..0] IN_SEL CLK_DIV DDS_UPDATE[3..0] DDS_SYNC_CLK0 DDS_PLL_LOCK[3..0] SYNC_SMP_ERR[3..0] DDS_Profile DDS_I/O_RESET DDS_RESET LED[7..0] ATT_CLK ATT_LE ATT_RSTn ATT_S_IN ATT_S_OUT
RE_DE[15..0]
IO0_CLK IO_A1 IO_A2 IO_A3 IO_A4 IO_A5 IO_A6 IO_A7 IO_B8_SCKI IO_B9 IO_B10 IO_B11 IO_B12 IO_B13 IO_B14 IO_B15
DDS_SYNC_CLKSEL DDS_SYNC_OUTEN DDS_SYNC_CLK_OUTEN

RE_DE[15..0]

LVDS_IFC_DDS.SchDoc U_LVDS_IFCA

IO0 IO1 IO2 IO3 IO4 IO5 IO6 IO7 LVDS0_P LVDS0_N LVDS1_P LVDS1_N LVDS7_P LVDS7_N
I2C_SDA I2C_SCL
RE_DE0 RE_DE1 RE_DE2 RE_DE3 RE_DE4 RE_DE5 RE_DE6 RE_DE7
EEM A
SDA SCL
RE_DE0 RE_DE1 RE_DE2 RE_DE3 RE_DE4 RE_DE5 RE_DE6 RE_DE7

LVDS_IFC_DDS.SchDoc U_LVDS_IFCB

IO0 IO1 IO2 IO3 IO4 IO5 IO6 IO7 LVDS0_P LVDS0_N LVDS1_P LVDS1_N LVDS7_P LVDS7_N
I2C_SDA I2C_SCL
RE_DE0 RE_DE1 RE_DE2 RE_DE3 RE_DE4 RE_DE5 RE_DE6 RE_DE7
EEM B
RE_DE8 RE_DE9 RE_DE10 RE_DE11 RE_DE12 RE_DE13 RE_DE14 RE_DE15

DDS_SYNC_CLKSEL DDS_SYNC_OUTEN

DDS_SYNC_CLK0 — 1k R31 — IC4 FIN1101K8X
P3V3_CLK2 — 1k R36 — 100 R32 — C1 100n — C13 100n — GND

IC9

DDS0_SYNC_OUT_P DDS0_SYNC_OUT_N — 100 R68
DDS0_SYNC_IN_P DDS0_SYNC_IN_N DDS1_SYNC_IN_P DDS1_SYNC_IN_N DDS2_SYNC_IN_P DDS2_SYNC_IN_N DDS3_SYNC_IN_P DDS3_SYNC_IN_N
P3V3_CLK1 P3V3_CLK2 GND
Si53304-B-GM
120R@100MHz — P3V3 — L13 — C8 1uF — C9 100nF — C10 100nF

IC16 FIN1101K8X
R114 100
C46 100nF

Trace lengths matched within each of DDS_SYNC_CLK[3:0], DDS_UDPATE[3:0], RF_SW_CTRL[3:0], IO[15:11] (RF_SW ctrl lines), DDS_SYNC_IN[3:0], DDS_RESET[3:0], DDS_CLK[3:0]

U_DDS_channel0
DDS_channel.SchDoc
U_DDS_channel1
DDS_channel.SchDoc
U_DDS_channel2
DDS_channel.SchDoc
U_DDS_channel3
DDS_channel.SchDoc

DAC_OUT_P DAC_OUT_N SYNC_OUT_P SYNC_OUT_N SYNC_CLK I/O_RESET RESET SYNC_IN_P SYNC_IN_N
SDO SDI SCKI CSN IO_UPDATE PLL_LOCK SYNC_SMP_ERR DDS_Profile DDS_CLKA_P DDS_CLKA_N DDS_CLKB_P DDS_CLKB_N

DDS_SDO0 DDS_SDI0 DDS_SCKI0 DDS_CSn0 DDS_UPDATE0 DDS_PLL_LOCK0 SYNC_SMP_ERR0 DDS_Profile DDS_CLKA0_P DDS_CLKA0_N DDS_CLKB0_P DDS_CLKB0_N
DDS_SDO1 DDS_SDI1 DDS_SCKI1 DDS_CSn1 DDS_UPDATE1 DDS_PLL_LOCK1 SYNC_SMP_ERR1 DDS_Profile DDS_CLKA1_P DDS_CLKA1_N DDS_CLKB1_P DDS_CLKB1_N
DDS_SDO2 DDS_SDI2 DDS_SCKI2 DDS_CSn2 DDS_UPDATE2 DDS_PLL_LOCK2 SYNC_SMP_ERR2 DDS_Profile DDS_CLKA2_P DDS_CLKA2_N DDS_CLKB2_P DDS_CLKB2_N
DDS_SDO3 DDS_SDI3 DDS_SCKI3 DDS_CSn3 DDS_UPDATE3 DDS_PLL_LOCK3 SYNC_SMP_ERR3 DDS_Profile DDS_CLKA3_P DDS_CLKA3_N DDS_CLKB3_P DDS_CLKB3_N

DDS0_SYNC_OUT_P DDS0_SYNC_OUT_N DDS_SYNC_CLK0 DDS_I/O_RESET DDS_RESET DDS0_SYNC_IN_P DDS0_SYNC_IN_N
DDS1_SYNC_IN_P DDS1_SYNC_IN_N
DDS2_SYNC_IN_P DDS2_SYNC_IN_N
DDS3_SYNC_IN_P DDS3_SYNC_IN_N

U_Supply_DDS
Supply_DDS.SchDoc
SDA SCL

FTG1 FTG2 FTG3 FTG4

LED0 LED1 LED2 LED3 LED4 LED5 LED6 LED7 — R27 R28 R29 R30 R43 R44 R25 R26 — 1% 470 — LD5A LD5B LD6A LD6B LD8A LD8B LD2A LD2B — BOT TOP — Green Red
DDS0 LEDs
DDS1 LEDs
DDS2 LEDs
DDS3 LEDs

Project/Equipment ARTIQ/SINARA

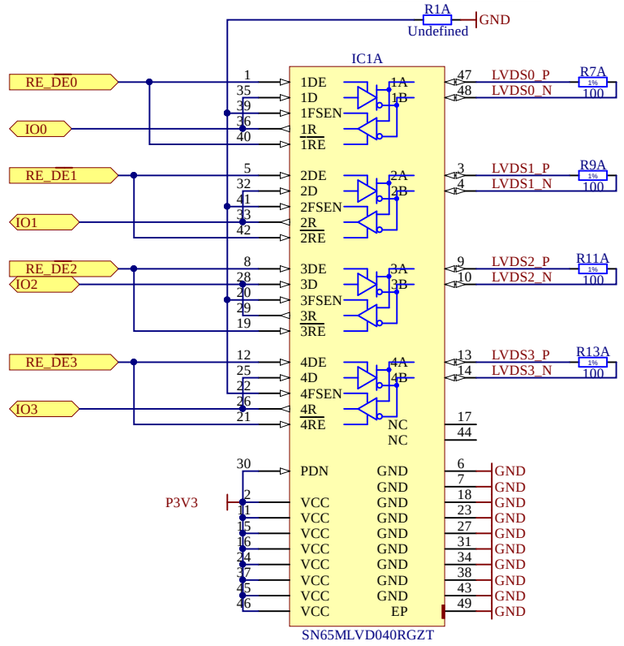
Document **3U DDS (URUKUL)** *Top entity*

Warsaw Univeristy of Technology *ISE*
Nowowiejska 15/19

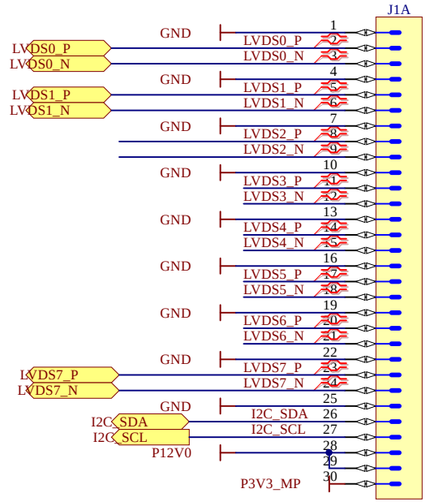
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.10.2017
File	PCB_3U_DDS.schdoc
Print Date	17.10.2017 12:22:49 Sheet 1 of 7

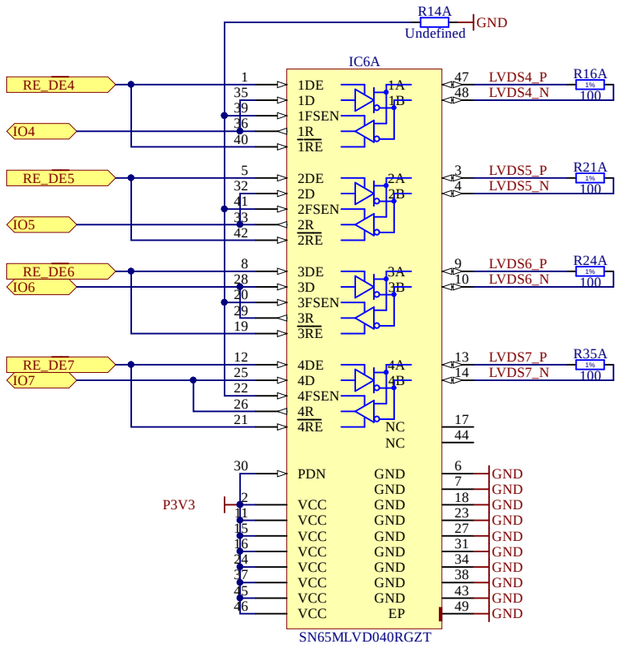
ARTIQ — Size A3 — Rev -

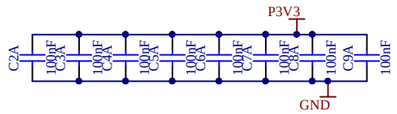
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

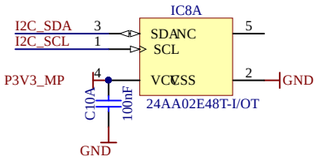


EEM Connector
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A



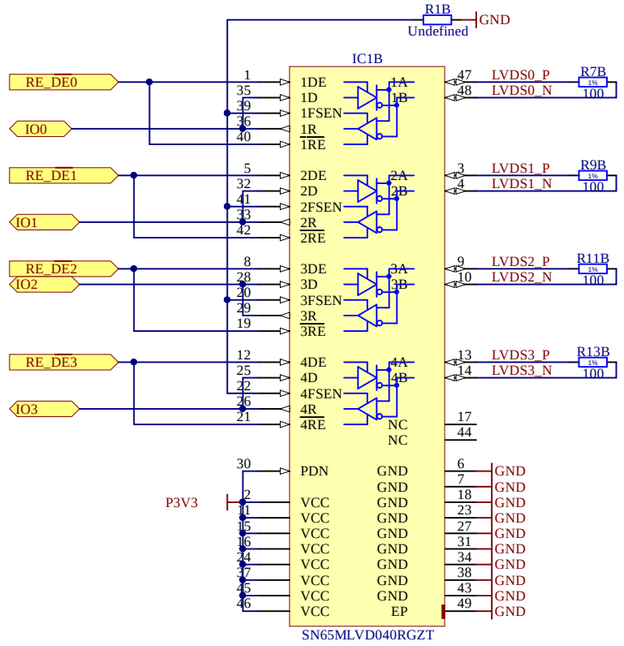




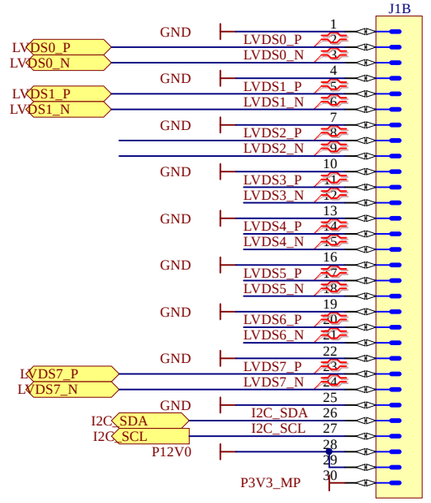


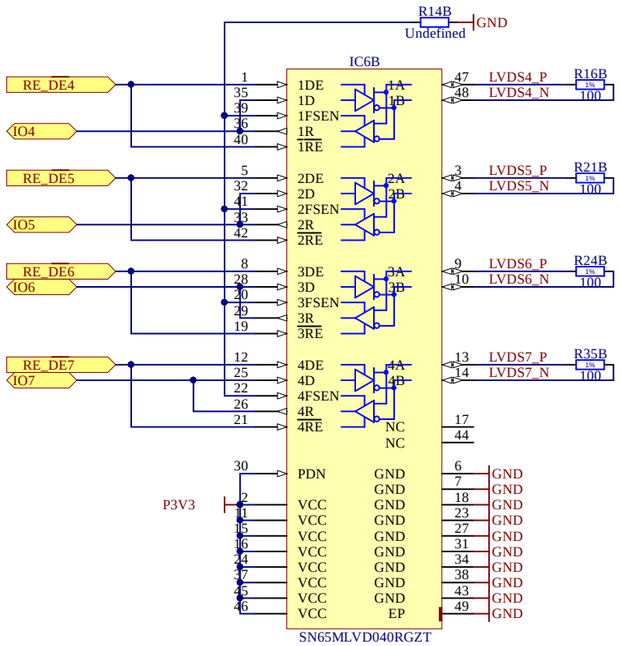
Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	10.10.2017
		File LVDS_IFC_DDS.SchDoc	
		Print Date 17.10.2017 12:22:49	Sheet 2 of 7
Warsaw Univeristy of Technology *Nowowiejska 15/19*	*ISE*	ARTIQ	Size A3 / Rev -

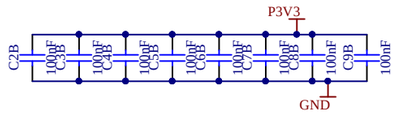
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

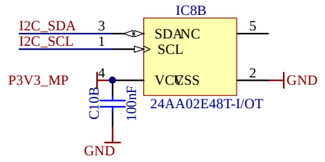


EEM Connector
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A

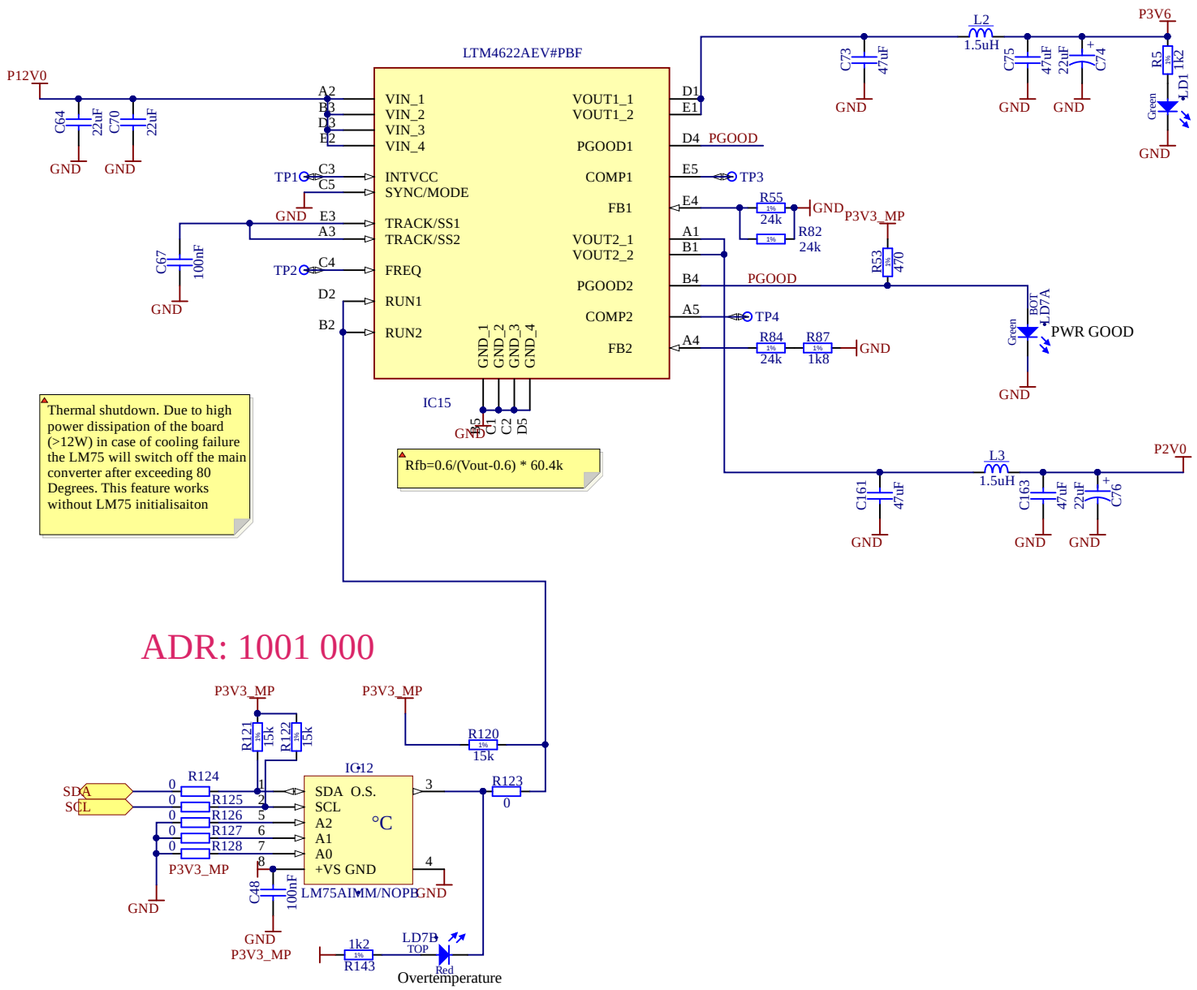




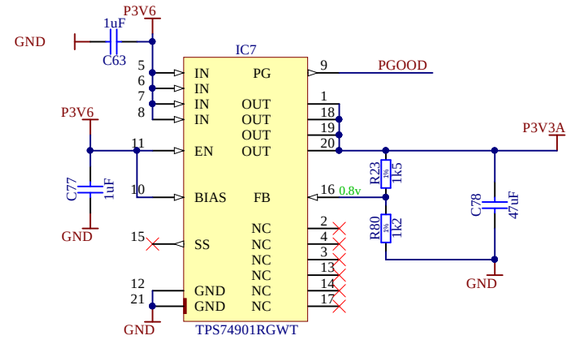


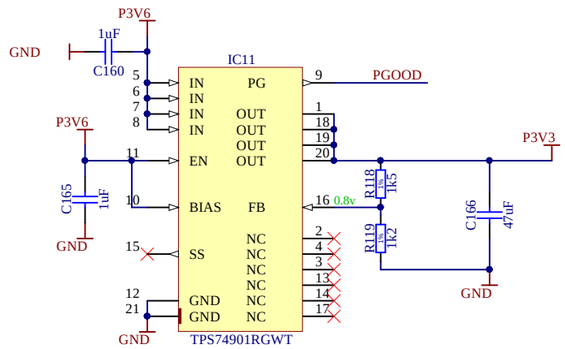


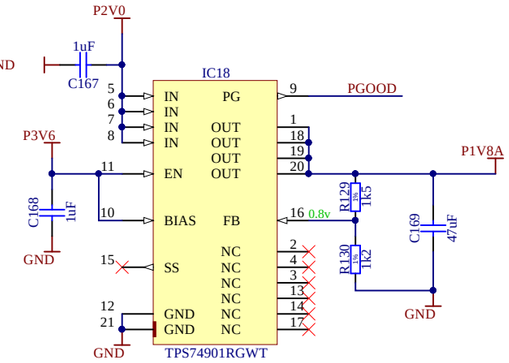
Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	10.10.2017
		File LVDS_IFC_DDS.SchDoc	
		Print Date 17.10.2017 12:22:50	Sheet 2 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	*ISE*	ARTIQ	Size A3 / Rev -



ADR: 1001 000

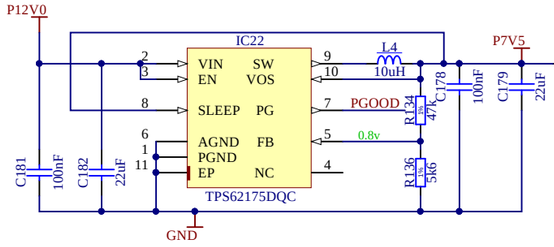


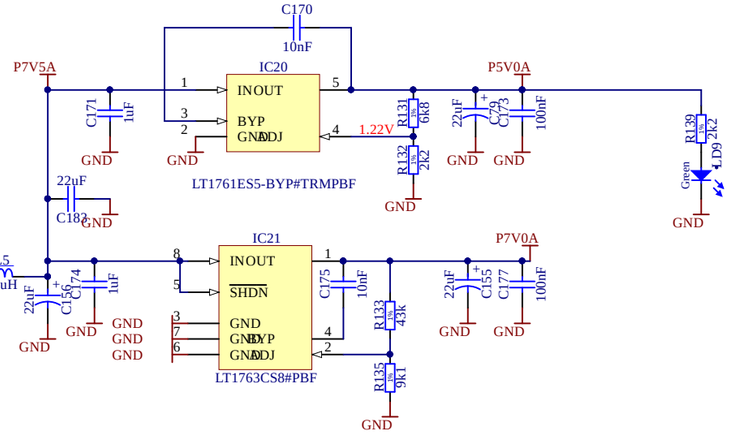


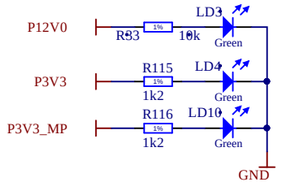


Power budget (max ratings):

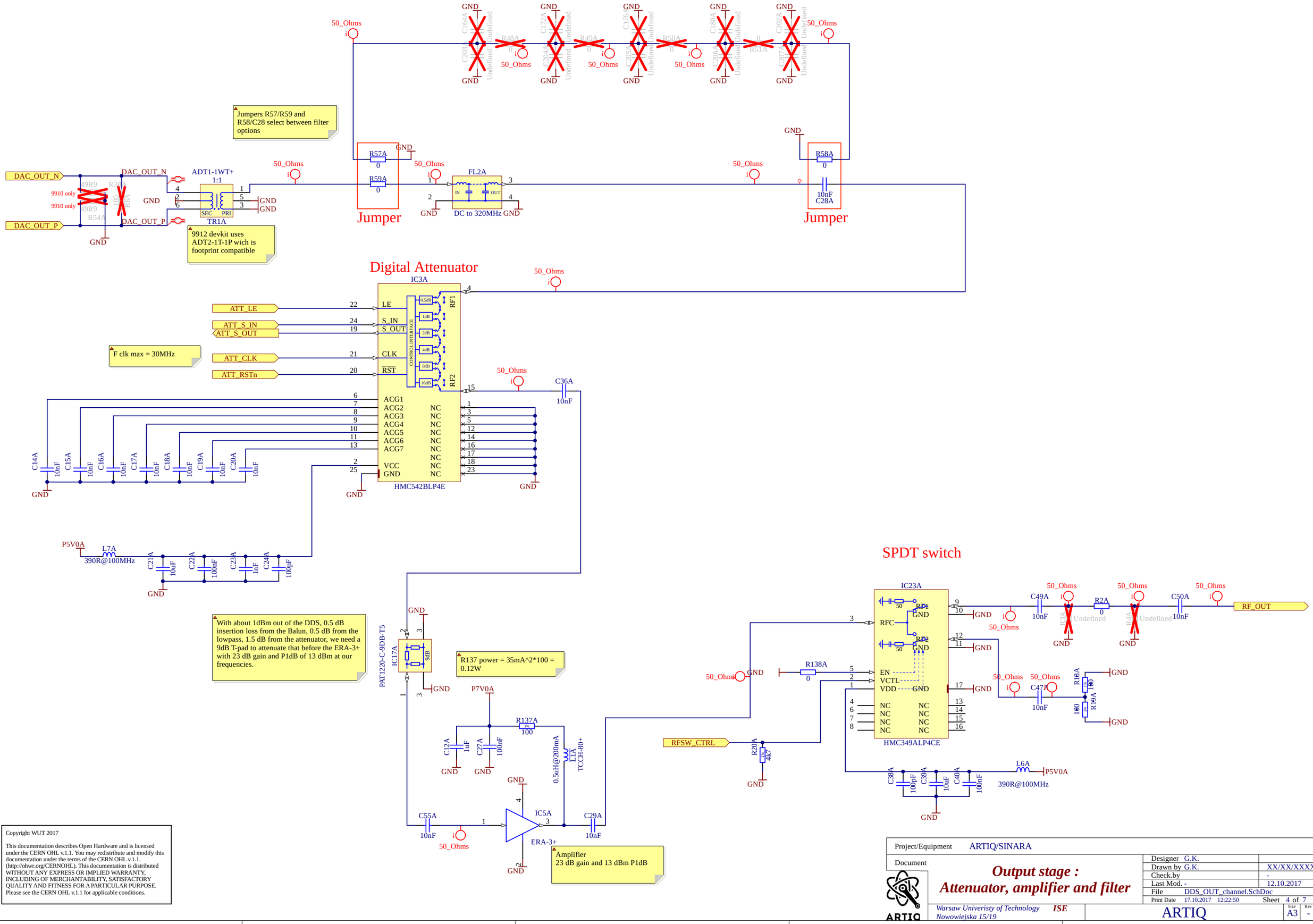
	AD9912 variant(mA)	AD9910 variant(mA)
P3V3:		
LVDS interface 4x	660	660
LVDS load 4x24mA	96	96
CPLD	100	100
Si53312-B-GM	240	240
Si453304	-	100
DDS AVDD3	4*(9,6+31)=133,6	4*29=116
DDS DVDDIO	4*3=12	4*11=44
TOTAL P3V3	1121	1246
TOTAL POWER	3.7	3.9
P1V8:		
DDS AVDD	4*(48+136)=736	4*110=440
DDS DVDD	4*246=984	4*222=888
TOTAL P1V8	1720	1328
TOTAL POWER	3,096	2.39
P5V0		
HMC542BLP4E	4*2.9=11.6	4*2.9=11.6
HMC349LP4C	4*3.5=14	4*3.5=14
TOTAL 5V0	25.6	25.6
TOTAL POWER	0,125	0,125
P7V0		
ERA-3XSM+	4*35=150	4*35=150
TOTAL POWER	1.05	1.05
DC/DC converter losses		
TPS62175 eff .95	0,05*(.27+0,026)*7,5=0.11	0,05*(.27+0,026)*7,5=0.11
LTM:3.6V eff .9	0.1*1,321*3,6=0,47	0,1*1,346*3,6=0,48
LTM:2V eff .87	0.13*1,721*2=0,44	0.13*1.328*2=0.34
LDO losses		
2V->1.8V	0.34	0,26
3.6V->3.3V	0.396	0.4
7.5V->7V	0,135	0,135
7.5V->5V	0,064	0,064
Total power from 12V	9.95W	9.05
Total current from 12V	0.83A	0.75A



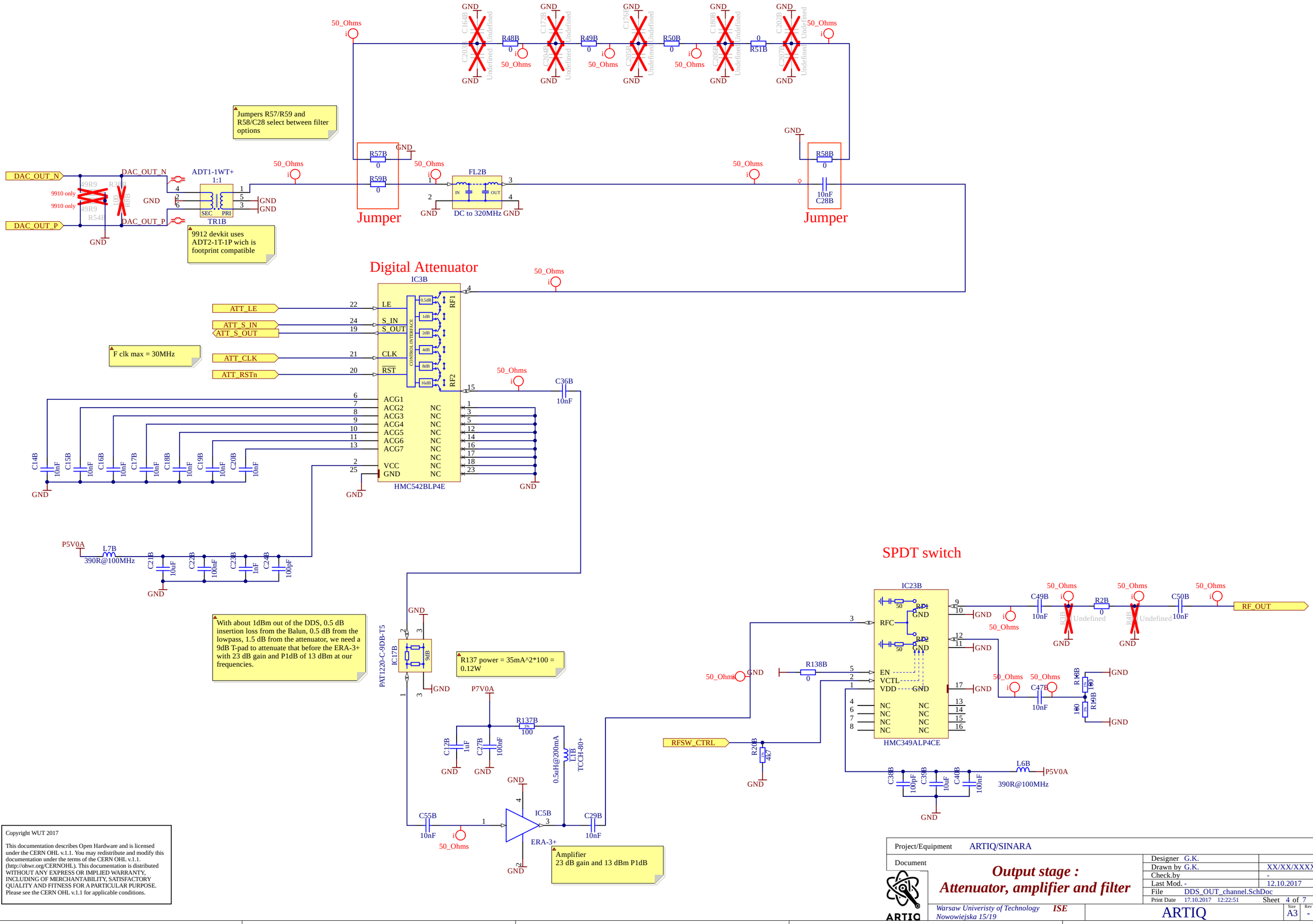


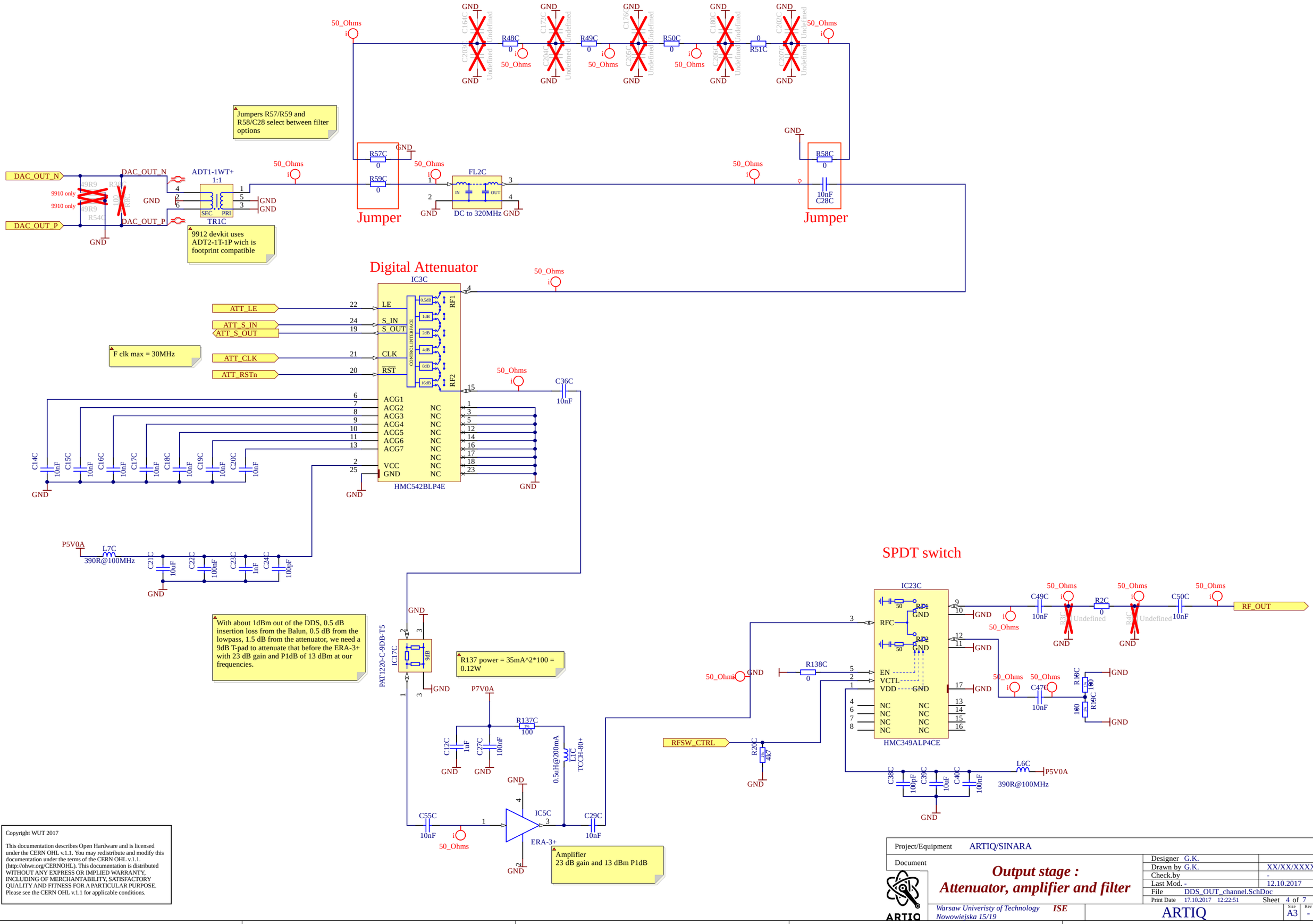


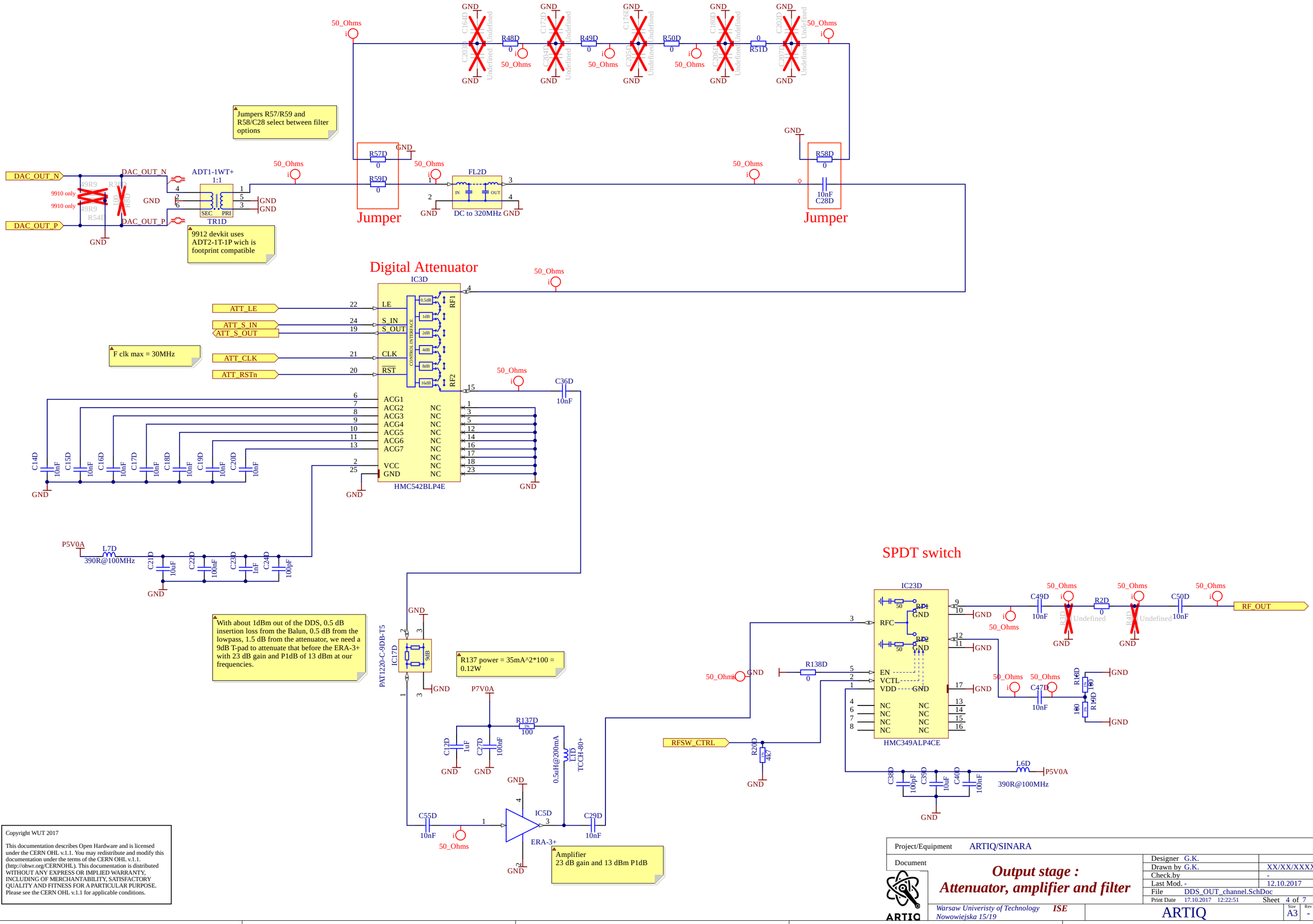
Project/Equipment	ARTIQ/SINARA		
Document	**Power supply DC/DC & LDOs**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	10.10.2017
		File Supply_DDS.SchDoc	
		Print Date 17.10.2017 12:22:50	Sheet 3 of 7
Warsaw Univeristy of Technology ISE *Nowowiejska 15/19*	ARTIQ	Size A3	Rev -



Project/Equipment	ARTIQ/SINARA
Document	**Output stage : Attenuator, amplifier and filter**
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 12.10.2017
File	DDS_OUT_channel.SchDoc
Print Date	17.10.2017 12:22:50 Sheet 4 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19 ISE	ARTIQ Size A3 Rev -


50_Ohms
GND
R48B
R49B
R50B
R51B
C164B
C172B
C176B
C180B
C202B
C203B
C204B
C205B
C206B
C207B
Undefined
Jumpers R57/R59 and R58/C28 select between filter options
R57B
R59B
R58B
Jumper
Jumper
FL2B
DC to 320MHz
DAC_OUT_N
DAC_OUT_P
ADT1-1WT+
1:1
TR1B
SEC
PRI
9910 only
49R9
R54B
R53B
100
R58B
9912 devkit uses ADT2-1T-1P wich is footprint compatible
Digital Attenuator
IC3B
HMC542BLP4E
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
F clk max = 30MHz
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB
1dB
2dB
4dB
8dB
16dB
RF1
RF2
ACG1
ACG2
ACG3
ACG4
ACG5
ACG6
ACG7
NC
VCC
GND
C14B
C15B
C16B
C17B
C18B
C19B
C20B
C36B
10nF
P5V0A
L7B
390R@100MHz
C21B
C22B
C23B
C24B
10uF
100nF
1nF
100pF
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.
IC17B
PAT1220-C-9DB-T5
9dB
R137 power = 35mA^2*100 = 0.12W
P7V0A
R137B
C12B
C27B
1uF
0.5uH@200mA
L1B
TCCH-80+
IC5B
ERA-3+
C55B
C29B
Amplifier
23 dB gain and 13 dBm P1dB
SPDT switch
IC23B
HMC349ALP4CE
RFC
EN
VCTL
VDD
RFSW_CTRL
R20B
4k7
R138B
C49B
C50B
R2B
R3B
R4B
C47B
R46B
R45B
RF_OUT
L6B
C38B
C39B
C40B
Copyright WUT 2017
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter
Designer G.K.
Drawn by G.K.
XX/XX/XXXX
Check.by -
Last Mod. -
12.10.2017
File DDS_OUT_channel.SchDoc
Print Date 17.10.2017 12:22:51
Sheet 4 of 7
Warsaw Univeristy of Technology
Nowowiejska 15/19
ISE
ARTIQ
Size A3
Rev -


50_Ohms
GND
R48C
R49C
R50C
R51C
C203C
C204C
C205C
C206C
C207C
Jumpers R57/R59 and R58/C28 select between filter options
R57C
R59C
Jumper
FL2C
DC to 320MHz
R58C
10nF C28C
Jumper
DAC_OUT_N
DAC_OUT_P
9910 only
49R9
R54C
R8C
ADT1-1WT+ 1:1
TR1C
SEC PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible
Digital Attenuator
IC3C
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
F clk max = 30MHz
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB
1dB
2dB
4dB
8dB
16dB
RF1
RF2
ACG1
ACG2
ACG3
ACG4
ACG5
ACG6
ACG7
NC
VCC
GND
HMC542BLP4E
C14C
C15C
C16C
C17C
C18C
C19C
C20C
10nF
C36C
P5V0A
L7C
390R@100MHz
C21C
C22C
C23C
C24C
10uF
100nF
1nF
100pF
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.
PAT1220-C-9DB-T5
IC17C
9dB
R137 power = 35mA^2*100 = 0.12W
P7V0A
R137C
100
C12C
1uF
C27C
100nF
0.5uH@200mA
L1C
TCCH-80+
C55C
IC5C
C29C
ERA-3+
Amplifier
23 dB gain and 13 dBm P1dB
SPDT switch
IC23C
RFC
RF1
RF2
EN
VCTL
VDD
HMC349ALP4CE
R138C
RFSW_CTRL
R20C
4k7
C49C
R2C
C50C
RF_OUT
C47C
R46C
R45C
C38C
C39C
C40C
L6C
390R@100MHz
Copyright WUT 2017
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter
Designer G.K.
Drawn by G.K. XX/XX/XXXX
Check.by -
Last Mod. - 12.10.2017
File DDS_OUT_channel.SchDoc
Print Date 17.10.2017 12:22:51 Sheet 4 of 7
Warsaw Univeristy of Technology ISE
Nowowiejska 15/19
ARTIQ
Size A3
Rev -



Project/Equipment: ARTIQ/SINARA

Document: **Output stage : Attenuator, amplifier and filter**

Designer	G.K.
Drawn by	G.K.
Check.by	-
Last Mod.	-
File	DDS_OUT_channel.SchDoc
Print Date	17.10.2017 12:22:51
Sheet	4 of 7
Size	A3
Rev	-

XX/XX/XXXX

12.10.2017

Warsaw Univeristy of Technology
Nowowiejska 15/19
ISE
ARTIQ

separate RSET and loop filter components due to layout constraints

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Loop filter calculation:
Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

R=859R
Cs=522p
Cp=27p

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

separate RSET and loop filter components due to layout constraints

Loop filter calculation:
Reference input frequency : 31.25MHz
PFD : 31.25MHz
multiplication factor:32
system clock frequency : 1GHz
desired phase margin: 45deg
Open loop BW: 3MHz

R=859R
Cs=522p
Cp=27p

Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.10.2017
File	DDS_channel.SchDoc
Print Date	17.10.2017 12:22:52 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

separate RSET and loop filter components due to layout constraints

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Loop filter calculation:
Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

R=859R
Cs=522p
Cp=27p

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

separate RSET and loop filter components due to layout constraints

Loop filter calculation:
Reference input frequency : 31.25MHz
PFD : 31.25MHz
multiplication factor:32
system clock frequency : 1GHz
desired phase margin: 45deg
Open loop BW: 3MHz

R=859R
Cs=522p
Cp=27p

Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.10.2017
File	DDS_channel.SchDoc
Print Date	17.10.2017 12:22:52 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

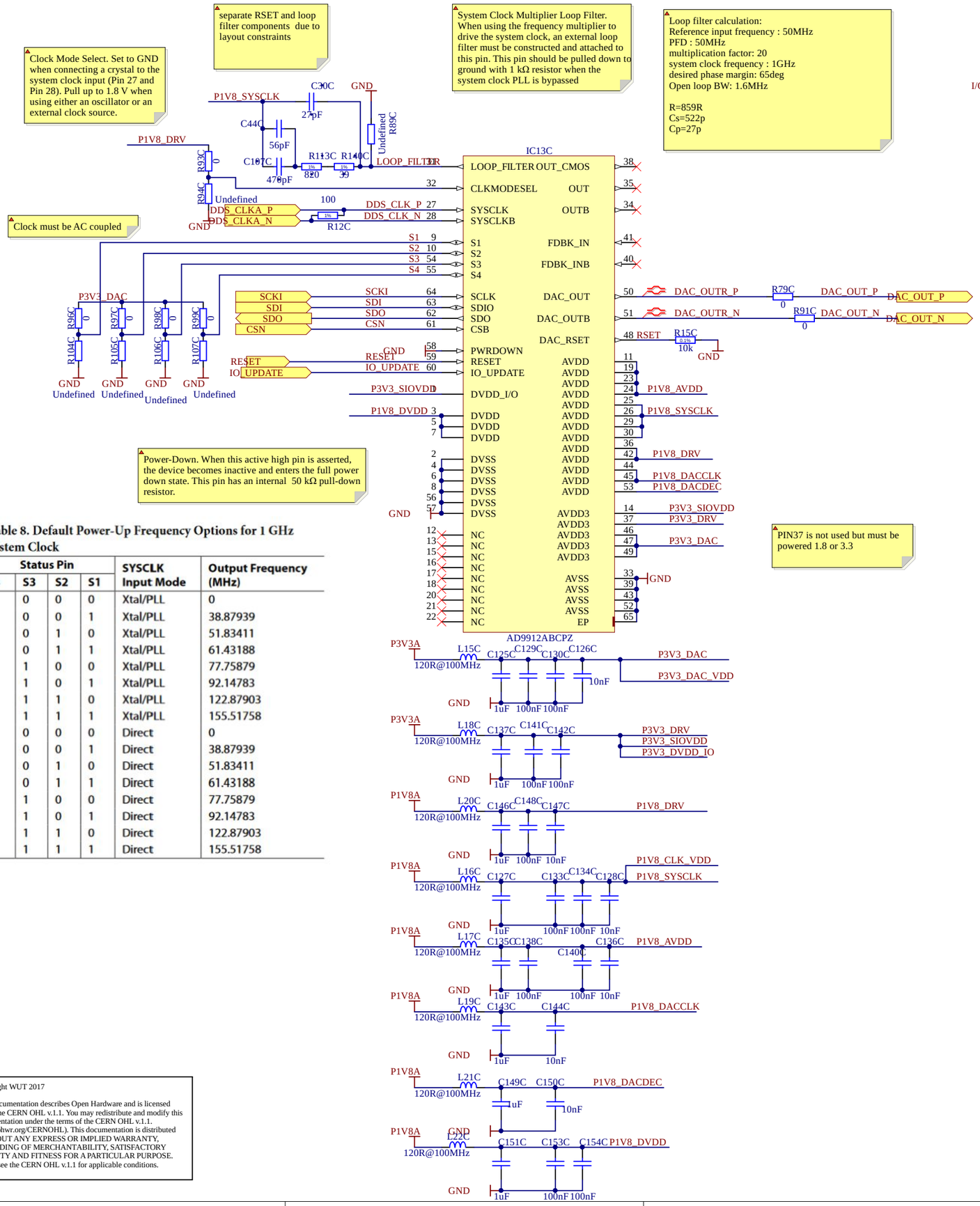


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.10.2017
File	DDS_channel.SchDoc
Print Date	17.10.2017 12:22:53 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

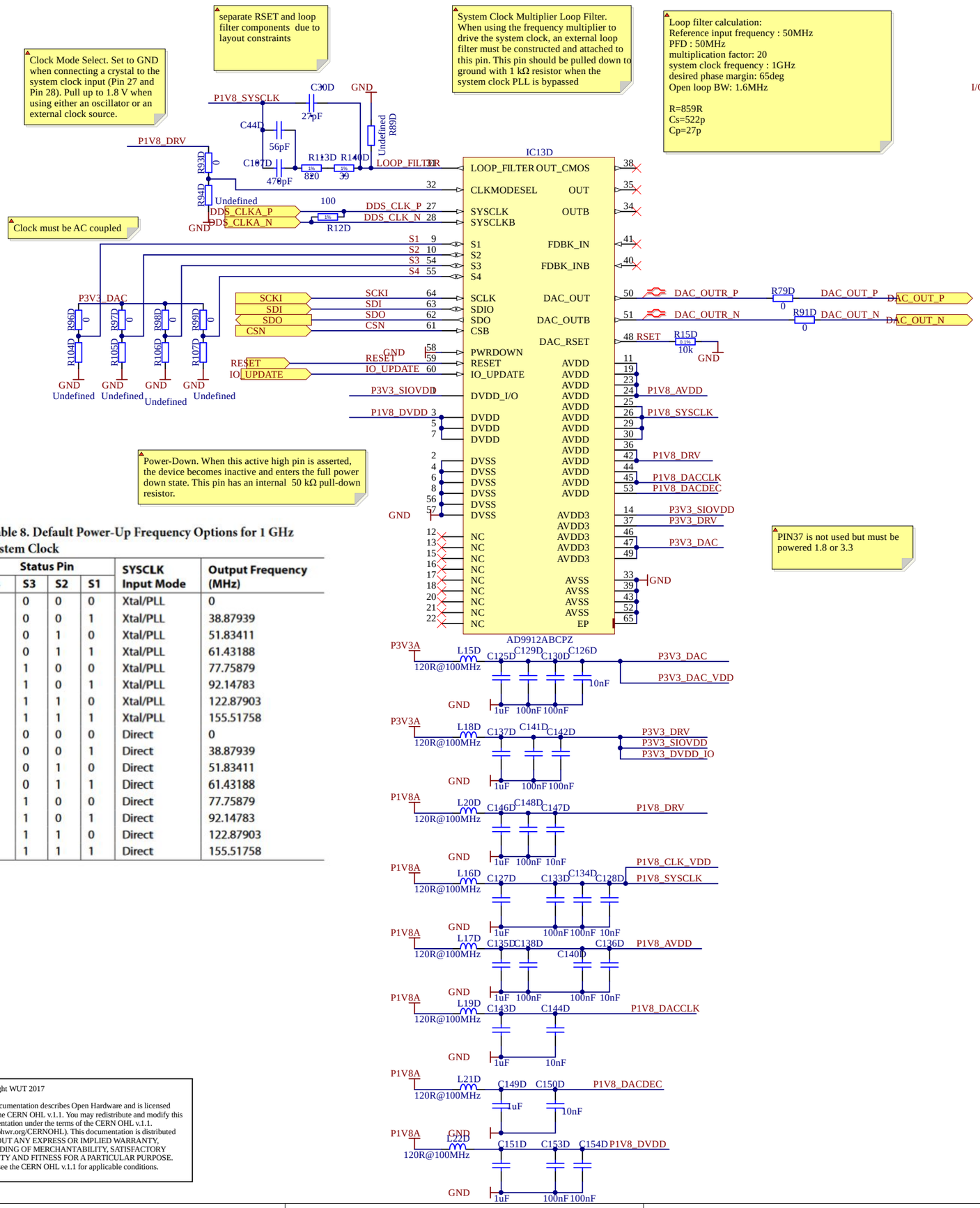
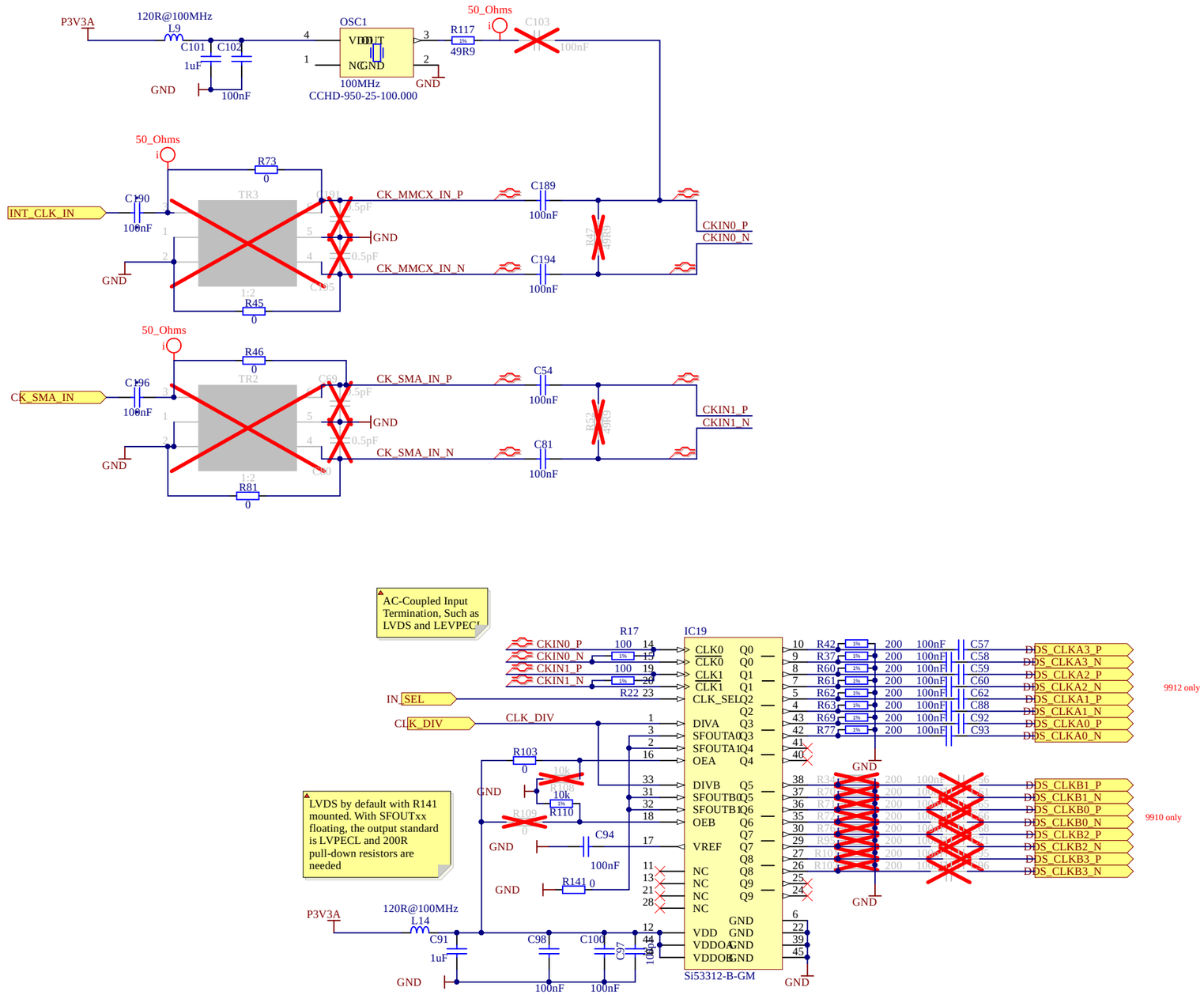


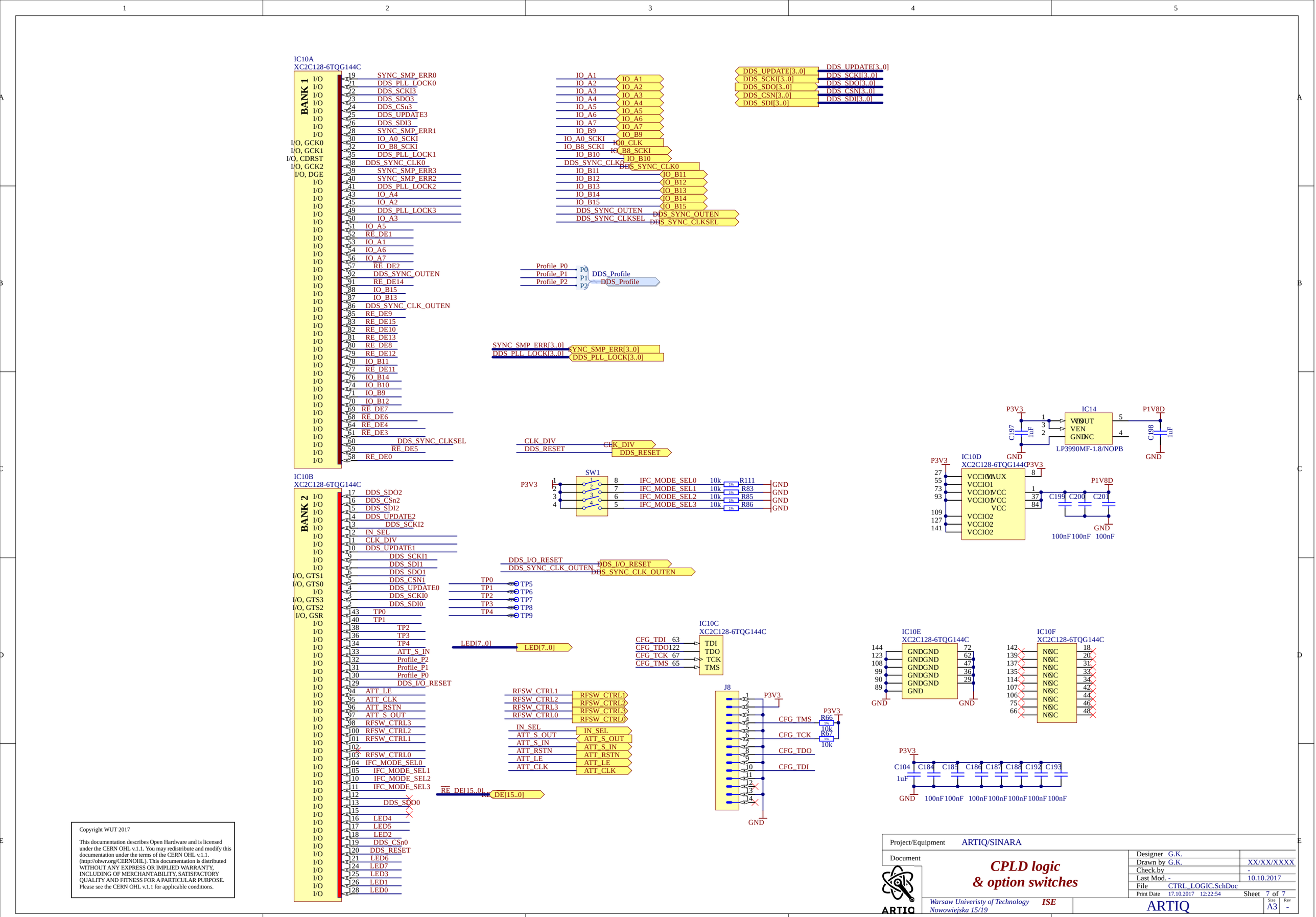
Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

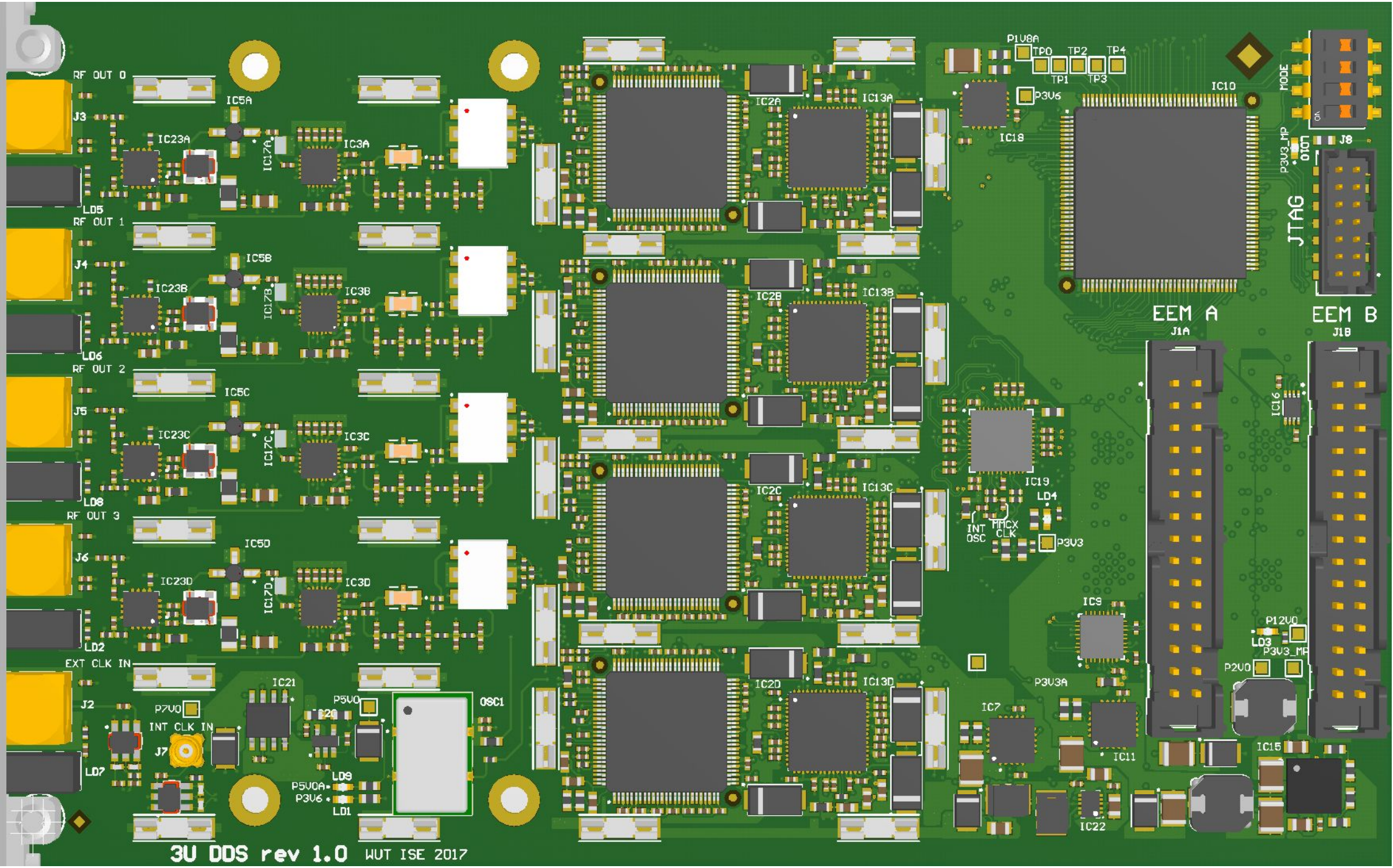
Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

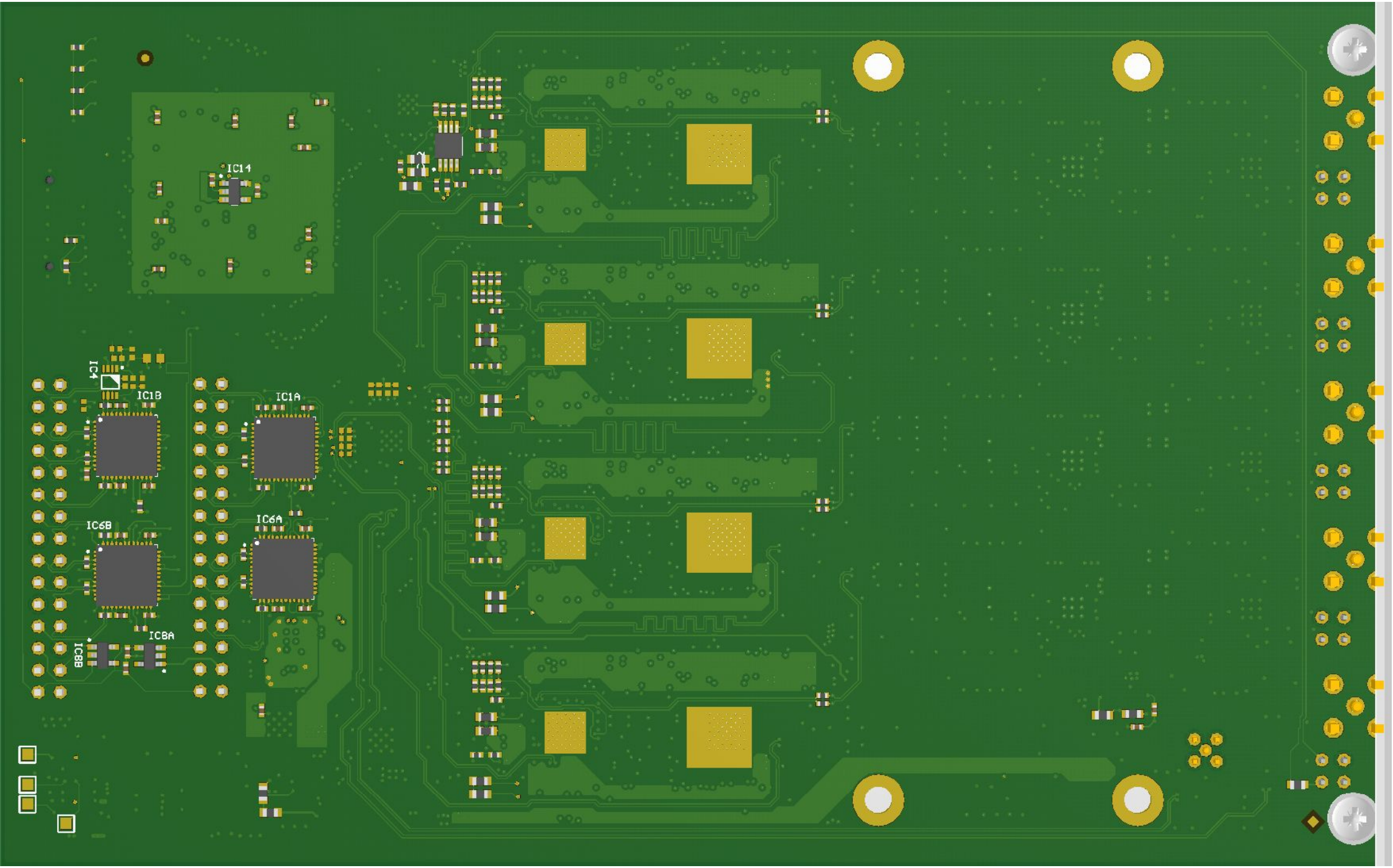
Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.10.2017
File	DDS_channel.SchDoc
Print Date	17.10.2017 12:22:53 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -



Project/Equipment	ARTIQ/SINARA		
Document	**Clock distribution and generation**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	12.10.2017
		File CLK_INPUT.SchDoc	
		Print Date 17.10.2017 12:22:54	Sheet 6 of 7
Warsaw Univeristy of Technology ISE *Nowowiejska 15/19*	ARTIQ	Size A3	Rev -

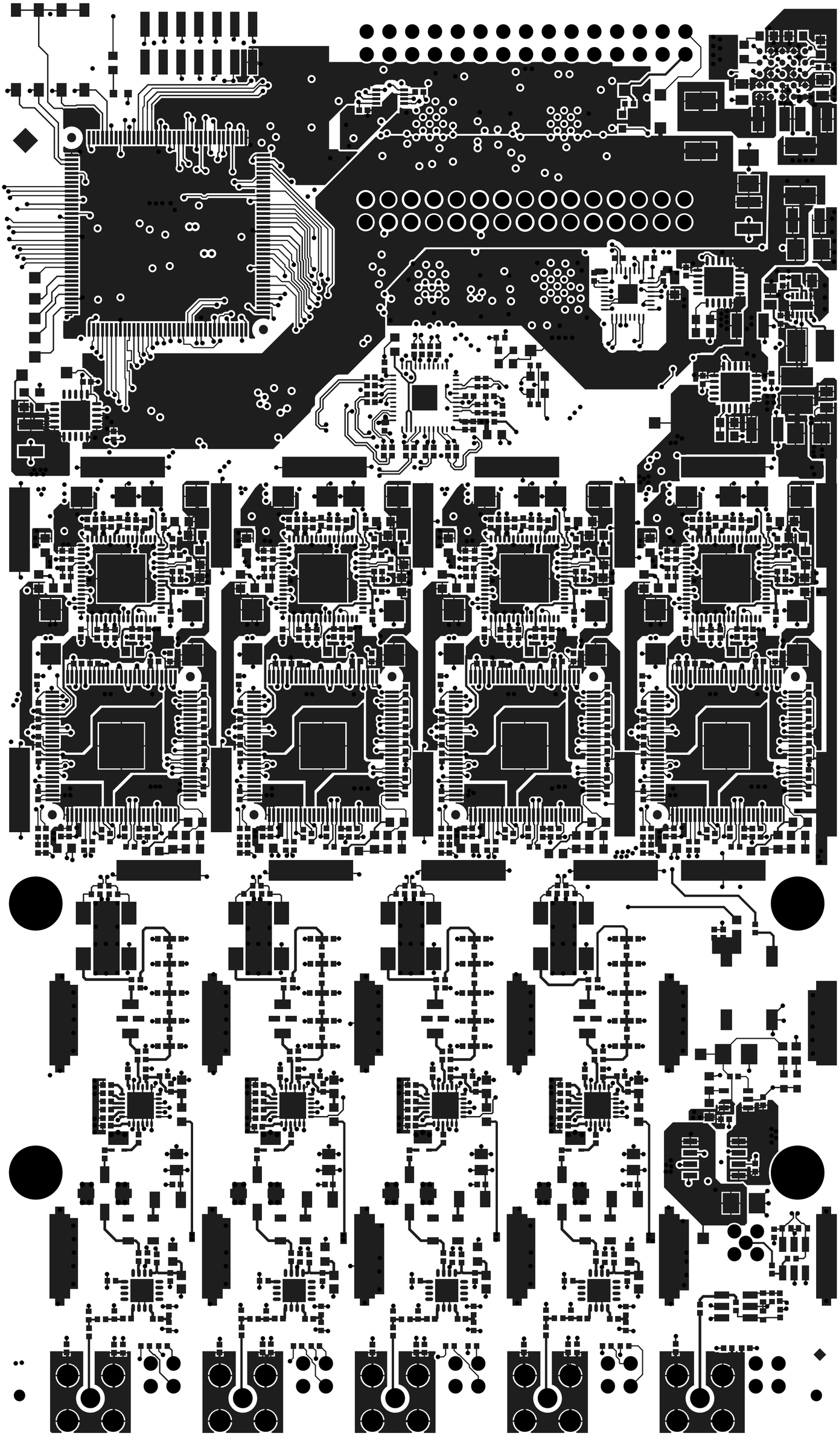

IC10A
XC2C128-6TQG144C
BANK 1
IC10B
XC2C128-6TQG144C
BANK 2
IC10C
XC2C128-6TQG144C
IC10D
XC2C128-6TQG144C
IC10E
XC2C128-6TQG144C
IC10F
XC2C128-6TQG144C
IC14
LP3990MF-1.8/NOPB
SW1
J8
DDS_UPDATE[3..0]
DDS_SCKI[3..0]
DDS_SDO[3..0]
DDS_CSN[3..0]
DDS_SDI[3..0]
SYNC_SMP_ERR[3..0]
DDS_PLL_LOCK[3..0]
DDS_Profile
LED[7..0]
RE_DE[15..0]
P3V3
P1V8D
GND
Copyright WUT 2017
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
Project/Equipment ARTIQ/SINARA
Document
CPLD logic & option switches
Designer G.K.
Drawn by G.K. XX/XX/XXXX
Check.by -
Last Mod. - 10.10.2017
File CTRL_LOGIC.SchDoc
Print Date 17.10.2017 12:22:54 Sheet 7 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19
ISE
ARTIQ
Size A3
Rev -

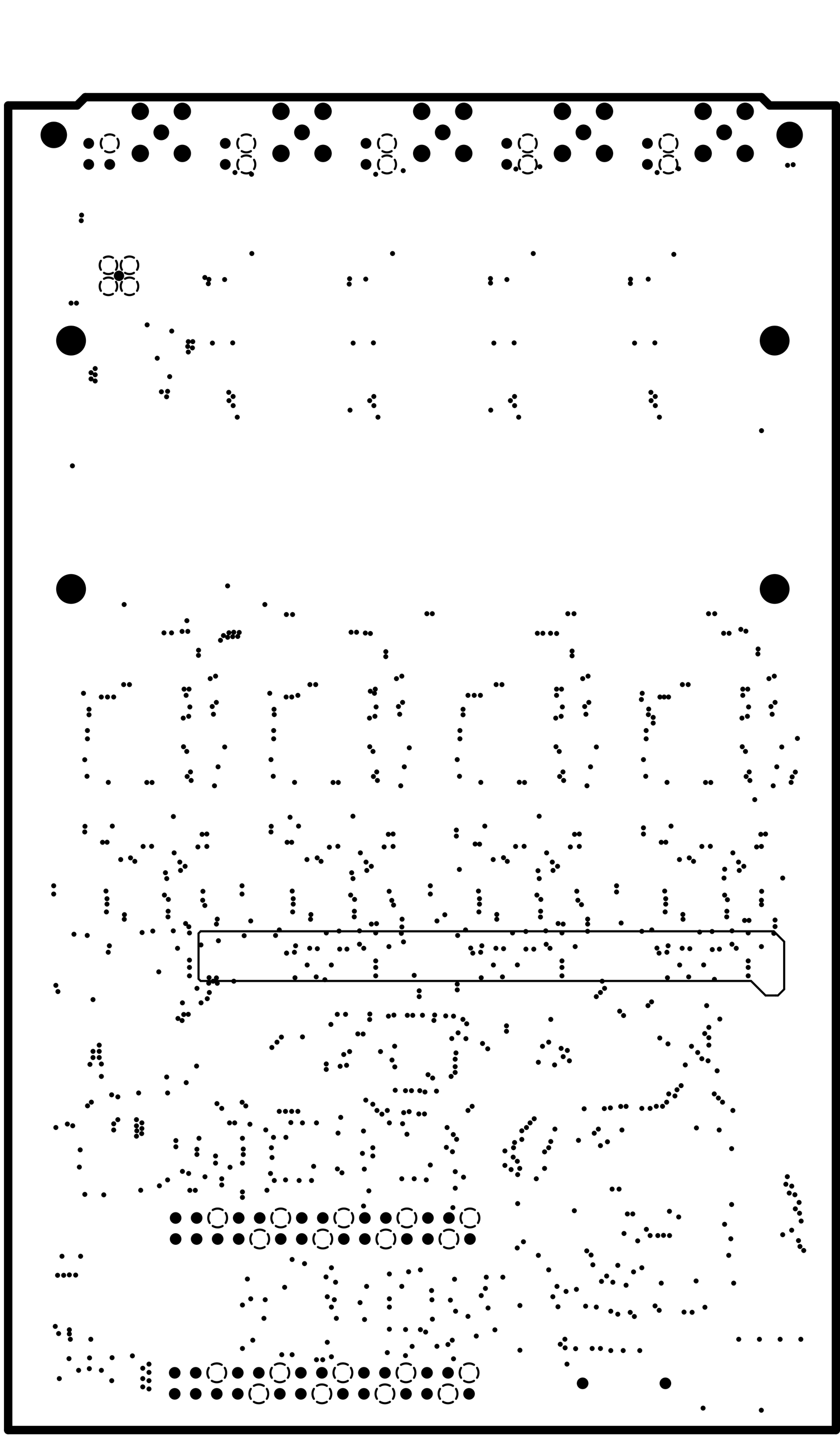

RF OUT 0
RF OUT 1
RF OUT 2
RF OUT 3
EXT CLK IN
INT CLK IN
EEM A
EEM B
JTAG
MODE
3U DDS rev 1.0
WUT ISE 2017

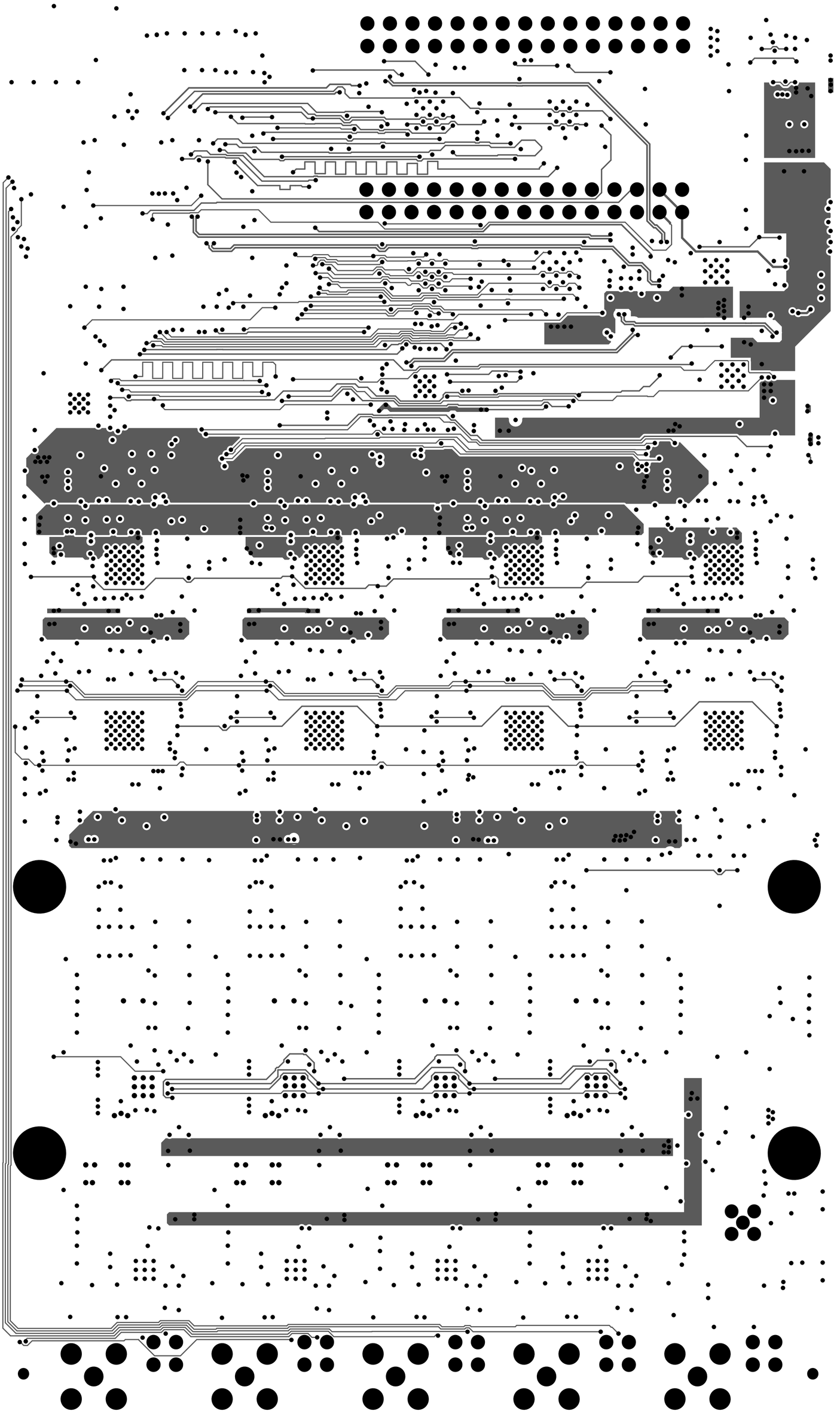

IC14
IC4
IC1B
IC1A
IC6B
IC6A
IC8A
IC8B

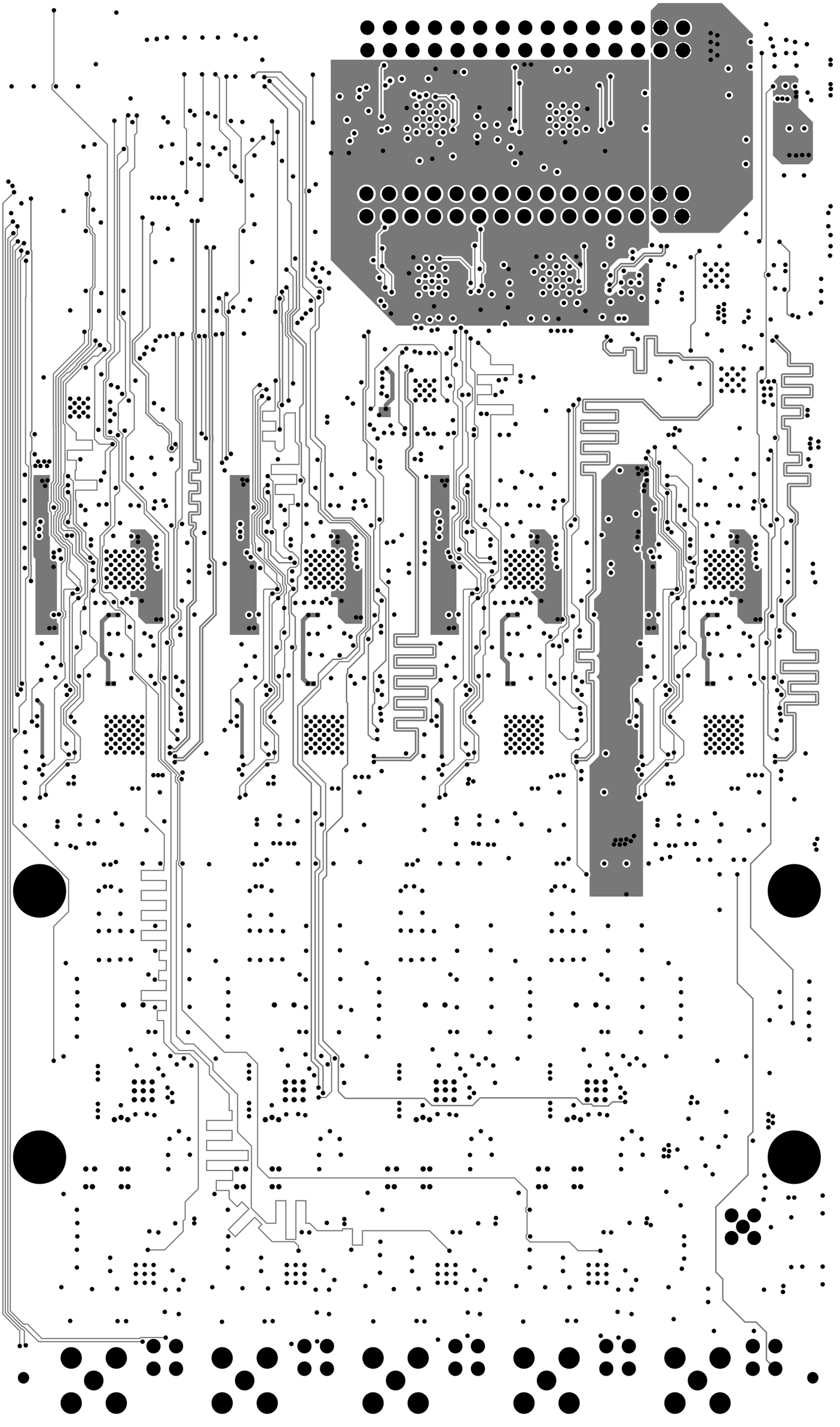
RF OUT 0
J3
LD5
RF OUT 1
J4
LD6
RF OUT 2
J5
LD8
RF OUT 3
J6
LD2
EXT CLK IN
J2
LD7
P7V0
INT CLK IN
J7
IC21
P5V0
IC20
OSC1
LD9
P5V0A
P3V6
LD1
IC5A
IC5B
IC5C
IC5D
IC23A
IC23B
IC23C
IC23D
IC17A
IC17B
IC17C
IC17D
IC3A
IC3B
IC3C
IC3D
IC2A
IC2B
IC2C
IC2D
IC13A
IC13B
IC13C
IC13D
P1V8A
TP0
TP1
TP2
TP3
TP4
P3V6
IC18
IC10
MODE
ON
1 2 3 4
J8
P3V3_MP
JTAG
EEM A
J1A
EEM B
J1B
IC16
IC19
LD4
INT OSC
MMCX CLK
P3V3
IC9
P12V0
LD3
P3V3_MP
P2V0
P3V3A
IC7
IC11
IC15
IC22
30
30

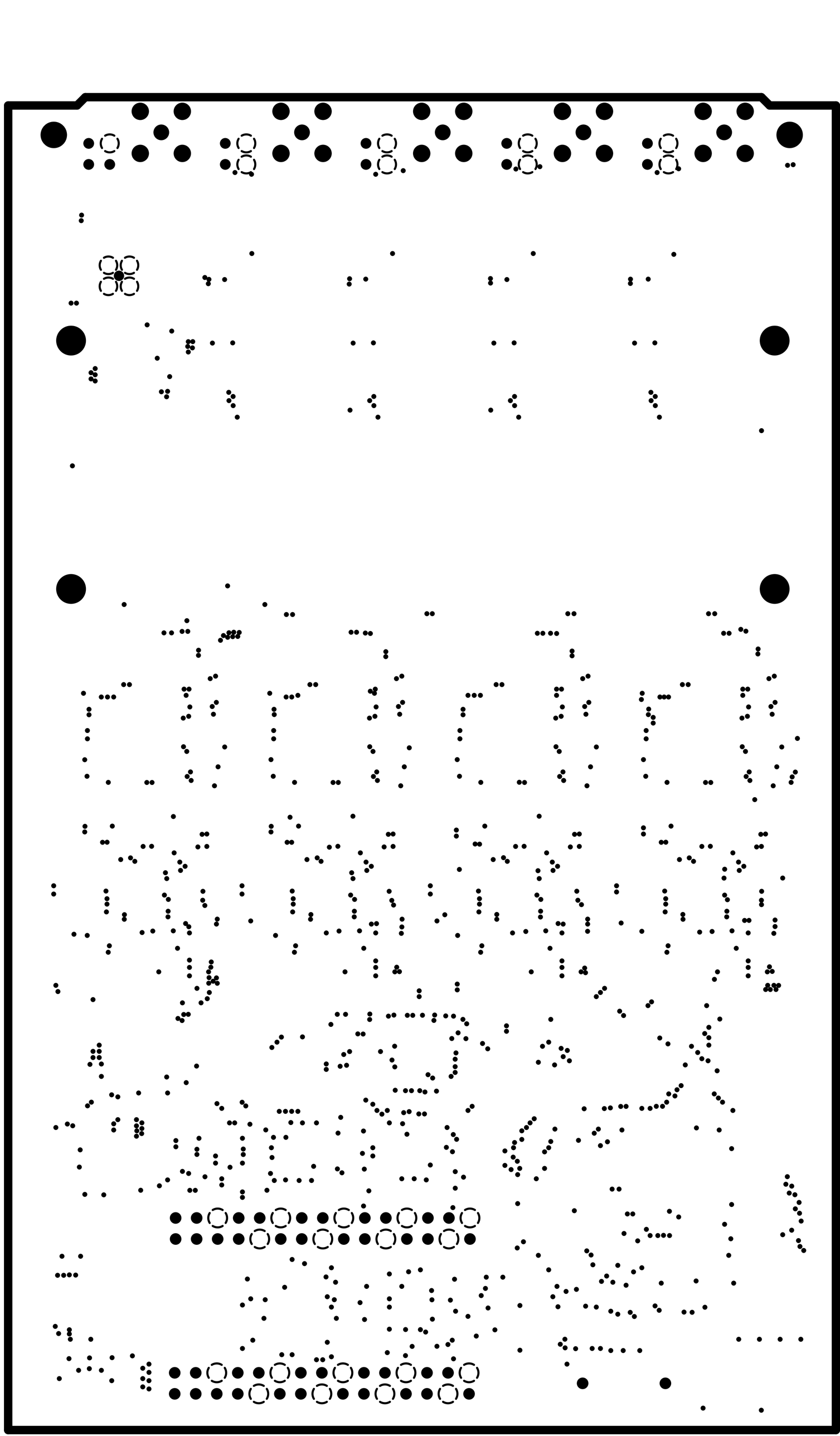
3U DDS rev 1.0 WUT ISE 2017

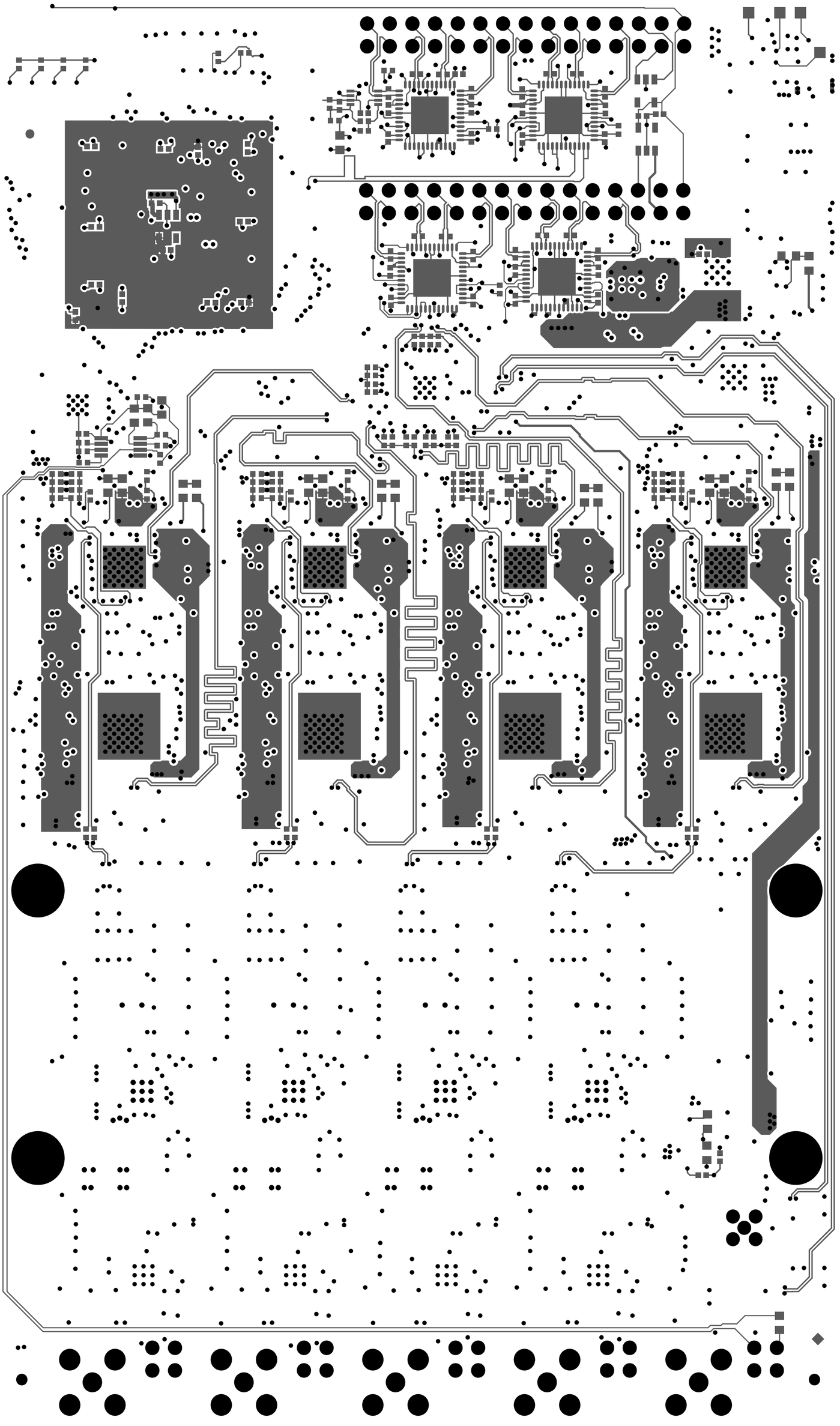












IC15

IC14

IC4

IC1A

IC1B

IC6A

IC6B

IC8A

IC8B