shield clips

CLIP1 CLIP2 CLIP3 CLIP4 CLIP5
CLIP6 CLIP7 CLIP8 CLIP9 CLIP10 CLIP27
CLIP11 CLIP12 CLIP13 CLIP14 CLIP15 CLIP28
CLIP16 CLIP17 CLIP18 CLIP19 CLIP20 CLIP29
CLIP21 CLIP22 CLIP23 CLIP24 CLIP25 CLIP26
(all GND)

Ext clock input

Clock from Kasli

Output SMAs

U_CTRL_LOGIC
CTRL_LOGIC.SchDoc

RFSW_CTRL0..3, DDS_SDO[3..0], DDS_SDI[3..0], DDS_SCKI[3..0], DDS_CSn[3..0], IN_SEL, CLK_DIV, DDS_UPDATE[3..0], DDS_SYNC_CLK0, DDS_PLL_LOCK[3..0], SYNC_SMP_ERR[3..0], DDS_Profile, DDS_I/O_RESET, DDS_RESET, LED[7..0], ATT_CLK, ATT_LE, ATT_RSTn, ATT_S_IN, ATT_S_OUT

RE_DE[15..0] → RE_DE[15..01]

IO_A1 IO_A2 IO_A3 IO_A4 IO_A5 IO_A6 IO_A7
IO_B8_SCKI IO_B9 IO_B10 IO_B11 IO_B12 IO_B13 IO_B14 IO_B15

DDS_SYNC_CLKSEL, DDS_SYNC_OUTEN, DDS_SYNC_CLK_OUTEN

LVDS_IFC_DDS.SchDoc U_LVDS_IFC — EEM A

IO0..IO7, LVDS0_P/N, LVDS1_P/N, LVDS7_P/N, I2C_SDA, I2C_SCL
RE_DE0 RE_DE1 RE_DE2 RE_DE3 RE_DE4 RE_DE5 RE_DE6 RE_DE7

LVDS_IFC_DDS.SchDoc U_LVDS_IFC — EEM B

RE_DE8 RE_DE9 RE_DE10 RE_DE11 RE_DE12 RE_DE13 RE_DE14 RE_DE15

U_CLK_INPUT
CLK_INPUT.SchDoc

CK_SMA_IN, IN_SEL, CLK_DIV, INT_CLK_IN
DDS_CLKA0_P/N, DDS_CLKA1_P/N, DDS_CLKA2_P/N, DDS_CLKA3_P/N, DDS_CLKB0_P/N, DDS_CLKB1_P/N, DDS_CLKB2_P/N, DDS_CLKB3_P/N

C37 10nF, C42 10nF, R6 0, J2 SMA 50_Ohms, J7 MMCX

PLACE IT CLOSE TO LVDS Rx/Tx

DDS_SYNC_CLK0 → R31 1k → R32 100 → IC4 FIN1101K8X (EN, GND, VCC)
P3V3_CLK2 → R36 1k, R39 1k, C1 100nF, C13 100nF
IC9

DDS0_SYNC_OUT_P/N → R68 100 → IC16 Si53304-B-GM
CLK0 CLK0 CLK1 CLK1 CLK_SEL SFOUTA0 SFOUTA1 OE0 OE1 OE2 SFOUTB0 SFOUTB1 OE3 OE4 OE5 VREF VDD VDDOA VDDOB
Q0 Q0 Q1 Q1 Q2 Q2 Q3 Q3 Q4 Q4 Q5 Q5
DDS0_SYNC_IN_P/N, DDS1_SYNC_IN_P/N, DDS2_SYNC_IN_P/N, DDS3_SYNC_IN_P/N

120R@100MHz L13, C86 1uF, C89 100nF, C90 100nF
120R@100MHz L8, C45 1uF, C46 100nF
R114 100, FB_SYNC_P, FB_SYNC_N

LED0..LED7 — R25..R44 470 — LD2A BOT, LD2B TOP, LD5A BOT, LD5B TOP, LD6A BOT, LD6B TOP, LD8A BOT, LD8B TOP — Green

U_DDS_OUT_channel0..3
DDS_OUT_channel.SchDoc

DAC_OUT_P/N, RF_OUT, ATT_CLK, RFSW_CTRL, ATT_LE, ATT_RSTn, ATT_S_IN, ATT_S_OUT
RF_OUT0..3 — 50_Ohms
RFSW_CTRL0..3

U_DDS_channel0..3
DDS_channel.SchDoc

DAC_OUT_P/N, SYNC_OUT_P/N, SYNC_CLK, I/O_RESET, RESET, SYNC_IN_P/N, SDO, SDI, SCKI, CSN, IO_UPDATE, PLL_LOCK, SYNC_SMP_ERR, DDS_Profile, DDS_CLKA_P/N, DDS_CLKB_P/N
DDS_SDO0..3, DDS_SDI0..3, DDS_SCKI0..3, DDS_CSn0..3, DDS_UPDATE0..3, DDS_PLL_LOCK0..3, SYNC_SMP_ERR0..3, DDS_CLKA0_P/N, DDS_CLKA1_P/N, DDS_CLKA2_P/N, DDS_CLKA3_P/N, DDS_CLKB0_P/N, DDS_CLKB1_P/N, DDS_CLKB2_P/N, DDS_CLKB3_P/N

U_Supply_DDS
Supply_DDS.SchDoc
FTG1 FTG2 FTG3 FTG4

When routing please do a reasonable (100ps) length match within each of DDS_SYNC_CLK[3:0], DDS_UPDATE[3:0], RFSW_CTRL[3:0], IO[15:11] (nominally the RFSW_CTRL lines), DDS[3:0]_SYNC_IN, DDS_RESET and a really good one on DDS_CLK[3:0]_[PN].

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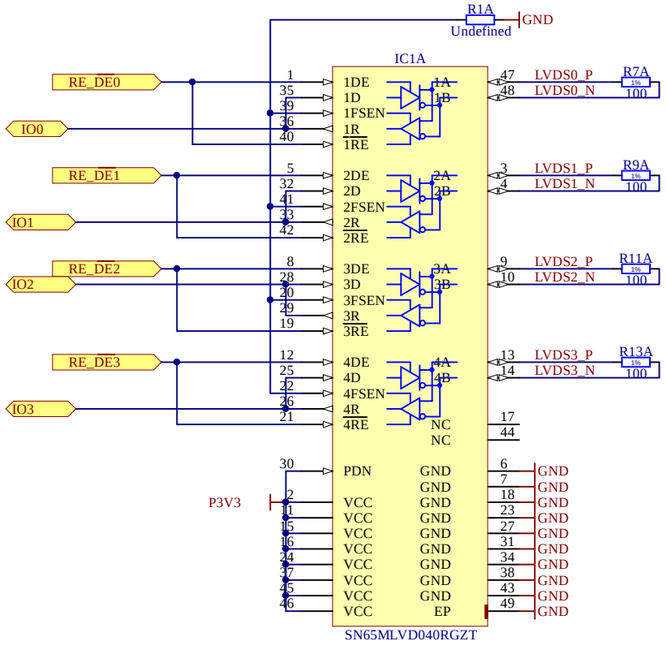
Project/Equipment	ARTIQ/SINARA
Document	3U DDS (URUKUL) Top entity
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 20.09.2017
File	PCB_3U_DDS.schdoc
Print Date	21.09.2017 01:14:45 Sheet 1 of 7

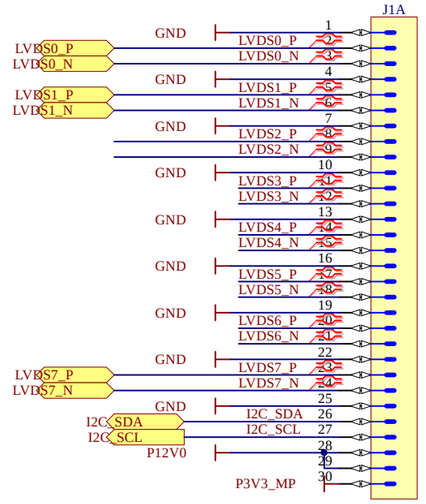
Warsaw Univeristy of Technology
Nowowiejska 15/19
ISE

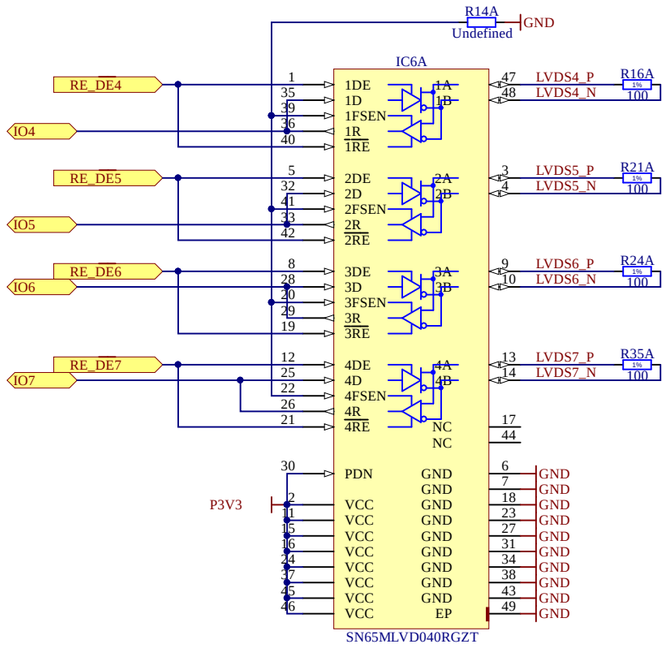
ARTIQ — Size A3 — Rev -

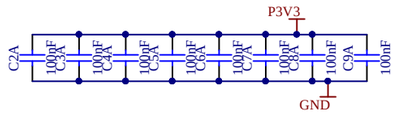
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

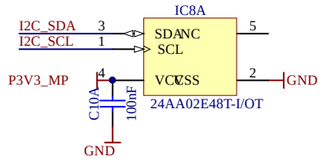


This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A









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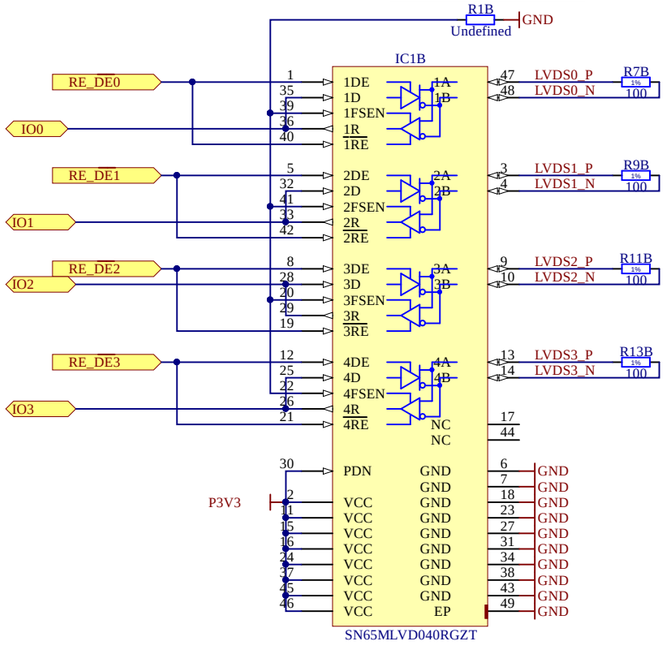
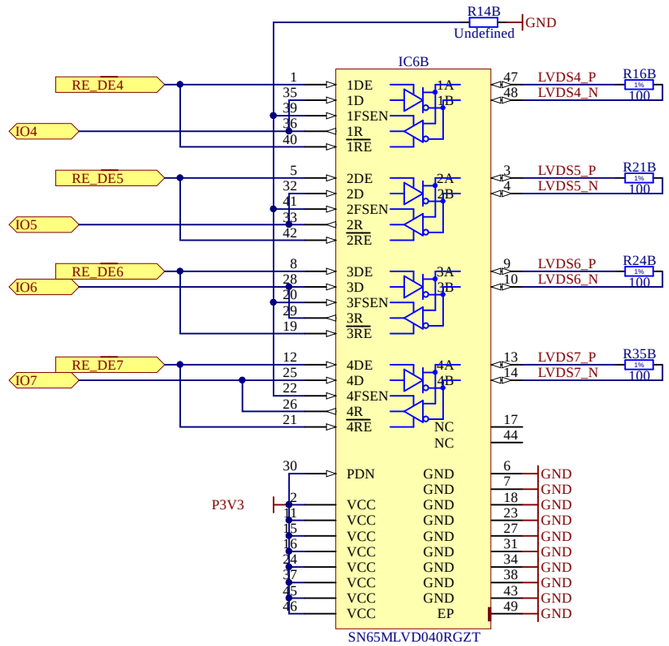
Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File LVDS_IFC_DDS.SchDoc	
		Print Date 21.09.2017 01:14:46	Sheet 2 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	*ISE*	ARTIQ	Size A3 / Rev -

FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output





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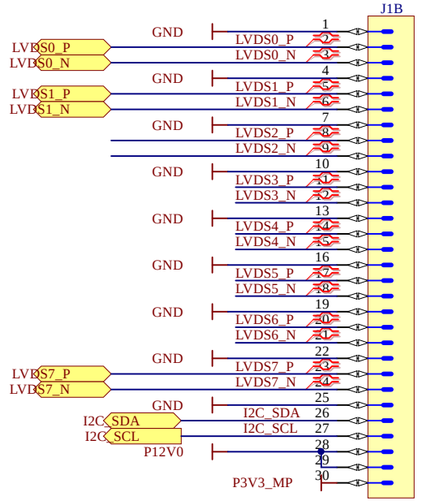
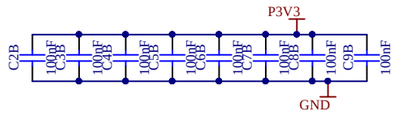
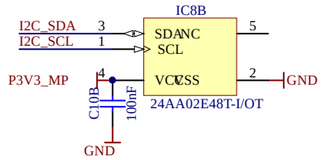
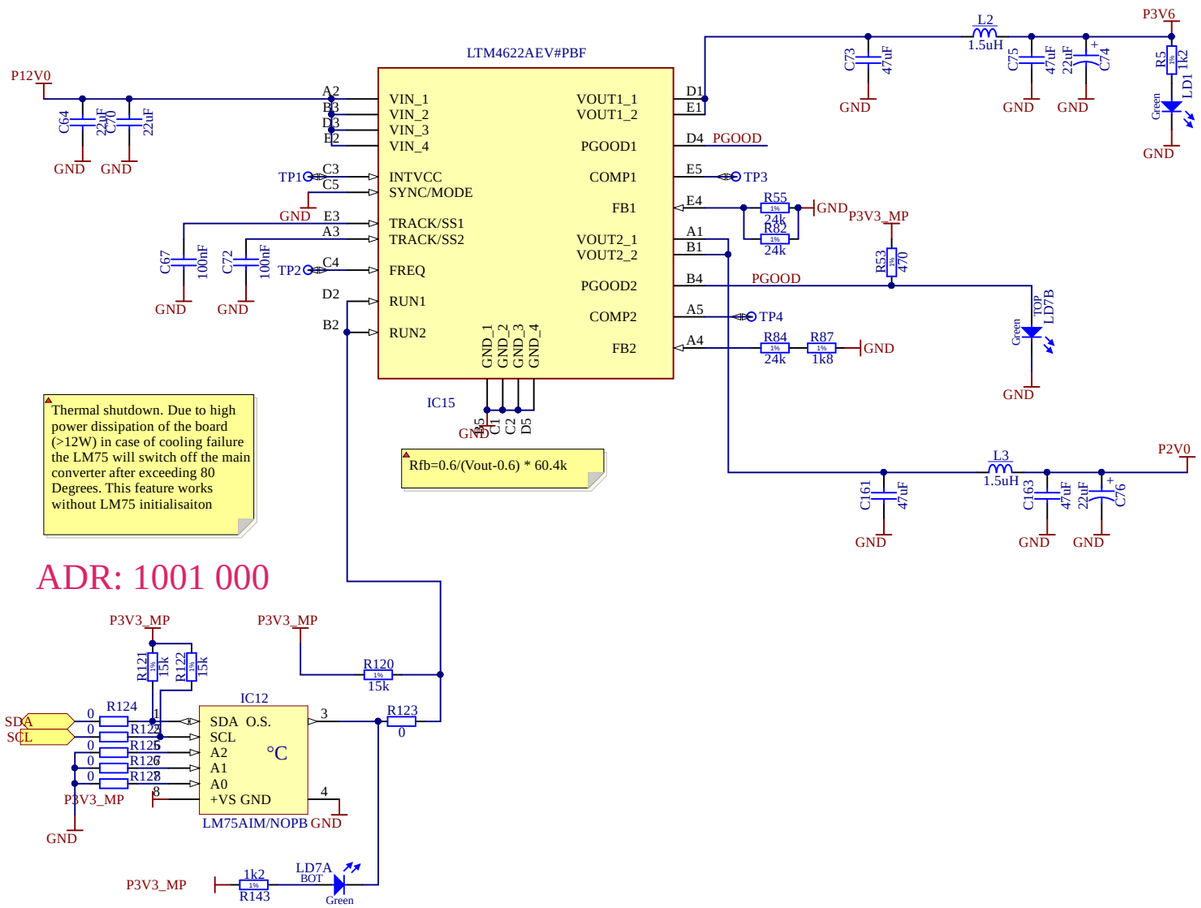
This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A







Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File LVDS_IFC_DDS.SchDoc	
		Print Date 21.09.2017 01:14:46	Sheet 2 of 7
Warsaw Univeristy of Technology *Nowowiejska 15/19* *ISE*	ARTIQ	Size A3	Rev -


LTM4622AEV#PBF
P12V0
VIN_1
VIN_2
VIN_3
VIN_4
INTVCC
SYNC/MODE
TRACK/SS1
TRACK/SS2
FREQ
RUN1
RUN2
VOUT1_1
VOUT1_2
PGOOD1
COMP1
FB1
VOUT2_1
VOUT2_2
PGOOD2
COMP2
FB2
GND_1
GND_2
GND_3
GND_4
IC15
P3V6
P3V3_MP
P2V0
PGOOD
TP1
TP2
TP3
TP4
L2
1.5uH
L3
1.5uH
R5 1K2
LD1
Green
R53 470
LD7B
TOP
R55 24k
R82 24k
R84 24k
R87 1k8
C64 22uF
C70 22uF
C67 100nF
C72 100nF
C73 47uF
C75 47uF
C74 22uF
C161 47uF
C163 47uF
C76 22uF
GND
Thermal shutdown. Due to high power dissipation of the board (>12W) in case of cooling failure the LM75 will switch off the main converter after exceeding 80 Degrees. This feature works without LM75 initialisaiton
Rfb=0.6/(Vout-0.6) * 60.4k
ADR: 1001 000
IC12
LM75AIM/NOPB
SDA O.S.
SCL
A2
A1
A0
+VS GND
°C
R120 15k
R121 15k
R122 15k
R123 0
R124 0
R125 0
R126 0
R127 0
R128 0
SDA
SCL
LD7A
BOT
R143 1k2
IC7
IC11
IC18
TPS74901RGWT
IN
IN
IN
IN
PG
OUT
OUT
OUT
EN
BIAS
FB
SS
NC
GND
GND
PGOOD
P3V3A
P3V3
P1V8A
0.8v
C63 1uF
C77 1uF
C78 47uF
R23 1K5
R80 1K2
C160 1uF
C165 1uF
C166 47uF
R118 1K5
R119 1K2
C167 1uF
C168 1uF
C169 47uF
R129 1K5
R130 1K2
IC20
LT1761ES5-BYP#TRMPBF
INOUT
BYP
GND
ADJ
1.22V
P7V5A
P5V0A
C170 10nF
C171 1uF
C172 22uF
C173 100nF
R131 6K8
R132 2K2
R139 2K2
LD3
C182 22uF
IC22
TPS62175DQC
VIN
EN
SLEEP
AGND
PGND
EP
SW
VOS
PG
FB
NC
L4 10uH
L5 10uH
P7V5
R134 47k
R136 5k6
C178 100nF
C179 22uF
C181 100nF
C182 22uF
IC21
LT1763CS8#PBF
SHDN
C174 1uF
C175 10nF
C155 22uF
C177 100nF
R133 43k
R135 9k1
P7V0A
Power budget (max ratings):
AD9912 variant(mA)
AD9910 variant(mA)
P3V3:
LVDS interface 4x 660 660
LVDS load 4x24mA 96 96
CPLD 100 100
ADCLK948 230 230
DDS AVDD3 4*(9,6+31)=133,6 4*29=116
DDS DVDDIO 4*3=12 4*11=44
TOTAL P3V3 1121 1146
TOTAL POWER 3.7 3.7
P1V8:
DDS AVDD 4*(48+136)=736 4*110=440
DDS DVDD 4*246=984 4*222=888
TOTAL P1V8 1720 1328
TOTAL POWER 3,096 2.39
P5V0
HMC542BLP4E 4*2.9=11.6 4*2.9=11.6
HMC349LP4C 4*3.5=14 4*3.5=14
TOTAL 5V0 25.6 25.6
TOTAL POWER 0,125 0,125
P7V0
ERA-3XSM+ 4*35=150 4*35=150
TOTAL POWER 1.05 1.05
DC/DC converter losses
TPS62175 eff .95 0,05*(.27+0,026)*7,5=0.11 0,05*(.27+0,026)*7,5=0.11
LTM:3.6V eff .9 0.1*1,321*3,6=0,47 0,1*1,346*3,6=0,48
LTM:2V eff .87 0.13*1,721*2=0,44 0.13*1.328*2=0.34
LDO losses
2V->1.8V 0.34 0,26
3.6V->3.3V 0.396 0.4
7.5V->7V 0,135 0,135
7.5V->5V 0,064 0,064
Total power from 12V 9.95W 9.05
Total current from 12V 0.83A 0.75A
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Project/Equipment ARTIQ/SINARA
Document
Power supply DC/DC & LDOs
Designer G.K.
Drawn by G.K. XX/XX/XXXX
Check.by -
Last Mod. - 18.09.2017
File Supply_DDS.SchDoc
Print Date 21.09.2017 01:14:46
Sheet 3 of 7
Warsaw Univeristy of Technology ISE
Nowowiejska 15/19
ARTIQ
Size A3
Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

50_Ohms
C164A Undefined
R48A 0
C172A Undefined
R49A 0
C176A Undefined
R50A 0
C180A Undefined
R51A 0
C203A Undefined
C204A Undefined
C205A Undefined
C206A Undefined
C207A Undefined
GND

DAC_OUT_N
DAC_OUT_P
49R9 9910 only
R38A 0
R39A 0
ADT1-1WT+ 1:1
TR1A
SEC PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible

R57A 0
R59A 0
Jumper
FL2A
IN OUT
DC to 320MHz
R58A 0
10nF C28A
Jumper

Digital Attenuator
F clk max = 30MHz
IC3A
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB 1dB 2dB 4dB 8dB 16dB
RF1
RF2
ACG1 ACG2 ACG3 ACG4 ACG5 ACG6 ACG7
NC
VCC GND
HMC542BLP4E
C14A C15A C16A C17A C18A C19A C20A 10nF
C36A 10nF

P5V0A
L7A 390R@100MHz
C21A 10uF
C22A 100nF
C23A 1nF
C24A 100pF

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R137 power = 35mA^2*100 = 0.12W

PAT1220-C-9DB-T5
IC17A 9dB
P7V0A
R137A 100
C12A 1uF
C27A 100nF
L1A TCCH-80+ 0.5uH@200mA
C55A 10nF
IC5A
ERA-3+
C29A 10nF
R61A Undefined

SPDT switch
IC23A
RFC
RD1 RD2
EN VCTL VDD
NC
HMC349ALP4CE
RFSW_CTRL
R20A 4k7
R138A 0
C49A 10nF
R23A Undefined
R2A 0
R24A Undefined
C50A 10nF
RF_OUT
C47A 10nF
R16A 180
R15A 180
C38A 100pF
C39A 10uF
C40A 100nF
L6A 390R@100MHz

Amplifier
~23 gain and 13 dBm P1dB

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Project/Equipment	ARTIQ/SINARA
Document	**Output stage : Attenuator, amplifier and filter**
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	DDS_OUT_channel.SchDoc
Print Date	21.09.2017 01:14:47 Sheet 4 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

Jumper

Jumper

Digital Attenuator

F clk max = 30MHz

HMC542BLP4E

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R137 power = 35mA^2*100 = 0.12W

SPDT switch

HMC349ALP4CE

Amplifier
~23 dB gain and 13 dBm P1dB

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Project/Equipment	ARTIQ/SINARA
Document	**Output stage : Attenuator, amplifier and filter**
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	DDS_OUT_channel.SchDoc
Print Date	21.09.2017 01:14:47 Sheet 4 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
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For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

50_Ohms
C164C Undefined
R48C 0
C172C Undefined
R49C 0
C176C Undefined
R50C 0
C180C Undefined
R51C 0
C202C Undefined
C203C Undefined
C204C Undefined
C205C Undefined
C206C Undefined
C207C Undefined
GND

DAC_OUT_N
DAC_OUT_P
49R9 9910 only
R38C 0
ADT1-1WT+ 1:1
TR1C
SEC PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible

R57C 0
R59C 0
Jumper
FL2C
DC to 320MHz
R58C 0
10nF C28C
Jumper

Digital Attenuator
F clk max = 30MHz

IC3C
HMC542BLP4E
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB 1dB 2dB 4dB 8dB 16dB
RF1
RF2
ACG1 ACG2 ACG3 ACG4 ACG5 ACG6 ACG7
NC
VCC GND
C14C 10nF
C15C 10nF
C16C 10nF
C17C 10nF
C18C 10nF
C19C 10nF
C20C 10nF
C36C 10nF

P5V0A
L7C 390R@100MHz
C21C 10uF
C22C 100nF
C23C 1nF
C24C 100pF

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

PAT1220-C-9DB-T5
IC17C 9dB

R137 power = 35mA^2*100 = 0.12W

P7V0A
R137C 100
C12C 1uF
C27C 100nF
L1C 0.5uH@200mA TCCH-80+
IC5C ERA-3+
C55C 10nF
C29C 10nF

Amplifier
~23 dB gain and 13 dBm P1dB

SPDT switch
IC23C
HMC349ALP4CE
RFC RF1 RF2 GND
EN VCTL VDD
RFSW_CTRL
R20C 4k7
R138C 0
C49C 10nF
R2C 0
C50C 10nF
RF_OUT
C47C 10nF
R140C 180
R141C 180
L6C 390R@100MHz
C38C 100pF
C39C 10uF
C40C 100nF

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Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter

Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	DDS_OUT_channel.SchDoc
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Nowowiejska 15/19

ARTIQ Size A3 Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

50_Ohms
C164D Undefined
R48D 0
C172D Undefined
R49D 0
C176D Undefined
R50D 0
C180D Undefined
R51D 0
C202D Undefined
C203D Undefined
C204D Undefined
C205D Undefined
C206D Undefined
C207D Undefined
GND

DAC_OUT_N
DAC_OUT_P
49R9 R38D
9910 only
49R9 R37D
9910 only
R39D 0
GND
ADT1-1WT+ 1:1
TR1D
SEC PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible

R57D 0
R59D 0
Jumper
FL2D
IN OUT
DC to 320MHz
R58D 0
10nF C28D
Jumper

Digital Attenuator

F clk max = 30MHz

IC3D HMC542BLP4E
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB 1dB 2dB 4dB 8dB 16dB
RF1
RF2
ACG1 ACG2 ACG3 ACG4 ACG5 ACG6 ACG7
NC
VCC GND
C14D 10nF
C15D 10nF
C16D 10nF
C17D 10nF
C18D 10nF
C19D 10nF
C20D 10nF
C36D 10nF

P5V0A
L7D 390R@100MHz
C21D 10uF
C22D 100nF
C23D 1nF
C24D 100pF

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

PAT1220-C-9DB-T5
IC17D 9dB

R137 power = 35mA^2*100 = 0.12W

P7V0A
R137D 100
C12D 1uF
C27D 100nF
0.5uH@200mA
L1D TCCH-80+
IC5D ERA-3+
C55D 10nF
C29D 10nF
R31D Undefined

Amplifier
~23 dB gain and 13 dBm P1dB

SPDT switch

IC23D HMC349ALP4E
RFC
RF1 RF2
EN VCTL VDD
NC
R138D 0
RFSW_CTRL
R20D 4k7
C49D 10nF
C50D 10nF
R2D 0
R32D Undefined
R47D Undefined
RF_OUT
C47D 10nF
R140D 180
R145D 180
L6D 390R@100MHz
C38D 100pF
C39D 10uF
C40D 100nF

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Project/Equipment	ARTIQ/SINARA
Document	**Output stage : Attenuator, amplifier and filter**
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	DDS_OUT_channel.SchDoc
Print Date	21.09.2017 01:14:48 Sheet 4 of 7
Warsaw Univeristy of Technology ISE Nowowiejska 15/19	ARTIQ Size A3 Rev -

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK	Output Frequency
S4	S3	S2	S1	Input Mode	(MHz)
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

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Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 19.09.2017
File	DDS_channel.SchDoc
Print Date	21.09.2017 01:14:48 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

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1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

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Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 19.09.2017
File	DDS_channel.SchDoc
Print Date	21.09.2017 01:14:49 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE ARTIQ Size A3 Rev -

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0	1	0	0	Xtal/PLL	77.75879
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0	1	1	0	Xtal/PLL	122.87903
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1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

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Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 19.09.2017
File	DDS_channel.SchDoc
Print Date	21.09.2017 01:14:49 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

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0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

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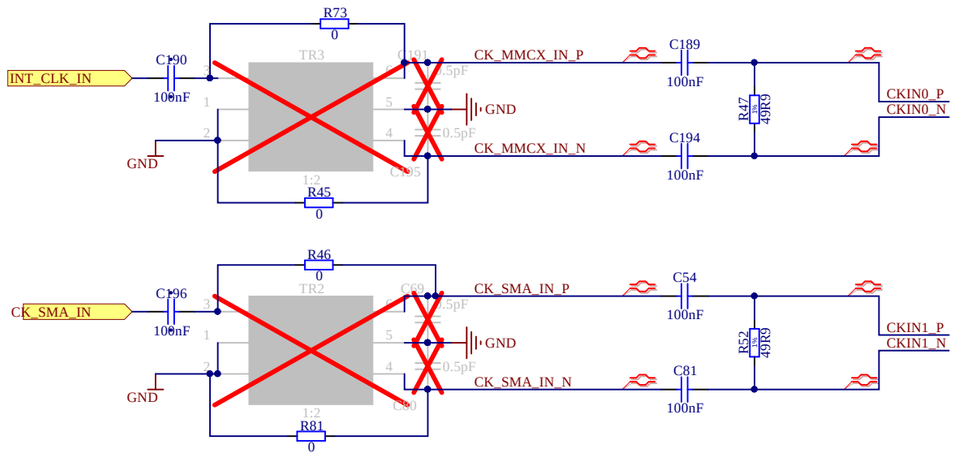
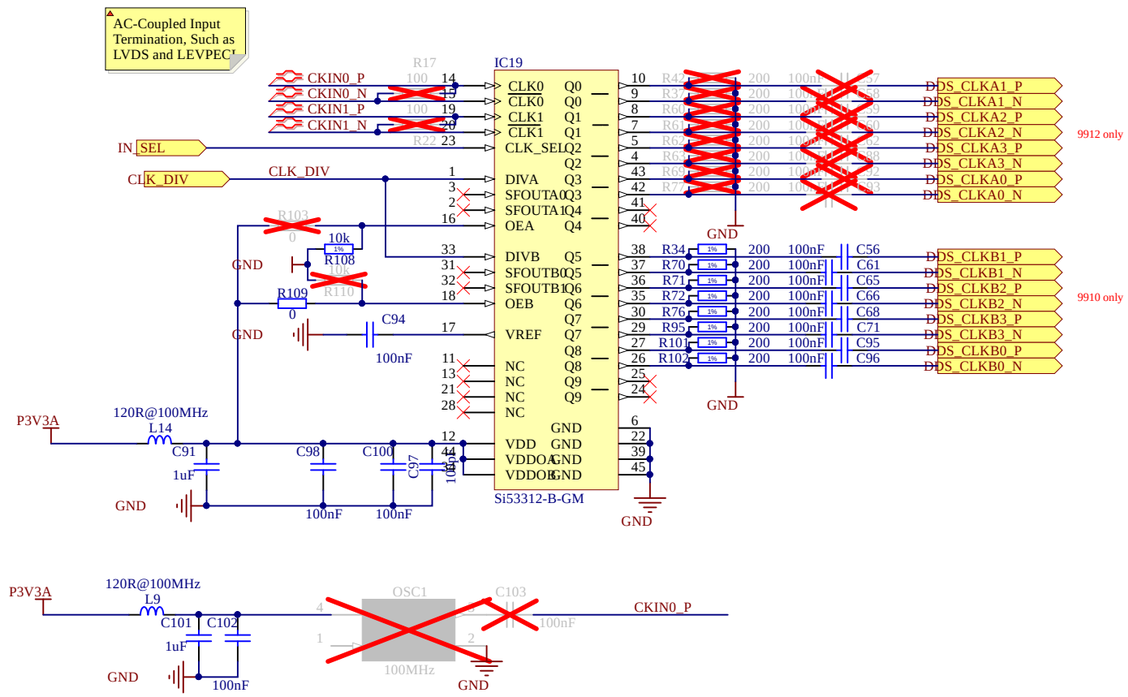
Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 19.09.2017
File	DDS_channel.SchDoc
Print Date	21.09.2017 01:14:50 Sheet 5 of 7
Warsaw Univeristy of Technology ISE Nowowiejska 15/19	ARTIQ Size A3 Rev -





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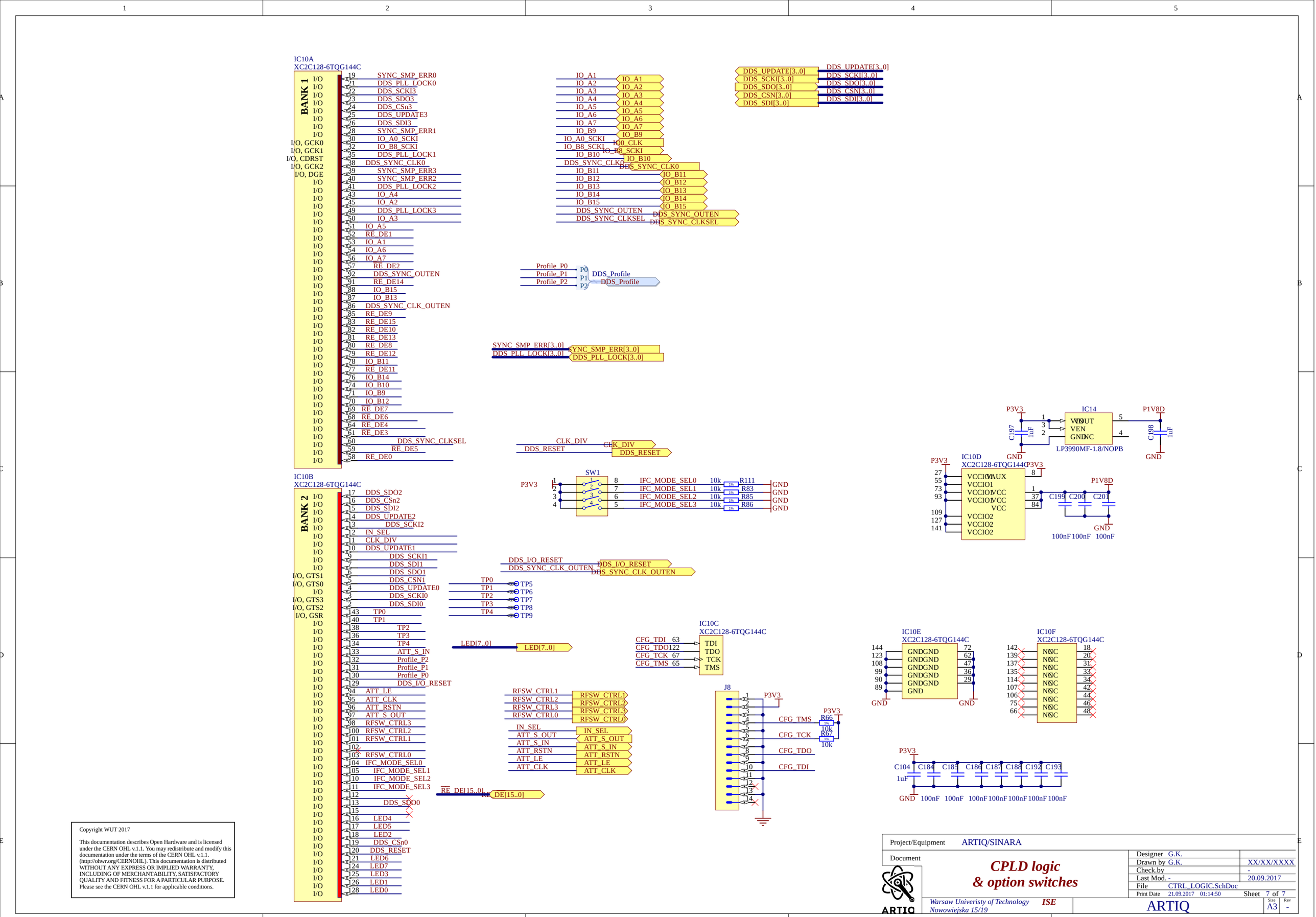
Project/Equipment	ARTIQ/SINARA		
Document	**Clock distribution and generation**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File CLK_INPUT.SchDoc	
		Print Date 21.09.2017 01:14:50	Sheet 6 of 7
Warsaw Univeristy of Technology *Nowowiejska 15/19*	*ISE*	ARTIQ	Size A3 / Rev -



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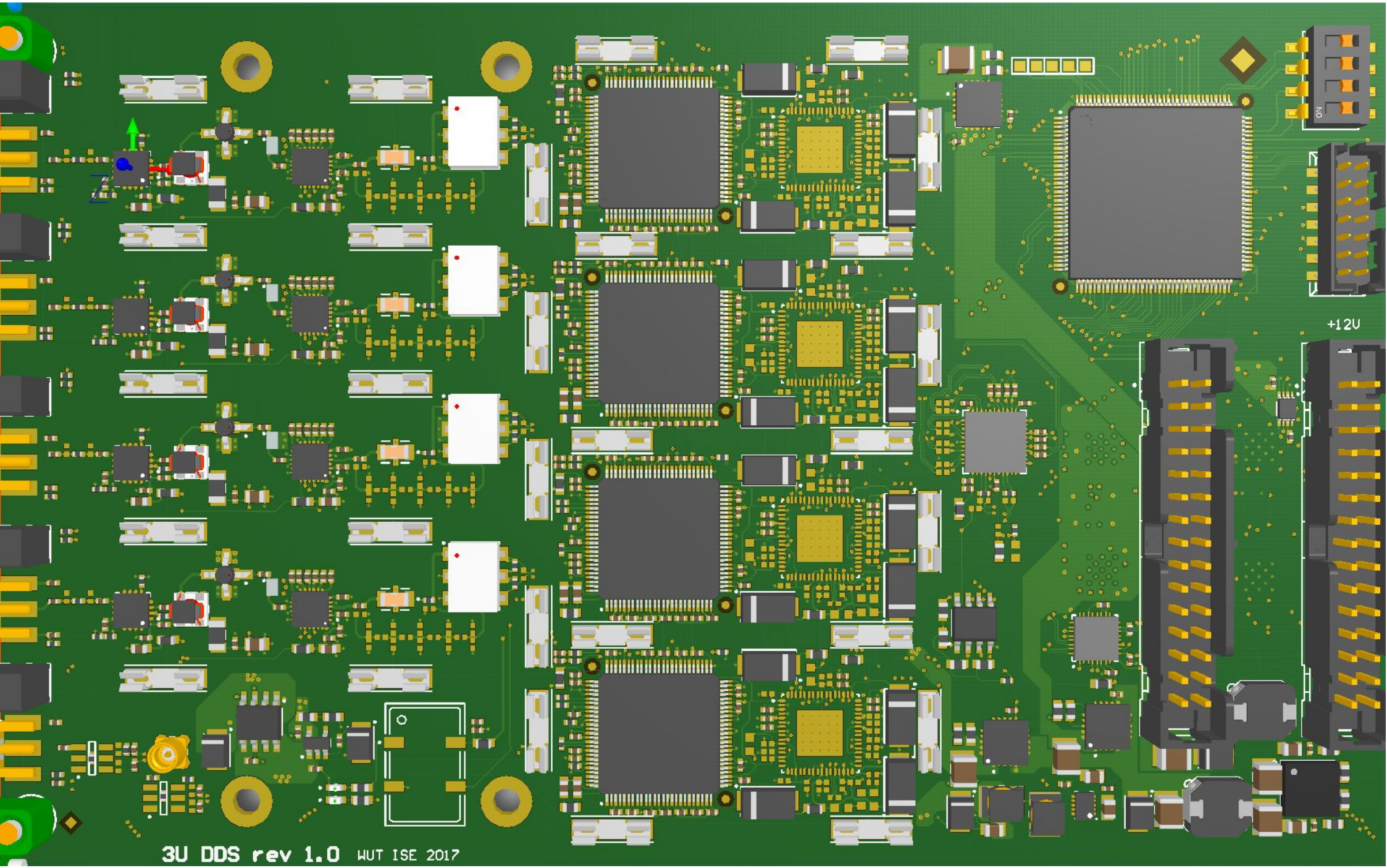
Project/Equipment	ARTIQ/SINARA
Document	**CPLD logic & option switches**
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 20.09.2017
File	CTRL_LOGIC.SchDoc
Print Date	21.09.2017 01:14:50 Sheet 7 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -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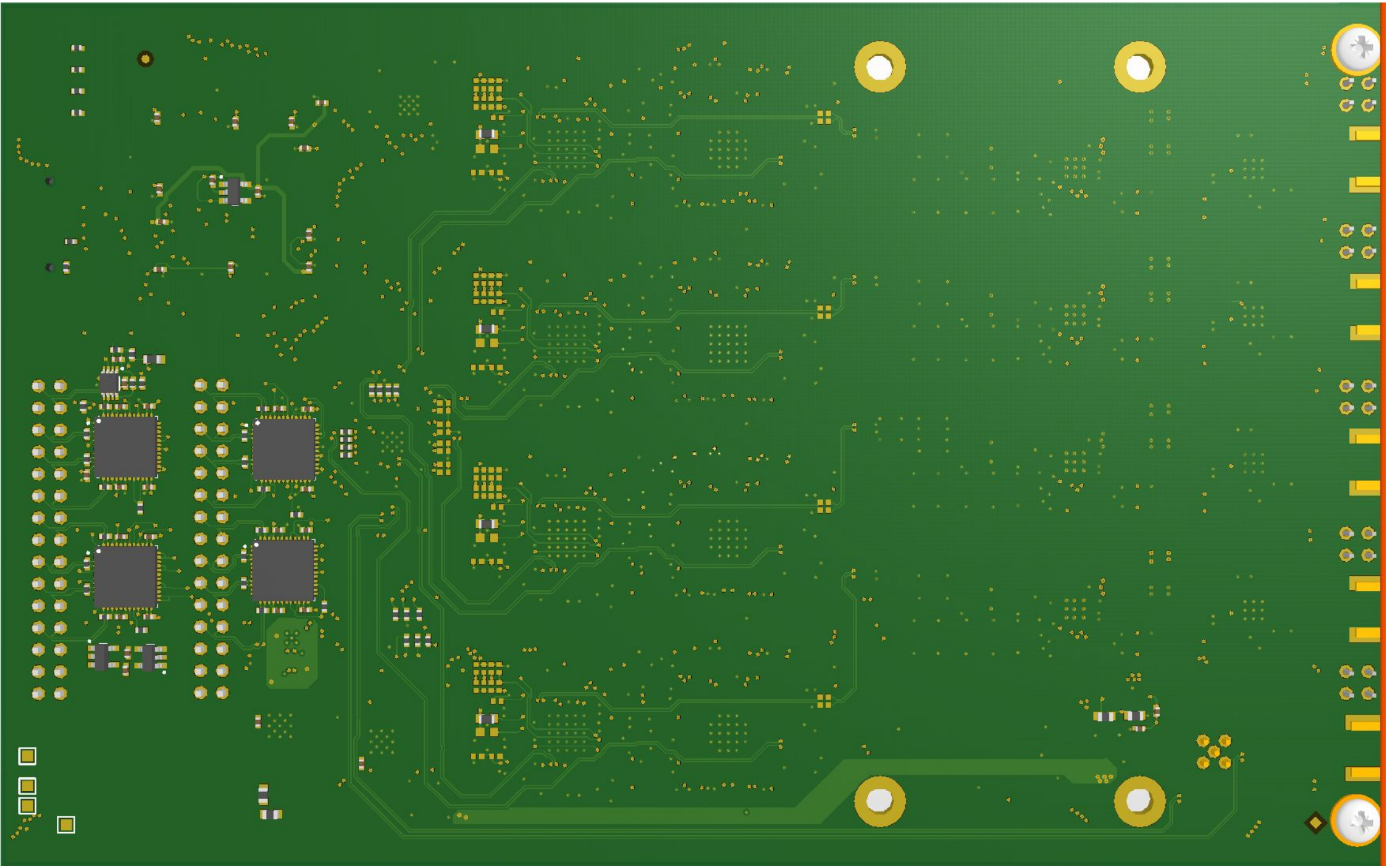

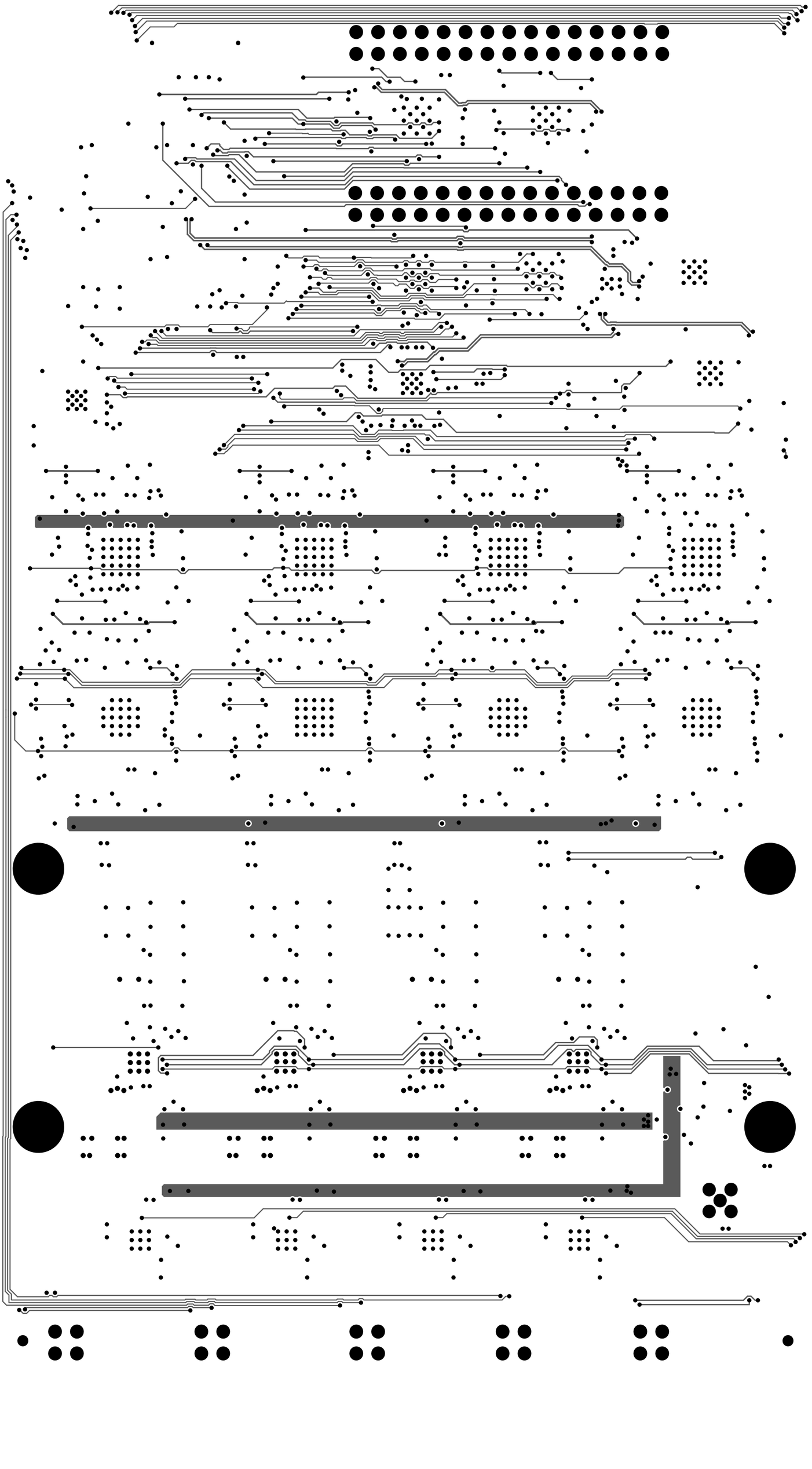

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