shield clips

CLIP1 CLIP2 CLIP3 CLIP4 CLIP5
CLIP6 CLIP7 CLIP8 CLIP9 CLIP10 CLIP27
CLIP11 CLIP12 CLIP13 CLIP14 CLIP15 CLIP28
CLIP16 CLIP17 CLIP18 CLIP19 CLIP20 CLIP29
CLIP21 CLIP22 CLIP23 CLIP24 CLIP25 CLIP26
(all GND)

Ext clock input

Clock from Kasli

Output SMAs

U_CLK_INPUT
CLK_INPUT.SchDoc
CK_SMA_IN, IN_SEL, CLK_DIV, INT_CLK_IN
DDS_CLKA0_P/N, DDS_CLKA1_P/N, DDS_CLKA1_N, DDS_CLKA2_P/N, DDS_CLKA3_P/N, DDS_CLKB0_P/N, DDS_CLKB1_P/N, DDS_CLKB2_P/N, DDS_CLKB3_P/N

U_CTRL_LOGIC
CTRL_LOGIC.SchDoc
RFSW_CTRL0..3, RE_DE[15..0], IO0_CLK, IO_A1..A7, DDS_SDO[3..0], DDS_SDI[3..0], DDS_SCKI[3..0], DDS_CSN[3..0], IN_SEL, CLK_DIV, DDS_UPDATE[3..0], DDS_SYNC_CLK0, DDS_PLL_LOCK[3..0], SYNC_SMP_ERR[3..0], DDS_Profile, DDS_I/O_RESET, DDS_RESET, LED[7..0], ATT_CLK, ATT_LE, ATT_RSTn, ATT_S_IN, ATT_S_OUT, IO_B8_SCKI, IO_B9, IO_B10, IO_B11, IO_B12, IO_B13, IO_B14, IO_B15, DDS_SYNC_CLKSEL, DDS_SYNC_OUTEN, DDS_SYNC_CLK_OUTEN

LVDS_IFC_DDS.SchDoc U_LVDS_IFC
EEM A
IO0..IO7, LVDS0_P/N, LVDS1_P/N, LVDS7_P/N, I2C_SDA, I2C_SCL, RE_DE0..RE_DE7

LVDS_IFC_DDS.SchDoc U_LVDS_IFC
EEM B
IO0..IO7, LVDS0_P/N, LVDS1_P/N, LVDS7_P/N, I2C_SDA, I2C_SCL, RE_DE8..RE_DE15

PLACE IT CLOSE TO LVDS Rx/Tx
IC4, FIN1101K8X

PLACE IT CLOSE TO LVDS Rx/Tx
IC9, Si53304-B-GM

U_DDS_OUT_channel0
DDS_OUT_channel.SchDoc
DAC_OUT_P/N, RF_OUT, ATT_CLK, RFSW_CTRL, ATT_LE, ATT_RSTn, ATT_S_IN, ATT_S_OUT

U_DDS_OUT_channel1
DDS_OUT_channel.SchDoc
DAC_OUT_P/N, RF_OUT, ATT_CLK, RFSW_CTRL, ATT_LE, ATT_RSTn, ATT_S_IN, ATT_S_OUT

U_DDS_OUT_channel2
DDS_OUT_channel.SchDoc
DAC_OUT_P/N, RF_OUT, ATT_CLK, RFSW_CTRL, ATT_LE, ATT_RSTn, ATT_S_IN, ATT_S_OUT

U_DDS_OUT_channel3
DDS_OUT_channel.SchDoc
DAC_OUT_P/N, RF_OUT, ATT_CLK, RFSW_CTRL, ATT_LE, ATT_RSTn, ATT_S_IN, ATT_S_OUT

U_DDS_channel0
DDS_channel.SchDoc
DAC_OUT_P/N, SDO, SDI, SCKI, CSN, IO_UPDATE, PLL_LOCK, SYNC_SMP_ERR, DDS_Profile, DDS_CLKA0_P/N, DDS_CLKB0_P/N, SYNC_OUT_P/N, SYNC_CLK, I/O_RESET, RESET, SYNC_IN_P/N, DDS_CLKA_P/N, DDS_CLKB_P/N

DDS_channel.SchDoc U_DDS_channel1
DAC_OUT_P/N, SDO, SDI, SCKI, CSN, IO_UPDATE, PLL_LOCK, SYNC_SMP_ERR, DDS_Profile, DDS_CLKA1_P/N, DDS_CLKB1_P/N, SYNC_OUT_P/N, SYNC_CLK, I/O_RESET, RESET, SYNC_IN_P/N, DDS_CLKA_P/N, DDS_CLKB_P/N

DDS_channel.SchDoc U_DDS_channel2
DAC_OUT_P/N, SDO, SDI, SCKI, CSN, IO_UPDATE, PLL_LOCK, SYNC_SMP_ERR, DDS_Profile, DDS_CLKA2_P/N, DDS_CLKB2_P/N, SYNC_OUT_P/N, SYNC_CLK, I/O_RESET, RESET, SYNC_IN_P/N, DDS_CLKA_P/N, DDS_CLKB_P/N

DDS_channel.SchDoc U_DDS_channel3
DAC_OUT_P/N, SDO, SDI, SCKI, CSN, IO_UPDATE, PLL_LOCK, SYNC_SMP_ERR, DDS_Profile, DDS_CLKA3_P/N, DDS_CLKB3_P/N, SYNC_OUT_P/N, SYNC_CLK, I/O_RESET, RESET, SYNC_IN_P/N, DDS_CLKA_P/N, DDS_CLKB_P/N

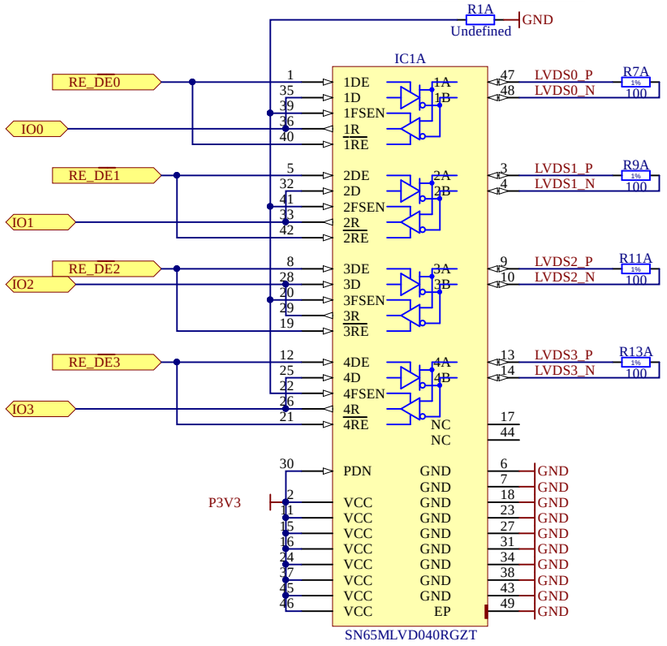
When routing please do a reasonable (100ps) length match within each of DDS_SYNC_CLK[3:0], DDS_UPDATE[3:0], RFSW_CTRL[3:0], IO[15:11] (nominally the RFSW_CTRL lines), DDS[3:0]_SYNC_IN, DDS_RESET and a really good one on DDS_CLK[3:0]_[PN].

U_Supply_DDS
Supply_DDS.SchDoc

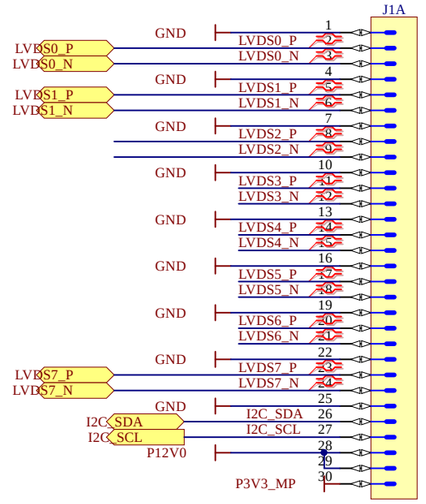
FTG1 FTG2 FTG3 FTG4

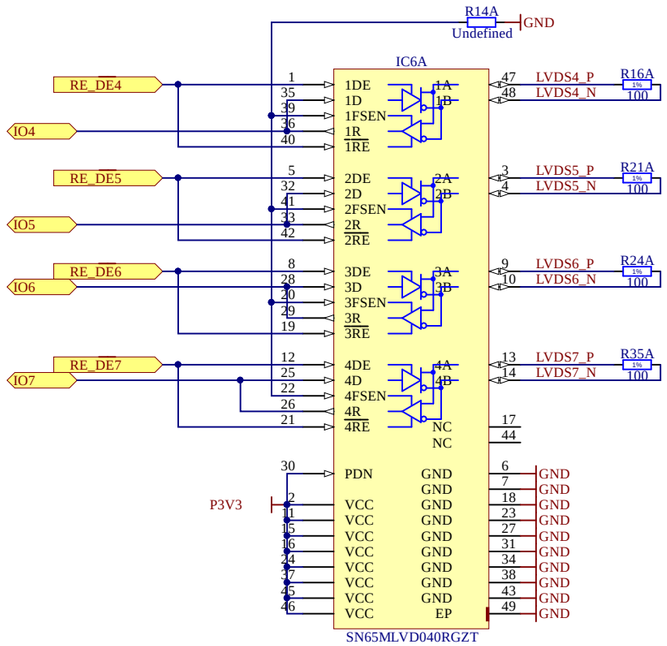
Project/Equipment	ARTIQ/SINARA
Document	3U DDS (URUKUL) Top entity
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 21.09.2017
File	PCB_3U_DDS.schdoc
Print Date	21.09.2017 20:32:23 Sheet 1 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19 ISE	ARTIQ Size A3 Rev -

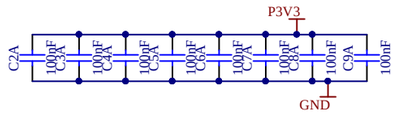
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

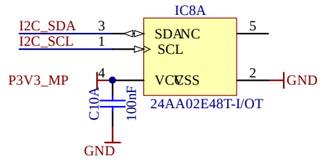


This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A



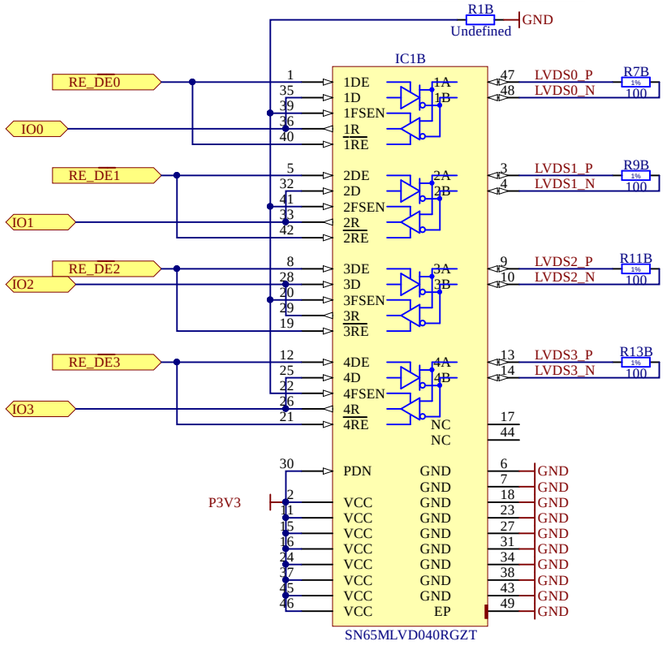




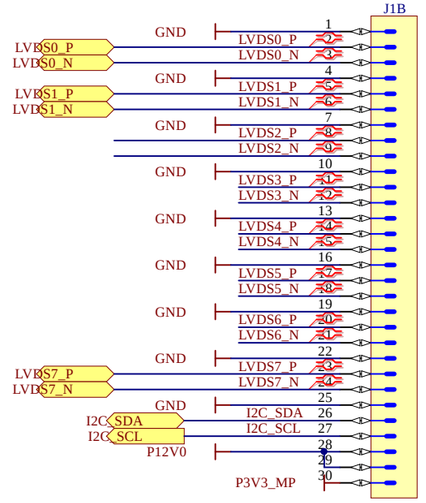


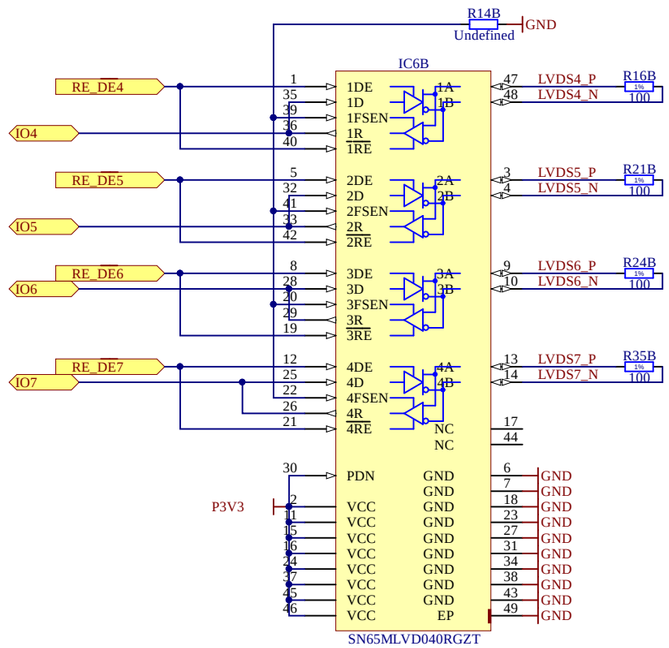
Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File LVDS_IFC_DDS.SchDoc	
		Print Date 21.09.2017 20:32:24	Sheet 2 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	*ISE*	ARTIQ	Size A3 / Rev -

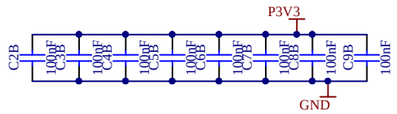
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

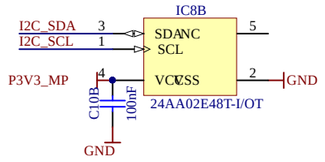


This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A

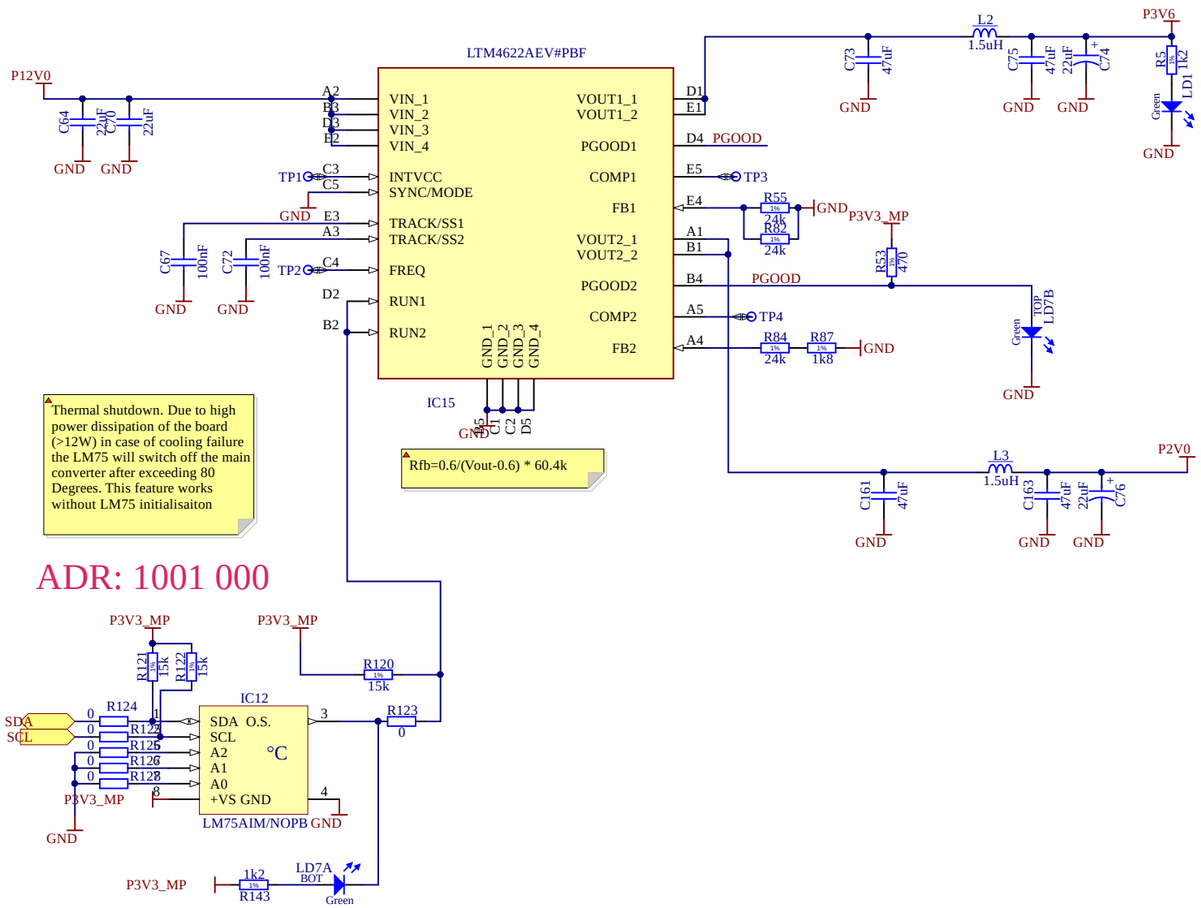








Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File LVDS_IFC_DDS.SchDoc	
		Print Date 21.09.2017 20:32:24	Sheet 2 of 7
Warsaw Univeristy of Technology *Nowowiejska 15/19* *ISE*	ARTIQ	Size A3	Rev -



Power budget (max ratings):

	AD9912 variant(mA)	AD9910 variant(mA)
P3V3:		
LVDS interface 4x	660	660
LVDS load 4x24mA	96	96
CPLD	100	100
ADCLK948	230	230
DDS AVDD3	4*(9,6+31)=133,6	4*29=116
DDS DVDDIO	4*3=12	4*11=44
TOTAL P3V3	1121	1146
TOTAL POWER	3.7	3.7
P1V8:		
DDS AVDD	4*(48+136)=736	4*110=440
DDS DVDD	4*246=984	4*222=888
TOTAL P1V8	1720	1328
TOTAL POWER	3,096	2.39
P5V0		
HMC542BLP4E	4*2.9=11.6	4*2.9=11.6
HMC349LP4C	4*3.5=14	4*3.5=14
TOTAL 5V0	25.6	25.6
TOTAL POWER	0,125	0,125
P7V0		
ERA-3XSM+	4*35=150	4*35=150
TOTAL POWER	1.05	1.05
DC/DC converter losses		
TPS62175 eff .95	0,05*(.27+0,026)*7,5=0.11	0,05*(.27+0,026)*7,5=0.11
LTM:3.6V eff .9	0.1*1,321*3,6=0,47	0,1*1,346*3,6=0,48
LTM:2V eff .87	0.13*1,721*2=0,44	0.13*1.328*2=0.34
LDO losses		
2V->1.8V	0.34	0,26
3.6V->3.3V	0.396	0.4
7.5V->7V	0,135	0,135
7.5V->5V	0,064	0,064
Total power from 12V	9.95W	9.05
Total current from 12V	0.83A	0.75A

Project/Equipment	ARTIQ/SINARA		
Document	**Power supply DC/DC & LDOs**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	21.09.2017
		File Supply_DDS.SchDoc	
		Print Date 21.09.2017 20:32:24	Sheet 3 of 7
Warsaw Univeristy of Technology ISE Nowowiejska 15/19	ARTIQ	Size A3	Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

50_Ohms
C164A 0 Undefined
R48A 0
C172A 0 Undefined
R49A 0
C176A 0 Undefined
R50A 0
C180A 0 Undefined
R51A 0
C203A 0 Undefined
C204A 0 Undefined
C205A 0 Undefined
C206A 0 Undefined
C207A 0 Undefined
GND

DAC_OUT_N
DAC_OUT_P
49R9 9910 only
R38A 0
R39A 0
ADT1-1WT+ 1:1
TR1A
SEC PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible

R57A 0
R59A 0
Jumper
FL2A
IN OUT
DC to 320MHz
R58A 0
10nF C28A
Jumper

Digital Attenuator
F clk max = 30MHz
IC3A
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB 1dB 2dB 4dB 8dB 16dB
RF1
RF2
ACG1 ACG2 ACG3 ACG4 ACG5 ACG6 ACG7
NC
VCC GND
HMC542BLP4E
C14A C15A C16A C17A C18A C19A C20A 10nF
C36A 10nF

P5V0A
L7A 390R@100MHz
C21A 10uF
C22A 100nF
C23A 1nF
C24A 100pF

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R137 power = 35mA^2*100 = 0.12W

PAT1220-C-9DB-T5
IC17A 9dB
P7V0A
R137A 100
C12A 1uF
C27A 100nF
L1A TCCH-80+ 0.5uH@200mA
C55A 10nF
IC5A ERA-3+
C29A 10nF
R32A Undefined

SPDT switch
IC23A
RFC
RF1
RF2
EN
VCTL
VDD
HMC349ALP4CE
R138A 0
RFSW_CTRL
R20A 4k7
C49A 10nF
R2A 0
C50A 10nF
RF_OUT
C47A 10nF
R16A 180
R19A 180
C38A 100pF
C39A 10uF
C40A 100nF
L6A 390R@100MHz

Amplifier
~23 dB gain and 13 dBm P1dB

Project/Equipment	ARTIQ/SINARA
Document	**Output stage : Attenuator, amplifier and filter**
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 21.09.2017
File	DDS_OUT_channel.SchDoc
Print Date	21.09.2017 20:32:25 Sheet 4 of 7
Warsaw Univeristy of Technology ISE Nowowiejska 15/19	ARTIQ Size A3 Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

Digital Attenuator

F clk max = 30MHz

Jumper

Jumper

9912 devkit uses ADT2-1T-1P wich is footprint compatible

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R137 power = 35mA^2*100 = 0.12W

SPDT switch

Amplifier
~23 dB gain and 13 dBm P1dB

Project/Equipment	ARTIQ/SINARA		
Document	**Output stage : Attenuator, amplifier and filter**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	21.09.2017
		File DDS_OUT_channel.SchDoc	
		Print Date 21.09.2017 20:32:25	Sheet 4 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19 *ISE*	ARTIQ	Size A3	Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

Jumper

Jumper

Digital Attenuator

F clk max = 30MHz

HMC542BLP4E

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R137 power = 35mA^2*100 = 0.12W

SPDT switch

HMC349ALP4CE

Amplifier
~23 dB gain and 13 dBm P1dB

Project/Equipment	ARTIQ/SINARA
Document	**Output stage : Attenuator, amplifier and filter**
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 21.09.2017
File	DDS_OUT_channel.SchDoc
Print Date	21.09.2017 20:32:25 Sheet 4 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
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Jumper

Jumper

Digital Attenuator

F clk max = 30MHz

HMC542BLP4E

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R137 power = 35mA^2*100 = 0.12W

SPDT switch

HMC349ALP4CE

Amplifier
~23 dB gain and 13 dBm P1dB

ERA-3+

9912 devkit uses ADT2-1T-1P wich is footprint compatible

Project/Equipment	ARTIQ/SINARA		
Document	**Output stage : Attenuator, amplifier and filter**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	21.09.2017
		File DDS_OUT_channel.SchDoc	
		Print Date 21.09.2017 20:32:26	Sheet 4 of 7
Warsaw Univeristy of Technology ISE *Nowowiejska 15/19*	ARTIQ	Size A3	Rev -

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Project/Equipment ARTIQ/SINARA

Document **9910 & 9912 DDS**

Designer	G.K.	
Drawn by	G.K.	XX/XX/XXXX
Check.by		-
Last Mod.	-	21.09.2017
File	DDS_channel.SchDoc	
Print Date	21.09.2017 20:32:26	Sheet 5 of 7

Warsaw Univeristy of Technology ISE
Nowowiejska 15/19

ARTIQ | Size A3 | Rev -

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

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0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 21.09.2017
File	DDS_channel.SchDoc
Print Date	21.09.2017 20:32:27 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 21.09.2017
File	DDS_channel.SchDoc
Print Date	21.09.2017 20:32:27 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

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1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Project/Equipment ARTIQ/SINARA

Document **9910 & 9912 DDS**

Designer	G.K.	
Drawn by	G.K.	XX/XX/XXXX
Check.by		-
Last Mod.	-	21.09.2017
File	DDS_channel.SchDoc	
Print Date	21.09.2017 20:32:28	Sheet 5 of 7

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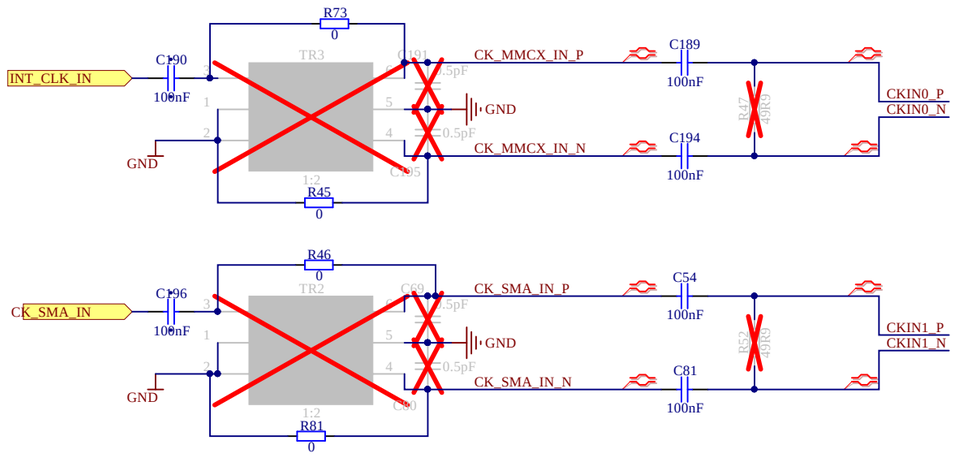
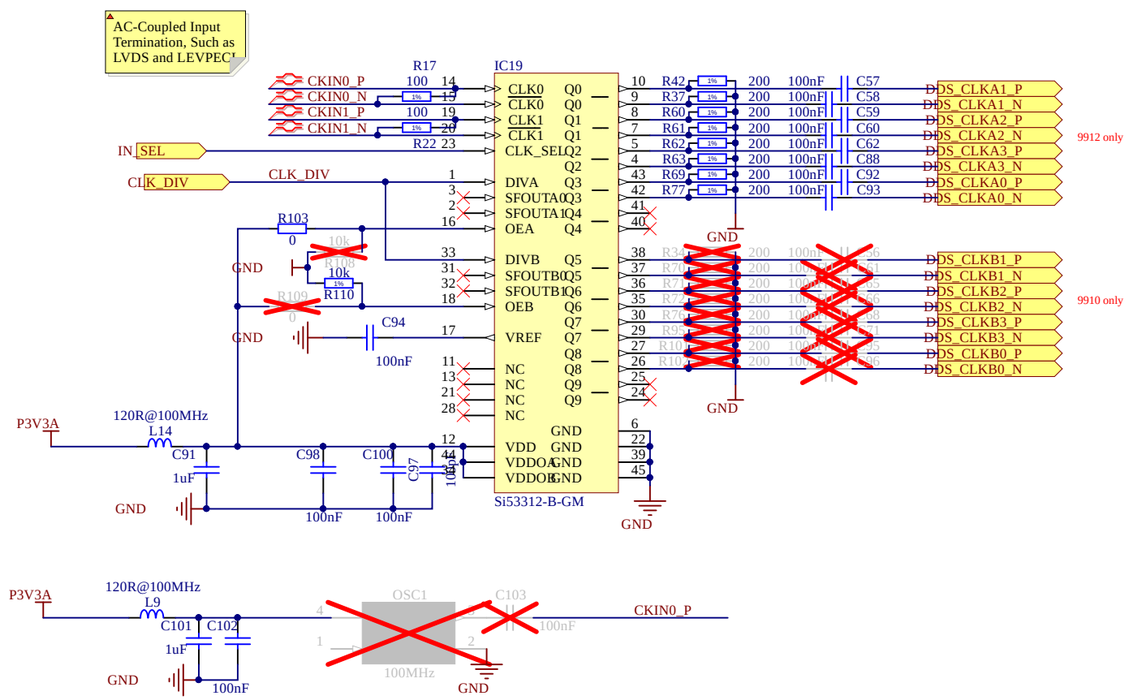
Nowowiejska 15/19

ARTIQ | Size A3 | Rev -





Project/Equipment: ARTIQ/SINARA

Document: **Clock distribution and generation**

Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	CLK_INPUT.SchDoc
Print Date	21.09.2017 20:32:28 Sheet 6 of 7

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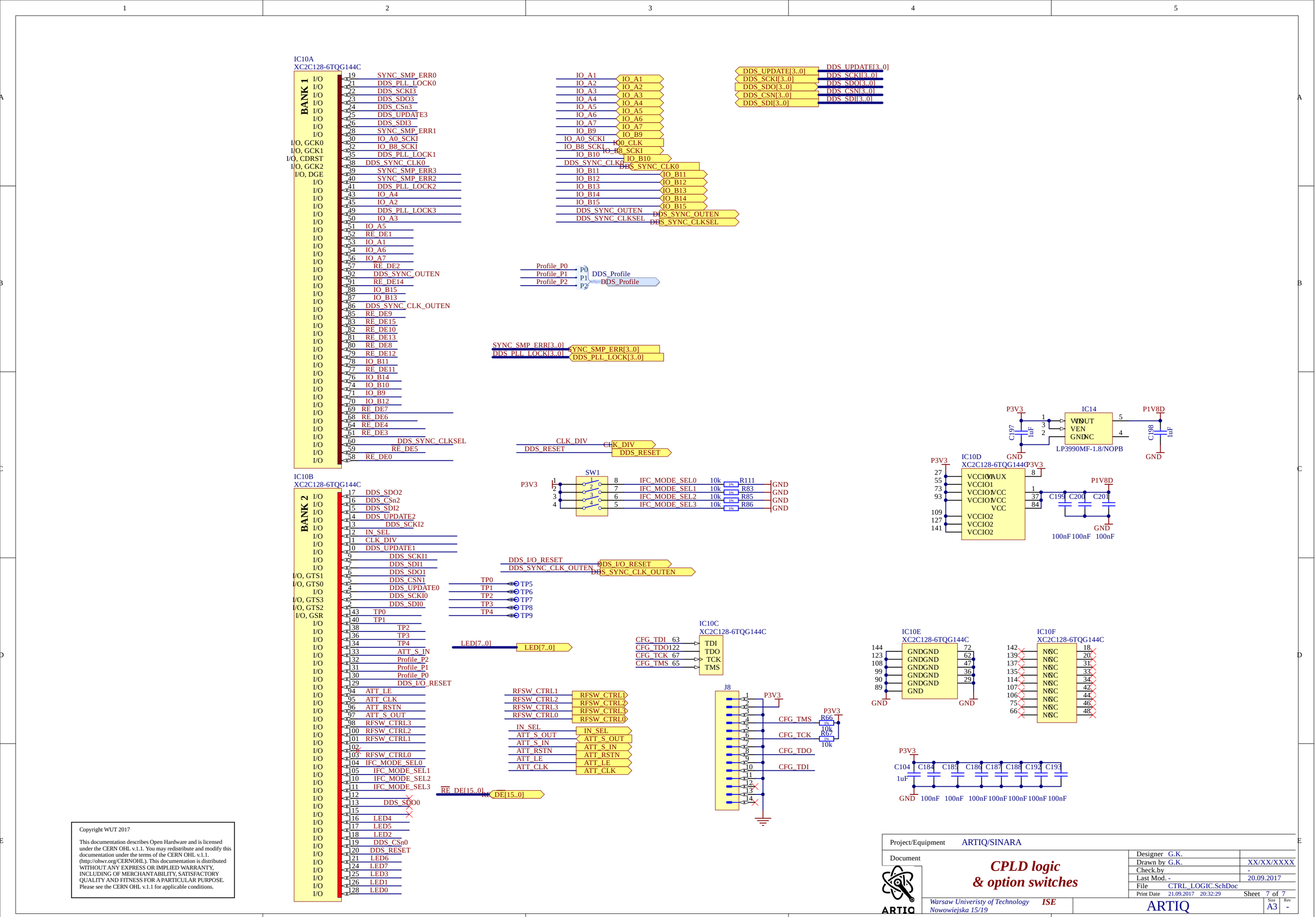
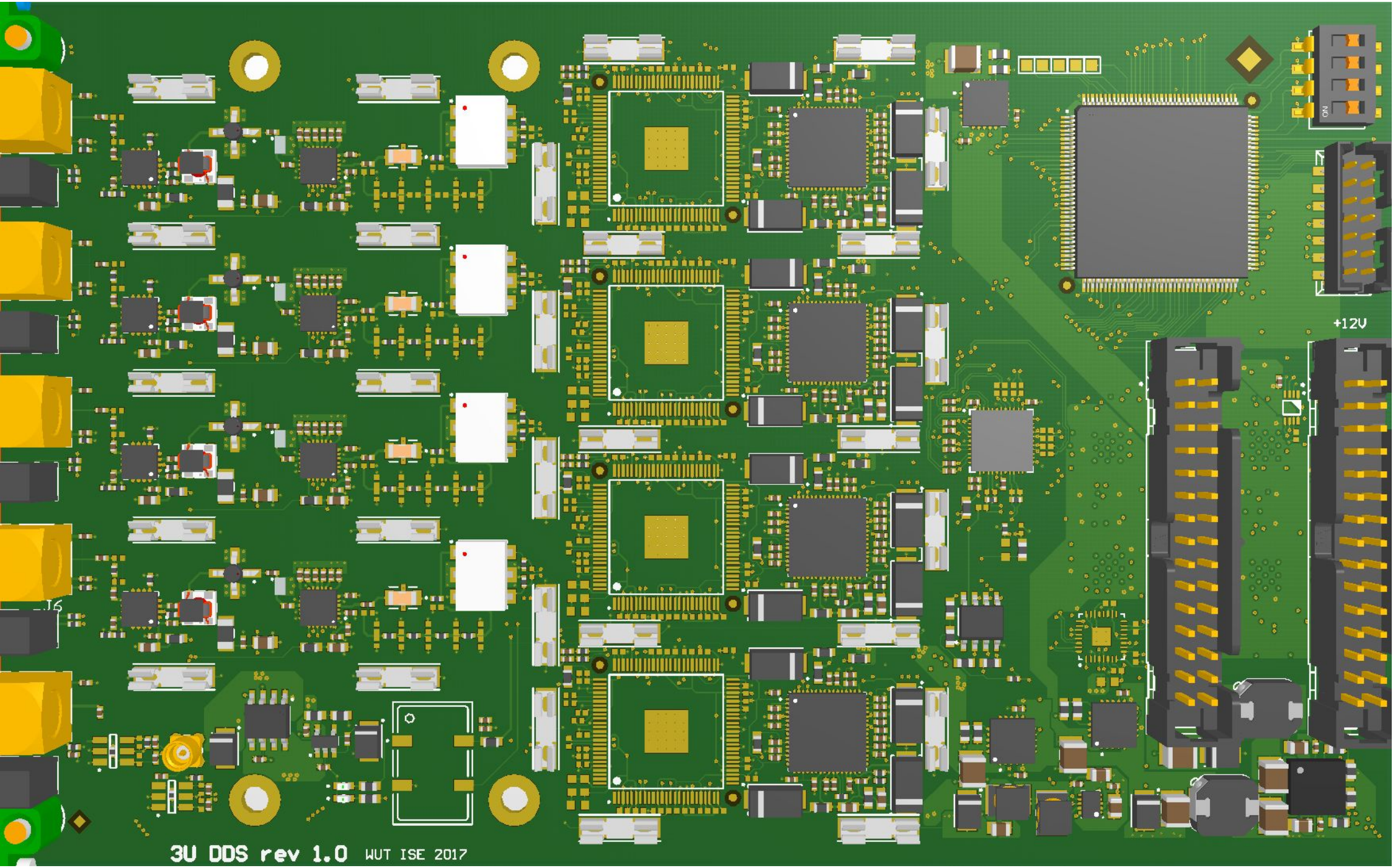
Nowowiejska 15/19

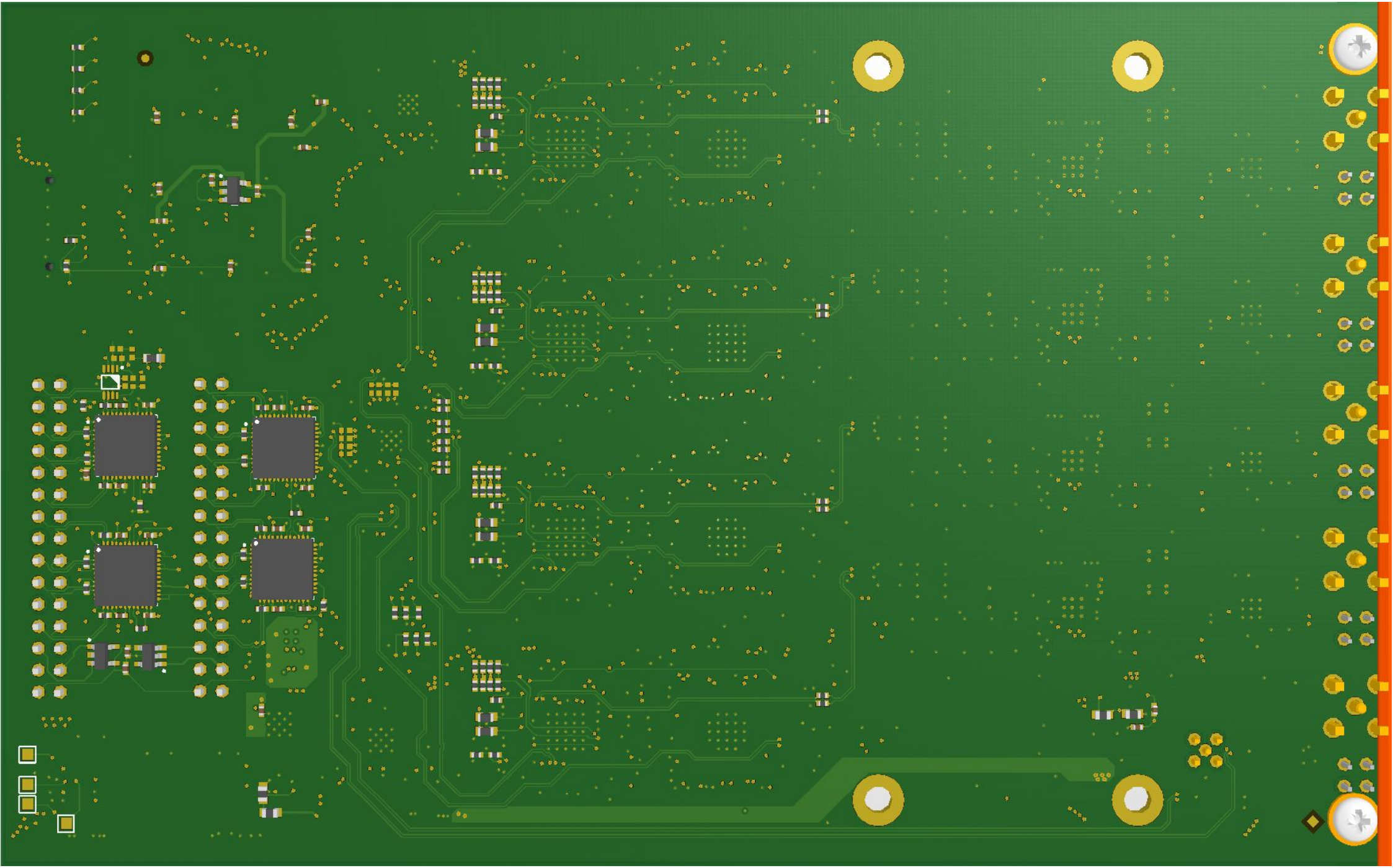
ARTIQ

Size A3 Rev -



Project/Equipment	ARTIQ/SINARA
Document	**CPLD logic & option switches**
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 20.09.2017
File	CTRL_LOGIC.SchDoc
Print Date	21.09.2017 20:32:29 Sheet 7 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -


+12V
3U DDS rev 1.0
WUT ISE 2017



ON
1 2 3 4

+12V

TO KASLI/METLINO VHDCI

30

30

J6

3U DDS rev 1.0 WUT ISE 2017