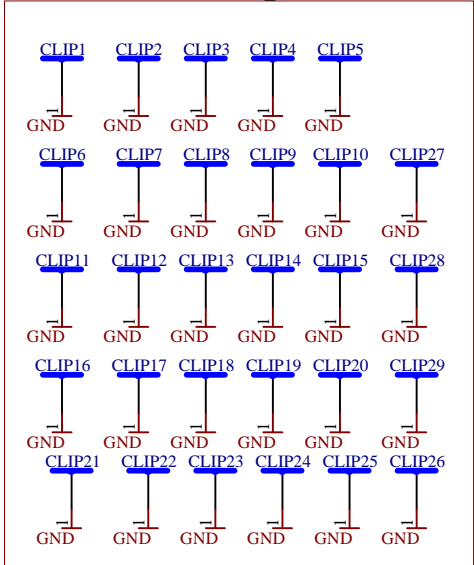


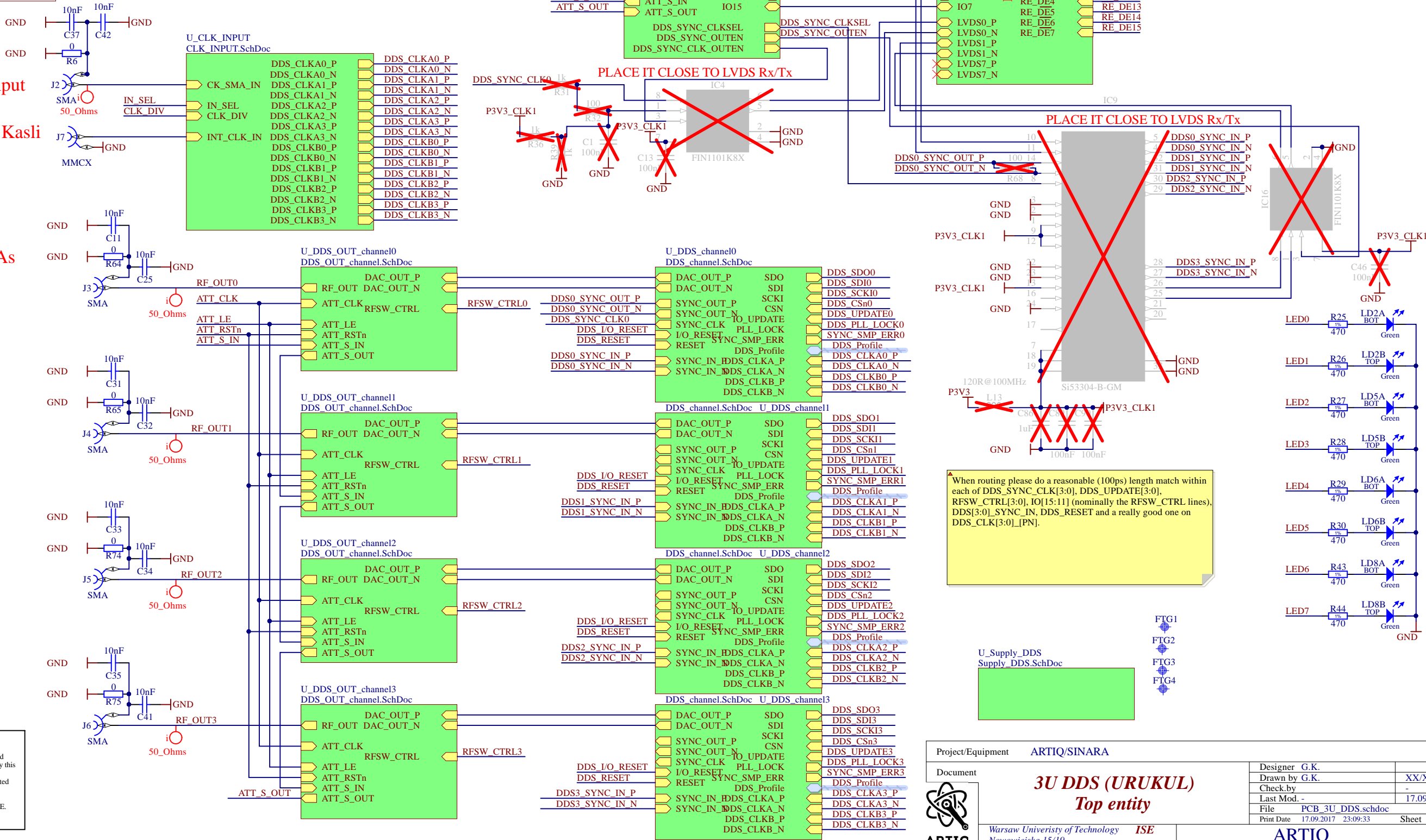
shield clips



Ext clock input

Clock from Kasli

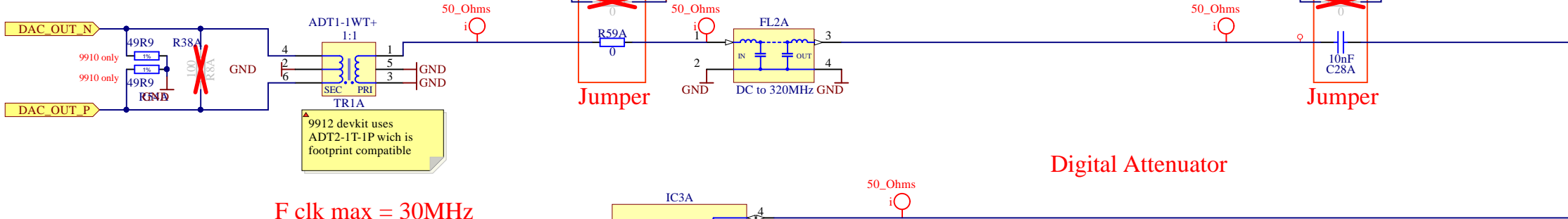
Output SMAs



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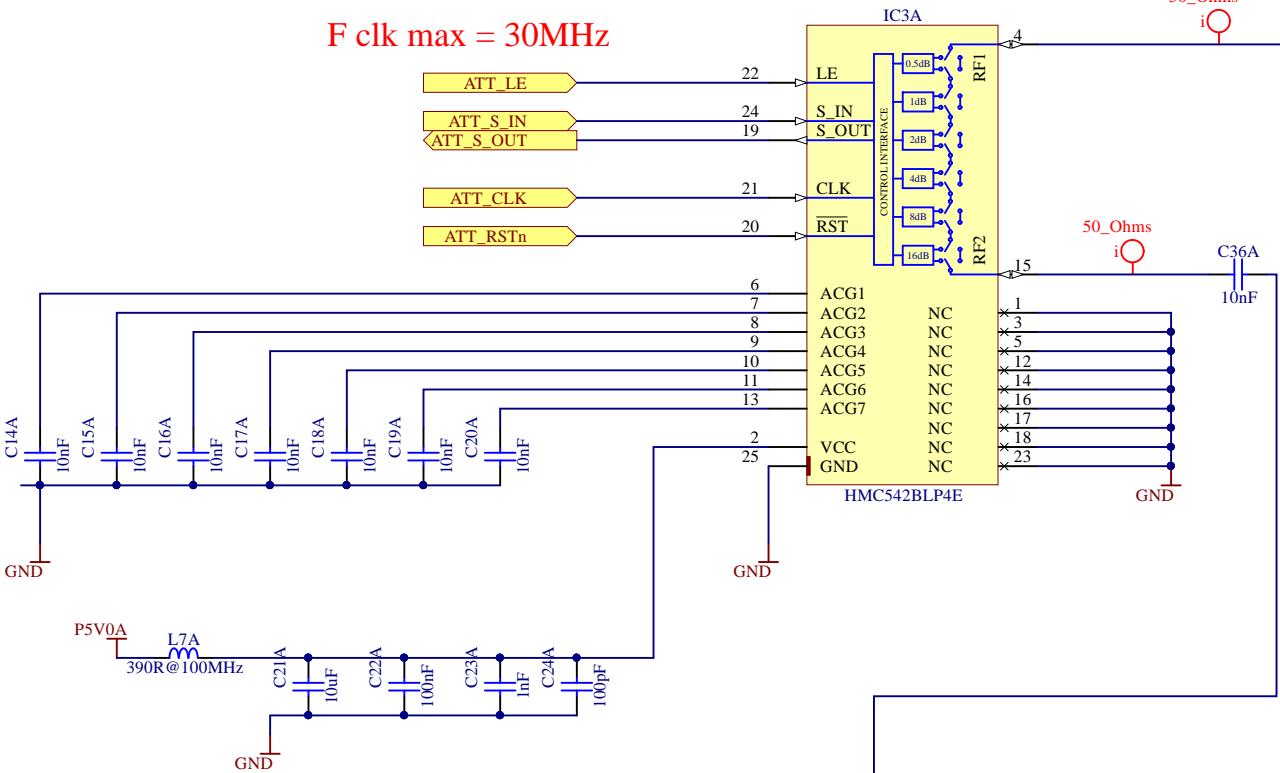
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Designer		G.K.	XX/XX/XXXX
Drawn by		G.K.	-
Check by		-	17.09.2017
Last Mod.		-	-
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Print Date		17.09.2017 23:09:33	Size A3
Warsaw University of Technology		ISE	Rev -
Nowowiejska 15/19		ARTIQ	-

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28) for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom Filter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder



F clk max = 30MHz

Digital Attenuator



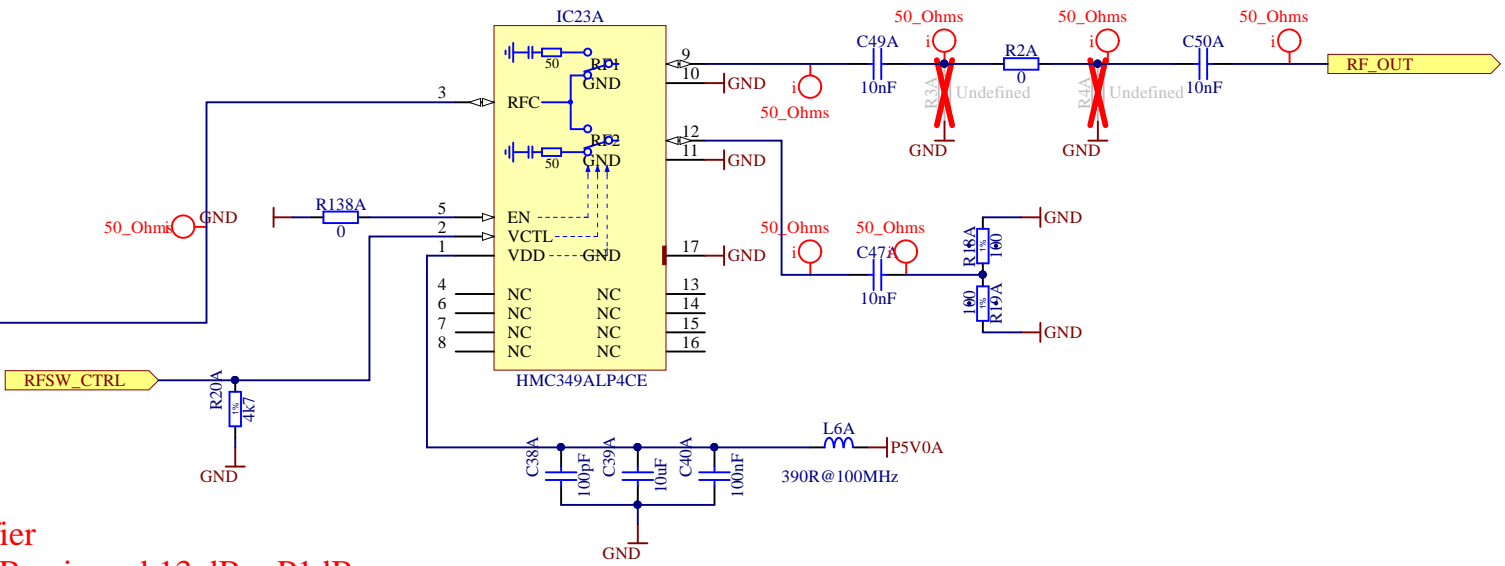
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R5 power = $65\text{mA}^2 \times 39 = 0.16\text{W}$

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Amplifier
~23 dB gain and 13 dBm P1dB

SPDT switch



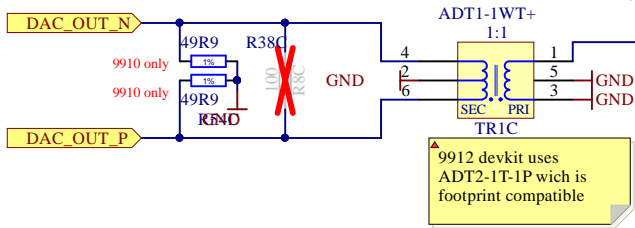
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		Check by	-
		Last Mod.	17.09.2017
File	DDS_OUT_channel.SchDoc	Print Date	17.09.2017 23:09:35
		Sheet	4 of 7
		Size	A3
		Rev	-

Output stage :
Attenuator, amplifier and filter

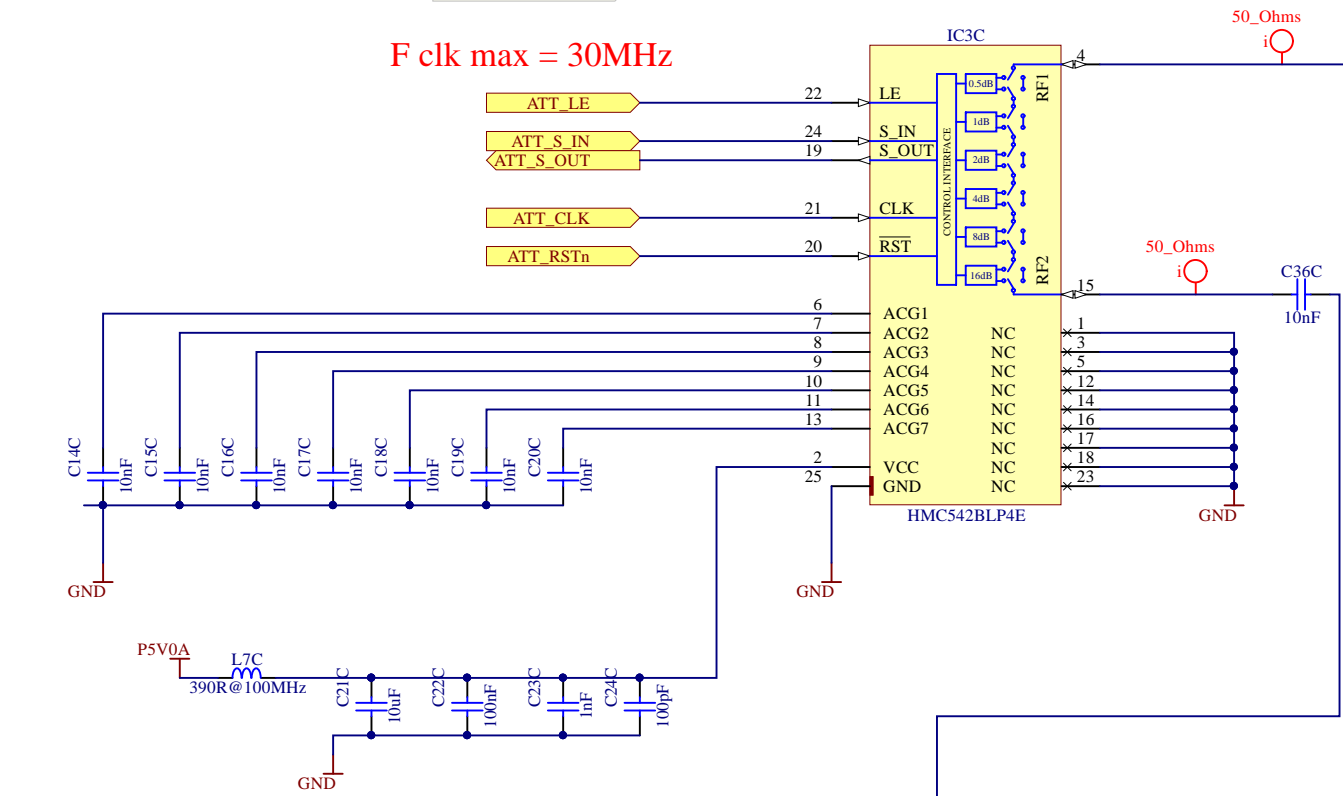
Warsaw University of Technology ISE
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ARTIQ

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28) for jumper configuration see ADC_channel sheet
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F clk max = 30MHz



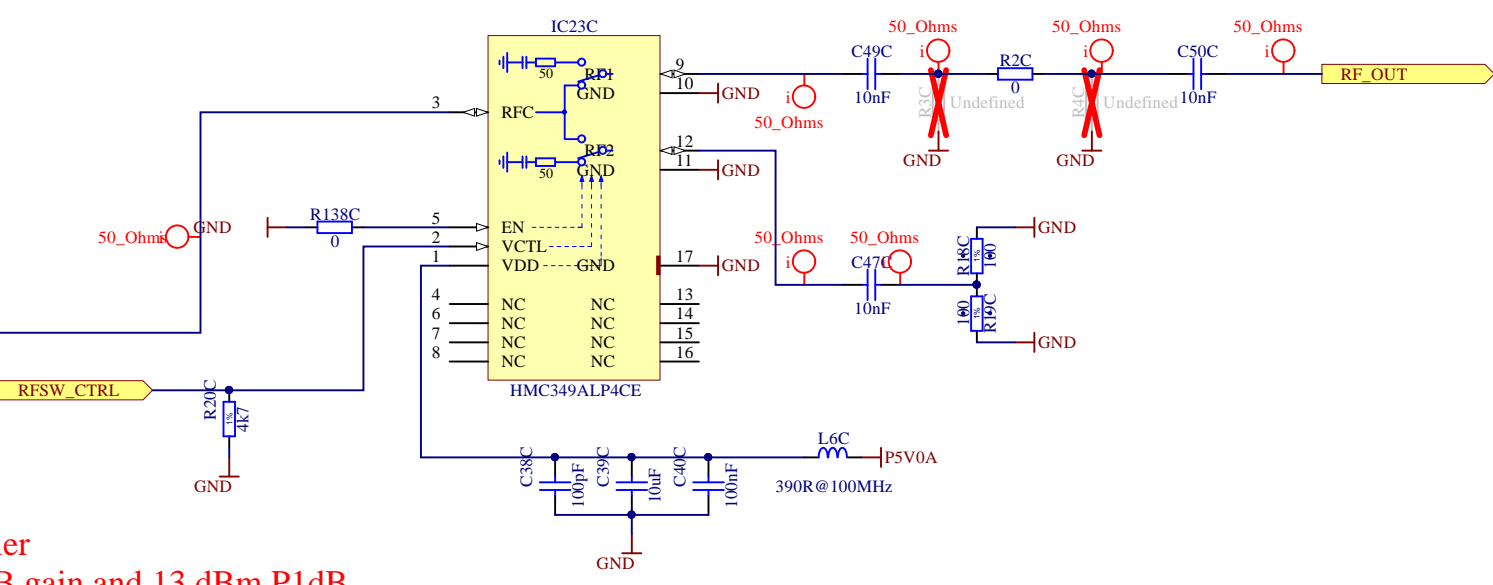
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

$R5 \text{ power} = 65\text{mA}^2 \cdot 39 = 0.16\text{W}$

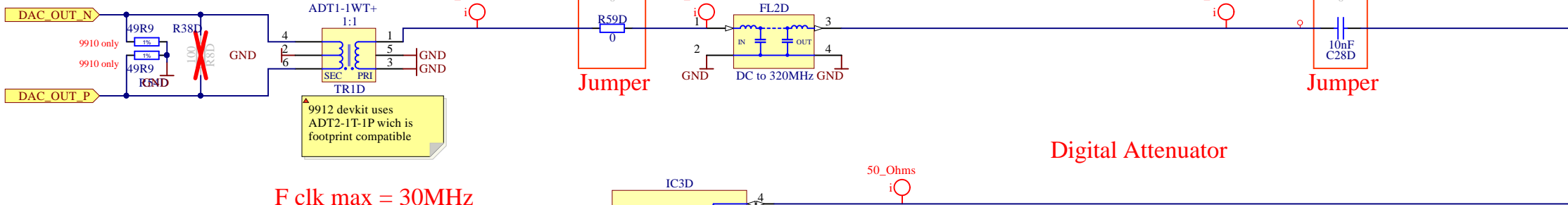
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Amplifier
~23 dB gain and 13 dBm P1dB

SPDT switch

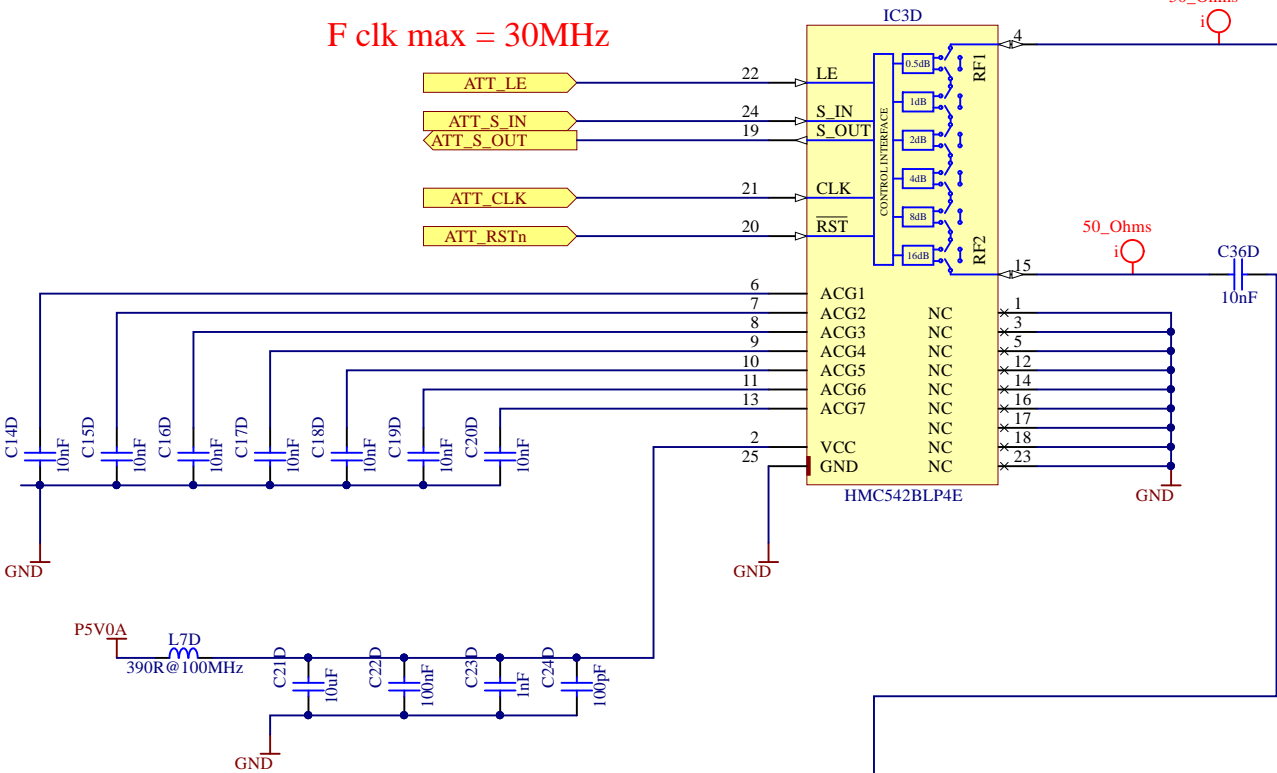


One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28) for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom Filter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder



F clk max = 30MHz

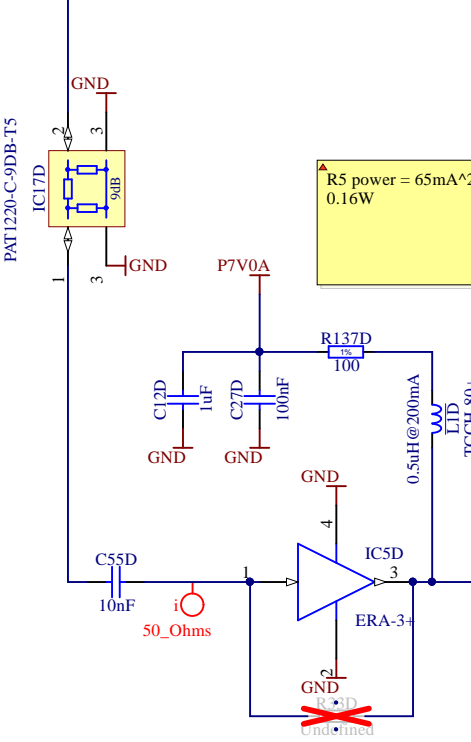
Digital Attenuator



With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

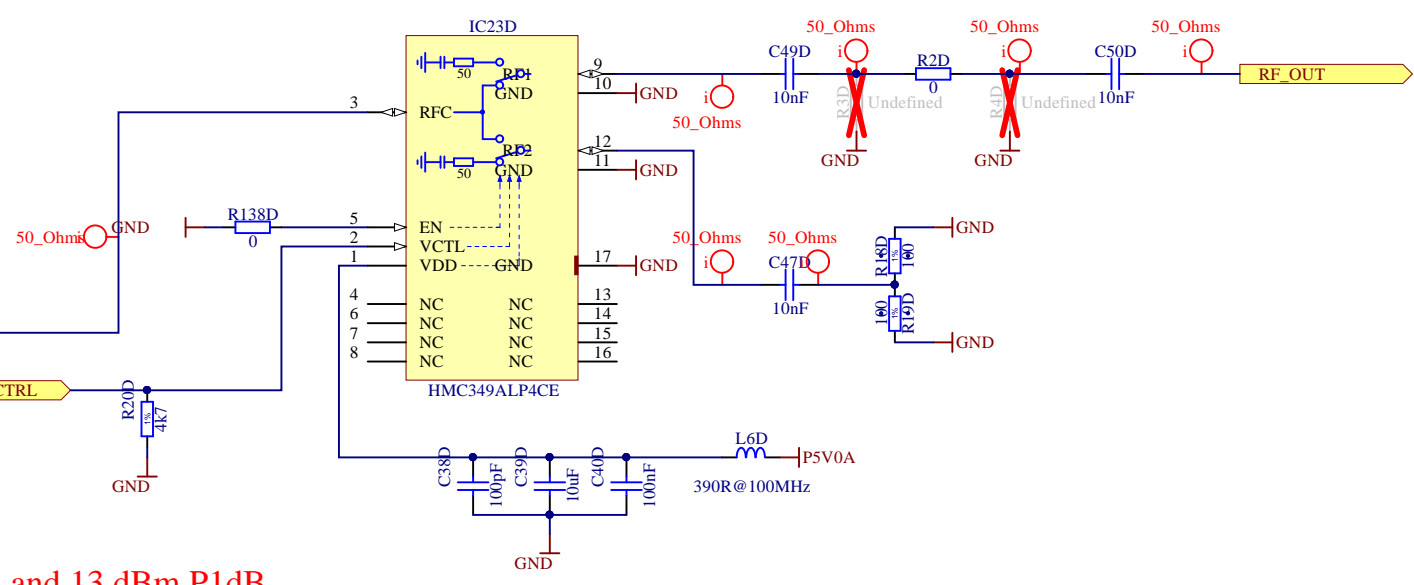
R5 power = $65\text{mA}^2 \cdot 39 = 0.16\text{W}$

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Amplifier
~23 dB gain and 13 dBm P1dB

SPDT switch



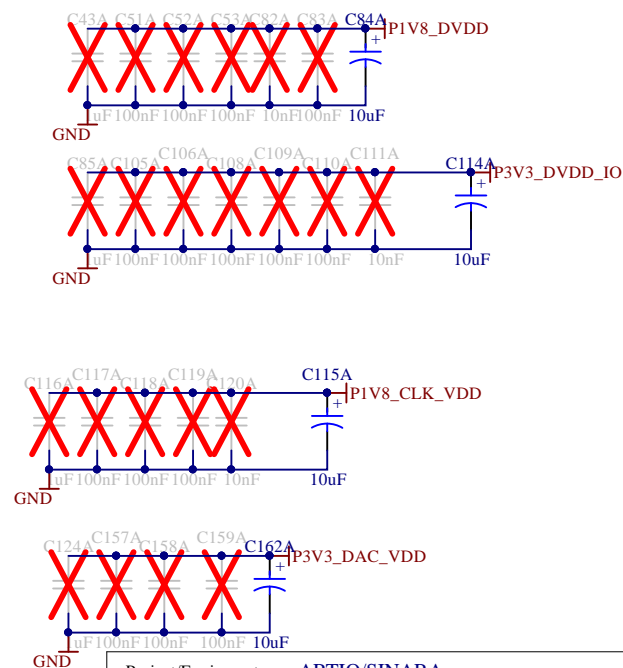
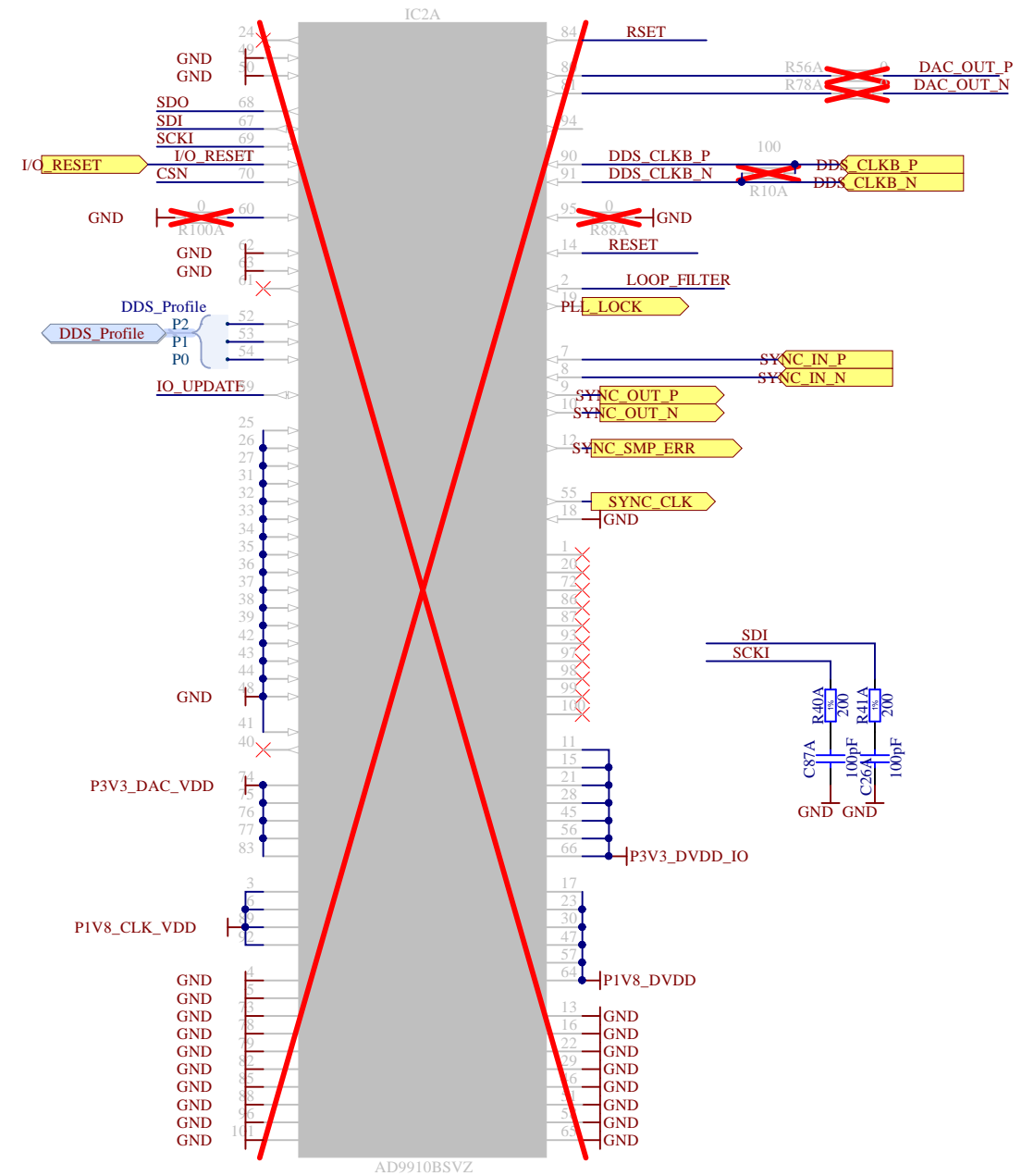
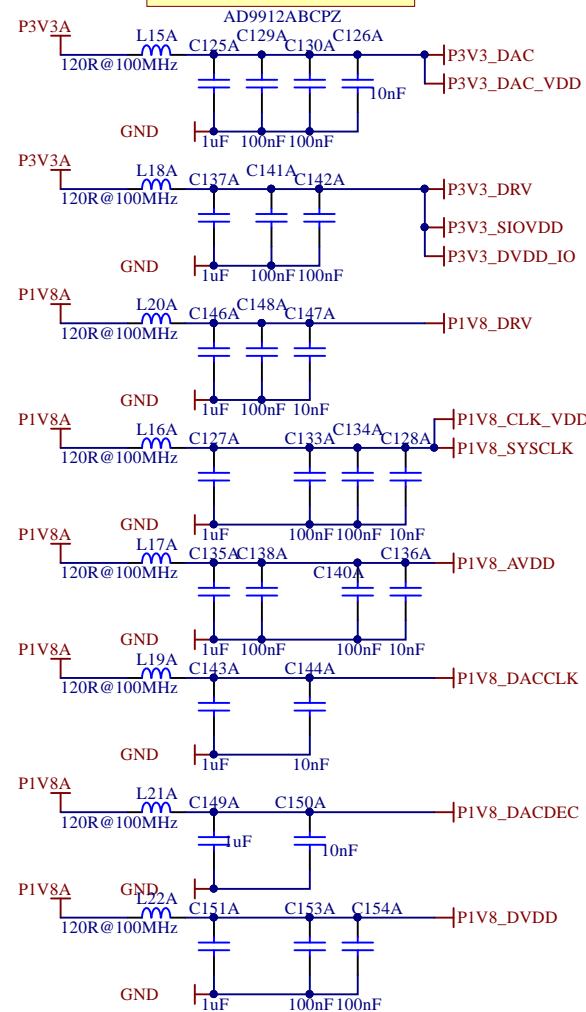
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File	DDS_OUT_channel.SchDoc	Print Date	17.09.2017 23:09:36
		Sheet	4 of 7
		Size	A3
		Rev	-

Output stage :
Attenuator, amplifier and filter

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ARTIQ

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758



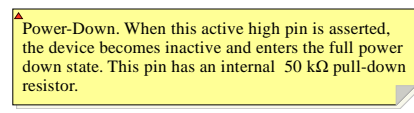
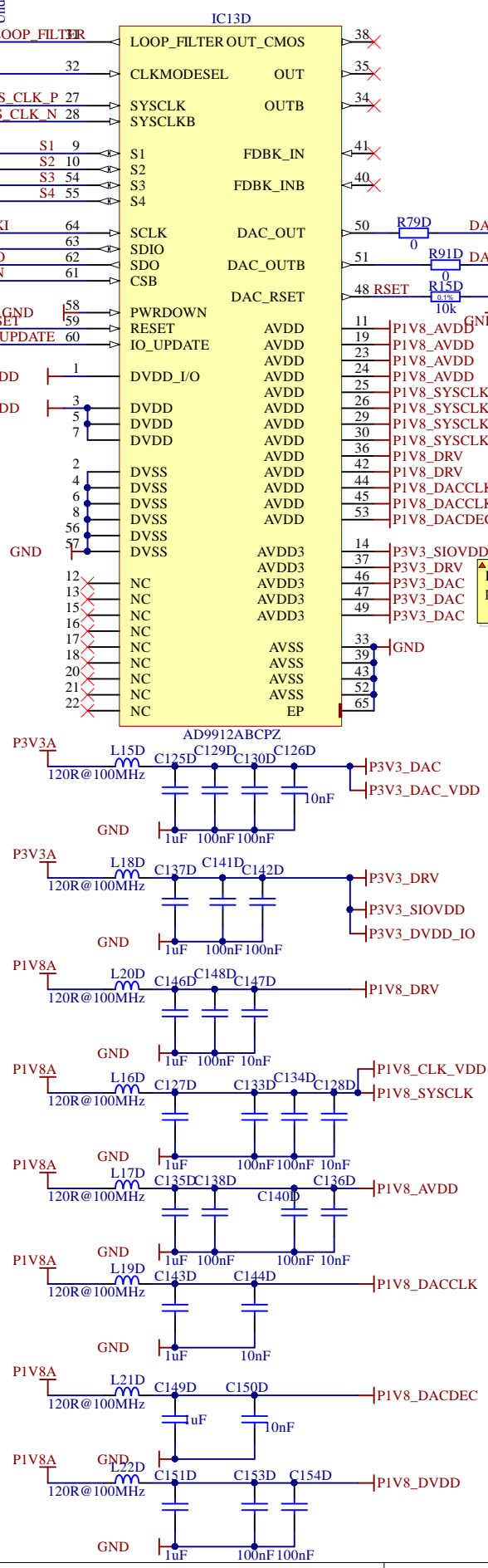


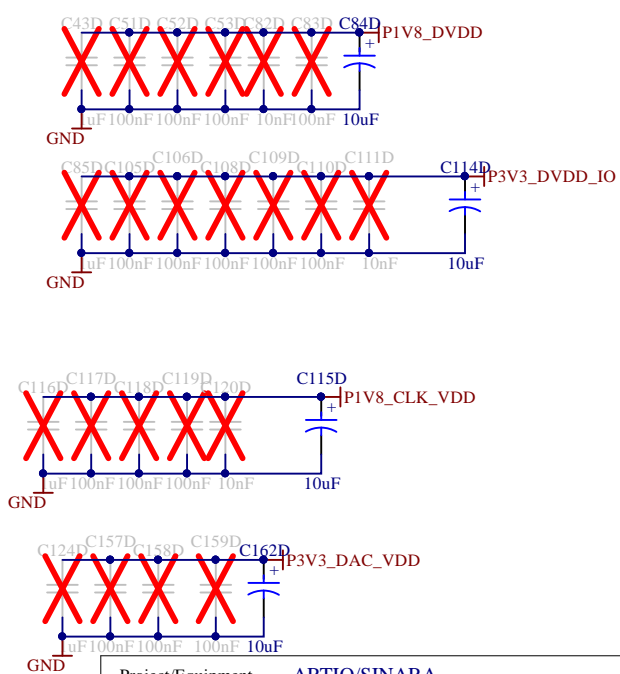
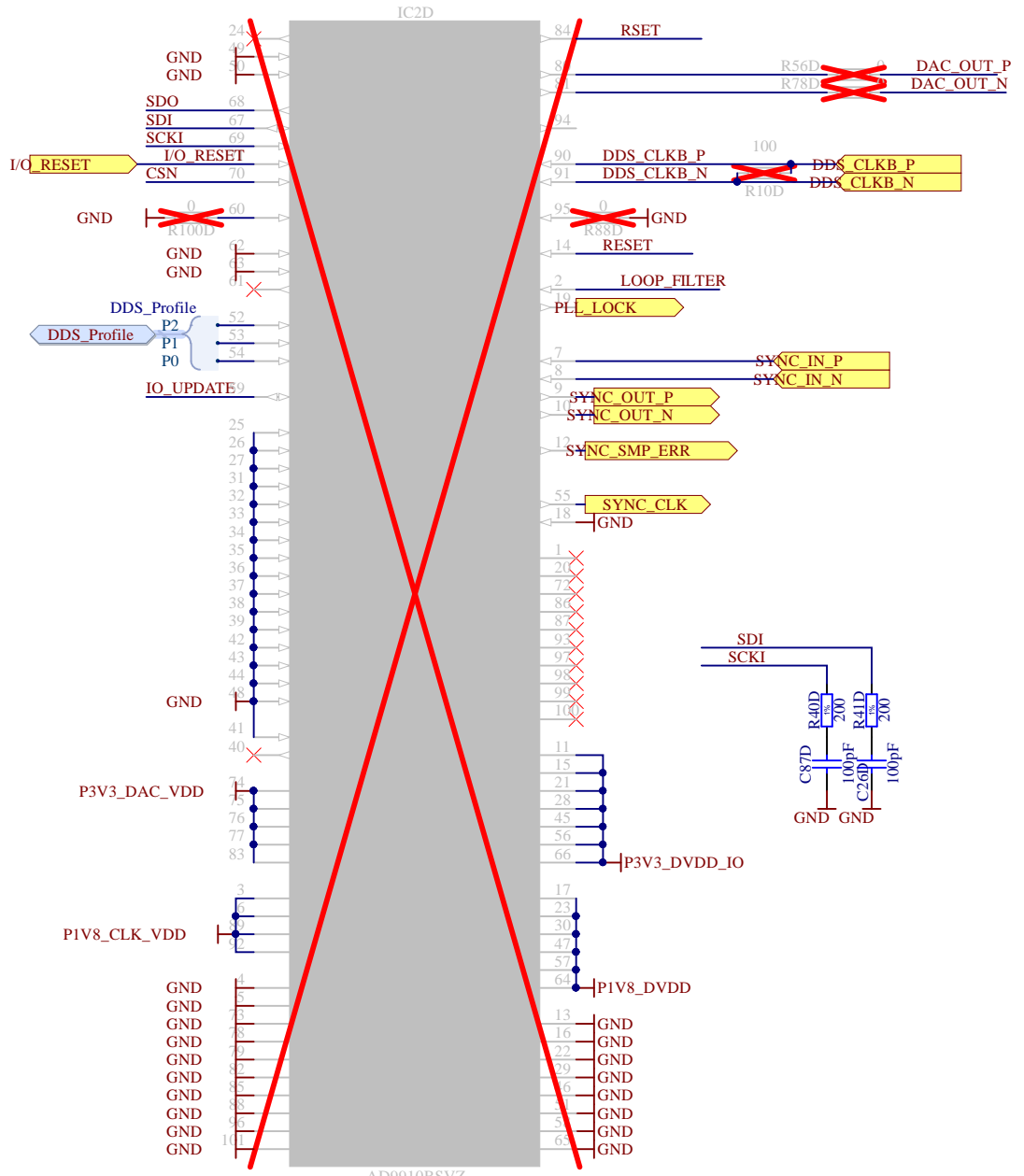
Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

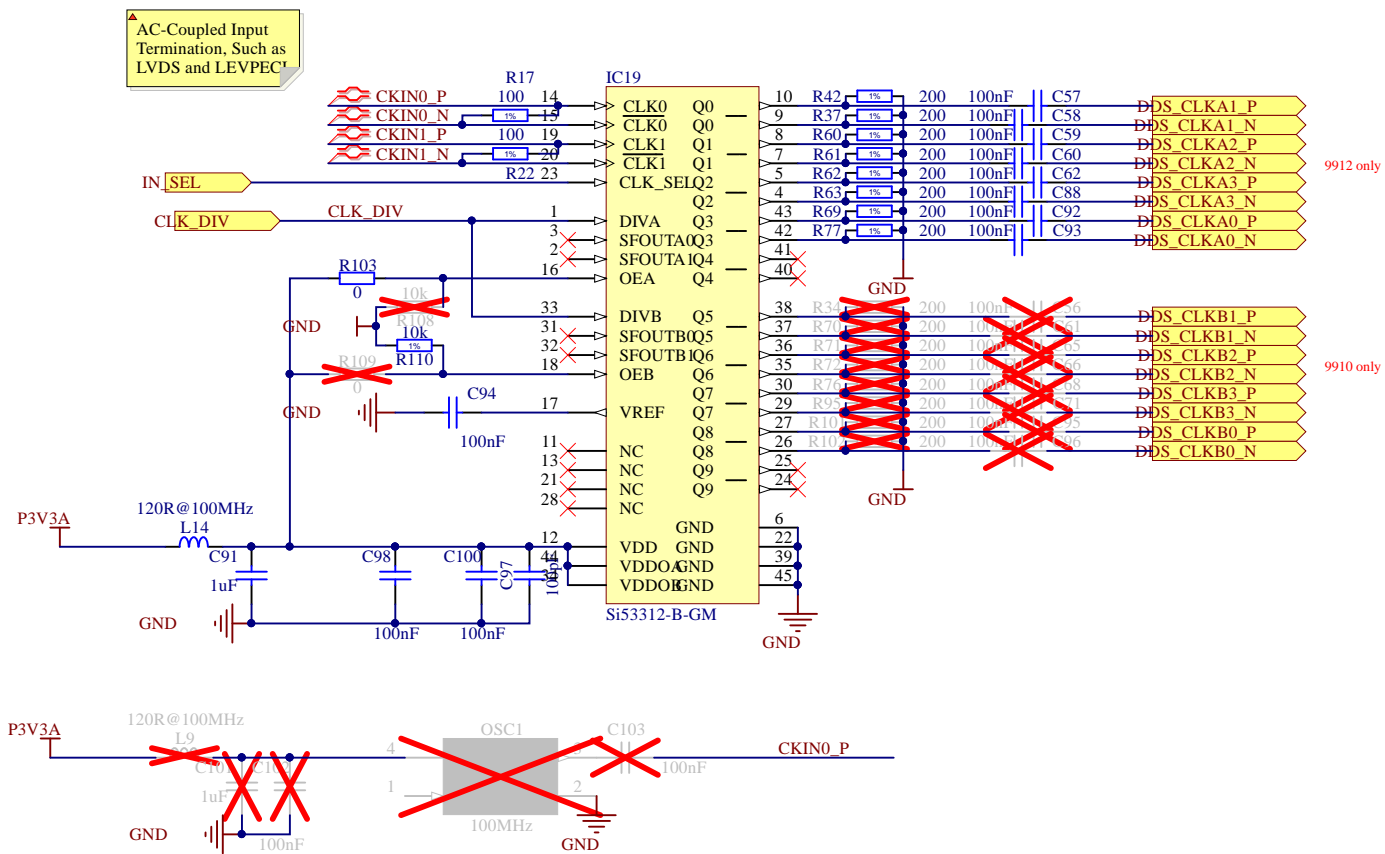
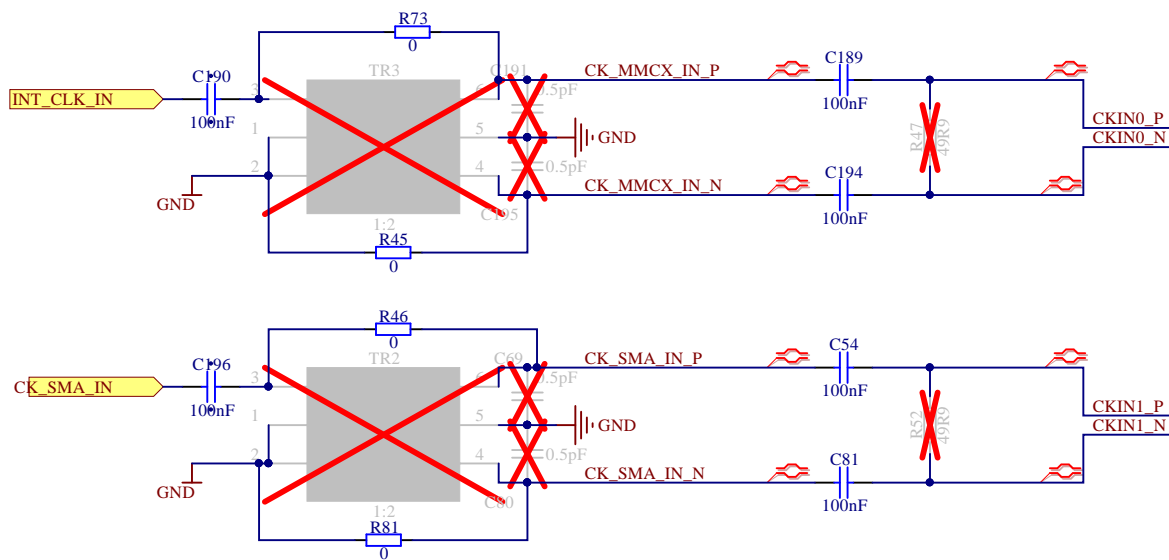
Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758



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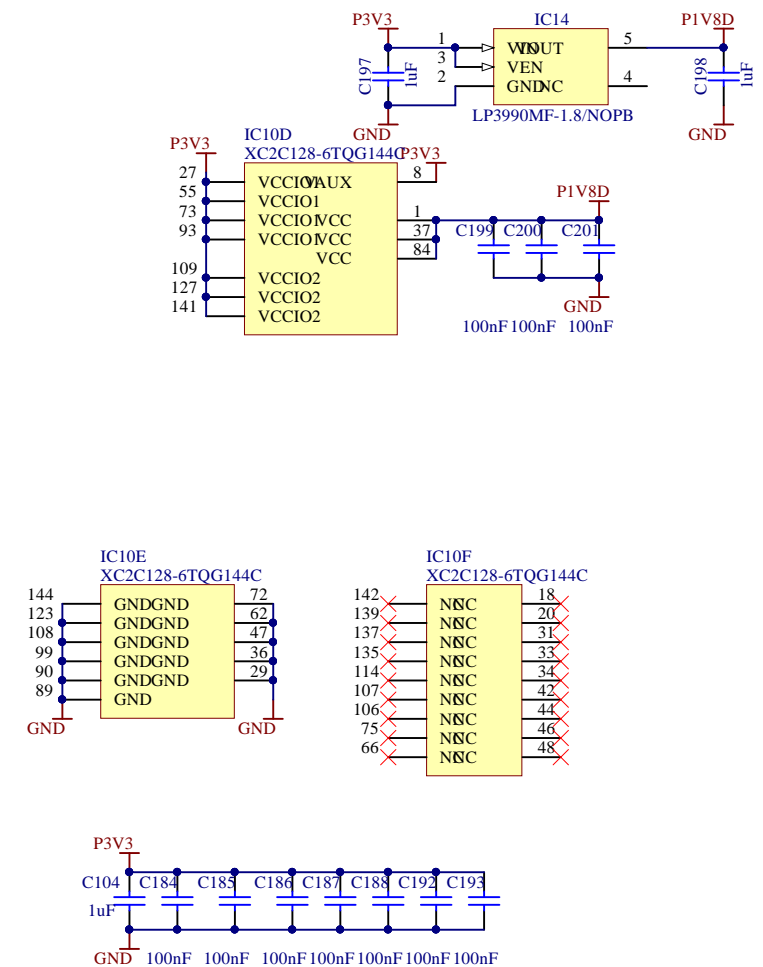
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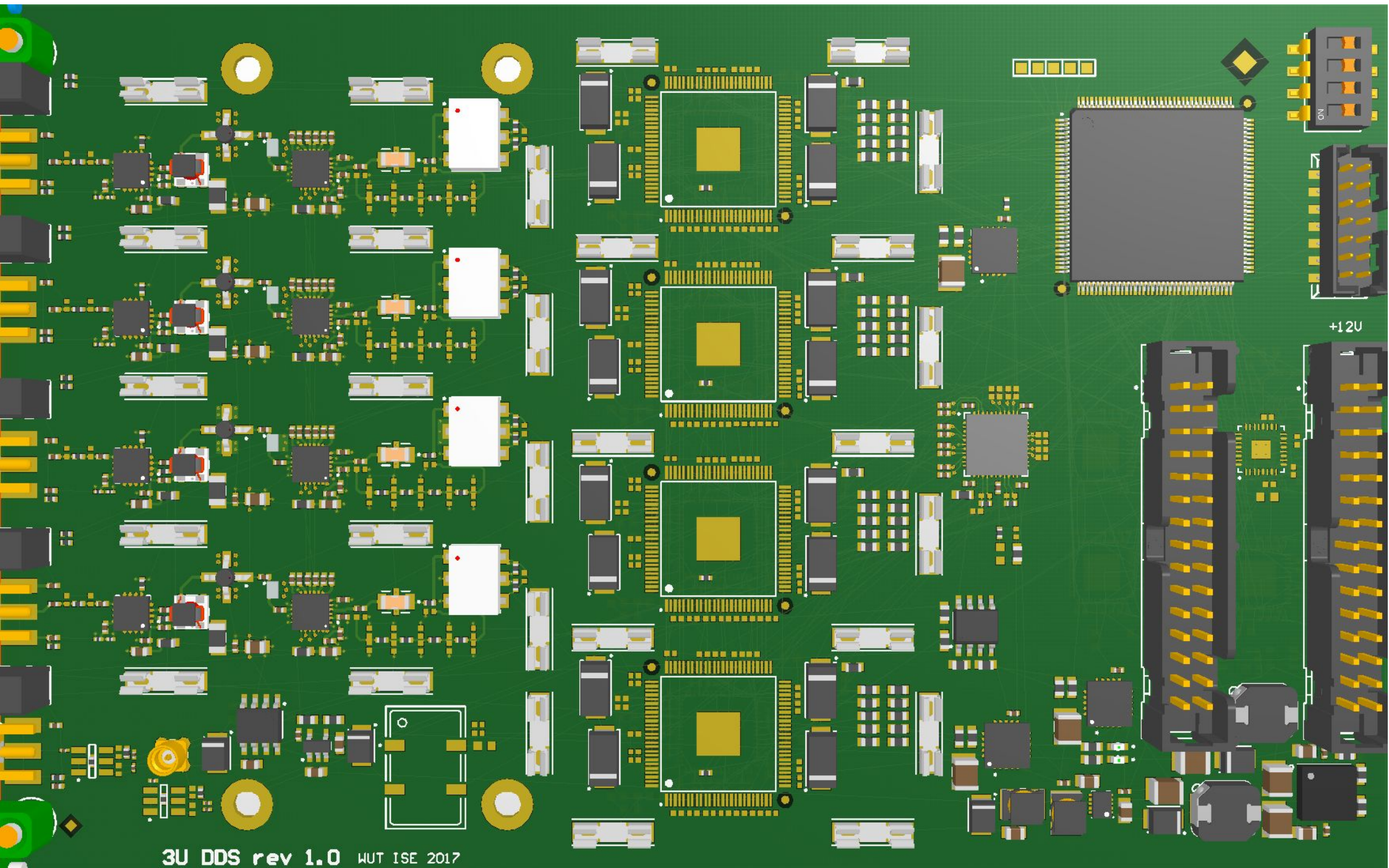




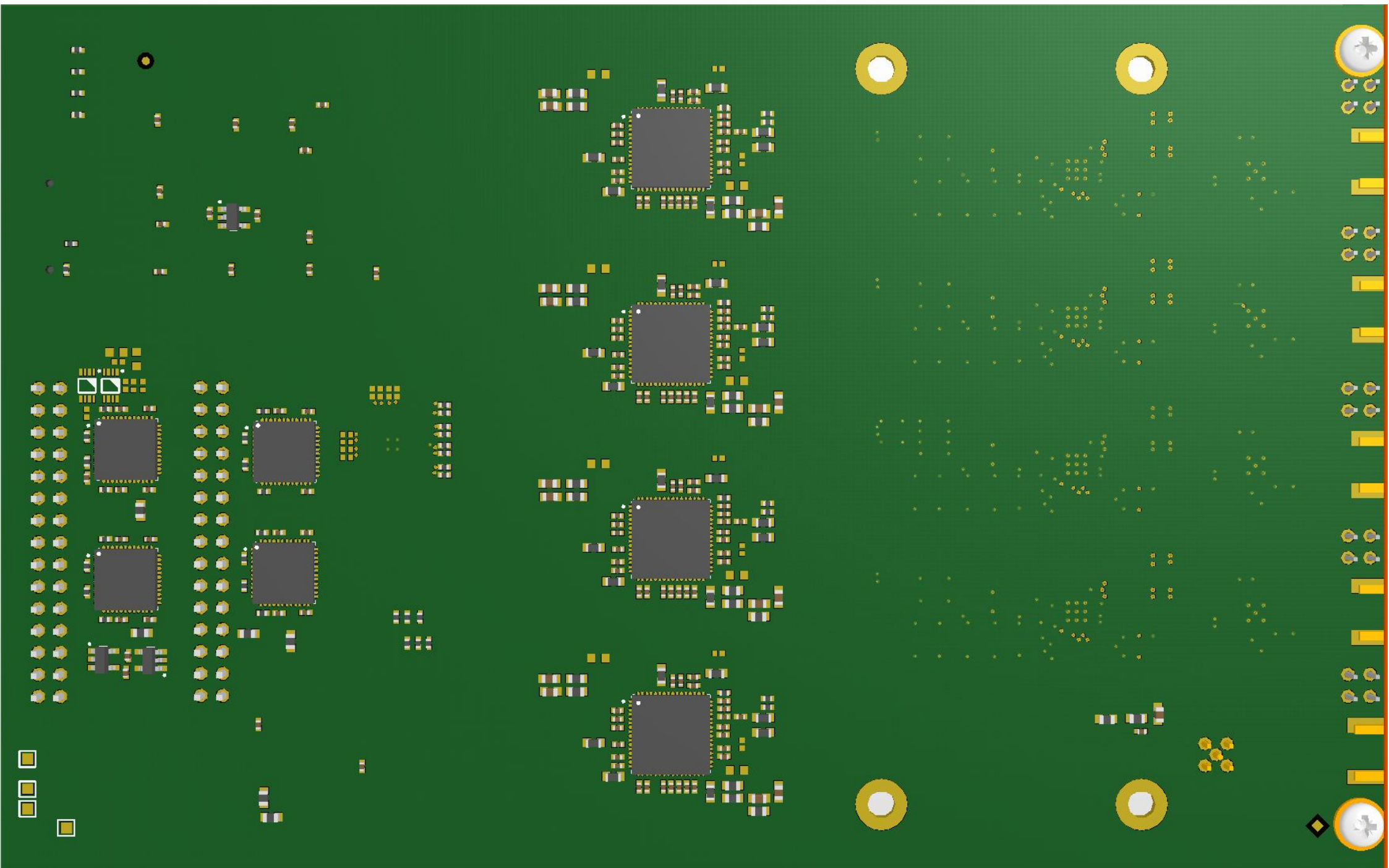
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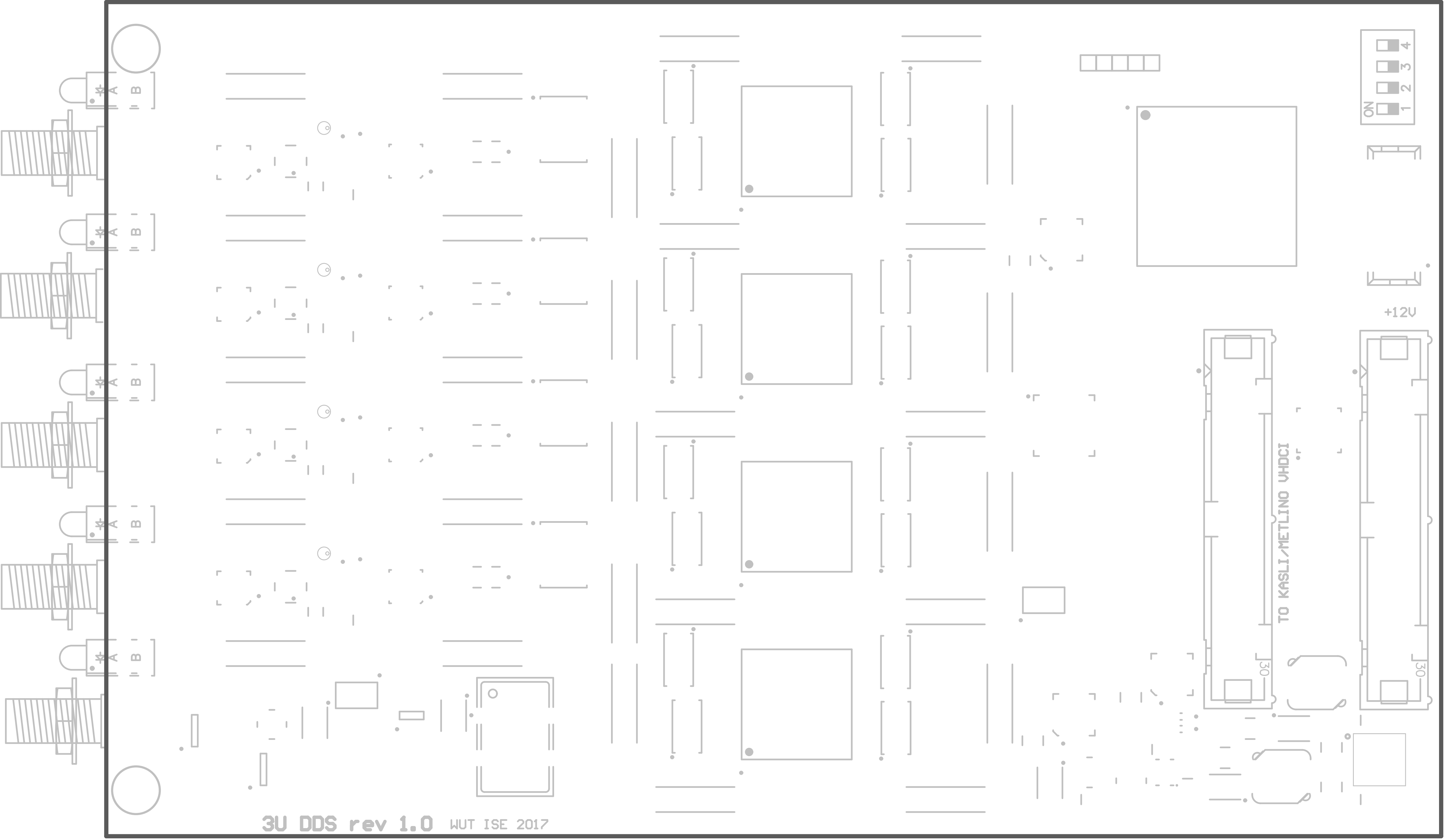
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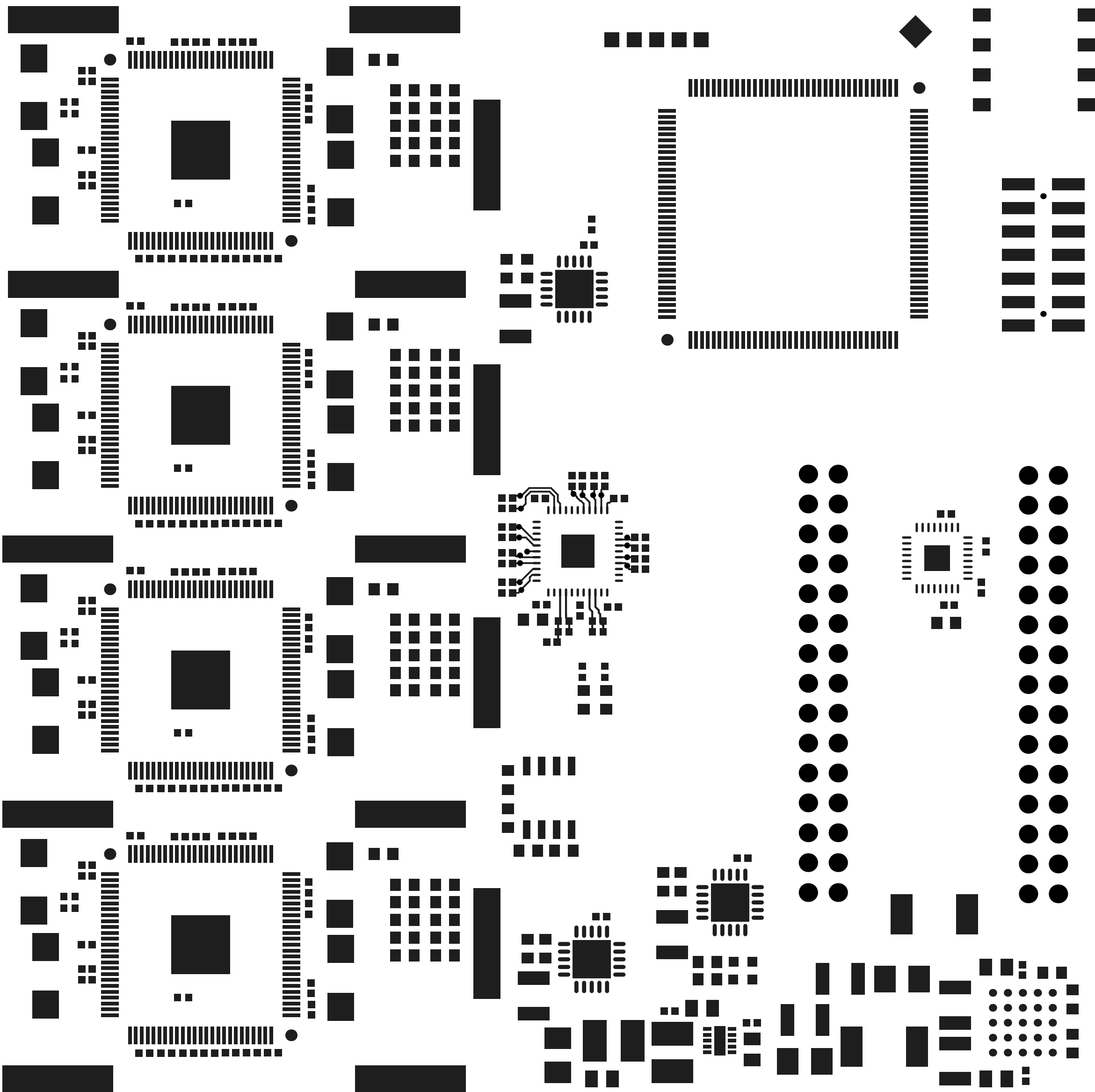
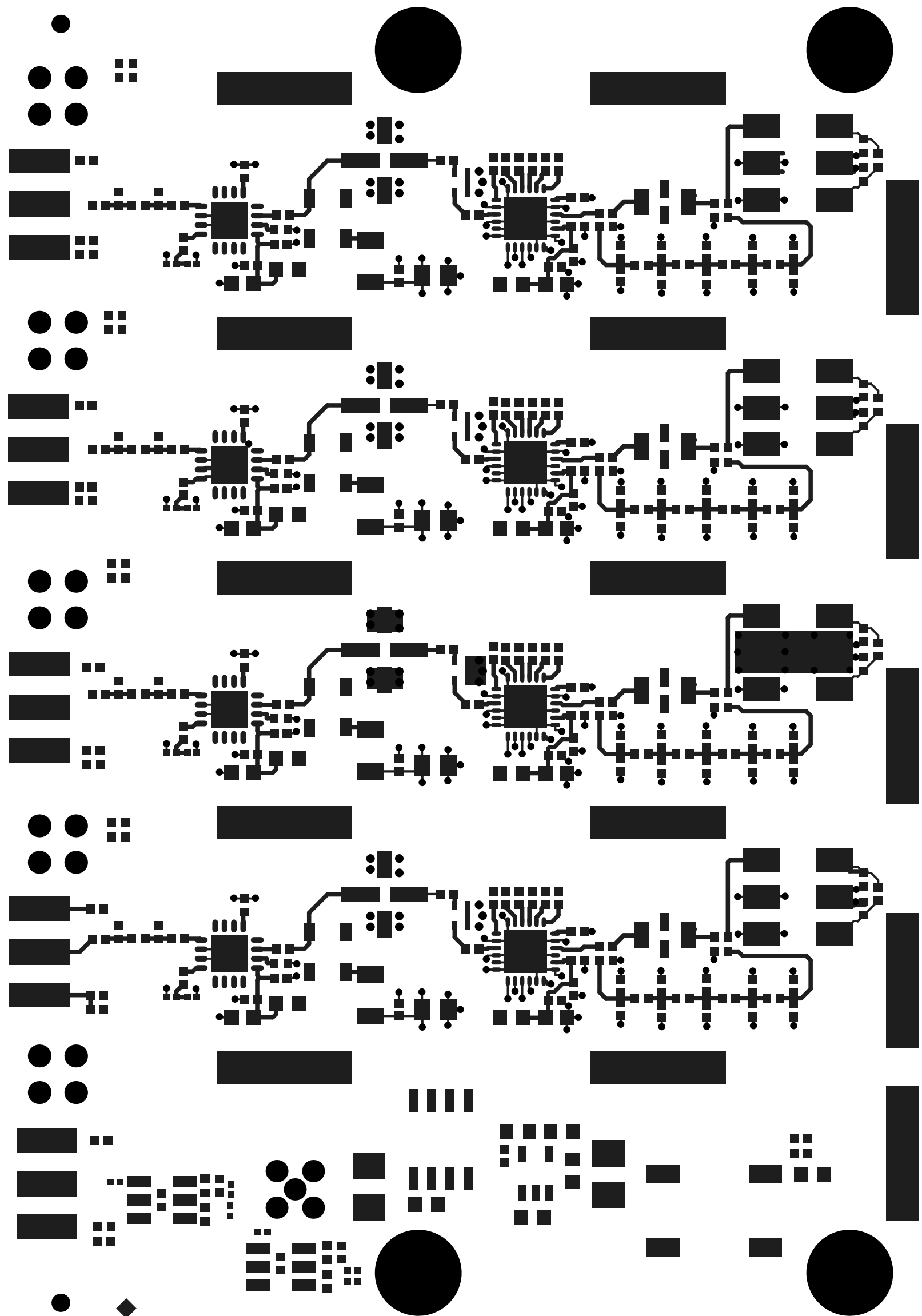




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