shield clips

CLIP1 CLIP2 CLIP3 CLIP4 CLIP5 CLIP30 CLIP31
CLIP6 CLIP7 CLIP8 CLIP9 CLIP10 CLIP27
CLIP11 CLIP12 CLIP13 CLIP14 CLIP15 CLIP28
CLIP16 CLIP17 CLIP18 CLIP19 CLIP20 CLIP29
CLIP21 CLIP22 CLIP23 CLIP24 CLIP25 CLIP26
(all 1 GND)

Ext clock input

Internal clock input

Output SMAs

SMA Insulating washers

WASHER1 D11.1xd6.6 WASHER2 D11.1xd6.6
WASHER3 D11.1xd6.6 WASHER4 D11.1xd6.6
WASHER5 D11.1xd6.6 WASHER6 D11.1xd6.6
WASHER7 D11.1xd6.6 WASHER8 D11.1xd6.6
WASHER9 D11.1xd6.6 WASHER10 D11.1xd6.6

U_CTRL_LOGIC
CTRL_LOGIC.SchDoc

RFSW_CTRL0..3, DDS_SDO[3..0], DDS_SDI[3..0], DDS_SCKI[3..0], DDS_CSn[3..0], IN_SEL, CLK_DIV, DDS_UPDATE[3..0], DDS_SYNC_CLK0, DDS_PLL_LOCK[3..0], SYNC_SMP_ERR[3..0], DDS_Profile, Master_RESET, DDS_I/O_RESET, DDS_RESET[3..0], LED[7..0], ATT_CLK, ATT_LE, ATT_RSTn, ATT_S_IN, ATT_S_OUT
RE_DE[15..0] → RE_DE[15..0]
EEM0_0..7, EEM1_0..7
DDS_SYNC_CLKSEL, DDS_SYNC_OUTEN, DDS_SYNC_CLK_OUTEN

LVDS_IFC_DDS.SchDoc U_LVDS_IFCA
EEM0..7, LVDS0_P/N, LVDS1_P/N, LVDS7_P/N
I2C_SDA, I2C_SCL → SDA, SCL
EEM 0
RE_DE0..7

LVDS_IFC_DDS.SchDoc U_LVDS_IFCB
EEM0..7, LVDS0_P/N, LVDS1_P/N, LVDS7_P/N
I2C_SDA, I2C_SCL
EEM 1
RE_DE0, RE_DE8..RE_DE15

DDS_CLK
U_CLK_INPUT
CLK_INPUT.SchDoc
CK_SMA_IN, IN_SEL, CLK_DIV, INT_CLK_IN
DDS_CLKA0..3_P/N, DDS_CLKB0..3_P/N

C37 10nF, C42 10nF, R6 0, SG0, SMA J2, 50_Ohms
J7 MMCX, 50_Ohms
C11 10nF, SG1, R64 0, C25 10nF, SMA J3, RF_OUT0, 50_Ohms
C31 10nF, SG2, R65 0, C32 10nF, SMA J4, RF_OUT1, 50_Ohms
C33 10nF, SG3, R74 0, C34 10nF, SMA J5, RF_OUT2, 50_Ohms
C35 10nF, SG4, R75 0, C41 10nF, SMA J6, RF_OUT3, 50_Ohms
ATT_S_OUT → R47 1% 470

U_DDS_OUT_channel0..3
DDS_OUT_channel.SchDoc
RF_OUT, DAC_OUT_P/N, ATT_CLK, ATT_LE, ATT_RSTn, ATT_S_IN, ATT_S_OUT, RFSW_CTRL
RFSW_CTRL0..3

U_DDS_channel0..3
DDS_channel.SchDoc
DAC_OUT_P/N, SYNC_OUT_P/N, SYNC_CLK, I/O_RESET, RESET, SYNC_IN_P/N, Master_RESET
SDO, SDI, SCKI, CSN, IO_UPDATE, PLL_LOCK, SYNC_SMP_ERR, DDS_Profile, DDS_CLKA0_P/N, DDS_CLKB0_P/N
DDS_SDO0..3, DDS_SDI0..3, DDS_SCKI0..3, DDS_CSn0..3, DDS_UPDATE0..3, DDS_PLL_LOCK0..3, SYNC_SMP_ERR0..3, DDS_CLKA1_P/N, DDS_CLKB1_P/N, DDS_CLKA2_P/N, DDS_CLKB2_P/N, DDS_CLKA3_P/N, DDS_CLKB3_P/N
DDS0_SYNC_OUT_P/N, DDS_SYNC_CLK0, DDS_I/O_RESET, DDS_RESET0, DDS0_SYNC_IN_P/N
DDS1_SYNC_OUT_P/N, DDS_SYNC_CLK1, DDS_I/O_RESET, DDS_RESET1, DDS1_SYNC_IN_P/N
DDS2_SYNC_OUT_P/N, DDS_SYNC_CLK2, DDS_I/O_RESET, DDS_RESET2, DDS2_SYNC_IN_P/N
DDS3_SYNC_OUT_P/N, DDS_SYNC_CLK3, DDS_I/O_RESET, DDS_RESET3, DDS3_SYNC_IN_P/N

DDS_SYNC_CLK0 → R31 1k 1% → P3V3_CLK2 → R32 100 1% → IC4 FIN1101K8X (EN, GND, VCC, GND)
C1 100nF, C13 100nF, R36 1k 1%, R39 1k 1%

IC9
DDS0_SYNC_OUT_P/N → R52 470 1%, R68 100 1%
CLK0, CLK0, CLK1, CLK1, CLK_SEL
Q0, Q0, Q1, Q1, Q2, Q2 → DDS0_SYNC_IN_P/N, DDS1_SYNC_IN_P/N
SFOUTA0, SFOUTA1, OE0, OE1, OE2
SFOUTB0, SFOUTB1, OE3, OE4, OE5 → DDS3_SYNC_IN_P/N, DDS2_SYNC_IN_P/N, FB_SYNC_P/N
VREF, VDD, VDDOA, VDDOB
R53 470 1%
Si53304-B-GM

IC16 FIN1101K8X
R114 100

120R@100MHz L8, C45 1uF, P3V3 → P3V3_CLK2
120R@100MHz L13, P1V8A, R150 Undefined, C86 1uF, C89 100nF, C90 100nF, P3V3_CLK1
C46 100nF, P3V3_CLK2

Trace lengths matched within each of DDS_SYNC_CLK[3:0], DDS_UDPATE[3:0], RF_SW_CTRL[3:0], IO[15:11] (RF_SW ctrl lines), DDS_SYNC_IN[3:0], DDS_RESET[3:0], DDS_CLK[3:0]

FTG1, FTG2, FTG3, FTG4

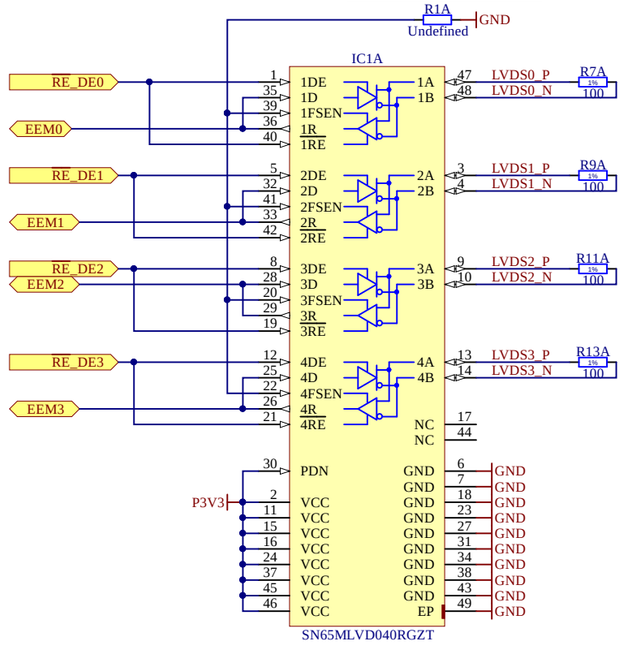
U_Supply_DDS
Supply_DDS.SchDoc
SDA, SCL

LED0..7: R27..R26 470 1%, LD5A..LD2B BOT/TOP Green/Red
DDS0 LEDs, DDS1 LEDs, DDS2 LEDs, DDS3 LEDs

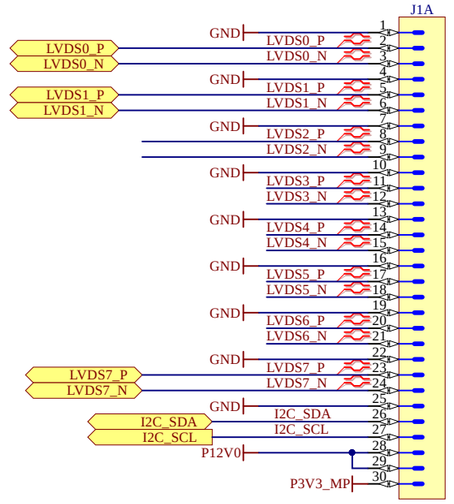
Project/Equipment	ARTIQ/SINARA
Document	3U DDS (URUKUL) v1.1 Top entity
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 11.01.2018
File	Urukul.schdoc
Print Date	11.01.2018 01:08:20 Sheet 1 of 7

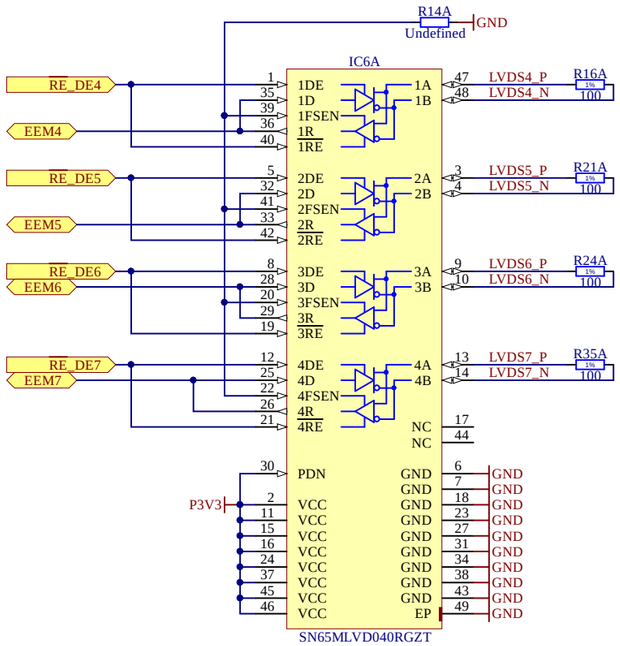
Warsaw Univeristy of Technology ISE
Nowowiejska 15/19
ARTIQ
Size A3 Rev -

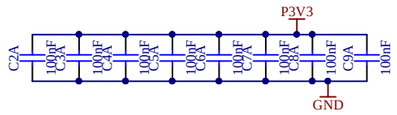
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

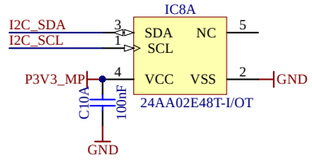


EEM Connector
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A



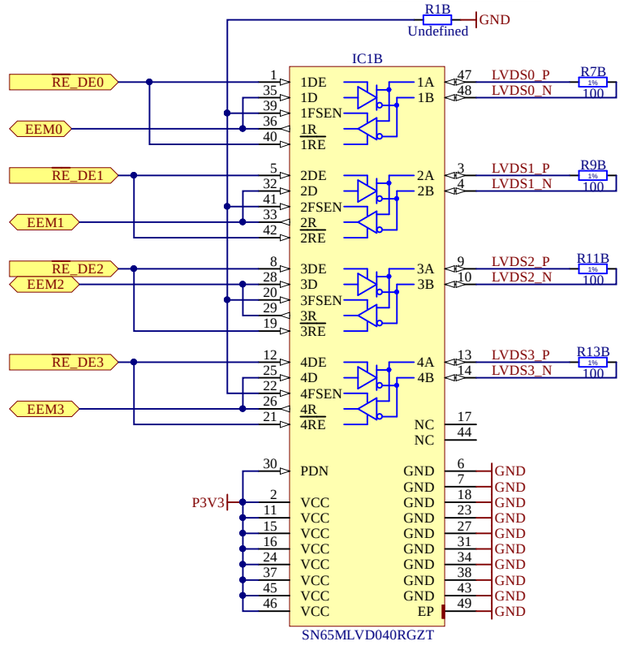




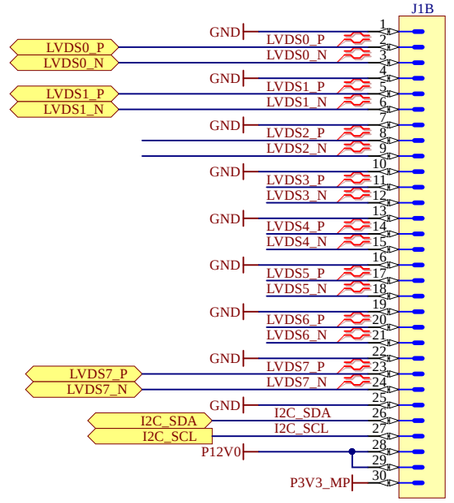


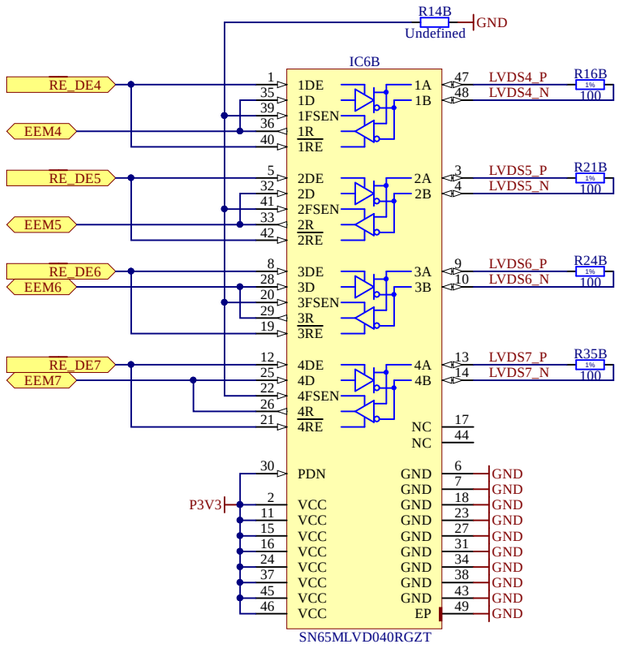
Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	11.01.2018
		File LVDS_IFC_DDS.SchDoc	
		Print Date 11.01.2018 01:08:20	Sheet 2 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	*ISE*	ARTIQ	Size A3 / Rev -

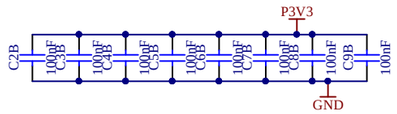
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

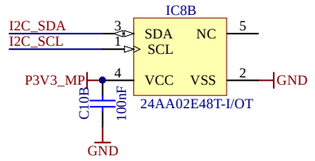


EEM Connector
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A

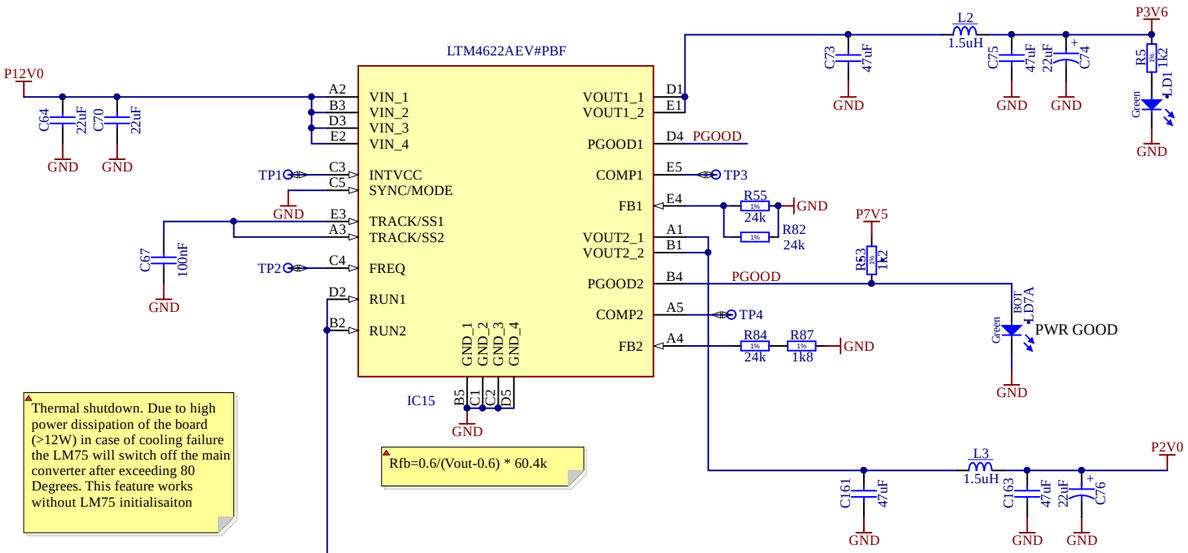


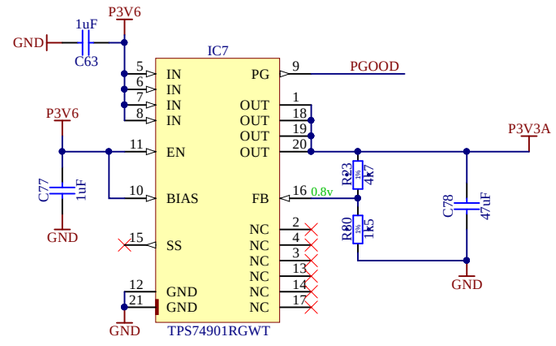


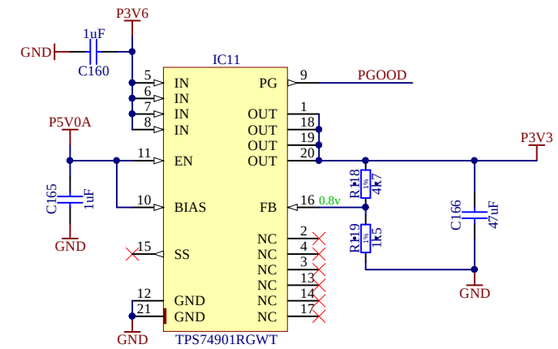


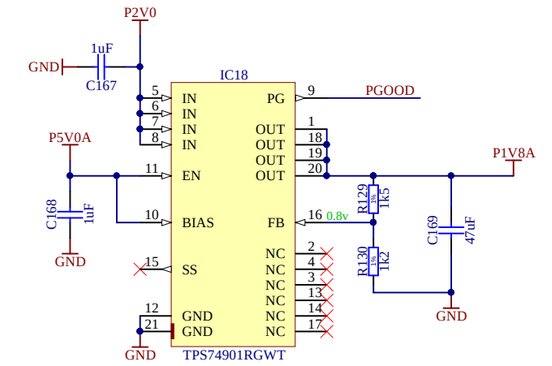


Project/Equipment	ARTIQ/SINARA		
Document	**LVDS to LVTTL interface & EEM connector**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	11.01.2018
		File LVDS_IFC_DDS.SchDoc	
		Print Date 11.01.2018 01:08:20	Sheet 2 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	*ISE*	ARTIQ	Size A3 / Rev -





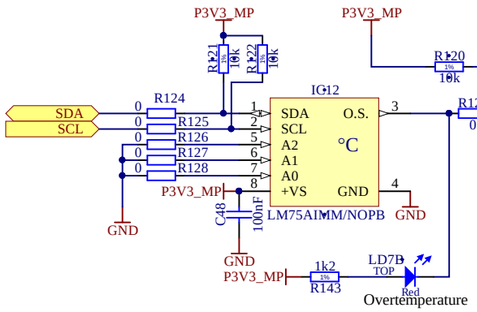


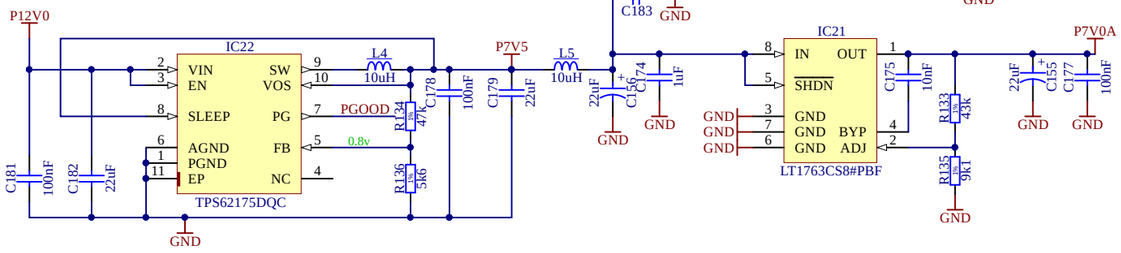


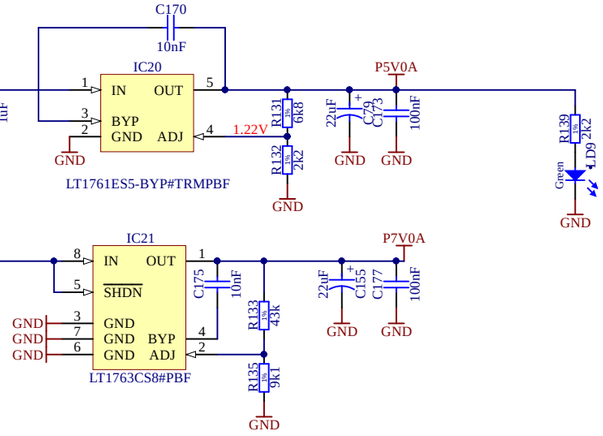
Power budget (max ratings):

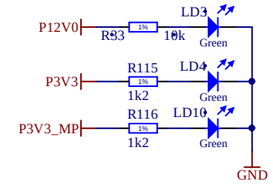
	AD9912 variant(mA)	AD9910 variant(mA)
P3V3:		
LVDS interface 4x	660	660
LVDS load 4x24mA	96	96
CPLD	100	100
Si53312-B-GM	240	240
Si53304	-	200
DDS AVDD3	4*(9,6+31)=133,6	4*29=116
DDS DVDDIO	4*3=12	4*11=44
TOTAL P3V3	1121	1346
TOTAL POWER	3.7	4.4
P1V8:		
DDS AVDD	4*(48+136)=736	4*110=440
DDS DVDD	4*246=984	4*222=888
TOTAL P1V8	1720	1328
TOTAL POWER	3,096	2.39
P5V0		
HMC542BLP4E	4*2.9=11.6	4*2.9=11.6
HMC349LP4C	4*3.5=14	4*3.5=14
TOTAL 5V0	25.6	25.6
TOTAL POWER	0,125	0,125
P7V0		
ERA-3XSM+	4*35=150	4*35=150
TOTAL POWER	1.05	1.05
DC/DC converter losses		
TPS62175 eff .95	0,05*(.27+0,026)*7,5=0.11	0,05*(.27+0,026)*7,5=0.11
LTM:3.6V eff .9	0.1*1,321*3,6=0,47	0,1*1,346*3,6=0,48
LTM:2V eff .87	0.13*1,721*2=0,44	0.13*1.328*2=0.34
LDO losses		
2V->1.8V	0.34	0,26
3.6V->3.3V	0.396	0.4
7.5V->7V	0,135	0,135
7.5V->5V	0,064	0,064
Total power from 12V	9.95W	9.45
Total current from 12V	0.83A	0.75A

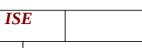
ADR: 1001 000



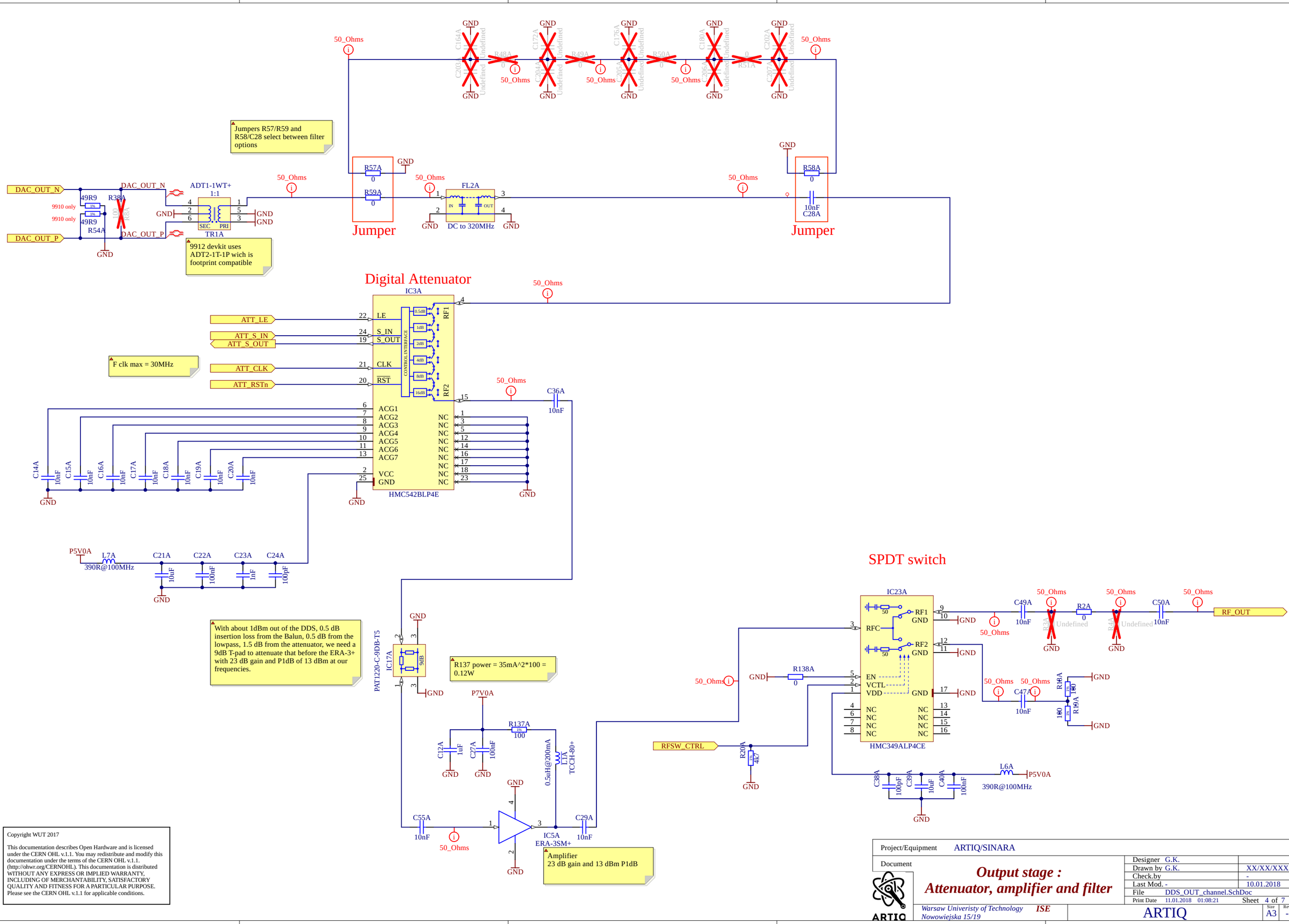








Project/Equipment	ARTIQ/SINARA		
Document	**Power supply DC/DC & LDOs**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	11.01.2018
		File Supply_DDS.SchDoc	
		Print Date 11.01.2018 01:08:21	Sheet 3 of 7
Warsaw Univeristy of Technology ISE *Nowowiejska 15/19*	ARTIQ	Size A3	Rev -


50_Ohms
GND
C164A
C203A
R48A
C172A
C204A
R49A
C176A
C205A
R50A
C180A
C206A
R51A
C202A
C207A
Undefined
Jumpers R57/R59 and R58/C28 select between filter options
R57A
R59A
R58A
10nF
C28A
Jumper
DAC_OUT_N
DAC_OUT_P
49R9
R38A
R54A
9910 only
100
R8A
ADT1-1WT+
1:1
SEC
PRI
TR1A
9912 devkit uses ADT2-1T-1P wich is footprint compatible
FL2A
IN
OUT
DC to 320MHz
Digital Attenuator
IC3A
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
F clk max = 30MHz
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB
1dB
2dB
4dB
8dB
16dB
RF1
RF2
ACG1
ACG2
ACG3
ACG4
ACG5
ACG6
ACG7
NC
VCC
HMC542BLP4E
C14A
C15A
C16A
C17A
C18A
C19A
C20A
C36A
P5V0A
L7A
390R@100MHz
C21A
C22A
C23A
C24A
10uF
100nF
1nF
100pF
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.
PAT1220-C-9DB-T5
IC17A
9dB
R137 power = 35mA^2*100 = 0.12W
P7V0A
R137A
C12A
C27A
0.5uH@200mA
L1A
TCCH-80+
C55A
C29A
IC5A
ERA-3SM+
Amplifier
23 dB gain and 13 dBm P1dB
SPDT switch
IC23A
RF1
RF2
RFC
EN
VCTL
VDD
HMC349ALP4CE
RF_OUT
C49A
C50A
R2A
C47A
R138A
R20A
RFSW_CTRL
C38A
C39A
C40A
L6A
390R@100MHz
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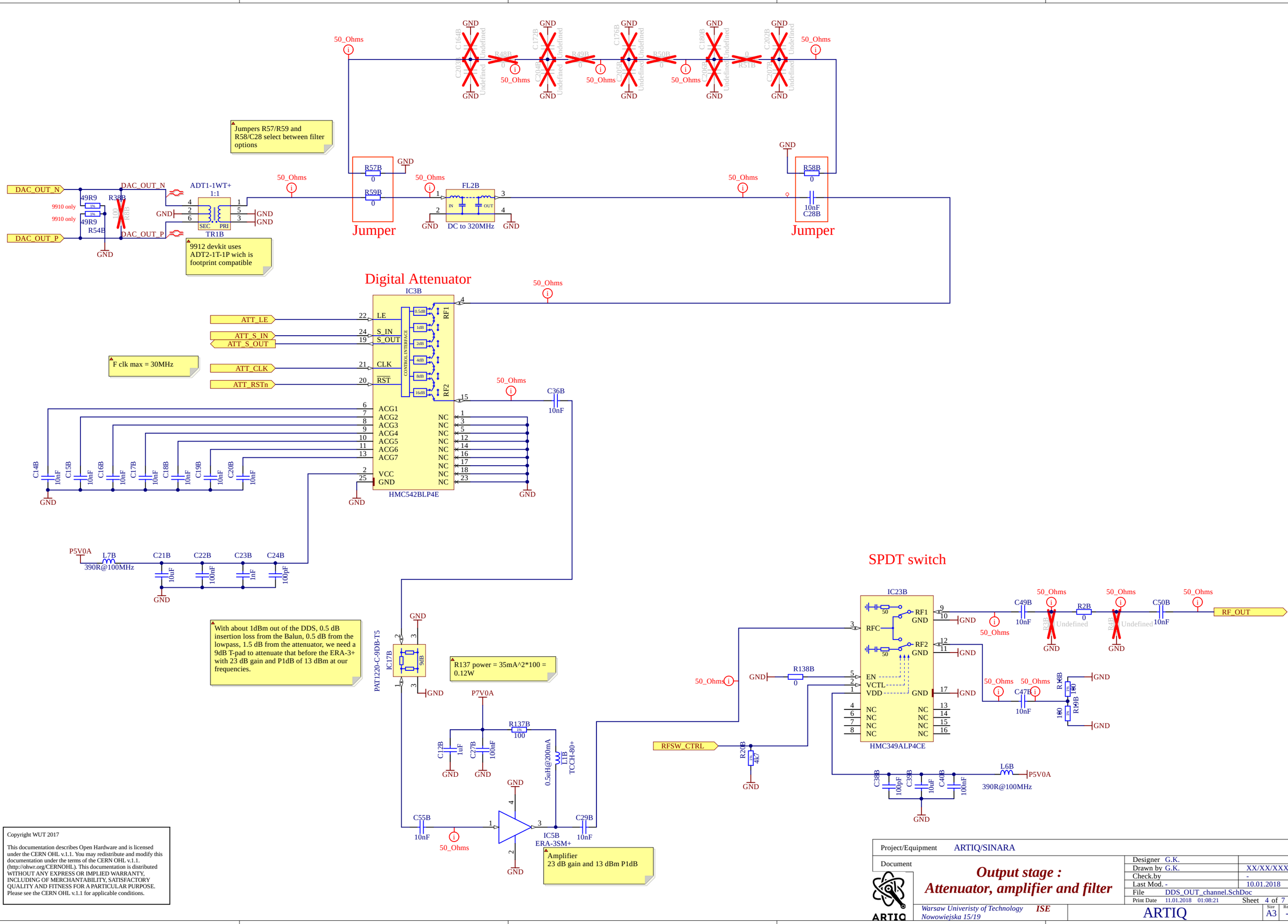
Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter
Designer G.K.
Drawn by G.K. XX/XX/XXXX
Check.by -
Last Mod. - 10.01.2018
File DDS_OUT_channel.SchDoc
Print Date 11.01.2018 01:08:21 Sheet 4 of 7
Warsaw Univeristy of Technology ISE
Nowowiejska 15/19
ARTIQ
Size A3
Rev -


50_Ohms
GND
C164B
C172B
C176B
C180B
C202B
R48B
R49B
R50B
R51B
C203B
C204B
C205B
C206B
C207B
Undefined
Jumpers R57/R59 and R58/C28 select between filter options
R57B
R59B
R58B
Jumper
Jumper
10nF
C28B
DAC_OUT_N
DAC_OUT_P
49R9
R54B
R38B
R88B
9910 only
ADT1-1WT+
1:1
TR1B
SEC
PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible
FL2B
IN
OUT
DC to 320MHz
Digital Attenuator
IC3B
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
F clk max = 30MHz
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB
1dB
2dB
4dB
8dB
16dB
RF1
RF2
ACG1
ACG2
ACG3
ACG4
ACG5
ACG6
ACG7
VCC
NC
HMC542BLP4E
C14B
C15B
C16B
C17B
C18B
C19B
C20B
C36B
10nF
P5V0A
L7B
390R@100MHz
C21B
C22B
C23B
C24B
1uF
100nF
1nF
100pF
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.
PAT1220-C-9DB-T5
IC17B
9dB
R137 power = 35mA^2*100 = 0.12W
P7V0A
R137B
100
C12B
C27B
0.5uH@200mA
L1B
TCCH-80+
C55B
C29B
IC5B
ERA-3SM+
Amplifier
23 dB gain and 13 dBm P1dB
SPDT switch
IC23B
RF1
RF2
RFC
EN
VCTL
VDD
HMC349ALP4CE
R138B
RFSW_CTRL
R20B
4k7
C49B
C50B
R2B
R3B
R4B
RF_OUT
C47B
C38B
C39B
C40B
L6B
390R@100MHz
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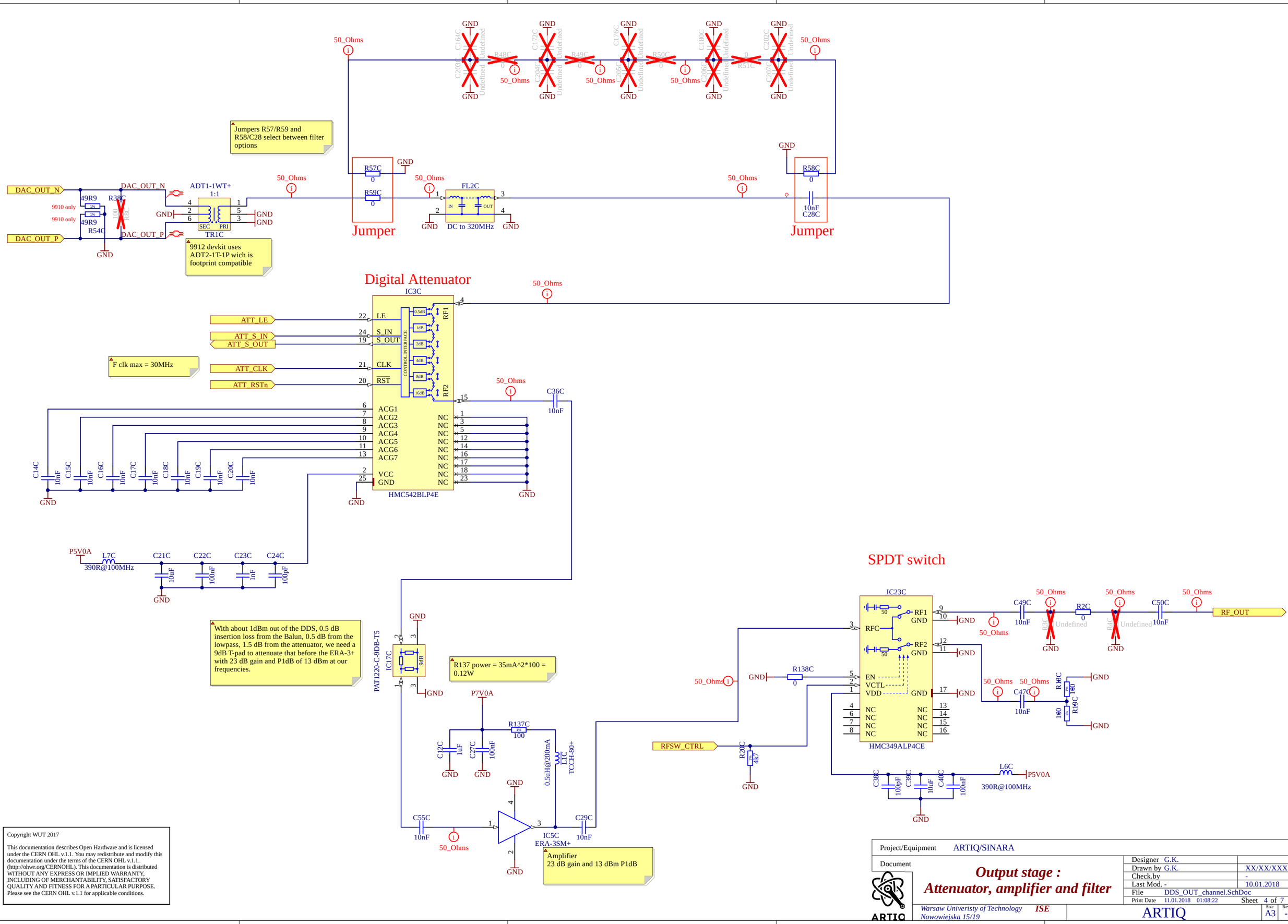
Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter
Designer G.K.
Drawn by G.K.
XX/XX/XXXX
Check.by -
Last Mod. -
10.01.2018
File DDS_OUT_channel.SchDoc
Print Date 11.01.2018 01:08:21
Sheet 4 of 7
Warsaw Univeristy of Technology
Nowowiejska 15/19
ISE
ARTIQ
Size A3
Rev -


50_Ohms
GND
C164C
C203C
R48C
C172C
C204C
R49C
C176C
C205C
R50C
C180C
C206C
R51C
C202C
C207C
Undefined
Jumpers R57/R59 and R58/C28 select between filter options
R57C
R59C
R58C
Jumper
Jumper
DAC_OUT_N
DAC_OUT_P
49R9
R54C
R38C
100
R39C
9910 only
ADT1-1WT+
1:1
TR1C
SEC
PRI
9912 devkit uses ADT2-1T-1P wich is footprint compatible
FL2C
DC to 320MHz
10nF
C28C
Digital Attenuator
IC3C
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
F clk max = 30MHz
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
0.5dB
1dB
2dB
4dB
8dB
16dB
RF1
RF2
ACG1
ACG2
ACG3
ACG4
ACG5
ACG6
ACG7
VCC
NC
HMC542BLP4E
C36C
10nF
C14C
C15C
C16C
C17C
C18C
C19C
C20C
P5V0A
L7C
390R@100MHz
C21C
C22C
C23C
C24C
10uF
100nF
1nF
100pF
With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.
PAT1220-C-9DB-T5
IC17C
9dB
R137 power = 35mA^2*100 = 0.12W
P7V0A
R137C
100
C12C
1uF
C27C
100nF
0.5uH@200mA
L1C
TCCH-80+
C55C
10nF
IC5C
ERA-3SM+
C29C
10nF
Amplifier
23 dB gain and 13 dBm P1dB
SPDT switch
IC23C
RF1
RF2
RFC
EN
VCTL
VDD
HMC349ALP4CE
R138C
RFSW_CTRL
R20C
4k7
C49C
R2C
C50C
RF_OUT
C47C
R46C
R45C
C38C
100pF
C39C
10uF
C40C
L6C
390R@100MHz
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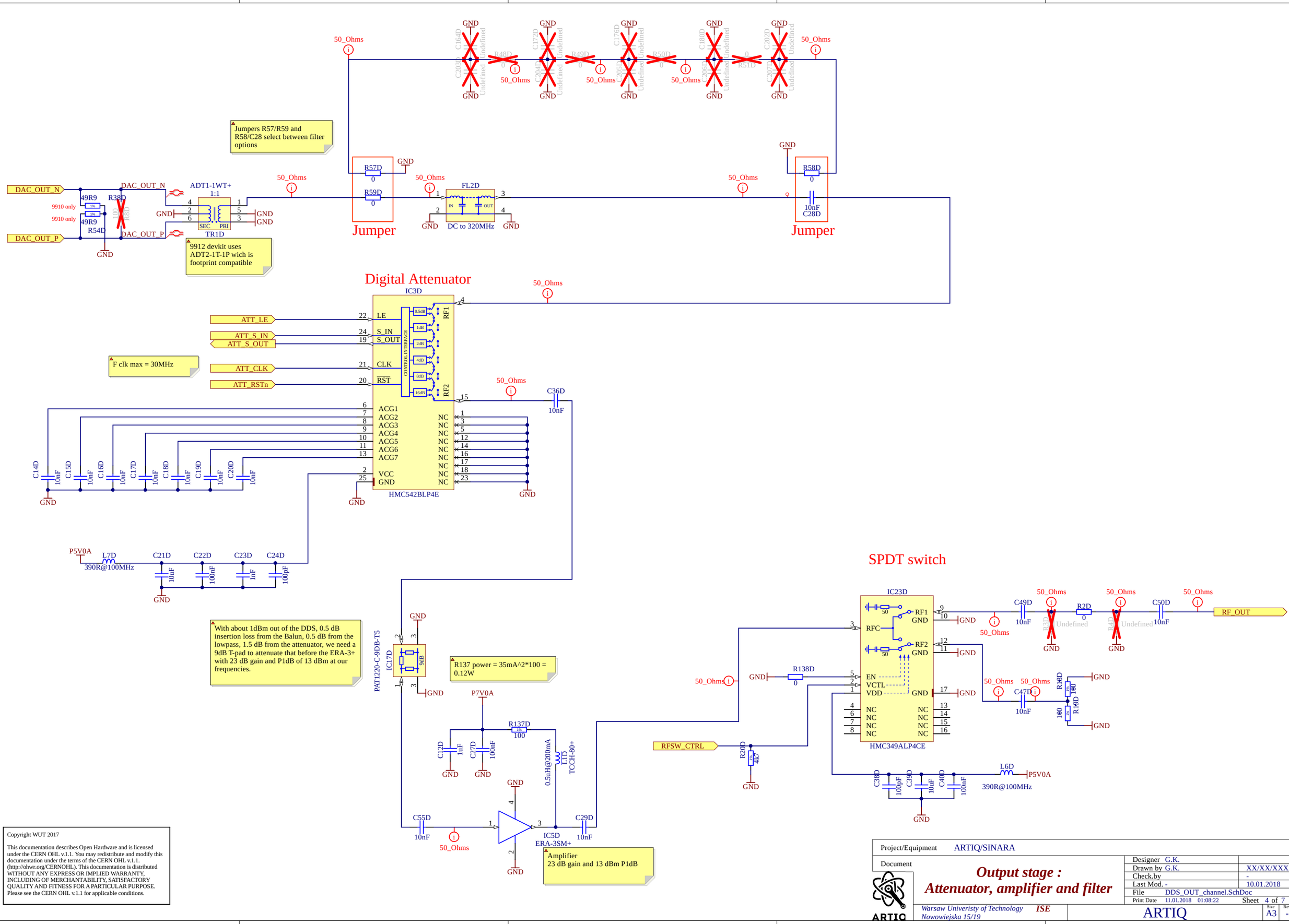
Project/Equipment ARTIQ/SINARA
Document
Output stage : Attenuator, amplifier and filter
Designer G.K.
Drawn by G.K. XX/XX/XXXX
Check.by -
Last Mod. - 10.01.2018
File DDS_OUT_channel.SchDoc
Print Date 11.01.2018 01:08:22 Sheet 4 of 7
Warsaw Univeristy of Technology ISE
Nowowiejska 15/19
ARTIQ
Size A3 Rev -



Project/Equipment	ARTIQ/SINARA		
Document	**Output stage : Attenuator, amplifier and filter**	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	10.01.2018
		File DDS_OUT_channel.SchDoc	
		Print Date 11.01.2018 01:08:22	Sheet 4 of 7
Warsaw Univeristy of Technology ISE Nowowiejska 15/19	ARTIQ	Size A3	Rev -

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

separate RSET and loop filter components due to layout constraints

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Loop filter calculation:
Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

Loop filter calculation:
Reference input frequency : 31.25MHz
PFD : 31.25MHz
multiplication factor:32
system clock frequency : 1GHz
desired phase margin: 45deg
Open loop BW: 3MHz

separate RSET and loop filter components due to layout constraints

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Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 11.12.2017
File	DDS_channel.SchDoc
Print Date	11.01.2018 01:08:22 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

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Reference input frequency : 50MHz
PFD : 50MHz
multiplication factor: 20
system clock frequency : 1GHz
desired phase margin: 65deg
Open loop BW: 1.6MHz

Clock must be AC coupled

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

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IC13B
AD9912ABCPZ

IC2B
AD9910BSVZ

Loop filter calculation:
Reference input frequency : 31.25MHz
PFD : 31.25MHz
multiplication factor:32
system clock frequency : 1GHz
desired phase margin: 45deg
Open loop BW: 3MHz

separate RSET and loop filter components due to layout constraints

Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 11.12.2017
File	DDS_channel.SchDoc
Print Date	11.01.2018 01:08:23 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

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IC13C
AD9912ABCPZ

IC2C
AD9910BSVZ

Loop filter calculation:
Reference input frequency : 31.25MHz
PFD : 31.25MHz
multiplication factor:32
system clock frequency : 1GHz
desired phase margin: 45deg
Open loop BW: 3MHz

separate RSET and loop filter components due to layout constraints

Project/Equipment	ARTIQ/SINARA		
Document	9910 & 9912 DDS	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	11.12.2017
		File DDS_channel.SchDoc	
		Print Date 11.01.2018 01:08:24	Sheet 5 of 7
Warsaw Univeristy of Technology ISE Nowowiejska 15/19	ARTIQ	Size A3	Rev -

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

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System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

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multiplication factor: 20
system clock frequency : 1GHz
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Open loop BW: 1.6MHz

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Loop filter calculation:
Reference input frequency : 31.25MHz
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multiplication factor:32
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Open loop BW: 3MHz

separate RSET and loop filter components due to layout constraints

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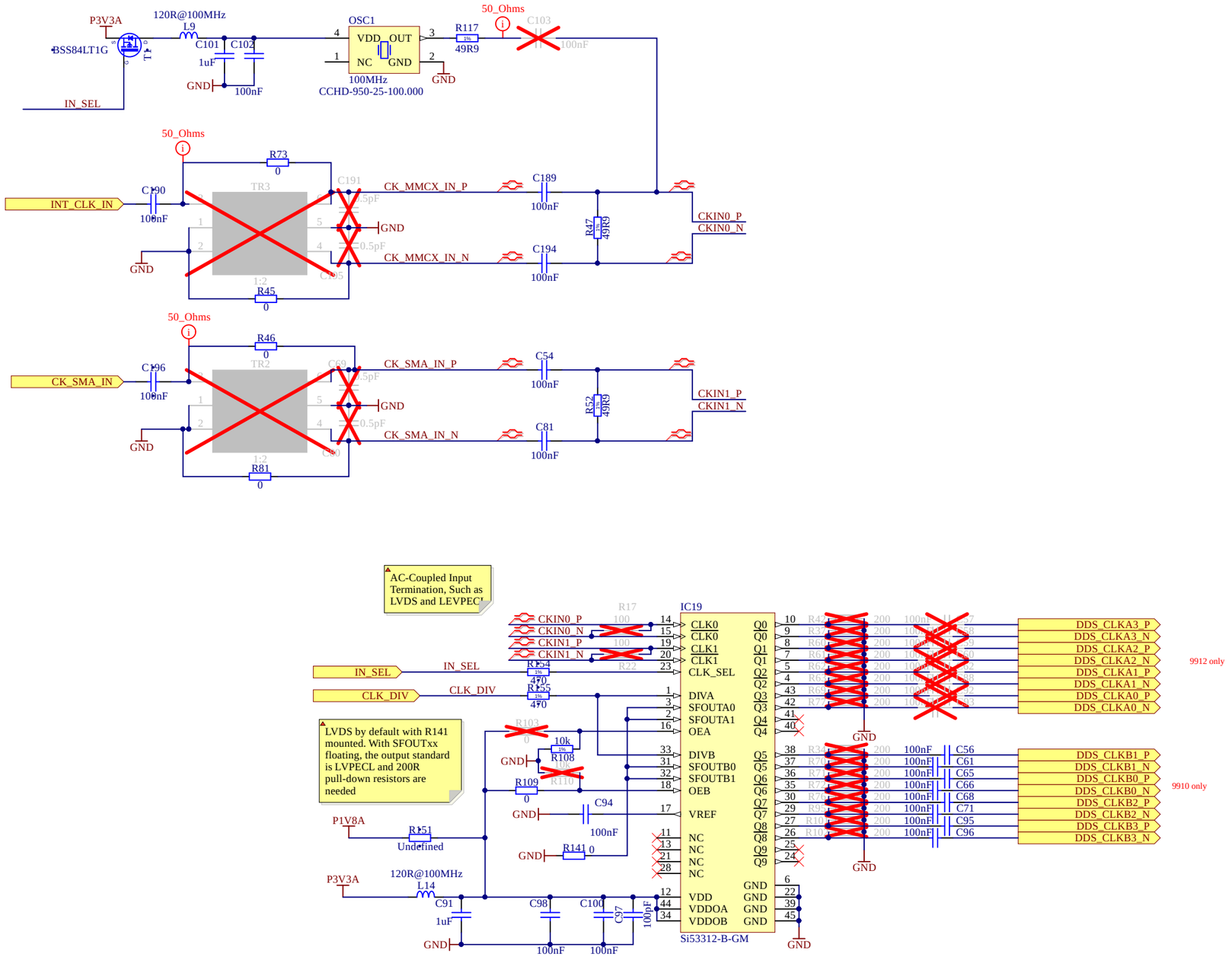
Project/Equipment	ARTIQ/SINARA
Document	9910 & 9912 DDS
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 11.12.2017
File	DDS_channel.SchDoc
Print Date	11.01.2018 01:08:24 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -



Project/Equipment	ARTIQ/SINARA		
Document	**Clock distribution and generation**	Designer G.K.	
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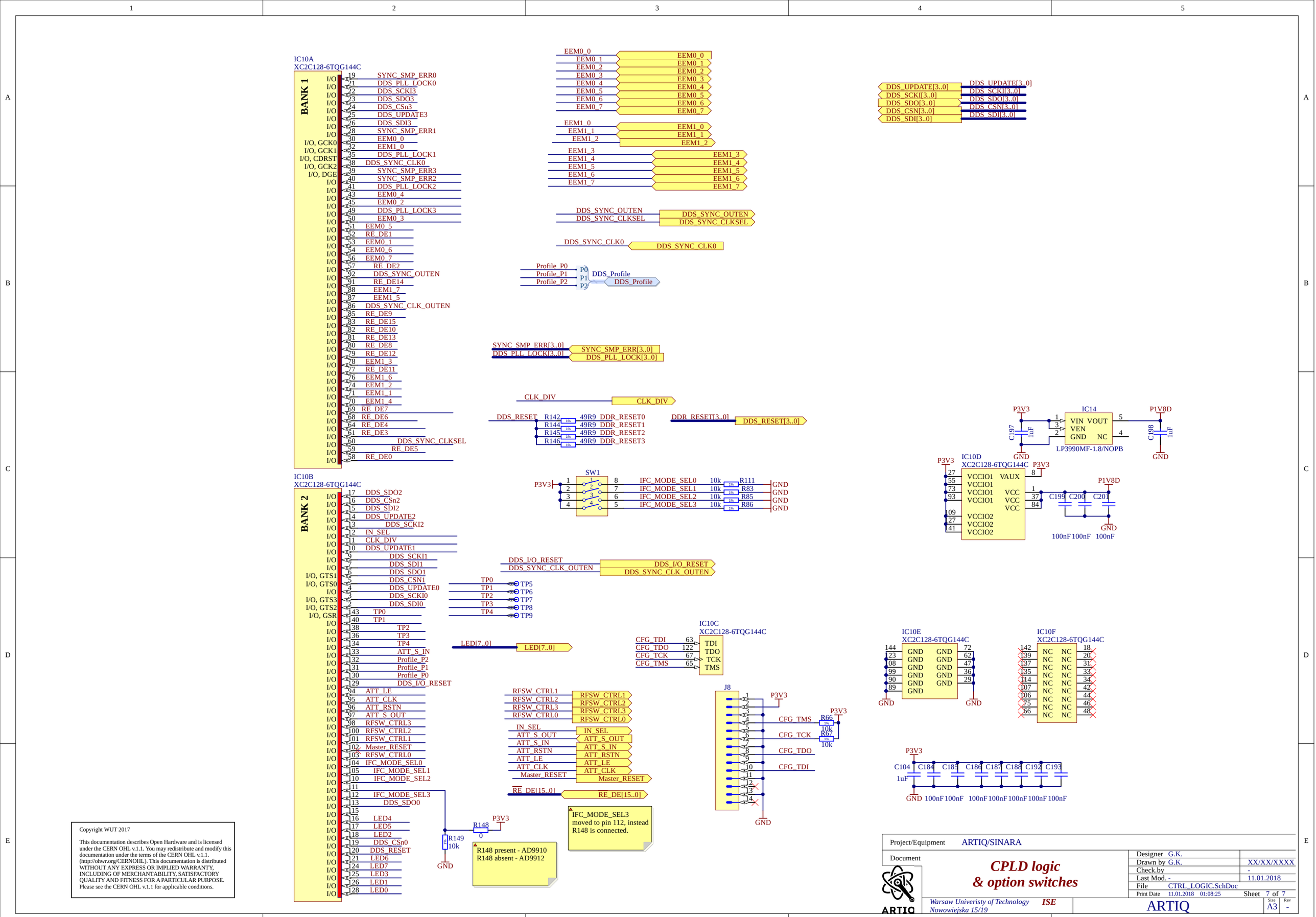
		Check.by	-
		Last Mod. -	10.01.2018
		File CLK_INPUT.SchDoc	
		Print Date 11.01.2018 01:08:24	Sheet 6 of 7
Warsaw Univeristy of Technology *Nowowiejska 15/19*	*ISE*	ARTIQ	Size A3 / Rev -


IC10A
XC2C128-6TQG144C
BANK 1
I/O 19 SYNC_SMP_ERR0
I/O 21 DDS_PLL_LOCK0
I/O 22 DDS_SCKI3
I/O 23 DDS_SDO3
I/O 24 DDS_CSn3
I/O 25 DDS_UPDATE3
I/O 26 DDS_SDI3
I/O 28 SYNC_SMP_ERR1
I/O, GCK0 30 EEM0_0
I/O, GCK1 32 EEM1_0
I/O, CDRST 35 DDS_PLL_LOCK1
I/O, GCK2 38 DDS_SYNC_CLK0
I/O, DGE 39 SYNC_SMP_ERR3
I/O 40 SYNC_SMP_ERR2
I/O 41 DDS_PLL_LOCK2
I/O 43 EEM0_4
I/O 45 EEM0_2
I/O 49 DDS_PLL_LOCK3
I/O 50 EEM0_3
I/O 51 EEM0_5
I/O 52 RE_DE1
I/O 53 EEM0_1
I/O 54 EEM0_6
I/O 56 EEM0_7
I/O 57 RE_DE2
I/O 92 DDS_SYNC_OUTEN
I/O 91 RE_DE14
I/O 88 EEM1_7
I/O 87 EEM1_5
I/O 86 DDS_SYNC_CLK_OUTEN
I/O 85 RE_DE9
I/O 83 RE_DE15
I/O 82 RE_DE10
I/O 81 RE_DE13
I/O 80 RE_DE8
I/O 79 RE_DE12
I/O 78 EEM1_3
I/O 77 RE_DE11
I/O 76 EEM1_6
I/O 74 EEM1_2
I/O 71 EEM1_1
I/O 70 EEM1_4
I/O 69 RE_DE7
I/O 68 RE_DE6
I/O 64 RE_DE4
I/O 61 RE_DE3
I/O 60 DDS_SYNC_CLKSEL
I/O 59 RE_DE5
I/O 58 RE_DE0
IC10B
XC2C128-6TQG144C
BANK 2
I/O 17 DDS_SDO2
I/O 16 DDS_CSn2
I/O 15 DDS_SDI2
I/O 14 DDS_UPDATE2
I/O 13 DDS_SCKI2
I/O 12 IN_SEL
I/O 11 CLK_DIV
I/O 10 DDS_UPDATE1
I/O 9 DDS_SCKI1
I/O 7 DDS_SDI1
I/O 6 DDS_SDO1
I/O, GTS1 5 DDS_CSN1
I/O, GTS0 4 DDS_UPDATE0
I/O 3 DDS_SCKI0
I/O, GTS3 2 DDS_SDI0
I/O, GTS2 143 TP0
I/O, GSR 140 TP1
I/O 138 TP2
I/O 136 TP3
I/O 134 TP4
I/O 133 ATT_S_IN
I/O 132 Profile_P2
I/O 131 Profile_P1
I/O 130 Profile_P0
I/O 129 DDS_I/O_RESET
I/O 94 ATT_LE
I/O 95 ATT_CLK
I/O 96 ATT_RSTN
I/O 97 ATT_S_OUT
I/O 98 RFSW_CTRL3
I/O 100 RFSW_CTRL2
I/O 101 RFSW_CTRL1
I/O 102 Master_RESET
I/O 103 RFSW_CTRL0
I/O 104 IFC_MODE_SEL0
I/O 105 IFC_MODE_SEL1
I/O 110 IFC_MODE_SEL2
I/O 111
I/O 112 IFC_MODE_SEL3
I/O 113 DDS_SDO0
I/O 115
I/O 116 LED4
I/O 117 LED5
I/O 118 LED2
I/O 119 DDS_CSn0
I/O 120 DDS_RESET
I/O 121 LED6
I/O 124 LED7
I/O 125 LED3
I/O 126 LED1
I/O 128 LED0
EEM0_0 EEM0_1 EEM0_2 EEM0_3 EEM0_4 EEM0_5 EEM0_6 EEM0_7
EEM1_0 EEM1_1 EEM1_2 EEM1_3 EEM1_4 EEM1_5 EEM1_6 EEM1_7
DDS_UPDATE[3..0] DDS_SCKI[3..0] DDS_SDO[3..0] DDS_CSN[3..0] DDS_SDI[3..0]
DDS_SYNC_OUTEN DDS_SYNC_CLKSEL
DDS_SYNC_CLK0
Profile_P0 Profile_P1 Profile_P2 P0 P1 P2 DDS_Profile
SYNC_SMP_ERR[3..0] DDS_PLL_LOCK[3..0]
CLK_DIV
DDS_RESET R142 R144 R145 R146 49R9 DDR_RESET0 DDR_RESET1 DDR_RESET2 DDR_RESET3
DDR_RESET[3..0]
SW1 P3V3 IFC_MODE_SEL0 IFC_MODE_SEL1 IFC_MODE_SEL2 IFC_MODE_SEL3 10k R111 R83 R85 R86 GND
DDS_I/O_RESET DDS_SYNC_CLK_OUTEN
TP0 TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9
LED[7..0]
IC10C
XC2C128-6TQG144C
CFG_TDI 63 CFG_TDO 122 CFG_TCK 67 CFG_TMS 65 TDI TDO TCK TMS
RFSW_CTRL1 RFSW_CTRL2 RFSW_CTRL3 RFSW_CTRL0
IN_SEL ATT_S_OUT ATT_S_IN ATT_RSTN ATT_LE ATT_CLK Master_RESET
RE_DE[15..0]
R148 P3V3 0
R149 10k GND
R148 present - AD9910
R148 absent - AD9912
IFC_MODE_SEL3 moved to pin 112, instead R148 is connected.
J8 P3V3 CFG_TMS CFG_TCK CFG_TDO CFG_TDI R66 R67 10k GND
IC10E
XC2C128-6TQG144C
GND
IC10F
XC2C128-6TQG144C
NC
P3V3 C197 1uF GND IC14 VIN VOUT VEN GND NC LP3990MF-1.8/NOPB C198 1uF P1V8D
IC10D
XC2C128-6TQG144C
VCCIO1 VAUX VCC VCCIO2
C199 C200 C201 100nF 100nF 100nF
C104 C184 C185 C186 C187 C188 C192 C193 1uF 100nF
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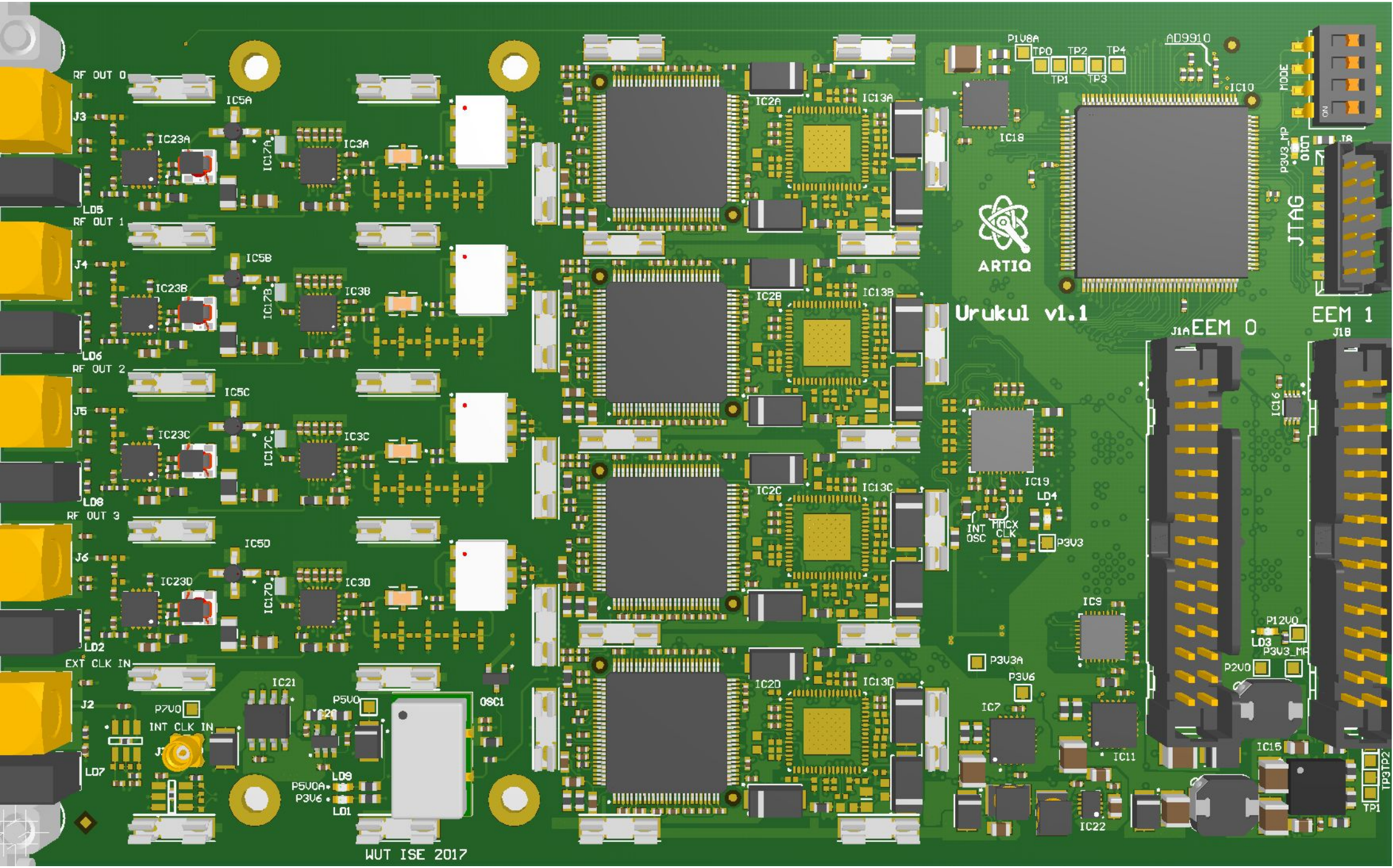
Project/Equipment ARTIQ/SINARA
Document
CPLD logic & option switches
Designer G.K.
Drawn by G.K. XX/XX/XXXX
Check.by -
Last Mod. - 11.01.2018
File CTRL_LOGIC.SchDoc
Print Date 11.01.2018 01:08:25 Sheet 7 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19 ISE
ARTIQ
Size A3 Rev -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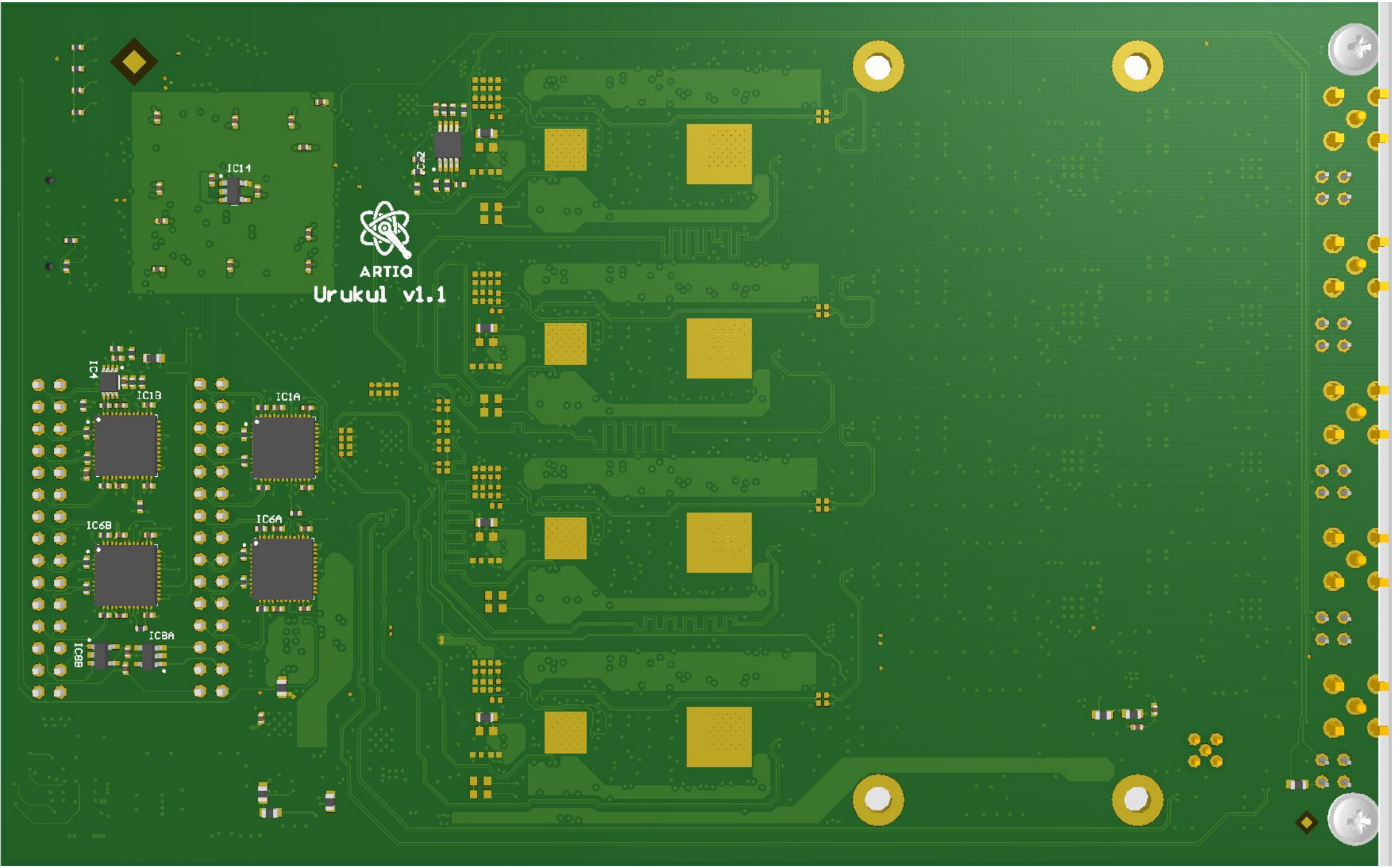
RF OUT 1
RF OUT 2
RF OUT 3
EXT CLK IN
INT CLK IN
Urukul v1.1
ARTIQ
EEM 0
EEM 1
JTAG
AD9910
WUT ISE 2017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IC2
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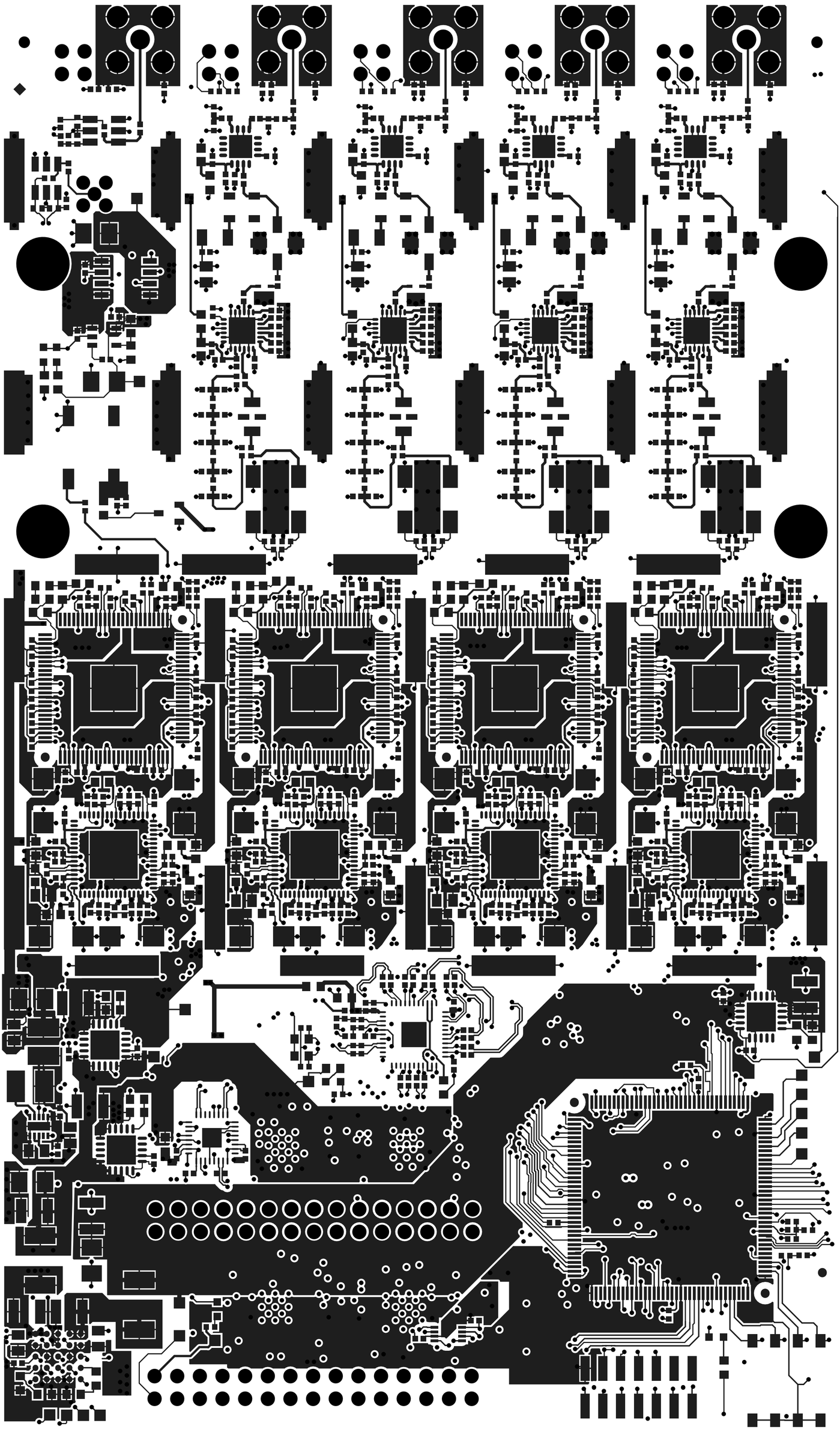
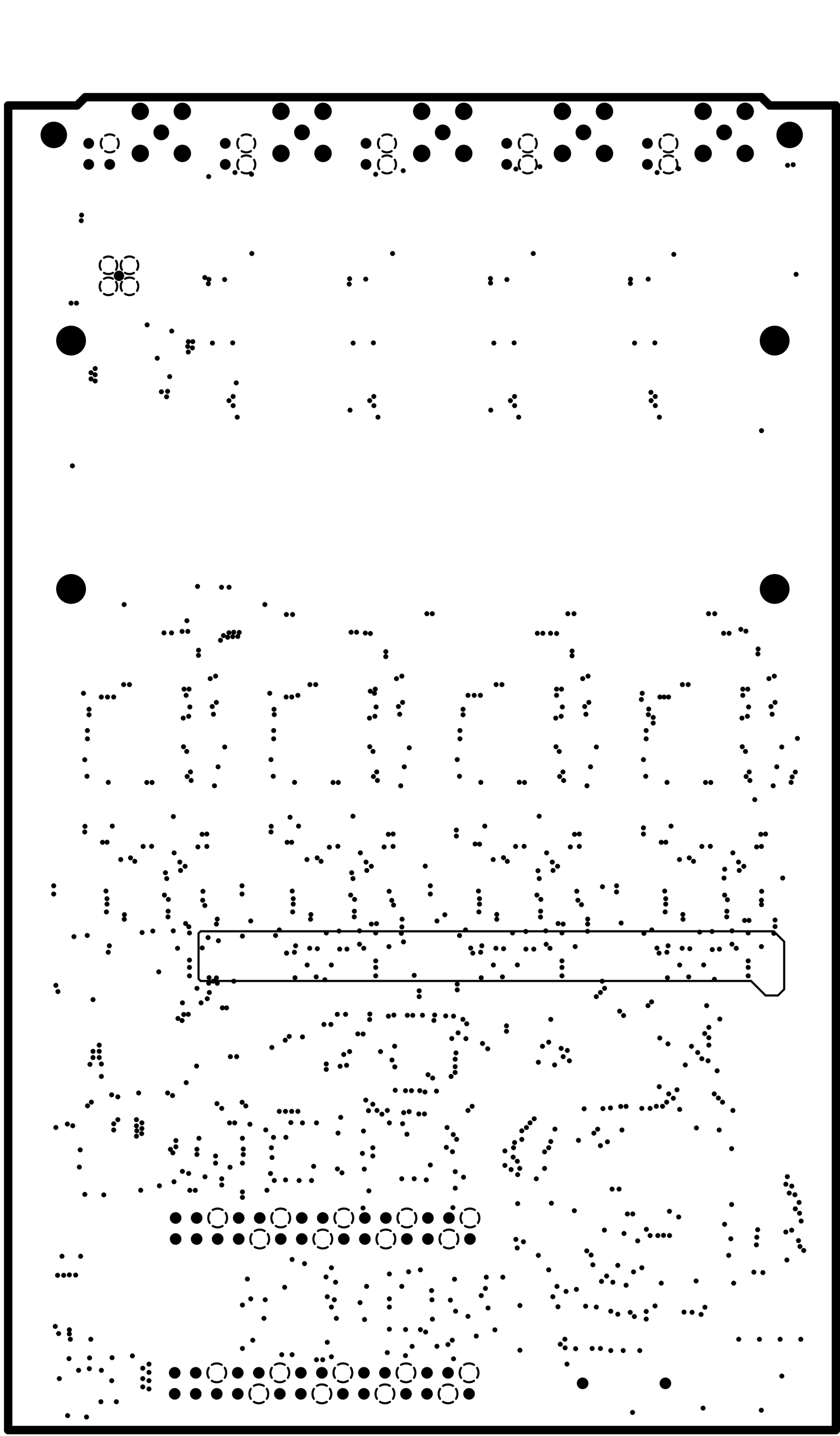
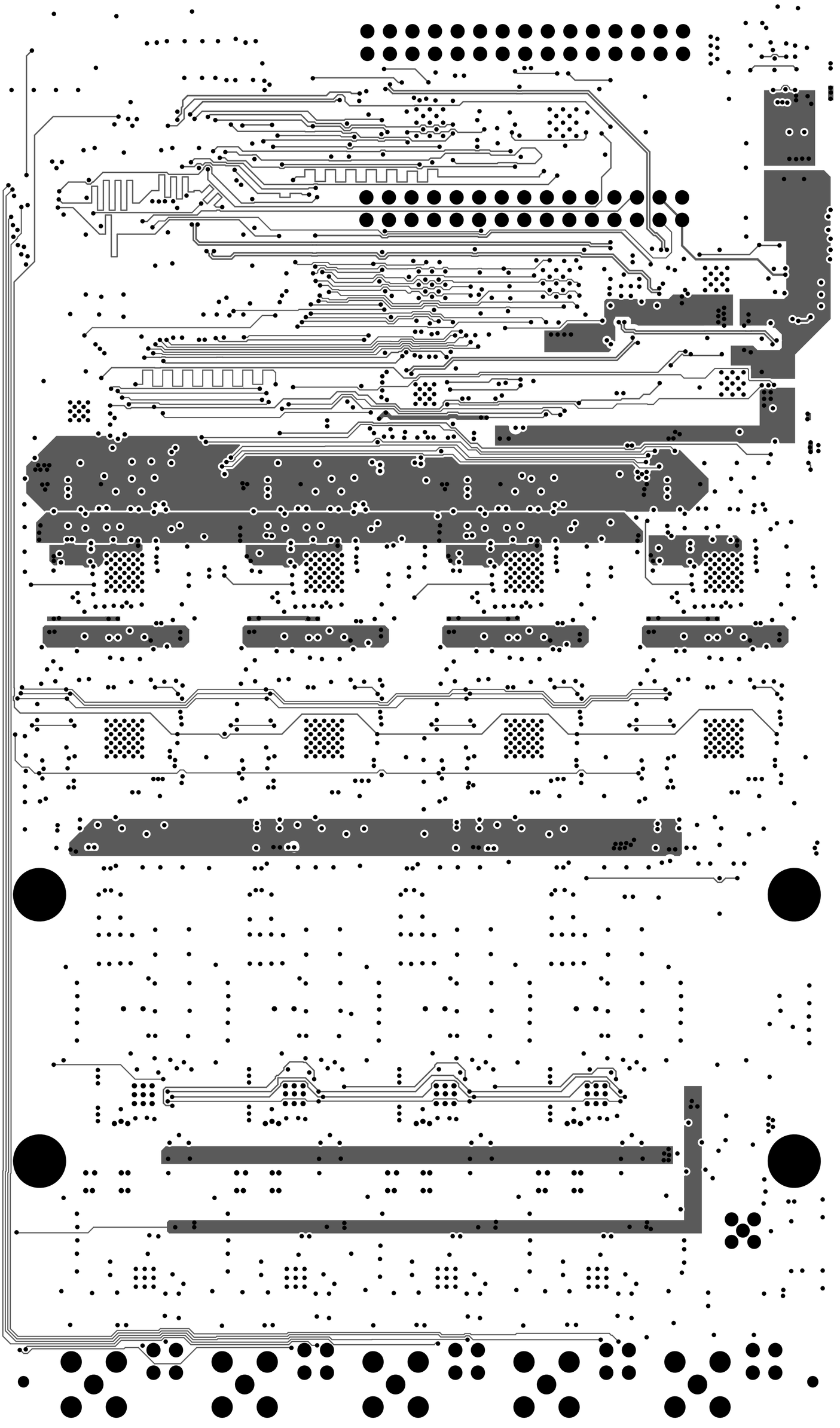
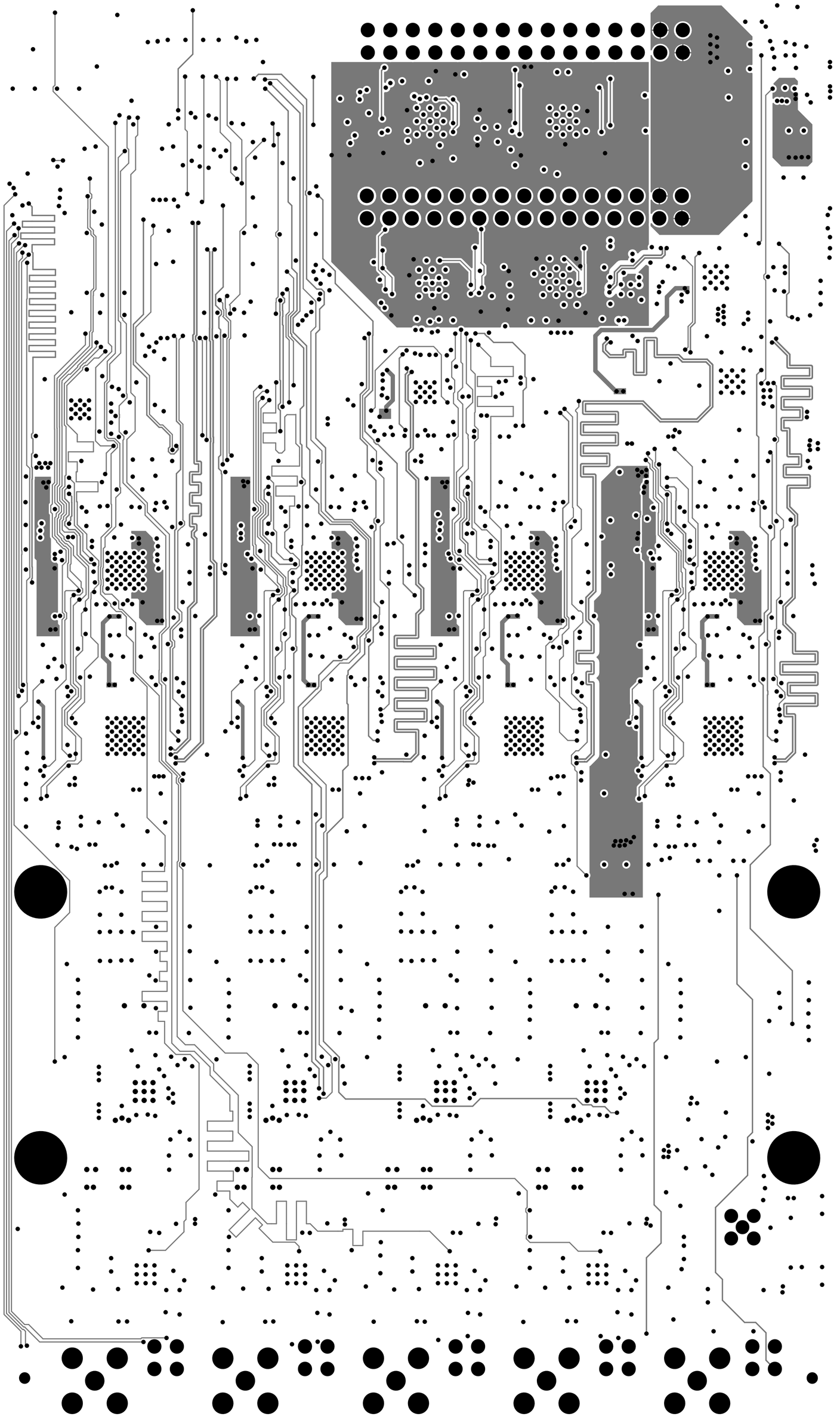
Urukul v1.1
IC4
IC1B
IC1A
IC6B
IC6A
IC8A
IC8B

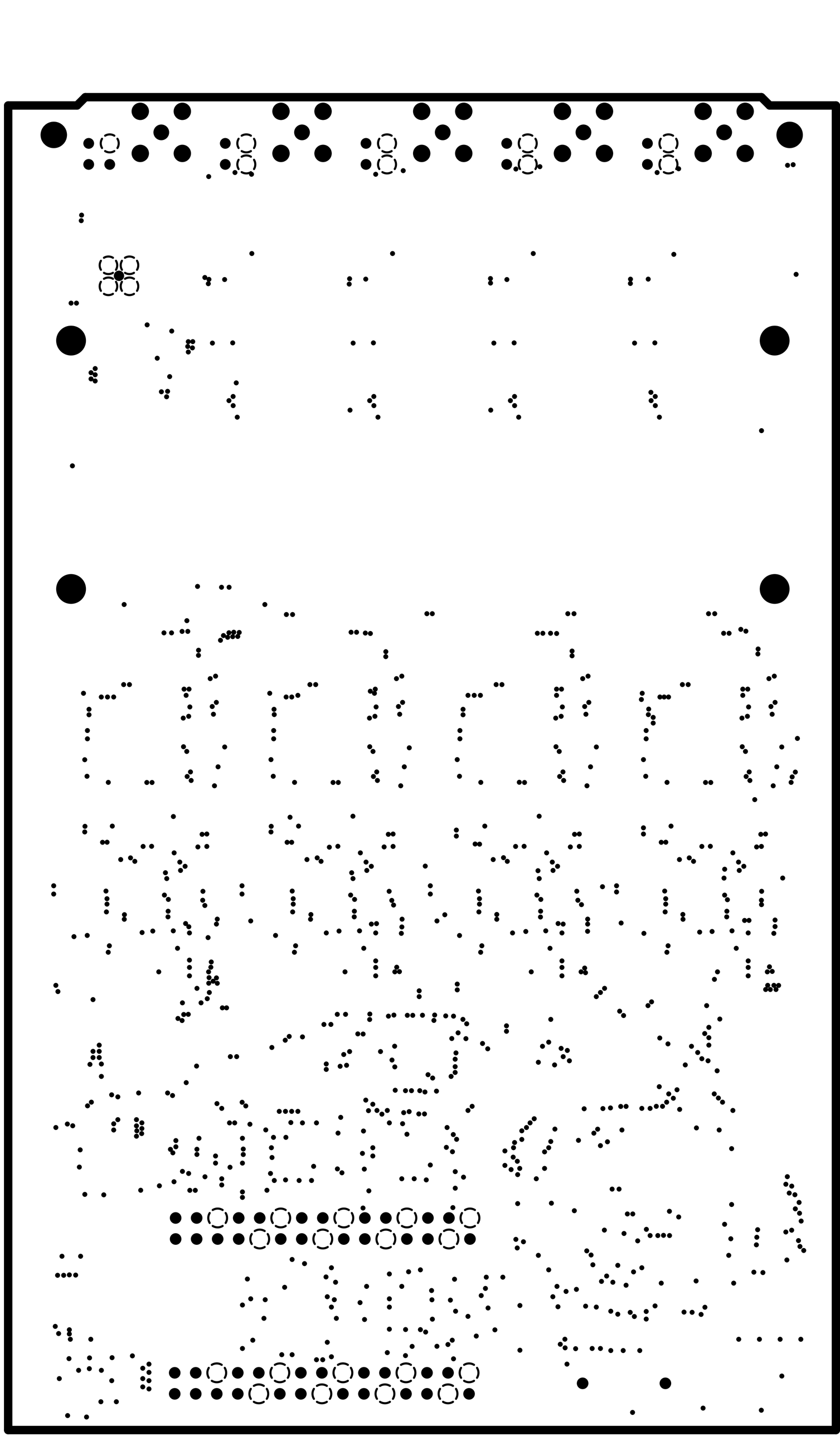
RF OUT 0
RF OUT 1
RF OUT 2
RF OUT 3
EXT CLK IN
INT CLK IN
J1A
EEM 0
J1B
EEM 1
Urukul v1.1
ARTIQ
WUT ISE 2017

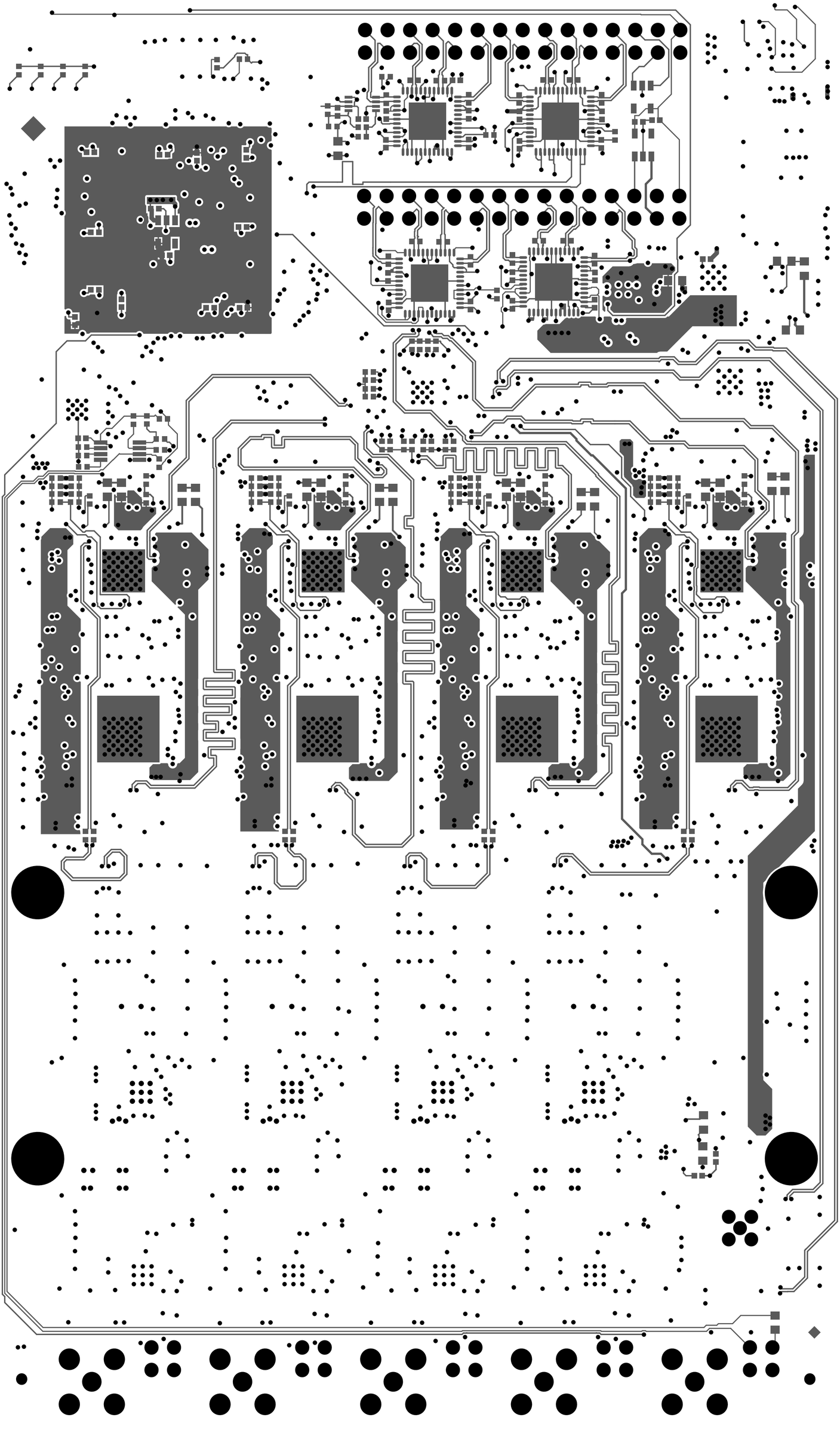












IC15
IC14
ARTIQ
Urukul v1.1
IC4
IC1A
IC1B
IC6A
IC6B
IC8A
IC8B