SFU

Simon Fraser University
Engineering Science Department

Final Project Implementation Manual

ENSC 350: Digital System Design
Spring 2024

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Set up Quartus Prime 23.1std and Program Code to FPGA Board

1. Click the **Quartus** under your Start (Quartus Prime 23.1std)

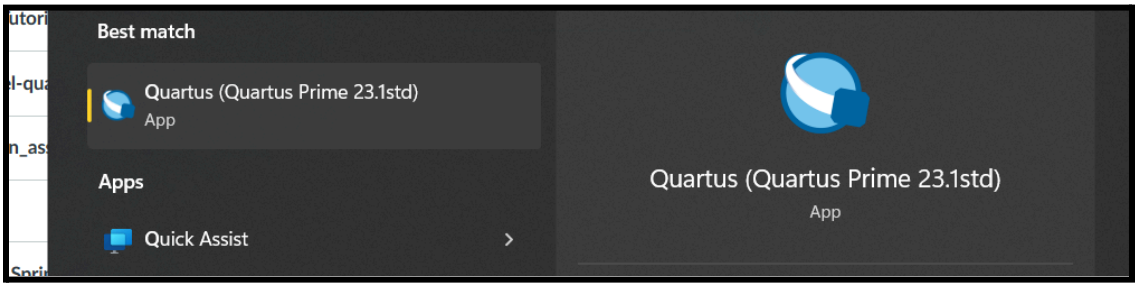


Figure 1: Quartus in Start Menu

2. After the program has opened, **click 'Open Project'** under the file tab. Find the correct project, and click 'Open'. The project should be saved as a **QPF File**.

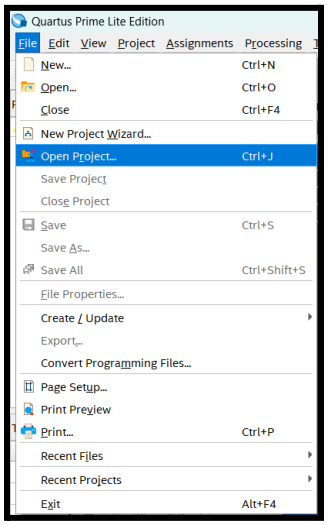


Figure 2: Open Project Under File Tab

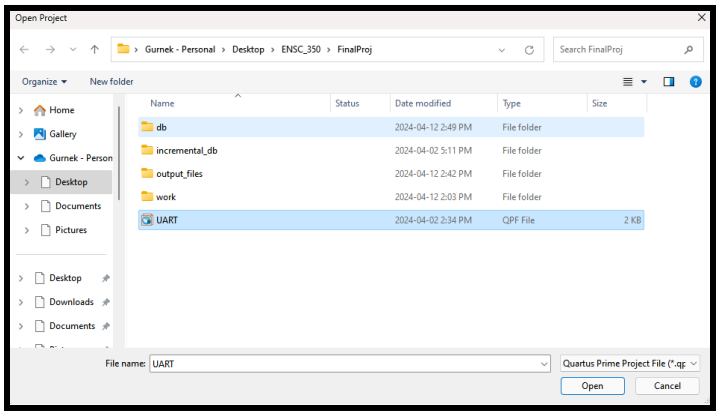


Figure 3: UART QPF File

3. Make sure ‘UART’ is set as the top entity under the project navigator tab. To check, click the drop down beside project navigator and select ‘Hierarchy’.
   NOTE: If it is not the top level entity, click the drop down again and select ‘Files’. From there right click on the ‘UART.vhd’ file and select ‘Set as Top-Level Entity’.

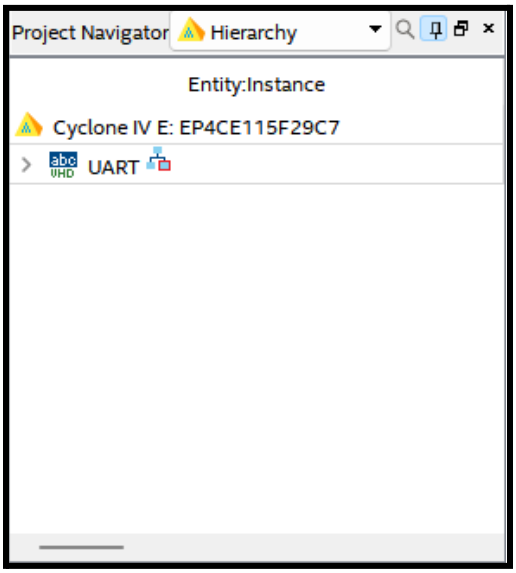


Figure 4: UART Set as Top-Level Entity Under Hierarchy

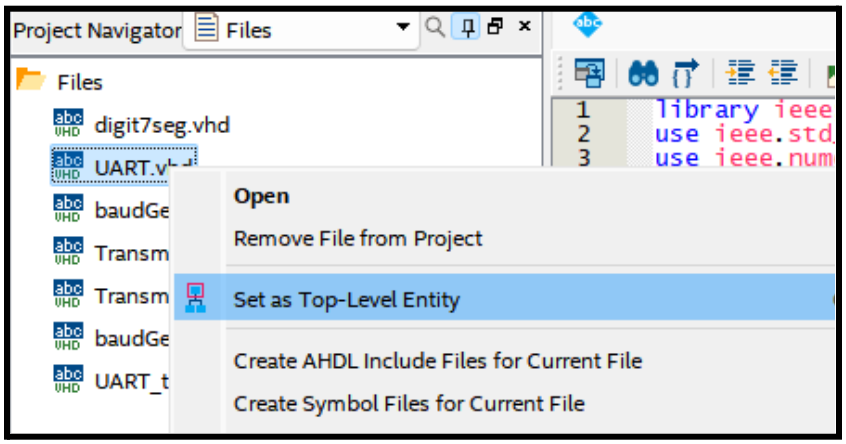


Figure 5: Set UART as Top-Level Entity Under Files (If not set already)

4. Click the **Start Compilation Button** at the top of the window or Press down ‘Ctrl + L’.

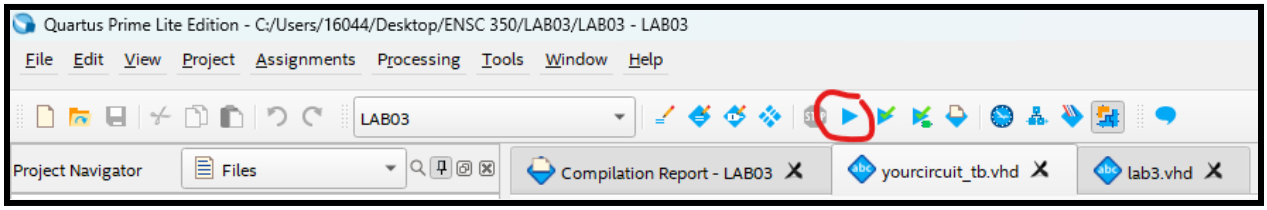


Figure 6: Location of Compliation Button in Quartus

5. While the code is being compiled. Let's connect the board to the computer. Make sure the setup is the same as figure 7. Connect your board to your computer using the USB blaster cable, and plug in the power cord into the board. Connect the RS-232 cable to the board and the computer. **Power it on**.

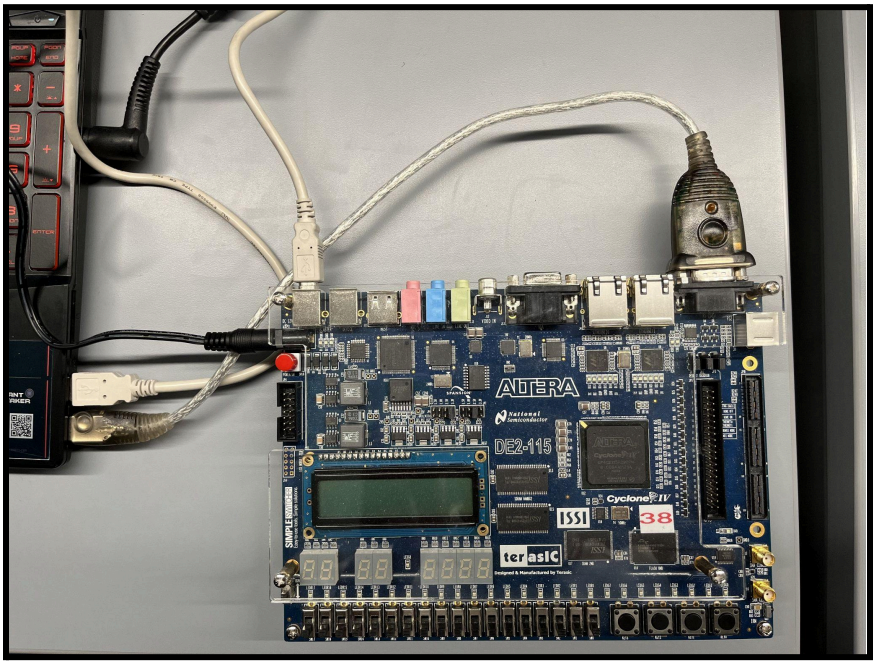


Figure 7: Overview of FPGA Setup

6. Once the project has finished compiling, go to **Tools** → **Programmer**. Click Hardware Setup, and **make sure 'JTAG' is selected**. If so, press Start. Ensure you have the correct device selected (EP4CE115F29). **Press 'Start'**.

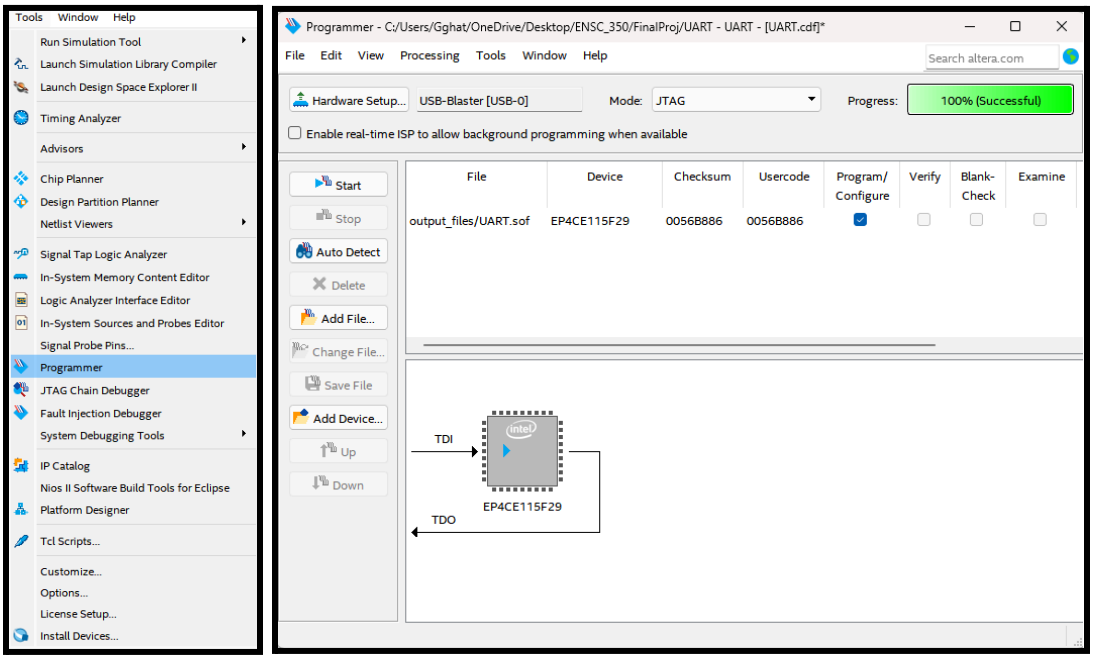


Figure 8: Steps to Program file to the board

Set up PuTTY

1. Search for **PuTTY** and click the PuTTY under your Start. **Note:** If PuTTY is not installed, look for downloadable link in the appendix)

Figure 9: PuTTY in Start Menu

2. Click SSH -> Serial under the Connection Tab on the left side, and enter these commands. Ensure that Speed(baud) is set to 19200, Parity is set to EVEN, and Flow control is set to RTS/CTS. (Refer to Figure #)
   NOTE: Serial line to connect to may be different. Go to device manager and expand the "Ports (COM & LPT)" tab to find the correct COM port. In this case it is COM5.

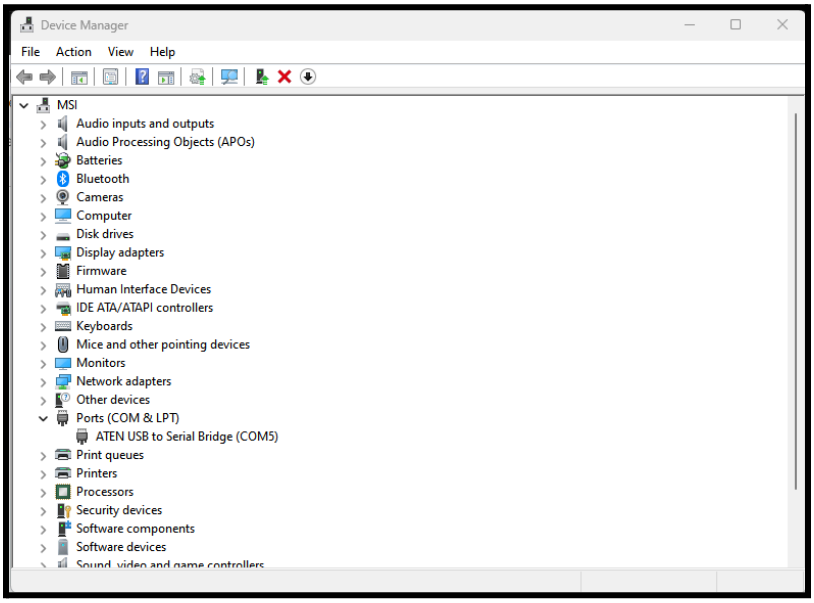


Figure 10: Device Manager to FInd COM Port

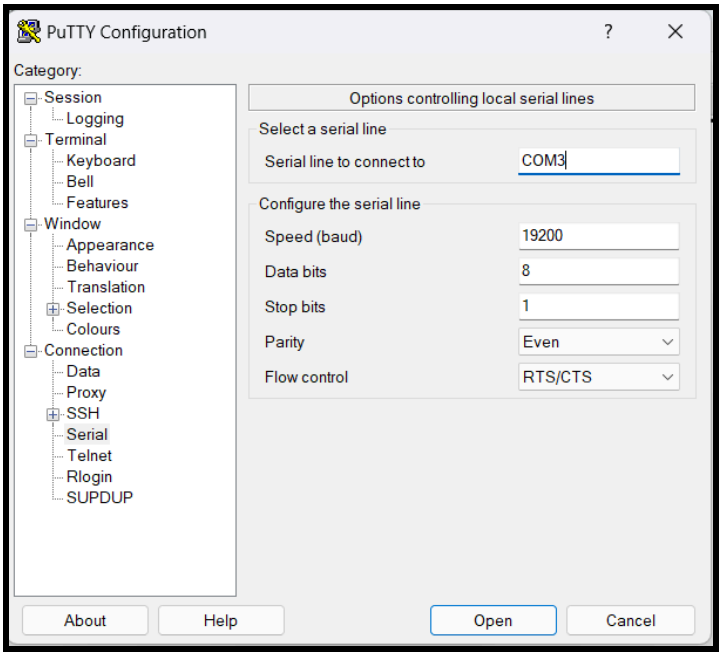


Figure 11: PuTTY Parameter Inputs

3. The setup is complete!

How to Run the Application Using the Programmed Board with PuTTY

For our implementation, we made a half-duplex, meaning our project is only capable of transmitting data to other devices, but not capable of receiving data.
Once you have completed the set up steps above, and your board has been programmed, perform the following steps in order to transmit:

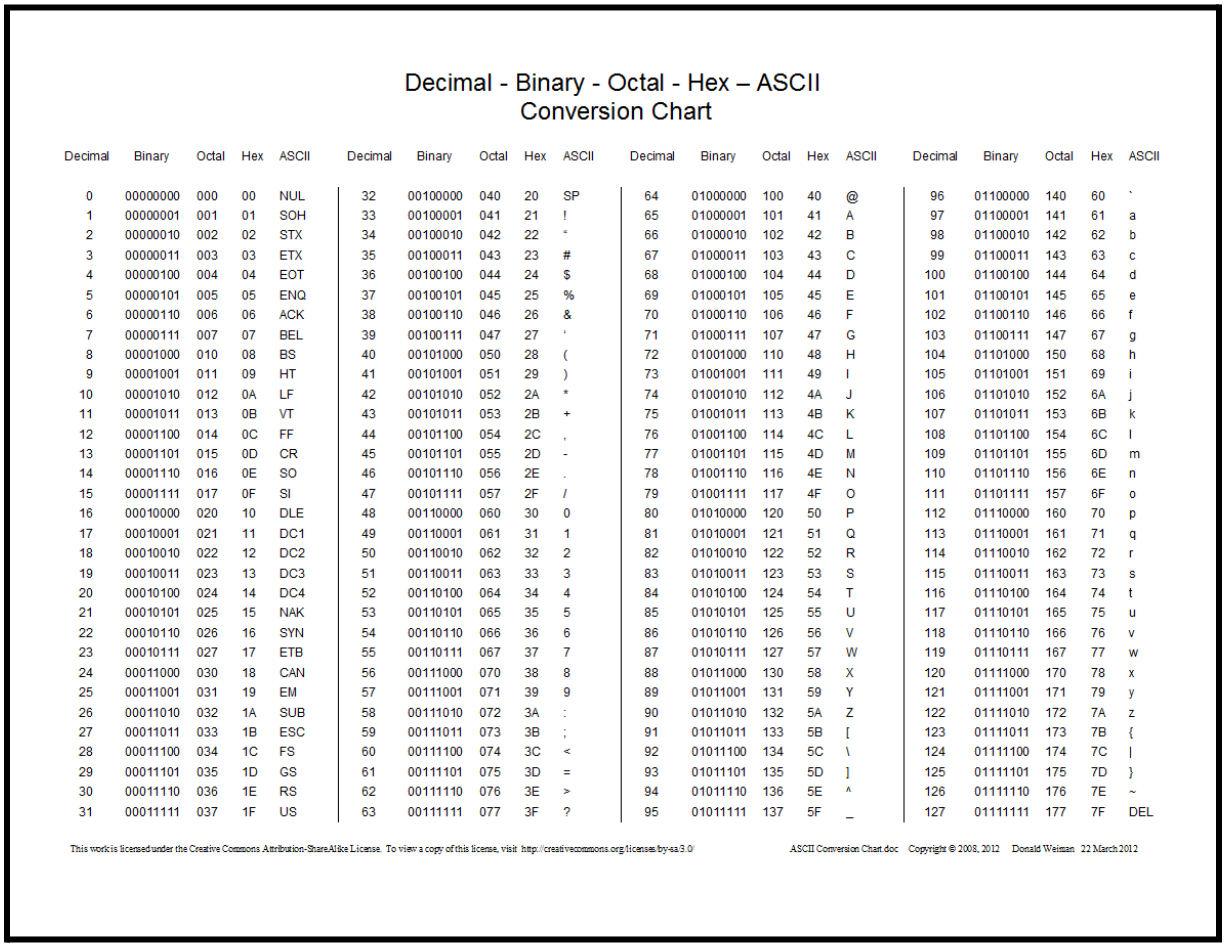
1. Plug in your RS-232 cable into the board (ensure you are using RS-232 port and not VGA port) and the other end into your device with PuTTY installed on it.
2. Set up your PuTTY according to the steps above and click open.
3. Input your data using the slider switches 7 down to 0. Make sure you input an ASCII character. You should see corresponding red LEDs light up.
4. Click the push-button labeled KEY0 to send the data. You should see green LED0 light up while you press the button.
5. You should see the correct ASCII character output on PuTTY's terminal.
7. Talk about how we implemented the switches (how to transmit)
8. Done

Appendix:

Download Quartus on Windows:
https://www.intel.com/content/www/us/en/software-kit/795127/intel-quartus-prime-standard-edition-design-software-version-23-1-for-windows.html

PuTTY executable link:
https://the.earth.li/~sgtatham/putty/latest/w64/putty.exe

ASCII Table:



Decimal - Binary - Octal - Hex – ASCII
Conversion Chart

Decimal	Binary	Octal	Hex	ASCII	Decimal	Binary	Octal	Hex	ASCII	Decimal	Binary	Octal	Hex	ASCII	Decimal	Binary	Octal	Hex	ASCII
0	00000000	000	00	NUL	32	00100000	040	20	SP	64	01000000	100	40	@	96	01100000	140	60	`
1	00000001	001	01	SOH	33	00100001	041	21	!	65	01000001	101	41	A	97	01100001	141	61	a
2	00000010	002	02	STX	34	00100010	042	22	"	66	01000010	102	42	B	98	01100010	142	62	b
3	00000011	003	03	ETX	35	00100011	043	23	#	67	01000011	103	43	C	99	01100011	143	63	c
4	00000100	004	04	EOT	36	00100100	044	24	$	68	01000100	104	44	D	100	01100100	144	64	d
5	00000101	005	05	ENQ	37	00100101	045	25	%	69	01000101	105	45	E	101	01100101	145	65	e
6	00000110	006	06	ACK	38	00100110	046	26	&	70	01000110	106	46	F	102	01100110	146	66	f
7	00000111	007	07	BEL	39	00100111	047	27	'	71	01000111	107	47	G	103	01100111	147	67	g
8	00001000	010	08	BS	40	00101000	050	28	(	72	01001000	110	48	H	104	01101000	150	68	h
9	00001001	011	09	HT	41	00101001	051	29	)	73	01001001	111	49	I	105	01101001	151	69	i
10	00001010	012	0A	LF	42	00101010	052	2A	*	74	01001010	112	4A	J	106	01101010	152	6A	j
11	00001011	013	0B	VT	43	00101011	053	2B	+	75	01001011	113	4B	K	107	01101011	153	6B	k
12	00001100	014	0C	FF	44	00101100	054	2C	,	76	01001100	114	4C	L	108	01101100	154	6C	l
13	00001101	015	0D	CR	45	00101101	055	2D	-	77	01001101	115	4D	M	109	01101101	155	6D	m
14	00001110	016	0E	SO	46	00101110	056	2E	.	78	01001110	116	4E	N	110	01101110	156	6E	n
15	00001111	017	0F	SI	47	00101111	057	2F	/	79	01001111	117	4F	O	111	01101111	157	6F	o
16	00010000	020	10	DLE	48	00110000	060	30	0	80	01010000	120	50	P	112	01110000	160	70	p
17	00010001	021	11	DC1	49	00110001	061	31	1	81	01010001	121	51	Q	113	01110001	161	71	q
18	00010010	022	12	DC2	50	00110010	062	32	2	82	01010010	122	52	R	114	01110010	162	72	r
19	00010011	023	13	DC3	51	00110011	063	33	3	83	01010011	123	53	S	115	01110011	163	73	s
20	00010100	024	14	DC4	52	00110100	064	34	4	84	01010100	124	54	T	116	01110100	164	74	t
21	00010101	025	15	NAK	53	00110101	065	35	5	85	01010101	125	55	U	117	01110101	165	75	u
22	00010110	026	16	SYN	54	00110110	066	36	6	86	01010110	126	56	V	118	01110110	166	76	v
23	00010111	027	17	ETB	55	00110111	067	37	7	87	01010111	127	57	W	119	01110111	167	77	w
24	00011000	030	18	CAN	56	00111000	070	38	8	88	01011000	130	58	X	120	01111000	170	78	x
25	00011001	031	19	EM	57	00111001	071	39	9	89	01011001	131	59	Y	121	01111001	171	79	y
26	00011010	032	1A	SUB	58	00111010	072	3A	:	90	01011010	132	5A	Z	122	01111010	172	7A	z
27	00011011	033	1B	ESC	59	00111011	073	3B	;	91	01011011	133	5B	[	123	01111011	173	7B	{
28	00011100	034	1C	FS	60	00111100	074	3C	<	92	01011100	134	5C	\	124	01111100	174	7C	|
29	00011101	035	1D	GS	61	00111101	075	3D	=	93	01011101	135	5D	]	125	01111101	175	7D	}
30	00011110	036	1E	RS	62	00111110	076	3E	>	94	01011110	136	5E	^	126	01111110	176	7E	~
31	00011111	037	1F	US	63	00111111	077	3F	?	95	01011111	137	5F	_	127	01111111	177	7F	DEL