Computer Architecture HW#1

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Q1.

(A) Performance expressed in instructions per second $= \frac{\text{Clock Rate}}{\text{CPI}}$

P_1 : $\frac{3GHz}{1.5} = 2\times10^9$ instructions per second

P_2 : $\frac{2.5GHz}{1.0} = 2.5\times10^9$ instructions per second

P_3 : $\frac{4.0GHz}{2.2} \approx 1.82\times10^9$ instructions per second

$\therefore$ P_2 has the highest performance expressed in instructions per second.

(B) number of cycles = Clock Rate × Execution time

number of instructions = number of Cycles / CPI

i) Cycles

P1 : $3GHz \times 10s = 3\times10^{10}$ cycles

P2 : $2.5GHz \times 10s = 2.5\times10^{10}$ cycles

P3 : $4.0GHz \times 10s = 4.0\times10^{10}$ cycles

ii) Instructions

P1 : $3\times10^{10} / 1.5 = 2.0\times10^{10}$ instructions

P2 : $2.5\times10^{10} / 1.0 = 2.5\times10^{10}$ instructions

P3 : $4.0\times10^{10} / 2.2 \approx 1.82\times10^{10}$ instructions

(C) execution time (CPU Time) $= \frac{\text{CPU Clock Cycles}}{\text{Clock Rate}} = \frac{\text{Instruction Count} \times \text{CPI}}{\text{Clock Rate}}$

$(1-\frac{30}{100}) \times$ execution time $= IC \times (1+\frac{20}{100}) \times CPI / \text{Clock Rate}'$

$\text{Clock Rate}' = \frac{12}{7} \times \text{Clock Rate} \approx 1.71 \times \text{Clock Rate}$

$\therefore$ Clock Rate' for each processor :

P1 : $1.71 \times 3GHz = 5.13 GHz$

P2 : $1.71 \times 2.5GHz = 4.275 GHz$

P3 : $1.71 \times 4.0GHz = 6.84 GHz$

Q2.

(A) $P_{dynamic}$ = Capacitive load × Voltage^2 × Frequency

· Pentium 4 Prescott : $90W = \frac{1}{2} \times \text{Capacitive load} \times (1.25V)^2 \times 3.6GHz$

$\text{Capacitive load} = 2 \times \frac{90W}{(1.25V)^2 \times 3.6GHz} = 32nF$

· Core i5 Ivy Bridge : $40W = \frac{1}{2} \times \text{Capacitive load} \times (0.9V)^2 \times 3.4GHz$

$\text{Capacitive load} = 2 \times \frac{40W}{(0.9V)^2 \times 3.4GHz} \approx 29.04nF$

(B) Percentage of Static Power in Total Dissipated Power $= \left(\frac{P_{static}}{P_{dynamic} + P_{static}}\right) \times 100$

- Pentium 4 Prescott : $\frac{10W}{10W + 90W} \times 100 = 10\%$
- Core i5 Ivy Bridge : $\frac{30W}{30W + 40W} \times 100 \approx 42.86\%$

Ratio of static power to dynamic power $= \frac{P_{static}}{P_{dynamic}}$

- Pentium 4 Prescott : $\frac{10W}{90W} = \frac{1}{9} \approx 0.11$
- Core i5 Ivy Bridge : $\frac{30W}{40W} = \frac{3}{4} = 0.75$

(C) $P_{total} = P_{dynamic} + P_{static} = \frac{1}{2}CV^2f + VI$, $0.9\, P_{total} = \frac{1}{2}CV'^2f + V'I$ (전압은 양수이므로 이차방정식의 해에서 양수인 해)

- Pentium 4 Prescott : $90 = \frac{1}{2} \times 32 \times V'^2 \times 3.6 + V' \times \frac{10}{1.25} = 57.6V'^2 + 8V'$, $V' \approx 1.182V$ $\therefore$ 0.068V reduced
- Core i5 Ivy Bridge : $63 = \frac{1}{2} \times 29.04 \times V'^2 \times 3.4 + V' \times \frac{30}{0.9} = 49.368V'^2 + \frac{100}{3}V'$, $V' \approx 0.84V$ $\therefore$ 0.06V reduced

$\therefore$ $V_{pentium}$ should be reduced by 5.4%, $V_{core\ i5}$ should be reduced by 6.34%

Q3.

(A) execution time = IC × CPI × Clock Cycle time

$750s = 2.389E12 \times CPI \times 0.333ns$

$CPI = \frac{750s}{2.389E12 \times 0.333ns} = \frac{750s}{2389 \times 0.333s} \approx 0.9428$

(B) $SPEC_{ratio} = \frac{\text{Reference Time}}{\text{Execution Time}} = \frac{9650s}{750s} \approx 12.87$

(C) CPU time$'$ $= (1 + \frac{10}{100}) \times IC \times CPI \times$ Clock Cycle time

$= 1.1 \times IC \times CPI \times$ Clock Cycle time $= 1.1 \times$ CPU time

$\therefore$ 10% increase of CPU time

(D) CPU time$'$ $= (1 + \frac{10}{100}) \times IC \times (1 + \frac{5}{100}) \times CPI \times$ Clock Cycle time

$= 1.155 \times IC \times CPI \times$ Clock Cycle time $= 1.155 \times$ CPU time

$\therefore$ 15.5% increase of CPU time

(E) $SPEC_{ratio}' = \frac{\text{Reference time}}{1.155 \times \text{Execution time}} = SPEC_{ratio} / 1.155 \approx 11.14$ ((D) 에서의 change 라고 가정했습니다.)

$\therefore$ change of SPEC ratio = 12.87 − 11.14 = 1.73 , 1.73 decreased

ratio of change $= \frac{SPEC\ ratio'}{SPEC\ ratio} \approx 0.87$, 13% decreased

(F) $700s = (1 - \frac{15}{100}) \times 2.389E12 \times CPI' / 4GHz$

$CPI' = \frac{700s \times 4GHz}{0.85 \times 2.389E12} = \frac{2800}{0.85 \times 2389} \approx 1.38$

(G) increase ratio of CPI $= \frac{1.38}{0.9428} \approx 1.46$

increase ratio of clock rate $= \frac{4GHz}{3GHz} \approx 1.33$

$\therefore$ they are disimilar because instruction count has been reduced by 15%.

(H) Cpu time reduced by 6.7% $\left(\frac{750-700}{750}\times 100 \approx 0.67\right)$

(I) $\left(1-\frac{10}{100}\right)\times 960\,s = IC \times 1.61 / 4GHz$ (960 ns 가 아니라 960s 로 계산했습니다.)

$\therefore IC = \frac{0.9\times 960s \times 4GHz}{1.61} \approx 2147\times 10^9$ instructions

(J) $0.9\times 0.9\times 960s = 2147\times 10^9 \times 1.61 / \text{clock rate}$

clock rate $= \frac{2147\times 10^9 \times 1.61}{0.9\times 0.9\times 960s} \approx 4.45\,GHz$ ((I) 에서 추가적으로 CPU time을 10% 감소한다고 가정했습니다.)

(K) In (I), $960s = IC\times 1.61 / 3GHz$, $IC = \frac{960s\times 3GHz}{1.61}$ ((I) 의 첫 CPU 에서 변한다고 가정했습니다.)

$\left(1-\frac{20}{100}\right)\times 960s = IC \times \left(1-\frac{15}{100}\right)\times 1.61 / \text{clock rate}$

clock rate $= 3\,GHz \times 0.85 \div 0.8 \approx 3.19\,GHz$

Q4.

CPU time $= \frac{IC \times CPI}{\text{Clock Rate}}$

Execution time = CPU time for FP + CPU time for INT + CPU time for L/S + CPU time for branch

$= \frac{50\times10^6\times1 + 110\times10^6\times1 + 80\times10^6\times4 + 16\times10^6\times2}{2\times10^9} = \frac{512\times10^6}{2\times10^9} = 0.256s$

(A) $\frac{0.256s}{2} = \frac{50\times10^6\times x + 110\times10^6\times1 + 80\times10^6\times4 + 16\times10^6\times2}{2\times10^9} = \frac{(462+50x)}{2\times10^3} = (231+25x)\times\frac{1}{1000}$

$128 = 231+25x$, $x = \frac{-103}{25}$

$\therefore$ we can't calculate improved CPI of FP instructions

(B) $0.128 = \frac{50\times10^6\times1 + 110\times10^6\times1 + 80\times10^6\times x + 16\times10^6\times2}{2\times10^9}$

$= \frac{(192+80x)\times10^6}{2\times10^9}$

$128 = 96+40x$, $x = \frac{32}{40} = 0.8$

$\therefore$ CPI of L/S instructions is improved by 5 times $\left(\because \frac{4}{0.8}=5\right)$

(C) CPI of FP, INT instructions : $1\times 0.6 = 0.6$

CPI of L/S, branch instructions : $4\times0.7 = 2.8$, $2\times0.7 = 1.4$

$\therefore$ Execution time $= \frac{50\times10^6\times0.6 + 110\times10^6\times0.6 + 80\times10^6\times2.8 + 16\times10^6\times1.4}{2\times10^9}$

$= 0.1712\,s$

Execution time is improved by 1.5 times. $\left(\because \frac{0.256}{0.1712}\approx 1.5\right)$