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An Audio Band Sigma-Delta Modulator with 103dB SNDR

Contents

1 Introduction

This report details the design a Sigma-Delta modulator in a design exercise. The specifications of this modulator are described in section 2. Full simulation of the design in macro-model in Cadence was not completed due to time constraints but no problems are anticipated.

Time constraints were aggravated due to experimentation with a CIFB design that required extensive modification in Simulink to be succesfully verified. Unfortunately, there were many bugs encountered due to inexperience editing Simulink models. Finally, this design was abandoned in favour of a more established design that could meet the specifications.

A 2+1 MASH converter was chosen with an OSR of 128 to give adequate margin on the specifications. It is shown that this is a robust design that is capable of meeting the specifications. Due to time constraints it was not feasible to implement all the required extra blocks to build this modulator in Cadence. Verification of the operation of the macro-model was performed on a first order modulator instead, as most noise is expected to be attributed to the first stage.

Table 2.0.1: A summary of the specifications required for this Sigma-Delta ADC.

Specification	Value
Supply Voltage (V_{dd})	$3.3V$
Differential Input Voltage	$1.8V_{rms}$
Reference voltage V_{refn}	$0V$
Refererence voltage V_{refp}	$0.9 \times V_{dd}$
Signal to Noise Ratio	$103dB$
Total Harmonic Distortion at full-scale	$-85dB$
NO audio band limit cycles or tones	N/A
A flat audio band noise profile	N/A
Exclusive voltage references	N/A
Clock Frequency	$12.288MHz$

2 Design

The specifications for this Sigma-Delta modulator to meet are shown in table 2.0.1. These specifications are a relatively low signal bandwidth and a very high SNDR that is characteristic of an audio band ADC. In this section different options are evaluated and chosen from to meet these specifications.

2.1 Noise in Switched Capacitor Integrators

For any size of modulator the noise will be dominated by the first integrator at the input[1]. Shown in table 2.1.1 are the required input capacitor sizings for different OSRs and for a presumed SNDR of 106dB for a small margin on the specifications. Also shown in table 2.1.1 are the required g_ms of the amplifiers in the first integrator for these capacitor sizes and settling errors required.

Quantisation noise is intended to be a very small part of the noise budget([2], p.437) - making the initial SNDR target 123dB. The capacitor sizes are found by equating the expected quantisation noise for a 123dB SNDR with the expected kT/C noise on the capacitor:

$$\frac{mkT}{COSR} = N_q^2 = \frac{V_{inRMS}^2}{10^{\frac{SNDR}{10}}} = \frac{1.8^2}{10^{\frac{106}{10}}} = 8.14 \times 10^{-11} \tag{2.1.1}$$

$$C = \frac{mkT}{OSRN_q^2} = \frac{4 \times 1.23 \times 10^{-23} \times 293}{OSR \times 8.14 \times 10^{-11}} \tag{2.1.2}$$

Where V_{inRMS} is the RMS differential voltage range and $m = 4$ for a differential circuit.

To find the required g_m, linear settling is assumed, and the settling time is dependent on OSR:

$$\tau_{settling} = \frac{256 \times T_{clk}}{2 \times OSR} \tag{2.1.3}$$

Table 2.1.1: A table summarising the required capacitor sizes and amplifier g_ms for different OSRs.

OSR	Required Capacitor Size (F)	Required Amplifier g_m (S)
2	8.855×10^{-11}	2.305×10^{-4}
4	4.427×10^{-11}	2.305×10^{-4}
8	2.214×10^{-11}	2.305×10^{-4}
16	1.107×10^{-11}	2.305×10^{-4}
32	5.534×10^{-12}	2.305×10^{-4}
64	2.767×10^{-12}	2.305×10^{-4}
128	1.384×10^{-12}	2.305×10^{-4}
256	6.918×10^{-13}	2.305×10^{-4}

Where $\tau_{settling}$ is the settling time. To settle to within $\sqrt{8.14\times10^{-11}} = 9.02\times10^{-6}V_{RMS}$ over the $1.8V_{RMS}$ range of the circuit:

$$e^{\frac{-\tau_{settling}g_m}{C}} = \frac{9.02\times10^{-6}}{1.8} \tag{2.1.4}$$

$$g_m = -\frac{C\times\ln\frac{9.02\times10^{-6}}{1.8}}{\tau_{settling}} \tag{2.1.5}$$

Neglecting second order effects it appears that there is no downside to choosing a high OSR in the design of a Sigma-Delta modulator. Effects such as slew rate and switch delays will affect these problems, however. Without more complex simulation analysis it is difficult to quantify these other effects and it can only be said that these effects will exist. Therefore, a high OSR is recommended for this design.

2.2 Modulator Choice

Shown in table 2.2.1 are the major possible options that are projected based on graphs by Schreier & Temes([3], p.112-113) and lecture notes. This list is also limited to the options that are possible using the provided tools.

This list is reduced in that many of the CIFB designs are impossible to realise due to time constraints - they would require learning how to edit Simulink designs to add different quantisers and additional modulator stages. Initial attempts to edit Simulink designs were unsuccessful, therefore limiting the possibilities to third order designs with different OSRs.

It was possible to use MASH converter designs existing to meet the specifications with a lower OSR than would be required by a CIFB design. Unfortunately it has been shown in section 2.1 that this is not a first order concern - in fact, it's recommended to pick the highest possible OSR. A problem with MASH converter designs anticipated would be noise leakage([3], p.132) - due to mismatches in the transfer functions of the different stages.

An additional problem with a MASH converter design is that simulations showed it would

Table 2.2.1: A table summarising design options evaluated during the design.

Architecture	Order	OSR	Peak Nominal Observed SNDR(dB)	Notes
CIFB	3	128	109.0	Margin on specifications not high enough.
CIFB	3	256	128.1	
MASH	2+1	128	126.8	Stable, established design.
MASH	1+1+1	128	126.9	Error correcting abilities less effective than 2+1 design.

not have a completely flat audio band noise profile. This can be seen in figure 2.2 and can be compared with figure 2.2.

Originally, a 3rd order CIFB design with an OSR of 256 was chosen as the design as it was able to meet the flat audio band noise profile requirement thanks to its optimised NTF. Other advantages include it's simplicity with single-bit feedback and the anticipation of efficiency with the optimised transfer function. Unfortunately, this design proved impossible due to stability and requirements for modification in Simulink that were unsuccessful.

The second choice was a MASH 2+1 converter with an OSR of 128. Problems outlined above have been considered in the verification of the design in section 3.

2.3 Schematic

The top level functional diagram of a two stage 2+1 MASH modulator is shown in figure 2.3. This design comprises several standard blocks that can be further broken down into their circuit implementations.

2.3.1 Silva-Steensgaard Modulator

The first stage in this design is a second order modulator in a configuration known as a Silva-Steensgaard modulator. A differential circuit implementation of this circuit is shown in figure 2.3.1.

The gain elements and summing elements in this part of the design are implemented using capacitors. A differential multi-bit ADC and DAC must be implemented for this design to be created. A flash ADC implements the 2-bit ADC and an example circuit seen in figure 2.3.1 could be used to create the reference voltages if applied differentially.

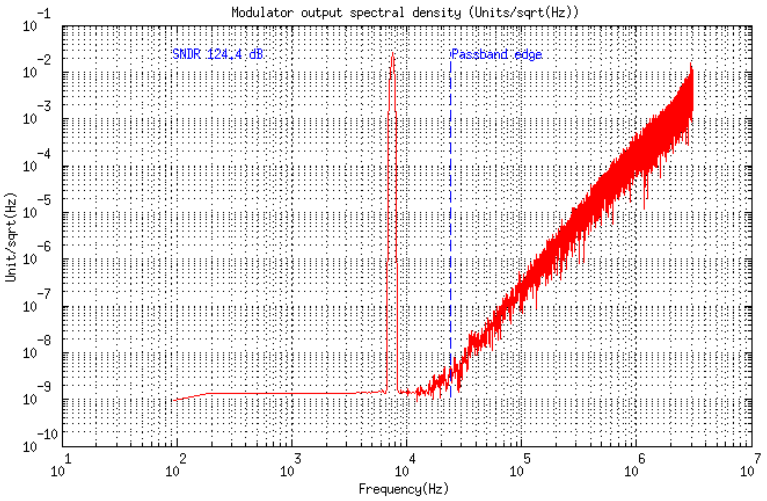

Figure 2.2.1: An example of a possible nominal MASH SNDR profile with a sine wave input.

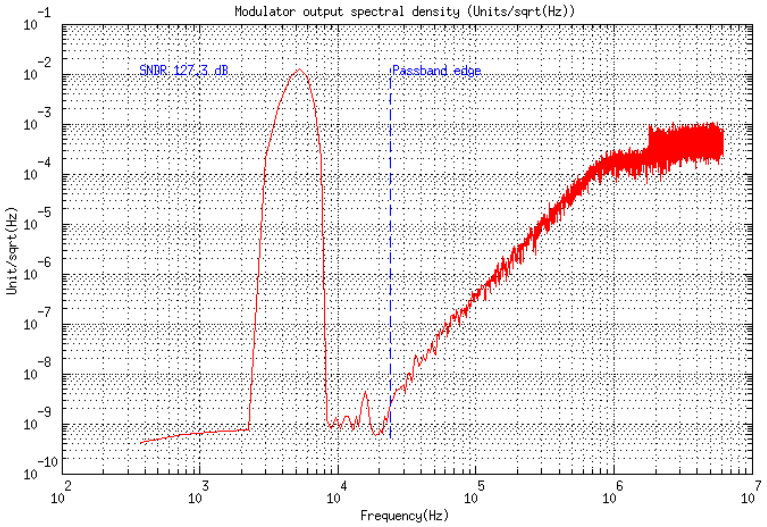

Figure 2.2.2: An example of a possible nominal CIFB SNDR profile with a sine wave input.

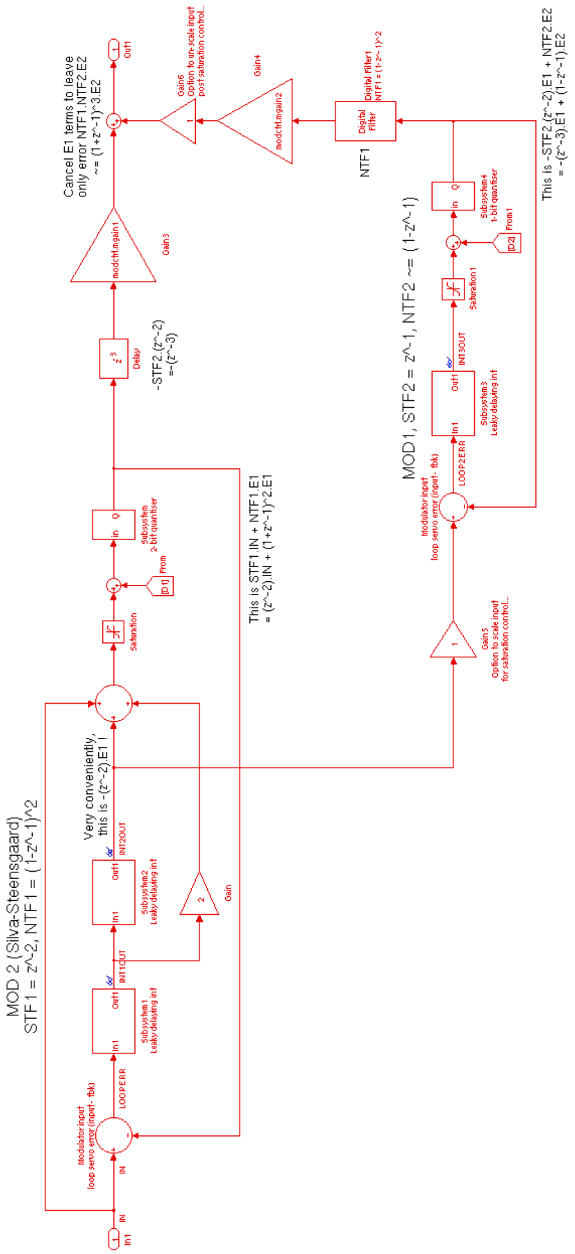

Figure 2.3.1: Top level functional block diagram of the MASH modulator chosen in this design.

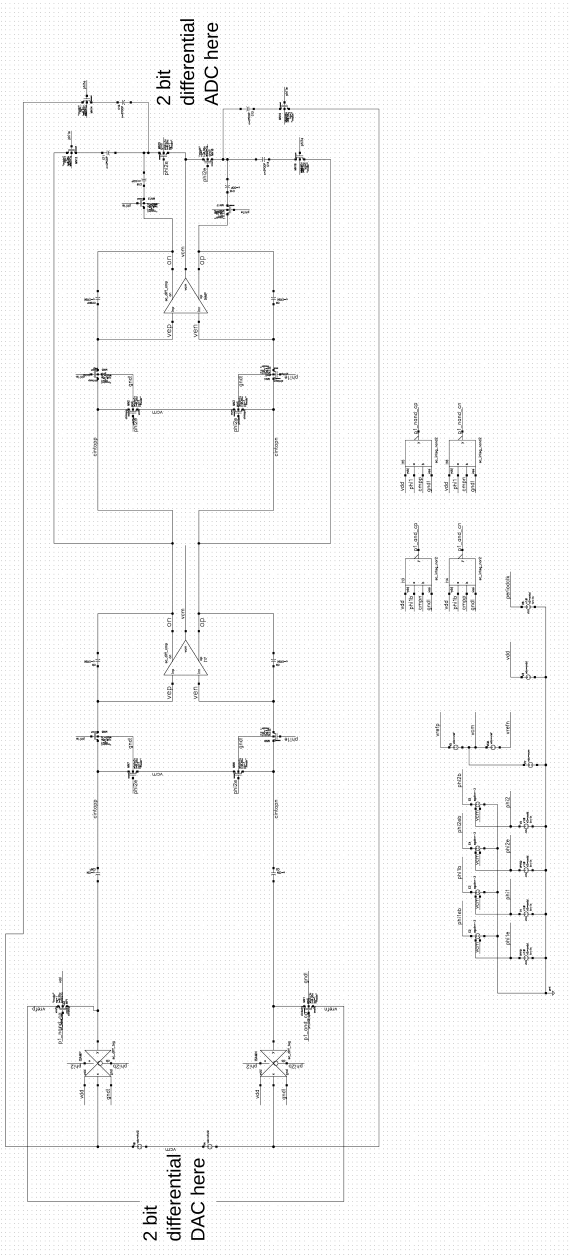

Figure 2.3.2: A differential implementation on the Silva-Steensgaard modulator.

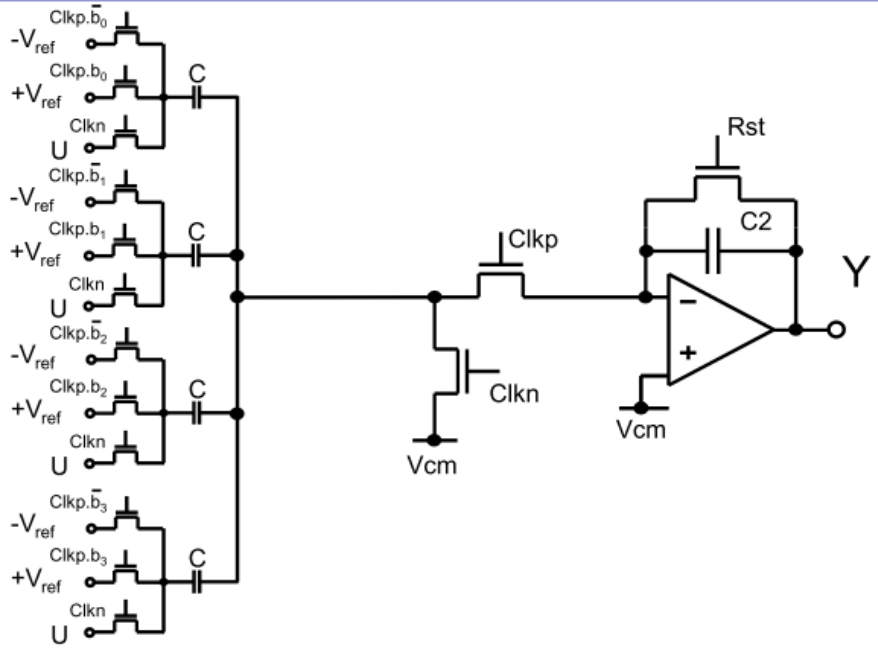

Figure 2.3.3: A multi-bit DAC switched capacitor implementation[4].

2.3.2 First Order Modulator

An example schematic for the first order modulator involved in this design is shown in figure 2.3.2. This is the second modulator in the design and is a standard differential modulator design.

A latched comparator is required to implement the single bit quantiser in the design. Designing this is a transistor level piece of design, and was not included in the design of the circuit.

2.3.3 Digital Signal Processing

The final signal processing in this modulator design is performed in the digital domain. A three cycle delay element, two gain operations and a summing element must be implemented in the digital design. This will also have to be combined with a digital filter after quantising prior to mixing.

Without any of these components in the library available to the design at this point the implementation in Cadence could not be completed. It will be demonstrated that this design will be successful upon completion.

2.4 Component Sizing

The components in the first integrator are assumed to contribute the vast majority of the noise in the design. Due to this, only the switches and capacitors in this part of the design are

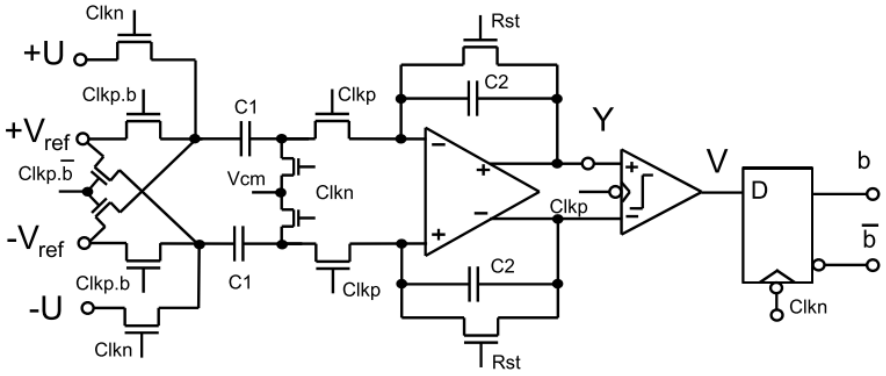

Figure 2.3.4: A differential implementation of a first order modulator[4].

considered in terms of their noise contribution. The required capacitor size for a 256 OSR and noise expectation comparable to an SQNR of 106dB is shown in table 2.1.1.

The switches in the design must also be sized - similarly to the expected g_m required for settling. Effective resistance of the switches must be designed in order that the voltage settles to within the required accuracy:

$$R_{switch} = -\frac{\tau_{settling}}{C \ln \frac{9.02\times10^{-6}}{1.8}} \tag{2.4.1}$$

This evaluates to an effective switch resistance of 4819.59Ω.

The required g_m of the amplifier contributes to the required sizing of the input devices for the amplifier - along with estimations of bias currents required. An approximate minimum bias current can be estimated by the current required to slew the entire signal range in half a settling period.

$$I = \frac{dV}{dt}C = \frac{2 \times 1.8}{4.069 \times 10^{-8}}(6.918 \times 10^{-13}) = 6.121 \times 10^{-5}A \tag{2.4.2}$$

A bias current of approximately $100\mu A$ is therefore recommended in the input amplifier. Assuming an AMS process it is therefore possible to size the input devices for the settling requirements.

$$g_m = \sqrt{\frac{2K'_p W|I_D|}{L}} \tag{2.4.3}$$

$$\frac{W}{L} = \frac{g_m^2}{2K'_p|I_D|} = \frac{(2.305 \times 10^{-4})^2}{2(14 \times 10^{-6})(100 \times 10^{-6})} = 18.975 \tag{2.4.4}$$

Where $K'_p = 14\mu A/V^2$ - assuming PMOS input devices for lower noise performance. Requirements for wider devices due to slewing or gain requirements could change this estimation, but it provides a lower bound.

The remaining components - switches and capacitors in the design - will all be sized smaller than those at the input as the input referred effect of these components will be negligible. Schreier & Temes estimate the influence of capacitors in further stages to be approximately 0.01%([2], p.441) of the input capacitor's contribution. From this, it can be estimated that capacitors of 20fF would be a safe value, and this would ease settling requirements in the circuit - switches could be up to 50 times more resistive, and therefore 50 times less wide.

2.5 Conclusion

The design of this circuit was mainly a process of choosing a modulator architecture and OSR. Initial choices failed in simulation, forcing the choice of a dependable architecture. A 2+1 MASH converter with an OSR of 128 was chosen and the sizes of the various components were estimated.

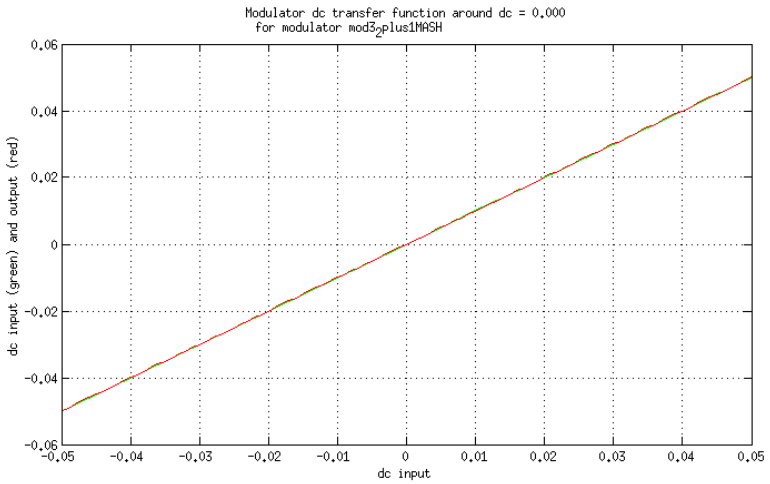

Figure 3.1.1: DC input voltage to DC output voltage for a finite gain of ...

3 Verification

3.1 DC Stability

Tones at the output of a modulator will degrade the SQNR performance of a circuit during normal operation. Also, the effects of DC inputs on the stability of the loop must also be investigated to find the input range of the modulator over which it is stable. The effect on output DC response from an input DC sweep due to finite amplifier gain is another important factor. The transient output of this modulator was inspected for various input voltages and found to be stable.

3.1.1 DC input voltage - DC output voltage

The effect of finite gain amplifiers on a design can be to cause "dead zones" to appear in the transfer function of DC input to DC output. This design is expected to be resistant to this effect as it is effectively a third order design and the width of the dead zone can be expected to be proportional to $\frac{1}{A^3}$.

The results of this design to this test are shown in figure 3.1.1. No dead zones are visible at any zoom level - the dead zones produced are smaller than the resolution of the sweep. This suggests it is likely the non-linearity will not affect the design.

3.2 DC input voltage - baseband power

A sweep of DC input voltages while monitoring the baseband power will detect tones appearing at those input voltages. The result of this test is shown in figure 3.2. This was run with saturation limits in both integrators equal to 2.546V, to reflect the signal range required of the real circuits.

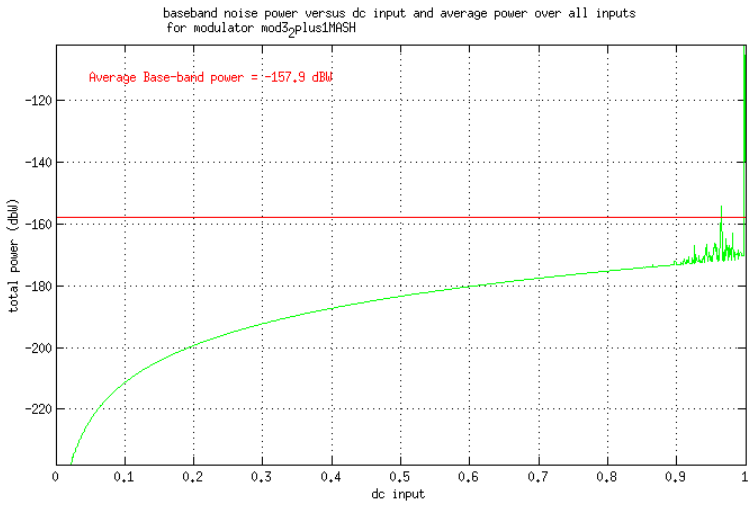

Figure 3.2.1: Nominal baseband power resulting from a sweep of DC inputs.

The baseband power never exceeds -103dB, so it can be expected that the circuit is well within specification.

3.3 SQNR Stability

To verify the performance of a Sigma-Delta modulator it's necessary to verify the resolution of the circuit at many input amplitudes and in cases involving non-ideal components. The cases tested here are:

- Capacitor mismatch
- Finite gain
- Stage mismatch
- Finite signal swing

Without mismatch, but with a finite gain of 1000 and a finite signal swing equal to that expected in the amplifier of 2.546V differential, the results of a sweep of input sine amplitudes is shown in figure 3.3.

3.3.1 Capacitor Mismatch

Capacitor mismatch causes a mismatch in the multiplication stages of the amplifier. In the matlab model there are various precise multiplication elements that can be varied. The variation expected in capacitors is 0.4%, so a variation in these values of 0.4% must be tested. For a design

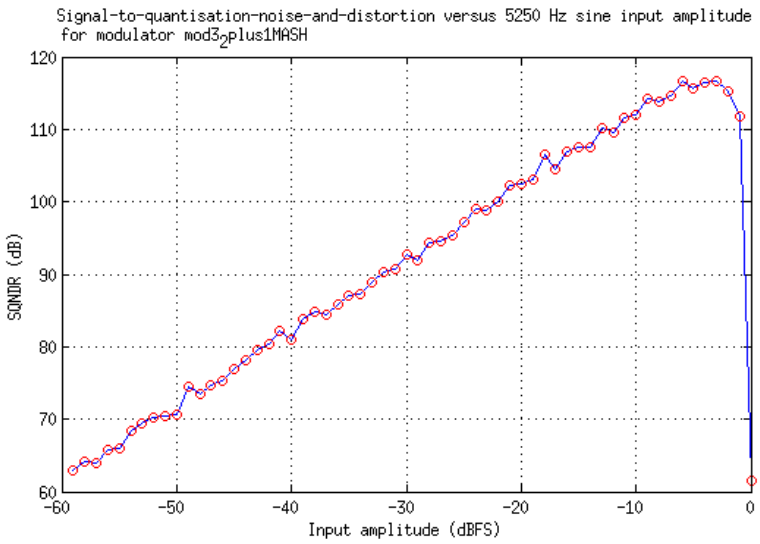

Figure 3.3.1: SQNR resulting from a sweep of different input amplitudes of a sine wave without mismatch is shown.

margin, this can be increased to 1% mismatch on the two gains to modify in the design, shown in figure 2.3.

Applying gain mismatch of 1% in all four possible configurations; the worst observed result is shown in figure 3.3.1 - swept for all input amplitudes. The worst observed was a combination of 99% mgain2 and 101% mgain1. Figure 3.3.1 shows that the circuit is still able to meet the specification.

3.3.2 Effect of Noise Leakage

Noise leakage is governed by the mismatch of transfer functions from the fist and second stages of the modulator([3], p.132). This requires modifying gain components defining the individual stages. With the worst case gains from the previous section set, these two internal gain blocks were modified by 1% mismatch to find the worst combination. The result is shown in a sweep of all input amplitudes in figure 3.3.2.

3.4 Cadence Tests

To show that the sizing of devices in section 2.4 is correct the modulator should be simulated to show that the input referred noise is as low as expected. Unfortunately, the full modulator was not implemented in Cadence, making this full simulation impossible. To prove that the sizing is adequate a first order modulator noise simulation was performed with the input capacitor and g_m sizing calculated applied.

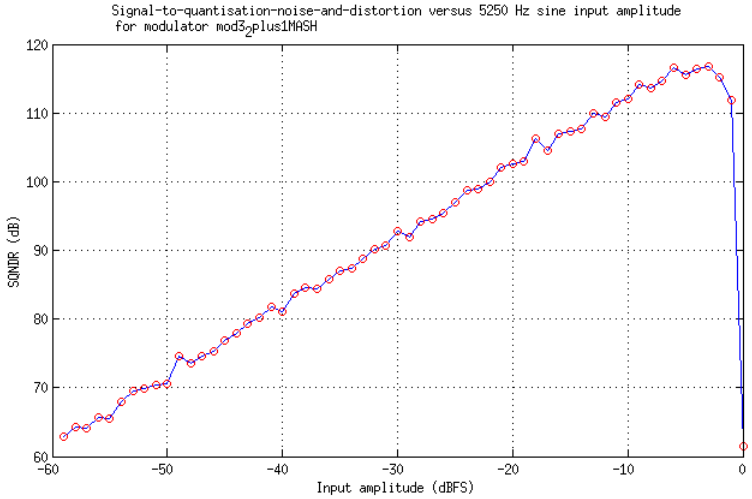

Figure 3.3.2: SQNR resulting from a sweep of different input amplitudes of a sine wave with capacitor mismatch is shown.

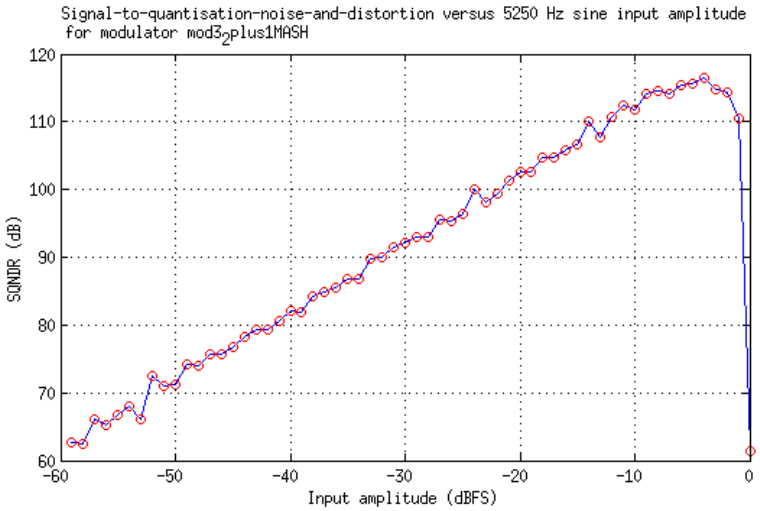

Figure 3.3.3: SQNR resulting from a sweep of different input amplitudes of a sine wave with transfer function mismatch is shown.

First order calculations proved to be inaccurate at this point and it was necessary to further increase the size of the input capacitors to meet the noise requirements.

3.5 Conclusion

Although a full simulation of a macro-model implementation of the modulator has not been completed, the simulation results presented here show that this circuit is capable of meeting the specifications as described. Non-ideal effects have been considered in the matlab simulations and noise has been investigated in the Cadence simulations. From these results the circuit can be expected to work if completed.

4 Conclusion

This design exercise has resulted in a delta-sigma modulator design that is very likely to be succesful. It is expected that this modulator is able to meet the required SNDR specification. Also, implementation and non-ideal component implications have been taken into account.

References

[1] Henderson R. Sigma-Delta Data Converters - Lecture 8. Edinburgh: University of Edinburgh; 2013.

[2] Steensgaard J, Silva J, Schreier R, Temes GC. Noise in Switched-Capacitor Delta-Sigma Data Converters. In: Understanding Sigma-Delta Data Converters. Wiley; 2004. .

[3] Schreier R, Temes GC. Higher-Order Delta-Sigma Modulation. In: Understanding Sigma-Delta Data Converters. Wiley; 2004. .

[4] Henderson R. Sigma-Delta Data Converters - Lecture 7. Edinburgh: University of Edinburgh; 2013.