ECE1388 VLSI Design Methodology

Lecture 4: Non-ideal Transistors

Adapted from Weste, Harris CMOS VLSI Design

Outline

- Transistor I-V Review
- Non-ideal Transistor Behavior
  - Velocity Saturation
  - Channel Length Modulation
  - Body Effect
  - Leakage
  - Temperature Sensitivity
- Process and Environmental Variations
  - Process Corners

Ideal Transistor I-V

- *Shockley* 1st order transistor models

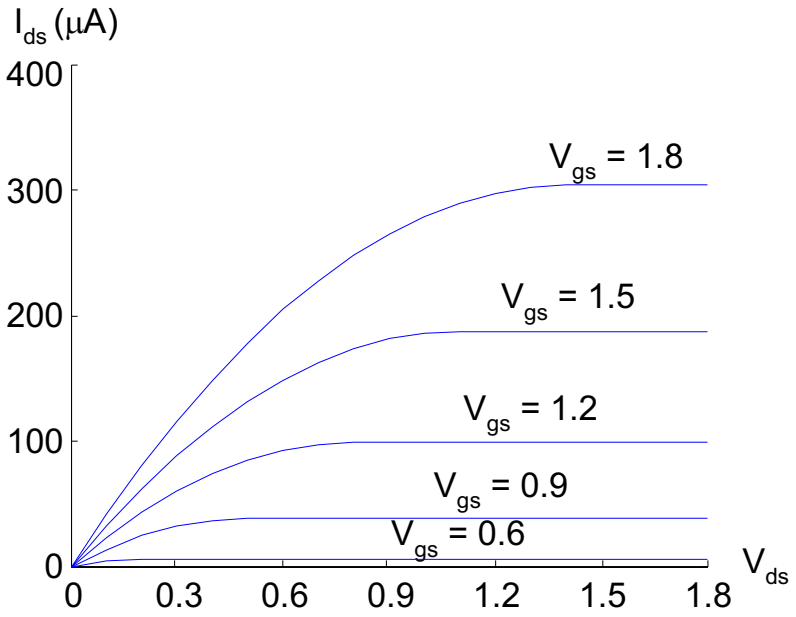
$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

- Recall: these can be derived by answering the questions:
  - How much charge $Q_{channel}$ is in the channel
  - How much time *t* each carrier takes to cross

  $I_{ds} = Q_{channel} / t$

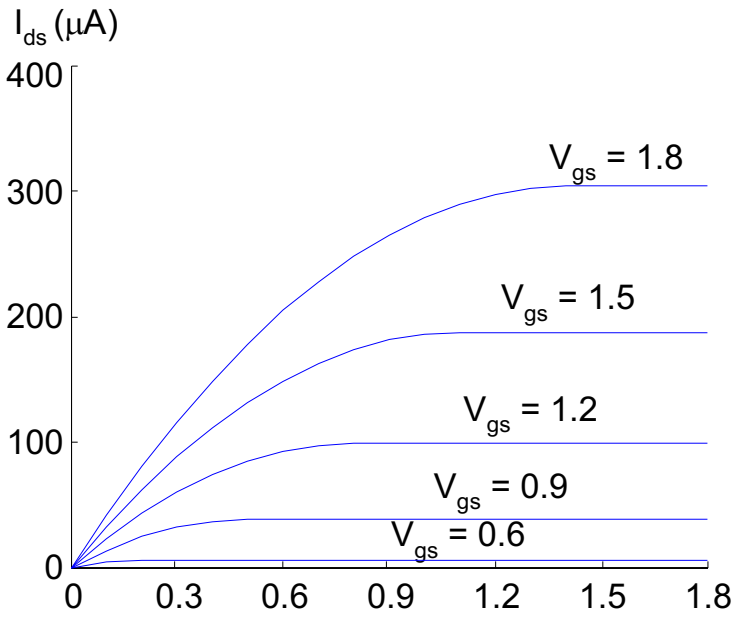
Ideal nMOS I-V Plot

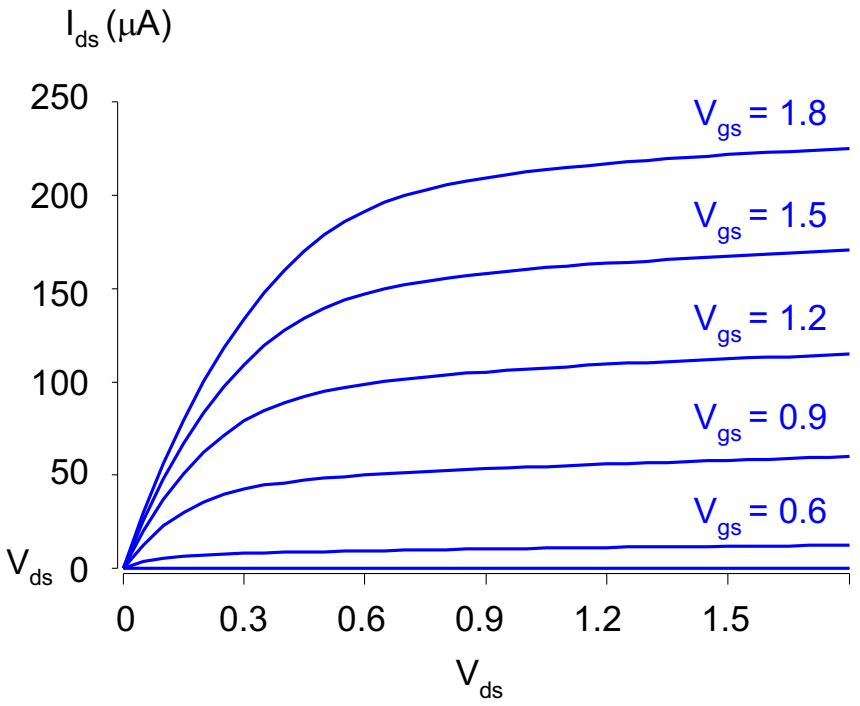
- 180 nm TSMC process
- Ideal model
  - $\beta = 155(W/L)\ \mu A/V^2$
  - $V_t = 0.4$ V
  - $V_{DD} = 1.8$ V



Ideal vs Simulated nMOS

- 180 nm TSMC process
- Ideal model
  - $\beta = 155(W/L)\ \mu A/V^2$
  - $V_t = 0.4$ V
  - $V_{DD} = 1.8$ V
- BSIM 3v3 SPICE models
- What differs?





Ideal vs Simulated nMOS

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  - $V_t = 0.4$ V
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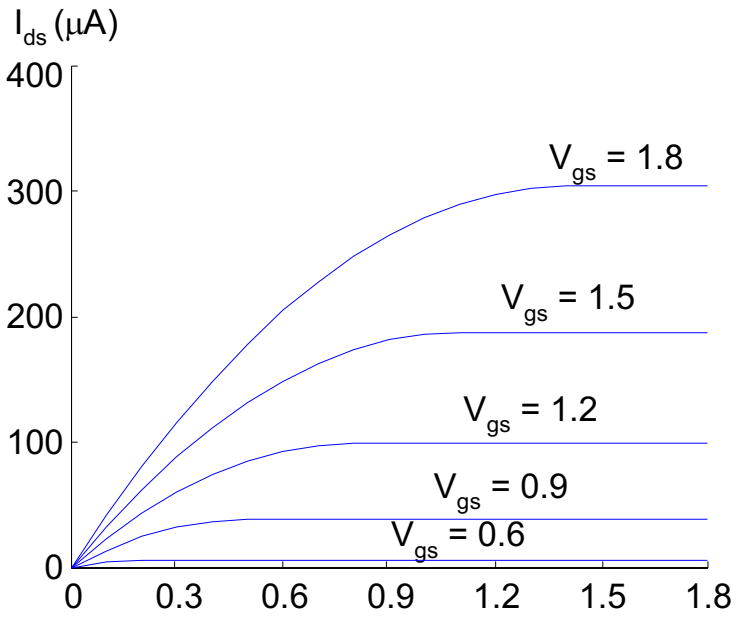
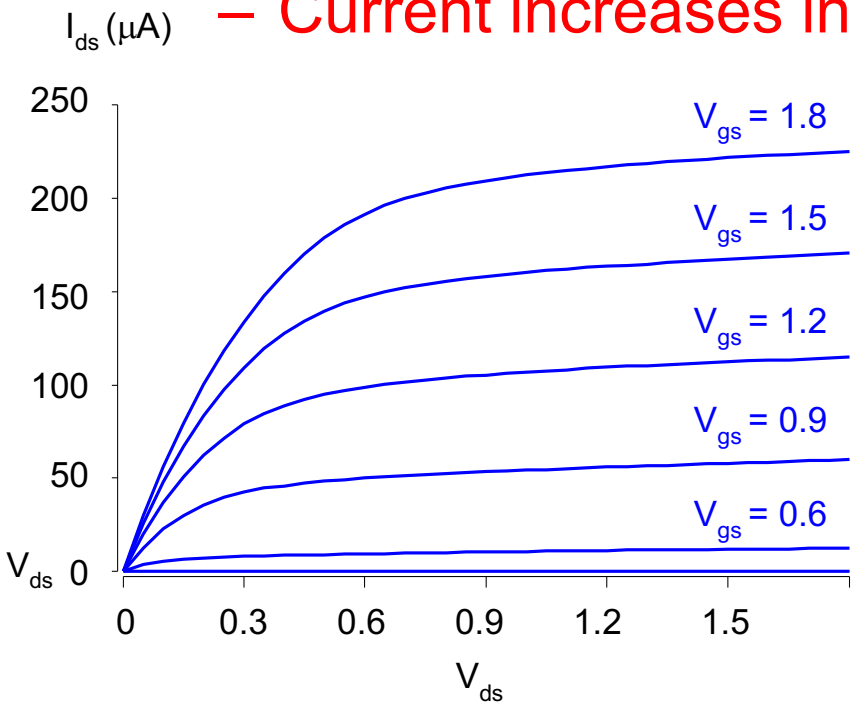
- BSIM 3v3 SPICE models
- What differs?
  - Less ON current
  - No square law
  - Current increases in sat

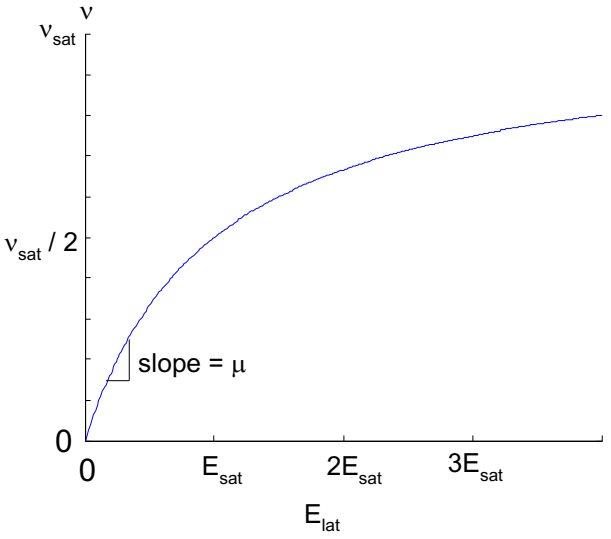




Velocity Saturation

- We assumed carrier velocity is proportional to E-field
  - $v = \mu E_{lat} = \mu V_{ds}/L$
- At high fields, this ceases to be true
  - Carriers scatter off atoms
  - Velocity reaches v_{sat}
    - Electrons: 6-10 x 10^6 cm/s
    - Holes: 4-8 x 10^6 cm/s
  - Better model

$$v = \frac{\mu E_{lat}}{1 + \frac{E_{lat}}{E_{sat}}} \Rightarrow v_{sat} = \mu E_{sat}$$



Vel Sat I-V Effects

- Ideal transistor ON current increases with V^2

$$I_{ds} = \mu C_{\text{ox}} \frac{W}{L} \frac{\left(V_{gs} - V_t\right)^2}{2} = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

- Velocity-saturated ON current increases with V

$$I_{ds} = C_{\text{ox}} W \left(V_{gs} - V_t\right) v_{sat}$$

- Real transistors are partially velocity saturated
  - Approximate with α-power law model
  - $I_{ds} \propto V^{\alpha}$
  - $1 < \alpha < 2$ determined empirically

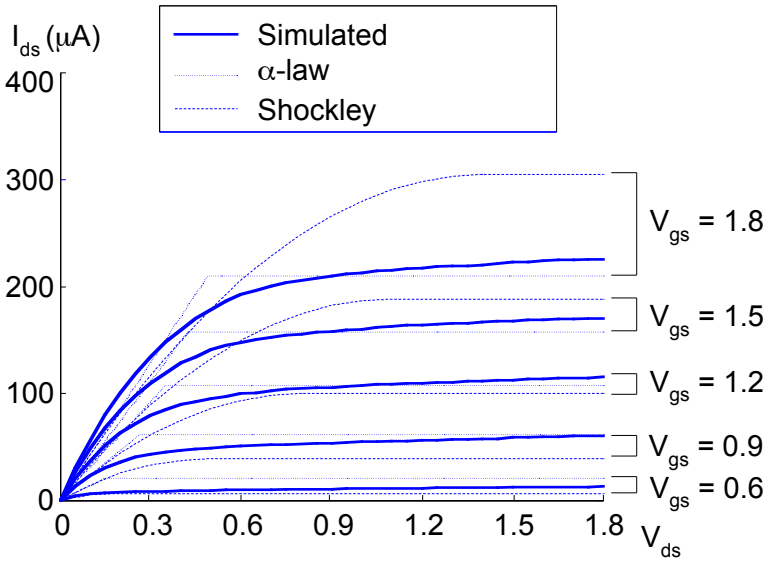
α-Power Model

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ I_{dsat}\dfrac{V_{ds}}{V_{dsat}} & V_{ds} < V_{dsat} \quad \text{linear} \\ I_{dsat} & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

$$I_{dsat} = P_c \frac{\beta}{2}\left(V_{gs} - V_t\right)^{\alpha}$$

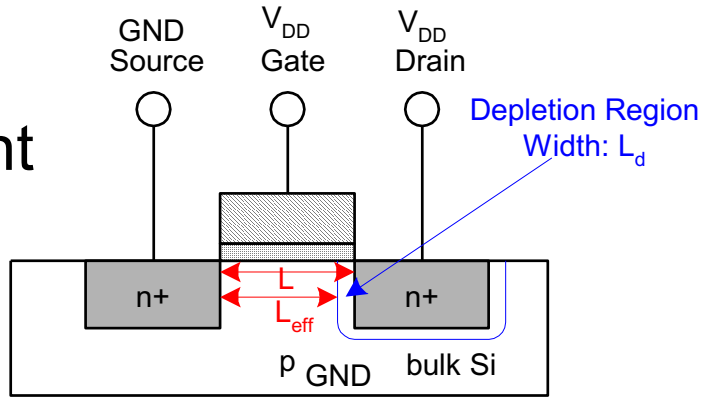
$$V_{dsat} = P_v \left(V_{gs} - V_t\right)^{\alpha/2}$$

$$\alpha, \beta P_c, P_v - \textit{parameters}$$

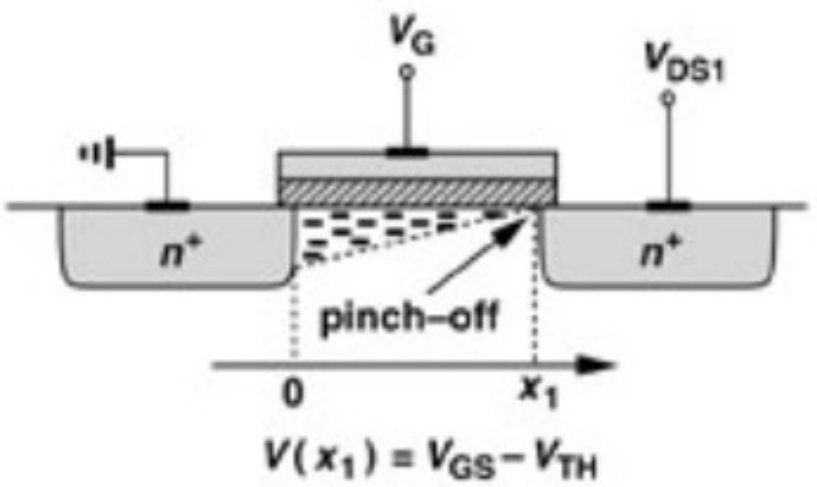


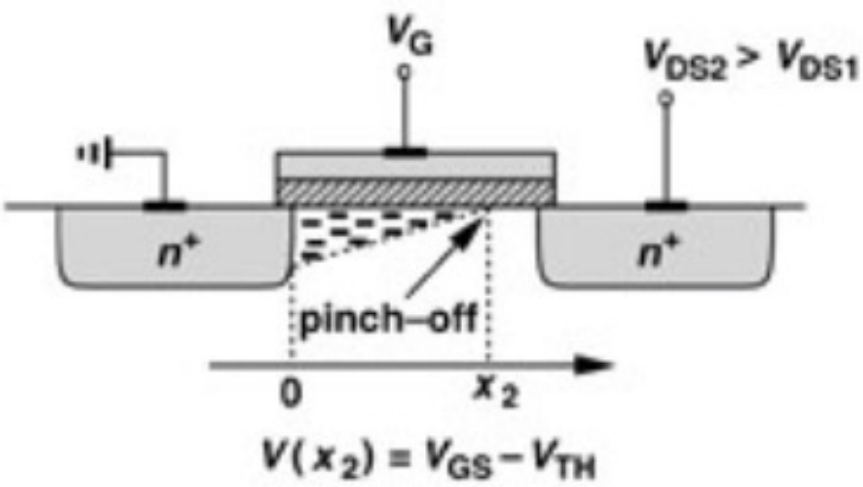
Channel Length Modulation

- Reverse-biased p-n junctions form a *depletion region*
  - Region between n and p with no carriers
  - Width of depletion L_d region grows with reverse bias
  - $L_{eff} = L - L_d$
- Shorter L_{eff} gives more current
  - I_{ds} increases with V_{ds}
  - Even in saturation



Chan Length Modulation I-V

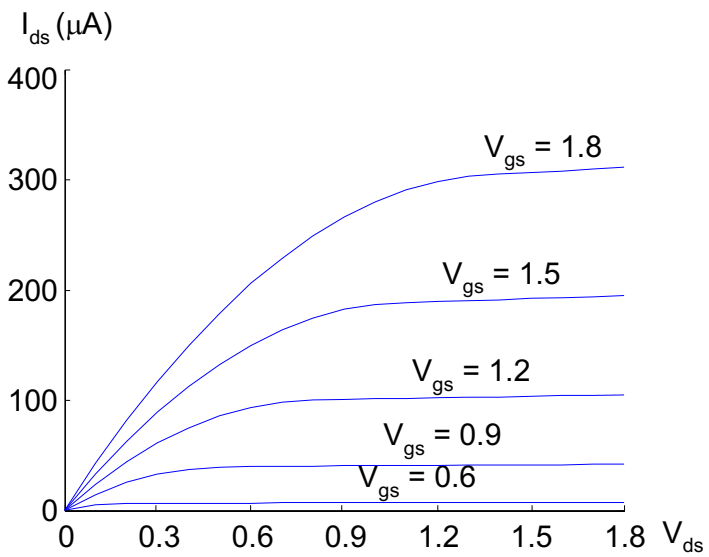




- wider drain depletion → shorter channel
- but same voltage across it → higher I_{ds}

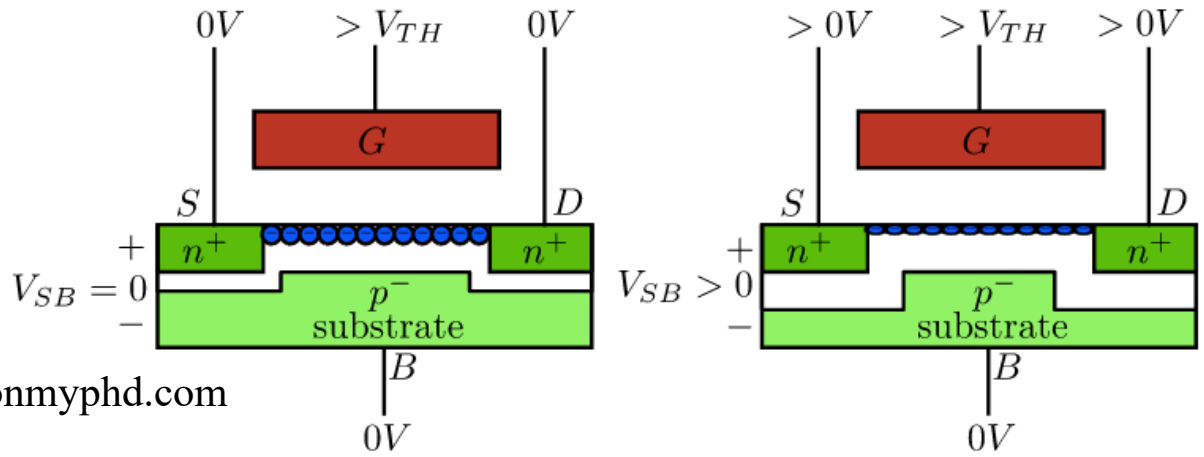
$$I_{ds} = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2\left(1 + \lambda V_{ds}\right)$$

- *λ-channel length modulation coeff.*
  - empirically fit to I-V characteristics
  - not the same as the feature size



Body Effect

- V_t increases if source voltage increases wrt bulk:
  - the source is connected to the channel
  - thus the depletion region surrounding them thickens
    - more electrons in the substrate are attracted towards the channel and recombine resulting in more depletion layer bound charge
  - this reduces the channel depth
  - and higher Vg is needed to make channel deeper
- Increase in V_t with V_s is called the *body effect*
- A.k.a. back-gate effect (10-20% effect of the front gate)



Body Effect Model

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

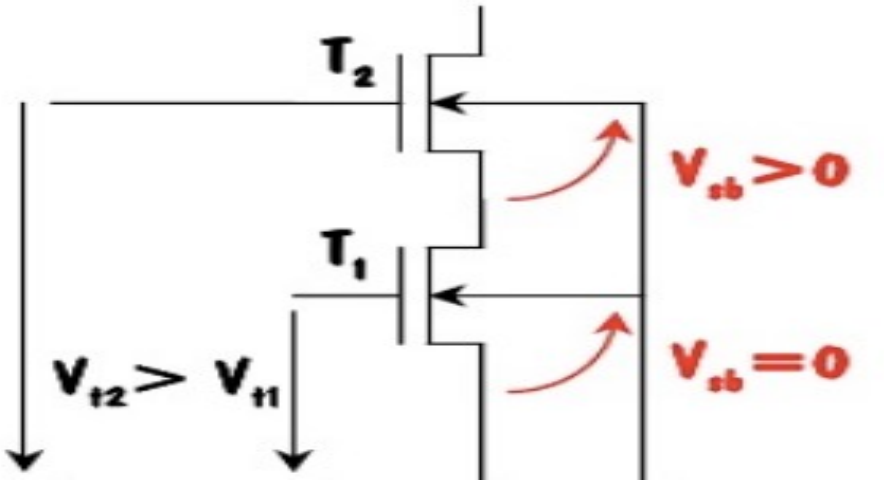
- ϕ_s = *surface potential* at threshold

$$\phi_s = 2v_T \ln\frac{N_A}{n_i}$$

  - depends on doping level N_A
  - and intrinsic carrier concentration n_i

- γ = *body effect coefficient*

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si}N_A} = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

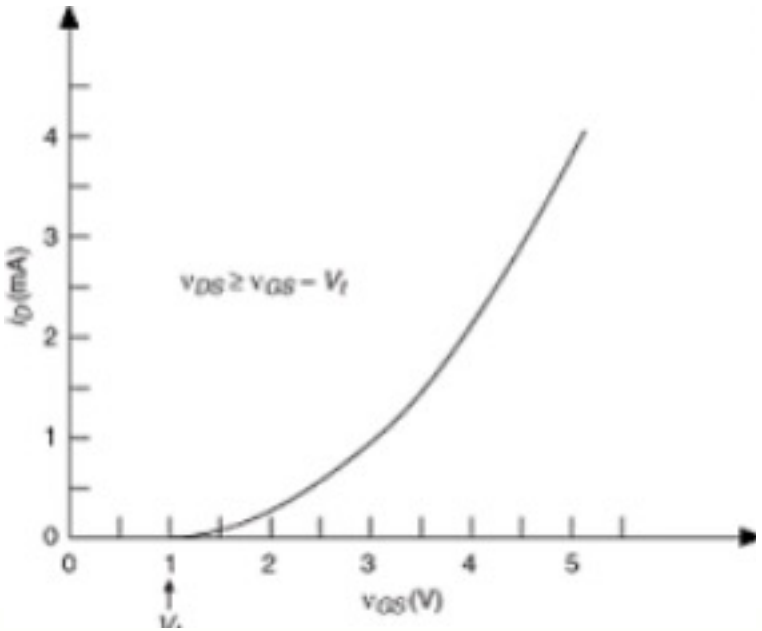


Dr. Jacomet notes, slide share

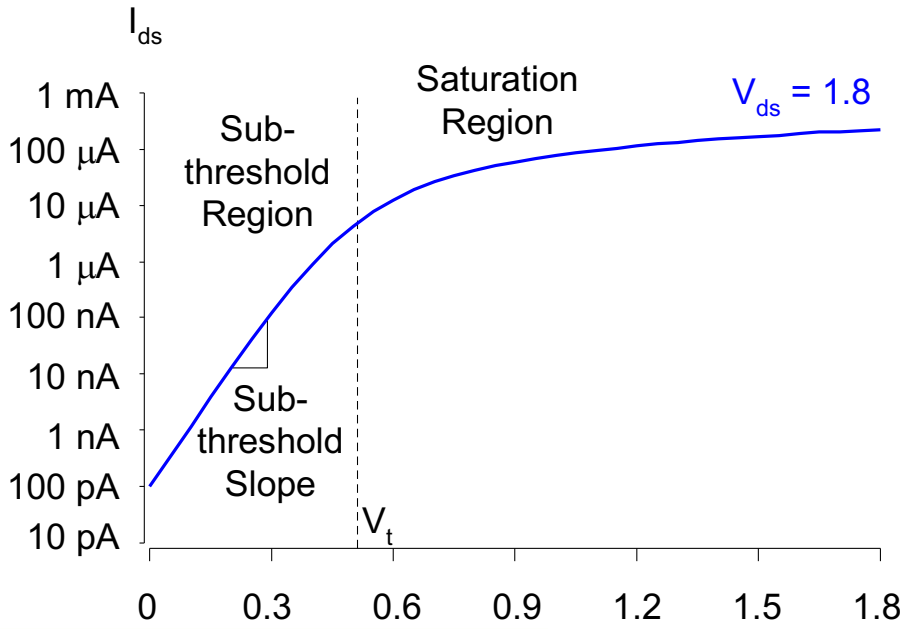
Leakage Sources

- Subthreshold conduction
  - Transistors can't abruptly turn ON or OFF
- Junction leakage
  - Reverse-biased PN junction diode current
- Gate leakage
  - Tunneling through ultrathin gate dielectric
- Other (not covered in detail)
  - *Eg, Below 50nm: gate-induced drain leakage (tunneling-based leakage where gate overlaps drain)*
  - *Punchthrough, etc*
- Subthreshold leakage used to be the biggest source in modern transistors
- In modern processes, gate leakage is often significant

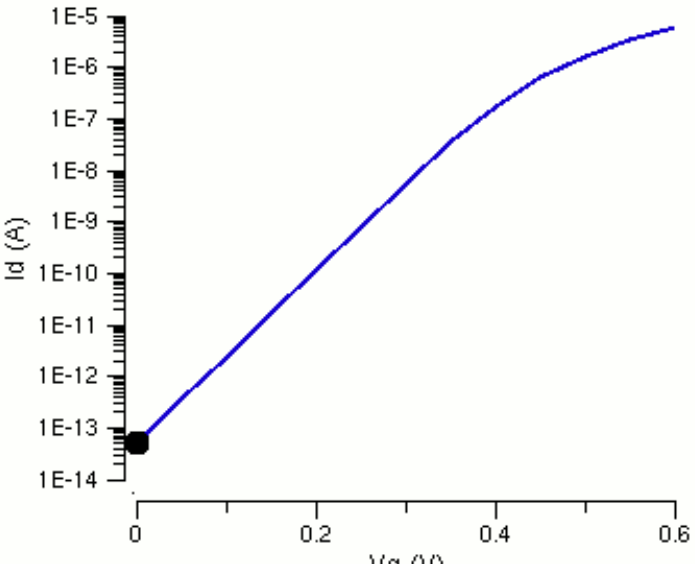
OFF Transistor Behavior

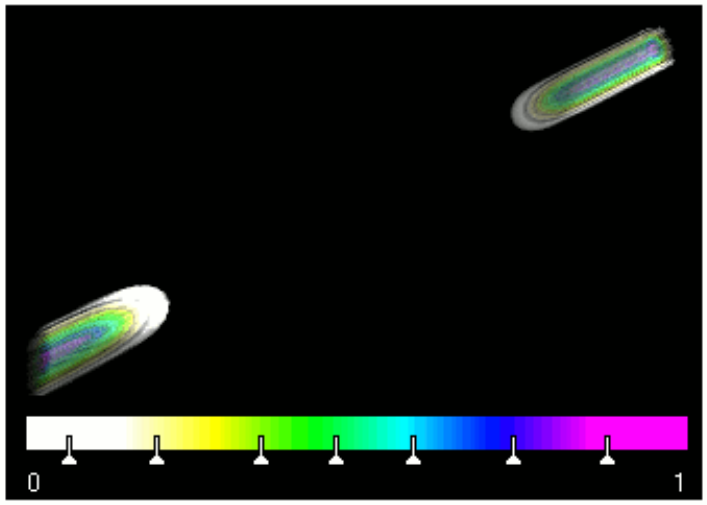


Id-Vg Characteristics



3D electron density for Vd=0.6





electron density for = 1-Vd=0.6V-Vg=0V

Wikipedia

- Current doesn't go to 0 in cutoff
- Simulation of electron density in a nanowire MOSFET. Vt=0.45 V

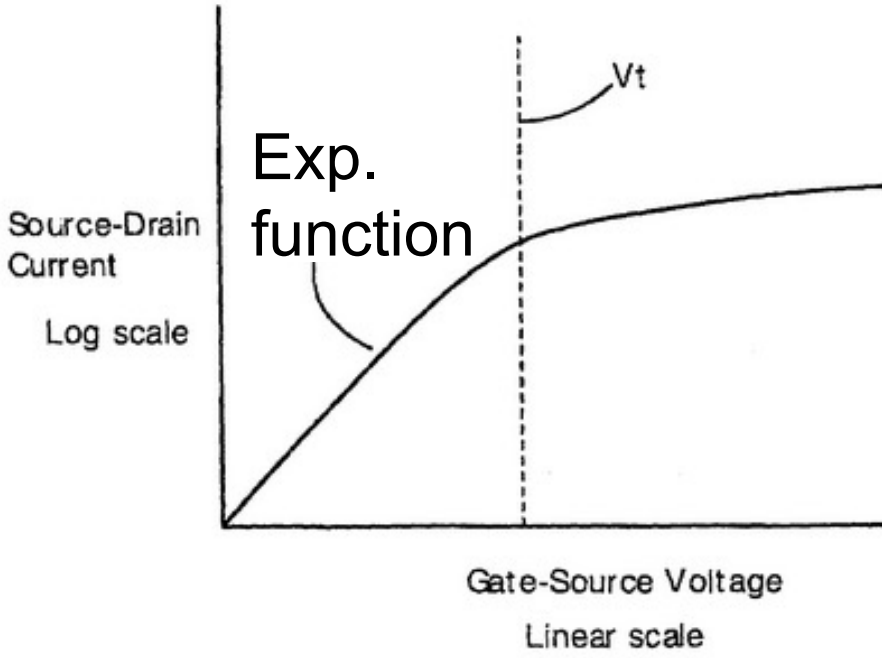
Subthreshold Leakage

- Subthreshold leakage exponential with V_{gs}

$$I_{ds} = I_{ds0} e^{\frac{V_{gs} - V_t}{n v_T}} \left(1 - e^{\frac{-V_{ds}}{v_T}} \right)$$

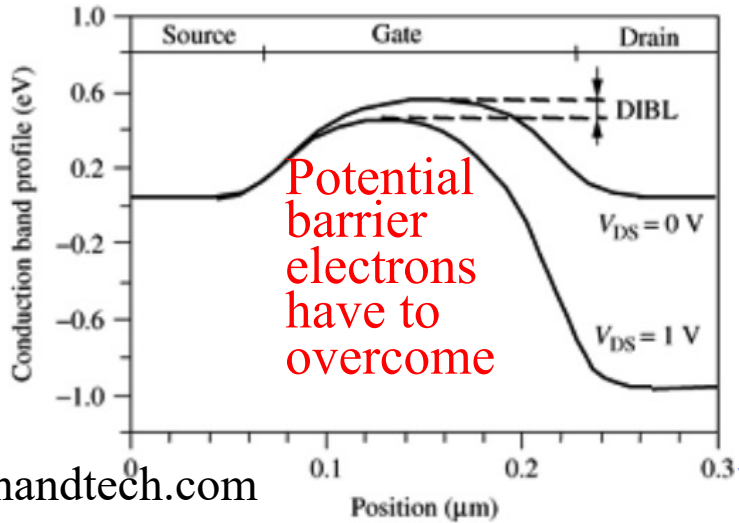
$$I_{ds0} = \beta v_T^2 e^{1.8}$$

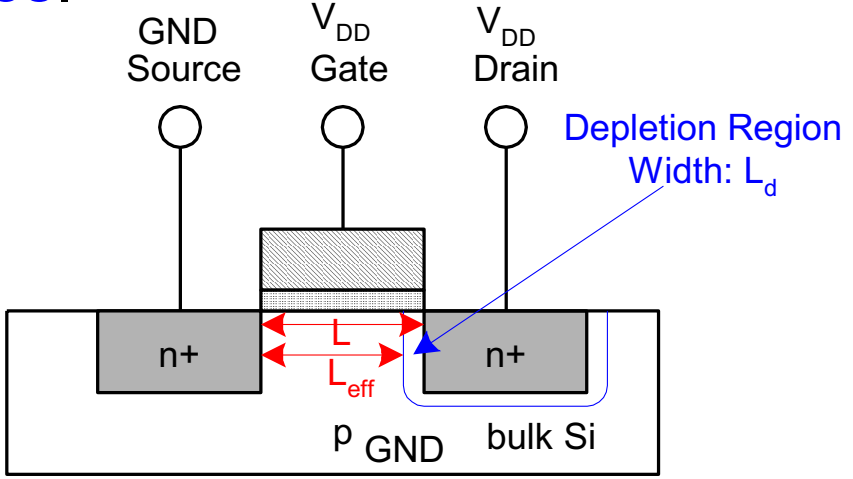
- n is process dependent,
  - typically 1.4-1.5



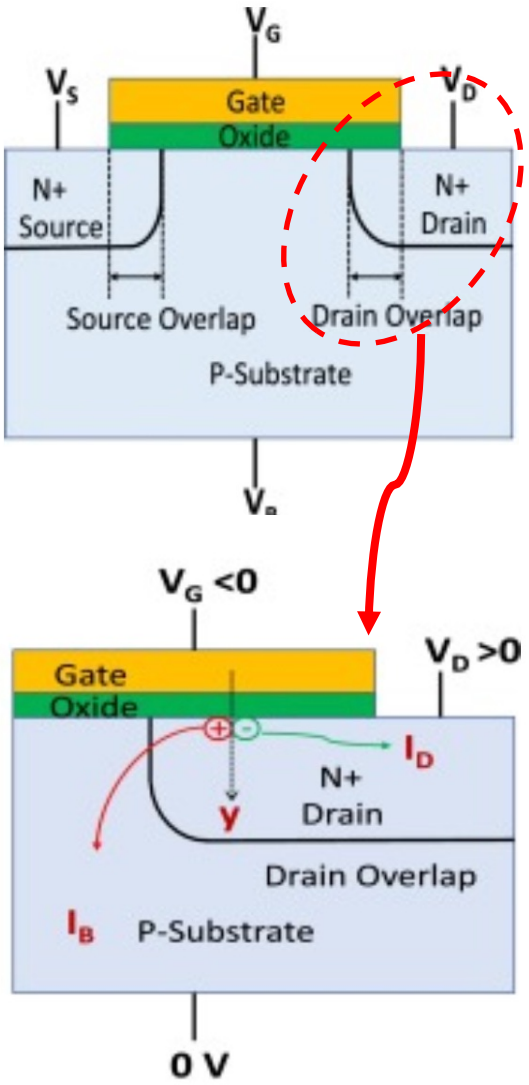
Drain-Induced Barrier Lowering (DIBL)

- As Vd increases, the depletion region of the drain *pn*-junction widens and extends under gate
- The drain assumes a greater portion of the burden of balancing under-gate depletion region charge, leaving a smaller burden for the gate
- The gate attracts more electrons into the channel
  - *i.e.*, the potential barrier for electrons is lowered.
- Modeled as decrease in V_t: $V_t' = V_t - \eta V_{ds}$
  - subthreshold leakage increases.





Gate-Induced Drain Leakage (GIDL)



- In deep subthreshold Vgs<0
- Large negative Vgd for Vd>0
  - Causes current from D to Bulk
  - Called GIDL
- Nature of this current:
  - Large depletion under G-D overlap
  - High vertical E-field
  - Valence band electrons tunnel into the conduction band
  - This results in the formation of electron-hole pairs
  - Contribute to OFF leakage current

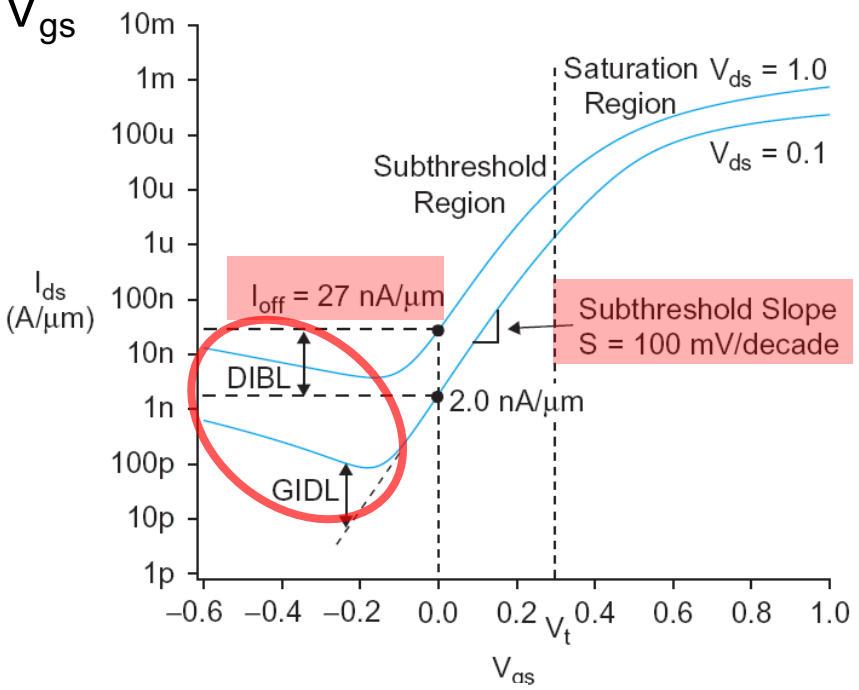
S.K. Kurinec, in Encyclopedia of Materials: Science and Technology, 2001

Subthreshold Leakage

- Subthreshold leakage exponential with V_{gs}

$$I_{ds} = I_{ds0} e^{\frac{V_{gs} - V_{t0} + \eta V_{ds} - k_\gamma V_{sb}}{n v_T}} \left(1 - e^{\frac{-V_{ds}}{v_T}}\right)$$

- n is process dependent
  - typically 1.3-1.7



- Rewrite relative to I_{off} on log scale

$$I_{ds} = I_{off} 10^{\frac{V_{gs} + \eta(V_{ds} - V_{dd}) - k\gamma V_{sb}}{S}} \left(1 - e^{\frac{-V_{ds}}{v_t}}\right)$$

$$S = \left[\frac{d\left(\log_{10} I_{ds}\right)}{dV_{gs}}\right]^{-1} = n v_T \ln 10$$

- S ≈ 100 mV/decade @ room temperature

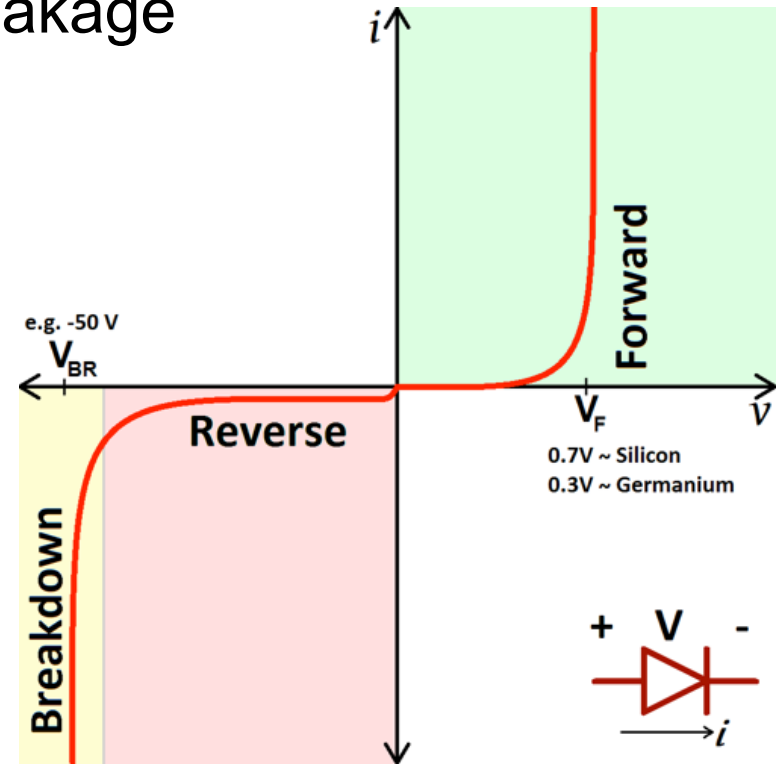
DIBL: Drain-Induced Barrier Lowering
GIDL: Gate-Induced Drain Leakage

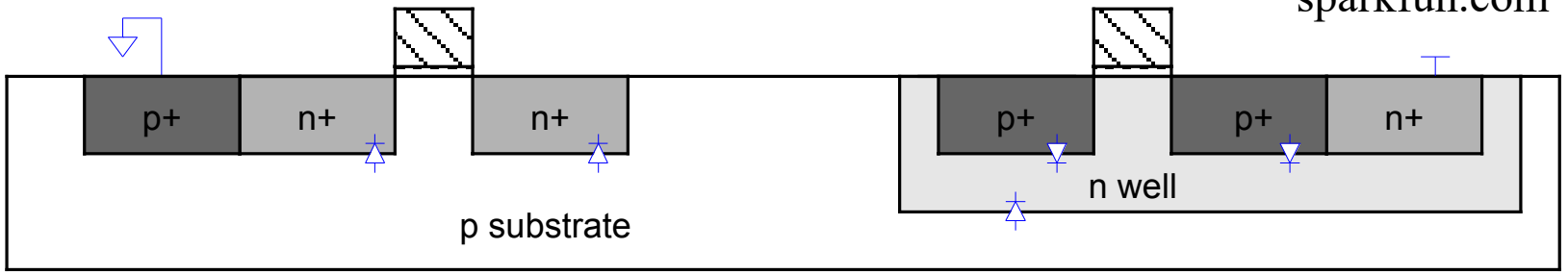
Junction Leakage

- Reverse-biased pn-junctions has leakage

$$I_D = I_S\left(e^{\frac{V_D}{v_T}} - 1\right)$$

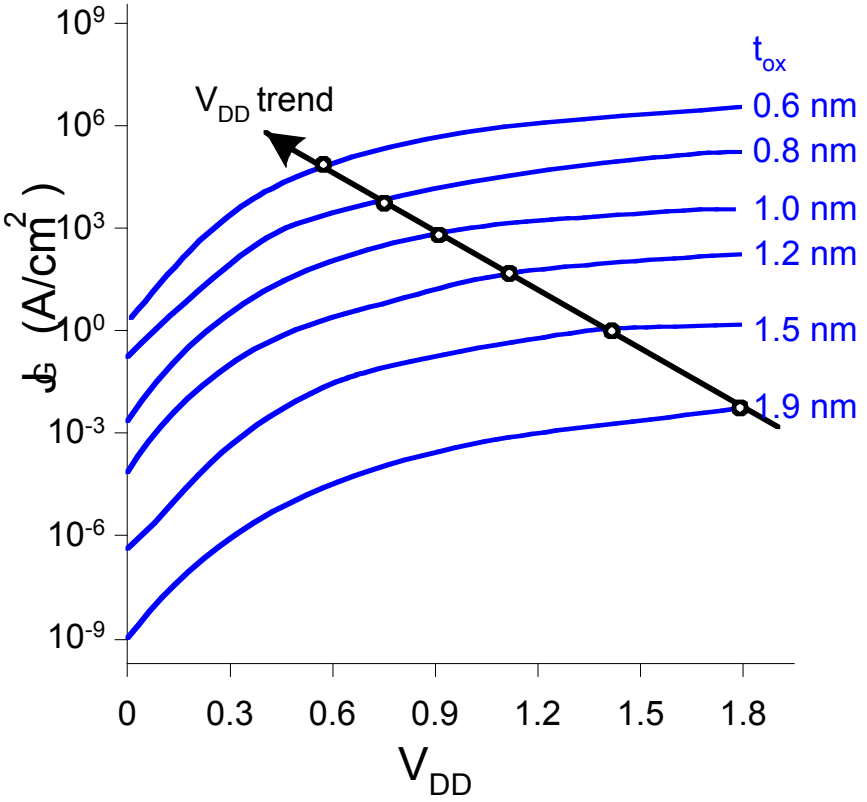
- I_s depends on
  - doping levels and
  - area and
  - perimeter of diffusion regions
  - Typically < 1 fA/μm²



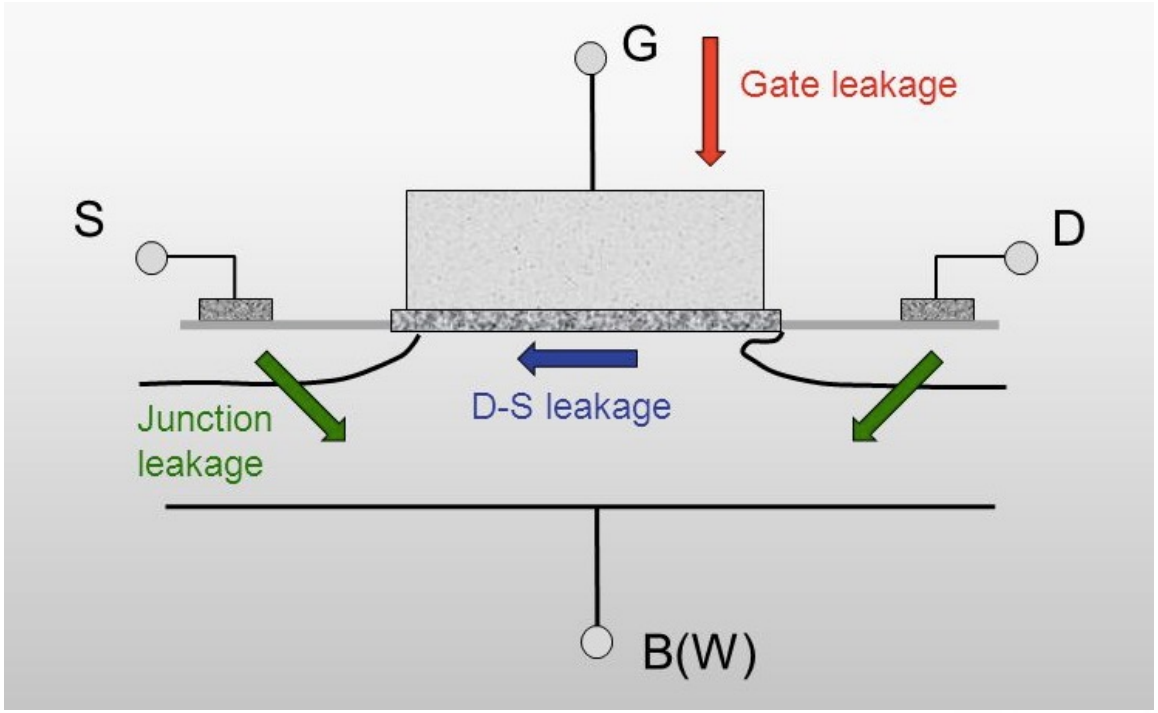


Gate Leakage

- Carriers may tunnel thorough very thin gate oxides
- Predicted tunneling current (from [Song01])
- Negligible for older processes
- Becoming critically important



Leaky nMOS Switch



Three main leakage phenomena

Prof. J. Rabaey. U. Berkeley class notes 2008

Three main phenomena

plus additional types of leakage

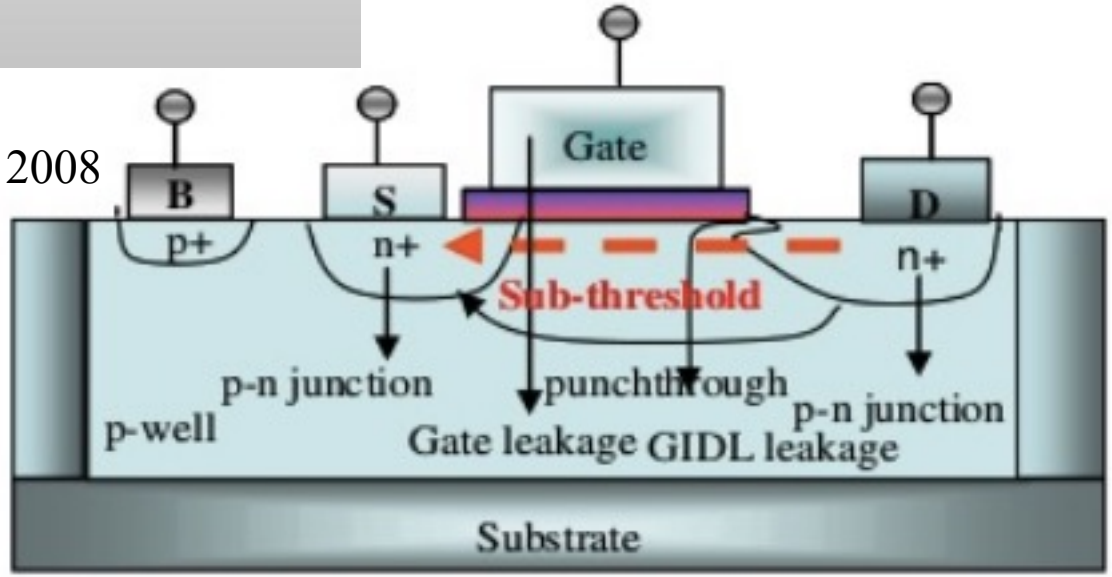


Fig. by Dr. S.D. Pabale

The Ideal MOS Transistor

Fully Surrounding Metal Electrode

Fully Enclosed, Depleted Semiconductor

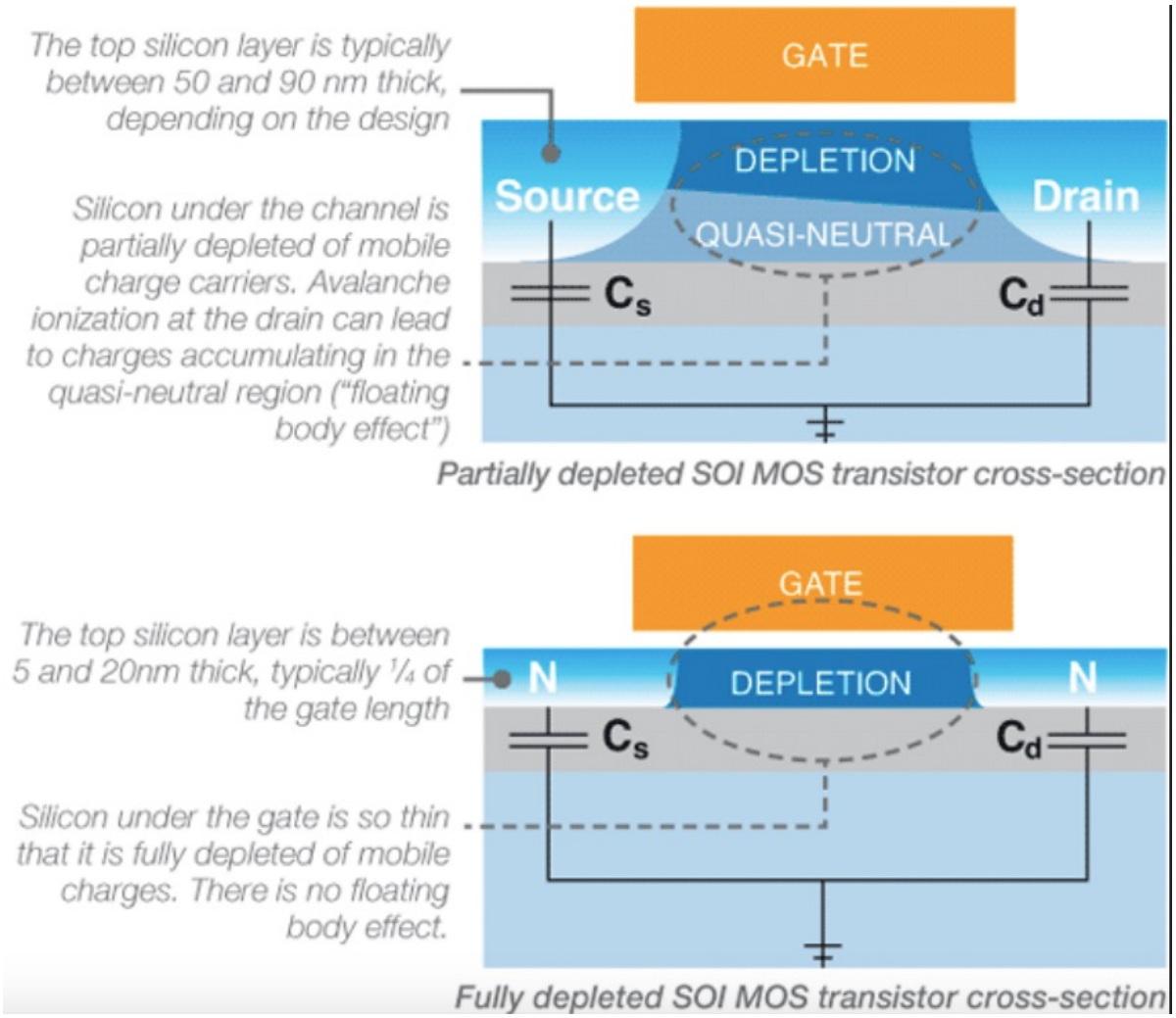
High-K Gate Insulator

Low Resistance Source/Drain

Band Engineered Semiconductor

From My Files

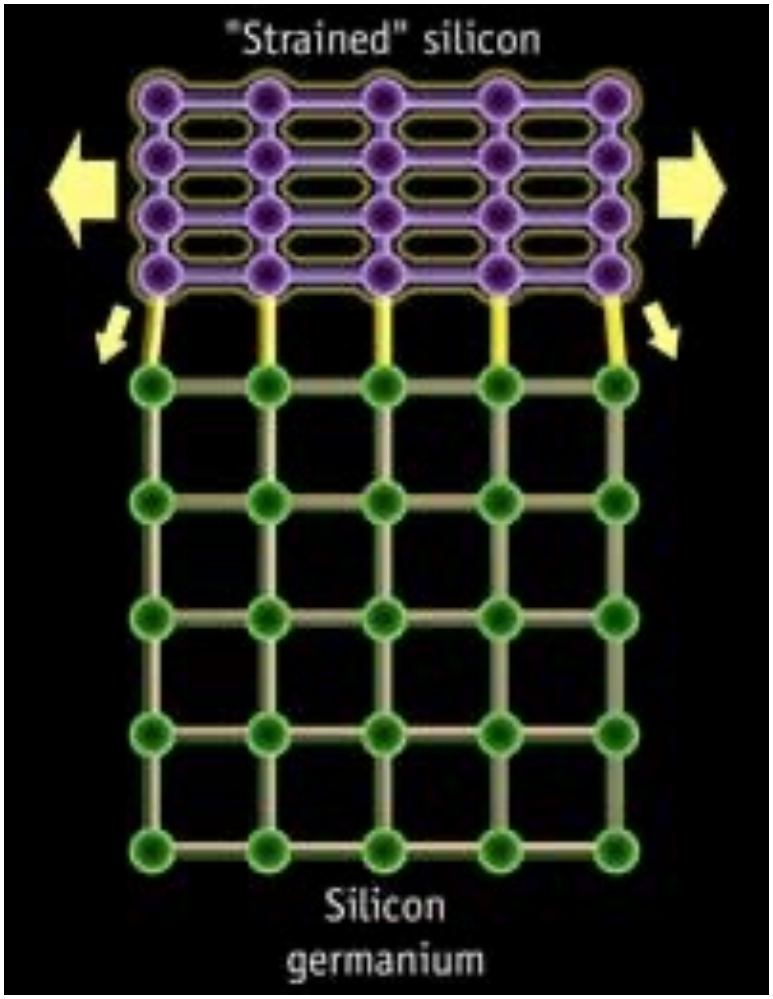
Silicon-on-Insulator (SOI)



- Available since late 1990s
- Less parasitic capacitance
- Less leakage "far away from gate"
- PD-SOI - the bulk of Si isn't connected to a terminal the body "floats" – use FDSOI
  - history effect
- Expensive and used in niche applications
  - RF and space

https://www.anandtech.com/show/8223/an-introduction-to-semiconductor-physics-technology-and-industry/5

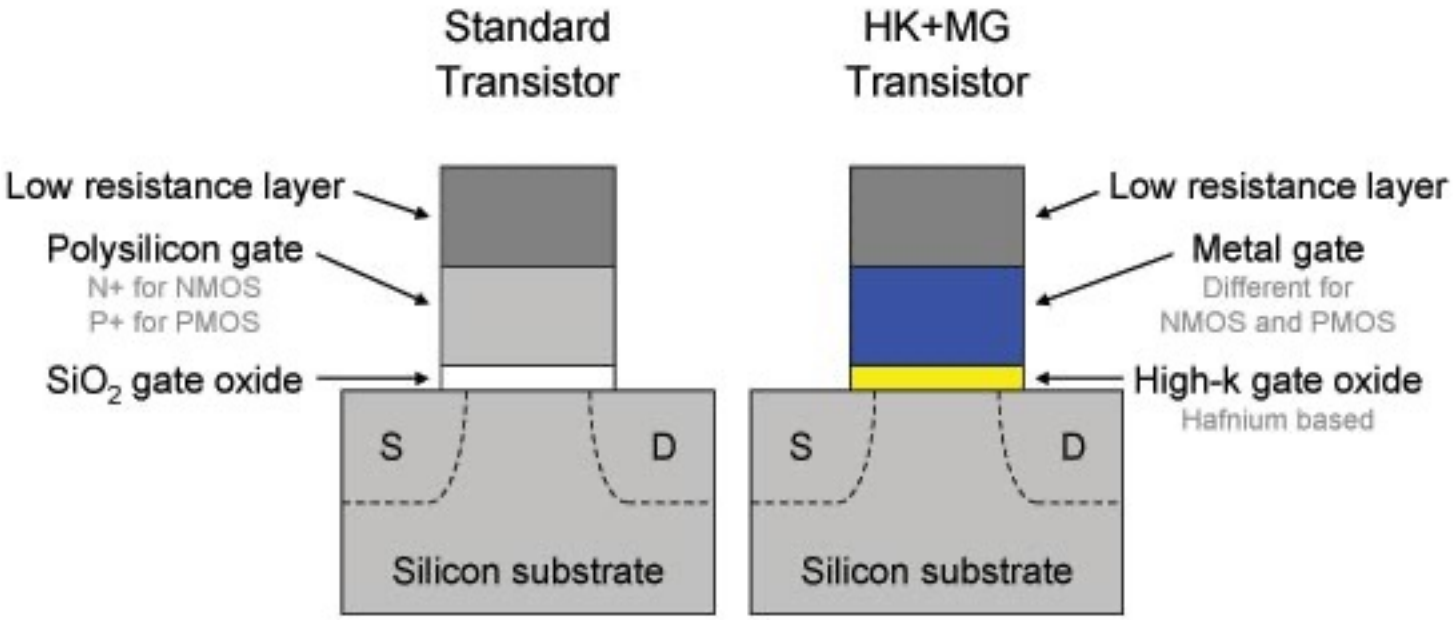
Strained Silicon



- Introduced as early as 2003
  - Intel's 90nm process
- Use silicone germanium (SiGe) or silicon carbide (SiC) in the source and drain)
- Silicon in the channel is stretched past its normal interatomic distance and reduces the effects of electrostatic forces
  - strained silicon
- This increases the mobility of charge carriers in the channel
  - increasing drive current and
  - overall transistor performance

https://www.anandtech.com/show/8223/an-introduction-to-semiconductor-physics-technology-and-industry/5

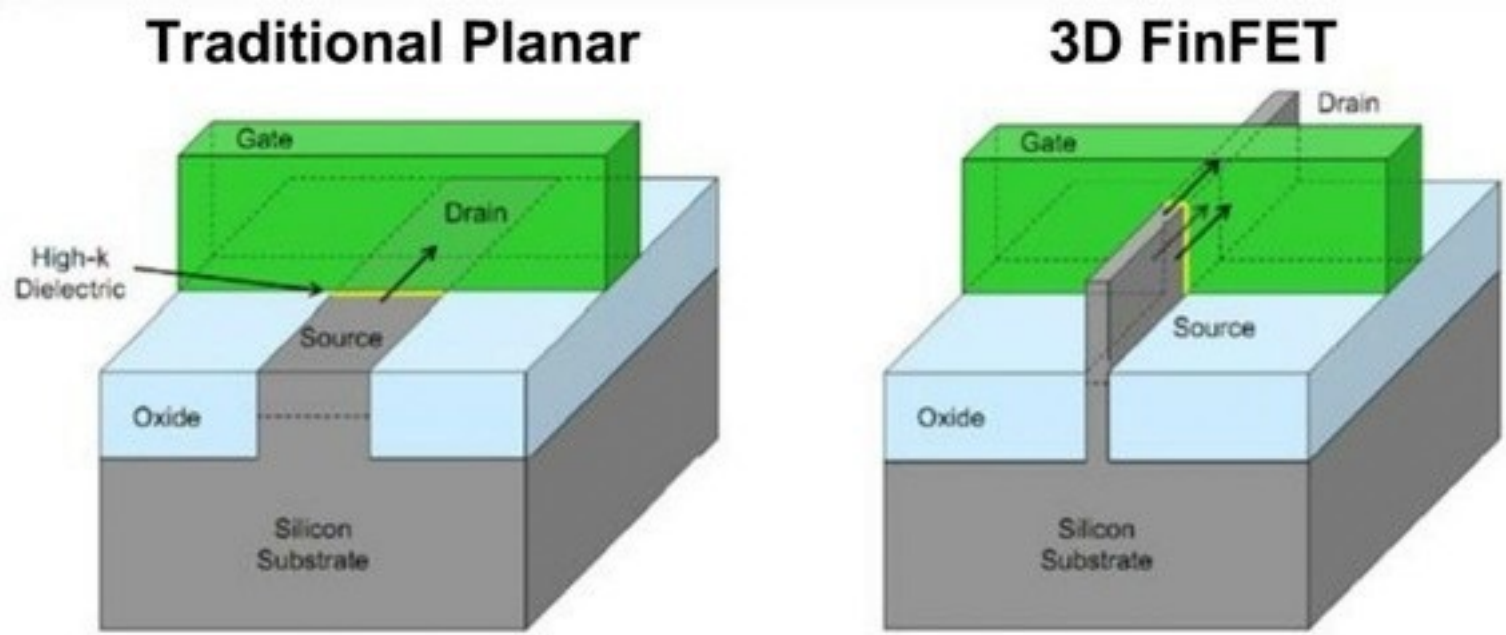
High-k/Metal Gate



- Since ~2007 - the 45nm node and below
- SiO_2 suffers from tunneling → use high-K dielectric
- More complex than simple chemical vapor deposition of SiO_2.
- Polysilicon can not be used with high-K dielectric
  - their interface is prone to defect formation, which leads to high Vt and degraded channel μ → use metal gate

https://www.anandtech.com/show/8223/an-introduction-to-semiconductor-physics-technology-and-industry/5

Tri-gate Transistors: FinFETs



Traditional 2-D planar transistor form a conducting channel in the silicon region under the gate electrode when in the "on" state

3-D Tri-Gate transistor form conducting channels on three sides of a vertical fin structure, providing "fully depleted" operation

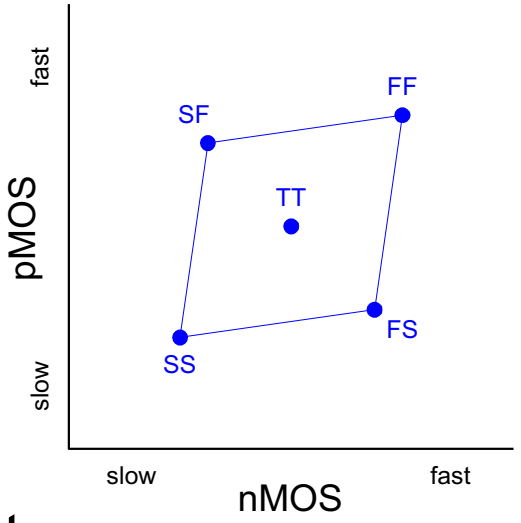
- Gate is wrapped around the channel, like a fin
- The channel is very small and is fully depleted like FD-SOI
- DIBL is reduced → much lower off current
- 22nm and below

So What?

- So what if transistors are not ideal?
  - They still behave like switches.
- But these effects matter for…
  - Supply voltage choice
  - Transistor sizing (e.g., in logical effort)
  - Quiescent power consumption
  - Pass transistors
  - Temperature of operation

Parameter Variation

- Transistors have uncertainty in parameters
  - Process: L_{eff}, V_t, t_{ox} of nMOS and pMOS
  - Vary around typical (T) values
- Fast (F)
  - L_{eff}: short
  - V_t: low
  - t_{ox}: thin
- Slow (S): opposite
- Not all parameters are independent for nMOS and pMOS



Environmental Variation

- V_{DD} and T also vary in time and space
- Fast:
  - V_{DD}: high
  - T: low

Corner	Voltage	Temperature
F	1.98	0 C
T	1.8	70 C
S	1.62	125 C

Process Corners

- Process corners describe worst case variations
  - If a design works in all corners, it will probably work for any variation.
- Describe corner with four letters (T, F, S)
  - nMOS speed
  - pMOS speed
  - Voltage
  - Temperature

Important Corners

- Some critical simulation corners include

Purpose	nMOS	pMOS	V_{DD}	Temp
Cycle time	S	S	S	S
Power	F	F	F	F
Subthreshold leakage	F	F	F	S
Pseudo-nMOS	S	F	?	?