ECE1388 VLSI Design Methodology

Lecture 10: Combinational Circuit Design

Adapted from Weste, Harris CMOS VLSI Design

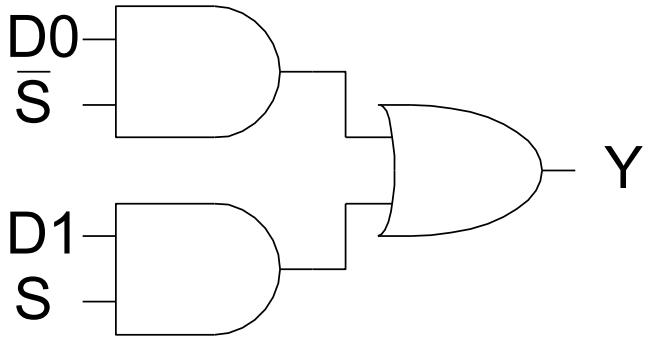
Outline

- Bubble Pushing
- Compound Gates
- Logical Effort Example
- Input Ordering
- Asymmetric Gates
- Skewed Gates
- Best P/N ratio

Example 1

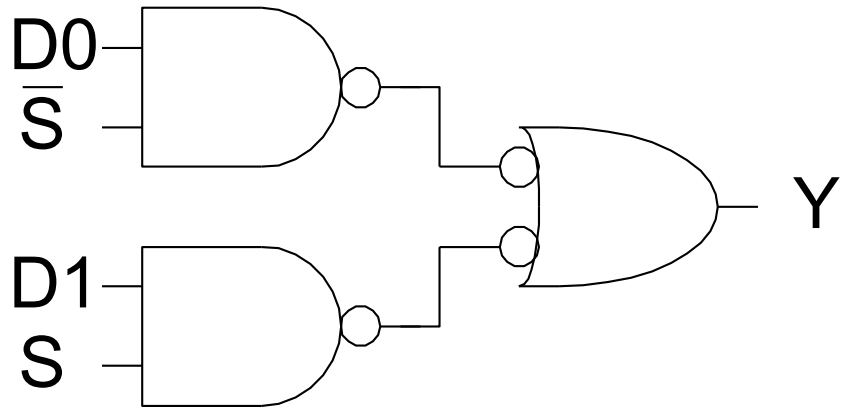
```
module mux(input  s, d0, d1,
           output y);

   assign y = s ? d1 : d0;
endmodule
```

1) Sketch a design using AND, OR, and NOT gates.
   Assume ~S is available.



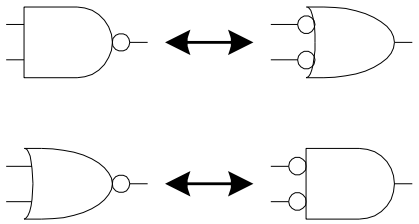
Example 2

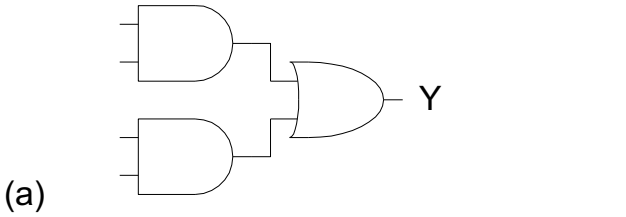
2) Sketch a design using NAND, NOR, and NOT gates.
Assume ~S is available.

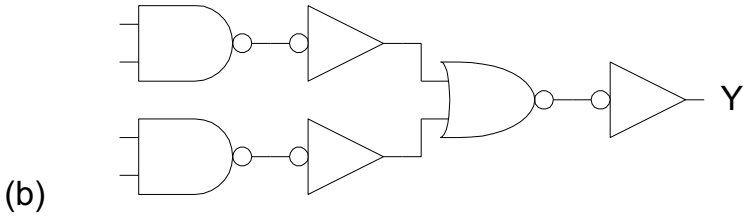


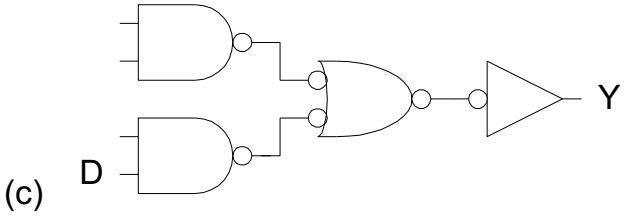
Bubble Pushing

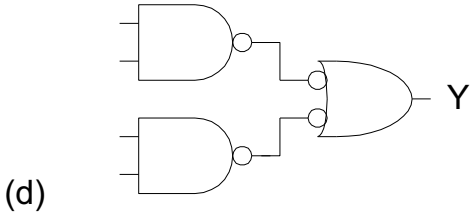
- Start with network of AND / OR gates
- Convert to NAND / NOR + inverters
- Push bubbles around to simplify logic
  - Remember DeMorgan's Law





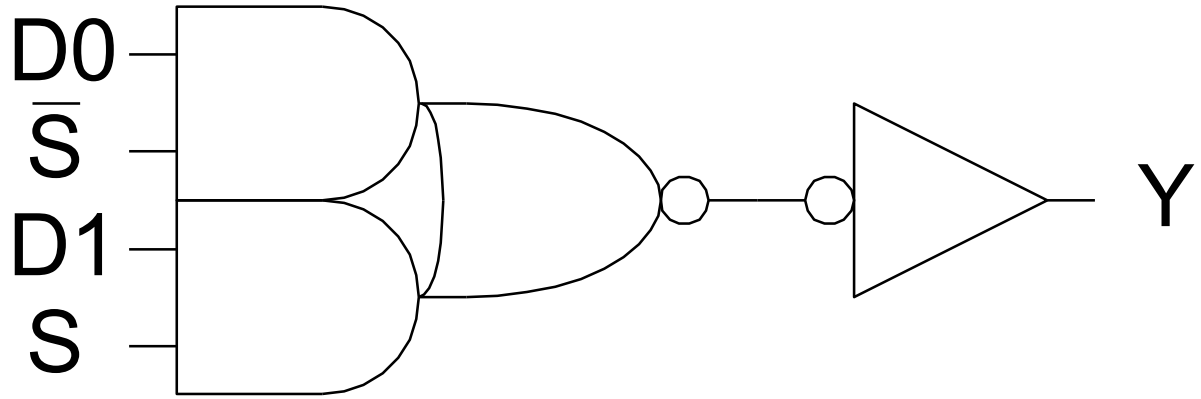






Example 3

3) Sketch a design using one compound gate and one NOT gate. Assume ~S is available.

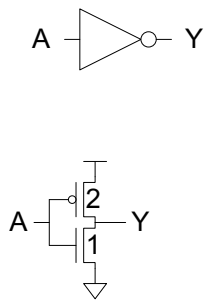


Compound Gates

- Logical Effort of compound gates

unit inverter

$Y = \overline{A}$

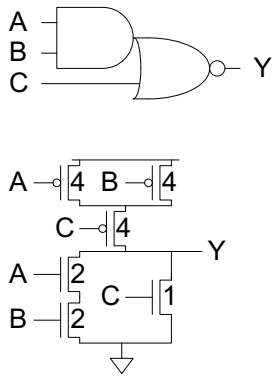


$g_A = 3/3$

$p = 3/3$

AOI21

$Y = \overline{A \bullet B + C}$



$g_A = 6/3$

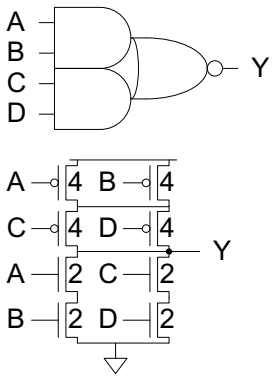
$g_B = 6/3$

$g_C = 5/3$

$p = 7/3$

AOI22

$Y = \overline{A \bullet B + C \bullet D}$



$g_A = 6/3$

$g_B = 6/3$

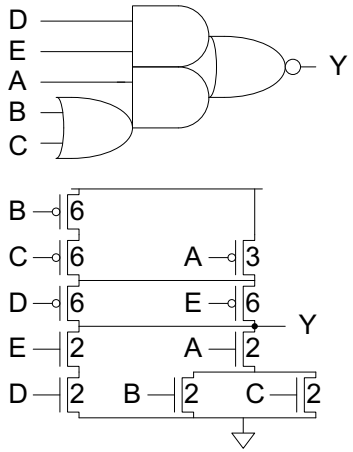
$g_C = 6/3$

$g_D = 6/3$

$p = 12/3$

Complex AOI

$Y = \overline{A \bullet (B + C) + D \bullet E}$



$g_A = 5/3$

$g_B = 8/3$

$g_C = 8/3$

$g_D = 8/3$

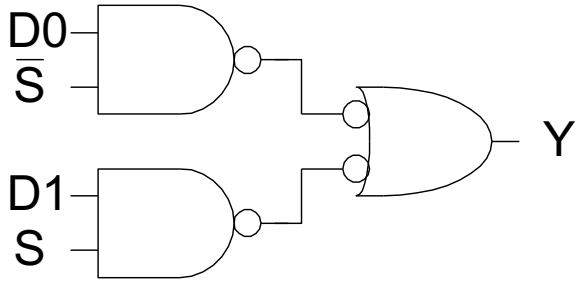
$g_E = 8/3$

$p = 16/3$

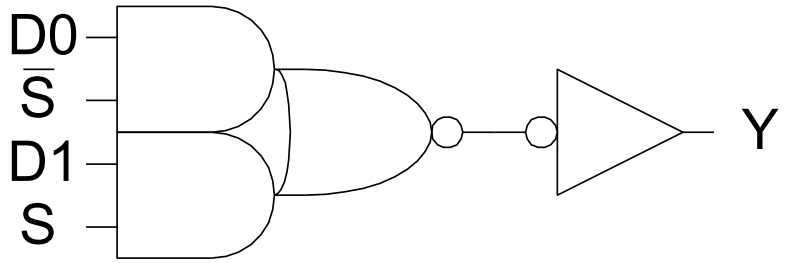
Example 4

- The multiplexer has a maximum input capacitance of 16 units on each input. It must drive a load of 160 units. Estimate the delay of the two designs.

H = 160 / 16 = 10 B = 1 N = 2



$$P = 2 + 2 = 4$$
$$G = (4/3)\bullet(4/3) = 16/9$$
$$F = GBH = \left(16/9\right)\bullet 1 \bullet 10 = 17.8$$
$$\hat{f} = \sqrt[N]{F} = 4.2$$
$$D = N\hat{f} + P = 12.4\tau$$

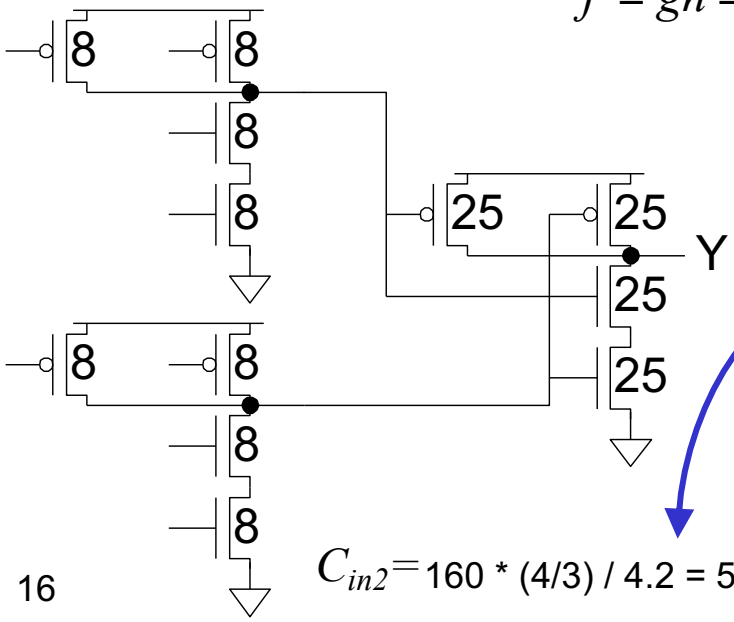


$$P = 4 + 1 = 5$$
$$G = (6/3)\bullet(1) = 2$$
$$F = GBH = 20$$
$$\hat{f} = \sqrt[N]{F} = 4.5$$
$$D = N\hat{f} + P = 14\tau$$

Example 5

- Annotate your designs with transistor sizes that achieve this delay.

$$\hat{f} = gh = g\frac{C_{out}}{C_{in}} \Rightarrow C_{in_i} = \frac{C_{out_i} g_i}{\hat{f}}$$



$C_{in1} =$ 16

$C_{in2} =$ 160 * (4/3) / 4.2 = 50

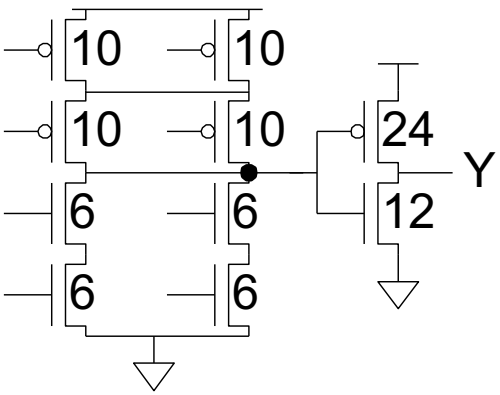
Repeated from the previous slide:

$g = 4/3$

$G = (4/3)\cdot(4/3) = 16/9;\ B = 1;\ H = 160/16 = 10$

$F = GBH = (16/9)\cdot 1 \cdot 10 = 17.8$

$\hat{f} = \sqrt[N]{F} = 4.2$



$C_{in1} =$ 16

$C_{in2} =$ 60 * 1 / 4.5 = 36

(10.66 rounded to 10, 5.33 rounded to 6; Sum=16)

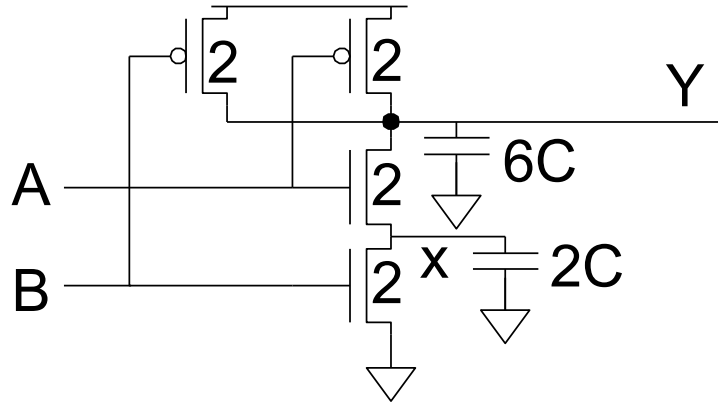
$g = 1$

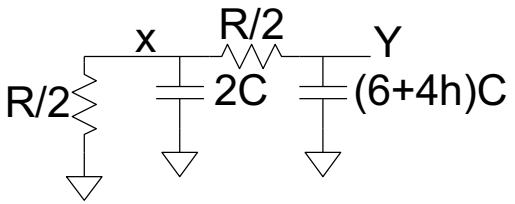
$G = (6/3)\cdot(1) = 2;\ B = 1;\ H = 160/16 = 10$

$F = GBH = 20$

$\hat{f} = \sqrt[N]{F} = 4.5$

Recall: Input Order





- Calculate *parasitic delay* for Y falling
  - If A arrives latest? 2τ *(node x already discharged)*

$$t_{pdf} = \left[\left(6+4h\right)C\right]\left(\tfrac{R}{2}+\tfrac{R}{2}\right) = \left(6+4h\right)RC$$

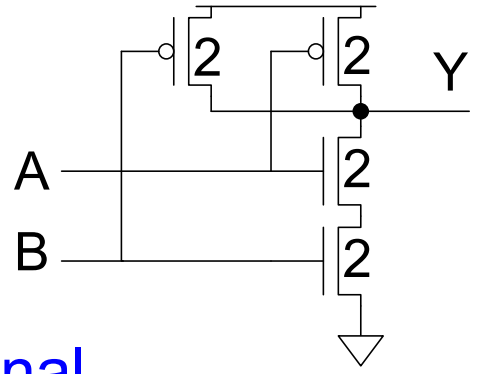
  - If B arrives latest? 2.33τ *(node x not discharged)*

$$t_{pdf} = \left(2C\right)\left(\tfrac{R}{2}\right)+\left[\left(6+4h\right)C\right]\left(\tfrac{R}{2}+\tfrac{R}{2}\right) = \left(7+4h\right)RC$$

$$d = t_{pdf} / 3RC \;\; and \;\; h = 0$$

Inner & Outer Inputs

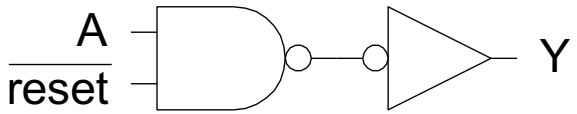
- *Inner* input is closest to output (A)
- *Outer* input is closest to rail (B)



- If input arrival time is known
  - Connect latest input to inner terminal

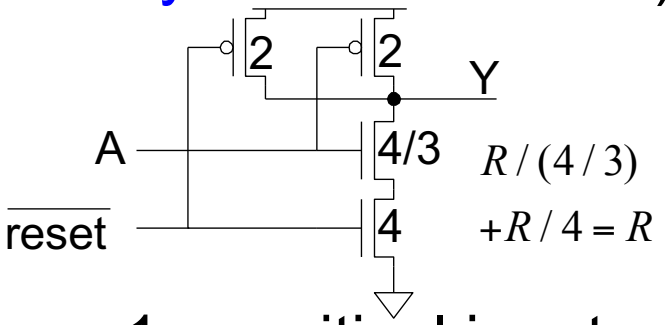
Asymmetric Gates

- Asymmetric gates favor one input over another
- Ex: suppose input A of a NAND gate is most critical
  - Use smaller transistor on A (less capacitance)
  - Boost size of noncritical input
  - So total resistance is same



- $g_A = (2+4/3)/3=10/9$ (< 4/3=12/9 for symmetric NAND2)
- $g_B = 6/3=2$ (for reset input)
- $g_{total} = g_A + g_B = 28/9$

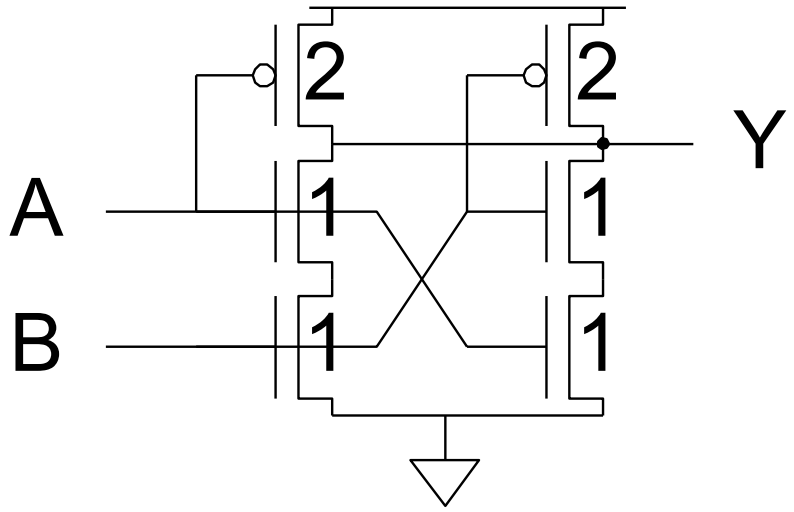
  (> 4/3+4/3=24/9)



- Asymmetric gate can approach g = 1 on critical input
- But total logical effort goes up

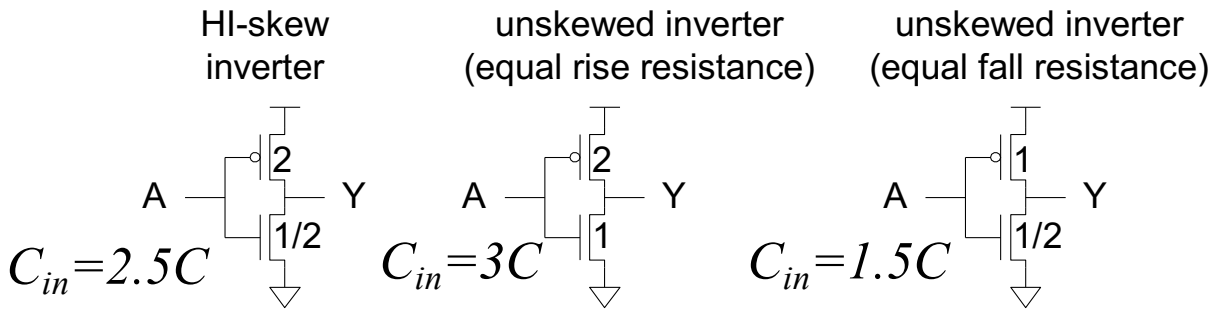
Symmetric Gates

- Inputs can be made perfectly symmetric



Skewed Gates

- Skewed gates favor one edge over another
- Ex: suppose the rising output of inverter is most critical
  - Downsize noncritical nMOS transistor



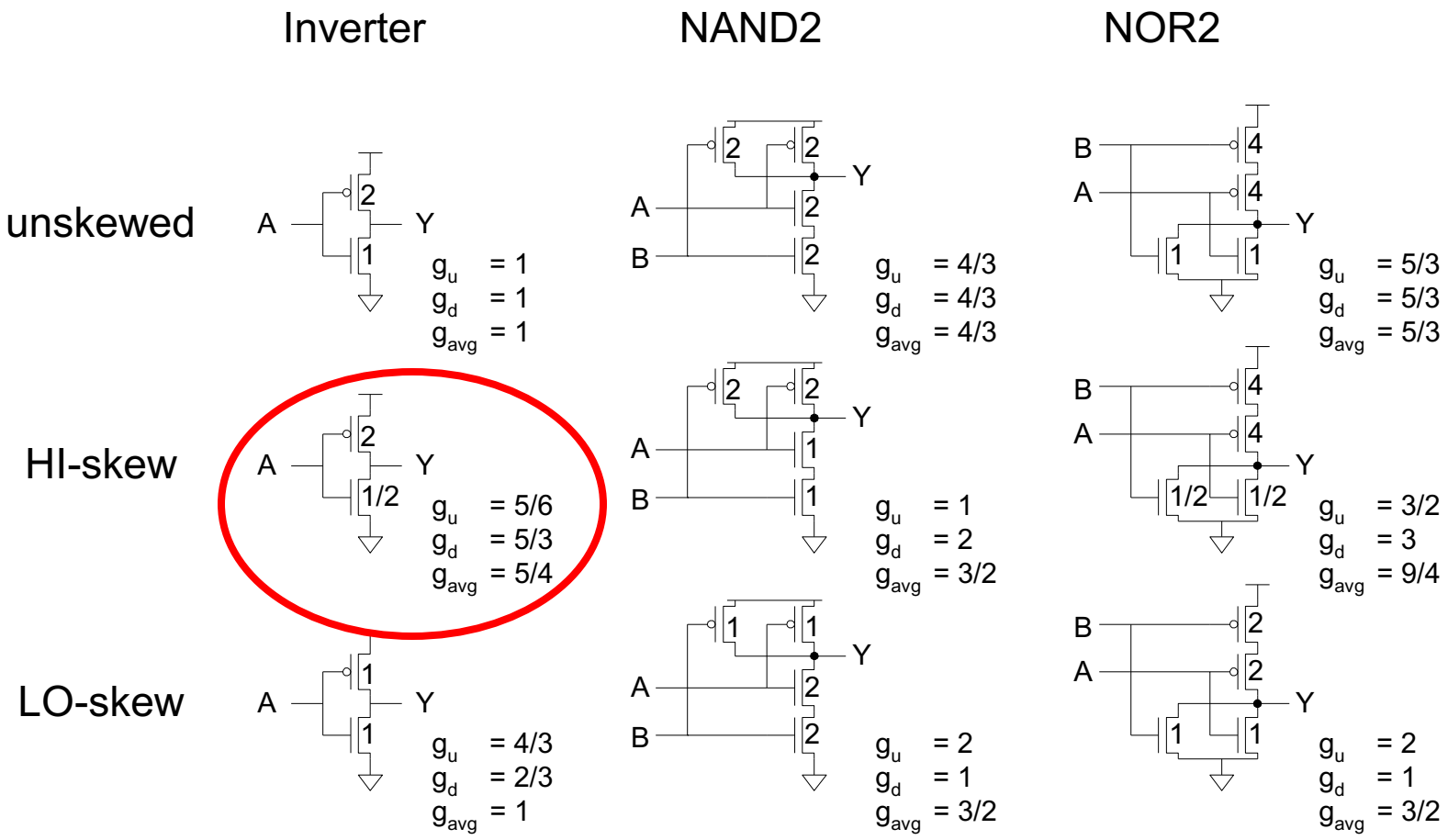
- Calculate logical effort by comparing to *unskewed* inverter with same effective resistance on that edge.
  - g_u = 2.5 / 3 = 5/6 < 1 → improved vs unit inverter
  - g_d = 2.5 / 1.5 = 5/3 > 1 → worse vs unit inverter
  - g_{ave} = (5/6+5/3)/2=5/4 > 1 → worse vs unit inverter

HI- and LO-Skew

- Def: Logical effort of a skewed gate for a particular transition is the ratio of the input capacitance of that gate to the input capacitance of an unskewed inverter delivering the same output current for the same transition.

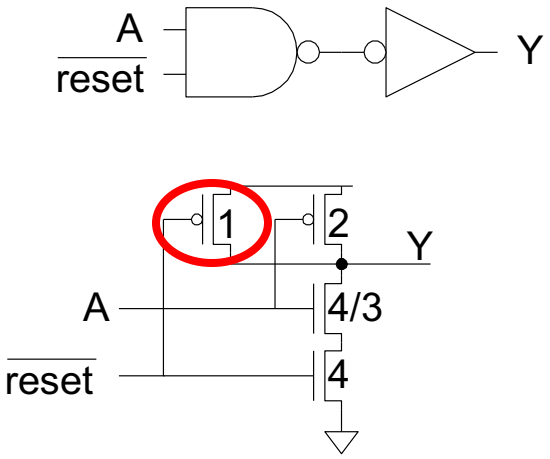
- Skewed gates reduce size of noncritical transistors
  - HI-skew gates favor rising output (small nMOS)
  - LO-skew gates favor falling output (small pMOS)
- Logical effort is smaller for favored direction
- But larger for the other direction

Catalog of Skewed Gates



Asymmetric Skew

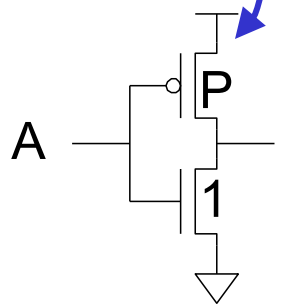
- Combine asymmetric and skewed gates
  - Downsize noncritical transistor on unimportant input
  - Reduces parasitic delay for critical input



Best P/N Ratio for Min Delay

- For best noise margins we have selected $W_p/W_n=\mu_n/\mu_p$
  - e.g., $\mu_n/\mu_p = 2$ in textbook
- For least average delay, choose $W_p/W_n=\sqrt{\mu_n/\mu_p}$

- Proof for inverter with no load
  - Define $\mu=\mu_n/\mu_p$; P is size parameter (not paras. delay)
  - $t_{pdf} = RC_{out} = P+1$ - *as C_{out}=P+1 and R=1 for NMOS*
  - $t_{pdr} = (P+1)(\mu/P)$ - *as xP wider but $x\mu$ slower*
  - $t_{pd} = (P+1)(1+\mu/P)/2 = (P + 1 + \mu + \mu/P)/2$
  - $dt_{pd} / dP = (1- \mu/P^2)/2 = 0$
  - Least delay for P = $\sqrt{\mu} = \sqrt{\mu_n/\mu_p}$



Preferred P/N Ratios

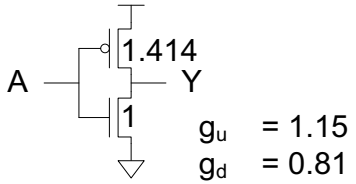
- Often, best P/N ratio is chosen as $Wp/Wn=\sqrt{\mu_n/\mu_p}$
  - Degrades noise margin somewhat
  - Only improves average delay *slightly* for inverter
  - But significantly decreases area and power
- Ex: inverter - best speed, good area/power/noise-tolerance

  NAND: best noise-tolerance, good speed/area/power

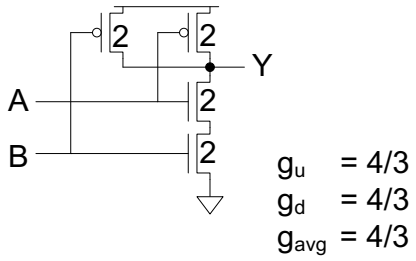
  NOR: good area/speed/power; lower noise-tolerance

fastest P/N ratio

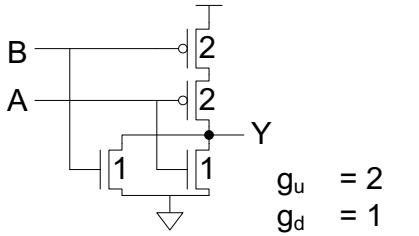
Inverter



NAND2



NOR2



Observations

- For speed:
  - NAND vs. NOR
  - Many simple stages vs. fewer high fan-in stages
  - Delay-critical input
    - Should be connected closest to the output
- For area and power:
  - Many simple stages vs. fewer high fan-in stages