ECE1388 VLSI Design Methodology

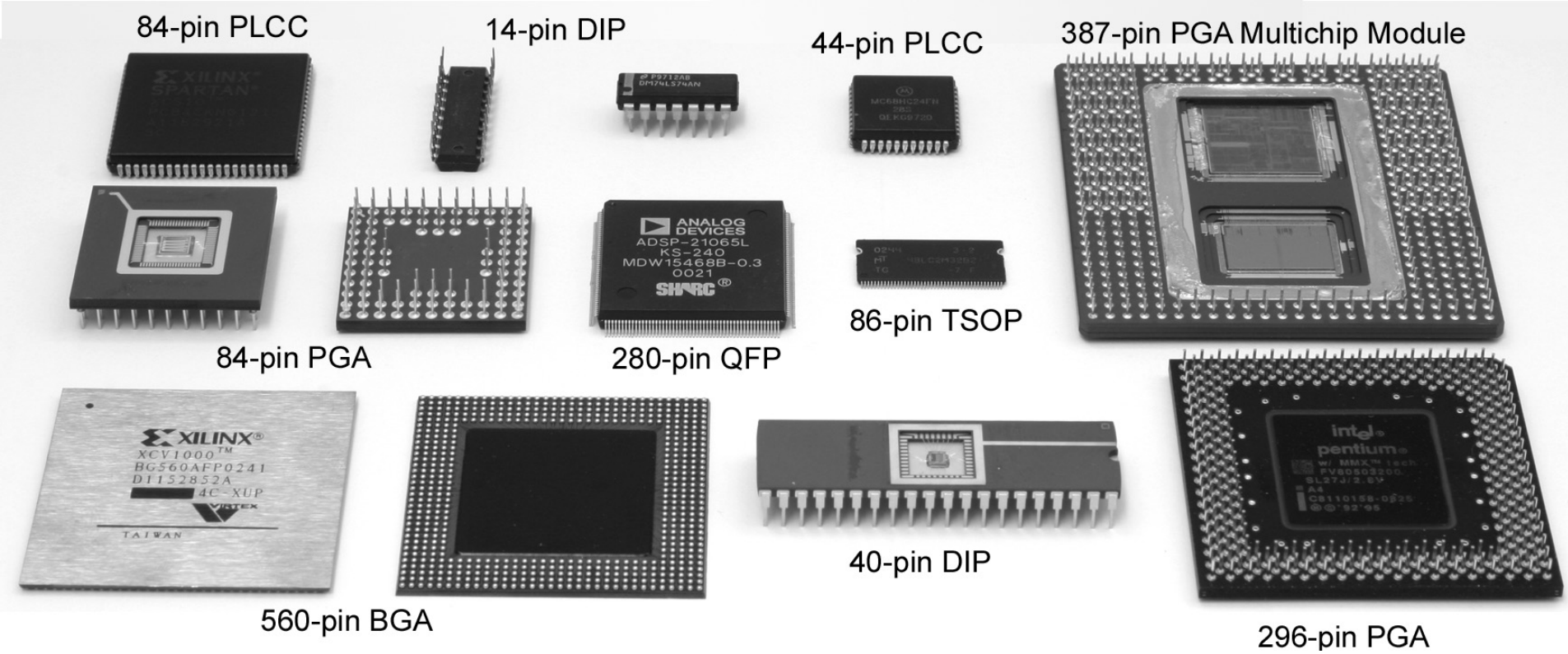
Lecture 9: Packaging, Power and Clock Distribution

Adapted from Weste, Harris CMOS VLSI Design

Outline

- Packaging
- Power Distribution
- Clock Distribution

History of Package Types



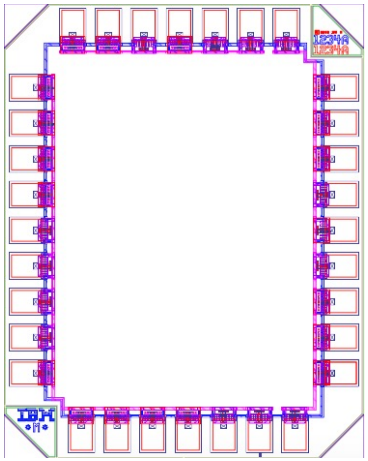
- Through-hole vs. surface mount

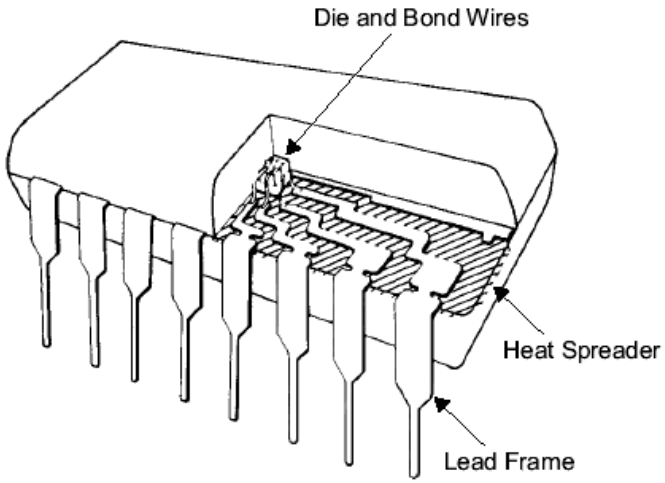
Packages

- Package functions
  - Electrical connection
    - of signals and power from chip to board
    - little delay or distortion
  - Mechanical connection
    - Fastens chip to board
    - Protects chip from mechanical damage
  - Heat management
    - Removes heat produced on chip
    - Compatible with thermal expansion
  - Inexpensive to manufacture and test

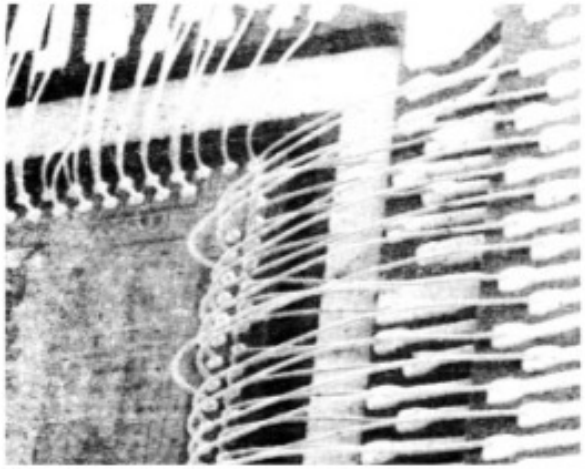
Chip-to-Package Bonding

- Traditionally, chip is surrounded by *pad frame*
  - Metal pads on 100 – 200 μm pitch
  - Gold *bond wires* attach pads to package
  - *Lead frame* distributes signals in package
  - Metal *heat spreader* helps with cooling





I/O Interconnect

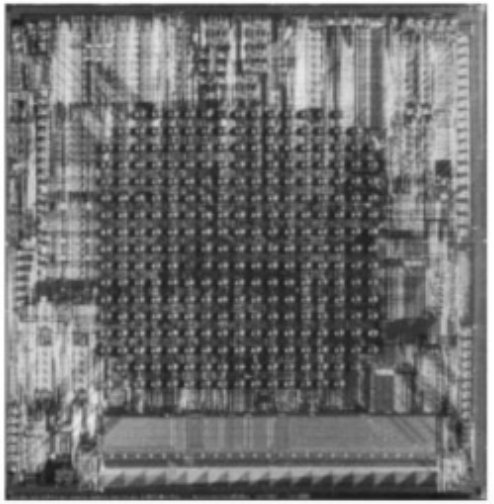


Source: IEPS 1990

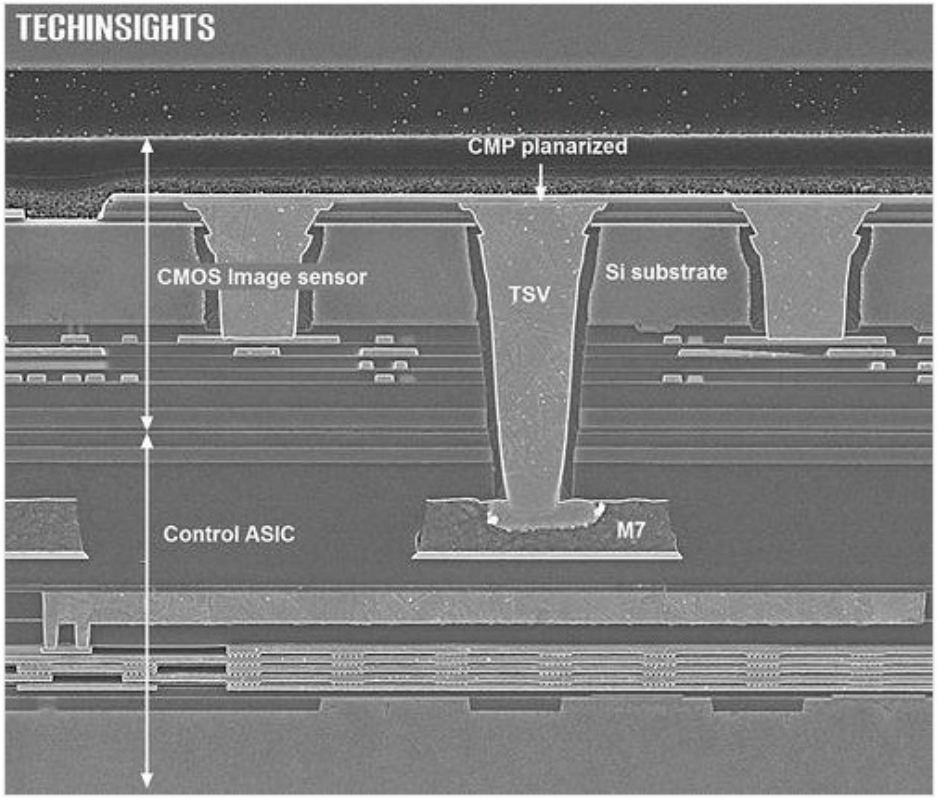
Source: Motorola

- Wirebonding
- Tape-automated bonding (TAB)

- Flip-chip bonding
- Through-silicon Via (TSV)

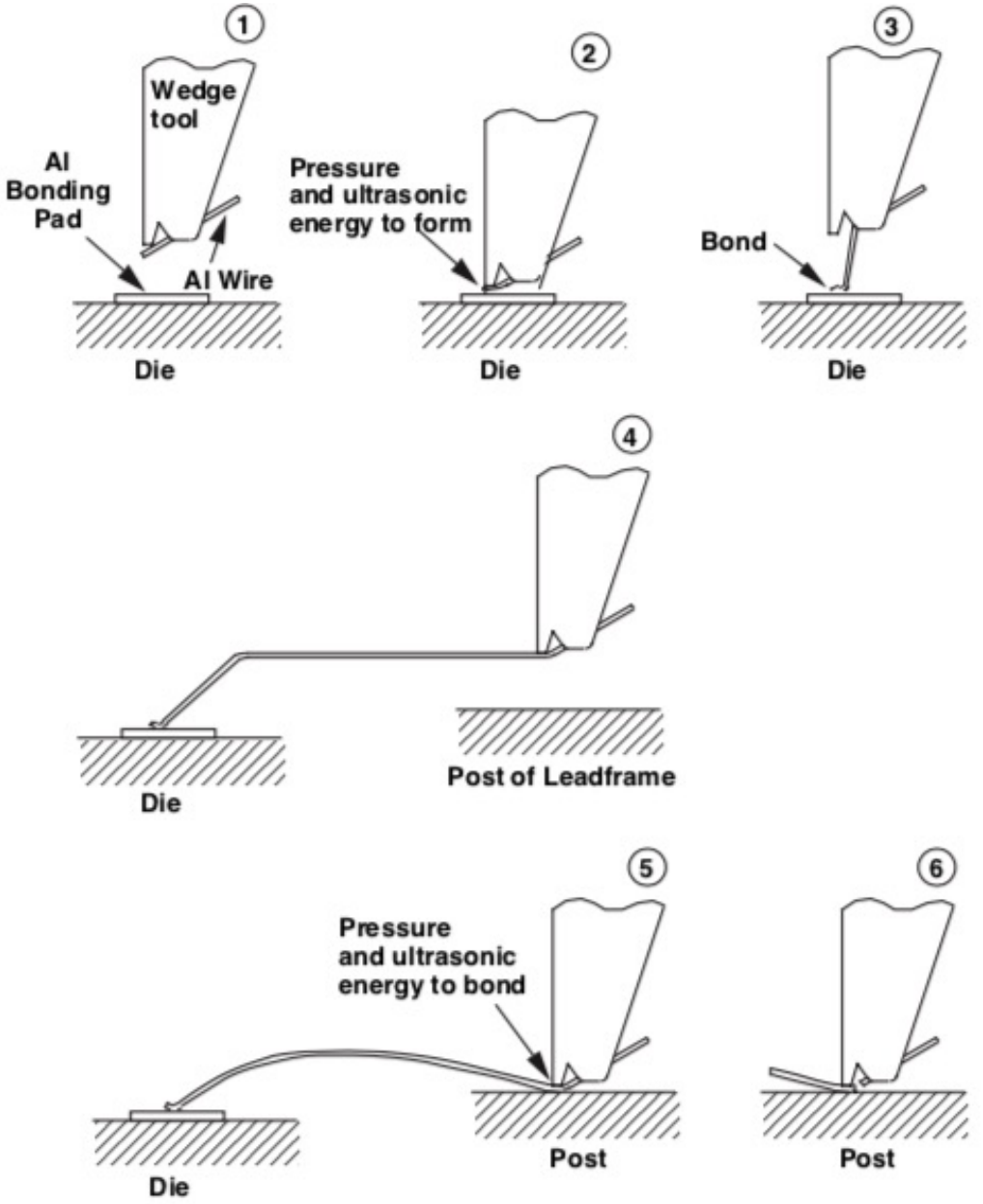


Courtesy of IBM

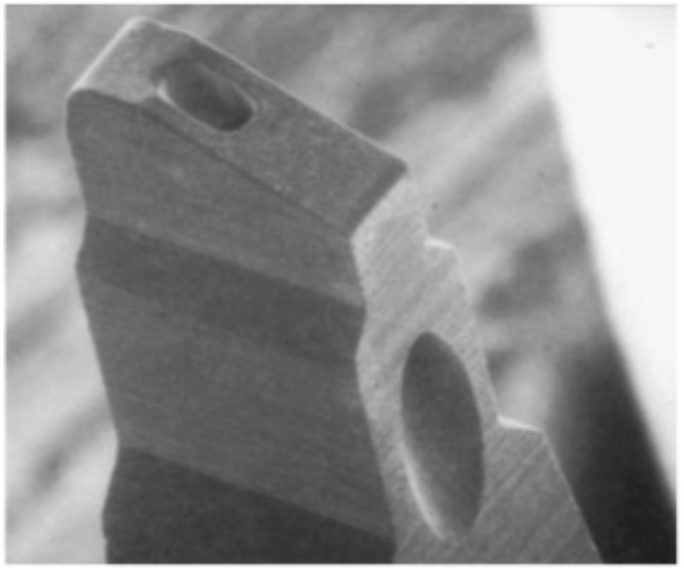


Sony IMX240 Cross Section (Source: TechInsights)

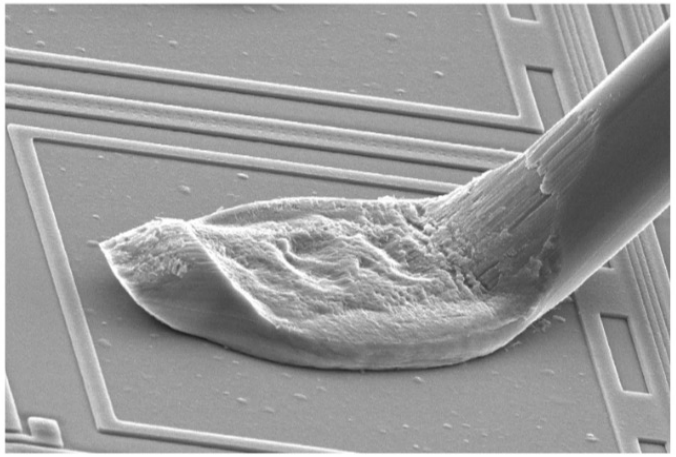
Wedge Wirebonding



Source: National Bureau of Standards/ICE, "Roadmaps on Packaging Solutions" 15027B

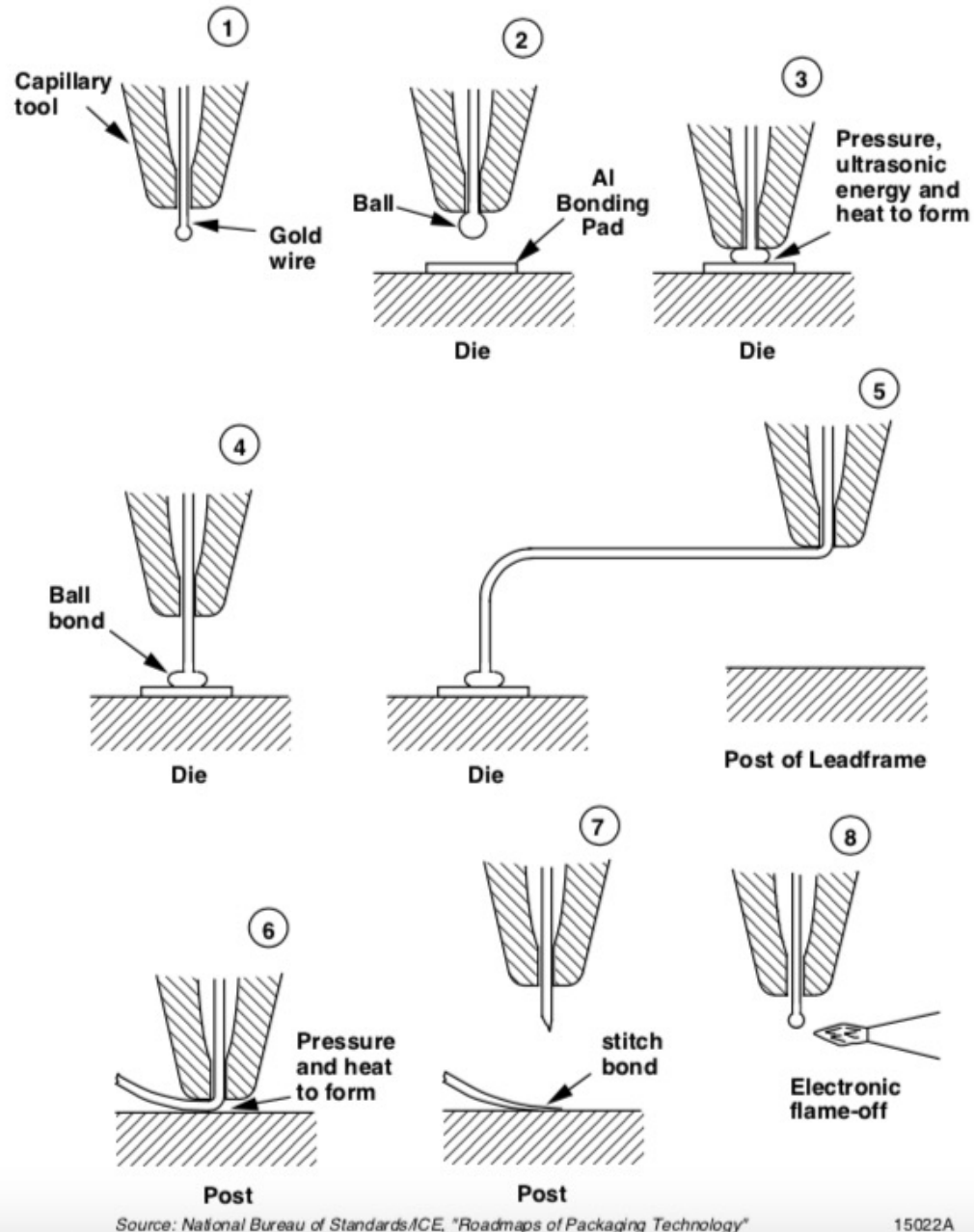


Source: Micro Swiss/ ICE, "Roadmaps of Packaging Technology" 22512



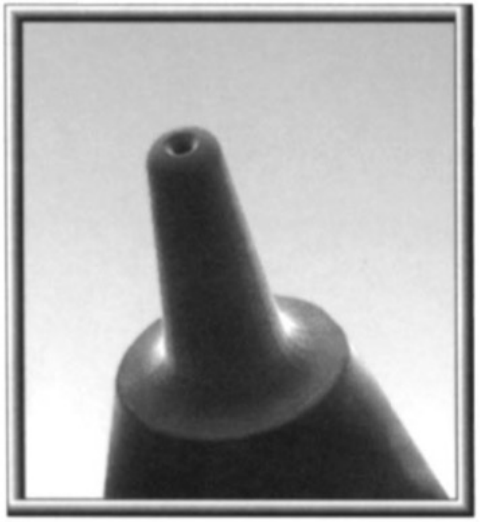
Source: ICE, "Roadmaps of Packaging Technology" 22537

Thermocompression Wirebonding

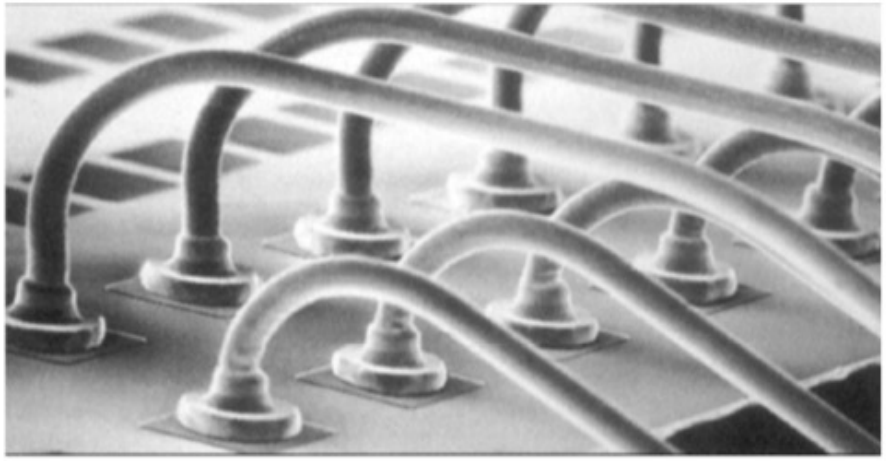


Source: National Bureau of Standards/ICE, "Roadmaps of Packaging Technology" 15022A

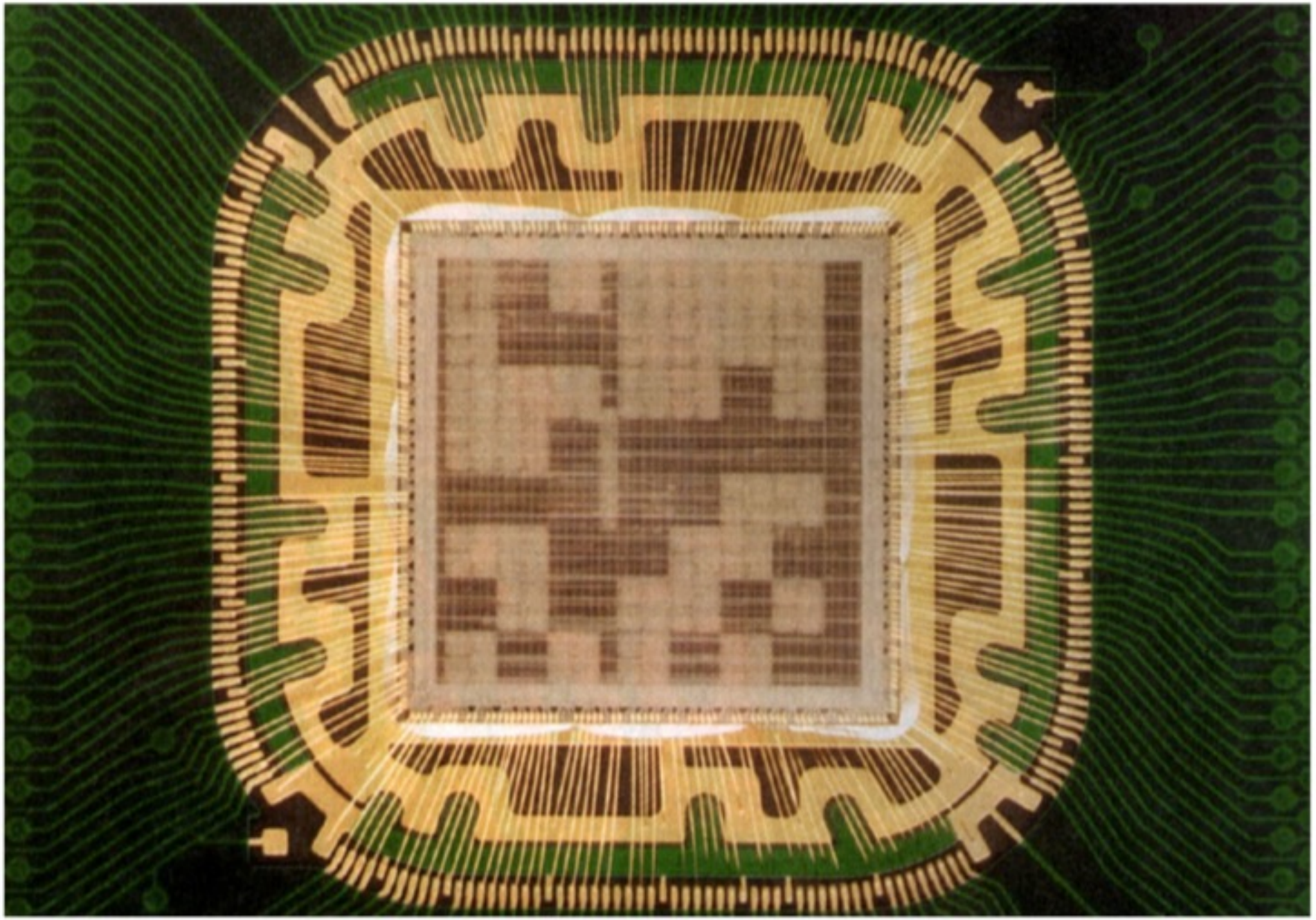
- Thermocompression
- Thermosonic



Source: Micro-Swiss/CE, "Roadmaps of Packaging Technology"

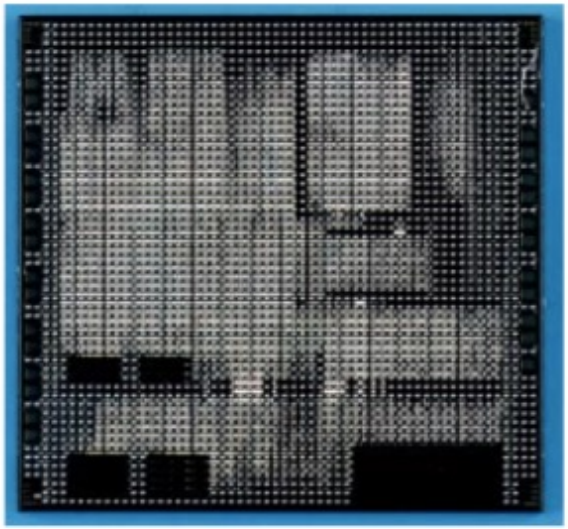


Source: Gaiser Tool Company/ICE, "Roadmaps of Packaging Technology" 22514

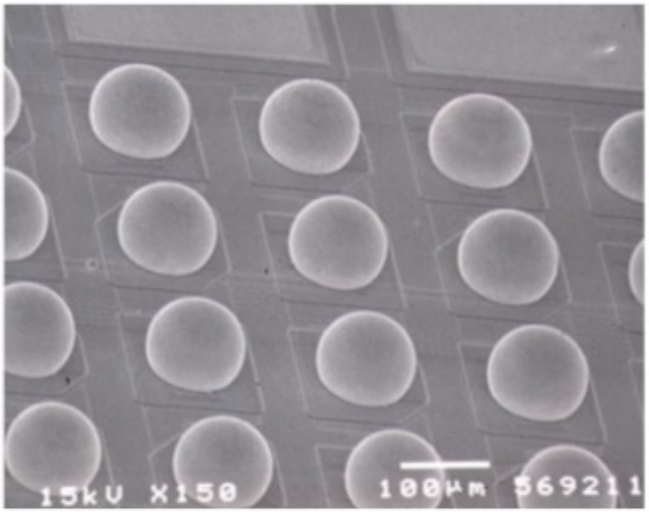


Source: Electronic Design/ICE, "Roadmaps of Packaging Technology"

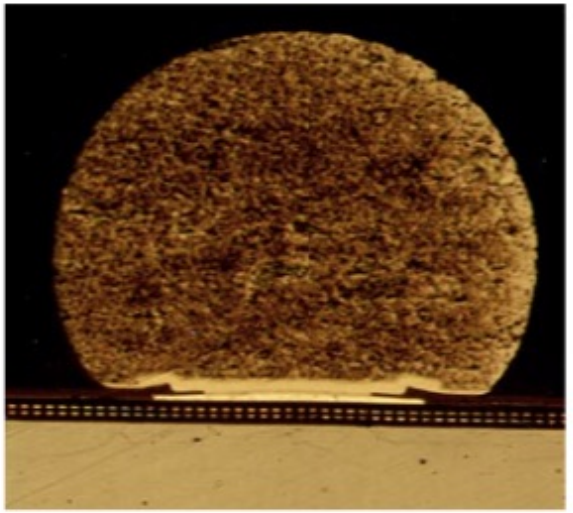
Flip-Chip I/O



900 Ball Flip Chip ASIC



Close Up of the 5mil Diameter Solder Balls on the ASIC



Cross Section of Solder Ball Showing the UBM on the ASIC

Source: Fujitsu Computer Packaging Technology/ICE, "Roadmaps of Packaging Technology"

22552

- Bond wires contribute parasitic inductance
- *Flip-chip* places connections across surface of die rather than around periphery
  - Top level metal pads covered with solder balls
  - Chip flips upside down
  - Carefully aligned to package (done blind!)
  - Heated to melt balls
  - Also called *C4* (Controlled Collapse Chip Connection)

I/O Interconnect Specs

	Resistance Per Length	Inductance Per Length	Typical Lengths	Typical Resistances	Typical Inductances
Wirebond	1 Ohm/inch	25nH/inch	50-100mils	50-100mOhms	1.2-2.5nH
TAB	0.25 Ohm/inch	21nH/inch	100-300mils	25-75mOhms	2.1-6.3nH
Flip Chip	0.08 Ohm/inch	18nH/inch	3-6mils	<1mOhm	<0.1nH

Source: ICE, "Roadmaps of Packaging Technology"

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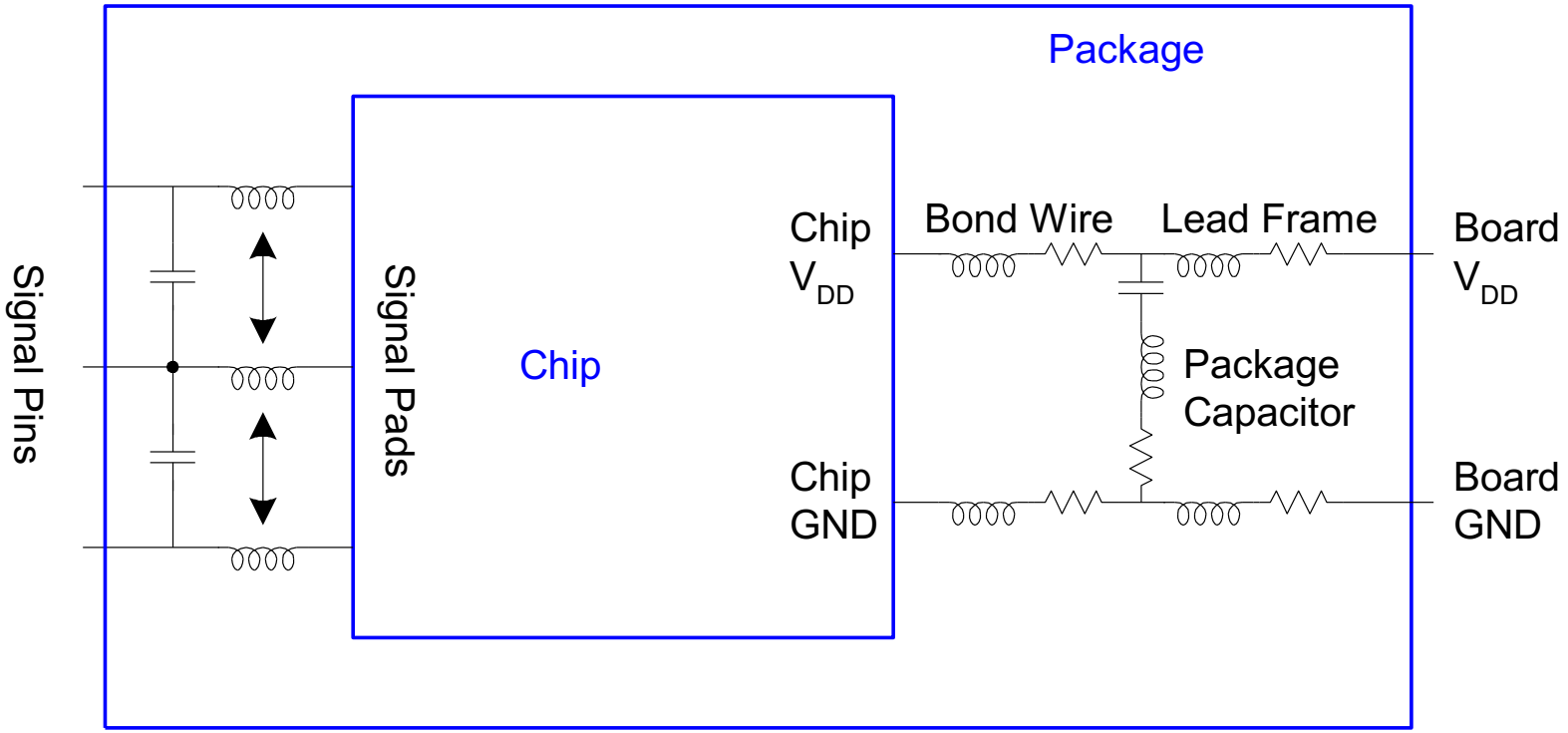
Package Parasitics

- Use many V_{DD}, GND in parallel
  - Inductance, I_{DD}



Heat Dissipation

- 60 W light bulb has surface area of 120 cm^2
- Itanium 2 die dissipates 130 W over 4 cm^2
  - Chips have enormous power densities
  - Cooling is a serious challenge
- Package spreads heat to larger surface area
  - Heat sinks may increase surface area further
  - Fans increase airflow rate over surface area
  - Liquid cooling used in extreme cases ($$$)

Thermal Resistance

- $\Delta T = \theta_{ja} P$
  - ΔT: temperature rise on chip
  - θ_{ja}: thermal resistance of chip junction to ambient
  - P: power dissipation on chip

- Thermal resistances combine like resistors
  - Series and parallel

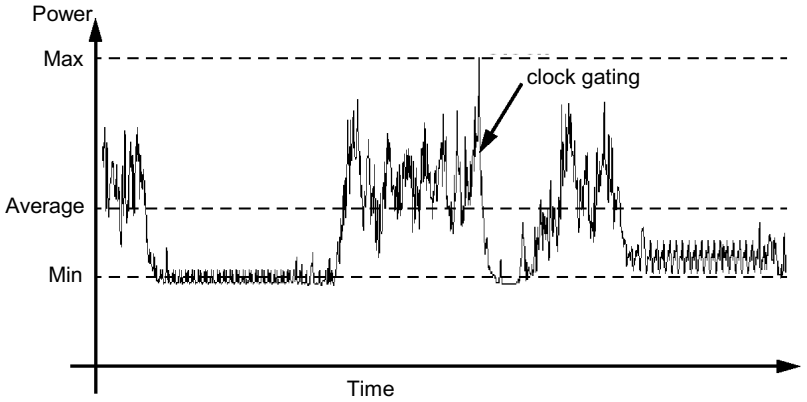
- $\theta_{ja} = \theta_{jp} + \theta_{pa}$
  - Series combination

Power Distribution

- Power Distribution Network functions
  - Carry current from pads to transistors on chip
  - Maintain stable voltage with low noise
  - Provide average and peak power demands
  - Provide current return paths for signals
  - Avoid electromigration & self-heating wearout
  - Consume little chip area and wire
  - Easy to lay out

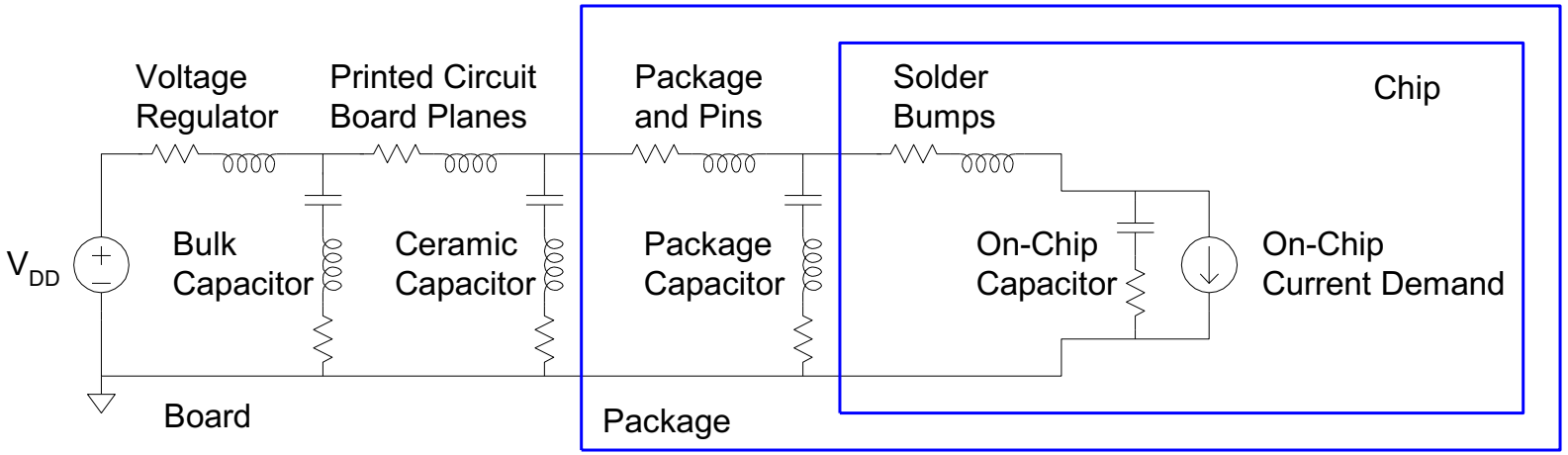
Power Requirements

- $V_{DD} = V_{DDnominal} - V_{droop}$
- Want V_{droop} < +/- 10% of V_{DD}
- Sources of V_{droop}
  - IR drops
  - L di/dt noise
- I_{DD} changes on many time scales



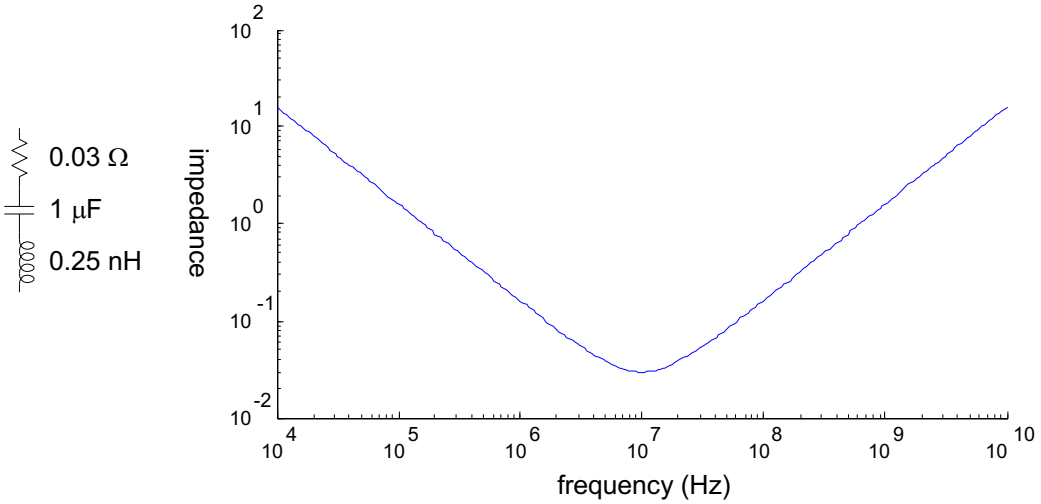
Power System Model

- Power comes from regulator on system board
  - Board and package add parasitic R and L
  - Bypass capacitors help stabilize supply voltage
  - But capacitors also have parasitic R and L
- Simulate system for time and frequency responses



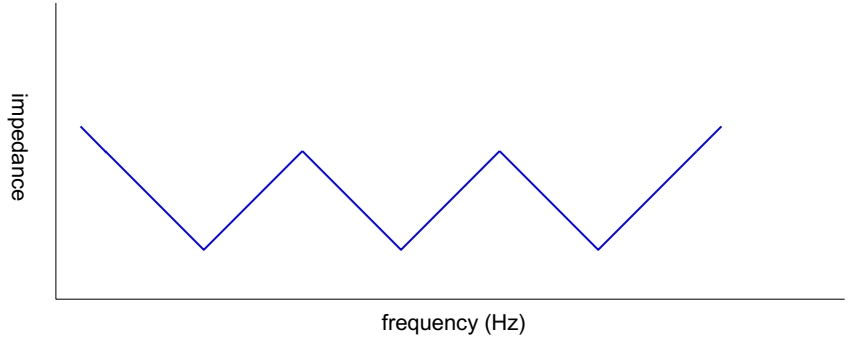
Bypass Capacitors

- Need low supply impedance at all frequencies
- Ideal capacitors have impedance decreasing with ω
- Real capacitors have parasitic R and L
  - Leads to resonant frequency of capacitor



Frequency Response

- Use multiple capacitors in parallel
  - Large capacitor near regulator has low impedance at low frequencies
  - But also has a low self-resonant frequency
  - Small capacitors near chip and on chip have low impedance at high frequencies
- Choose caps to get low impedance at all frequencies



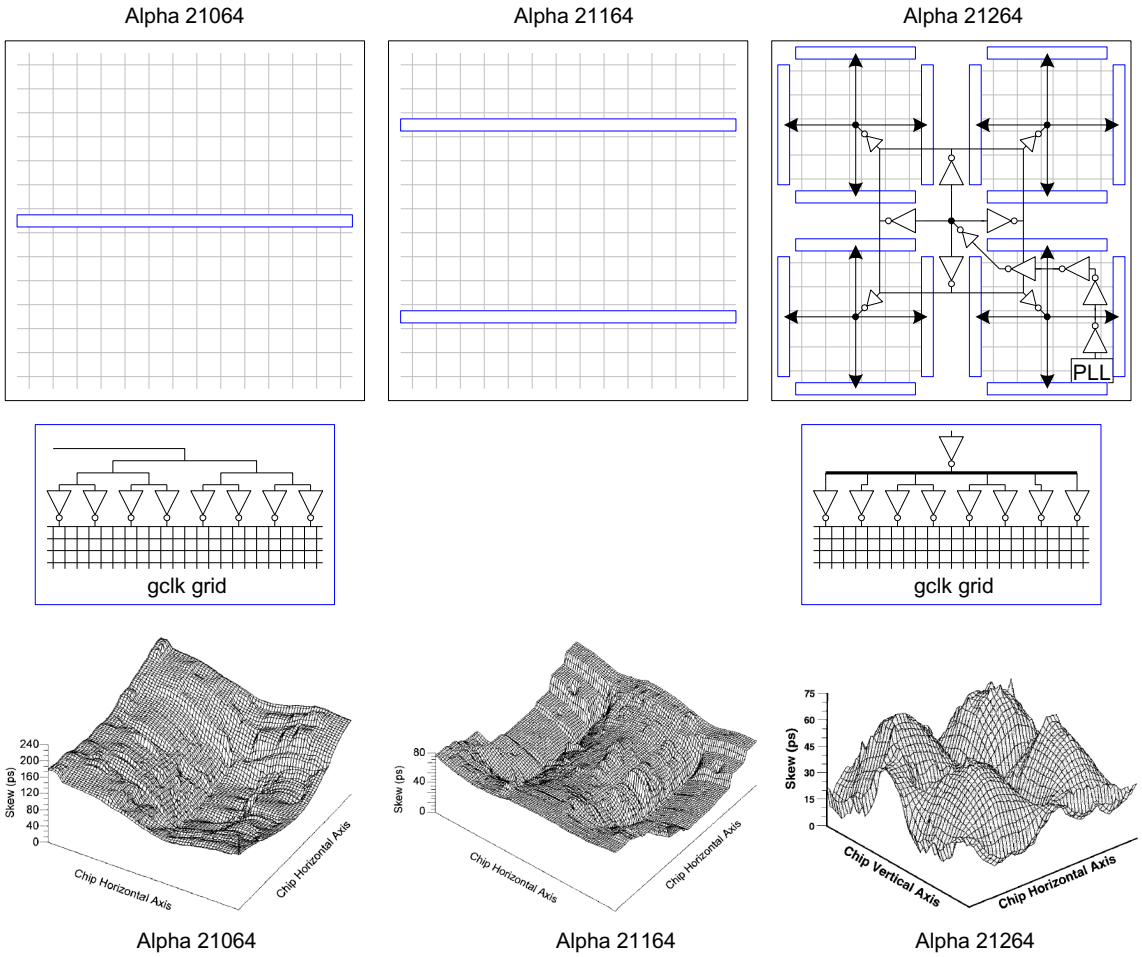
Clock Dist. Networks

- *Ad hoc*
- Grids
- H-tree
- Hybrid

Clock Grids

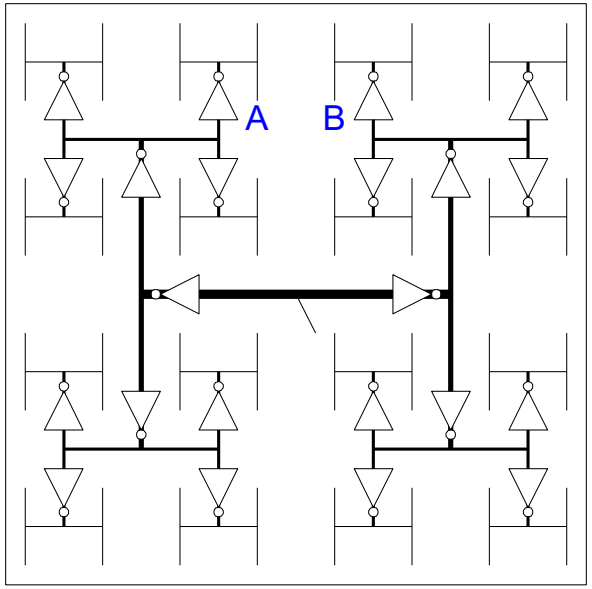
- Use grid on two or more levels to carry clock
- Make wires wide to reduce RC delay
- Ensures low skew between nearby points
- But possibly large skew across die

Alpha Clock Grids



H-Trees

- Fractal structure
  - Gets clock arbitrarily close to any point
  - Matched delay along all paths
- Delay variations cause skew
- A and B might see big skew



Hybrid Networks

- Use H-tree to distribute clock to many points
- Tie these points together with a grid

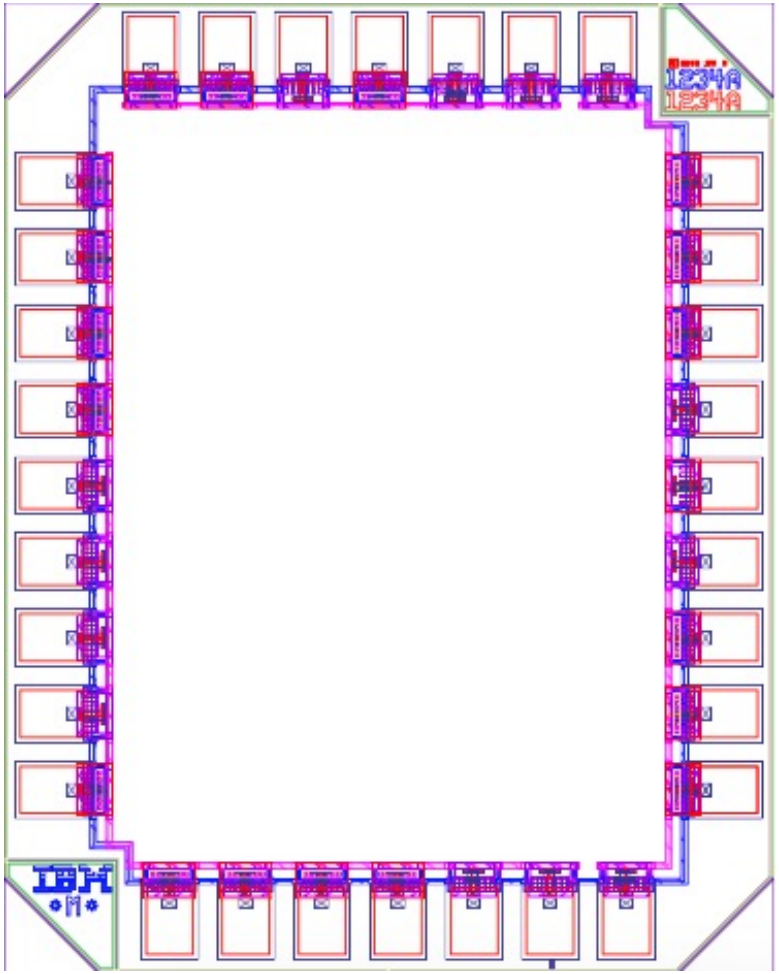
- Ex: IBM Power4, PowerPC
  - H-tree drives 16-64 sector buffers
  - Buffers drive total of 1024 points
  - All points shorted together with grid

Input / Output

- Input/Output System functions
  - Communicate between chip and external world
  - Drive large capacitance off chip
  - Operate at compatible voltage levels
  - Provide adequate bandwidth
  - Limit slew rates to control di/dt noise
  - Protect chip against electrostatic discharge
  - Use small number of pins (low cost)

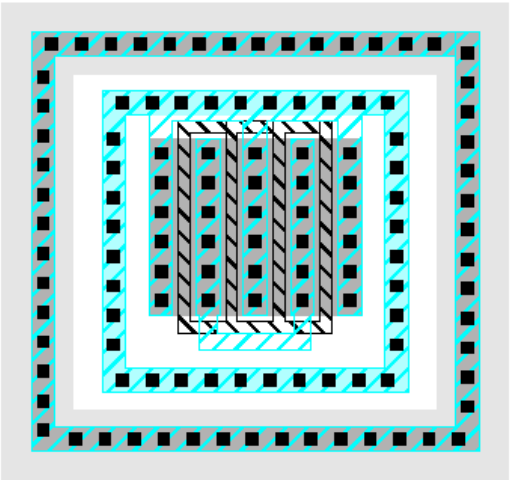
I/O Pad Design

- Pad types
  - V_{DD} / GND
  - Output
  - Input
  - Bidirectional
  - Analog



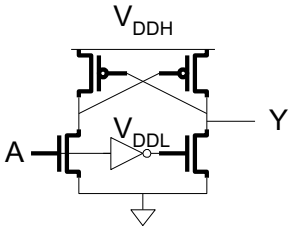
Output Pads

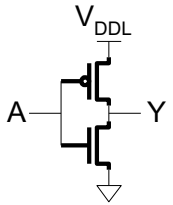
- Drive large off-chip loads (2 – 50 pF)
  - With suitable rise/fall times
  - Requires chain of successively larger buffers
- Guard rings to protect against latchup
  - Noise below GND injects charge into substrate
  - Large nMOS output transistor
  - p+ inner guard ring
  - n+ outer guard ring
    - In n-well



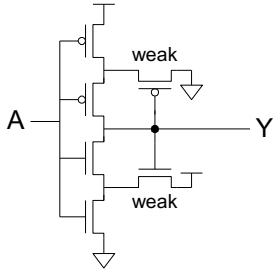
Input Pads

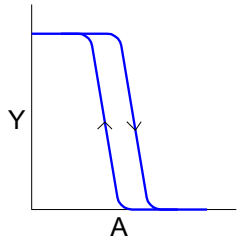
- Level conversion
  - Higher or lower off-chip V
  - May need thick oxide gates





- Noise filtering
  - Schmitt trigger
  - Weak transistors introduce positive feedback
  - The resulting hysteresis changes V_{IH}, V_{IL}

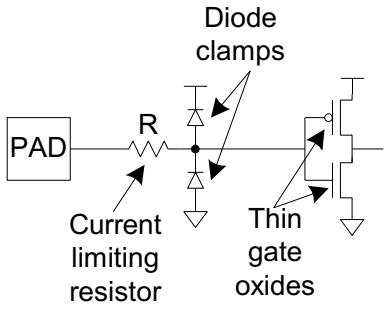


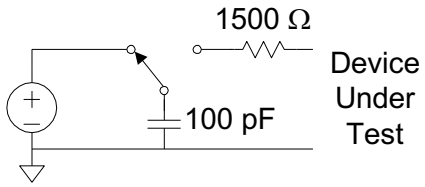


- Protection against electrostatic discharge

ESD Protection

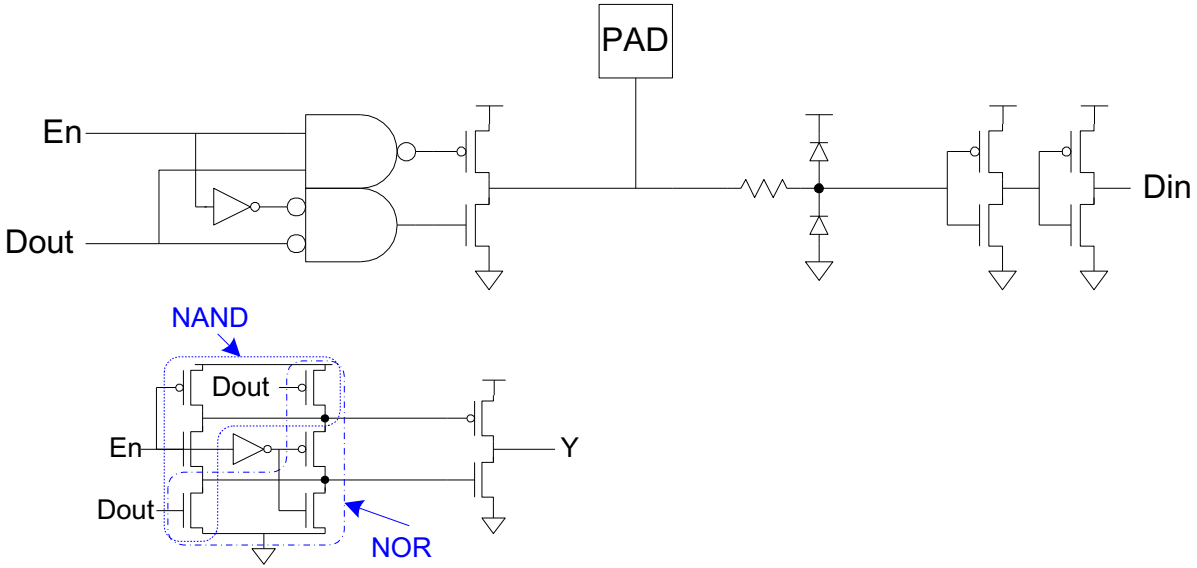
- Static electricity builds up on your body
  - Shock delivered to a chip can fry thin gates
  - Must dissipate this energy in protection circuits before it reaches the gates
- ESD protection circuits
  - Current limiting resistor
  - Diode clamps
- ESD testing
  - Human body model
  - Views human as charged capacitor





Bidirectional Pads

- Combine input and output pad
- Need tristate driver on output
  - Use enable signal to set direction
  - Optimized tristate avoids huge series transistors



Analog Pads

- Pass analog voltages directly in or out of chip
  - No buffering
  - Protection circuits must not distort voltages

MOSIS I/O Pad

- 1.6 μm two-metal process
  - Protection resistors
  - Protection diodes
  - Guard rings
  - Field oxide clamps