ECE 1388 2025F VLSI Design Methodology (tentative)

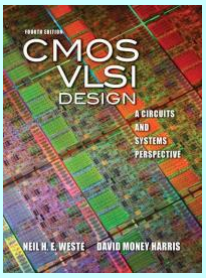
Overview: The course introduces a design methodology for very-large-scale-integration (VLSI) circuits using advanced computer-aided-design (CAD) tools. The focus is on learning Cadence integrated circuit (IC) design tools to implement the IC design flow. The methodology includes the steps of: custom digital circuit design, automated digital circuit synthesis, digital and mixed-signal circuit simulation, custom layout design, and automated layout generation. The course includes several projects using a 65nm CMOS process: (1) transistor characterization, (2) full custom digital circuit and layout design, (3) automated digital circuit synthesis and layout place-and-route, and (4) team-based design of a full IC employing the methodology learned in the course.

Schedule: Friday 9am – 11:45am in AB-107 (~3 hours as opposed to conventional 2 hours, to allow for time for tutorials, discussions and other components of the course)

Instructor:

- Roman Genov
- Email: ask1388@eecg.utoronto.ca (this alias forwards email to the instructor and all TAs – all very personal questions that do not qualify for Piazza can be sent here – see qualifications how to decide on this below) or roman@eecg.utoronto.ca (the instructor only – for very confidential matters only)

Textbooks:



CMOS VLSI Design: A Circuit and Systems Perspective, by N. Weste and D. Harris, 4th edition, Addison Wesley, 2011. Lectures are delivered using slides closely following the textbook material, which are posted on the course website. These slides have evolved from their original version, with various annual updates and additions included due to the continuous developments in the subject area.

VLSI Design Methodology CAD Tools User's Manual.
The manual is for use in the laboratory section of the course and introduces students to commercially available VLSI IC design software from Cadence and Synopsys, with a special emphasis on the design in a 65nm CMOS technology.

Other supplementary material *(optional, for reference only, no need to purchase)*:

Digital Integrated Circuits: A Design Perspective, by J. Rabaey, A. Chandrakasan, and B. Nikolić, 2nd edition, Prentice Hall, 2003.

The Art of Analog Layout, by A. Hastings, Prentice Hall, 2000.

Pre-requisites
An undergraduate course on CMOS circuit design, and understanding of UNIX/LINUX operating system, such as ability to use UNIX commands at the prompt and to edit UNIX configuration files.

Inclusions
This course is open to graduate students from all research groups, not only from Electronics Group, and serves as introductory core course to *digital and mixed-signal IC design methodology*.

Exclusions
Students should not enroll in this course if they:
(1) possess good prior knowledge of IC design CAD tools from Cadence *or*
(2) possess advanced prior knowledge of digital IC design flow *or*
(3) are interested in purely circuit design (as opposed to *design methodology*) *or*
(4) cannot attend course lectures due to time conflicts *or*
(5) cannot allocate sufficient time to the course projects (that tend to be time-consuming).

Procedure for asking questions, in the order of priority:

Please note that not following this procedure closely may reflect on a student's mark, as well as their standing in class and reputation.

1. **Please post your questions (and answer questions by others to earn points for the course grade) on Piazza**. Nearly all questions in this course should be posted on Piazza. **Please adhere to the following guidelines that set expectations from all students**:

- **Do not disclose solutions** to assigned project problems when posting your questions.
- **Read all past posts** so that you do not repeat questions that have been answered.
- A high degree of **independent decision making is expected** in a graduate course, so make your best genuine effort to try to resolve your question on your own before posting.
- **Posting questions that have been answered, or questions that show that genuine effort to resolve this question before posting as expected from a graduate student has not been put in, or questions that show a student did not read an assignment carefully or does not have pre-requisites for this course** (e.g., knowledge of how to use UNIX commands at a prompt or knowledge of CMOS circuit design from an undergraduate course), **may reflect on that student's mark, as well as their standing in class and reputation.**

2. In rare cases, when you have a **very personal question relating to you only** (e.g., missing a class/deadline due to health issues, etc.) you can email ask1388@eecg.utoronto.ca – **please state at the beginning of your message why your question is not suitable for posting on Piazza and needs to be answered by email**. **Please make sure to include "ECE1388" in the subject line of your message so that it is not missed.**

3. Approach your instructor or TA before or during a break in any lecture or tutorial.

Lecture topics covered:

- The lectures serve to *review (mostly) digital circuit design topics* as needed to complete all projects in the course:
    1. Introduction to MOS Transistors and to Digital Circuits
    2. Layout and Fabrication
    3. CMOS Transistor Theory
    4. Non-Ideal Transistors
    5. DC & Transient Response
    6. CMOS Processing Technology
    7. Design for Optimum Speed: Logical Effort
    8. Design for Low Power
    9. Interconnect and Wire Engineering
    10. Packaging, Power and I/O
    11. Combinational Logic
    12. Digital Circuit Families
    13. Sequential Logic
    14. SRAM, DRAM and flash memories
    15. Design for Testability

Lab topics covered:

- There are 4 take-home labs. VLSI User's Manual is the basis for the labs as follows:
    1. Introduction. Cadence: A Beginner's Guide and Schematic Entry (Ch. 1-3)
    2. Cadence: Physical Layout and Analog Simulation (Ch. 4-5)
    3. Cadence: Digital Simulation with Hardware Description Languages (Ch. 6)
    4. Synopsis and Cadence: Logic Synthesis and Optimization; Place and Route (Ch. 7-8)
- The lab sequence is intended to gradually expose students to CAD tools design environments in order to complete the projects.
- TAs will answer questions by email

Tutorial topics covered:

- The tutorials provide intensive training in the use of CAD tools:
    1. Cadence Virtuoso Schematic Editor
    2. Cadence Virtuoso Layout Editor
    3. Layout of Parameterized Cells (P-cells)
    4. Digital Design Flow, from Synthesis to Place-and-route
    5. Verilog-A Language
    6. Mixed-signal Simulations within Cadence Virtuoso AMS Environment

Course projects (done individually, *any plagiarism will constitute academic offense*)

- The three course projects will be based on the labs, tutorials and textbook as follows:
    1. Device and Circuit Characterization and Basic Layout (Design Example: CMOS Transistor and Inverter)
    2. Digital Circuit and Layout Design for Optimum Performance (Design Example: 5-bit Register Decoder)

3. Digital Circuit Synthesis and Layout Place-and-Route (Design Example: 4x4-bit Unsigned Array Multiplier)

Note: the projects are simplified to the extent possible, but are time consuming due to the design methodology-oriented nature of the subject. *Please plan your time accordingly and start several weeks in advance of each deadline*.

Final project (team-based, typically teams of 4-5 students)

- The final project guides student teams through a simplified practical flow of a complete integrated circuit (IC) design starting from the project definition and system outline to the complete verified IC layout including a padframe. The project aims to help students apply skills learned in this course and other courses to the design of a die-level CMOS integrated circuit. The default final project topic is the Design of a CMOS Image Sensor Integrated Circuit. Some students may choose a different topic, subject to limitations.

- The final project runs in weeks 7-14 with the following weekly milestones:
    1. Group formation and project definition
    2. System outline (Written update 1)
    3. Circuit cells and simulations (First presentation, written update 2)
    4. Complete schematic
    5. Cell layout (Written update 3)
    6. Complete layout within a pad frame (Final presentation)
    7. LVS final check (Final report)

- The goal of the project is for students to develop/polish and demonstrate a number of skills including but not limited to:
    1. Understanding and mastery of the IC design flow
    2. Knowledgeable utilization of all lecture material within the final project
    3. Performing optimal circuit and layout design as part of an IC design flow
    4. Demonstrated ability to work efficiently within an IC design team
    5. Ability to communicate results effectively by way of two oral presentations
    6. Understanding all presentations and participation by asking/answering questions

- Previous years' final project web reports are available here 2004, 2006, and 2016 (topics listed can be outdated today, but the methodology is valid).

Grade breakdown

Course projects	30% - Total for the three individual projects
Final project	60% - The breakdown is given in the final project handout.
Class participation	10% - **Students are expected to participate in Piazza discussion by actively reading and answering questions from other students** – and this will be reflected in everyone's course grade. Piazza provides statistics on how many (correct and timely) answers each student has provided, demonstrating a student's learning progress, competence and engagement, and this information will contribute to this component of their course grade. Outside of the academic settings, online team discussions and group forums

	may often be the only available source of information, so we will emulate this in the course. (Please note that projects 1-3 are done independently, so directly sharing their solutions is not allowed, but other related questions can and should be answered.)

Course Website

The course will be administered via *Quercus*. All students must be able to access the website. Course announcements and handouts will be posted to this website. Within *Quercus*, we will be using:

Piazza – This term we will be using Piazza for class discussion and Q/A. Piazza is optimized for getting you the help you need fast and efficiently from classmates, the TAs, and the instructor. Rather than emailing the teaching staff, please post your questions and answers on Piazza. YOUR CORRECT AND TIMELY ANSWERS WILL BE COUNTED AND WILL CONTRIBUTE TO YOUR COURSE GRADE.

Cell Phone / Tablet / Laptop Usage In Class

Technology can support student learning, but it can also become a distraction. Research indicates that multi-tasking (texting, surfing the Internet, using social networks) during class time can have a negative impact on learning (Clapp, Rubens, Sabharwal & Gazzaley, 2011; Ellis, Daniels, Jauregui, 2010; Hembrooke & Gay, 2003). Out of respect for your fellow learners in this class, please **refrain from using laptops, tablets or mobile phones for entertainment during class** and do not display any material on a laptop which may be distracting or offensive to your fellow students. **Laptops/tablets may be used only for legitimate classroom purposes**, such as taking/reading class notes, downloading course information from Portal, or working on an assigned in-class exercise. Checking social media, email, texting, games, and surfing the Web are not legitimate classroom purposes. Such inappropriate laptop and mobile phone use is distracting to those seated around you.

Use of Generative Artificial Intelligence Tools

Students may use artificial intelligence tools, including generative AI, in this course as learning aids or to help produce assignments. However, students are ultimately accountable for the work they submit.

Students may not use artificial intelligence tools for taking tests, writing research papers, creating computer code, or completing major course assignments. However, these tools may be useful when gathering information from across sources and assimilating it for understanding.

The knowing use of generative artificial intelligence tools, including ChatGPT and other AI writing and coding assistants, for the completion of, or to support the completion of, an examination, term test, assignment, or any other form of academic assessment, may be considered an academic offense in this course.

Academic Integrity

All students are expected to follow the University's guidelines and policies on academic integrity. This means following the standards of academic honesty when writing assignments, collaborating with fellow students, and writing tests and exams. Ensure that the work you submit for grading represents your own honest efforts. Plagiarism—representing someone else's work as your own or submitting work that you have previously submitted for marks in another class or program—is a serious offence that can result in sanctions. Speak to the instructor or your TA for advice on anything that you find unclear. To learn more about how to cite and use source material appropriately and for other writing support, see the U of T writing support website. Consult the Code of Behaviour on Academic Matters for a complete outline of the University's policy and expectations. For more information, please see the U of T Academic Integrity website.

Notice of Video Recording / Sharing (*Download permissible; re-use prohibited*)

At any time during this course, some course participant interactions including your participation, may be recorded on video and will be available to students in the course for viewing remotely and after each session.

Course videos and materials belong to the instructors, the university, and/or other source depending on each specific situation, and are protected by copyright. In this course, students are permitted to download session videos and materials for their own academic use, but ***students may not copy, share, or use them for any other purpose*** without the explicit permission of the instructor.