

ECE1388 VLSI Design Methodology

Lecture 3: CMOS Transistor Theory

The Ideal MOS Transistor



**Fully Surrounding
Metal Electrode**



**Fully Enclosed,
Depleted
Semiconductor**

**High-K
Gate Insulator**

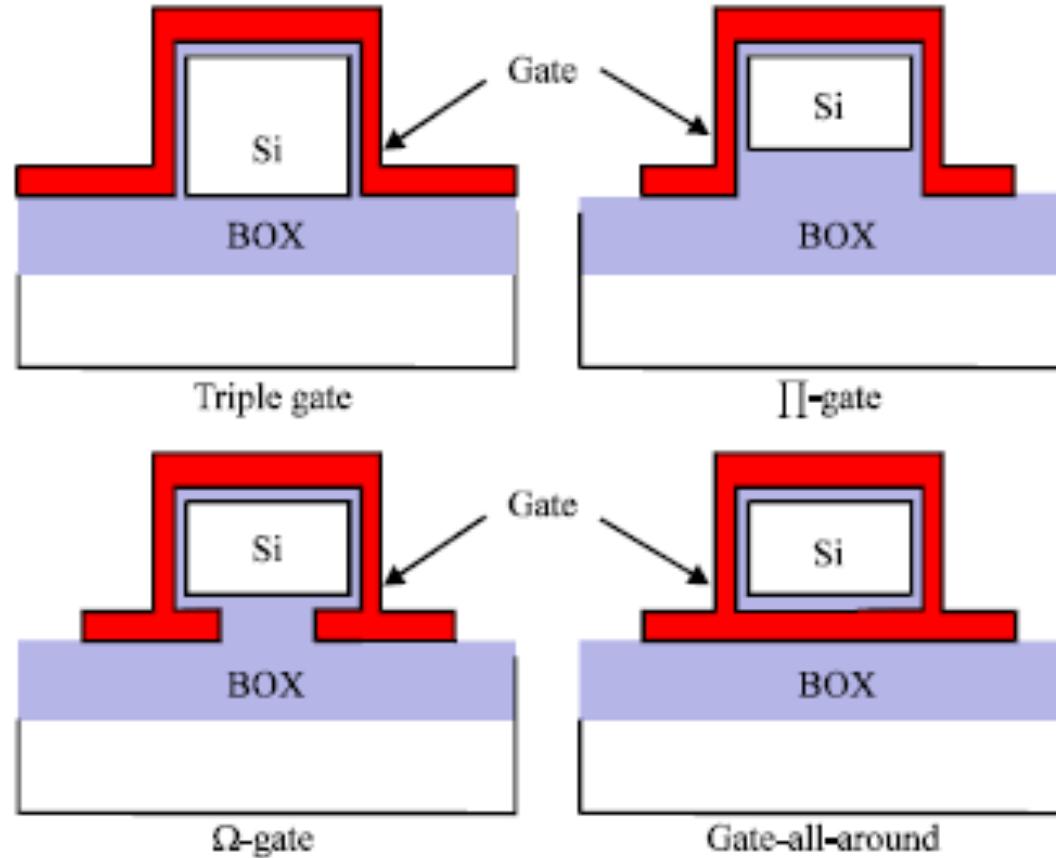
Allows for thicker
oxide for same
capacitance

**Band Engineered
Semiconductor**

**Low Resistance
Source/Drain**

From My Files

Multiple-gate FET concepts

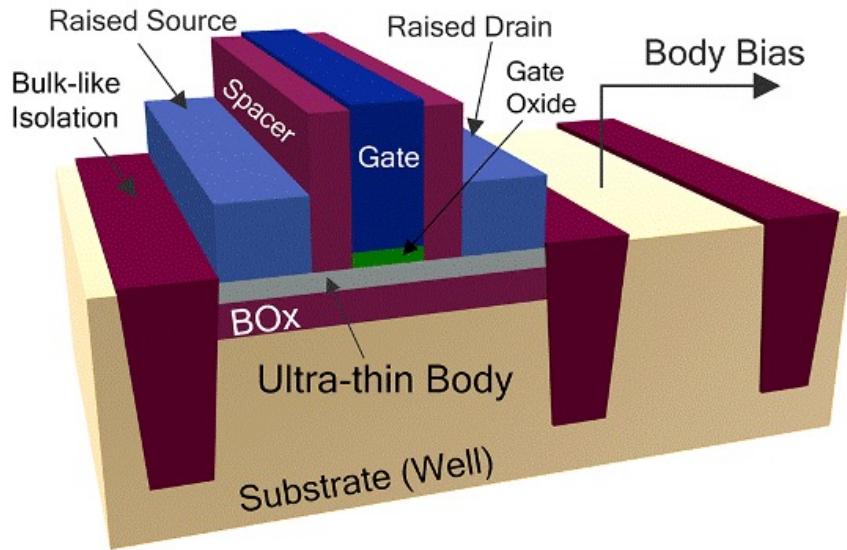


BOX: buried oxide

The Future of Non-planar Nanoelectronics MOSFET Devices: A Review," M.A. Riyadi et al, 2010

Most Real Transistors

2-D quasi 2-gate FD-SOI (ST)

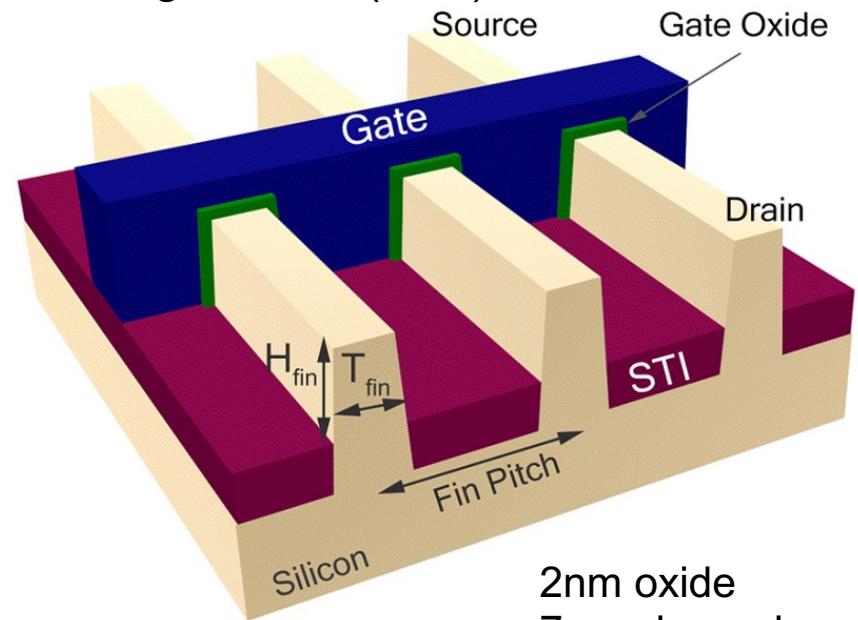


Side-wall **spacers** control short channel effects by offsetting ion implantation profiles from the edge of the gate

BOX: buried oxide

STI: shallow-trench isolation

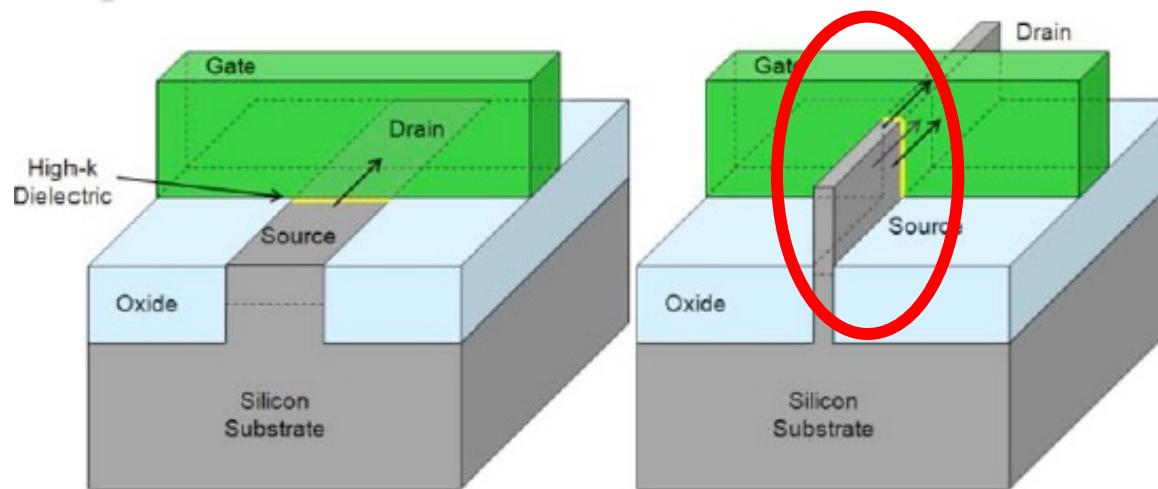
3-D trigate FET (Intel)



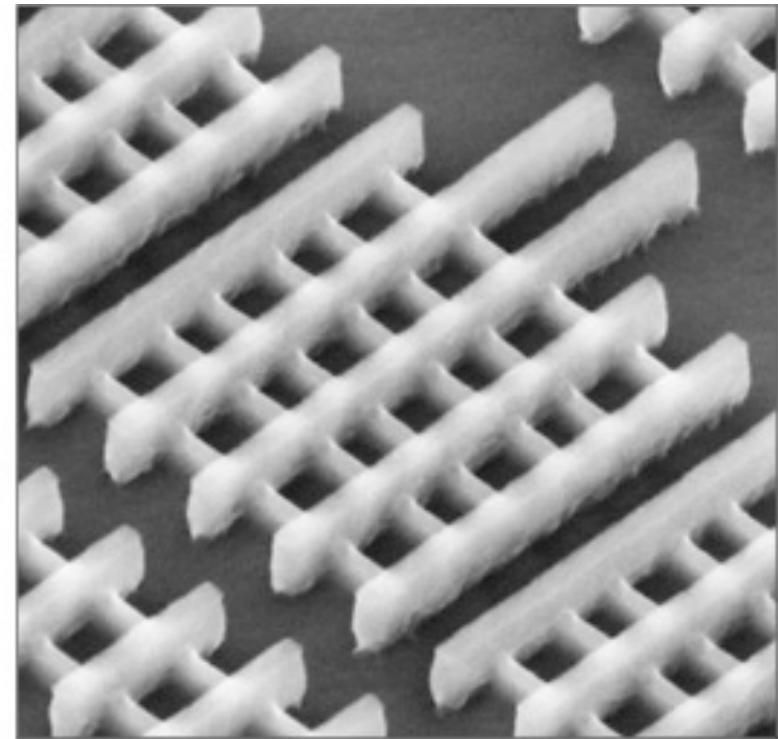
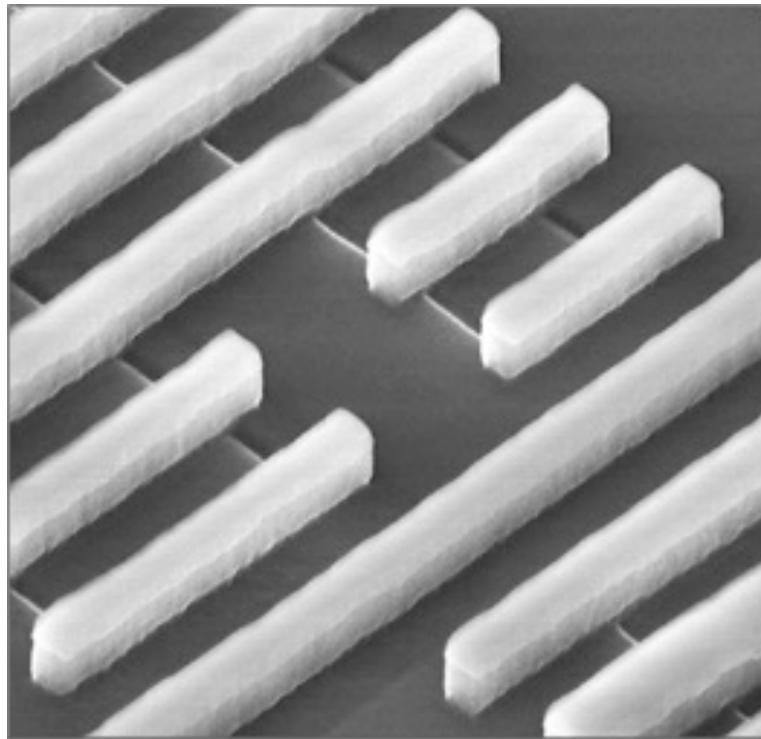
2nm oxide
7nm channel
20-24nm gate length
> 300 GHz speed

- **Better switch** - for same I_{on} :
 - lower I_{off} (lower off current)
 - lower V_{dd} (better electrostatics)

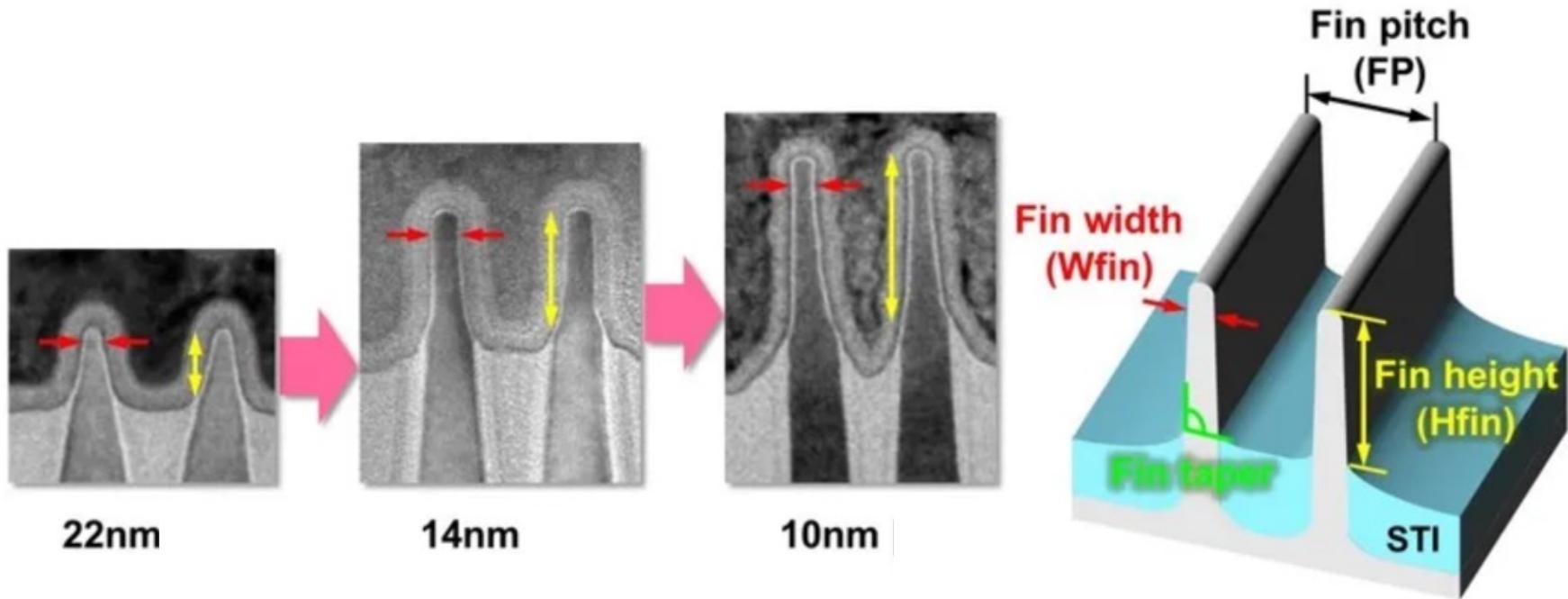
32nm planar vs. 22nm FinFET CMOS ICs



Intel



Transistor Fin Improvement



- Higher and narrower profiles are required for:
 - lower off current &
 - better electrostatics
- Key physical parameters

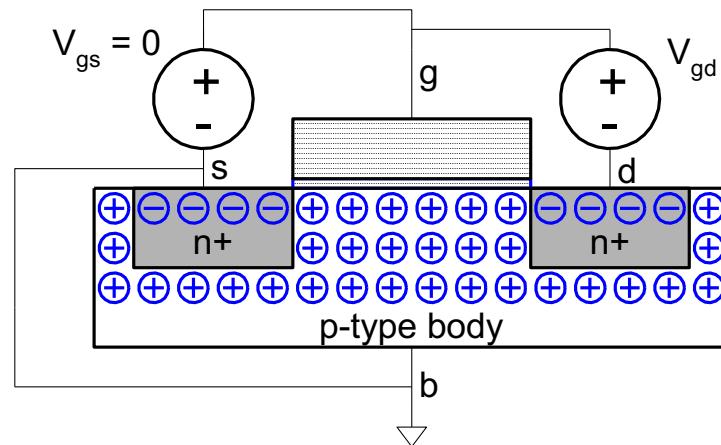
Semi Eng by Matt Cogorno

nMOS Cutoff

- ❑ No channel
- ❑ $I_{ds} = 0$

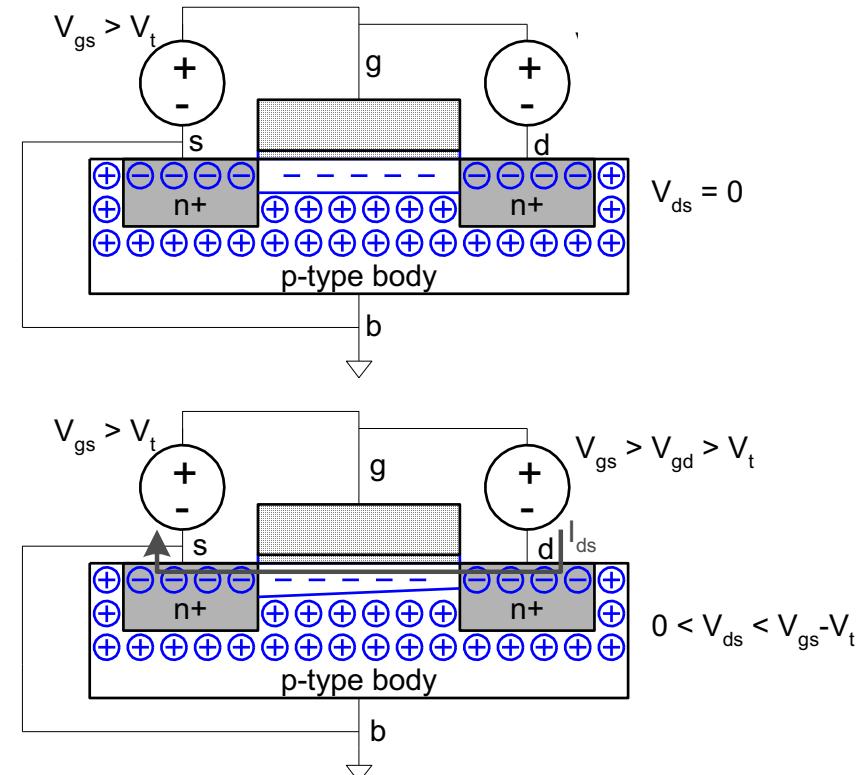
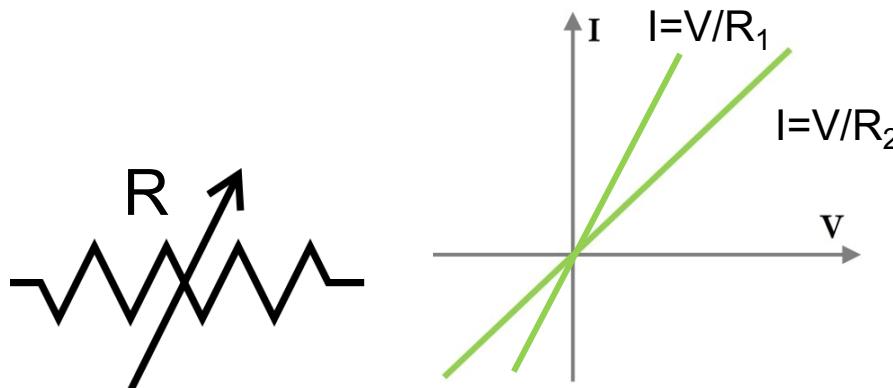


OFF SWITCH



nMOS Linear

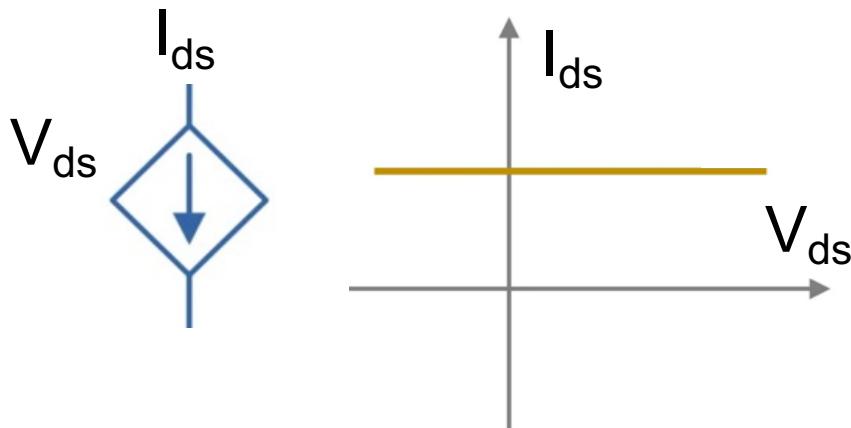
- Channel forms
- Current flows from d to s
 - e^- from s to d
- I_{ds} increases with V_{ds}
- Similar to **linear resistor**



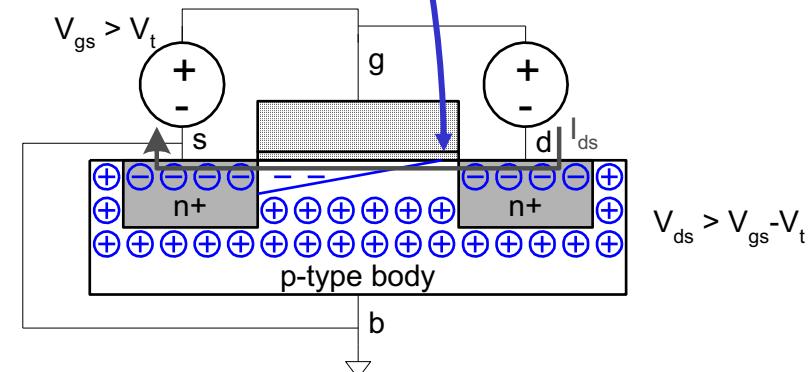
**VOLTAGE-CONTROLLED
RESISTOR**

nMOS Saturation

- ☐ Channel pinches off
- ☐ I_{ds} independent of V_{ds}
- ☐ We say current saturates
- ☐ Similar to **current source**
 - Used as an amplifier



CONTROLLED
CURRENT SOURCE



I-V Characteristics

- In Linear region, I_{ds} depends on
 - How much charge is in the channel?
 - How fast is the charge moving?
- $I_{ds} = C (\Delta V / \Delta t) = \Delta Q / \Delta t = Q_{\text{channel}} / t$
 - Q_{channel} - ?
 - t - ?

nMOS I-V Summary

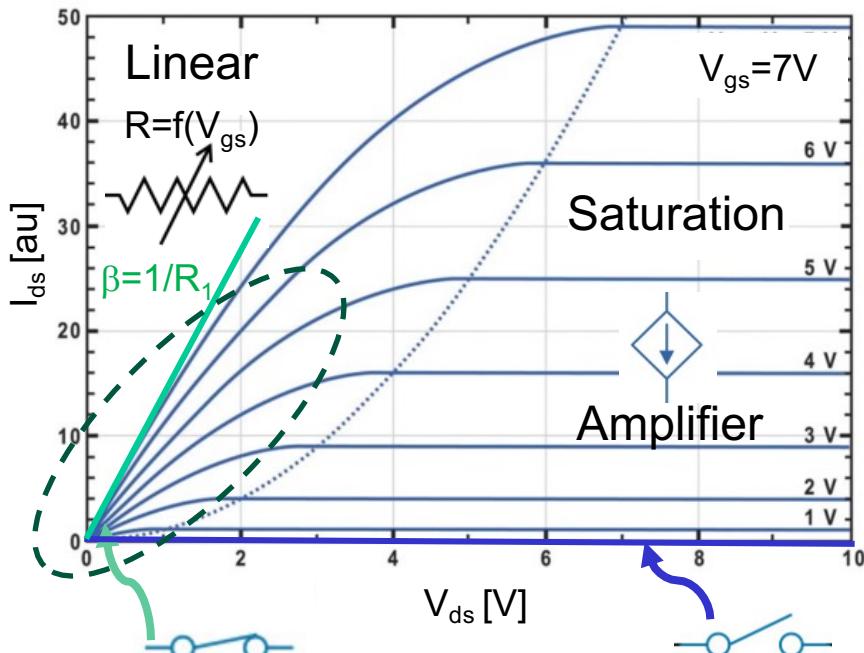
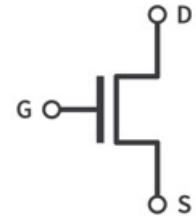
- Shockley 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2} \left(V_{gs} - V_t \right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

$$\beta = \mu C_{\text{ox}} \frac{W}{L}$$

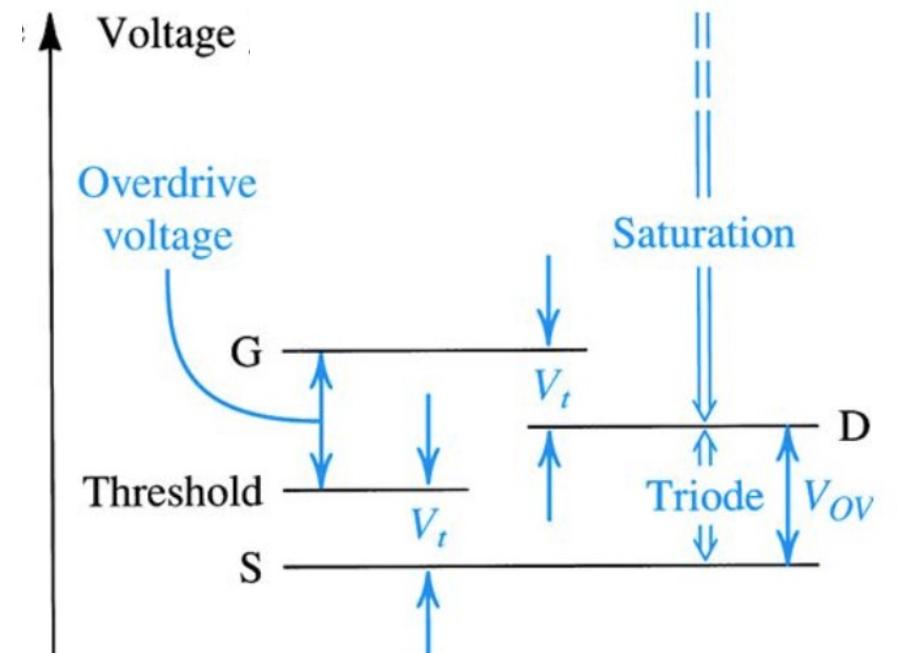
nMOS Modes of Operation

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$



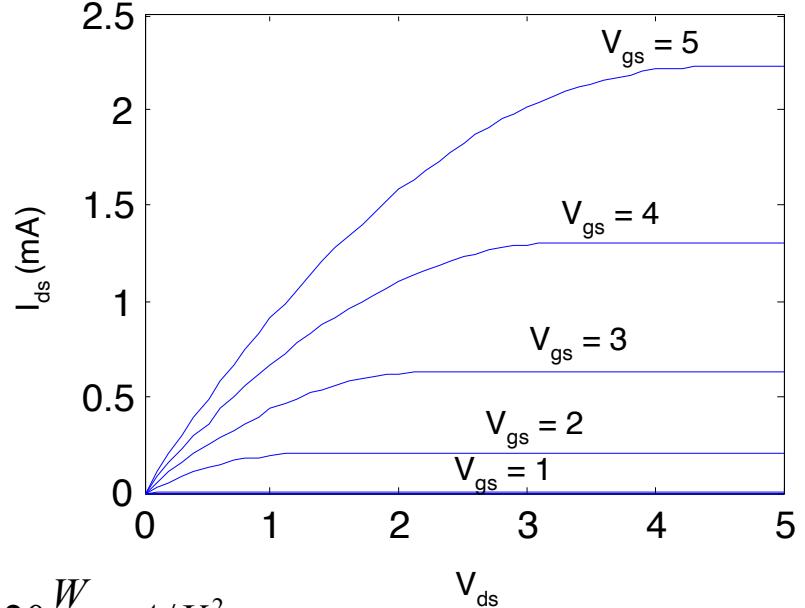
3: CMOS Transistor Theory

VLSI Design Methodology



Example

- A nMOS transistor in a 0.6 μm process
 - $t_{\text{ox}} = 100 \text{ \AA}$
 - $\mu = 350 \text{ cm}^2/\text{V}\cdot\text{s}$
 - $V_t = 0.7 \text{ V}$
- Plot I_{ds} vs. V_{ds}
 - $V_{\text{gs}} = 0, 1, 2, 3, 4, 5$
 - Use $W/L = 4/2 \lambda$



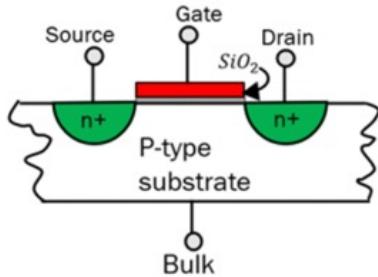
$$\beta = \mu C_{\text{ox}} \frac{W}{L} = (350) \left(\frac{3.9 \cdot 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}} \right) \left(\frac{W}{L} \right) = 120 \frac{W}{L} \mu\text{A}/\text{V}^2$$

pMOS I-V

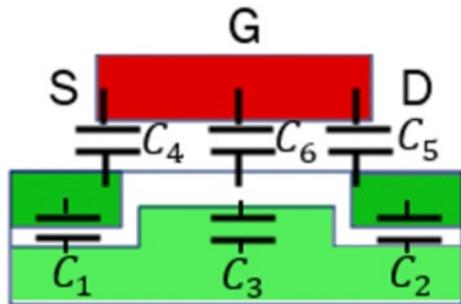
- All dopings and voltages are inverted for pMOS
- Mobility μ_p is determined by holes
 - **Typically 2-4x lower than that of electrons μ_n**
 - $120 \text{ cm}^2/\text{V}\cdot\text{s}$ in a $0.6 \mu\text{m}$ process
- Thus **pMOS must be wider to provide same current**
 - For simplicity, will sometimes assume $\mu_n / \mu_p = 2$

MOS Capacitances

- Any two conductors separated by an insulator have capacitance



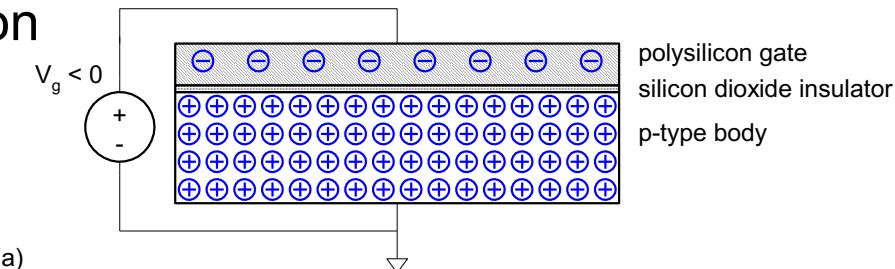
- **Gate-to-channel** capacitor is very important
 - C_6 - creates channel charge necessary for operation



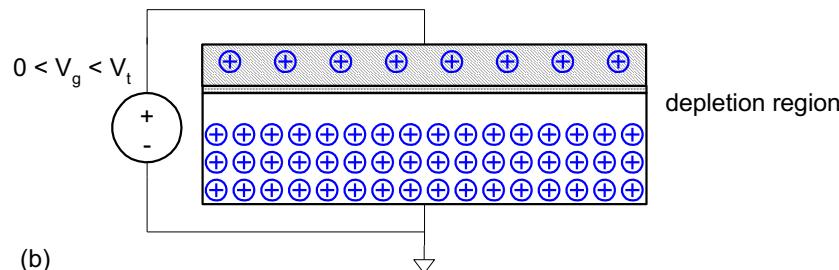
- **Source & drain have capacitance to body**
 - $C_{1,2}$ - across reverse-biased diodes
 - Called diffusion capacitance because it is associated with source/drain diffusion

MOS Capacitor

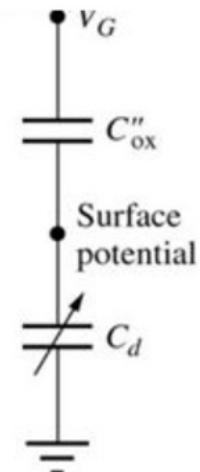
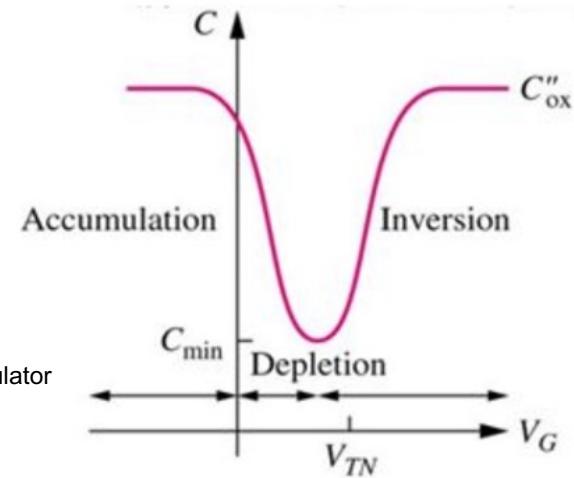
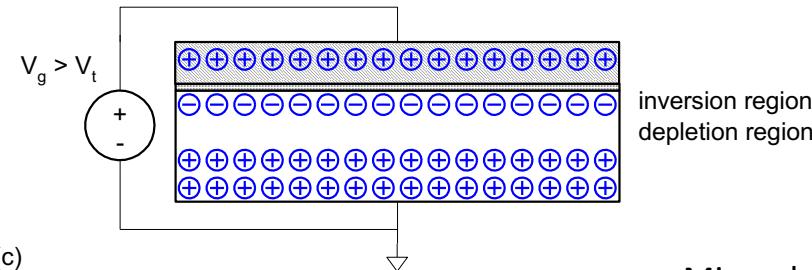
- Gate and body form MOS capacitor
- Operating modes
 - Accumulation



- Depletion

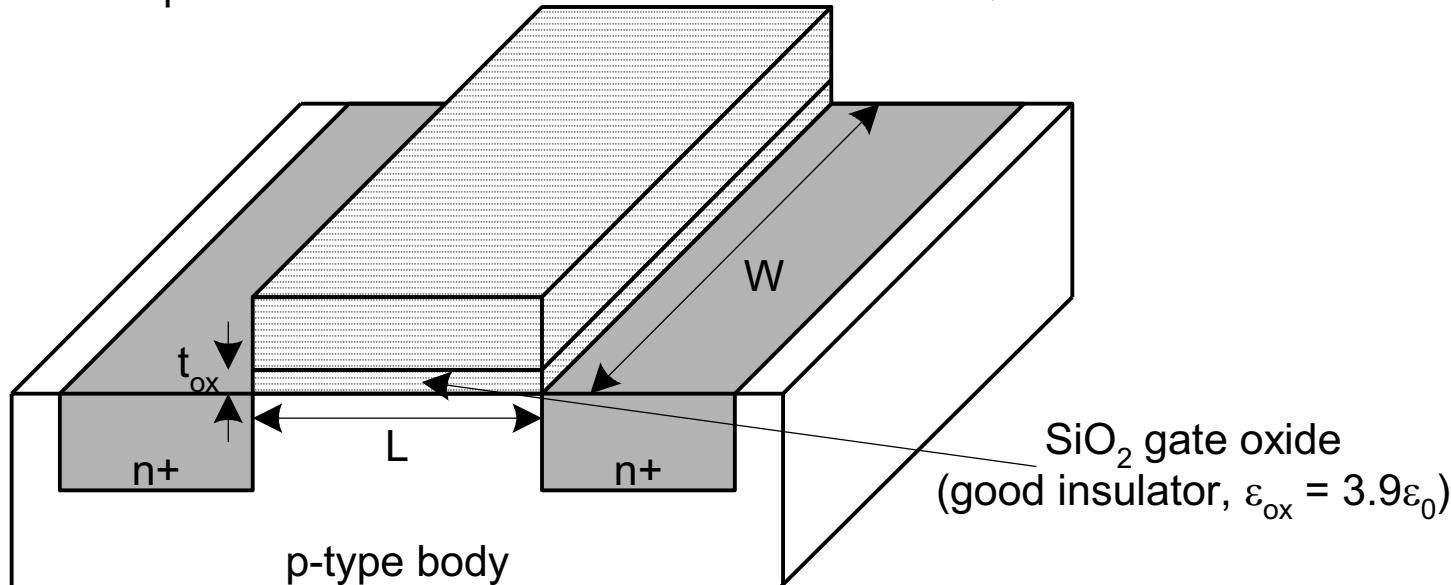


- Inversion



Gate Capacitance

- Approximate channel as connected to source
- $C_g = \epsilon_{ox} WL/t_{ox} = C_{ox} WL = C_{permicron} W$ (approx.= C_{gs})
- Linear: $C_{gs} = 1/2 C_g$; Saturation: $C_{gs} = 2/3 C_g$
- $C_{permicron}$ is typically about 2 fF/ μ m



Diffusion Capacitance

- C_{sb}, C_{db}
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
 - Use small diffusion nodes
 - **Contacted** diff in (b)
 - Comparable to C_g
 - Will assume $=C_g$
 - **Uncontacted** diff in (c)
 - Somewhat smaller
 - But not significantly
 - Will assume $=C_g$
 - Varies with process

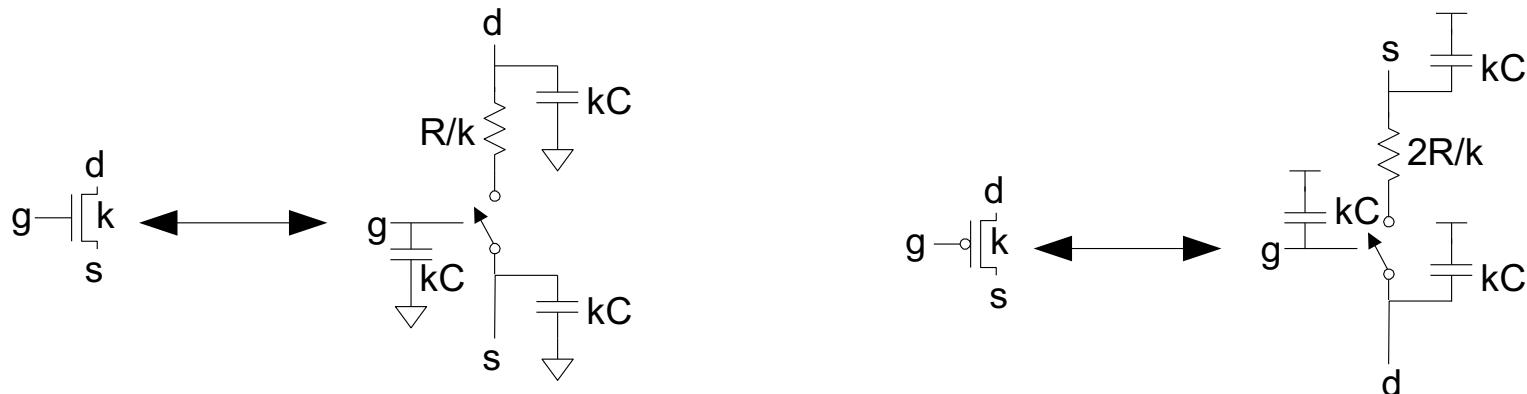


Effective Resistance

- Shockley models have limited value
 - Not accurate enough for modern transistors
 - Too complicated for much hand analysis
- Simplification: **treat transistor as resistor**
 - Replace $I_{ds}(V_{ds}, V_{gs})$ with effective resistance R
 - $I_{ds} = V_{ds}/R$
 - **R averaged across switching of digital gate**
- Too inaccurate to predict current at any given time
 - But **good enough to predict RC delay**

RC Delay Model

- Use equivalent circuits for MOS transistors
 - **Ideal switch + capacitance and ON resistance**
 - Unit nMOS has resistance R , capacitance C
 - Unit pMOS has resistance $2R$, capacitance C
- **Capacitance proportional to width**
- **Resistance inversely proportional to width**

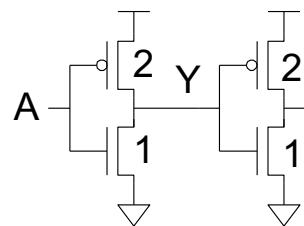


RC Values

- Capacitance
 - $C = C_g = C_s = C_d = 2 \text{ fF}/\mu\text{m}$ of gate width
 - Values similar across many processes
- Resistance
 - $R \approx 6 \text{ K}\Omega \cdot \mu\text{m}$ in 0.6um process
 - Improves with shorter channel lengths
- Unit transistors
 - **May refer to minimum contacted device ($4/2 \lambda$)**
 - Or maybe 1 μm wide device
 - Doesn't matter as long as you are consistent

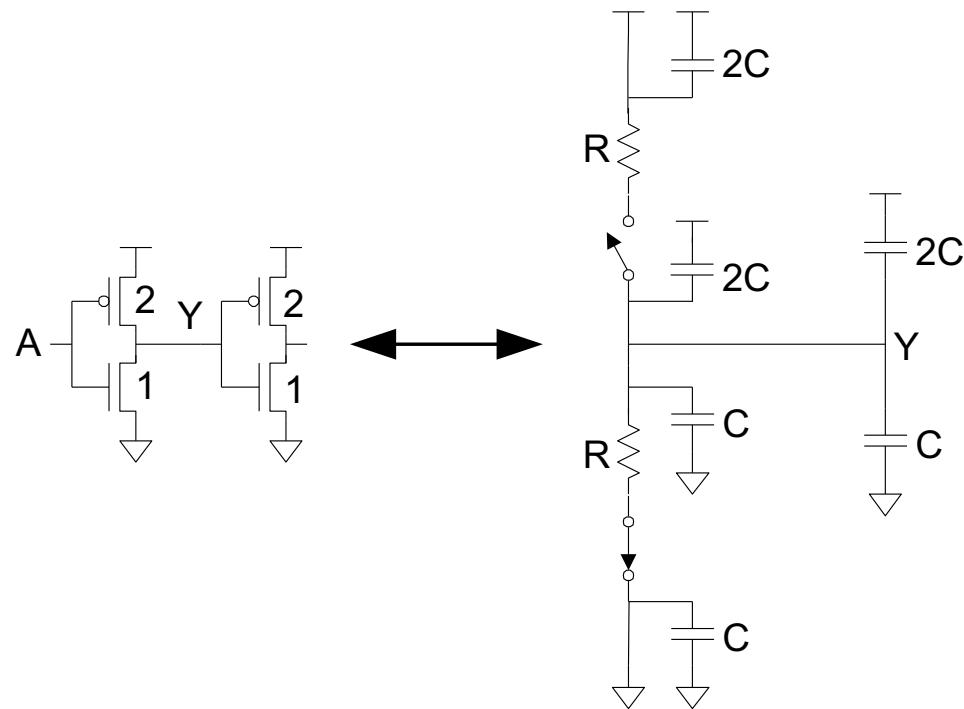
Inverter Delay Estimate

- Estimate the delay of a fanout-of-1 inverter



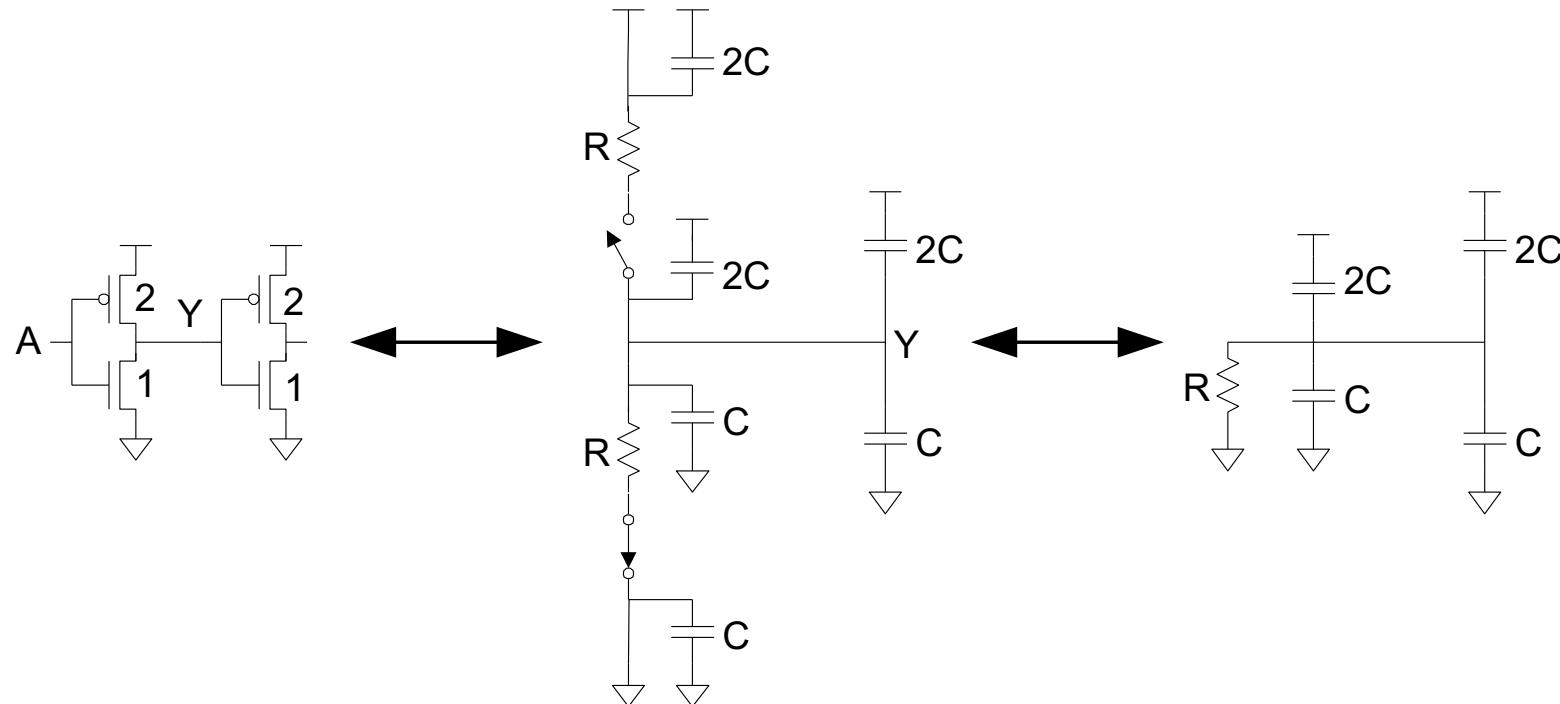
Inverter Delay Estimate

- Estimate the delay of a fanout-of-1 inverter



Inverter Delay Estimate

- Estimate the delay of a fanout-of-1 inverter

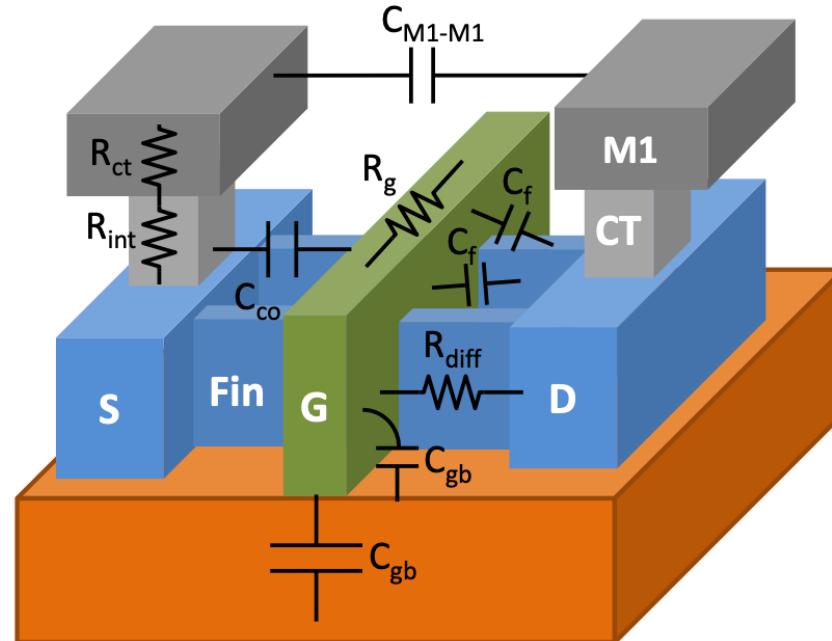


$$t_{pd} = \tau = 6RC$$

Extra RC Parasitics in FinFET

A better switch (lower I_{off} and lower V_{dd} for same I_{on}) but has higher parasitics

- Large contact resistance
- Low layer metals and poly have high resistance
- Tight metal pitches lead to large parasitic capacitances



Cap	Planar	FinFET
C_f		2.0X
C_{co}	1X	1.8X
C_{gb}		1.2X

Res	Planar	FinFET
R_g		1.5-2.5X
R_{ct}		1.5X
R_{int}	1X	1.3X
R_{diff}		1.3X

ISSCC'18 L. Loh; and CMC Workshop by TC Carusone