

Collection

Users can Collect posts into a printable, sortable format. Collections are a good way to organize posts for quick reading. A Collection must be created to tag posts. More Help

Thread:	Problem starting design_analyzer	Posted Date:	October 7, 2016 1:36 PM
Post:	Problem starting design_analyzer	Status:	Published
Author:	 Roman Genov	Overall Rating:	

Hello,

I have been working through chapter 7 in the "VLSI User Manual" and have been unable to get the design analyzer working. I have followed the instructions in the user manual to set up the environment but when I use the command "design_analyzer &". I get the following message:

/CMC/tools/synopsys/syn_vX-2005.09/linux/syn/bin/dc_view_exec: error while loading shared libraries: libtermcap.so.2: cannot open shared object file: No such file or directory

[1] Exit 127 design analyzer

Any help would be appreciated,

Peter

Tags: None

(Post is Unread)

Thread:	DRC problem	Posted Date:	October 20, 2016 8:39 PM
Post:	DRC problem	Status:	Published
Author:	 Roman Genov	Overall Rating:	

I am running DRC for inverter. The problem shown that "need nohmic within 5um of PMOS/avdcap/pdiffR/plres", couldn't figure it out. I have 9 PMOS in parallel, 4 of them shown the problem mention before.

Same problem happened to my NMOS, "need pohmic within 5um of NMOS/ndiffR/nwellR/PNPvertical"

Tags: None

(Post is Unread)

Thread:

EDI - SOC Encounter problem

Post:

EDI - SOC Encounter problem

Author:

 Roman Genov

Posted Date:

October 29, 2016 5:24 PM

Status:

Published

Overall Rating:

Hi,

I was trying to set up EDI following the VLSI manual. But i am getting the following errors, and COULD not run the tool....

This version was compiled on Thu Jul 15 13:17:23 PDT 2010.

Set DBUPerIGU to 1000.

Set net toggle Scale Factor to 1.00

Set Shrink Factor to 1.00000

Encounter terminated by internal (SEGV) error/signal...

*** Stack trace in log file.

Any idea? Thanks

Tags: None

(Post is Unread)

Thread:

Cannot find the IBM 0.13um Standard Cell Verilog file

Posted Date:

October 31, 2016 11:53 AM

Status:

Published

Overall Rating:

Post:

Cannot find the IBM 0.13um Standard Cell Verilog file

Author:

 Roman Genov

Hello everyone,

I cannot find the IBM 0.13um Standard Cell Verilog file in order to copy to the project working directory for Prj 3.How I can tackle this problem ?

With Regards,

Christos

Tags: None

(Post is Unread)

Thread: How to get back cmos35p shortcuts for cmrf8sf
Post: How to get back cmos35p shortcuts for cmrf8sf
Author:  Roman Genov

Posted Date: November 9, 2016 9:07 PM
Status: Published
Overall Rating:

I was wondering if anyone knew their way around the shortcut definition for the cmrf8sf library

Tags: None

(Post is Unread)

Thread: Standard Cell Library for CMRF8SF - Schematic Simulation

Post: Standard Cell Library for CMRF8SF - Schematic Simulation

Author:  Roman Genov

Posted Date: November 12, 2016 5:05 PM
Status: Published
Overall Rating:

I have been trying to import synthesized verilog (using ncverilog) files to Cadence to no success.

It seems that whatever Standard Cell Libraries available for Cadence (as found on Jaro's notes /CMC/kits/artisan-8rf/==README.jaro) are only symbol views.

Symbol views can't be simulated with the Cadence Analog tools.

So my question is:

- How, and can we do "spice-style" simulations with our synthesized Verilog schematics?

Tags: None

(Post is Unread)

Thread: Tutorial #6 - cannot open shared object file

Post: Tutorial #6 - cannot open shared object file

Author:  Roman Genov

Posted Date: November 16, 2016 6:43 PM
Status: Published
Overall Rating:

Hi, I'm encountering a strange problem in Tutorial #6 setting up environment step.

Apparently a shared library called "libXp.so.6" is missing - see screen-shot.

Does anyone else encountered the same issue?

Thanks all

Attachment:  Screen Shot 2016-11-16 at 18.41.55.png (65.123 KB)

Tags: None

(Post is Unread)

Thread:
CMRF8SF -- No valid layers in LSW

Post:
CMRF8SF -- No valid layers in LSW

Author:  Roman Genov

Posted Date: November 19, 2016 3:16 PM
Status: Published
Overall Rating:

Hello,

When I try to layout the final project using CMRF8SF technology, I find there is NO Valid Layers in LSW. There are three warnings when opening Virtuoso.

Can someone help me, please?

Thanks a lot,

Shengze

Attachment:  No_valid_layer_purpose_pairs.png (38.596 KB)

Tags: None

(Post is Unread)

Thread:
How to importing synthesized verilog with ibm13frvt.v?

Post:
How to importing synthesized verilog with ibm13frvt.v?

Author:  Roman Genov

Posted Date: November 19, 2016 7:12 PM
Edited Date: November 19, 2016 7:18 PM
Status: Published
Overall Rating:

Dear All,

I was successfully able to run AMS (mixed signal simulations) by importing multiplier verilog (unsynthesized) from project 3 to just familiarize myself with the flow mentioned in "TUTO6 - Mixed signal simulations.pdf". Simulation waveforms worked as expected.

Later, when I tried importing the multiplier_syn.v (synthesized verilog code), the import log showed up with bunch of low level blocks (i.e OA21XLTF, AOI22X1TF ...)

missing in my libraries which are specified in ibm13rfrvt.v verilog file.

So then I decided to import ibm13rfrvt.v verilog code in cadence so that I can have those missing low level cell views available in cadence. When I imported ibmrf13rv.v (fig 1) file, it created all the cell view blocks which are in the ibm13rfrvt.v file as verilog modules BUT it just created the symbol views (nothing like functional or schematic or verilog views which are useful for simulations, see fig 2). Then when I re-tried to import my multiplier_syn.v (synthesized verilog) it showed me following errors in import log (fig 3, fig 4).

The main question is that is there a library containing verilogams or functional blocks that are inside ibmrf13rv.v file so that we can simulate synthesized verilog code?

Attachment:  ams simulation import.tar.gz (154.161 KB)

Tags: None

(Post is Unread)

Thread: ERC errors
Post: ERC errors

Posted Date: November 22, 2016 5:10 PM
Status: Published
Overall Rating:

Author:  Roman Genov

Hi,

I asked this question in today's lecture.

I am using ibm 0.13um for the project. I have my part DRC and LVS clean but have a lot of ERC errors.

Unlike LVS, ERC doesn't show the errors in detail, the only thing I can do is click on each error and it will show me where the problem is, without any explanation. The errors exist on a lot of contacts and poly.

I followed the way I did the layout in 0.35um. Is there something special for 0.13um? Or is there a way I can see what caused the errors?

Thank you.

Tianxiang

Attachment:  Picture1.jpg (70.662 KB)

Tags: None

(Post is Unread)

Thread: LVS BOX and EXCLUDE CELL
Post: LVS BOX and EXCLUDE CELL
Author:  Roman Genov

Posted Date: December 1, 2016 8:59 AM
Status: Published
Overall Rating:

Hi,

I am a bit confused on how to use LVS BOX and EXCLUDE CELL to get lvs clean for netlist exported from encounter.

So now the problem is that we are missing layout/schematic for 0.13 IBM standard cell library. My understanding is that LVS BOX and EXCLUDE CELL are some commands from Mentor Grapgics Calibre tool that we can use to kinda "skip" the standard cells while checking top level connections.

Ok... Question : while we are expecting to use Cadence Virtuoso to read in the def , netlist (or stream in GDS), and run LVS check, how do we use commands from Mentor Graphics ?? They are different tools. How do we get them to work !??? Maybe I misunderstood something here ?! Anyone has any ideas?

Thanks,

Genwen

Tags: None

(Post is Unread)

Thread: problem opening Virtuoso AMS environment
Post: problem opening Virtuoso AMS environment
Author:  Roman Genov

Posted Date: December 8, 2016 11:07 PM
Status: Published
Overall Rating:

Hi,

I am having problem starting cadence by following the steps in TUTO6. it gives me the following errors:

/CMC/tools/cadence/IC.5141.USR5.linux/tools/dfII/bin/32bit/icms.exe: error while loading shared libraries: libXp.so.6: cannot open shared object file: No such file or directory

[1] Exit 127 icms

I check that I do have access to /CMC/tools/cadence/IC.5141.USR5.linux/tools/dfII/bin/32bit/icms.exe. so I am confused now.

Anyone else has this problem??

Thanks

Yifeng

Tags: None

(Post is Unread)

Thread:

problem opening Cadence Virtuoso with 0.13nm library

Post:

problem opening Cadence Virtuoso with 0.13nm library

Author:



Roman Genov

Posted Date:

December 9, 2016 11:55 AM

Status:

Published

Overall Rating:

Hi all,

I am having some errors when loading the cadence virtuoso with cmrf8 library .. I am sure it worked fine for me before.. so not sure what happend..

I logged into ug250 machine with shh VNC.

Please see the picture for error and provide feedback/solution if you had the same problem before.

Thanks,

Genwen

Attachment: Capture.JPG (20.378 KB)

Tags: None

(Post is Unread)

Thread:

ERC Failing to run

Post:

ERC Failing to run

Author:

Anonymous

Posted Date:

September 21, 2017 3:35 PM

Status:

Published

Overall Rating:

Hi,

I am having a problem related to section 4.4 in the lab manual. When I attempt to run the ERC check on the extracted layout of my ring oscillator I get a message informing me that the ERC job has failed. When I attempt to view the associated errors, the CIW terminal informs me that no error file exists. My layout passes the DRC with no problems. What is the cause for this? Any help is appreciated.

Thanks

Tags: None

(Post is Unread)

Thread: Poly1 to Metal1 via
Post: Poly1 to Metal1 via
Author:  Ming Jia Gong

Posted Date: September 22, 2017 1:47 PM
Edited Date: September 22, 2017 1:53 PM
Status: Published
Overall Rating:

Hi,

Did anyone manage to create a via from poly1 layer to metal1 in Cadence?

I can't seem to find any way to create one, only from one metal layer to another metal layer, and DRC keeps giving me a "floating poly1" error.

Tags: None

(Post is Read)

Thread: Poly1 to Metal1 via
Post: RE: Poly1 to Metal1 via
Author:  Ming Jia Gong

Posted Date: September 22, 2017 2:08 PM
Status: Published
Overall Rating:

Nevermind, I found the solution browsing the 2016 Discussion Board

Tags: None

(Post is Read)

Thread: Poly1 to Metal1 via
Post: RE: Poly1 to Metal1 via
Author:  Matthew Walker

Posted Date: September 25, 2017 10:49 PM
Status: Published
Overall Rating:

I had the same feelings as you - wasn't sure if it was a bug or I did something wrong. Via some youtube videos, I discovered this seems to have been fixed/added in later versions of Cadence. I solved it (and future problems like this) by making a minimum-size poly-to-metal1, m1-to-nwell, and m1-to-psubstrate cells, so I can just pull instances of them in, in the future.

Tags: None

(Post is Unread)

Thread:

Remote Login for Cadence on Windows

Post:

Remote Login for Cadence on Windows

Author:

Justin Kim

Posted Date:

September 27, 2017 2:03 PM

Status:

Published

Overall Rating:

I was wondering which programs were used to remote logging into the server for running Cadence on the Windows machine during the tutorial 1/2. I'm currently using Xming and PuTTY to remote login into the server for running Cadence but am running into disconnecting issues as well as laggy interface but I didn't see this happen during the tutorial when Navid was demonstrating Cadence on his Windows laptop.

Thank you.

Tags: None

(Post is Unread)

Thread:

Remote Login for Cadence on Windows

Post:

RE: Remote Login for Cadence on Windows

Author:

Mehrdad Malekmohammadi

Posted Date:

September 29, 2017 4:17 PM

Status:

Published

Overall Rating:

Hi,

If you are connecting from home, the connection would be slow due to the firewalls of u of t network and your connection would be timed out. otherwise if you are connecting inside u of t network, the connection should be fine.

There are many machines to connect to. If you feel the connection is slow, you can always try connecting to other machines.

Cheers,

Tags: None

(Post is Unread)

Thread:

Remote Login for Cadence on Windows

Post:

RE: Remote Login for Cadence on Windows

Author:

Navid Sarhangnejad

Posted Date:

October 3, 2017 3:39 PM

Status:

Published

Overall Rating:

Hi,

I was using VNCServer to my own linux machine in the lab. Outside of university it works pretty fine as well, but you need to make a VPN connection to UofT network.

I am not sure if you can start vnc session on the ug network. You have to check that.

The command to start it is vncserver or vnc4server. You have to check the command manual to run it properly.

Cheers,

Navid

Tags: None

(Post is Unread)

Thread:

Remote Login for Cadence on Windows

Post:

RE: Remote Login for Cadence on Windows

Author:



Matthew Walker

Posted Date:

October 4, 2017 12:34 AM

Status:

Published

Overall Rating:

Quite good performance outside of the UofT network here too. The best thing is to use VNC, and forward a port over ssh to a random ug machine, but X forwarding works well too.

There is this guide for VNC

<http://www.eecg.utoronto.ca/~vaughn/ece297/ECE297/assignments/vnc/vnc.pdf>

Tags: None

(Post is Unread)

Thread:

About include file

Post:

About include file

Author:



Ran Duan

Posted Date:

September 27, 2017 8:48 PM

Status:

Published

Overall Rating:

When I run simulation,it fails,and shows that the Include file (icdhspice.init) can not be opened.

And if I set the include file into icdhspice.init.ORIGINAL_BAD,it works.

So can I use icdhspice.init.ORIGINAL_BAD instead of icdhspice.init under environment options?

Tags: None

(Post is Unread)

Thread: About include file
Post: RE: About include file
Author:  Gianluca Roberts

Posted Date: October 1, 2017 9:56 PM
Status: Published
Overall Rating:

Not sure. The regular path to the Include file is working for me. Are you referring to when you specify the Include File in the Analog Design Environment -> Environment Options?

If so, make sure you are including the whole path to the Include file...
/CMC/kits/cmosp35/models/hspice/icdhspice.init

... and that you indicate "hspice" in the radio button of Include/Stimulus File Syntax.

Tags: None

(Post is Unread)

Thread: LVS: divaLVS.rul file not found
Post: LVS: divaLVS.rul file not found
Author:  James Stubbs

Posted Date: October 6, 2017 1:35 PM
Status: Published
Overall Rating:

Hello,

When I open LVS, I get a dialog that says "The selected LVS Run directory does not match the Run Form." Then, when I run LVS, an error message says divaLVS.rul does not exist, even though it says divaLVS.rul in the rules file.

Any help would be appreciated.

Tags: None

(Post is Unread)

Thread: LVS: divaLVS.rul file not found
Post: RE: LVS: divaLVS.rul file not found
Author:  Rahul Gulve

Posted Date: October 6, 2017 4:17 PM
Status: Published
Overall Rating:

Yeah I am also experiencing same problem

Tags: None

(Post is Unread)

Thread: LVS: divaLVS.rul file not found
Post: LVS: divaLVS.rul file not found
Author:  Gianluca Roberts

Posted Date: October 7, 2017 4:22 PM
Status: Published
Overall Rating:

Post: RE: LVS: divaLVS.rul file not found **Status:** Published
Author:  James Stubbs **Overall Rating:**

You solve this problem by putting "cmosp35" in the Rules Library field.

Tags: None

(Post is Unread)

Thread: LVS: divaLVS.rul file not found **Posted Date:** October 9, 2017 12:53 PM
Post: RE: LVS: divaLVS.rul file not found **Status:** Published
Author:  Rahul Gulve **Overall Rating:**

Thanks

It worked.

Tags: None

(Post is Unread)

Thread: Analog Environment Simulation Failing after working for a week **Posted Date:** October 6, 2017 4:59 PM
Status: Published
Overall Rating:

Post:
Analog Environment Simulation Failing after working for a week

Author:  James Stubbs

I have been running simulations fine in analog environment for a week with no issues. Yesterday, I tried to simulate and got the error in the attached JPG. Not sure how to fix it.

Attachment:  Capture.JPG (24.918 KB)

Tags: None

(Post is Unread)

Thread: Analog Environment Simulation Failing after working for a week **Posted Date:** October 7, 2017 4:11 PM
Status: Published
Overall Rating:

Post:
RE: Analog Environment Simulation Failing after working for a week

Author:  Richard Lin

In the ADE properties did you set the Environment to include "icdhspice.init"?

Tags: None

(Post is Unread)

Thread:

Analog Environment Simulation Failing after working
for a week

Posted Date:

October 7, 2017 4:24 PM

Status:

Published

Overall Rating:

Post:

RE: Analog Environment Simulation Failing after
working for a week

Author:



James Stubbs

It turned out that I has two sources driving the same pin. This made an error that I found in the output log.

Tags: None

(Post is Unread)

Thread:

Cadence Encounter Startup Error

Posted Date:

October 30, 2017 3:29 PM

Post:

Cadence Encounter Startup Error

Status:

Published

Author:



Ivan Radovic

Overall Rating:

Hi all,

When attempting to start up Cadence encounter to complete part 3 of Project 3, I am consistently receiving a frozen or hanged window. The terminal output seems to invoke some redirections and ends with the statement:

' [1] + Suspended (tty output) encounter'

I have attached a screenshot to show the hanged window I'm referring to. I am simply running the 'encounter' command listed in the project document (part 3 step 1).

Any help is appreciated.

Ivan

Attachment: [encounter_hang.png](#) (544.589 KB)

Tags: None

(Post is Read)

Thread: Cadence Encounter Startup Error **Posted Date:** November 1, 2017 9:09 PM
Post: RE: Cadence Encounter Startup Error **Status:** Published
Author:  **Gerard O'Leary**

Hi Ivan,

Can you try running the "fg" command to see if it reappears? If you run "jobs" what does it say?

Can you try sourcing the following and trying again?:

source /CMC/tools/CSHRCs/Cadence.EDI.14

Can you try SSHing to a different machine and tell me if the problem persists?

Thanks,

Gerard

Tags: None

(Post is Read)

Thread: Cadence Encounter Startup Error **Posted Date:** November 2, 2017 4:59 PM
Post: RE: Cadence Encounter Startup Error **Status:** Published
Author:  **Gerard O'Leary**

Also, if you are using SSH to connect to this machine from a linux machine, please be sure to use "ssh -X -Y". "-X" enables X11 forwarding, and "-Y" enables trusted X11 forwarding.

If connecting from a Windows machine, ensure that your SSH enables "trusted X11 forwarding".

Tags: None

(Post is Read)

Thread: Cadence Encounter Startup Error **Posted Date:** November 3, 2017 11:27 AM
Post: RE: Cadence Encounter Startup Error **Status:** Published
Author:  **Ivan Radovic**

Hi Gerard,

The problem seems to have resolved itself and Cadence encounter is working as intended. Guess I just had some bad luck the first time.

Thanks for your help.

Ivan

Tags: None

(Post is Unread)

Thread: cmrf8sf include file error
Post: cmrf8sf include file error
Author:  Deng Pan

Posted Date: November 12, 2017 6:38 PM
Status: Published
Overall Rating:

Hi Prof. Genov,

When I tried to simulate my schematic with cmrf8sf tech. in the analog design environment, I get the error shown in the picture attached

The include file I inserted for the HSPICE simulator is the one given on Jaro's README document:

/CMC/kits/cmrf8sf/IBM_PDK/cmrf8sf/V1.1.0.3DM/HSPICE/models/hspice_exampl

What is the working include file for cmrf8sf?

 [error_screenshot.png](#) (13.656 KB)

Tags: None

(Post is Unread)

Thread: cmrf8sf include file error
Post: RE: cmrf8sf include file error
Author:  Navid Sarhangnejad

Posted Date: November 14, 2017 8:29 AM
Status: Published
Overall Rating:

Hi Deng,

It looks like that you have an instance T4 in your design that doesn't have any of the required views. It is mentioned in the error that you posted.

Tags: None

(Post is Unread)

Thread: Error during circuit read-in found by spectre
Post: Error during circuit read-in found by spectre
Author:  Durand Jarrett-Amor

Posted Date: November 12, 2017 7:37 PM
Status: Published
Overall Rating:

Hi,

I'm using IBM 130nm technology and I'm having trouble running simulations using spectre. Specifically, I'm running into troubles including the model files for spectre and I keep getting the error "Illegal library definition." I followed the README.jaro.hints for /CMC/kits/cmrf8sf, but still cannot run the simulator using spectre. I've included screenshots of the error message I'm getting.

Some help would be greatly appreciated.

Thanks,

Durand

Attachment:  Screenshot at 2017-11-12 19-30-23.png (56.202 KB)

Tags: None

(Post is Unread)

Thread: CMRF8SF: HSPICE simulator
Post: CMRF8SF: HSPICE simulator
Author:  Gianluca Roberts

Posted Date: November 24, 2017 3:00 AM
Edited Date: November 24, 2017 3:00 AM
Status: Published
Overall Rating:

Hi everyone,

I am trying to use HSPICE to simulate my analog circuits using the CMRF8SF technology. I'm want to use HSPICE over Spectre as HSPICE can be done through command line and is much faster than using the Analog Design Environment GUI. Unfortunately, I am encountering issues that appear to be related to reading various Verilog-A modules and invoking the Verilog-A compiler, but there is no LM_LICENCE_FILE in the current environment. I have attached my input HSPICE file and the output file for reference. Which environment variable(s) should be set to enable this HSPICE execution?

Attachment:  hspice.out (5.667 KB)

Tags: None

(Post is Unread)

Thread: CMRF8SF: HSPICE simulator **Posted Date:** November 24, 2017 11:02 AM

Post: RE: CMRF8SF: HSPICE simulator **Status:** Published
Author:  Navid Sarhangnejad **Overall Rating:**

Hi Gianluca,

I am not very familiar of using hspice or spectre through command line, so I can't easily say what the problem is. What I understood is that the LM_LICENSE_FILE is not set even when you run Cadence and ADE for your simulation! One question, I assume you have used the -hdl option for your hspice command?!

If you haven't found the solution yet, please send an email to ask1388 and include the your procedure (the input/output files and the command you use).

Thanks,

Navid

Tags: None

(Post is Unread)

Thread: divaEXT.rul and divaDRC.rul not found
Post: divaEXT.rul and divaDRC.rul not found
Author:  Justin Kim

Posted Date: November 24, 2017 1:39 PM
Status: Published
Overall Rating:

Hello,

I tried to run the DRC check (and extract function) in the layout editor but it gives me the error message, "Failed to find DRC rules divaDRC.rul in library cmrf8sf."

I also could not find the files in the Cadence kits folder. Is there another way to add these files for the cmrf8sf technology?

Thank you.

Tags: None

(Post is Unread)

Thread: divaEXT.rul and divaDRC.rul not found
Post: RE: divaEXT.rul and divaDRC.rul not found
Author:  Navid Sarhangnejad

Posted Date: November 24, 2017 2:47 PM
Status: Published
Overall Rating:

Hi Justin,

Please read the /CMC/kits/cmrf8sf/==README.jaro.hints

You better use Calibre for DRC and LVS, there is no need for divaxxx.rul files.

Tags: None

(Post is Unread)

Thread:

Layer (M1, NW, PC) must be within chip edge DRC
Error

Posted Date:

November 25, 2017 9:59 AM

Status:

Published

Overall Rating:

Post:

Layer (M1, NW, PC) must be within chip edge DRC
Error

Author:



Ivan Radovic

Hi all,

While running DRC for some of my layout blocks I am getting a few errors that claim various errors are not within the chip edge. The exact wording is:
"M1 must be within CHIPEDGE >= 0.00"

Does anyone know how to resolve this? Additionally I get some other errors pertaining to E1 and LY density being below a certain threshold which I can't really figure out.

Any help is appreciated

Tags: None

(Post is Unread)

Thread:

Layer (M1, NW, PC) must be within chip edge DRC
Error

Posted Date:

November 26, 2017 10:23 PM

Status:

Published

Overall Rating:

Post:

RE: Layer (M1, NW, PC) must be within chip edge
DRC Error

Author:



Ran Duan

Hi Ivan,

Do u use the CMRF8SF technology? If yes, when u set the DRC environment, you have to change the selection "CHIP" into "CELL".

I also met the errors corresponding to E1 and LY. I deleted the click of GRE2 and GRLY6 under "DRC checking set up". It passed successfully at last. But I don't know whether this method is right or not.

Hope it could help.

Ran

Tags: None

(Post is Unread)

Thread:

Layer (M1, NW, PC) must be within chip edge DRC
Error

Posted Date:

November 27, 2017 4:03 PM

Status:

Published

Overall Rating:

Post:

RE: Layer (M1, NW, PC) must be within chip edge
DRC Error

Author:



Ivan Radovic

Hi Ran,

Thank you, this did fix the problem for me. Unless the TA's say otherwise I think it is a reasonable solution seeing as you receive these errors whenever you run the DRC on a non blank layout, hence I don't think they could be related to your design.

Regards,

Ivan

Tags: None

(Post is Unread)

Thread:

Layer (M1, NW, PC) must be within chip edge DRC
Error

Posted Date:

November 28, 2017 9:50 AM

Status:

Published

Overall Rating:

Post:

RE: Layer (M1, NW, PC) must be within chip edge
DRC Error

Author:



Ran Duan

You are welcome^ ^

Tags: None

(Post is Unread)

← OK

Collection

Users can Collect posts into a printable, sortable format. Collections are a good way to organize posts for quick reading. A Collection must be created to tag posts. [More Help](#)

Thread: ISML Project: Clock-phase generator simulation and layout
Posted Date: October 25, 2016 5:24 PM
Status: Published
Overall Rating:

Post: ISML Project: Clock-phase generator simulation and layout

Author:  Roman Genov

Clock-phase generator simulation and layout

Contact: Reza - m.reza@ece.utoronto.ca

Recommended group size: 2

Tags: None

(Post is Unread)

Thread: ISML Project: 16-bit digital filter for simulation and layout
Posted Date: October 25, 2016 5:25 PM
Edited Date: October 25, 2016 5:26 PM
Status: Published
Overall Rating:

Post: ISML Project: 16-bit digital filter for simulation and layout

Author:  Roman Genov

16-bit CIC digital filter for simulation and layout

Contact: Reza - m.reza@ece.utoronto.ca

Recommended group size: 2

Tags: None

(Post is Unread)

Thread: ISML Project: 16-bit reconfigurable accumulate and dump decimation 2nd order digital filter
Posted Date: October 25, 2016 5:26 PM
Edited Date: October 25, 2016 5:27 PM
Status: Published
Overall Rating:

Post: ISML Project: 16-bit reconfigurable accumulate and dump decimation 2nd order digital filter

Author:  Roman Genov

16-bit reconfigurable accumulate and dump decimation 2nd order digital filter
Contact: Reza - m.reza@ece.utoronto.ca
Recommended group size: 2 to 3

Tags: None

(Post is Unread)

Thread: ISML Project: VLSI Implementation of the Hyperbolic CORDIC Algorithm
Posted Date: October 25, 2016 5:28 PM
Status: Published
Overall Rating:

Post:

ISML Project: VLSI Implementation of the Hyperbolic CORDIC Algorithm

Author:



Roman Genov

VLSI Implementation of the Hyperbolic CORDIC Algorithm

Contact: Gerard - gerard.oleary@mail.utoronto.ca

Recommended group size: 2 to 4

Tags: None

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Author:

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Contact: Navid - sarhangn@ece.utoronto.ca

Tags: None

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first update on Nov 1st Tuesday

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Author:

Roman Genov

Posted Date:

October 29, 2016 2:30 PM

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Author:

Roman Genov

Posted Date:

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Tags: None

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Author:  Daniel Rozhko

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Daniel

Tags: None

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Posted Date: October 25, 2016 5:24 PM
Status: Published
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Post: ISML Project: Clock-phase generator simulation and layout

Author:  Roman Genov

Clock-phase generator simulation and layout

Contact: Reza - m.reza@ece.utoronto.ca

Recommended group size: 2

Tags: None

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Edited Date: October 25, 2016 5:26 PM
Status: Published
Overall Rating:

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Author:  Roman Genov

16-bit CIC digital filter for simulation and layout

Contact: Reza - m.reza@ece.utoronto.ca

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Author:  Roman Genov

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Recommended group size: 2 to 3

Tags: None

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Author:



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Tags: None

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Author:



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