ECE1388

Final Project Guidelines (Tentative)

1. Summary and Goal

The final project guides student teams through a simplified practical design flow of a complete integrated circuit (IC) design starting from the project definition and system outline to a complete verified IC layout including a padframe. The project aims to help students apply skills learned in this course and other courses to the design of a die-level CMOS integrated circuit (a.k.a. "chip").

The function of the chip is that of students' choice subject to limitations described below in the "Scope" section.

The goal of the project is for students to develop/polish and demonstrate a number of skills including but not limited to:

- understanding and mastery of the IC design flow as described herein
- knowledgeable utilization of all course material within the final project
- performing optimal circuit and layout design as part of an IC design flow
- demonstrated ability to work efficiently within an IC design team
- ability to communicate results effectively by way of oral presentations/ updates
- understanding all presentations and participation by asking/answering questions.

The only technology supported in the course is **TSMC 65nm technology** (with access with a signed NDA). Students cannot use other technologies in this course (except for very occasional special cases with a pre-approval from the instructor and only if the NDA is signed by the student's research supervisor, and only on the condition that no assistance is provided for this project by the teaching team).

2. Milestones

The final project runs approximately between the 7th and the 14th weeks of the course with the following *tentative* schedule (the course outline always contains the most up-to-date version of this schedule):

Week	Topic	Format
7	Team formation and project definition	*Discussion on each team's project topic*
8	System outline	*Written update (Up to 5 slides, please submit only one file per team)*
9	Circuit cells and simulations	
10	Break	
11	Complete schematic	*Initial presentation (by all teams, please submit only one file per team)*
12	Cell layout	
13	Complete layout within a pad frame	*Final presentation (covers all weeks, please submit only one file per team)*
14	LVS final check and final report	*Final report submission (2 pages of text + figures)*

3. Scope

The project focuses on the flow of the design of a complete CMOS integrated circuit chip. A default technology of choice will be announced in class. A padframe library for this technology including both cell schematics and layouts will be provided. Students should plan to utilize no more than approximately 4mm^2 area in this technology (including the padframe). Certain deviations from this area guideline are permitted with proper justification.

A degree of freedom in choosing the function(s) and specifications of the chip is allowed, subject to the instructor's approval during/before the first week of the project. If you are looking for a project idea, please choose from manuscripts from the following publications only:

IEEE Spectrum (you can choose a topic of interest when browsing it online)
IEEE International Conference on Solid-State Circuits
IEEE Journal of Solid-State Circuits
IEEE Transactions on Biomedical Circuits and Systems
Science (papers that include integrated circuits)
Nature (papers that include integrated circuits)

Please *do not read/select papers that are more than 5 years old*. Any paper that is older or is chosen from another conference/journal will need to be approved by the instructor on a case-by-case basis (and is not recommended).

Each team is highly encouraged to choose a topic that is forward-looking in terms of technological progress in the field of IC design, and that includes elements which are not only technically up-to-date and educational for the audience, but are also novel and even audience-inspiring. The project does not necessarily require innovation by students, rather novel aspects of the project can be sourced from above listed venues (with proper citations on each slide that uses a borrowed figure/idea).

4. Format of the Written Update and of the two Presentations

The written update should contain up to 5 slides, and no presentation is needed. The two oral presentations should be in the form of *high-quality well-polished* slides with key messages clearly and concisely presented. Each presentation will be short (approximately 5 to 10 minutes per team depending on the number of teams). So, it is important to make your presentation focused and only present the most important information. You may find it useful to practice your presentation before the class.

In each presentation, please order your slides to answer the following three key questions in this general order:

1. **What?**
    - E.g., what are you doing?
    - Tip: *it helps to give a brief tutorial on the subject to introduce it; please repeat this in every presentation as the audience may not know/remember this.*
2. **Why?**

- E.g., why are you doing this?
- Tip: the question "Why?" is most often overlooked.
  - 1. Explain why the topic you choose is important and where the proposed IC is used (imaging explaining this to your grandparents).
  - 2. Explain how your approach differs from a conventional one, by describing the latter first.
- Tip: *the question "Why?" is most often overlooked and is generally the most challenging for students, so please pay careful attention to it.*

3. How?

- E.g., how will you go about doing this?
- Here you can present your approach
- Tip: *please select only the most important/key points to cover and choose the points that are most innovative / inspiring / educational.*

Please see section "Group formation and project definition" for an example of such an organization.

In each presentation/written update please include *at least three* references to *specific topics* covered in the lecture notes (cite lecture topic and slide #) or the corresponding textbook (cite chapter and section/subsection name and page #s), mark it with a *big green check mark symbol* ✓. Every presentation should include at least three check marks referring to *new* (non-repeating from a previous presentation) topics. By week 12 you should have demonstrated that you have utilized at least 70% of the course lecture material topics in your design.

Additional presentation information is provided in the "Presentation Tips" section.

For each presentation, please submit a pdf hardcopy of your slides on the course website, under the corresponding submission category, at least one hour before the class starts, one file per team. Please bring your own laptop to present your slides.

5. Guidelines for Weekly Milestones

5.1. Group formation and project definition

Students should work in a team unless approved otherwise by the instructor (the team size is announced in class each year and depends on the enrollment, typically 3-4 students per team; 2 or 5 may be possible in special cases). Each team designs one chip. The project work should be divided approximately uniformly among all team members and the presentation time should also be divided approximately equally.

Each team has to come up with a project definition based on their interests and preferences. The project definition should include:

- The project title
- Team members
- Targeted function(s) performed by the chip (*what do you propose to do*?)
- A table of detailed specifications for the chip (*what specifically do you propose to achieve*?)
- Proposed applications / impact / importance / motivation / rationale (*why do you choose to do this*?)

- Rough block diagram of the chip (*how do you propose to accomplish the proposed by means of a VLSI architecture*?)
- Rough floor plan of the chip (*how do you propose to accomplish the proposed by means of a VLSI layout implementation corresponding to the VLSI architecture*?)
- References to any relevant sources of information should be made on all slides that use information from other sources (e.g., a footnote containing: authors, manuscript name, and the location of research, such as a university or a company). *No existing material can be reused without a proper reference.*

Some level of guessing in defining a rough block diagram and a floor plan is allowed at this stage in the project as long as some thought is given to them. Qualitative rather than qualitative treatment of these is sufficient at this stage. These are to be refined in the next phases of the project (and usually require some experience and iteration back from the schematic and layout design phase).

5.2. System outline

Goal (what?) and Motivation (why?): First, refine/repeat the information covered in "Group formation and project definition" section above in a succinct and concise way. *Do not forget to include motivation for your project topic choice and for any design choice you are making in each update/presentation*. Next, consider some key points regarding the system outline components as described next.

Table of Specifications: Please do not forget to include a table of *target performance specifications* for your design. These may be approximate at this point, but should be compared against *achieved performance specifications* in the final presentation (explaining reasons for any differences).

Block diagram: Define a refined block diagram of the chip you want to implement, with the functional description of the major parts (e.g.: integrator, multiplier, etc). The description should be fully quantitative with clear specification of where signals flow (What is input and output, and how components are interfaced?) and how data is handled (analog, digital, continuous-time, discrete). Find values or ranges of operational values for any parameters governing the system (e.g., coefficients of filters), and analyze the operation at the system level (What are the output waveforms and intermediate waveforms for given input waveforms?). When in doubt or certain parts are not clearly defined or optimized at the system level, do some necessary simulations (at the block-diagram level).

Floor Plan: Define the refined floor plan of the chip you want to implement. Place all major functional blocks of the system within the padframe and state their approximate dimensions. Here you can rely on your own or existing estimates of the size of layouts of your functional blocks. You will need to open the padframe library in order to obtain pad cell dimensions and to see an example of pad organization in a padframe. You should show how you propose to organize pads in your own padframe (as long as it is rectangular).

Tips: show refined system block diagram, with quantitative description of operation including I/O and interfacing waveforms (obtained from top-level simulations, if necessary); show refined floor plan. The term "refined" here refers to an improvement over the information reported at the "project definition" milestone.

5.3. Circuit cells and simulations

Come up with (elegant) circuits implementing parts of the system (e.g., amplifiers, integrators, modulators, ...). Retain the hierarchy and organizational structure of the block diagram level design. Make sure signals interface properly (in format, impedance, and in timing) between different circuit cells, according to the arrangement of the blocks. Define all bias levels (or how they are constructed from other supplied bias levels through additional bias circuitry) and voltage or current waveforms used in the timing and control of the circuits. Simulate the design.

Tips: clearly annotate the circuit diagrams and corresponding signal diagrams of all cells used to represent the functional blocks in your system, retaining the hierarchical structure. Define bias levels and signal / control waveforms, and include simulation results. Keep showing the system block diagram (or floor plan) on each presentation slide (e.g., in the upper right corner) and highlight on it the block being presented in a current slide.

5.4. Complete schematic

Arrange instances of the cells combining to construct the overall system and implement all its functions. Pay much attention to the detail of correctly interfacing the circuit blocks, and make sure the design reflects the hierarchical and modular structure of the system-level block diagram. Typically, the amount of circuitry needed to interface all blocks together should be much smaller than the actual circuitry contained within the circuit blocks themselves.

Tips: The requirements are the same as for the cell-level design above, but now at the top-level of the hierarchy. Keep showing the system block diagram (or floor plan) on each presentation slide (e.g., in a corner) and highlight on it the block being presented in a current slide. Use vectorized instances for arrays of cells and buses when appropriate (e.g., a 16x8 array of SRAM cells should be shown as one symbol with an instance label showing that it is instantiated in a 16x8 array).

5.5. Cell layout

Layout key cells in Cadence. Make sure the cells abut properly when later combined together (e.g., as instances in an array). There should be a sufficient number of Vdd and GND connections to wells and the substrate (one bulk contact per 5 or fewer transistors connecting to that bulk). Lines should be sized according to the amount of current they need to accommodate. While short lines locally connecting gates can be poly, lines that carry current or that need to respond fast to voltage changes should be metals. For large-scale signal interconnect on a 2-D grid, use odd metals horizontally and even metals vertically (or vice versa) and make sure to be consistent in order to avoid cross-over via bridges.

Tips: Label the I/O interfaces and signal/power lines of all cells with meaningful names (GND, Vdd, CARRY, Vin, Iout,...) which conform with the schematic. Run a DRC on the layout file for each cell. Then run LVS on the layout and schematics files, and correct the layout vs. the schematics until both converge. To your advantage, you should start running DRC and LVS on the cells in the earliest stages of the layout. Keep showing the system block diagram (or floor plan) on each presentation slide (e.g., in a corner) and highlight on it the block being presented in a current slide.

5.6. Complete layout within a padframe and final project presentation

Combine the cells in the layout to implement the complete schematics as previously defined, and add the interfacing circuitry at appropriate levels in the hierarchy of cells. Retain the structure of the schematics, with coinciding names for the cells in the layout and the subcircuits in the schematic. Make sure to interconnect power and signal lines correctly, with power lines (GND, Vdd, ...) having a large width. Use shielding for sensitive signals.

Include the total layout in a pad frame (provided) and route the external pin connections. Keep in mind the useful area that you can fill up with your circuits to fit within the padframe. Avoid wasting silicon area. Is your chip area core-limited or pad-limited? You are not required to complete top-level DRC or LVS at this stage but should show your chip core layout within a padframe, even if not wired up to it yet.

Every group should give a final presentation in class focusing on the final product – the complete chip and including key points from the entire project.

5.7. LVS final check and final report

Run a complete DRC on the entire chip layout file. Then run LVS on the complete layout and schematics files, and correct the layout vs. the schematics until both converge. To your advantage, you should start running LVS and DRC on the cells in the earliest stages of the layout. The final LVS check also marks the end of the project (approximately two weeks after the final project presentations). You have the chance to make changes according to discussions in class, etc.

Every project group will generate a final report (***2 pages or text, plus as many figures as you would like including schematic diagrams, layouts or key blocks and the entire chip***) in electronic format (see below), describing the chip. It should be clear from the report what the chip is supposed to do, and who did exactly what in the project. The report should be to the point, with as little general background information and as much chip specifics as possible. Please include the final DRC and LVS reports results page (only the last summary page, one for DRC and one for LVS).

Electronic format: The report needs to be submitted as a soft copy (two versions - one in pdf and the other in html format) online, and needs to include all graphics and other referenced documents. All class reports may be posted on the web, accessible from the class web page. The total size of your submission cannot exceed 10MB (save all images at a monitor resolution). Please include a path to your Cadence library in your report. Make sure to use a library name that is representative of your project.

6. Evaluation

Quality of delivery: Written update and two oral presentations	45 %
Technical content: System design, circuit schematic, layout, DRC, LVS and final report.	45 %
Engagement: presence in class (please avoid late arrivals); questions and written feedback to presenters - students are expected to actively ask questions during presentations and to provide written feedback to each	10 %

presenting team through a google form; students will also be asked to self-report the number of questions they asked each team.	

7. Presentation Tips Checklist ***(please follow closely, complete and attach as the last page for each submitted presentation's pdf file)***

✓	*Insert a check mark to the left of each item below*
☐	**1. Include names of all presenters on the first slide, and next to the name: a photo of each presenter so names are easy to remember by everyone, the program the presenter is enrolled in (e.g., MASc/MEng/PhD), their group (e.g., Electronics), and university where the previous degree was obtained.**
☐	2. Number all your slide pages.
☐	3. Do not use acronyms in the title (or slide titles) unless those are common knowledge.
☐	4. Minimum font size in all slides is 16 points for best visibility.
☐	***5. Do not make slides overly verbose and do not try to fit all unimportant details about your project into the slides.***
☐	**6. Bullets: one line of text per bullet (no text paragraphs).**
☐	7. Every borrowed figure should include a citation to the source at the bottom of the page (actual authors, paper name, journal name, university/company of the authors; do not just write [1], [2], etc, and do not list these at the end).
☐	8. Each presenter should use up the same time (e.g., 1min per person - this time will be assigned in class for each upcoming presentation).
☐	9. Do not present more than 2 (3 max) slides per minute.
☐	**10. If the presentation generates questions from audience members who got sincerely interested in the subject as a result of the presentation, this is a bonus for the presenters. Work on making your presentation being easy to follow and engaging / inspiring for your audience.**
☐	11. Please bring and use a pointer when presenting (either a **large**-size cursor or an actual pointer, like a pen or a long stick).
☐	**12. In each presentation, please remind the audience *what* you are doing (an educational intro) and *why* (a motivation*). Do not skip this.**
☐	13. When presenting cell schematics/layouts, keep showing the system block diagram on each slide (e.g., in the upper right corner) and highlight on it the block being presented in a current slide.
☐	14. When presenting schematics, consider redrawing circuits in a circuit drawing program (e.g., Visio or Xcircuit). You can try capturing Cadence schematics but make sure those are not too busy. This means use three-terminal, not four-terminal MOS symbols to avoid drawing bulk connection wires that obscure the view, turn off labels for the symbol instance number and other irrelevant labels of MOS symbols. There is also a way to invert colors when printing schematics from Cadence so that the background is white and the circuits are black (this may be the easier option).
☐	15. When presenting layouts, make sure that they can be properly seen (ideally bring it to white background when exporting from Cadence, zoom in sufficiently close to allow the audience to appreciate the density and style of layout, highlight some key most interesting layout techniques, etc).
☐	16. ***Bring a timer to time yourself. When the time is up and your timer rings, your team has to wrap up your team's presentation within 2-3 sentences (no longer than an extra minute).***

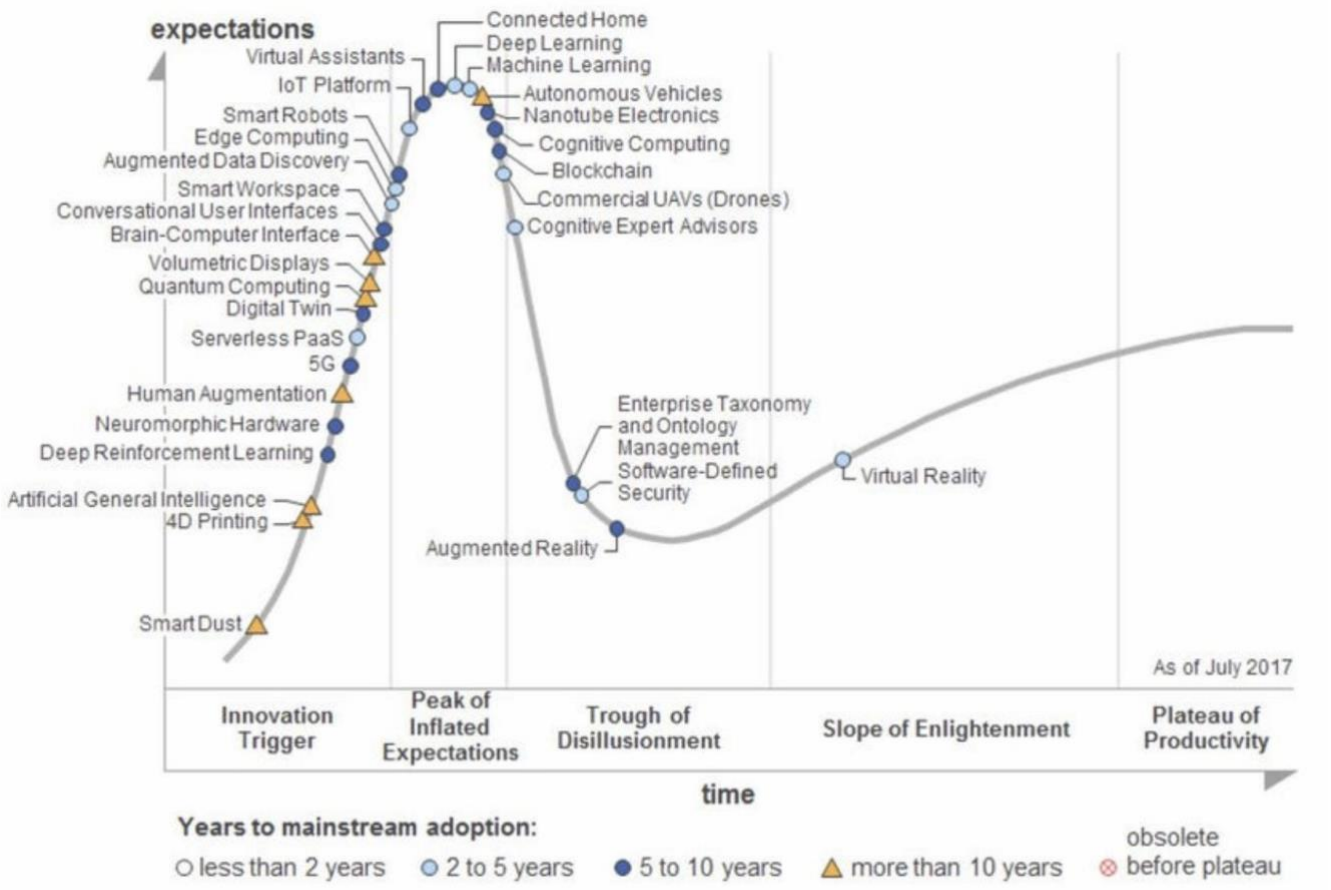
8. Q/A Section:

Q. How do I choose a topic for a project?

A. Besides the information provided in Section “Scope” above, please consider Gartner's Hype Cycle for Emerging Technologies for the past 10 years, available online as images and choose a topic that is forward-looking. A few examples are shown below:

Figure 1. Hype Cycle for Emerging Technologies, 2015
Source: Gartner (August 2015)

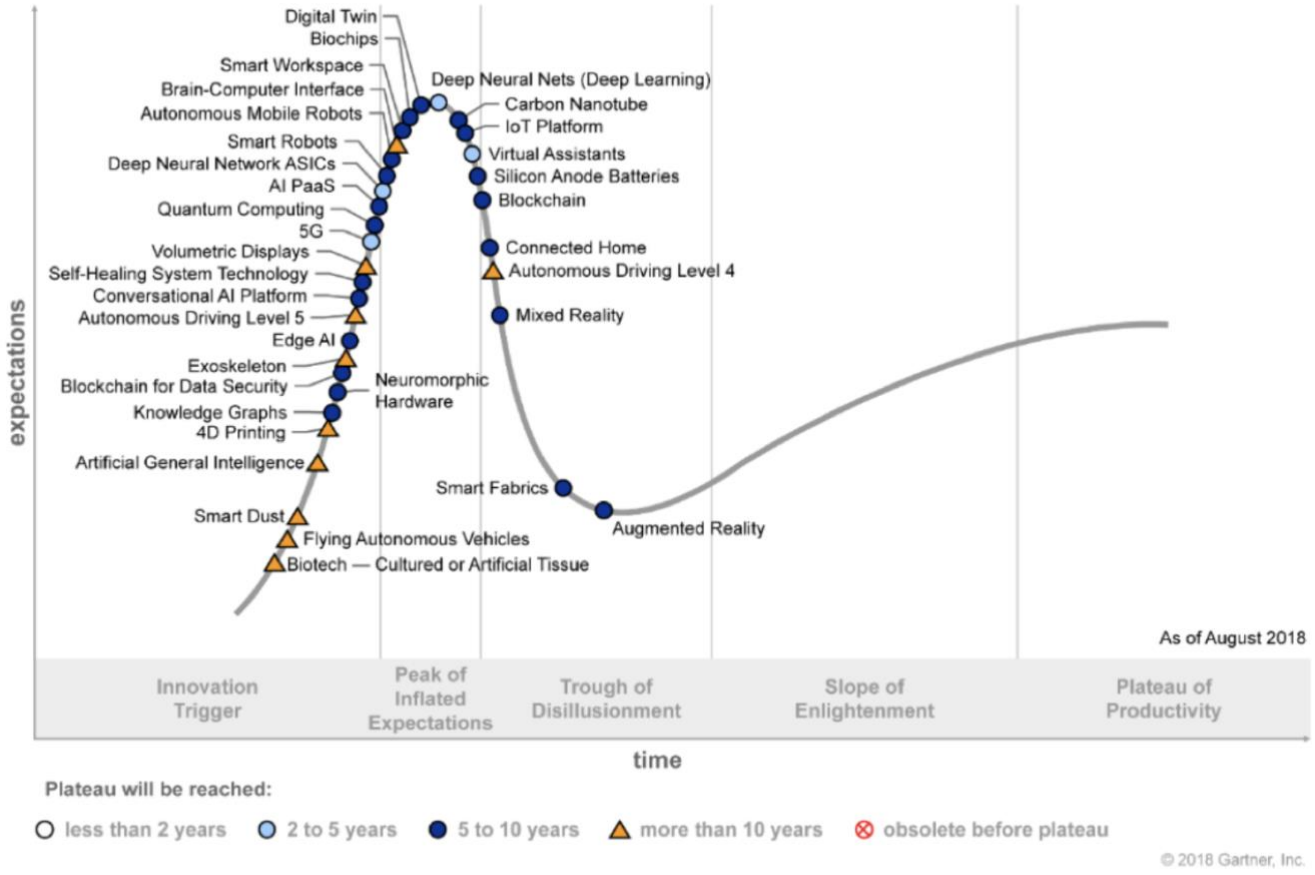
Source: Gartner (July 2016)



Note: PaaS = platform as a service; UAVs = unmanned aerial vehicles

Source: Gartner (July 2017)

Figure 1. Hype Cycle for Emerging Technologies, 2018



Source: Gartner (August 2018)

Gartner Hype Cycle for Emerging Technologies, 2019

Plateau will be reached:

○ less than 2 years ● 2 to 5 years ● 5 to 10 years ○ more than 10 years ● obsolete before plateau

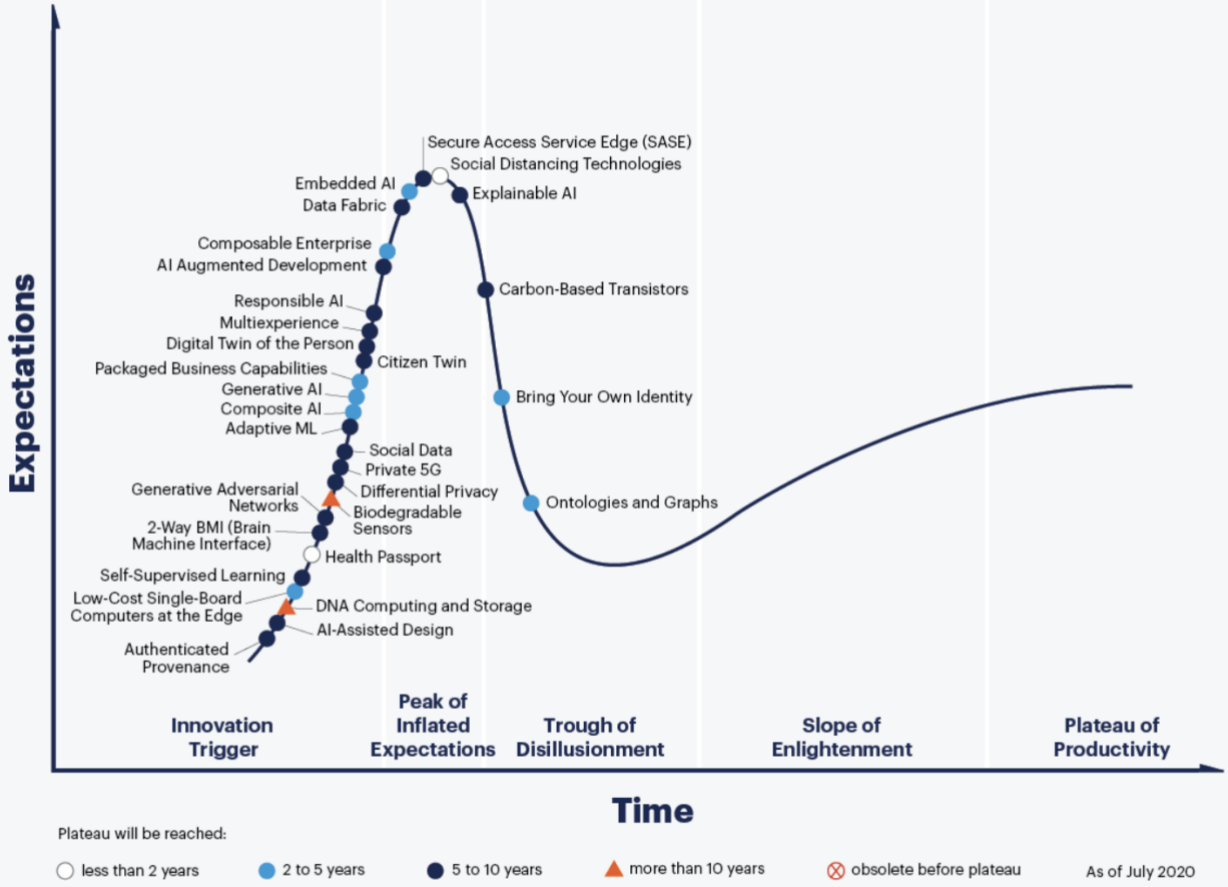
As of August 2019

gartner.com/SmarterWithGartner

Source: Gartner

Gartner

Hype Cycle for Emerging Technologies, 2020



Plateau will be reached:

○ less than 2 years ● 2 to 5 years ● 5 to 10 years ▲ more than 10 years ⊗ obsolete before plateau

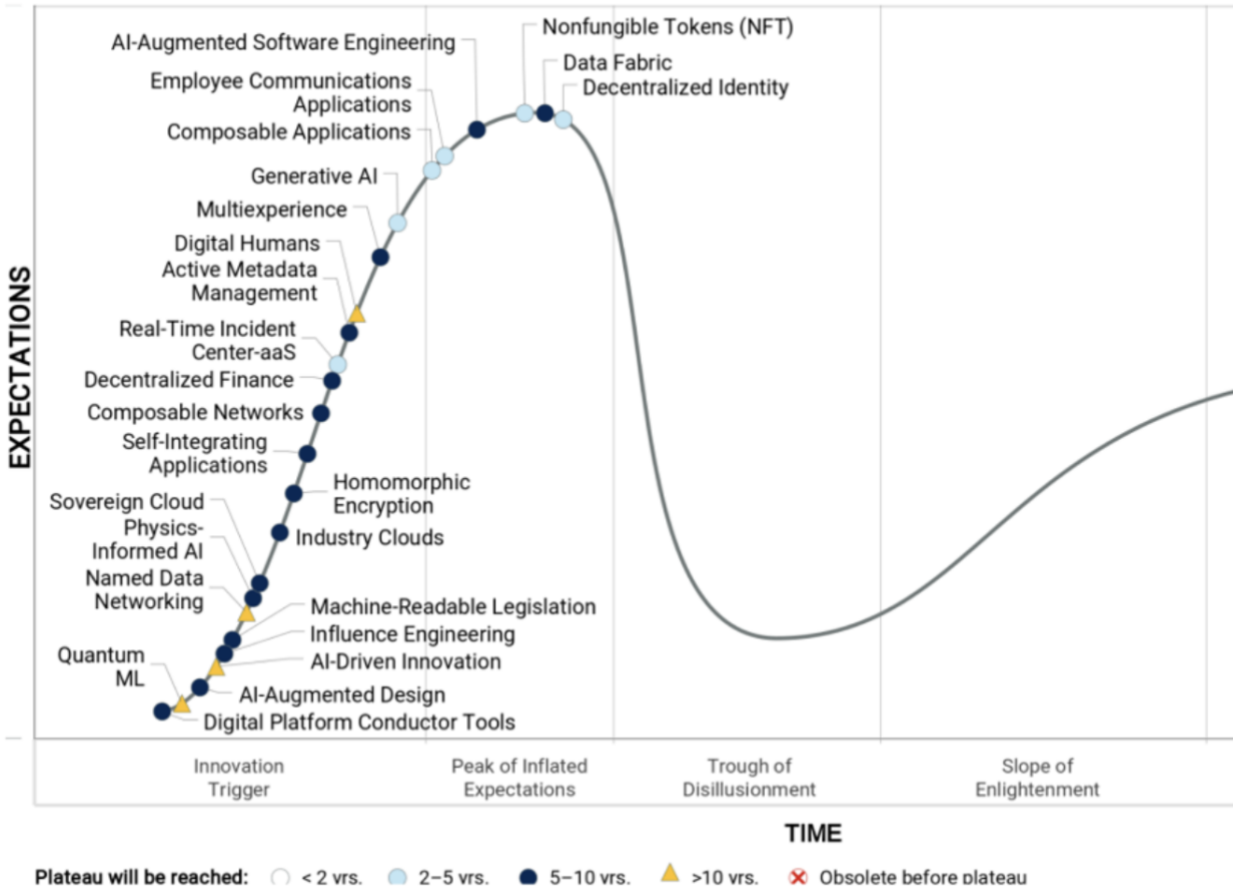
As of July 2020

gartner.com/SmarterWithGartner

Source: Gartner

Gartner

Figure 1. Hype Cycle for Emerging Technologies, 2021



Source: Gartner (August 2021)

747576

Hype Cycle for Emerging Tech, 2022

Plateau will be reached: