ECE1388 VLSI Design Methodology 2025 Outline (tentative, periodically updated)

Week		Topic	Meeting Format	Textbook, 4th Edition	Lab / Final Project	Projects Deliverables
1	Sept. 5	Introduction to the course. Students getting to know each other and starting to form their final project teams.	Review of Course Syllabus and Outline	Sec. 1.3, 1.4	Lab 1: Lab Manual Ch. 1-3	-
2	Sept. 12	Introduction to the field. Introduction to MOS Transistors and to Digital Circuits. Layout and Fabrication.	Lectures 0, 1, 2	Sec. 1.5, 2.1-2.3.1, 2.5.4, 4.3.1-4.3.3	Lab 2: Lab Manual Ch. 4-5 (skip 5.6)	Project 1 out
3	Sept. 19	Cadence Virtuoso Schematic Editor and Layout Editor. Layout of Parameterized Cells (P-cells)	Tutorials 1, 2	Sec. 2.4, 7.1-7.2, 2.5.1-2.5.3, 4.1-4.3	Lab 3: Lab Manual Ch. 6	-
4	Sept. 26	CMOS Transistor Theory. Non-Ideal Transistors. DC & Transient Response.	Lectures 3, 4, 5	-	-	**Project 1 due** (Fri) Project 2 out
5	Oct. 3	CMOS Processing Technology. Design for Optimum Speed: Logical Effort. Design for Low Power. Interconnect and Wire Engineering.	Silicon Run I Video (watch at home), Lectures 6, 7, 8	Sec. 3.1-3.3, 4.4-4.5, 5.1-5.3	Lab 4: Lab Manual Ch. 7-8	-
6	Oct. 10	Engineering. Packaging, Power, Clock and I/O.	Lectures 9, Discussion on teams' topics	Sec. 6.1-6.4, 13.1-13.4, 13.6	*Final Project Introduction*	Project 3 out
7	Oct. 17	Combinational Circuit Design. Circuit Families. Sequential Circuit Design	Lectures 10, 11, 12	Sec. 9.1-9.2, 10.1-10.3	*Team formation and project definition*	**Project 2 due** (Fri)
8	Oct. 24	Digital Design Flow, from Synthesis to Place-and-route.	Tutorials 3, 4	-	*System outline*	**Final project written update due**: System outline (5-slide)
9	Oct. 31	Fall study break	-	-	-	-
10	Nov. 7	Verilog-A Language. Mixed-signal Simulations within Cadence Virtuoso AMS Environment.	Tutorials 5, 6	-	*Circuit cells and simulations*	**Project 3 due** (Fri)
11	Nov. 14	**Workshop #1 on the Latest Trends In Integrated Systems** (teams receive initial feedback from audience)	Student Team Presentations	-	*Complete schematic*	**Final project first presentation:** Complete schematics
12	Nov. 21	Memories: SRAM, DRAM, EEPROM/Flash. Design for Testability	Lectures 13, 14, 15	Sec. 12.1-12.6, 15.1-15.7	*Cell layout*	-
13	~Nov. 28 (TBD)	**Workshop #2 on the Latest Trends In Integrated Systems** (teams receive comprehensive feedback from audience)	Student Team Presentations	-	*Complete layout within a pad frame*	**Final project second presentation** (full-chip LVS is optional)
14	~Dec. 22 (TBD)	-	-	-	*Full-chip LVS & DRC checks*	**Final report due** (2-page text + figures)