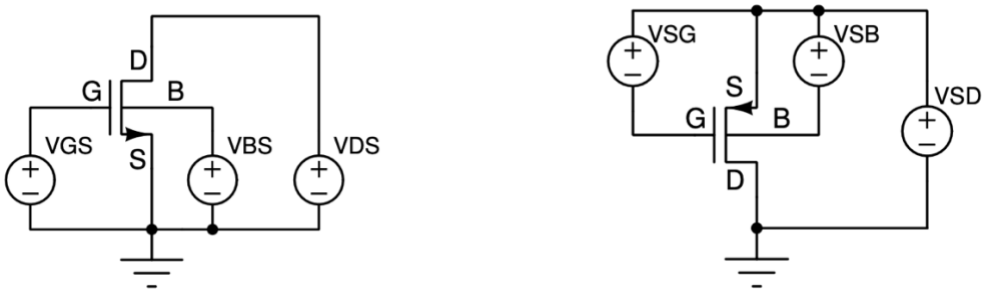
ECE1388 Project 1

Device and Circuit Characterization

- Bonus questions are worth an extra 10% of this assignment grade.
- Assume: *Vdd* = 1*V.*
- Assume minimum gate length. For this technology λ = 30nm.
- Consult sections 2.4 and 8.4 of the textbook.

1 Device characterization

1. Use Cadence Composer to generate I-V curves for nMOS and pMOS transistors in the 65nmCMOS process (similar to those in Figures 8.16 and 8.17 in the textbook). Plot the eight curves on a single page for Wp = 64 units, and Wn = 32 units (for subfigure (b) in both figures, use twice the minimum gate length). Note that the term 'units' refers to the number of multiples of a unit-sized transistor, i.e., first instantiate a transistor with unit-sized parameters of gate width = 4 and gate length = 2 (minimum gate length), and then set the multiplier field to be the desired value of Wn or Wp.
   Hint*: Read* ***Sec. 5.6*** *of the* ***VLSI User Manual*** *on how to generate tabular textual results data to be imported into MATLAB for plotting.*



(a) NMOS test setup. (b) PMOS test setup.

Figure 1: Setup for device characterization.

2. **BONUS** Determine empirical velocity saturation models for the transistors in question 1 above for Wn,p = 32 units (Read Sec. 2.4.1 of the textbook). Do not neglect channel length modulation. Use MATLAB for curve fitting. Plot transistor I-V characteristics (Ids vs. Vds) based on the fitted models on the respective plots obtained using Cadence simulations (two plots with five curves each, one simulated, one fitted, on the same scale, all on one page). Extract and describe quantitatively transistor parameters for the following effects: channel length modulation (lambda), threshold voltage (constant-current, or maximum-g_m extraction method), subthreshold leakage, DIBL.

2 Circuit design and characterization (Inverter)

1. Read section 8.4.3 and consider Figure 8.22 (note that in this figure, X refers to an inverter instance name, not a multiplication factor). Following a similar procedure, determine the effective gate capacitance of a 64/32 inverter (i.e., Wp=64 units, Wn=32 units, both transistors are of minimum length). To do so, place an additional load-on-load inverter of size 1024/512 units after the X5 inverter (the load) in the chain.
   ***Hint**: For faster operation, it is a good practice to use fingered or parallel transistors for wide transistors.*
   ***Hint**: For better accuracy, use the pulse source with period ≤ 1ns and rise/fall time ≤ 1ps.*

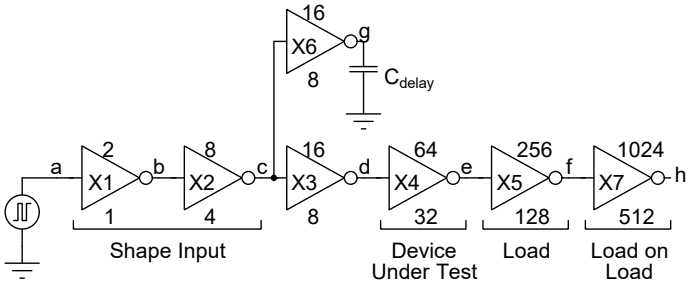
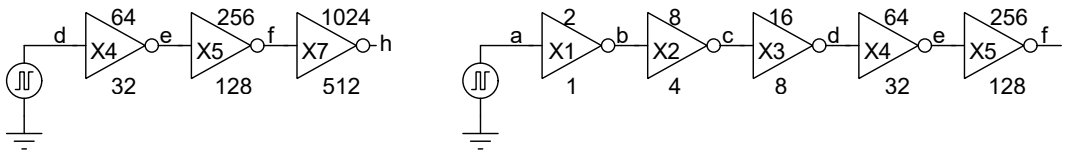


Figure 2: Inverter chain.

2. Calculate the effective resistance of single nMOS (Wn = 32 units) and pMOS (Wp = 64 units) transistors without calculating parasitic capacitances following the discussion in section 8.4.5 (hint: calculate the difference between delays at different fanouts). Omit the delay-estimation inverter (X6 in Figure 8.22) in the test bench schematic. Since you have already obtained the total gate capacitance in question 2.1, do not include the multiple of 3 in your propagation delay expressions. Observe that the diffusion capacitance terms cancel out.

3. By what percentage does the delay of the 64/32 inverter from question 2.1 change if the input is driven by a voltage step rather than a pair of shaping inverters X1 and X2? Assume an ideal input voltage step (e.g., by setting rise/fall time to 1 ps). In the test bench schematic, do not include the delay estimation inverter (X6 in Figure 8.22), but keep the X5 (the load) and the previously added load-on-load (1024/512) inverters. Refer to Figure 3a below for the circuit diagram.

4. Using the test bench from question 2.1 (with the X6 delay estimation inverter omitted), by what percentage does the delay of the 64/32 inverter change if the load-on-load inverter is omitted? Refer to Figure 3b for the circuit diagram.



(a) Input without the shaping inverters. (b) Output without the load-on-load inverter.

Figure 3: Inverter chain under different characterization conditions.

5. **BONUS:** Use the values for the extracted gate capacitance and effective resistance of single nMOS and pMOS transistors obtained in questions 2.1 and 2.2 to hand-calculate propagation delays of a fanout-of-5 inverter sized 64/32 (hint: do not forget that the parasitic capacitances are different for nMOS and pMOS devices). Obtain the propagation delays using Cadence Composer simulation and compare the percentage change in the results.

3 Layout design and post-layout simulation (Inverter)

1. Find the input and output logic levels and the high and low noise margins for the 64/32 inverter.
2. What Wp/Wn ratio yields equal (and thus maximum) noise margins for an inverter with Wn=32 units (assuming the minimum gate length for both transistors).
3. Implement layout, and perform DRC and LVS for an inverter with the Wp/Wn ratio found in question 3.2. Follow standard-cell layout style and use proper transistor fingering techniques. Label all I/O and global nodes. Include a layout image and an LVS results file printout in your report. Simulate the extracted view to obtain the voltage transfer characteristic and compare the noise margin values with those obtained in question 3.1.