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Thread:
Project 2 - 1.1 - Delay in units of what?
Post:
Project 2 - 1.1 - Delay in units of what?
Author: Minghua Zhao

Posted Date: October 9, 2016 7:34 PM
Status: Published
Overall Rating:

Just wanted some clarification on the requested delay estimation on question 1.1

Are the estimations required in units of seconds? Or units of 'tau' τ

If it is seconds, could someone please point me to the right chapter in the book? Specifically on the definition of 'tau'. I'm not sure if 'tau' = RC is just the delay for a unit sized transistor, in which case I don't know how to quite calculate it.... yet....

Thanks,

Minghua

Tags: None Add

Reply Quote Mark as Unread

Thread:
Project 2 - 1.1 - Delay in units of what?
Post:
RE: Project 2 - 1.1 - Delay in units of what?

Posted Date: October 10, 2016 10:50 AM
Status: Published
Overall Rating:

Author: Xunjun Mo

I think you can take a look at chapter 4, especially section 4.3 RC Delay model and 4.4 Linear Delay model. And I think equation (4.15) in page 151 can exactly answer your question.

Hope it helps.

XunJun

Tags: None Add

Reply Quote Mark as Unread

Thread: Project 2 - 1.1 - Delay in units of what?
Post: RE: Project 2 - 1.1 - Delay in units of what?
Author: Minghua Zhao

Posted Date: October 12, 2016 7:22 PM
Status: Published
Overall Rating:

Ah hah. Got it. Thanks!

Tags: None Add

Reply Quote Mark as Unread

Thread: Project 1.2 estimating the area
Post: Project 1.2 estimating the area
Author: Tianxiang Chen

Posted Date: October 12, 2016 3:00 PM
Status: Published
Overall Rating:

Hi,

For this question, how should we estimate the area based on the gate size found in Q1.1?

I mean, sometimes the Cin we found in Q1.1 is even way smaller than a unit size one. (For example, Cin<1 for a NAND5, whose Cin is 7 for a unit size one). Should in this case I just use the minimum possible size?

Tags: None Add

Reply Quote Mark as Read

Thread: Project 1.2 estimating the area
Post: RE: Project 1.2 estimating the area
Author: Xunjun Mo
Posted Date: October 12, 2016 7:25 PM
Status: Published
Overall Rating:

I have the same question here.

Tags: None Add

Reply Quote Mark as Read

Thread: Project 1.2 estimating the area
Post: RE: Project 1.2 estimating the area
Author: Minghua Zhao
Posted Date: October 12, 2016 8:03 PM
Status: Published
Overall Rating:

Same question

Tags: None Add

Reply Quote Mark as Read

Thread: Project 1.2 estimating the area
Post: RE: Project 1.2 estimating the area
Author: Shu Wang
Posted Date: October 13, 2016 4:53 PM
Status: Published
Overall Rating:

bump

Tags: None Add

Reply Quote Mark as Read

Thread: Project 1.2 estimating the area
Post: RE: Project 1.2 estimating the area
Author: Ziming Li
Posted Date: October 14, 2016 11:29 PM
Status: Published
Overall Rating:

I have same question here too

Tags: None Add

Reply Quote Mark as Read

Thread: Project 1.2 estimating the area
Post: RE: Project 1.2 estimating the area
Author: Navid Sarhangnejad
Posted Date: October 17, 2016 10:56 AM
Status: Published
Overall Rating:

Hi,

Yes, you have to obey the minimum size rule. Do not use smaller than one unit size.

Tags: None Add

Reply Quote Mark as Read

Thread: Problem in transistor sizing
Post: Problem in transistor sizing
Author: Xunjun Mo
Posted Date: October 12, 2016 7:00 PM
Status: Published
Overall Rating:

Hi everyone,

I have a problem regarding the sizing of transistor. In the assumption of example 4.5.3 in the textbook, it gives a measure of capacitance (for both Cin and Cout of the path) in terms of the load of unit size transistor. However, when I try to size all transistors in my fastest decoder, I calculated some transistor sizes like 0.92 and 1.38. And specifically, my questions are the following:

1. Is there a constraint that we need to use transistors having width being integer multiple of unit size transistor? For example, can we use transistor with width equals to 1.5 times of the unit width?

2. Is it correct to define a unit size transistor (with width = w, for example), then use a transistor that has its width smaller than w? Or I should just round it to unit width?

Thanks.

Xunjun

Tags: None Add

Reply Quote Mark as Read

Thread: Problem in transistor sizing
Post: RE: Problem in transistor sizing
Author: Genwen Zhao
Posted Date: October 12, 2016 10:43 PM
Status: Published
Overall Rating:

Hi,

my understanding is that 1 unit width is 4 λ . and based on 0.35 technode, λ = 0.2 micron . If 1 unit width is smaller than that, we will be in trouble doing layout.. especially when you have size 0.92/1.38..

so really, when you say gate size 0.92 /1.38, your actual gate width for pmos is 0.92 * 4 λ , and nmost as 1.38 * 4 λ . So you don't really need to size your gate into integer. you can specify gate width to whatever you want(>0.35micron), and use multiplier. but make sure they result the same gate width.

I could be wrong on this :)

Thanks

Genwen

Tags: None Add

Reply Quote Mark as Read

Thread: Problem in transistor sizing
Post: RE: Problem in transistor sizing
Author: Navid Sarhangnejad
Posted Date: October 17, 2016 11:05 AM
Status: Published
Overall Rating:

You have to make sure you don't use smaller than minimum size.

For widths larger than 1 unit width, you can use non-integer values. For simplicity let's say that you can round it to one decimal value (1.38 --> 1.4), but when you want to implement it in Cadence, you might need to round it again to the nearest multiple of 0.025um.

Tags: None Add

Reply Quote Mark as Read

Thread: Problem in transistor sizing
Post: RE: Problem in transistor sizing
Author: Minghua Zhao
Posted Date: October 17, 2016 8:44 PM
Status: Published
Overall Rating:

Just wanted a clarification on why we can use non-integer values for widths larger than 1 unit width.

For 350nm technology, lambda = 0.2um

The way I understand it, if fabrications sizes are smaller than 0.2um, the technology has troubles in fabrication accuracy.

(i.e. imagine working at Intel with 10nm devices)

So 1.4 * 0.2 = 0.28um

That 0.08um when fabricated would be a very iffy measure no? Assuming we are back in time and 350nm was state-of-the-art, or we don't have high-tech fab.

Tags: None Add

Reply Quote Mark as Read

Thread: Problem in transistor sizing
Post: RE: Problem in transistor sizing
Author: Genwen Zhao
Posted Date: October 17, 2016 10:28 PM
Status: Published
Overall Rating:

if the tech node is 350nm, that means the minimal size you can fabricate is 350nm. that is why in lab 1, 1 unit gate length is 2 lambda, and 1 unit gate width is 4 lambda. You can NOT fabricate any size lower than that, like 0.28um.... this will require smaller tech node.

say you have width 1.4x, it doesn't mean it is 1.4 x lambda. i think in this lab2, 1 unit size should be 4 x lambda instead(same as lab1). so the actual total gate width = 1.4 * 4 * 0.2 = 1.12 um. Now you can define W as 0.56 um, and make multiplier to 2, because 0.56*2 = 1.12 um. However, i don't believe you can set your W to 0.28 um and multiplier to 4. it has to be at least > 0.35 um.

Tags: None Add

Reply Quote Mark as Read

Thread: Problem in transistor sizing
Post: RE: Problem in transistor sizing
Author: Xingyu Wan
Posted Date: October 24, 2016 1:48 PM
Status: Published
Overall Rating:

Hi, I have a question about the size. When I create the layout, I round the size to the nearest multiple of 0.025um. So the size in layout is a little different with the size in schematic. Do I need to change the size in schematic to be the same size in layout?

Thank you very much!

Tags: None Add

Reply Quote Mark as Read

Thread: Problem in transistor sizing
Post: RE: Problem in transistor sizing
Author: Yifeng Zhang
Posted Date: October 24, 2016 2:39 PM
Status: Published
Overall Rating:

Hi Xingyu,

yes, you need to change the size in schematic to match the size in your layout in order to get LVS clean. You just need to make sure your size is multiple of 0.025um otherwise you will get DRC error in your layout.

Thanks

Tags: None Add

Reply Quote Mark as Read

Thread: Problem in transistor sizing
Post: RE: Problem in transistor sizing
Author: Xunjun Mo
Posted Date: October 24, 2016 11:52 PM
Status: Published
Overall Rating:

Hi,

My experience is that when I round the width in layout, I can still pass the LVS even if I don't do the same to the width in schematic. I think such small difference (rounding error) won't trigger error in LVS test.

XunJun

Tags: None Add

Reply Quote Mark as Read

Thread: NAND5 Switching Prob
Posted Date: October 13, 2016 5:18 PM

Post: NAND5 Switching Prob
Author: Shu Wang
Status: Published
Overall Rating:

To calculate for dynamic power consumption, we need to calculate for activity factor. In the textbook only the switching prob of 2-input gates are listed, how do we calculate it for 5-input? (i.e. NAND5) Or do we assume alpha=1/2?

Tags: None Add

Reply Quote Mark as Read

Thread: NAND5 Switching Prob
Post: RE: NAND5 Switching Prob
Author: Minghua Zhao
Posted Date: October 13, 2016 10:29 PM
Status: Published
Overall Rating:

Since from AND2 and AND3 is just adding the third input probability to the multipliers, I think NAND5 would be extending the same logic from NAND2.

i.e. 1-PaPbPcPdPe

Tags: None Add

Reply Quote Mark as Read

Thread: standard cell height
Post: standard cell height
Author: Yifeng Zhang
Posted Date: October 14, 2016 12:47 PM
Status: Published
Overall Rating:

Hi all,

what is the height of a standard cell? Can we define our own height for the inv and nand gate in project2 ? or we need to follow the height of nand/nor gate in the wcells library?

Thanks

Yifeng

Tags: None Add

Reply Quote Mark as Unread

Thread: standard cell height
Posted Date: October 15, 2016 10:20 AM

Post: RE: standard cell height
Author: Genwen Zhao
Status: Published
Overall Rating:

same question !

Tags: None Add

Reply Quote Mark as Unread

Thread: standard cell height
Post: RE: standard cell height
Author: Navid Sarhangnejad
Posted Date: October 17, 2016 11:10 AM
Status: Published
Overall Rating:

You can choose whatever value you want for your cell's height. You can also use the same as in wcell library, but that might not be the optimum for your layout in the sense of total area.

Tags: None Add

Reply Quote Mark as Unread

Thread: Input switching speed and simulation
Post: Input switching speed and simulation
Author: Minghua Zhao
Posted Date: October 19, 2016 11:39 PM
Status: Published
Overall Rating:

How do we get around to simulating our decoder?

i.e. I want to run through all address possibilities to generate all active word lines, and see if my decoder works.

Are we expected to do that with the Analog Simulator? Make a pulse for each input to the decoder? It just seems a bit clunky because the switching frequency of each input is different. I was wondering if there was an easier way around it.

Looked briefly into Verilog / VHDL from Chapter 6, but it doesn't look very relevant to Project 2 problem. I could be wrong, so anyone with clues, please share ;)

Ah yes, one more thing is the pulse speed of the input. I heard 100ps mentioned last tutorial, but just wanted to confirm.

Tags: None Add

Reply Quote Mark as Unread

Thread: Input switching speed and simulation
Post: RE: Input switching speed and simulation
Author: Genwen Zhao
Posted Date: October 20, 2016 12:08 PM
Status: Published
Overall Rating:

you could go for Verilog approach, but this could be fair amount of work :) which is kinda like what we will be doing for project3, where you may need to develop verilog code, synthesize it and extract a symbol to use in your test bench.

I think Navid mentioned in class that you can set up individual supply to each Addr bit, and set them to different switching frequencies(refer to Q1.3 where the Address combinations are "rolling" over once in 32 us, based on this you can calculate MSB - LSB switching frequencies)

I personally think this is a pretty easy approach.

Tags: None Add

Reply Quote Mark as Unread

Thread: Input switching speed and simulation
Post: RE: Input switching speed and simulation
Author: Minghua Zhao
Posted Date: October 20, 2016 9:01 PM
Status: Published
Overall Rating:

I thought we could do digital simulation similarly for how there is an "Analog Simulation" feature.

Like export the schematic (or symbol) as Verilog, write the inputs in Verilog, and check the output.

Anyways, thanks.

Tags: None Add

Reply Quote Mark as Unread

Thread: Input switching speed and simulation
Post: RE: Input switching speed and simulation
Author: Navid Sarhangnejad
Posted Date: October 21, 2016 10:30 AM
Status: Published
Overall Rating:

Genwen is right, it's probably easier if you do an analog simulation.

You can write a Verilog/VHDL model and then generate both schematic and layout from it. But I don't know any way of generating a Verilog code based on your schematic!

In your analog simulations, you can use 5 vpulse sources to generate pulses at the 5 frequencies you need. In case you don't want to use shaping inverters at the input, I suggested to use rise/fall times of [at least] 100ps (up to 400ps).

Tags: None Add

Reply Quote Mark as Unread

Thread: running power simulation
Post: running power simulation
Author: Genwen Zhao
Posted Date: October 22, 2016 6:37 PM
Status: Published
Overall Rating:

Hi,

I am trying to obtain simulated total/static power dissipation. I am using what Navid suggested, setting up 5 different power supplies for 5 input address bits.

To estimate the power, I am logging the current going into the decoder from vdd.

However, looking at the waveform, I realized some resonant activities on current after the address switching.. and current can go negative !

My understanding is after the switching, the current should be stable.. which is static power dissipation. the spike during the switching will be the dynamic power.

But then why is the current negative ???? When we calculate the power, do we integrate the abs(current) ?

Attachment: current.png (48.192 KB)

Tags: None Add

Reply Quote Mark as Read

Thread: running power simulation
Post: RE: running power simulation
Author: Xunjun Mo
Posted Date: October 23, 2016 3:19 PM
Status: Published
Overall Rating:

Hi,

Initially, I got the same plot as yours. After discussion with Terry, I changed the setting of transient analysis to step=10ps, range from 0 to 3us. And I got a plot with much less (almost no) "oscillation" in current. I think the current isn't really oscillating (i.e., there is not really large signal current flowing from ground to vdd at any instant). And there is no single discrete current measurement to be in opposite direction. The reason for the "oscillatory behavior" in the plot is the following: The switching current is like a delta function, which is very steep. When plotted, the CAD tool tries to use some kind of polynomial fitting algorithm to connect discrete measured current values into smooth curve. And it results in the "oscillatory behavior" observed in your plot.

I try to use the calculator to compute both the integral of the current and the integral of the magnitude of the current. And I got exactly the same result. If the integral function in calculator just sums all discrete measured values, then I think the fact that having the same integral supports the reasoning above.

XunJun

Attachment: zoomin.png (16.809 KB)

Tags: None Add

Reply Quote Mark as Read

Thread: running power simulation
Post: RE: running power simulation
Author: **Xunjun Mo**
Posted Date: October 23, 2016 3:50 PM
Status: Published
Overall Rating:

I also try to simply increase the resolution (i.e., by changing the step size to be 10ps). It works too. The oscillatory behavior is suppressed.

Attachment: Screenshot.png (31.238 KB)

Tags: None Add

Reply Quote Mark as Read

Thread: running power simulation
Post: RE: running power simulation
Author: **Dhruv Patel**
Posted Date: October 23, 2016 7:03 PM
Status: Published
Overall Rating:

Hi, Genwen:

For power calculation, just for the safe calculations, you shouldn't integrate the absolute value of the current, as it may falsify the net current supplied by the source. You should integrate the current over the period of the time to get the average current supplied by the source. Effects like clock feed through may produce voltages slightly higher than VDD producing current going in reverse direction. Therefore, for more accurate calculation you should just integrated the actual value of the current. Then you can multiply that average current value by the VDD to get the total average power.

Tags: None Add

Reply Quote Mark as Read

Thread: running power simulation
Post: RE: running power simulation
Author: Qijun Wen
Posted Date: October 23, 2016 11:34 PM
Status: Published
Overall Rating:

Hi

First, I also get the same plot as yours.

I think, for the total power dissipation, we can just integrated the actual value of current(not the abs value of current) over a period of time, for example 0 to 32u for all the combination of the address. And then use the equation 5.3 in the textbook to calculate the total power.

But for the static power, I have the same question about the "negative" current.

After switching, the current will first "oscillated", and then become stable. I think we could use the stable value of the current to calculate the static power. In this way, we will take the "oscillated" as part of the dynamic power. Some of this stable value could be negative. I think we can minimize the effect of the negative value by calculating the average value across all combinations of the address.

Qijun Wen

Tags: None Add

Reply Quote Mark as Read

Thread: running power simulation
Post: RE: running power simulation
Author:
Posted Date: October 24, 2016 9:38 AM
Status: Published
Overall Rating:

Genwen Zhao

Hi Qijun,

I totally agree with you. For static power, we should be looking for a stable current after the oscillation before the next address switching comes. However, one problem for me is that, seems like the oscillation goes on forever !! I have tried to extend the settling time between each address switching, but doesn't help much..

I am using 200ps raise/fall time for power supply. running the tran analysis from 0 - 32u with step of 10p .

Thanks

Tags: None Add

Reply Quote Mark as Read

Thread: running power simulation
Post: RE: running power simulation
Author: **Xunjun Mo**
Posted Date: October 25, 2016 12:16 AM
Status: Published
Overall Rating:

Hi,

Regarding the oscillatory behavior in transient current, I asked Navid this question in today's office hour. And my previous understanding is wrong. Here is my understanding of his answer: The simulator does get some oscillatory behavior in numerical simulation result. However, such result, i.e., current may flow from ground to vdd at some moment in time, is due to the inaccuracy of the numerical methods for transient analysis when dealing with "delta shape" transient current. In reality, there is no such oscillatory behavior. And one of the direct ways to improve the accuracy is through decreasing the time step in transient simulation.

XunJun

Tags: None Add

Reply Quote Mark as Read

Thread: need final proj members
Post: need final proj members
Author: **Shu Wang**
Posted Date: October 23, 2016 4:29 PM
Status: Published
Overall Rating:

Brett (masc) and I (meng) are looking for two more fellas for the final project.

PM me if interested, thanks.

Tags: None Add

Reply Quote Mark as Unread

Thread: need final proj members
Post: RE: need final proj members
Author: Srinidhi Balasubrahmanya
Posted Date: October 31, 2016 12:59 PM
Status: Published
Overall Rating:

I'm Sri, and my friend Jai are looking for teammates. We would like to talk to you guys

Sri

Tags: None Add

Reply Quote Mark as Unread

Thread: Attenuation of each stage during extracted layout simulation
Post: Attenuation of each stage during extracted layout simulation
Author: Christos Konstantopoulos
Posted Date: October 23, 2016 10:55 PM
Edited Date: October 23, 2016 11:37 PM
Status: Published
Overall Rating:

Good evening to everybody,

I have a problem . Each of my sized stages attenuate the input signal during the extracted layout simulation

while the schematic simulation is fine. Could you please send me any ideas what goes wrong ?

With regsrds,

Christos

Tags: None Add

Reply Quote Mark as Read

Thread: Attenuation of each stage during extracted layout simulation
Post: RE: Attenuation of each stage during extracted layout simulation
Author: Minghua Zhao

Posted Date: October 27, 2016 8:15 PM
Status: Published
Overall Rating:

Maybe not the same problem as yours, but my extracted simulation is also behaving strangely - my word_line outputs are growing exponentially

LVS passes...

Tags: None Add

Reply Quote Mark as Read

Thread: Simulation Error
Post: Simulation Error
Author: Srinidhi Balasubrahmanya

Posted Date: October 25, 2016 6:32 PM
Status: Published
Overall Rating:

I got my LVS pass, but when I try to simulate the Symbol from the extracted view with the same connections as had been done for Question 2, I get the error saying "*Error* Trying to plot expression <VT("/net46" "/nfs/ug/homes-1/b/balasu98/CMOSP35/simulation/Q2_Proj2_LaySymbol/hspiceS/schematic")>, which does not evaluate to an object that can be plotted, like waveform or parametric wave. Please refer to the Wavescan User Guide to see what all types of objects can be plotted in Wavescan. Expression which evaluates to only those type(s) of objects can be plotted." I believe I have selected voltages to be plotted,which makes this error no sense.

Any help?

Thanks

Sri

Tags: None Add

Reply Quote Mark as Read

Thread: Simulation Error
Post: RE: Simulation Error
Author: Ziming Li

Posted Date: October 26, 2016 6:21 PM
Status: Published
Overall Rating:

Hi Srinidhi,

If you select the node of a generated symbol, it might give you this error. What I found out can work is by connecting a Vdc with 0 V on top and select the node or wire from Vdc source to plot. See the attached figure for example.

I hope it helps.

Best,

Ziming

Attachment: Screenshot.png (5.251 KB)

Tags: None Add

Reply Quote Mark as Read

Thread: Simulation Error
Post: RE: Simulation Error
Author: **Srinidhi Balasubrahmanya**
Posted Date: October 30, 2016 11:38 PM
Status: Published
Overall Rating:

I did that, it helped. Thanks

Tags: None Add

Reply Quote Mark as Read

Thread: Simulation Error
Post: RE: Simulation Error
Author: **Jianxiong Xu**
Posted Date: October 30, 2016 5:50 PM
Status: Published
Overall Rating:

You need to add "extracted" before the "schematic" in your simulation environment.

Tags: None Add

Reply Quote Mark as Read

Thread: Looking for teammates
Post: Looking for teammates
Author: **Srinidhi Balasubrahmanya**
Posted Date: October 30, 2016 11:36 PM
Status: Published
Overall Rating:

Hello,

Me and Jaimin are looking for teammates for the final project. We are interested in a preferably learning oriented kind of the project, not the research oriented. If anyone is interested to tam up, or anyone of your team could take two of us, we could discuss about it.

I'm mostly towards the Digital Design and architecture and Jaimin is into Digital design as well as coding.

Looking forward for responses

Thanks

Sri

Tags: None Add

Reply Quote Mark as Unread

Thread: Project 3 - File not found
Post: Project 3 - File not found
Author: Minghua Zhao
Posted Date: October 31, 2016 9:10 PM
Status: Published
Overall Rating:

In the Handout it says:

You will also need to copy & paste the IBM 0.13um Standard Cell Verilog file from the following network location to your project working directory:

`/fs1/vrg/CMC/kits/artisan-8rf/aci/sc-x.20090122/verilog/ibm13rfrvt.v`
This file contains the Verilog descriptions of all the standard cells in this technology, and must be included to perform functional simulation of the synthesized and placed & routed designs.

But I can't find the file `/fs1/vrg/CMC/kits/artisan-8rf/aci/sc-x.20090122/verilog/ibm13rfrvt.v`

```
ug207:~> ls -l /fs1/vrg/CMC/kits/artisan-8rf/aci/sc-x.20090122/verilog/ibm13rfrvt.v
ls: cannot access /fs1/vrg/CMC/kits/artisan-8rf/aci/sc-x.20090122/verilog/ibm13rfrvt.v: No such file or directory
```

I did not see any file called "ibm13rfrvt.v" under the Course Documents posted online either.

Am I missing something?

Tags: None Add

Reply Quote Mark as Read

Thread: Project 3 - File not found
Post: RE: Project 3 - File not found
Author: Minghua Zhao
Posted Date: October 31, 2016 9:12 PM
Status: Published
Overall Rating:

Nevermind.

Answer found in the other topic

https://portal.utoronto.ca/webapps/discussionboard/do/message?action=list_messages&forum_id=_530949_1&nav=discussion_board_entry&conf_id

Tags: None Add

Reply Quote Mark as Read

Thread: project3- can not open encounter
Post: project3- can not open encounter
Author: Xingyu Wan
Posted Date: November 1, 2016 5:54 PM
Edited Date: November 1, 2016 5:56 PM
Status: Published
Overall Rating:

When I try to run the Cadence Encounter place & route tool with the following command: `encounter`, it shows "Encounter terminated by internal (SEGV) error/signal..." Does anyone know how to solve this problem?

Thanks!

Xingyu Wan

Tags: None Add

Reply Quote Mark as Unread

Thread: project3- can not open encounter
Post: RE: project3- can not open encounter
Author: Minghua Zhao
Posted Date: November 1, 2016 6:01 PM
Status: Published
Overall Rating:

I have the same problem

Tags: None Add

Reply Quote Mark as Unread

Thread: project3- can not open encounter
Post: RE: project3- can not open encounter
Author: Minghua Zhao
Posted Date: November 3, 2016 6:02 PM
Status: Published
Overall Rating:

confirming that it works when loging-in remotely

Tags: None Add

Reply Quote Mark as Unread

Thread: project3- can not open encounter
Post: RE: project3- can not open encounter
Author: Ziming Li
Posted Date: November 1, 2016 6:07 PM
Status: Published
Overall Rating:

Same question here

Tags: None Add

Reply Quote Mark as Unread

Thread: project3- can not open encounter
Post: RE: project3- can not open encounter
Author: Yinze Fan
Posted Date: November 1, 2016 6:07 PM
Status: Published
Overall Rating:

Same problem :(

Tags: None Add

Reply Quote Mark as Unread

Thread: project3- can not open encounter
Post: RE: project3- can not open encounter
Author: Xunjun Mo
Posted Date: November 1, 2016 6:16 PM
Status: Published
Overall Rating:

I have the same problem. And here is my screen capture.

Attachment: Screenshot-2.png (52.096 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread: project3- can not open encounter
Post: RE: project3- can not open encounter
Author: Navid Sarhangnejad
Posted Date: November 2, 2016 4:52 PM
Status: Published
Overall Rating:

Is this the complete error message you see?

Is there any warning when you open a new terminal?

Tags: None Add

Reply Quote Mark as Unread

Thread: project3- can not open encounter
Post: RE: project3- can not open encounter
Author: Xunjun Mo
Posted Date: November 2, 2016 7:15 PM
Status: Published
Overall Rating:

Hi,

I don't think there is any warning. I include another screen capture, such that it's even more clear.

XunJun

Attachment: Screenshot.png (80.912 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread: project3- can not open encounter
Post: RE: project3- can not open encounter
Author: Navid Sarhangnejad
Posted Date: November 3, 2016 10:50 AM
Status: Published
Overall Rating:

Hi XunJun,

Does it work by remote connection (ssh, putty, etc.)?

Can you also upload the "encounter.log" file?

Thanks,

Navid

Tags: None Add

Reply Quote Mark as Unread

Thread: project3- can not open encounter
Post: RE: project3- can not open encounter
Author: Isa Khan
Posted Date: November 3, 2016 4:10 PM
Status: Published
Overall Rating:

I have the same issue. I've attached the encounter.log file.

Attachment: encounter.log (13.088 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread: project3- can not open encounter
Post: RE: project3- can not open encounter
Author: Xunjun Mo
Posted Date: November 3, 2016 4:54 PM
Status: Published
Overall Rating:

Hi Navid,

Remote connection works for me. I tried to remotely connect to ug150, ug220 and ug250, and they all work. So I think I will just do part 3 remotely. And Isa have uploaded the log file above. Thanks!

Xunjun

Tags: None Add

Reply Quote Mark as Unread

Thread: project3- can not open encounter
Post: RE: project3- can not open encounter
Author:
Posted Date: November 2, 2016 12:05 AM
Status: Published
Overall Rating:

Qijun Wen

Hi

Same problem when I using the ug machine in GB.

However I can open it by connecting to the ug machine remotely with ssh :)

Tags: None Add

Reply Quote Mark as Unread

Thread: project3- can not open encounter
Post: RE: project3- can not open encounter
Author: **Yifeng Zhang**

Posted Date: November 2, 2016 4:36 PM
Status: Published
Overall Rating:

Hi,

It works fine for me when i remote from home using putty/Xming. however i do have the same problem when running it in any of the ug machine.

Thanks

Yifeng

Tags: None Add

Reply Quote Mark as Unread

Thread: Project3 -- part2.2 -- a problem about generated estimated area unit
Post: Project3 -- part2.2 -- a problem about generated estimated area unit
Author: **Shengze Gao**

Posted Date: November 1, 2016 6:07 PM
Edited Date: November 1, 2016 6:08 PM
Status: Published
Overall Rating:

Hello,

The attached plot is part of my area report of synthesized multiplier. I wonder why the total area is undefined and what is the unit of the total cell area.

Really appreciate if anyone can help.

Thanks,

Shengze Gao

```
Number of ports:                 16
Number of nets:                  65
Number of cells:                 51
Number of references:             9

Combinational area:         498.240204
Noncombinational area:        0.000000
Net Interconnect area:       undefined  (No wire load specified)

Total cell area:            498.240021
Total area:                  undefined
```

Tags: None Add

Reply Quote Mark as Unread

Thread:
Project3 -- part2.2 -- a problem about generated estimated area unit

Post:
RE: Project3 -- part2.2 -- a problem about generated estimated area unit

Author: **Xingyu Wan**

Posted Date: November 1, 2016 6:16 PM
Status: Published
Overall Rating:

I think that the reason why the total area is undefined might be that the net interconnect area is undefined, which is stated on the picture.

Tags: None Add

Reply Quote Mark as Unread

Thread:
Project3 -- part2.2 -- a problem about generated estimated area unit

Post:
RE: Project3 -- part2.2 -- a problem about generated estimated area unit

Author: **Minghua Zhao**

Posted Date: November 2, 2016 8:49 PM
Status: Published
Overall Rating:

My vote of the unit goes in "um"

Tags: None Add

Reply Quote Mark as Unread

Thread: Project3 -- part2.2 -- a problem about generated estimated area unit
Post: RE: Project3 -- part2.2 -- a problem about generated estimated area unit
Author: Shengze Gao

Posted Date: November 10, 2016 10:29 PM
Status: Published
Overall Rating:

Yes, it is um^2 which could be proved by the report summary obtained in Part3.7.

Attachment: 000.png (23.867 KB)

Tags: None Add

Reply Quote Mark as Read

Thread: Project 3: Question on the unit of delay in timing report
Post: Project 3: Question on the unit of delay in timing report
Author: Xunjun Mo

Posted Date: November 1, 2016 6:08 PM
Status: Published
Overall Rating:

Hi,

I have a question on analyzing the timing report. Specifically, what is the unit of delay in timing report? Sometimes it shows 'r' and sometimes it shows 'f'. I think 'f' means femto. But what is 'r' then? Are any people having the same problem? And the screen capture of my timing report is attached. Thanks.

Xunjun

Attachment: Timing_report.png (55.175 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread: Project 3: Question on the unit of delay in timing report
Post: RE: Project 3: Question on the unit of delay in timing report
Author: Xingyu Wan

Posted Date: November 1, 2016 6:12 PM
Status: Published
Overall Rating:

I have the same question.

Tags: None Add

Reply Quote Mark as Unread

Thread:
Project 3: Question on the unit of delay in timing report
Post:
RE: Project 3: Question on the unit of delay in timing report
Author: **Yinze Fan**

Posted Date: November 1, 2016 6:17 PM
Status: Published
Overall Rating:

Just use total arrival time (1.51f in ur case) to calculate the clk frequency

Tags: None Add

Reply Quote Mark as Unread

Thread:
Project 3: Question on the unit of delay in timing report
Post:
RE: Project 3: Question on the unit of delay in timing report
Author: **Ziming Li**

Posted Date: November 1, 2016 6:26 PM
Status: Published
Overall Rating:

Hi Xunjun,

I don't really have "r" unit, all of them are "f", I think the reason could be that we are using different version of design vision. My log file looks like the following:]

Best,

Ziming

Attachment: Screenshot.png (24.273 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread:
Project 3: Question on the unit of delay in timing report
Post:

Posted Date: November 1, 2016 11:21 PM
Status: Published
Overall Rating:

RE: Project 3: Question on the unit of delay in timing report

Author: Genwen Zhao

By default, the unit for timing report is ns. "f" means falling transition, "r"mean rising transition

Tags: None Add

Reply Quote Mark as Unread

Thread:
Project 3: Question on the unit of delay in timing report

Post:
RE: Project 3: Question on the unit of delay in timing report

Author: Minghua Zhao

Posted Date: November 2, 2016 4:27 PM
Status: Published
Overall Rating:

That's an enlightening answer indeed.

Would you mind posting where you found the information?

Tags: None Add

Reply Quote Mark as Unread

Thread:
Project 3: Question on the unit of delay in timing report

Post:
RE: Project 3: Question on the unit of delay in timing report

Author: Genwen Zhao

Posted Date: November 2, 2016 9:22 PM
Status: Published
Overall Rating:

Hi,

All units are defined by technology file indeed. The Design Compiler reads in the technology file. From the synthesis_script.tcl. You see that the library is pointing to scx3_cmos8rf_rvt_tt_1p2v_25c.db

However, .db is not readable format. But its corresponding file is .lib (just think of it as different CAD tools use different format of the same file)

so if you take a look at this one:

/cmc/kits/artisan-8rf/aci/sc-x.20090122/synopsys/scx3_cmos8rf_rvt_tt_1p2v_25c.lib

/* unit attributes */ time_unit : "1ns"; voltage_unit : "1V"; current_unit : "1mA"; pulling_resistance_unit : "1kohm"; leakage_power_unit : "1pW"; capacitive_load_unit (1.0,pf);

That is how you find out the time unit is ns.

As for "f" and "r". That is based on my work experience :) I have dealt with a lot of timing analysis at work :)

Hope this help.

Tags: None Add

Reply Quote Mark as Unread

Thread: Diffrerent version of design_vision **Posted Date:** November 1, 2016 6:36 PM
Post: Diffrerent version of design_vision **Status:** Published
Author: Yinze Fan **Overall Rating:**

I noticed that schematics generated by 2012 and 2005 version of design vision are different. Also the total areas are different (2012 version has smaller area). Do we have to switch to the newer version or both of them are fine.

Tags: None Add

Reply Quote Mark as Unread

Thread: Diffrerent version of design_vision **Posted Date:** November 2, 2016 2:41 PM
Post: RE: Diffrerent version of design_vision **Status:** Published
Author: Genwen Zhao **Overall Rating:**

Hi,

Project 3 handout says we should load the 2011 version synopsys. So I assume we use the latest version :)

Tags: None Add

Reply Quote Mark as Unread

Thread: ncverilog error **Posted Date:** November 1, 2016 9:54 PM
Post: ncverilog error **Edited Date:** November 1, 2016 9:55 PM
Author: **Status:** Published

Shu Wang Overall Rating:

There is an error whenever I'm calling ncverilog. I did include all the source files in .cshrc

```
DEFINE cdsDefTechLib $CDS_INST_DIR/tools/dfII/etc/cdsDefTechLib
|
ncverilog: *W,DLCPTH (./cds.lib,1): cds.lib Invalid path '/CMC/tools/cadence/IUS.08.20.029.linux/tools/df
DEFINE basic $CDS_INST_DIR/tools/dfII/etc/cdslib/basic
|
ncverilog: *W,DLCPTH (./cds.lib,2): cds.lib Invalid path '/CMC/tools/cadence/IUS.08.20.029.linux/tools/df
DEFINE analogLib $CDS_INST_DIR/tools/dfII/etc/cdslib/artist/analogLib
|
ncverilog: *W,DLCPTH (./cds.lib,3): cds.lib Invalid path '/CMC/tools/cadence/IUS.08.20.029.linux/tools/df
DEFINE TSMCp35myPadFrame
|
ncverilog: *F,DLCSYN (./cds.lib,21): cds.lib Syntax error 'DEFINE TSMCp35myPadFrame'.
```

Thoughts?

Tags: None Add

Reply Quote Mark as Unread

Thread: ncverilog error
Post: RE: ncverilog error
Author: **Ziming Li**
Posted Date: November 1, 2016 10:50 PM
Status: Published
Overall Rating:

Hi Shu Wang,

Did you log out of the system and login back after you changed .cshrc file? you need to do so everytime you change this system file.

Best,

Ziming

Tags: None Add

Reply Quote Mark as Unread

Thread: ncverilog error
Post: RE: ncverilog error
Author: **Shu Wang**
Posted Date: November 2, 2016 2:00 PM
Status: Published
Overall Rating:

yup, same problem :(

Tags: None Add

Reply Quote Mark as Unread

Thread: ncverilog error
Post: RE: ncverilog error
Author: Gerard O'Leary
Posted Date: November 7, 2016 4:08 PM
Status: Published
Overall Rating:

Hi Shu,

Is this still an issue? Which machine are you running from? I don't have any problems opening it on UG241:

ug241:/> source /CMC/tools/CSHRCs/Synopsys.2011.09

ug241:/> design_vision
Design Compiler Graphical

DC Ultra (TM)

DFTMAX (TM)

Power Compiler (TM)

...

Version F-2011.09-SP4 for linux -- Mar 02, 2012

Copyright (c) 1988-2012 Synopsys, Inc.

Thanks,

Gerard

Tags: None Add

Reply Quote Mark as Unread

Thread: Question about encounter
Post: Question about encounter
Author: Qijun Wen
Posted Date: November 2, 2016 12:48 AM
Status: Published
Overall Rating:

Hi all,

I have 3 questions about place&route using encounter.

First question about placing the power stripes, does the handout Part3-2 means set the VDD to M3 with 1 width an 1 spacing and VSS to MQ with 1 width and 1 spacing? By default, the VSS goes before VDD, thus follow the instruction in Part3-2 I will set VDD to MQ, and VSS to M3.

Another question is about the power analysis in Part3-6. When I try to perform the power analysis following the instruction of the handout about Part3-6, I cannot choose run.

Does it means I have to set up the power analysis? Any tutorial material about the setting up the power analysis?(I can not find in the user manual.)

And last question is about the wcell_nopower.v file. It is said to be a file for project3, but I have no idea where to use it. Dose it relate to the power or time analysis. It seem to provide us the verilog model for some cell.

Thanks

Qijun Wen

Tags: None Add

Reply Quote Mark as Unread

Thread: Question about encounter
Post: RE: Question about encounter
Author: **Peter Hermansen**
Posted Date: November 2, 2016 11:33 AM
Status: Published
Overall Rating:

Hi Qijun,

To answer the first two of your questions:

You should have two metal strips in each M3 and MQ. One of the strips should be VSS and one should be VDD for both M3 and MQ, if there is a space between the names it should assign one to each. This should be set by default and you shouldn't have to change anything other than the width and spacing.

You will need to setup the power analysis. In the setup just leave everything on default and press 'OK'. Then you should be able to 'RUN" and select the activity factor and frequency.

As for you last question I am not too sure.

Peter

Tags: None Add

Reply Quote Mark as Unread

Thread: Question about encounter
Post: RE: Question about encounter
Author: **Qijun Wen**
Posted Date: November 3, 2016 11:12 PM
Status: Published
Overall Rating:

Hi Peter,

So you means we have preform the power analysis for different frequency manually. By setting the frequency 100 MHz, 200MHz ... 1GHz?

Thank you

Qijun

Tags: None Add

Reply Quote Mark as Unread

Thread: Question about encounter
Post: RE: Question about encounter
Author: **Tianxiang Chen**
Posted Date: November 4, 2016 5:23 PM
Status: Published
Overall Rating:

Yes, you can do that and use excel to generate a plot.

Tianxiang

Tags: None Add

Reply Quote Mark as Unread

Thread: Error in generated Netlist
Post: Error in generated Netlist
Author: **Srinidhi Balasubrahmanya**
Posted Date: November 2, 2016 4:37 PM
Status: Published
Overall Rating:

After the Synthesis using Standard Cells, Design Compiler's output multiplier_syn.v is having this error (attached screenshot)

Any suggestions on how could I correct them?

The primitive worklib.udp_* don't have any errors.

Thanks

Sri

Attachment: Error.png (38.088 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread: Error in generated Netlist
Post: RE: Error in generated Netlist
Author: Yifeng Zhang
Posted Date: November 2, 2016 4:38 PM
Status: Published
Overall Rating:

Hi

Did you include the `timescale 1ns/1ps at the beginning of your verilog code?

Thanks

Yifeng

Tags: None Add

Reply Quote Mark as Unread

Thread: Error in generated Netlist
Post: RE: Error in generated Netlist
Author: Srinidhi Balasubrahmanya
Posted Date: November 2, 2016 5:03 PM
Status: Published
Overall Rating:

Yes, I have done it.

Sri

Tags: None Add

Reply Quote Mark as Unread

Thread: Error in generated Netlist
Post: RE: Error in generated Netlist
Author: Minghua Zhao
Posted Date: November 2, 2016 6:24 PM
Status: Published
Overall Rating:

how about right before your multiplier module?

Tags: None Add

Reply Quote Mark as Unread

Thread: Error in generated Netlist
Post: RE: Error in generated Netlist
Author: Genwen Zhao
Posted Date: November 2, 2016 9:28 PM
Status: Published
Overall Rating:

hey Sri,

Are you sure this is an error from DC? it looks like error you got when you run ncverilog right ?

If this is the case, you are running sim for synthesized netlist. make sure you include the ibm standard cell verilog code AND make sure you put it first !!

ncverilog ibm_watever.v multiplier_syn.v test_bench.v

Thanks

Tags: None Add

Reply Quote Mark as Unread

Thread: Error in generated Netlist
Post: RE: Error in generated Netlist
Author: Srinidhi Balasubrahmanya
Posted Date: November 4, 2016 6:37 PM
Status: Published
Overall Rating:

Thanks Genwen. That helped. I got it fixed.

Sri

Tags: None Add

Reply Quote Mark as Unread

Thread: Question on project 3 Part I
Post: Question on project 3 Part I
Author: Xunjun Mo
Posted Date: November 3, 2016 5:52 PM
Status: Published
Overall Rating:

Hi,

I wonder if there is any constraint on the level of abstraction for the HDL code for the 4*4 unsigned multiplier? Specifically, do I have to construct the multiplier from adders? Or I can use higher level description for my HDL code? Thanks.

XunJun

Tags: None Add

Reply Quote Mark as Unread

Thread: Question on project 3 Part I
Post: RE: Question on project 3 Part I
Author: Minghua Zhao
Posted Date: November 3, 2016 6:05 PM
Status: Published
Overall Rating:

Hi XunJun,

From the reference in the textbook, the CSA and CPA modules were constructed with a combination of full adders and logic blocks. From my understanding the Verilog code should follow the same modularization.

Cheers

Tags: None Add

Reply Quote Mark as Unread

Thread: Question on project 3 Part I
Post: RE: Question on project 3 Part I
Author: Gerard O'Leary
Posted Date: November 7, 2016 3:26 PM
Status: Published
Overall Rating:

Hi XunJun,

As assumed by Minghua, it is expected that you will design the array multiplier without relying on the * operator.

Thanks,

Gerard

Tags: None Add

Reply Quote Mark as Unread

Thread: Geometry Error after placing Nano Route
Post: Geometry Error after placing Nano Route
Author: Ziming Li
Posted Date: November 4, 2016 11:21 AM
Status: Published
Overall Rating:

Hi,

When I'm working on Project 3 Part 3 Step 4 I'm getting geometry error (violation) after placing Nano Route. I've attached the marked part of layout and terminal message. I'm wondering what might cause this issue and whether anyone has similar issue? Noted that my verilog design did pass part 1 and part 2 analysis.

Thanks,

Ziming

Attachment: geometry error.png (7.365 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread: Geometry Error after placing Nano Route
Post: RE: Geometry Error after placing Nano Route
Author: Ziming Li

Posted Date: November 4, 2016 11:21 AM
Status: Published
Overall Rating:

And here is my terminal message after geometry verify

Attachment: violation.png (37.14 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread: Geometry Error after placing Nano Route
Post: RE: Geometry Error after placing Nano Route
Author: Ziming Li

Posted Date: November 4, 2016 1:11 PM
Status: Published
Overall Rating:

Never mind I found the reason. When I make verilog design based on figure 11.74, the bottom left CPA has a Cout that I just leave it there, which cause the issue. My understanding is that you cannot leave any output wire (other than you defined) without treatment. By manually assigned it to be zero and then re-do Part1 - Part3 things turn out to be fine.

Tags: None Add

Reply Quote Mark as Unread

Thread: Part 3.6 - Power Analysis
Post: Part 3.6 - Power Analysis
Author: Srinidhi Balasubrahmanya
Posted Date: November 4, 2016 6:54 PM
Status: Published
Overall Rating:

Hello,

I'm doing Power Analysis, part3.6, where it says "`Power > Power Analysis > Run`" But unless you Setup first, I am not able to "Run". And I am not sure what to select during Setup.

If you select 'Static', you can't have a frequency range.

If you select 'Dynamic', it asks for a library which I have no idea where to find.

I have attached a .docx which contains 3 screen shots which could probably explain it better

Any help would be appreciated.

Thanks

Sri

Attachment: Screenshots.docx (77.285 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread: Part 3.6 - Power Analysis
Post: RE: Part 3.6 - Power Analysis
Author: Gerard O'Leary
Posted Date: November 7, 2016 4:14 PM
Status: Published
Overall Rating:

Hi Sri,

Please use Encounter 9.1 for now for power analysis.

Thanks,

Gerard

Tags: None Add

Reply Quote Mark as Unread

Thread: Problems regarding LEF files
Posted Date: November 4, 2016 7:49 PM

Post: Problems regarding LEF files
Author: Jialing Wang
Status: Published
Overall Rating:

Hi guys, I cannot find the LEF files when I'm trying to import my design to the encounter. Does someone have the same problem? Thanks so much!

Tags: None Add

Reply Quote Mark as Unread

Thread: Problems regarding LEF files
Post: RE: Problems regarding LEF files
Author: Minghua Zhao
Posted Date: November 6, 2016 7:06 PM
Status: Published
Overall Rating:

What's the error message?

What step of Project 3 are you on?

Tags: None Add

Reply Quote Mark as Unread

Thread: Problems regarding LEF files
Post: RE: Problems regarding LEF files
Author: Gerard O'Leary
Posted Date: November 7, 2016 3:24 PM
Status: Published
Overall Rating:

Hi Jialing,

Do you mean you don't have access to the LEF files in encounter_config.conf? When you run the following, what do you see?:

ls -ltr /nfs/vrg/cmc/cmc/kits/artisan-8rf/aci/sc-x.20090122/lef/ibm13rfrvt_macros.lef

It looks ok on my end:

-rw-r--r--+ 1 cmcmgr cmrf8sf 2023691 Feb 3 2009 /nfs/vrg/cmc/cmc/kits/artisan-8rf/aci/sc-x.20090122/lef/ibm13rfrvt_macros.lef

This may be an issue with your 0.13um library permissions, so let me know asap.

Thanks,

Gerard

Tags: None Add

Reply Quote Mark as Unread

Thread: solved: Can't open encounter: internal error
Post: solved: Can't open encounter: internal error
Author: Shu Wang
Posted Date: November 6, 2016 4:25 PM
Edited Date: November 6, 2016 8:14 PM
Status: Published
Overall Rating:

See screenshot attached. Thanks.

EDIT: need solution for local access; laptop is getting fixed this week

Solution: ssh using local station

Attachment: encounter_err.png (16.135 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread: solved: Can't open encounter: internal error
Post: maybe
Author: Minghua Zhao
Posted Date: November 6, 2016 7:03 PM
Status: Published
Overall Rating:

Try to VNC from a Lab computer into another Lab computer

Tags: None Add

Reply Quote Mark as Unread

Thread: solved: Can't open encounter: internal error
Post: RE: maybe
Author: Shu Wang
Posted Date: November 6, 2016 8:18 PM
Status: Published
Overall Rating:

Thanks. If I had a dollar every time I ask a stupid question I'd have enough money to pay for my tuition.

Tags: None Add

Reply Quote Mark as Unread

Thread:
Posted Date: November 7, 2016 6:36 PM

solved: Can't open encounter: internal error
Post: RE: maybe
Author: Minghua Zhao

Status: Published
Overall Rating:

Haha, not a problem. Everyone's brains glitches at times.

Tags: None Add

Reply Quote Mark as Unread

Thread:
solved: Can't open encounter: internal error
Post:
RE: solved: Can't open encounter: internal error
Author: Gerard O'Leary

Posted Date: November 7, 2016 3:17 PM
Status: Published
Overall Rating:

Hi Shu,

This seems to work fine when SSHing to the machines - can you confirm that you only see this issue when logged on directly? i.e. physically sitting at the machine.

We're trying to reproduce this to get to the cause.

Thanks,

Gerard

Tags: None Add

Reply Quote Mark as Unread

Thread:
solved: Can't open encounter: internal error
Post:
RE: solved: Can't open encounter: internal error
Author: Shu Wang

Posted Date: November 9, 2016 4:55 PM
Status: Published
Overall Rating:

Hi Gerrard, yes I am unable to open Encounter via terminal on a local machine; and yes it works when SSH to another machine next to me!

Tags: None Add

Reply Quote Mark as Unread

Thread:

Posted Date: November 9, 2016 9:10 PM

Written Update - Week 10 Complete Schematic
Post: Written Update - Week 10 Complete Schematic
Author: Minghua Zhao

Status: Published
Overall Rating:

I just wanted to clarify, that the deliverable for next Tuesday is our last Tuesday Presentation Slides updated with the completed schematic diagrams.

(i.e. do we need simulations too, or just the schematic diagrams?)

Best Regards

Tags: None Add

Reply Quote Mark as Read

Select: All None
Mark Tag Text: Add

← OK

Thread: Project Submission Format - Project 1

Select: All None

2 Post(s) in this Thread 0 Unread

Message Actions Expand All Collapse All

Minghua Zhao 11 months ago

Project Submission Format - Project 1

COLLAPSE

Overall Rating:

Hi,

Is there a specification on the deliverables for the projects?

The project handout is not specific on what plots or calculations we have to include for many of the sections.

For example, can we submit hand-written calculations?

Thanks,

MZ

Reply Quote Edit Delete

Navid Sarhangnejad 11 months ago

RE: Project Submission Format - Project 1

Overall Rating:

Hello Minghua,

Your report can include any format like handwritten parts, exported images, screenshots and etc. Of course all should be neatly done and

make sure it's easily readable (for example, avoid black backgrounds).

You need to deliver whatever the questions are asking, and provide the solutions or approaches you have taken.

Regards,

Navid

Select: All None

Message Actions Expand All Collapse All

← OK

Collection

Users can Collect posts into a printable, sortable format. Collections are a good way to organize posts for quick reading. A Collection must be created to tag posts. More Help

Print Preview Filter

Sort by Thread Order Order ▼ Descending

Select: All None

Mark

Thread:
ISML Project: Clock-phase generator simulation and layout
Post:
ISML Project: Clock-phase generator simulation and layout
Author: Gerard O'Leary

Posted Date: October 25, 2016 5:24 PM
Status: Published
Overall Rating:

Clock-phase generator simulation and layout

Contact: Reza - m.reza@ece.utoronto.ca

Recommended group size: 2

Reply Quote Mark as Unread

Thread:
ISML Project: 16-bit digital filter for simulation and layout
Post:
ISML Project: 16-bit digital filter for simulation and layout
Author: Gerard O'Leary

Posted Date: October 25, 2016 5:25 PM
Edited Date: October 25, 2016 5:26 PM
Status: Published
Overall Rating:

16-bit CIC digital filter for simulation and layout
Contact: Reza - m.reza@ece.utoronto.ca

Recommended group size: 2

Reply Quote Mark as Unread

Thread:
ISML Project: 16-bit reconfigurable accumulate and dump decimation 2nd order digital filter
Post:
ISML Project: 16-bit reconfigurable accumulate and dump decimation 2nd order digital filter
Author: Gerard O'Leary

Posted Date: October 25, 2016 5:26 PM
Edited Date: October 25, 2016 5:27 PM
Status: Published
Overall Rating:

16-bit reconfigurable accumulate and dump decimation 2nd order digital filter
Contact: Reza - m.reza@ece.utoronto.ca
Recommended group size: 2 to 3

Reply Quote Mark as Unread

Thread:
ISML Project: VLSI Implementation of the Hyperbolic CORDIC Algorithm
Post:
ISML Project: VLSI Implementation of the Hyperbolic CORDIC Algorithm
Author: Gerard O'Leary

Posted Date: October 25, 2016 5:28 PM
Status: Published
Overall Rating:

VLSI Implementation of the Hyperbolic CORDIC Algorithm

Contact: Gerard - gerard.oleary@mail.utoronto.ca

Recommended group size: 2 to 4

Reply Quote Mark as Unread

Thread:
ISML Project: OpenMSP430 VLSI Implementation and Power Analysis
Post:
ISML Project: OpenMSP430 VLSI Implementation and Power Analysis
Author: Gerard O'Leary

Posted Date: October 25, 2016 5:29 PM
Status: Published
Overall Rating:

OpenMSP430 VLSI Implementation and Power Analysis

Contact: Gerard - gerard.oleary@mail.utoronto.ca

Recommended group size: 2 to 4

Reply Quote Mark as Unread

Thread: ISML project: 50-Column parallel Delta-Sigma incremental ADC for image sensor applications
Post: ISML project: 50-Column parallel Delta-Sigma incremental ADC for image sensor applications
Author: Navid Sarhangnejad

Posted Date: October 26, 2016 8:28 AM
Status: Published
Overall Rating:

50-Column parallel Delta-Sigma incremental ADC for image sensor application

Recommended group size: 3-4 people

Including IO LVDS channels:

Recommended group size: 5-6 people

Contact: Navid - sarhangn@ece.utoronto.ca

Reply Quote Mark as Read

Thread: first update on Nov 1st Tuesday
Post: first update on Nov 1st Tuesday
Author: Yifeng Zhang

Posted Date: October 29, 2016 2:30 PM
Status: Published
Overall Rating:

Hi,

For our very first final project written update, do we work on the Group formation and project definition or system outline?

Thanks

Reply Quote Mark as Unread

Thread: first update on Nov 1st Tuesday
Post: RE: first update on Nov 1st Tuesday

Posted Date: October 30, 2016 4:24 PM
Status: Published
Overall Rating:

Author: Ziming Li

Hi Yifeng,

According to final project intro doc and course outline website "http://www.eecg.utoronto.ca/~roman/teaching/1388/2016/assignments.htm", we are suppose to submit **system outline** on Tuesday. So you have to decide your team member and topic before Tuesday.

Best,

Ziming

Reply Quote Mark as Unread

Thread: first update on Nov 1st Tuesday
Post: RE: first update on Nov 1st Tuesday
Author: Shengze Gao
Posted Date: October 30, 2016 9:20 PM
Status: Published
Overall Rating:

According to the schedule of final project, we need to submit System Outline on this Tuesday. And we also need to briefly mention the Group formation and project definition at the beginning part of System Outline as indicated in Section5.2 of Final Project Handout. And make sure this written update is less than 10 slides.

Reply Quote Mark as Unread

Thread: Hardware Encription
Post: Hardware Encription
Author: Minghua Zhao
Posted Date: October 30, 2016 4:13 PM
Status: Published
Overall Rating:

I'm curious on how hardware encryption is built.

The resources I found online were very general (i.e. https://en.wikipedia.org/wiki/Hardware-based_full_disk_encryption)

So that's not nearly enough to get started on anything.

Are there research papers or algorithms TAs or Prof can share? Or any teaching material into what/how hardware encryption works? I want to read into it a bit.

Basically I would like to gage whether this topic is feasible as a Project Topic. I envision building part of an encryption algorithm in hardware. Our group size is 5

people.

Warm Regards,

Minghua

Reply Quote Mark as Read

Thread: Hardware Encription
Post: RE: Hardware Encription
Author: Minghua Zhao
Posted Date: October 30, 2016 4:27 PM
Status: Published
Overall Rating:

(Aside:

A bit about myself: I'm M.Eng in Electronics with an undergrad in Electrical Engineering at U of T, Majoring in areas of computer hardware and controls. I've been working in the software industry for the past 2 years. Some relevant courses I've taken:

- ECE451 - VLSI Systems and Design
- ECE552 - Computer Architecture
- ECE331 - Analog Electronics
- ECE334 - Digital Electronics
- ECE316 - Communication Systems
- ECE342 - Computer Hardware

)

Reply Quote Mark as Read

Thread: Looking to join a group
Post: Looking to join a group
Author: Jaimin Joshi
Posted Date: October 31, 2016 6:33 PM
Status: Published
Overall Rating:

Hi everyone,

I'm an MEng student and my previous work experience includes verification/validation and digital design for ASICs and FPGAs. I am open to both research and non-research based projects.

Please get in touch if you are looking for a group member or want to form a group.

Thanks,

Jaimin

Reply Quote Mark as Read

Select: All None

Mark

← OK

Collection

Users can Collect posts into a printable, sortable format. Collections are a good way to organize posts for quick reading. A Collection must be created to tag posts. More Help

Print Preview Filter

Sort by Thread Order Order ▼ Descending

Select: All None

Mark Tag Text: Add

Thread: Can't connect Poly1 to Metal1
Post: Can't connect Poly1 to Metal1
Author: Minghua Zhao
Posted Date: September 21, 2016 10:03 PM
Status: Published
Overall Rating:

When drawing poly1 path, "Change to Layer" doesn't offer an option for dropping a VIA to metal1

The reverse is true too (metal1-> change to layer -> poly1)

See attached screen shot for reference.

Am I missing something?

Attachment: Screenshot-1.png (110.579 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread: Can't connect Poly1 to Metal1
Post: RE: Can't connect Poly1 to Metal1
Author: Yifeng Zhang
Posted Date: September 24, 2016 1:48 PM
Status: Published
Overall Rating:

I have the same problem

Tags: None Add

Reply Quote Mark as Unread

Thread: Can't connect Poly1 to Metal1
Post: RE: Can't connect Poly1 to Metal1
Author: **Gerard O'Leary**
Posted Date: September 26, 2016 1:24 PM
Status: Published
Overall Rating:

Hi Minghua/Yifeng,

When you start a path from M1 then change to layer poly1 and complete the connection, a contact should automatically be placed (e.g. below). The reverse is also true. Alternatively, you can manually draw your contact.

Thanks,
Gerard

Attachment: poly1 to M1 (12.363 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread: Can't connect Poly1 to Metal1
Post: RE: Can't connect Poly1 to Metal1
Author: **Yifeng Zhang**
Posted Date: September 26, 2016 11:16 PM
Status: Published
Overall Rating:

Hi Gerard,

please see the attached picture. I was trying to draw m1 to poly. When I click on the 'Change to Layer' selection, there are only metal1 and metal2 options for me to choose. If i draw poly and change to m1, that selection becomes 'None'. Via_issue.png

Tags: None Add

Reply Quote Mark as Unread

Thread: Can't connect Poly1 to Metal1
Post: RE: Can't connect Poly1 to Metal1
Author: **Michael Halamicek**
Posted Date: September 26, 2016 5:10 PM
Status: Published
Overall Rating:

Alternatively, there is a cell in the "wcells" library called "con", which is just M1 and a contact. The contact is sized correctly and the M1 has the minimum enclosure to pass DRC.

Best ,

Michael

Tags: None Add

Reply Quote Mark as Unread

Thread:
Error opening Cadence with CMOSP35 kit
Post:
Error opening Cadence with CMOSP35 kit
Author:
Christos Konstantopoulos

Posted Date: September 23, 2016 12:42 PM
Status: Published
Overall Rating:

Dear all ,

I have followed the instructions, however I am getting this strange message while I am opening Cadence with kit CMOSP35

CMCcdsTech=cmosp35; export CMCcdsTech; icfb -log /guest/k/konsta26/CDSlogs/CDS.log.13173 -display localhost:23.0 &
ug180:~/CMOSP35%
/CMC/tools/cadence.2005a/IC.5141.USR2.linux/tools/dfII/bin/icfb.exe: error while loading shared libraries: libXp.so.6: cannot open shared object file: No such file or directory

Could you please help me?

With Regards,

Christos

Tags: None Add

Reply Quote Mark as Unread

Thread:
Error opening Cadence with CMOSP35 kit
Post:
RE: Error opening Cadence with CMOSP35 kit
Author:
Yifeng Zhang

Posted Date: September 23, 2016 9:29 PM
Status: Published
Overall Rating:

hi Christos, I had the same problem when I followed the steps from TA's announcement. Try to follow the VLSI manual and that solves my problem.

Thanks

Rudy

Tags: None Add

Reply Quote Mark as Unread

Thread: Error opening Cadence with CMOSP35 kit
Post: RE: Error opening Cadence with CMOSP35 kit
Author: Gerard O'Leary

Posted Date: September 26, 2016 1:05 PM
Status: Published
Overall Rating:

Hi Christos,

Thanks for posting here - I think we've resolved this offline.

For anyone else experiencing this issue, please follow the VLSI manual and ensure that you've sourced the appropriate CSHRCs, i.e.:

"source /CMC/tools/CSHRCs/Cadence"

Before running startCds.

Thanks,
Gerard

Tags: None Add

Reply Quote Mark as Unread

Thread: Netlist Generation Issue
Post: Netlist Generation Issue
Author: Michael Halamicek

Posted Date: September 26, 2016 4:51 PM
Status: Published
Overall Rating:

When I use ADE to generate netlists for circuits/subcircuits, the drain and source perimeter values always have an additional decimal. This throws an error in the CIW. I have attached a screenshot showing the problem. Simulations still run fully, but it is not clear how the faulty netlist affects the results. It would likely affect the computed drain and source cap values, which is not desirable.

It does not affect widths less than 1um, as those values are reported in nm.

It is not fixed by entering the device width in 1000's of nm as the values are automatically converted to um.

Thanks

Attachment: Capture.PNG (120.503 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread: Netlist Generation Issue
Post: RE: Netlist Generation Issue
Author: Michael Halamicek
Posted Date: September 26, 2016 5:11 PM
Status: Published
Overall Rating:

Should I contact Jaro with this issue?

Tags: None Add

Reply Quote Mark as Unread

Thread: Netlist Generation Issue
Post: RE: Netlist Generation Issue
Author: Navid Sarhangnejad
Posted Date: September 28, 2016 12:32 PM
Status: Published
Overall Rating:

Hello Michael,

Never contact Jaro directly. We will direct you to him if necessary.

I was trying to reproduce the error, but I couldn't! Could you please come to our office during the office hour tomorrow with your laptop to go through it together?

Thanks,

Navid

Tags: None Add

Reply Quote Mark as Unread

Thread: Netlist Generation Issue
Post: RE: Netlist Generation Issue
Author: Michael Halamicek
Posted Date: September 28, 2016 1:17 PM
Status: Published
Overall Rating:

Sounds good. I'll drop by after class.

Tags: None Add

Reply Quote Mark as Unread

Thread: Schematic Editor License Issue
Post: Schematic Editor License Issue
Author: Dhruv Patel
Posted Date: October 2, 2016 3:17 PM
Status: Published
Overall Rating:

Hi,

I am able to run cadence for cmosp35 kit and create cellview as well as able to access cmosp35 kit instances. However, whenever I create my own cellview and try to add an instance in the schematic editor, I get this error saying that it was unable to checkout a schematic editor license. As a result, I am unable to add any type of instances; in fact the instance window doesn't even open. I have attached the error log in an attachment.

Additional info: I am running this cadence from ug251 eecg server.

Thanks!

Dhruv

Attachment: schematic editor licensing issue.png (95.517 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread: Schematic Editor License Issue
Post: RE: Schematic Editor License Issue
Author: Gerard O'Leary
Posted Date: October 3, 2016 5:19 PM
Status: Published
Overall Rating:

Resolved.

Tags: None Add

Reply Quote Mark as Unread

Thread: LVS Rules file does not exist
Post: LVS Rules file does not exist
Author: Saba Zargham
Posted Date: October 4, 2016 7:22 PM
Status: Published
Overall Rating:

Hi,

So I've been trying to run LVS on my layout. I filled the "Rules file" section with "divaLVS.rul" as said in the user manual. But I keep getting the same error, " LVS rules

file does not exist or empty. The .rul also isn't available in the /LVS directory. So I was wondering if its a library access issue or something else?

Thanks in advance,
Saba

Tags: None Add

Reply Quote Mark as Unread

Thread: LVS Rules file does not exist
Post: RE: LVS Rules file does not exist
Author: Samuel Da Silva Carvalho
Posted Date: October 4, 2016 7:34 PM
Status: Published
Overall Rating:

Do you have a "/" before LVS on top of the LVS window? If you do, remove it.

Also try adding the "Rules library" as cmosp35.

Here's my screenshot so you can compare.

Attachment: Untitled.png (11.509 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread: LVS Rules file does not exist
Post: RE: LVS Rules file does not exist
Author: Jianxiong Xu
Posted Date: October 30, 2016 5:47 PM
Status: Published
Overall Rating:

You can add "cmosp35" in your rule library.

Tags: None Add

Reply Quote Mark as Unread

Thread: different simulation
Post: different simulation
Author: Yikun Guo
Posted Date: October 6, 2016 7:45 PM
Status: Published
Overall Rating:

Hi,

For the delay simulation, I find that if I change a lab and a computer, the result will change. Do you have any problem like that? And should the lab room number be mentioned in the report?

Tags: None Add

Reply Quote Mark as Unread

Thread: different simulation
Post: RE: different simulation
Author: **Navid Sarhangnejad**
Posted Date: October 12, 2016 9:13 AM
Status: Published
Overall Rating:

Hi Yikun,

Is the difference significant? Or it's less than 1% change in the resulting delay? If it's small, please neglect it.

Navid

Tags: None Add

Reply Quote Mark as Unread

Thread: Problem starting design_analyzer
Post: Problem starting design_analyzer
Author: **Peter Hermansen**
Posted Date: October 7, 2016 1:36 PM
Status: Published
Overall Rating:

Hello,

I have been working through chapter 7 in the "VLSI User Manual" and have been unable to get the design analyzer working. I have followed the instructions in the user manual to set up the environment but when I use the command "design_analyzer &". I get the following message:

/CMC/tools/synopsys/syn_vX-2005.09/linux/syn/bin/dc_view_exec: error while loading shared libraries: libtermcap.so.2: cannot open shared object file: No such file or directory

[1] Exit 127 design_analyzer

Any help would be appreciated,

Peter

Tags: None Add

Reply Quote Mark as Unread

Thread: Problem starting design_analyzer
Post: RE: Problem starting design_analyzer
Author: Tianxiang Chen
Posted Date: October 9, 2016 4:09 PM
Status: Published
Overall Rating:

Same problem here.

Tags: None Add

Reply Quote Mark as Unread

Thread: Problem starting design_analyzer
Post: RE: Problem starting design_analyzer
Author: Gerard O'Leary
Posted Date: October 12, 2016 1:48 PM
Status: Published
Overall Rating:

Hi Peter,

Did you run: source /CMC/tools/CSHRCs/Synopsys ?

It seems to be working fine on my end...

What version of Linux are you using? (uname -r)

Thanks,
Gerard

Tags: None Add

Reply Quote Mark as Unread

Thread: Problem starting design_analyzer
Post: RE: Problem starting design_analyzer
Author: Peter Hermansen
Posted Date: October 12, 2016 2:29 PM
Status: Published
Overall Rating:

Yes I did run 'source /CMC/tools/CSHRCs/Synopsys'.

uname returns: 3.16.0-4-amd64

Peter

Tags: None Add

Reply Quote Mark as Unread

Thread: Problem starting design_analyzer
Post: RE: Problem starting design_analyzer
Author: Gerard O'Leary
Posted Date: October 13, 2016 7:36 PM
Edited Date: October 13, 2016 7:36 PM
Status: Published
Overall Rating:

Hi Peter,

Ok I'm using a newer kernel. I'll CC you on an email and we'll try to get it resolved.

Thanks,
Gerard

Tags: None Add

Reply Quote Mark as Unread

Thread: Problem starting design_analyzer
Post: RE: Problem starting design_analyzer
Author: Genwen Zhao
Posted Date: October 17, 2016 10:38 PM
Status: Published
Overall Rating:

hey Gerard,

Why don't we use design vision instead of design analyzer? i think i can launch the design vision by

```
source /CMC/tools/CSHRCs/Synopsys.2011.09

However, when i launch either dc_shell / design_vision, i am getting some errors.

Initializing...

Error: unknown command '/*' (CMD-005)

Error: unknown command '*' (CMD-005)

Error: unknown command '*' (CMD-005)

Error: unknown command '*' (CMD-005)
```

```
Error: can't read "SYNOPSYS": no such variable        Use error_info for
more info. (CMD-013)

Error: unknown command '*' (CMD-005)

Error: unknown command '*/' (CMD-005)

Error: unknown command '/*' (CMD-005)

Error: unknown command '/*' (CMD-005)

Error: unknown command 'search_path' (CMD-005)

Error: unknown command 'search_path' (CMD-005)

etc.

I have looked at the .synopsys_dc.setup. i wonder if that tcl file has
outdated syntax ?

maybe we should use

set search_path {.}

instead of :

search_path = {.}

or is it also related to linux version? any thoughts?
```

Tags: None Add

Reply Quote Mark as Unread

Thread: Problem starting design_analyzer **Posted Date:** October 21, 2016 11:26 AM
Post: RE: Problem starting design_analyzer **Status:** Published
Author: Gerard O'Leary **Overall Rating:**

FYI We resolved Peter's issue separately - thanks for flagging this!

Hi Genwen,

Design Vision is the newest version of the tool, and you could technically use either (and we will be refreshing the VLSI design manual to use it after this semester.. seeing as DA has been phased out).

Given that the project is relatively small, it would be best if we all stick to design_analyzer for now. Are you having any issues launching this after following section 7.2 in the manual?

Thanks,

Gerard

Tags: None Add

Reply Quote Mark as Unread

Thread: Problem starting design_analyzer
Post: RE: Problem starting design_analyzer
Author: Genwen Zhao
Posted Date: October 21, 2016 9:49 PM
Status: Published
Overall Rating:

Hi Gerard,

I followed the 7.2, ran into the same issue as Peter.

Maybe you can pass me the solution too?

Thanks!

Tags: None Add

Reply Quote Mark as Unread

Thread: Problem starting design_analyzer
Post: RE: Problem starting design_analyzer
Author: Gerard O'Leary
Posted Date: November 3, 2016 12:26 PM
Status: Published
Overall Rating:

Hi Genwen,

Are you still having this issue?

It should have been resolved for all the UG machines.

Thanks,
Gerard

Tags: None Add

Reply Quote Mark as Unread

Thread: DRC problem
Post: DRC problem
Author: Yi Wang
Posted Date: October 20, 2016 8:39 PM
Status: Published
Overall Rating:

I am running DRC for inverter. The problem shown that "need nohmic within 5um of PMOS/avdcap/pdiffR/plres", couldn't figure it out. I have 9 PMOS in parallel, 4 of them shown the problem mention before.

Same problem happened to my NMOS, "need pohmic within 5um of NMOS/ndiffR/nwellR/PNPvertical"

Tags: None Add

Reply Quote Mark as Unread

Thread: DRC problem
Post: RE: DRC problem
Author: **Minghua Zhao**
Posted Date: October 20, 2016 9:03 PM
Status: Published
Overall Rating:

This was asked before in another thread:

https://portal.utoronto.ca/webapps/discussionboard/do/message?action=list_messages&forum_id=_530951_1&nav=discussion_board_entry&conf_id=

Tags: None Add

Reply Quote Mark as Unread

Thread: DRC problem
Post: RE: DRC problem
Author: **Gerard O'Leary**
Posted Date: October 21, 2016 11:31 AM
Status: Published
Overall Rating:

Hi Yi,

Please see Xunjun's answer in the link above - check your P-substrate contacts.

Thanks,

Gerard

Tags: None Add

Reply Quote Mark as Unread

Thread: EDI - SOC Encounter problem
Post: EDI - SOC Encounter problem
Posted Date: October 29, 2016 5:24 PM
Status: Published

Author: Genwen Zhao Overall Rating:

Hi,

I was trying to set up EDI following the VLSI manual. But i am getting the following errors, and COULD not run the tool....

This version was compiled on Thu Jul 15 13:17:23 PDT 2010.
Set DBUPerIGU to 1000.
Set net toggle Scale Factor to 1.00
Set Shrink Factor to 1.00000
Encounter terminated by internal (SEGV) error/signal...
*** Stack trace in log file.

Any idea? Thanks

Tags: None Add

Reply Quote Mark as Unread

Thread: EDI - SOC Encounter problem Posted Date: November 3, 2016 11:44 AM
Post: RE: EDI - SOC Encounter problem Status: Published
Author: Gerard O'Leary Overall Rating:

Hi Genwen,

This is very strange. I was able to open encounter on ug250 with the following:

source /CMC/tools/CSHRCs/Cadence.SOC

encounter -nowin

However, there seems to be an issue with UG:

```
- 132 through 180
- 201 through 249
```

I'm trying to get this resolved now, but in the meantime ug250 and ug251 should work.

On which machine did you see the error above? I wasn't able to replicate it.

Thanks,

Gerard

Tags: None Add

Reply Quote Mark as Unread

Thread: EDI - SOC Encounter problem
Post: RE: EDI - SOC Encounter problem
Author: Genwen Zhao
Posted Date: November 3, 2016 1:25 PM
Status: Published
Overall Rating:

Hi Gerard,

I don't have the machine name, but the PCs in GB251 computer lab are running on the machine that has this problem. I hope you can find out which machine is with this information.

Someone around school can provide the information maybe?

Thanks.

Tags: None Add

Reply Quote Mark as Unread

Thread: Cannot find the IBM 0.13um Standard Cell Verilog file
Post: Cannot find the IBM 0.13um Standard Cell Verilog file
Author: Christos Konstantopoulos
Posted Date: October 31, 2016 11:53 AM
Status: Published
Overall Rating:

Hello everyone,

I cannot find the IBM 0.13um Standard Cell Verilog file in order to copy to the project working directory for Prj 3.How I can tackle this problem ?

With Regards,

Christos

Tags: None Add

Reply Quote Mark as Unread

Thread: Cannot find the IBM 0.13um Standard Cell Verilog file
Post: RE: Cannot find the IBM 0.13um Standard Cell Verilog file
Author: Genwen Zhao
Posted Date: October 31, 2016 11:58 AM
Status: Published
Overall Rating:

```
try this :   /CMC/kits/artisan-8rf/aci/sc-x.20090122/verilog/ibm13rfrvt.v
```

Tags: None Add

Reply Quote Mark as Unread

Thread:
How to get back cmos35p shortcuts for cmrf8sf
Post:
How to get back cmos35p shortcuts for cmrf8sf
Author: **Minghua Zhao**

Posted Date: November 9, 2016 9:07 PM
Status: Published
Overall Rating:

I was wondering if anyone knew their way around the shortcut definition for the cmrf8sf library

Tags: None Add

Reply Quote Mark as Read

Thread:
How to get back cmos35p shortcuts for cmrf8sf
Post:
RE: How to get back cmos35p shortcuts for cmrf8sf
Author: **Dhruv Patel**

Posted Date: November 9, 2016 10:36 PM
Status: Published
Overall Rating:

Hi Minghua Zhao,

You can add following line in .myalias file where this .myalias file must be sourced from .cshrc file. You can always add many more shortcut in .myalias file if you want.

alias r130 /CMC/kits/local/bin/startCds -t cmrf8sf

In detail:

1) create a ".myalias" file in your home directory (naming is not important)

2) add the following line in your '.myalias' file

alias run130 /CMC/kits/local/bin/startCds -t cmrf8sf

3) now in your .cshrc file add the following line and save.

source .myalias

4) To make your shortcut effective, re-source .cshrc file by typing following command in your terminal

source .cshrc

5) now go to your project directory (~/cmrf8sf/) and type the following shortcut command. The cadence with 0.13 kit should openup.

run130

Tags: None Add

Reply Quote Mark as Read

Thread: How to get back cmos35p shortcuts for cmrf8sf
Post: RE: How to get back cmos35p shortcuts for cmrf8sf
Author: **Minghua Zhao**

Posted Date: November 9, 2016 11:35 PM
Status: Published
Overall Rating:

Hi Dhruv,

Thanks for your answer, but what I actually meant was shorcuts like Ctr+e, or Shift+e for descending hierarchies. Sometimes the zooming (z key) also behaves differently in the cmrf8sf kit.

Maybe I wasn't too clear.

Cheers

Tags: None Add

Reply Quote Mark as Read

Thread: How to get back cmos35p shortcuts for cmrf8sf
Post: RE: How to get back cmos35p shortcuts for cmrf8sf
Author: **Tianxiang Chen**

Posted Date: November 10, 2016 11:28 AM
Status: Published
Overall Rating:

Hi,

What you need is a bindkeys file. You can google "cadence bindkeys" online and easily find one better than the cmos35 "shortcut" you used.

After you download the bindkeys file (ends in .il, assuming its name is xx.il), you put it in your cmrf8sf directory, and add " load("xx.il") " at the end of .cdsinit file.

The bindkeys downloaded might have some compatibility problems with 0.13um we are using now, but it could be fixed case by case.

Tianxiang

Tags: None Add

Reply Quote Mark as Read

Thread:
How to get back cmos35p shortcuts for cmrf8sf
Post:
RE: How to get back cmos35p shortcuts for cmrf8sf
Author: **Yifeng Zhang**

Posted Date: November 20, 2016 12:22 PM
Status: Published
Overall Rating:

Hi,

copy the following cmd to your icfb window and hit enter, now you should be able to get all the bindkeys you used to have in 0.35um technology in the new cmrf8sf

load(strcat(ibmPdkPath "cmrf8sf/rel/cdslib51/Skill/ibmPdkBindkeysCDS.il"))

Tags: None Add

Reply Quote Mark as Read

Thread:
Standard Cell Library for CMRF8SF - Schematic Simulation
Post:
Standard Cell Library for CMRF8SF - Schematic Simulation
Author: **Minghua Zhao**

Posted Date: November 12, 2016 5:05 PM
Status: Published
Overall Rating:

I have been trying to import synthesized verilog (using ncverilog) files to Cadence to no success.

It seems that whatever Standard Cell Libraries available for Cadence (as found on Jaro's notes /CMC/kits/artisan-8rf/==README.jaro) are only symbol views.

Symbol views can't be simulated with the Cadence Analog tools.

So my question is:

- How, and can we do "spice-style" simulations with our synthesized Verilog schematics?

Tags: None Add

Reply Quote Mark as Unread

Thread: Standard Cell Library for CMRF8SF - Schematic Simulation
Post: RE: Standard Cell Library for CMRF8SF - Schematic Simulation
Author: Gerard O'Leary

Posted Date: November 21, 2016 3:43 PM
Status: Published
Overall Rating:

Hi Minghua,

Please see my post here:
https://portal.utoronto.ca/webapps/discussionboard/do/message?action=list_messages&forum_id=_530949_1&nav=discussion_board_entry&conf_id

For the purposes of this project, if you show that you don't have any timing issues in Encounter, or issues with post-synthesis simulation in NC Verilog, this should be sufficient.

Thanks,

Gerard

Tags: None Add

Reply Quote Mark as Unread

Thread: Standard Cell Library for CMRF8SF - Schematic Simulation
Post: RE: Standard Cell Library for CMRF8SF - Schematic Simulation
Author: Minghua Zhao

Posted Date: November 28, 2016 11:07 PM
Status: Published
Overall Rating:

Thanks Gerard~

Tags: None Add

Reply Quote Mark as Read

Thread: Tutorial #6 - cannot open shared object file
Post: Tutorial #6 - cannot open shared object file
Author: Minghua Zhao

Posted Date: November 16, 2016 6:43 PM
Status: Published
Overall Rating:

Hi, I'm encountering a strange problem in Tutorial #6 setting up environment step.

Apparently a shared library called "libXp.so.6" is missing - see screen-shot.

Does anyone else encountered the same issue?

Thanks all

Attachment: Screen Shot 2016-11-16 at 18.41.55.png (65.123 KB)

Tags: None Add

Reply Quote Mark as Read

Thread: Tutorial #6 - cannot open shared object file
Post: RE: Tutorial #6 - cannot open shared object file
Author: **Navid Sarhangnejad**

Posted Date: November 18, 2016 9:22 AM
Status: Published
Overall Rating:

Hi Minghua,

Could you please upload the source file you created, probably MSinit

Thanks,

Navid

Tags: None Add

Reply Quote Mark as Read

Thread: Tutorial #6 - cannot open shared object file
Post: RE: Tutorial #6 - cannot open shared object file
Author: **Minghua Zhao**

Posted Date: November 19, 2016 12:11 AM
Status: Published
Overall Rating:

Yup

Attachment: MSinit (184 B)

Tags: None Add

Reply Quote Mark as Read

Thread: Tutorial #6 - cannot open shared object file
Post: RE: Tutorial #6 - cannot open shared object file
Author: Minghua Zhao
Posted Date: November 19, 2016 12:11 AM
Status: Published
Overall Rating:

cds.lib too

Attachment: cds.lib (506 B)

Tags: None Add

Reply Quote Mark as Read

Thread: Tutorial #6 - cannot open shared object file
Post: RE: Tutorial #6 - cannot open shared object file
Author: Jaimin Joshi
Posted Date: November 19, 2016 6:33 PM
Status: Published
Overall Rating:

Try SSH into ug250 or 251 and execute the same sequence of commands. Solved the same problem for me.

Jaimin

Tags: None Add

Reply Quote Mark as Read

Thread: Tutorial #6 - cannot open shared object file
Post: RE: Tutorial #6 - cannot open shared object file
Author: Navid Sarhangnejad
Posted Date: November 21, 2016 10:55 AM
Status: Published
Overall Rating:

Thanks Jaimin,

Minghua, could you please confirm if this work around solves your problem?

Navid

Tags: None Add

Reply Quote Mark as Read

Thread:
CMRF8SF -- No valid layers in LSW
Post:
CMRF8SF -- No valid layers in LSW
Author: Shengze Gao

Posted Date: November 19, 2016 3:16 PM
Status: Published
Overall Rating:

Hello,

When I try to layout the final project using CMRF8SF technology, I find there is NO Valid Layers in LSW. There are three warnings when opening Virtuoso.

Can someone help me, please?

Thanks a lot,

Shengze

Attachment: No_valid_layer_purpose_pairs.png (38.596 KB)

Tags: None Add

Reply Quote Mark as Read

Thread:
CMRF8SF -- No valid layers in LSW
Post:
RE: CMRF8SF -- No valid layers in LSW
Author: Yifeng Zhang

Posted Date: November 20, 2016 12:12 PM
Status: Published
Overall Rating:

Hi,

you can try this, Edit -> Set Valid Layers... -> click "All Valid" in the popup window -> click OK. now you should have all layers

Thanks

Rudy

Tags: None Add

Reply Quote Mark as Read

Thread:

Posted Date: November 21, 2016 1:05 PM

Thread: CMRF8SF -- No valid layers in LSW
Post: RE: CMRF8SF -- No valid layers in LSW
Author: **Shengze Gao**

Status: Published
Overall Rating:

Hi, It turns out I forgot setting cmrf8sf as the technology when creating a new library. Thanks a lot though. Shengze

Tags: None Add

Reply Quote Mark as Read

Thread: CMRF8SF -- No valid layers in LSW
Post: RE: CMRF8SF -- No valid layers in LSW
Author: **Navid Sarhangnejad**

Posted Date: November 21, 2016 11:04 AM
Status: Published
Overall Rating:

Hi Shengze,

It looks like you either have not setup your tools properly, or you don't have proper access to the technology!

If you can come to the office hour today, we will have a look to it together.

Navid

Tags: None Add

Reply Quote Mark as Read

Thread: CMRF8SF -- No valid layers in LSW
Post: RE: CMRF8SF -- No valid layers in LSW
Author: **Shengze Gao**

Posted Date: November 21, 2016 1:10 PM
Status: Published
Overall Rating:

Hi Navid,

It was solved. I forgot to set cmrf8sf as the technology when creating a new library.

Thanks a lot though,

Shengze

Tags: None Add

Reply Quote Mark as Read

Thread:
How to importing synthesized verilog with ibm13rfrvt.v?
Post:
How to importing synthesized verilog with ibm13rfrvt.v?
Author: Dhruv Patel

Posted Date: November 19, 2016 7:12 PM
Edited Date: November 19, 2016 7:18 PM
Status: Published
Overall Rating:

Dear All,

I was successfully able to run AMS (mixed signal simulations) by importing multiplier verilog (unsynthesized) from project 3 to just familiarize myself with the flow mentioned in "TUT06 - Mixed signal simulations.pdf". Simulation waveforms worked as expected.

Later, when I tried importing the multiplier_syn.v (synthesized verilog code), the import log showed up with bunch of low level blocks (i.e OA21XLTF, AOI22X1TF ...) missing in my libraries which are specified in ibm13rfrvt.v verilog file.

So then I decided to import ibm13rfrvt.v verilog code in cadence so that I can have those missing low level cell views available in cadence. When I imported ibmrf13rvt.v (fig 1) file, it created all the cell view blocks which are in the ibm13rfrvt.v file as verilog modules BUT it just created the symbol views (nothing like functional or schematic or verilog views which are useful for simulations, see fig 2). Then when I re-tried to import my multiplier_syn.v (synthesized verilog) it showed me following errors in import log (fig 3, fig 4).

The main question is that is there a library containing verilogams or functional blocks that are inside ibmrf13rvt.v file so that we can simulate synthesized verilog code?

Attachment: ams simulation import.tar.gz (154.161 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread:
How to importing synthesized verilog with ibm13rfrvt.v?
Post:
RE: How to importing synthesized verilog with ibm13rfrvt.v?
Author: Jaimin Joshi

Posted Date: November 19, 2016 8:34 PM
Status: Published
Overall Rating:

I'm having the same problem. Anyone found a solution to this yet?

Tags: None Add

Reply Quote Mark as Unread

Thread:
How to importing synthesized verilog with ibm13rfrvt.v?
Post:
RE: How to importing synthesized verilog with ibm13rfrvt.v?
Author: **Minghua Zhao**

Posted Date: November 19, 2016 11:03 PM
Status: Published
Overall Rating:

That's the same problem I had.

I posted an inquiry in a different thread, but had no answer for a while.
https://portal.utoronto.ca/webapps/discussionboard/do/message?action=list_messages&forum_id=_530949_1&nav=discussion_board_entry&conf_id=

From Jaro's notes, it looks as if the standard cell libraries for the 13um technology is incomplete.

Or, as he puts it "only suited to run HDL simulations and not spice-level" (I'm paraphrasing)

Cheers

Tags: None Add

Reply Quote Mark as Unread

Thread:
How to importing synthesized verilog with ibm13rfrvt.v?
Post:
RE: How to importing synthesized verilog with ibm13rfrvt.v?
Author: **Dhruv Patel**

Posted Date: November 20, 2016 2:19 PM
Status: Published
Overall Rating:

From /CMC/kits/cmrf8sf/==README.jaro file, Jaro mentions to go to the /CMC/kits/artisan-8rf/==README.jaro file and in that file he mentions to import following library lines in CMRF8SF/cds.lib file (these should have cds_Sch blackbox schematic view):

---------- snip here ----
-- I/O libraries

DEFINE iogpil_cmrf8sf_rvt /CMC/kits/artisan-8rf/aci/io/symbols/dfII/iogpil_cmrf8sf_rvt
DEFINE iogpst_cmrf8sf_rvt /CMC/kits/artisan-8rf/aci/io/symbols/dfII/iogpst_cmrf8sf_rvt
-- standard-cell libraries
DEFINE ibm13rflpvt /CMC/kits/artisan-8rf/aci/sc-x/symbols/cadence/ibm13rflpvt
DEFINE ibm13rfrvt /CMC/kits/artisan-8rf/aci/sc-x/symbols/cadence/ibm13rfrvt
---------- snip here ----

The problem is that those libraries still don't have their their blackbox verilog or verilogams in them. So you won't be able to simulate them functionally. I tried to simulate it and the simulation runs without errors but the functionality isn't reflected. Those blocks would be just there as a dead.

Tags: None Add

Reply Quote Mark as Unread

Thread: How to importing synthesized verilog with ibm13rfrvt.v?
Post: RE: How to importing synthesized verilog with ibm13rfrvt.v?
Author: **Minghua Zhao**

Posted Date: November 20, 2016 2:04 PM
Status: Published
Overall Rating:

I just wanted to add to this.

The synthesized blocks won't pass DRC since the cells are only symbols.

Attachment: Screen Shot 2016-11-20 at 14.00.12.png (145.182 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread: How to importing synthesized verilog with ibm13rfrvt.v?
Post: RE: How to importing synthesized verilog with ibm13rfrvt.v?
Author: **Dhruv Patel**

Posted Date: November 20, 2016 2:22 PM
Status: Published
Overall Rating:

Hi Minghua Zhao,

Did you get the simulations functioning correctly after importing those blackbox libraries? My simulation works without errors but those blackbox blocks are just there as dead, so functionality wise its not working for me.

- Dhruv

Tags: None Add

Reply Quote Mark as Unread

Thread:
How to importing synthesized verilog with ibm13rfrvt.v?
Post:
RE: How to importing synthesized verilog with ibm13rfrvt.v?
Author: **Minghua Zhao**

Posted Date: November 20, 2016 4:12 PM
Status: Published
Overall Rating:

No, I never got simulations results either.

Tags: None Add

Reply Quote Mark as Unread

Thread:
How to importing synthesized verilog with ibm13rfrvt.v?
Post:
RE: How to importing synthesized verilog with ibm13rfrvt.v?
Author: **Gerard O'Leary**

Posted Date: November 21, 2016 3:27 PM
Status: Published
Overall Rating:

Hi all,

Just to confirm - you don't need to perform full functional verification within Virtuoso. Once you've verified your analog and digital components separately (using test vectors generated by your digital simulations), this should be sufficient.

Thanks,

Gerard

Tags: None Add

Reply Quote Mark as Unread

Thread:	ERC errors	**Posted Date:**	November 22, 2016 5:10 PM
Post:	ERC errors	**Status:**	Published
Author:	Tianxiang Chen	**Overall Rating:**	

Hi,

I asked this question in today's lecture.

I am using ibm 0.13um for the project. I have my part DRC and LVS clean but have a lot of ERC errors.

Unlike LVS, ERC doesn't show the errors in detail, the only thing I can do is click on each error and it will show me where the problem is, without any explanation. The errors exist on a lot of contacts and poly.

I followed the way I did the layout in 0.35um. Is there something special for 0.13um? Or is there a way I can see what caused the errors?

Thank you.

Tianxiang

Attachment: Picture1.jpg (70.662 KB)

Tags: None Add

Reply Quote Mark as Read

Thread:	LVS BOX and EXCLUDE CELL	**Posted Date:**	December 1, 2016 8:59 AM
Post:	LVS BOX and EXCLUDE CELL	**Status:**	Published
Author:	Genwen Zhao	**Overall Rating:**	

Hi,

I am a bit confused on how to use LVS BOX and EXCLUDE CELL to get lvs clean for netlist exported from encounter.

So now the problem is that we are missing layout/schematic for 0.13 IBM standard cell library. My understanding is that LVS BOX and EXCLUDE CELL are some commands from Mentor Grapgics Calibre tool that we can use to kinda "skip" the standard cells while checking top level connections.

Ok... Question : while we are expecting to use Cadence Virtuoso to read in the def , netlist (or stream in GDS), and run LVS check, how do we use commands from Mentor Graphics ?? They are different tools. How do we get them to work !??? Maybe I misunderstood something here ?! Anyone has any ideas?

Thanks,

Genwen

Tags: None Add

Reply Quote Mark as Unread

Thread: LVS BOX and EXCLUDE CELL
Post: RE: LVS BOX and EXCLUDE CELL
Author: Navid Sarhangnejad
Posted Date: December 1, 2016 9:41 AM
Status: Published
Overall Rating:

Hi Genwen,

You have to use calibre tools for LVS and DRC, which are from Mentor Graphics.

As an example, in the LVS window you have to go to LVS options (first enable it through the setup menu) and in the include tabs you have to put the commands in the Include SVRF Commands box. Then you can run the LVS.

One more point, you should do the LVS BOX / EXCLUDE CELL for your top level cell (the one exported from encounter). I mean you don't need to write the commands for every standard cell in your design.

Good luck,

Navid

Tags: None Add

Reply Quote Mark as Unread

Thread: LVS BOX and EXCLUDE CELL
Post: RE: LVS BOX and EXCLUDE CELL
Author: Genwen Zhao
Posted Date: December 2, 2016 9:35 AM
Status: Published
Overall Rating:

Hi Navid,

Thanks for the information.

Is there any library/setup we need for calibre ? like what we do for Synopsys/Cadence tools ?

Also, can you provide a command line on how to start the calibre tool? I barely used the tool before..

Thanks!

Genwen

Tags: None Add

Reply Quote Mark as Unread

Thread: LVS BOX and EXCLUDE CELL
Post: RE: LVS BOX and EXCLUDE CELL
Author: Navid Sarhangnejad
Posted Date: December 2, 2016 11:37 AM
Status: Published
Overall Rating:

Please read /CMC/kits/cmrf8sf/ ==README.jaro.hints for instructions on how to use them. I had pointed to read these document in the "Simulations on 0.13um technology and a few hints" announcement.

Tags: None Add

Reply Quote Mark as Unread

Thread: problem opening VIrtuoso AMS environment
Post: problem opening VIrtuoso AMS environment
Author: Yifeng Zhang
Posted Date: December 8, 2016 11:07 PM
Status: Published
Overall Rating:

Hi,

I am having problem starting cadence by following the steps in TUT06. it gives me the following errors:

/CMC/tools/cadence/IC.5141.USR5.linux/tools/dfII/bin/32bit/icms.exe: error while loading shared libraries: libXp.so.6: cannot open shared object file: No such file or directory

[1] Exit 127 icms

I check that I do have access to /CMC/tools/cadence/IC.5141.USR5.linux/tools/dfII/bin/32bit/icms.exe. so I am confused now.

Anyone else has this problem??

Thanks

Yifeng

Tags: None Add

Reply Quote Mark as Read

Thread:
problem opening Cadence Virtuoso with 0.13nm library
Post:
problem opening Cadence Virtuoso with 0.13nm library
Author: **Genwen Zhao**

Posted Date: December 9, 2016 11:55 AM
Status: Published
Overall Rating:

Hi all,

I am having some errors when loading the cadence virtuoso with cmrf8 library .. I am sure it worked fine for me before.. so not sure what happend..

I logged into ug250 machine with shh VNC.

Please see the picture for error and provide feedback/solution if you had the same problem before.

Thanks,

Genwen

Attachment: Capture.JPG (20.378 KB)

Tags: None Add

Reply Quote Mark as Unread

Thread:
problem opening Cadence Virtuoso with 0.13nm library
Post:
RE: problem opening Cadence Virtuoso with 0.13nm library
Author: **Navid Sarhangnejad**

Posted Date: December 9, 2016 2:35 PM
Status: Published
Overall Rating:

Hi Genwen,

I guess the problem is from the options you use for starting the vncserver. You have to use proper settings, as an example "-depth 24" for your vncserver command.

Cheers,

Navid

Tags: None Add

Reply Quote Mark as Unread

Thread:
problem opening Cadence Virtuoso with 0.13nm library

Post:
RE: problem opening Cadence Virtuoso with 0.13nm library

Author: **Genwen Zhao**

Posted Date: December 10, 2016 1:02 PM
Status: Published
Overall Rating:

Thanks Navid , it solved my problem! :)

Tags: None Add

Reply Quote Mark as Read

Select: All None
Mark Tag Text: Add

← OK