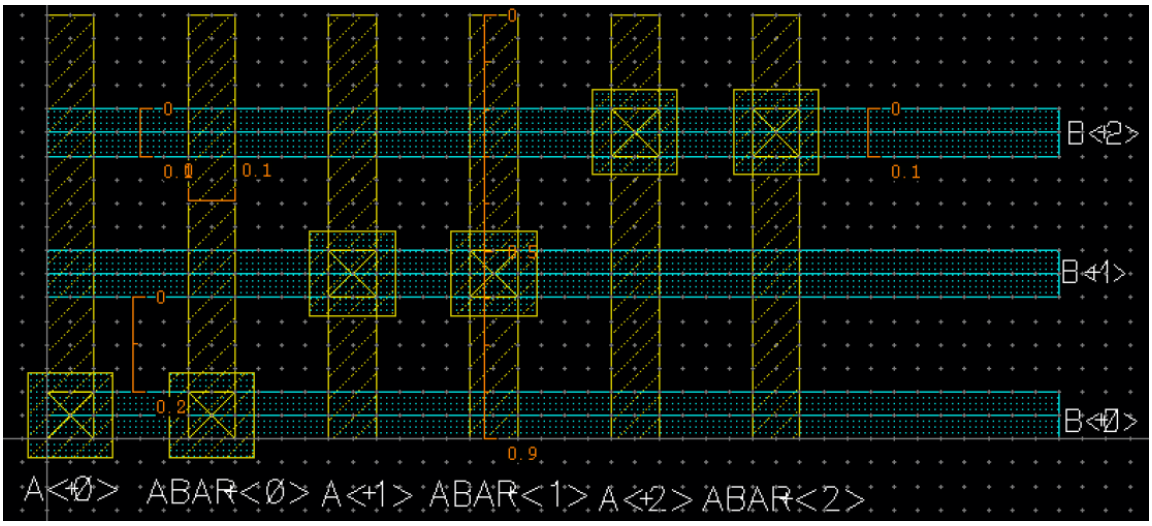
PCell tutorial supplement - ECE1388

3:8 Decoder Address bus connections using PCell

Repetition of layout pattern

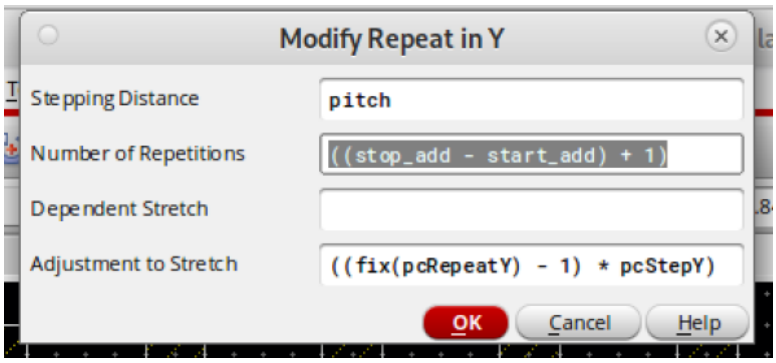
1. The first step is to make the general repetitive pattern of the decoder address bus in a New layout-view, as shown below:



2. To launch PCell tool in virtusoso:

   Launch → Plugins → Select “PCell”

3. Select all the M1, M2 lines and M1-M2 via (from above figure) and then From the toolbars above select ⇒ PCell → Repetition → Repeat in Y



pitch: User defined variable. Would be used to define the distance after which the layout pattern would be repeated

4. Save the Layout and then compile PCell using PCell → Compile → ToPCell (Select transistor from pop-up in case user compiling for the first time)
5. Check CIW window for “Compilation complete” message

Conditional Inclusion:

Now to connect the VIAs to proper logical connection , conditional Inclusion feature of PCell is helpful. We know the LSB, A<0> or ABAR<0> VIA connection repeats every alternate repetition of PCell.

Similarly we also know A<1>,ABAR<1> VIA repeats after 2^1 repetition and A<2>, ABAR<2> repeats after 2^2.

To implement this, you can following method:

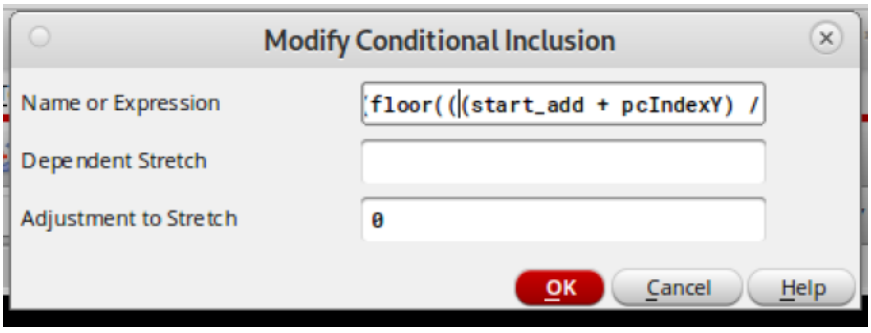
1. Select M1-M2 VIA on A<0> net
2. PCell → Conditional Inclusion → Define

   Name or Expression: **(mod(floor(((start_add + pcIndexY) / 1)) 2) == 1)**

   Please note:

   pcIndexY: Internal Skill parameter which tracks indexes in case of repetitions

   start_add : User defined Skill parameter for start Address (User must add these parameters during step-3 of “**Repetition of layout pattern**”)



3. Save the layout and Compile. Then confirm if the it is successful.

4. Similarly for VIAs on ABAR<0>, A<1>, ABAR<1>, A<2>, ABAR<2> you need to add Conditional Exclusions and compile after defining the every conditional inclusions.
5. Some of the expressions for A<0>, A<1> and A<2> are mentioned below for reference

VIA ABAR<0>

Name or Expression: **(mod(floor(((start_add + pcIndexY) / 1)) 2) == 0)**

VIA A<1>

Name or Expression: **(mod(floor(((start_add + pcIndexY) / 2)) 2) == 1)**

VIA ABAR<1>

Name or Expression: **(mod(floor(((start_add + pcIndexY) / 2)) 2) == 0)**

VIA A<2>

Name or Expression: **(mod(floor(((start_add + pcIndexY) / 4)) 2) == 1)**

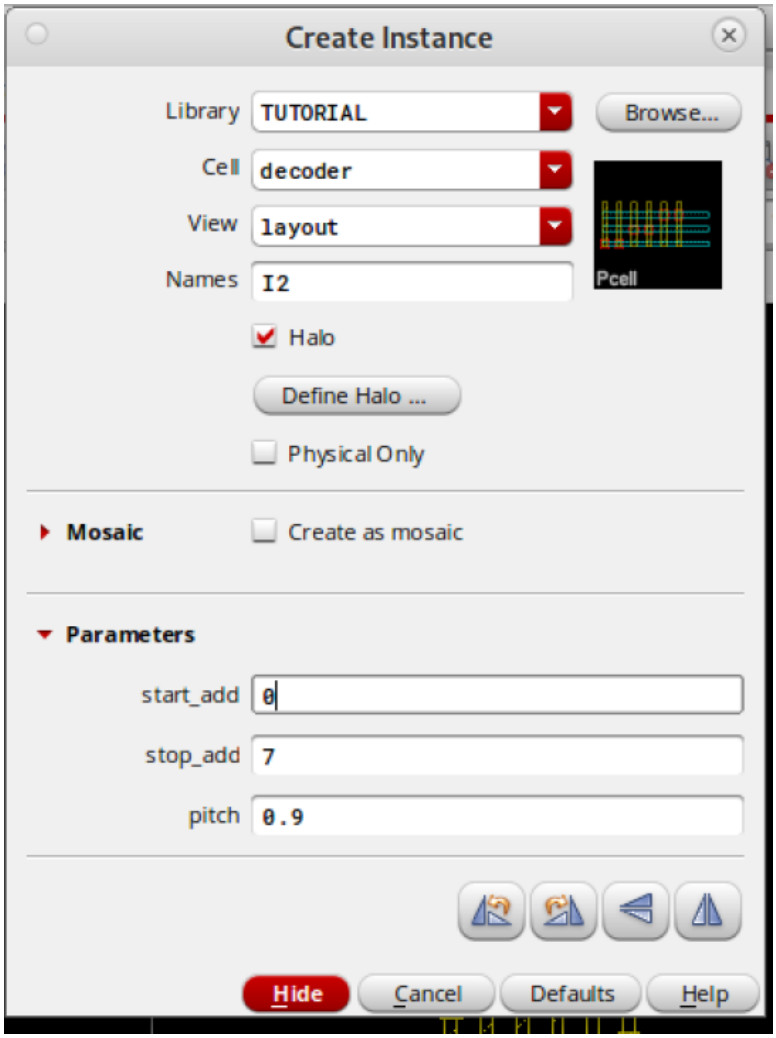
VIA ABAR<2>

Name or Expression: **(mod(floor(((start_add + pcIndexY) / 4)) 2) == 0)**

6. Save the Layout view.

Final outcome is shown below:

1. Open a new layout view.
2. Instantiate the PCell



3:8 Decoder address side connections: