ECE1388 – TUT02 – Cadence Layout Tutorial

This tutorial is helping you regarding the Virtuoso Layout Editor in Cadence. Described items are:

- Setting User Preferences
- Layout Tips
- Layer Select Window applications
- General Layout Rules
- Layout tips for Matching
- Layout tips for Noise Isolation
- Hotkeys
- Layout techniques for matching

Setting User preferences

- ✓ The user preferences form described in TUT01, applies to layout as well.
- ✓ In a layout window, the hotkey '*e*' will open the Display Options window. You can:
  - Enable 'Pin Names'
    - If you do not use this feature, you won't see the pin names in your layout and every time you need to check the properties.
  - Enable 'Cross Cursor'
    - This helps to align different cells in your layout.
  - Display levels:
    - In a hierarchical design, you can select what levels of hierarchy should be shown.
  - Change the grid:
    - In cmosp35 technology, the minimum is 0.05 and your grid should be an integer multiple of your minimum grid. Do not ever use other values, otherwise you'll get DRC "off-grid" errors. And other technologies has their own minimum grid
- ✓ In a layout window, the hotkey 'E' will open the Layout Editor Options window. You can:
  - 'Repeat Commands':
    - If disabled, you should select your command every time.
  - 'Gravity On':
    - If enabled, your pointer is automatically pulled towards the selected 'Types'.
    - 'Aperture' determines how far from the pointer the gravity function works.

Layout Tips

- ✓ Always be careful about your "Caps Lock" key. It is considered as holding down the Shift key when using the hotkeys!
- ✓ Use hierarchical instantiation as much as possible, and preferably the same hierarchy as in your schematic.
- ✓ Instantiate "Mosaic" instance when you need multiple of the same cell with regular pitch.
- ✓ Use multiple rows and column for your substrate contacts where ever possible. It helps having a more uniformly biased substrate.

LSW – Layer Select Window

In this window, you can find the available layers for the chosen technology. This window opens when you open a layout window and has the following functionalities:

- ✓ AV – All visible
  - o By clicking on it, all the layers will be shown.
- ✓ NV – Non visible
  - o It makes all the layers hidden, except the currently selected one.
- ✓ AS – All selectable
  - o You can select all the available layers in your layout window.
- ✓ NS – Non selectable
  - o You can't select any of the layers in the layout window
- ✓ Inst - Instance
  - o If deselected, you cannot select any of the blocks in your layout window.
- ✓ Pin – Pin
  - o If deselected, you cannot select any of the pins in your layout.
- ✓ You can change the visibility of each layer individually by the middle button of your mouse.
- ✓ You can change the "selectability" of each individual layer by the right mouse button.

General Layout Rules

- ✓ Use double(multiple)-vias when you have room. Especially in big circuits, that helps to improve yield in final products!
- ✓ Don't overlap long wires → prevent capacitive coupling
- ✓ For long interconnects, use larger than (at least 50%) minimum width and spacing. Larger width helps reducing open circuits and larger spacing lowers the chance for shorts between different lines. In fact knowing whether the technology of use is optimized for short circuits or open circuits, you can use the minimum size for either the width or the spacing.
- ✓ If the parasitic cap of the line is important:
  - o Run the parallel lines with large spacing
  - o Use adjacent metal layers perpendicularly
  - o And always check the extracted simulation
- ✓ Never underestimate the resistance of long interconnect lines. It can increase the time-constant of the node and consequently lower your speed. The resistance depends on the thickness of the metal, but 1mm of minimum sized line can have a resistance of several hundreds of Ohm.

Layout tips for matching

- ✓ Only use 90 degree angles
- ✓ All transistors that need matching should be in the same direction, don't have them perpendicular to each other

- ✓ Wide transistors are very susceptible to process variation, so better to average the effects of the gradient by spreading the width out → we achieve this by fingering the transistor and interdigitating the gates
- ✓ Use dummy circuits (transistors, capacitors or resistor units) around your components.

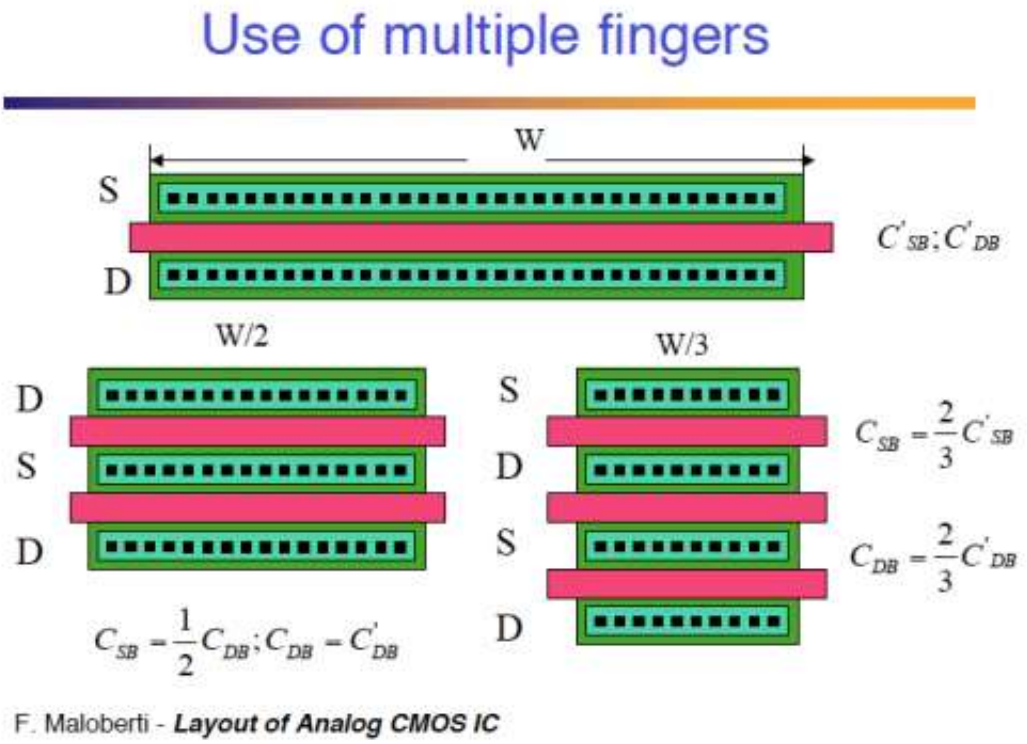
Layout tips for Noise Isolation

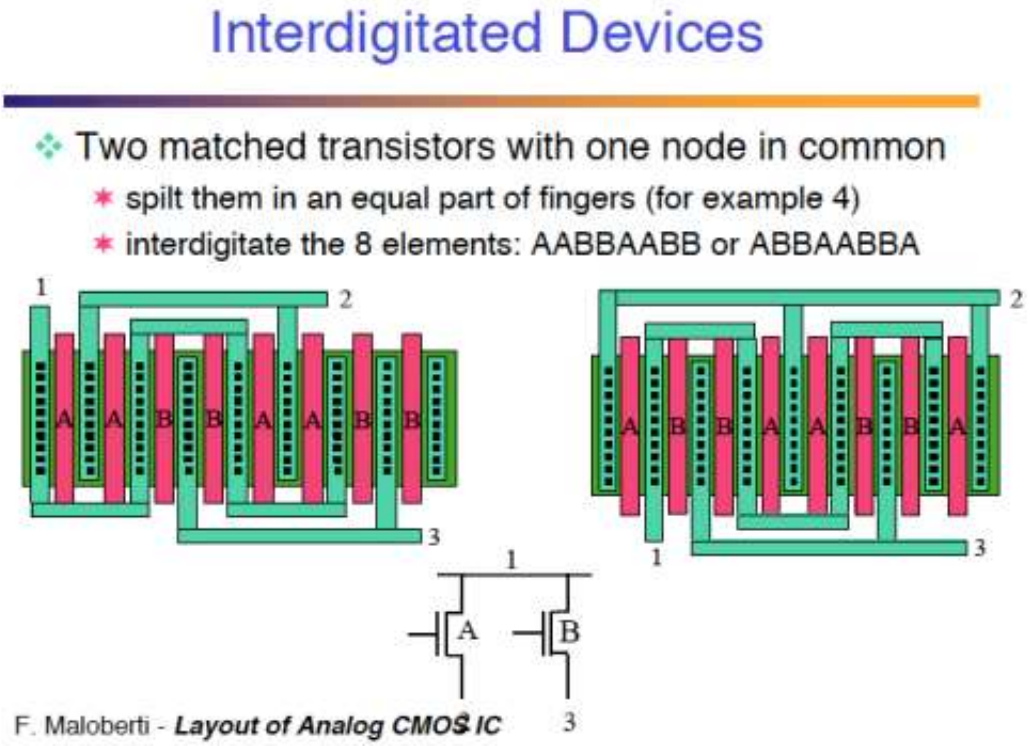
- ✓ Separate noisy digital circuitry from sensitive analog circuitry
- ✓ Use noise isolation ring → substrate ring, n-well ring, substrate ring
- ✓ Put substrate rings around all analog circuits

Hotkeys for Layout

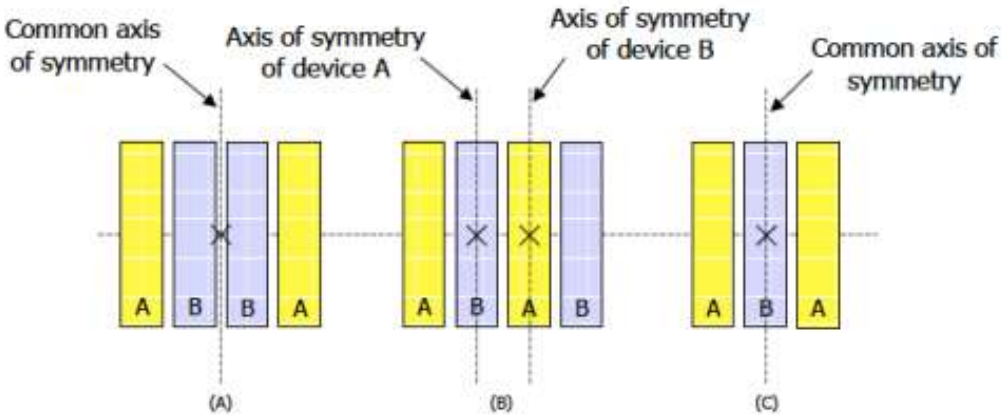
- ✓ ESC: cancels the current command.
- ✓ F3: opens the options window for the current command.
- ✓ u: undo
- ✓ ctrl + z: zoom in
  - Or zoom in to a small portion by drawing a box with right mouse button
- ✓ Z: zoom out
  - Or hold shift and draw a box with right mouse button
- ✓ r: draw rectangle
- ✓ s: stretch the edge of an item
- ✓ m: move and item
- ✓ M: merge multiple geometries in the same layer
- ✓ t: tap to a new layer by left click mouse on that layer in your layout window
- ✓ …

Layout Techniques for matching:





Axis of Symmetries



F. Maloberti - ***Layout of Analog CMOS IC***

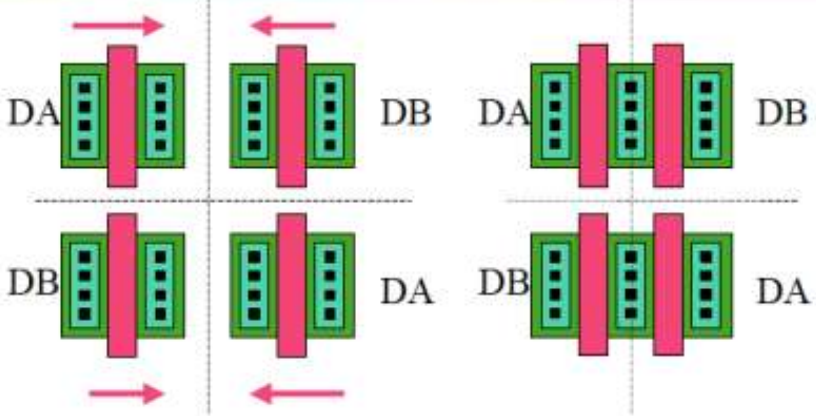
Interdigitiation Patterns

A	AA	AAA	AAAA
AB*	ABBA	ABBAAB*	ABABBABA
ABC*	ABCCBA	ABCBACBCA*	ABCABCCBACBA
ABCD*	ABCDDCBA	ABCBCADBCDA*	ABCDDCBAABCDDCBA
ABA	ABAABA	ABAABAABA	ABAABAABAABA
ABABA	ABABAABABA	ABABAABABAABABA	ABABAABABAABABAABABA
AABA*	AABAABAA	AABAAABAAABA*	AABAABAAAABAABAA
AABAA	AABAAAABAA	AABAAAABAAAABAA	AABAAAABAAAABAAAABAA

Note: not all the patterns permit a stacked layout

F. Maloberti - ***Layout of Analog CMOS IC***

Common Centroid



- Gradients in features are compensated for (at first approximation)
  - metal and poly interconnections are more complex

F. Maloberti - ***Layout of Analog CMOS IC***

Common Centroid Patterns

ABBA BAAB	ABBAABBA BAABBAAB	ABBAABBA BAABBAAB ABBAABBA	ABBAABBA BAABBAAB BAABBAAB ABBAABBA
ABA BAB	ABAABA BABBAB	ABAABA BABBAB ABAABA	ABAABAABA BABBABBAB BABBABBAB ABAABAABA
ABCCBA CBAABC	ABCCBAABC CBAABCCBA	ABCCBAABC CBAABCCBA ABCCBAABC	ABCCBAABC CBAABCCBA CBAABCCBA ABCCBAABC
AAB BAA	AABBAA BAAAAB	AABBAA BAAAAB AABBAA	AABBAA BAAAAB BAAAAB AABBAA

F. Maloberti - ***Layout of Analog CMOS IC***