Neol Solanki

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Industrial experience as **FPGA intern** and **ASIC clock intern**. Actively exploring full-time opportunities to leverage my skills for semiconductor industry benefaction. Proficiency in **FPGA, RTL, SoC**, **ASIC** design and verification.

SKILLS:

- **Programming skills**: Verilog, System Verilog, C, C++, Assembly, Perl
- **Design Concepts**: Static Timing Analysis, Finite State Machine, Network on Chip (NoC)
- **Tools**: Synopsys VCS, Synopsys Primetime, Cadence Xcelium, ModelSim, Matlab, Simulink, Vivado, Vivado HLS
- **Protocol:** AHB, APB
- **Universal Verification Methodology:** Assertions, Constrained Randomization

EXPERIENCE:

ASIC Clocks Intern | NVIDIA Corporation May 2022 – Aug 2022

- Worked on **clock methodology** and **optimized existing APIs with C++, Perl** reducing **time complexity and space complexity to O (1)** that can perform **Fan-in, Fan-out** of any given pin at the **large scale**
- **Validated** the same **APIs** by **building Quality Assurance test** in **C++, Perl** covering different possible scenarios and edge cases
- **Fixed bug** by building **centralized robust Perl script** using **regular expressions** leading to **75% decline in maintenance** for IP-DV teams

FPGA Intern | Sodick America Corporation Jan 2022 – May 2022

- **Developed and debugged C code from scratch** for **data protection** in the Serial Peripheral Interface (SPI) memory interfaced through **Advanced Peripheral Bus (APB)** with RISC processor
- **Verified the SPI memory opcodes** through digital oscilloscope by inspecting **waveforms in Logic Pro Software** on **Micro-Semi FPGA** Platform

PROJECTS:

ASIC design of Binary Phase shift key decoder with Verilog April 2022 – May 2022

- **Designed Costas loop** along with **43 tap Finite Impulse Response filter (sine and cosine)** including **Numerically Controlled Oscillator (NCO)** running on **200 MHz frequency**
- **Constructed match filter** with sampling rate **2.5 cycles/bit** to synchronize cosine filter's outcome according to phase of upcoming ADC signal using **correlation**

Synthesizable SoC design of Neural Network Evaluation engine based on System Verilog Aug 2021 – December 2021

- Built **accumulator** along with synopsis's **design ware 3 stage pipelined multiplier** to process data and weights from **external 2-clock cycle memory** with **4.8 Gops/sec rate**
- **Resolved the interfered latches** by ensuring the **precise initialization in Finite State Machine** as well as **solved negative slack** by pipelining the **multiplier from 3 stage to 7 stage** to reach **300 MHz operational frequency**
- **Created Arbiter** to accommodate **4 neural engine devices** along with **Network on Chip (NoC) interface**

YAPP router RTL architecture validation based on Universal Verification Methodology July 2021 – December 2021

- **Wrote test plan** with **5 UVCs such as clock and reset UVC, HBUS protocol UVC for control signal generation** and 3 output channel UVC and generated **10 different multichannel random and directed sequences** to the test-bench
- **Verified the router behavior** by building scoreboard using **Transaction-Level Modeling analysis FIFOs** as well as implemented simple **functional coverage model**

EDUCATION:

Master of Science in Electrical Engineering | *San Jose State University* | GPA: 3.7 / 4 December 2022

Bachelor of Technology in Electronics Engineering | *Birla Vishwakarma Mahavidyalaya* | GPA: 7.6 / 10 July 2020

PUBLICATION:

- **Performance Analysis of SoC and Hardware Design Flow in Medical Image Processing Using Xilinx Zed Board FPGA**
- **Analysis of Edge detection using Zynq based SoC FPGA**

CERTIFICATIONS:

- **SystemVerilog** for Design and Verification (Cadence Design Systems)
- SystemVerilog Accelerated Verification with **UVM** (Cadence Design Systems)
- Hardware Modeling using **Verilog** (NPTEL)