ECE455 - Lab1

Ghanan Gowripalan

20461804

[ggowripa@uwaterloo.ca](mailto:ggowripa@uwaterloo.ca)

**Accuracy:** When comparing the accuracy of the two approaches (for-loop vs interrupts), the clock implemented with the timer interrupts was more accurate. The clock with the interrupt performed exactly the same as an iPhone’s stopwatch app. The for-loop method was very close, however it seemed to be just slightly slower (after 10 minutes, there was an offset of < 1 second where the for-loop clock was lagging behind). Finding the correct value for the for-loop to create a 1 ms offset proved to be difficult as it took a lot of trial and error and multiple iterations.

**For-Loop Details:** For the for-loop implementation, a for-loop was created to loop (and do nothing in the loop) 24854 times to create a delay of approximately 1 ms. This for-loop was nested in another for-loop that would loop for X times, where X is the desired delay time in milliseconds. For the purpose of this lab, X was set to 1000. The value 24854 was determined by first setting the value to 25000 and letting the timer run for 10 minutes, while comparing it with an iPhone stopwatch app. After 10 minutes, it was found that the clock was slow by 3-4 (after running a few trials, average of 3.5 s offset was calculated). With this, the following formula was used to approximate for a better value for the internal for-loop.

Current\_value \* (10\_minutes\_in\_seconds - offset) = better\_value \* 10\_minutes\_in\_seconds

With Current\_value = 25000, offset = 3.5, and 10\_minutes\_in\_seconds = 600, better value was determined to be 24854. This value now gave an offset of < 1 second.

**Interrupt Details:** For the interrupt implementation, a match value of 25000000 was determined to create a tick every 1 second. This was calculated as follows:

The frequency of the clock being used is 12 MHz (F = 12000000 Hz)

The PLL0 multiplies this frequency by 100 (M = 100)

The PLL0 divides this frequency by 6 (N = 6)

With this, we can determine the PLL0 frequency by the following formula:

PLL0\_FREQ = 2 \* M \* F / N = 400000000 Hz

With this we can determine the CPU Clock frequency. We know from the configuration wizard that the CPU Clock frequency is equal to:

CPU\_FREQ = PLL0\_FREQ / 4 = 100000000 Hz

With this we can determine the TIMER0 Clock frequency. We know from the configuration wizard that the TIMER0 Clock frequency is equal to

PCLK\_TIMER0 = CPU\_FREQ / 4 = 25000000 Hz

Now we know that the clock at TIMER0 has a frequency of 25000000 Hz. This means, the match value should be 25000000 as in every cycle, the counter increments by 1, and after 25000000 cycles (exactly 1 second), the timer counter is equal to 25000000. At this point, an interrupt should be requested.