National University of Computer & Emerging Sciences – FAST Peshawar Campus

Assignment of DLD LAB

- ***Subject:*** *DLD Lab Assignment*
- ***Instructor:*** *Mam Anum Rashad*
- ***Written By:*** *Abdul Ghani Khan*
- ***Roll No:*** *22P-9037*
- ***Department:*** *Computer Science*
- ***Section:*** *BS(CS)-2A2*

Submit By

Abdul Ghani Khan

_____

Submit To

Mam Anum Rashad

_____

Question#1

Illustrate the block diagram of 8x1 Multiplexer using 4x1 and 2x1 Multiplexers. Simulate this

design in Multisim to verify the working of these cascaded multiplexers.

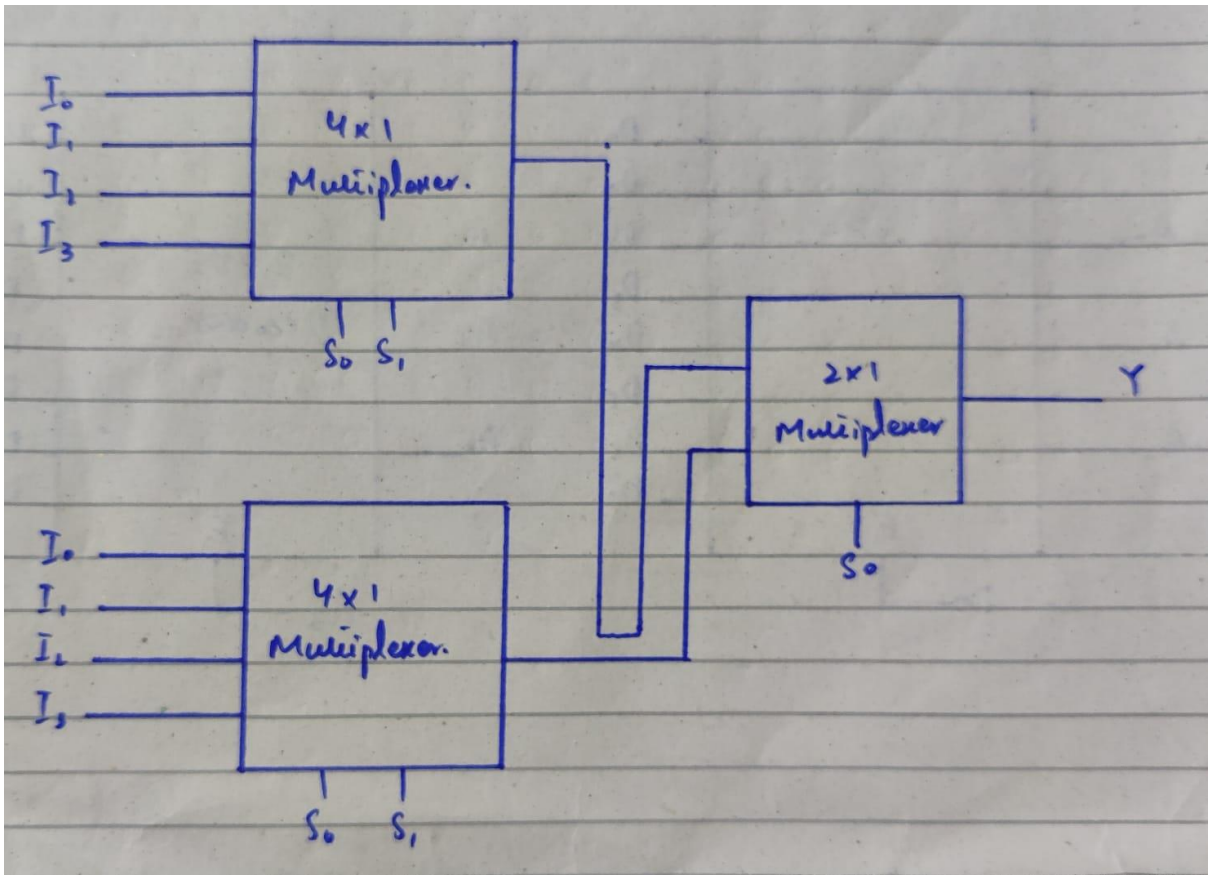
Also, create the truth table for 8x1 Multiplexer.

Simulation File Of Multi Sim Attached in the folder For Both The Questions.

Truth Table: -

Input			Output.
S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7.

Circuit:-


I0
I1
I2
I3
4x1
Multiplexer.
S0 S1
2x1
Multiplexer
Y
S0
I0
I1
I2
I3
4x1
Multiplexer.
S0 S1

Question#2

Illustrate the block diagram of 4 to 16 Decoder using 3 to 8 Decoders. You must show the calculation for the number of lower order Decoders required for the design of 4 to 16 Decoder.

Simulate the design in MultiSim to verify the working of the circuit.

Required number of lower order decoder:-

$\frac{m_2}{m_1}$

We know that in 4-16 decoder it has 4 inputs and 16 outputs on the other hand in 3-8 decoder it has 3 inputs and 8 outputs.

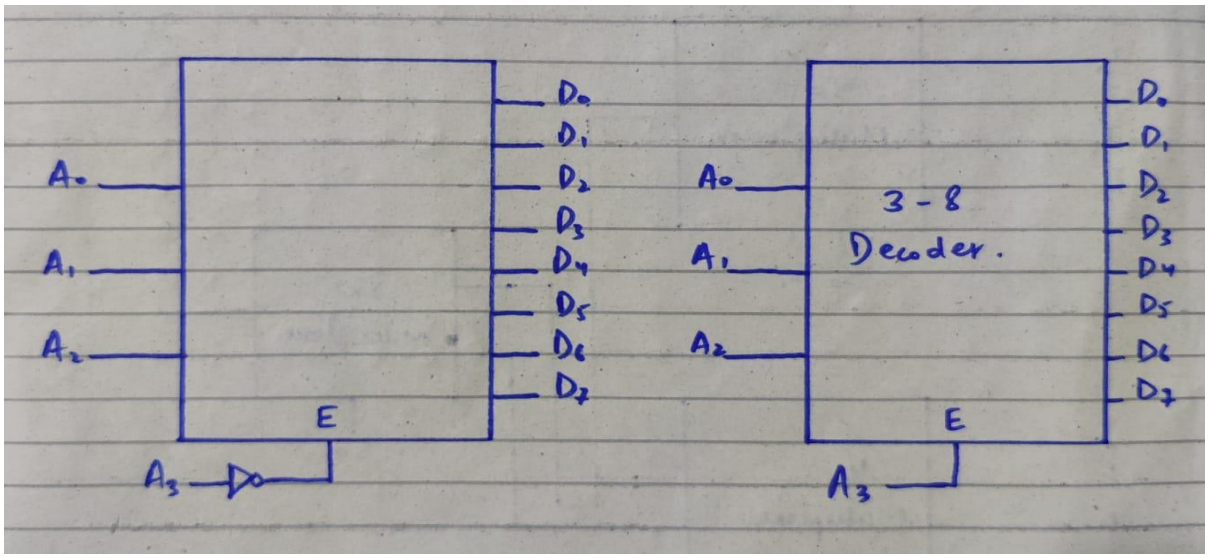
Using above formula m_2/m_1

$m_1 = 8$ and $m_2 = 16$

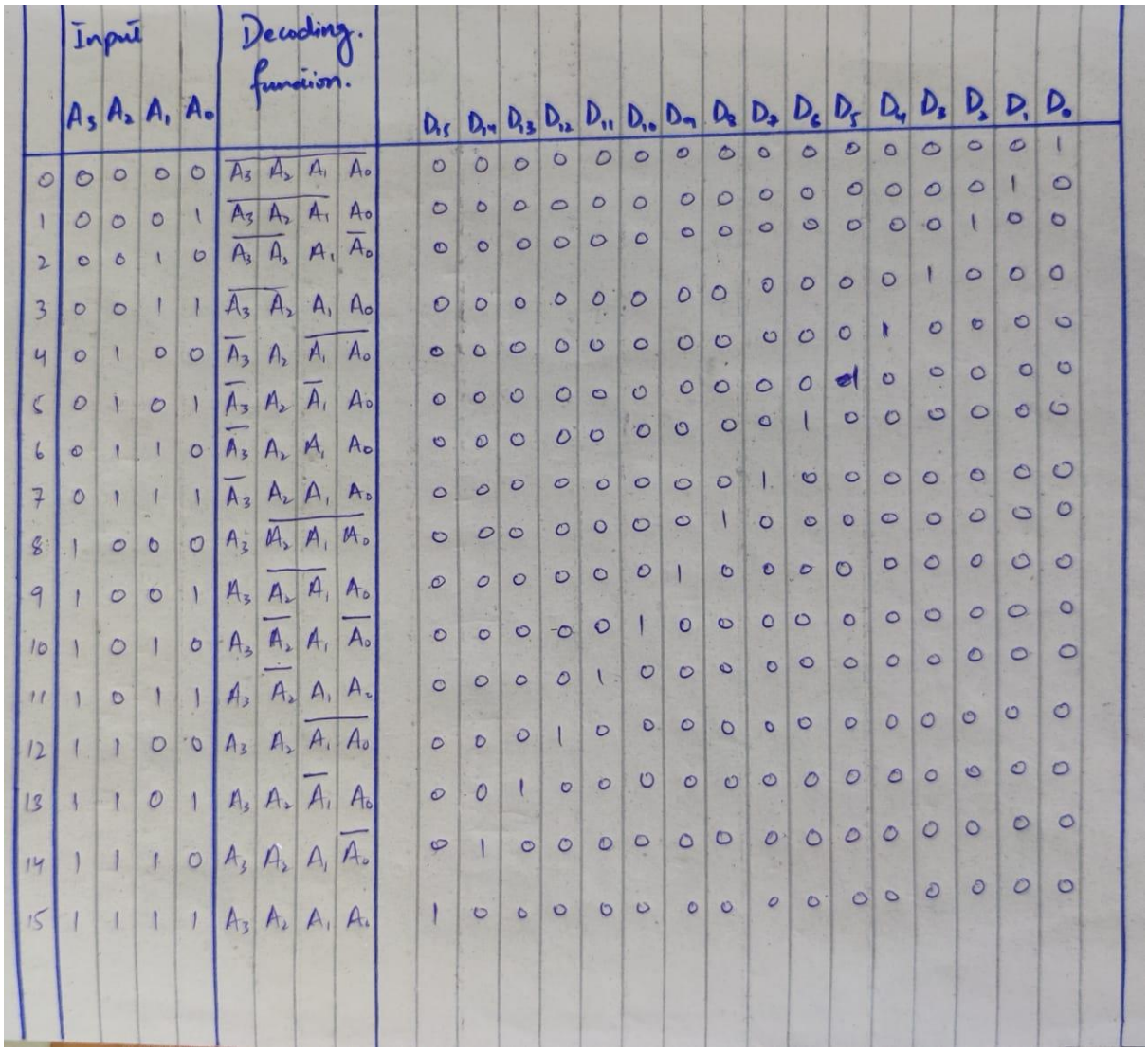
we get $\frac{16}{8} = 2$.

Hence, we need 2 3-8 decoder for implementing 1, 4-16 decoder.

Circuit:-



Truth Table:-



	Input				Decoding function.	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	A_3	A_2	A_1	A_0																	
0	0	0	0	0	$\overline{A_3}\,\overline{A_2}\,\overline{A_1}\,\overline{A_0}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	$\overline{A_3}\,\overline{A_2}\,\overline{A_1}\,A_0$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
2	0	0	1	0	$\overline{A_3}\,\overline{A_2}\,A_1\,\overline{A_0}$	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
3	0	0	1	1	$\overline{A_3}\,\overline{A_2}\,A_1\,A_0$	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
4	0	1	0	0	$\overline{A_3}\,A_2\,\overline{A_1}\,\overline{A_0}$	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
5	0	1	0	1	$\overline{A_3}\,A_2\,\overline{A_1}\,A_0$	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
6	0	1	1	0	$\overline{A_3}\,A_2\,A_1\,\overline{A_0}$	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
7	0	1	1	1	$\overline{A_3}\,A_2\,A_1\,A_0$	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
8	1	0	0	0	$A_3\,\overline{A_2}\,\overline{A_1}\,\overline{A_0}$	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
9	1	0	0	1	$A_3\,\overline{A_2}\,\overline{A_1}\,A_0$	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
10	1	0	1	0	$A_3\,\overline{A_2}\,A_1\,\overline{A_0}$	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
11	1	0	1	1	$A_3\,\overline{A_2}\,A_1\,A_0$	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
12	1	1	0	0	$A_3\,A_2\,\overline{A_1}\,\overline{A_0}$	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
13	1	1	0	1	$A_3\,A_2\,\overline{A_1}\,A_0$	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
14	1	1	1	0	$A_3\,A_2\,A_1\,\overline{A_0}$	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	1	1	1	1	$A_3\,A_2\,A_1\,A_0$	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0