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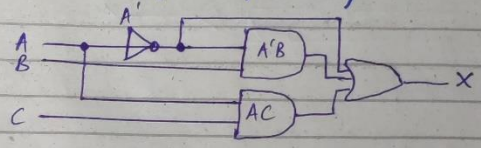
DLD ASSIGNMENT # 02

Question A :-

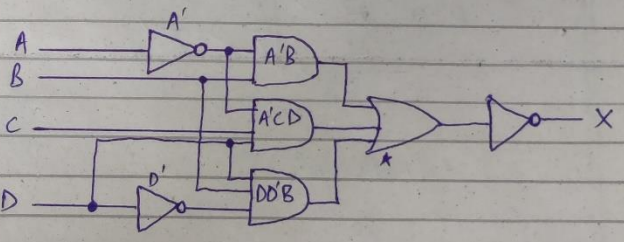
1. Write the output expression for each circuit in

(a)



$X = A' + A'B + AC$ /Ans.

(b)



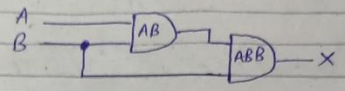
* $A'B + A'CD + DBD'$

Now lets pass them from the not gate.

$X = AB' + AC'D' + D'B'D$ /Ans.

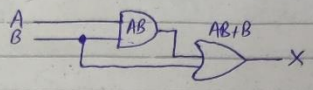
2. Write the output expression for each circuit as it appears in.

(a)



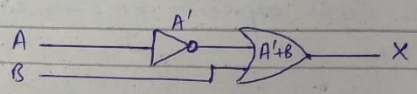
$X = AB.B.$

(b)



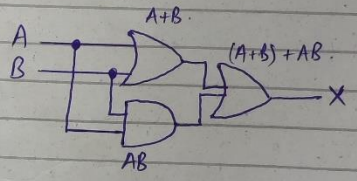
$X = AB + B$

(c)



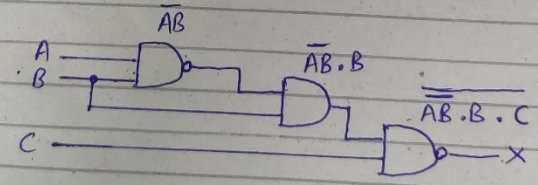
$X = A' + B$

(d)



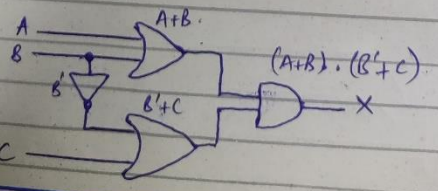
$X = (A+B) + AB.$

(e)



$X = AB.B'.C'$

(f)



$X = (A+B).(B'+C)$

Question C:

*Question B at end.

For each set of binary numbers, determine the output states for the comparator of Figure 6-21.

(a) $A_3 A_2 A_1 A_0 = 1010$
$B_3 B_2 B_1 B_0 = 1101$

Let start by comparing each bit from MSB

$A_3 = 1$, $B_3 = 1$ $A_3 = B_3$.

Let move on to the next as we can't decide from this one,

$B_2 = 1$, $A_2 = 0$ $A_2 < B_2$.

There's no point of comparing the rest but let's do it as the comparator will do and then make it will don't care. So $A < B$

$A_1 = 1$, $B_1 = 0$ $A_1 > B_1$ (D.C)
$A_0 = 0$, $B_0 = 1$ $A_0 < B_0$ (D.C).

Output :-

Hence the output states are,

$A < B = 1$ (High) and the rest are low which are ;

$A > B = 0$ and $A = B = 0$

(b) $A_3 A_2 A_1 A_0 = 1101$
$B_3 B_2 B_1 B_0 = 1101$

Comparing bit by bit.

$A_3 = B_3 = 1$.
$B_2 = A_2 = 1$.
$A_1 = B_1 = 1$.
$A_0 = B_0 = 1$

$A = B$.

Output :-

Hence, $A = B = 1$ (High) and the others are LOW that are,

$A < B = 0$, $A > B = 0$

(c) $A_3 A_2 A_1 A_0 = 1001$

$B_3 B_2 B_1 B_0 = 1000$

Comparing bit by bit ;

$A_3 = 1$,	$B_3 = 1$	$A_3 = B_3$.
$A_2 = 0$,	$B_2 = 0$	$A_2 = B_2$.
$A_1 = 0$,	$B_1 = 0$	$A_1 = B_1$
$A_0 = 1$,	$B_0 = 0$	$A_0 > B_0$

So $A > B$.

Output :-

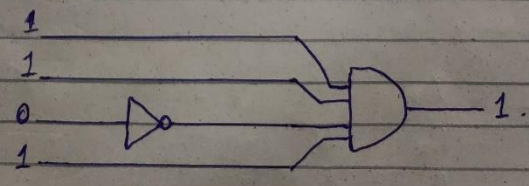
Hence $A > B = 1$ (High) and the others are Low that are,

$A = B = 0$, $A < B = 0$

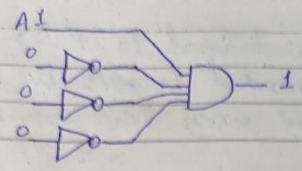
Question D:-

Show that the decoding logic for each of the following codes if an active HIGH (1) output is required.

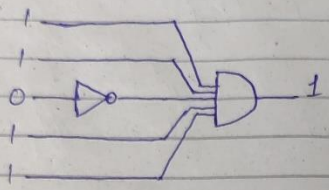
(a) 1101



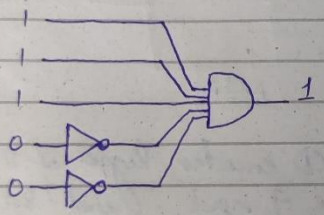
(b). 1000.



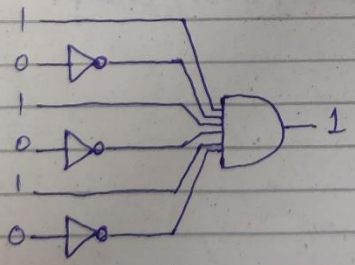
(c) 11011



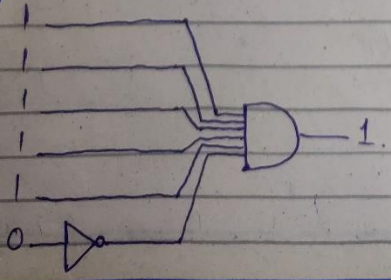
(d) 11100



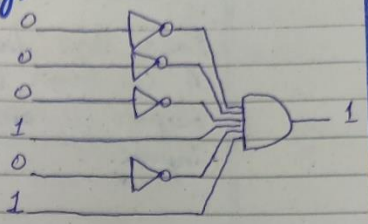
(e) 101010



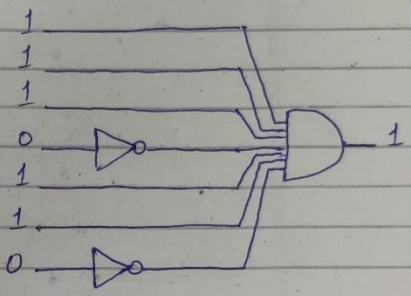
(f) 111110



(g) 000101.

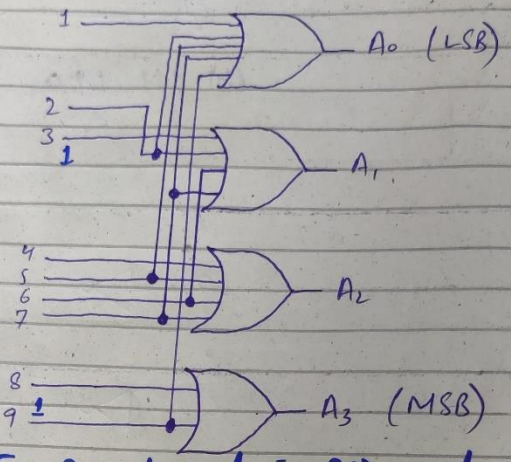


(h) 1110110



Question E :-

Basic logic diagram of a decimal to BCD encoder. A 0-digit is not needed because the BCD outputs are all LOW when there are no HIGH inputs.



- For the decimal-to-BCD encoder logic of the above figure assume that the 9 input and the 3 input are both HIGH. What is the output code? Is it a valid BCD (8421) code?

- **Output :-**

$A_3 = 1$, $A_2 = 0$, $A_1 = 1$, $A_0 = 1$

$A_3 A_2 A_1 A_0 = 1011$ and its an invalid BCD.

- **Reason :-**

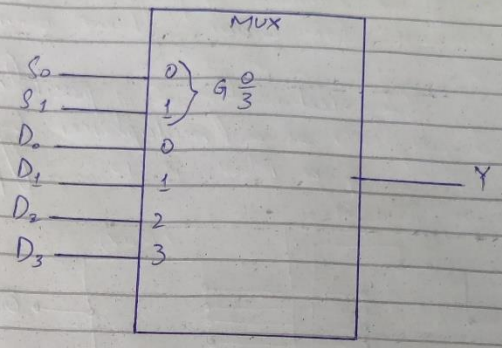
This an invalid BCD, as in BCD decimal digit is represented by 4-bit binary code which ranges from (0000 - 1001) or (0-9) but it is 1011 or 11 which is invalid.

oder.

HIGH

Question F:

For the multiplexer in the Below Figure, determine the output for the following input states:
$D_0 = 1$, $D_1 = 0$, $D_2 = 0$, $D_3 = 1$, $S_0 = 0$, $S_1 = 1$



As we know the multiplexer output expression:

$$\text{Output} : D_0 \bar{S_1} \bar{S_0} + D_1 \bar{S_1} S_0 + D_2 S_1 \bar{S_0} + D_3 S_1 S_0.$$

and also putting the values.

$$\text{Output} : 1\bar{1}\bar{0} + 0\bar{1}0 + 0\bar{1}\bar{0} + 110.$$
$$\text{Output} : 101 + 000 + 011 + 110$$
$$\text{Output} : 0 + 0 + 0 + 0.$$

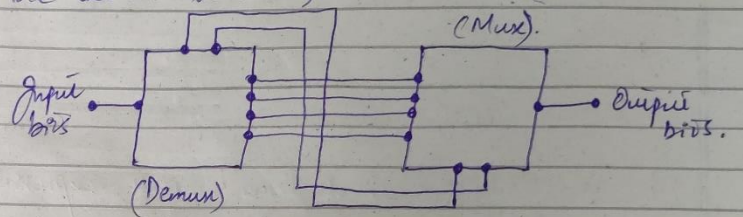
Output = 0

Question 9:

Can a demultiplexer be used as a multiplexer?

If we talk only about using a demux alone then we cannot perform such action because both circuit have own operation,

But technically it is possible, we can use a demultiplexer as a multiplexer by using a Demux circuit & a Mux is to perform the action that is,



Question B:

1. **What is a Full-Adder, also draw the complete logic circuit for Full Adder.**

For the full adder of your logic diagram, determine the outputs for each of the following inputs.

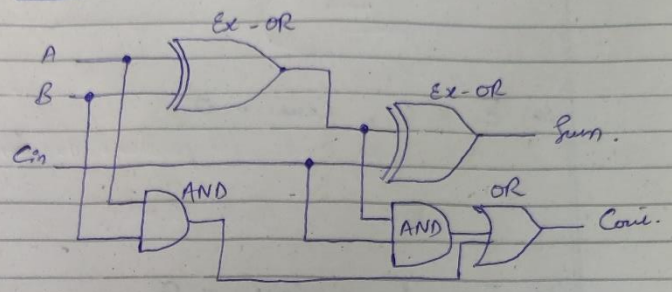
Full Adder :-

A full Adder is a digital logic circuit that adds three binary digits or even more when used multiple, also gives a carry bit as output.

It is used to perform addition of two binary number of any length. The three or more input bits

are usually referred to as A, B and Cin, where A and B are the bits to be added and Cin is the carry-in bit from the previous stage.

• **Logic Circuit :-**



(a) A = 0, B = 1, Cin = 0

Sum = 1, Carryout = 0.

(b) A = 1, B = 0, Cin = 1.

Sum = 0, Carryout = 1.

(c) A = 0, B = 0, Cin = 0

Sum = 0, carryout = 0.

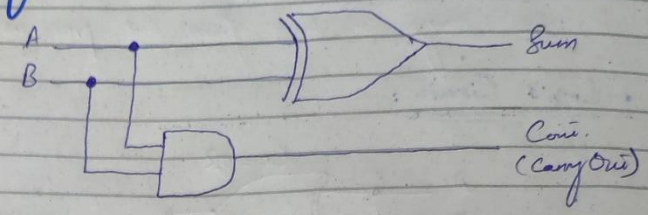
2. What is half adder?

What are the half-adder inputs that will produce the following outputs,

• **Half Adder:-**

A digital circuit that performs addition operation on a 2 input binary values gives 2 outputs that is sum and carry out.

• Logic Circuit :-



(a) $\Sigma = 0$, $C_{out} = 0$

The inputs that will produce this are,

$A = 0$ and $B = 0$.

(b) $\Sigma = 1$, $C_{out} = 0$

The inputs that will produce this are,

$A = 1$ and $B = 0$ or $B = 1$ and $A = 0$.

(c) $\Sigma = 0$, $C_{out} = 1$.

The inputs that will produce this output are,

$A = 1$ and $B = 1$.

THE END.