

10-12-2024

## CMOS

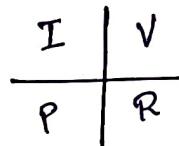
Dr. Parvin Zode

### Electronic Components

q - charge in Coulombs.

$$I = \frac{q}{t}$$

V, R, P, Energy.



Tools

Nspice

Xscheme

Sim

Magic

- Ladane
- microwind

DC

→ Drift velocity

AC

~~DDP~~, Power delay product.

$$R + jX_L$$

Capacitor  $\rightarrow$

→ Electrostatic energy storage

$$\rightarrow X_C = \frac{1}{2\pi f C} = \frac{1}{\omega C}$$

$$\rightarrow W = \frac{1}{2} CV^2$$

$$\rightarrow V = \frac{1}{C} \int_{t_0}^t i(t) dt + V(t_0)$$

$$\rightarrow i = C \frac{dV}{dt}$$

Inductor  $\rightarrow$

→ Electromagnetic storage.

$$X_L = 2\pi f L = \omega L$$

$$W = \frac{1}{2} L I^2$$

$$V = L \frac{di}{dt}$$

$$i = \frac{1}{L} \int v(t) dt + i(t_0)$$

Initial  
current  
Voltage at  $t_0$

Diode  $\rightarrow$

→ Knee voltage, cut in voltage

min. voltage at which junction starts conducting

→ Break down voltage.

conduction in Reverse  $\rightarrow$  Zener breakdown (Avalanche breakdown)

BJT  
PNP NPN

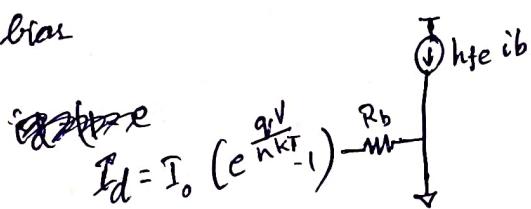
FET  
JFET MOSFET

$$(hfe)\beta = \frac{I_C}{I_B} \quad (\text{CE current gain}) > 1000$$

$$\alpha = \frac{I_E}{I_C} \quad (\text{CB current gain}) \leq 1$$

$i_p$  forward bias  
 $o_p$  reverse bias  
Biasing  
for amplifier.

bias



$$I_d = I_0 \left( e^{\frac{qV}{nKT}} - 1 \right)$$

$$\gamma = \frac{I_E}{I_B} \quad (\text{CC current gain})$$

ECL fastet  $\frac{o_p}{i_p}$

Small signal analysis.

(1)

• Characteristics (VI), Load Line, Q point.  
 ↓  
 (max operating voltage,  
 max op current)  
 → steady state (no input)  $(V_{Q_1/2}, I_{Q_1/2})$   
 voltage, current.  
 ↓  
 ideal

• Clipper & Clamper.

• Cut-off, Active, Saturation region  
 (R<sub>B</sub>, R<sub>D</sub>)      ↓  
 Amplifier.      (F<sub>B</sub>, F<sub>B</sub>)  
 (I<sub>P</sub>, O<sub>P</sub>)      (I<sub>P</sub>, O<sub>P</sub>)

SPICE → simulation program for with Integrated Circuit Emphasis.

Type of analysis

- DC operating point
- Transient analysis.
- Frequency analysis.
- Monte-Carlo analysis → (Worst case analysis)

→ Tolerance, ⇒ Max min operating voltage, current.

Advanced Simulation Feature

- Reverse saturation current slower after +10°C
- Parametric sweeps
- Optimization algorithm

10E ⇒ 10Ω

Mega \* (not) M

Dependent sources

mil =  $25.4 \times 10^{-6}$

$\mu \Rightarrow n$

.cir / .sp

Circuit Description

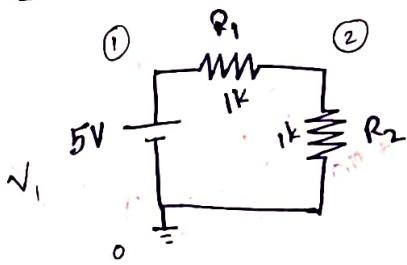
1. Title

2. .... +

§ .end

↳ line continued in next line

## NGspice



comment  
Voltage Divider

V1 1 0 5V  
R1 1 2 1k  
R2 2 0 1k

First line is always title.

source end value  
end element  
element meet

11-12-2014

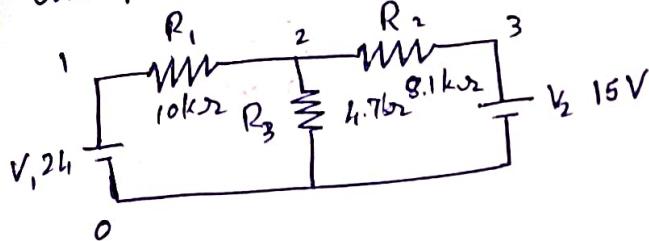
Netlist  $\rightarrow$  Description of circuit.

+ at end denote continue of line.

comment in a line is added after ; <comment>

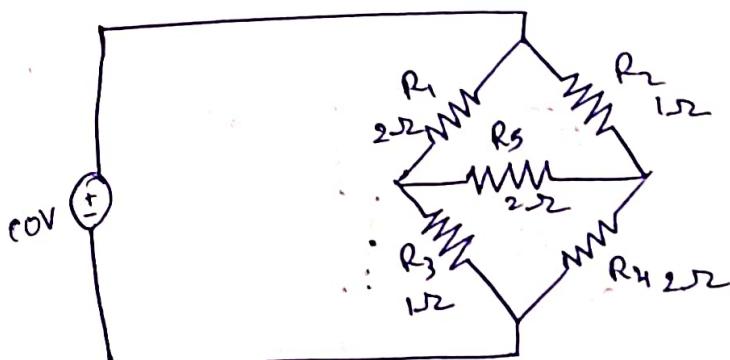
. before command

## Example 01



cadence

CIR  $\rightarrow$  schematic  
ngspice  $\rightarrow$  view, output file.

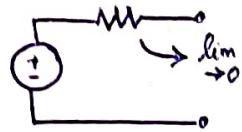


Simem  $\frac{t}{\text{ngspice}}$

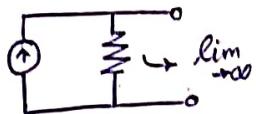
ngspice  
Synonym

Voltage source vs Current source.

→ const  $V$



const  $I$



$$\text{Circuit diagram showing a voltage source } V_i \text{ in series with a resistor } R_1. \text{ The output voltage } V_o \text{ is across } R_2. \Rightarrow V_o = \frac{R_2}{R_1 + R_2} V_i$$

$$I = I_1 + I_2$$

$$I_1 = \frac{V_i}{R_1}$$

$$I_2 = \frac{V_o}{R_2}$$

$$I = I_1 + I_2$$

$$I_1 = \frac{V_i}{R_1}$$

$$I_2 = \frac{V_o}{R_2}$$

$$I_1 R_1 = I_2 R_2$$

$$I_2 = I - I_1$$

$$I_2 = \frac{I_1 R_1}{R_2}$$

$$= \frac{I R_1}{R_2} - \frac{I_2 R_1}{R_2}$$

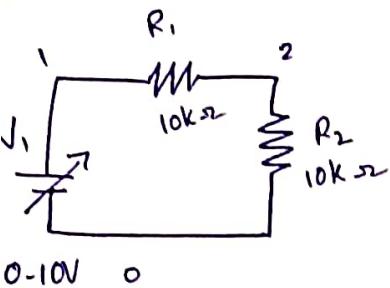
$$\frac{I_2 + I_1 R_1}{R_2} = \frac{I R_1}{R_2}$$

$$I_2 \left( \frac{R_2 + R_1}{R_2} \right) = I \frac{R_1}{R_2}$$

$$I_2 = I \frac{R_1}{R_1 + R_2}$$

$$\lim_{R_1 \rightarrow \infty} \frac{R_1}{R_1 + R_2}$$

DC sweep



+ DC sweep

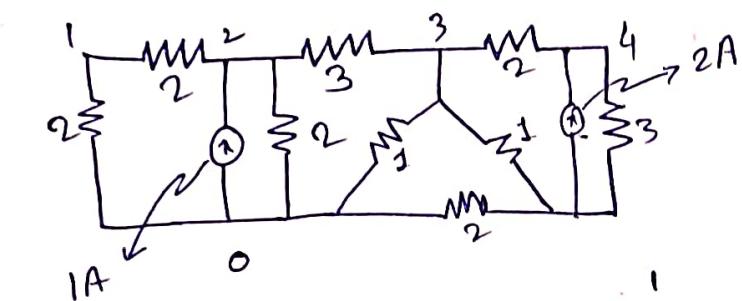
V1	1	0	10V
R1	1	2	10k
R2	2	0	10k

.dc v1 0 10 1

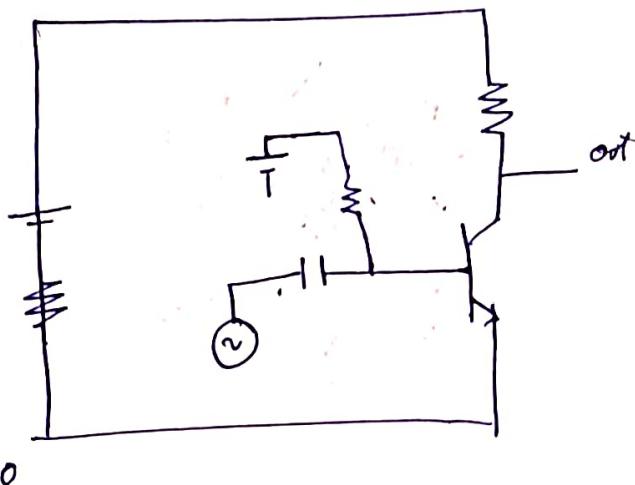
.print dc v(2)

.end

.dc <source> <from> <to> <steps>

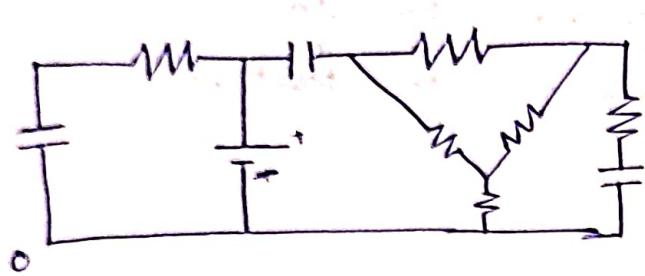


$v(c)$  → node  
 $i(c)$  → component

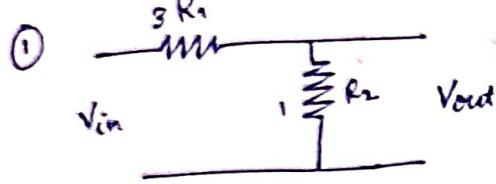


$$S_1 \xrightarrow{P} B \xrightarrow{?} G_e \rightarrow ?$$

$$\xrightarrow{N} P$$



### Sensitivity Analysis



$$\frac{\partial V_{out}}{\partial R_2} = \frac{(R_1 + R_2) - R_1}{(R_1 + R_2)^2} V_{in}$$

sens  $V_{out}$

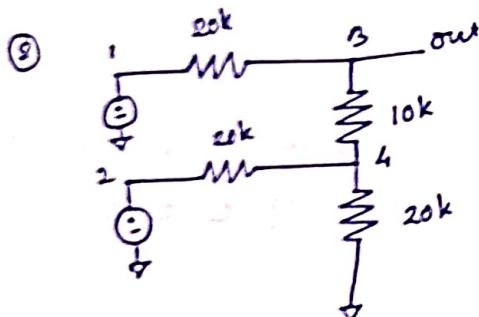
$$\Rightarrow \frac{\partial V_{out}}{\partial R_2} = \frac{R_1}{(R_1 + R_2)^2} V_{in}$$

$$V_{out} = \frac{R_2}{R_1 + R_2} V_{in}$$

$$\Rightarrow \frac{\partial V_{out}}{\partial R_1} = \frac{-R_2}{(R_1 + R_2)^2} V_{in}$$

$$\text{gain} = \frac{V_o}{V_{in}}$$

differentiation w.r.t  $R_2$



$V_{msb}$	1	0	0V
$V_{lsb}$	2	0	0V
$R_1$	1	3	20k
$R_2$	2	4	20k
$R_3$	3	4	10k
$R_4$	4	0	20k

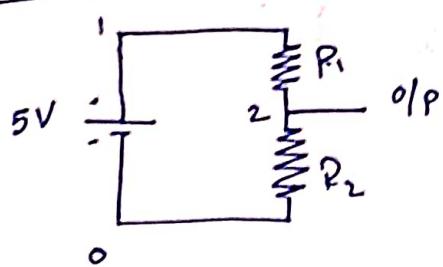
$t_f \rightarrow V(Q)$

### Transfer function

Voltage source short circuited

tf  $\rightarrow$  output < name of ip source

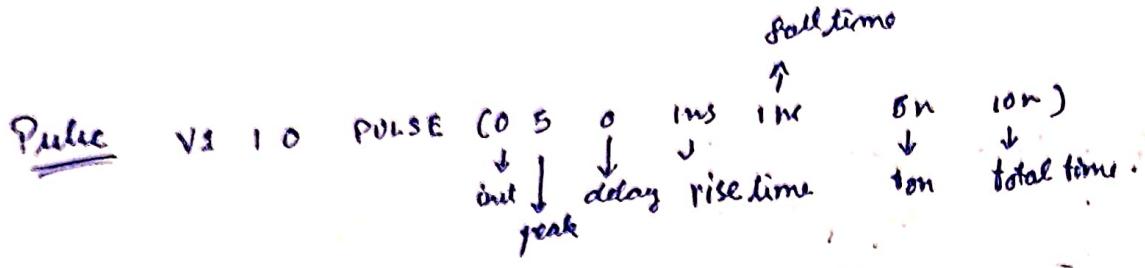
### Transient



print them C1, C2

.from 0 10ms 1ms

.tran <start><end><step>



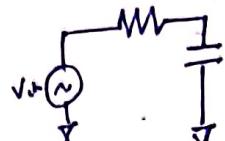
## RC circuit analysis

$$V_{in} V_{in} 0 \text{ DC } 0 \sin 0 1 200$$

$$R_1 V_{in} V_{out} 1k$$

$$C_L V_{out} 0 1\mu$$

.end



## AC analysis

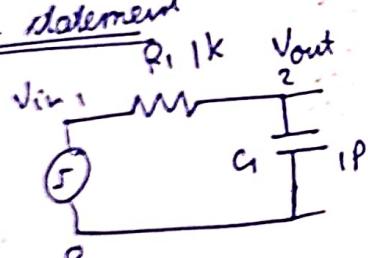
Decade, Octave, Decibelle dB

$$3\text{dB} \Rightarrow \sqrt{2}$$

Butterworth filter.

-20 dB/decade

## Pulse statement



$$R =$$

pulse 0 16n 00sn 10n

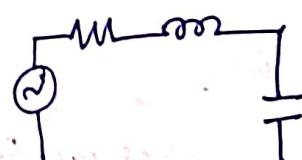
RESULT

$$\text{Time constant} \rightarrow \tau = R \times C$$

$$I = 1 \times 10^9 \times 1 \times 10^{-12}$$

$$= 1 \times 10^{-3}$$

$$= 1 \text{ nA}$$



→ Physical structure of MOSFET

→ Regions in MOSFET → Saturation  
→ cutoff

→ CMOS logic → Ratiored logic  
→ noise cancellor

→ transmission gate

→ Dynamic logic circuits

sequential, arithmetic ...

Different biasing techniques

- Baseline

- C-B bias

- Voltage divider

Quality Metrics - Performance, Power Dissipation, Cost, ...

IC classification - Digital integrated circuit, Analog, mixed signal

Multi-core → Increase in frequency not possible  
more core  $\Rightarrow$  more work, less on some frequencies.

mult chip design → signaling delay  
→ handshaking required.  
→ needs more area.

BJT  $\Rightarrow$  cannot be scaled down  $\rightarrow$  (unlike CMOS) channel length is fixed.

Transistor count, die size,  $\downarrow$  1/year, frequency, power dissipation,  
 $\times 2$  in year heat  $\Rightarrow$  thermal runaway

• power density (W/cm²)

1. MOS memory

2. analog

3. Display driver

4. Special purpose IC

MPU

MCU

DSP

Standard cell ASIC

FPGA

chip in IOT

Sensor

Semiconductor

Cost per 100 transistors decrease with new technology.

### Design Metrics

Cost, Reliability, Scalability, Speed, Power consumption, Energy to performance

Cost

Cost of integration.

→ NRE (Non recurring cost) Design time, effort, mask generation.

→ Recurring C

Yield

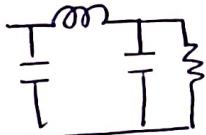
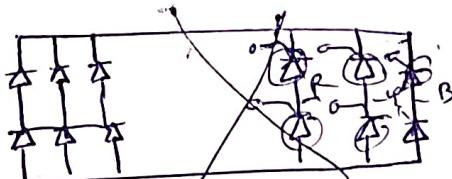
$$Y = \frac{\text{No of good chips / wafer}}{\text{Total number of chips}} \times 100$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield.}}$$

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ORCAD X CIS

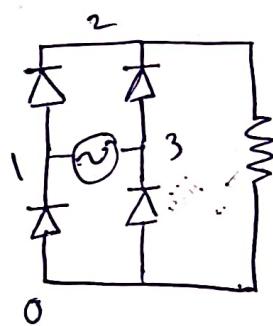
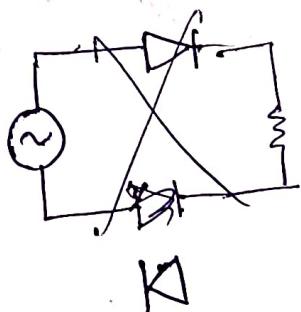
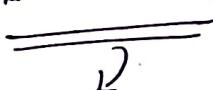
in 007



Scale should be

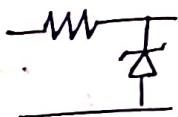
Set to V

Auto Range



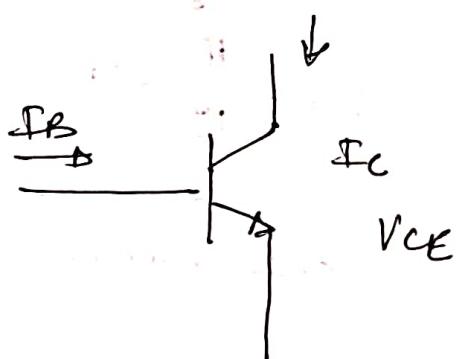
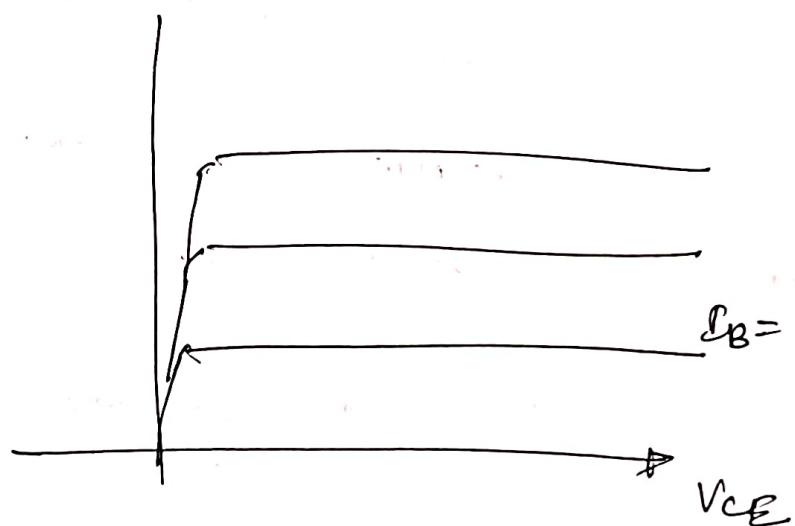
BC547  $\rightarrow$  BJT

84C5  $\rightarrow$  Zener with 5V



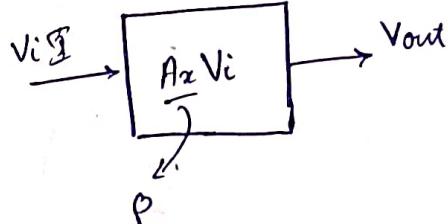
1-1

Se



13/12/2024

Zener heavily doped junction  
Zener Breakdown



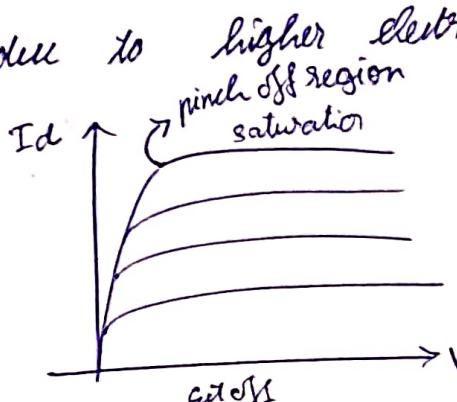
MOSFET as a switch

CMOS allow rail-to-rail logic voltage swing.  $\rightarrow$  independent of biasing resistor.

Enhancement  $\rightarrow$  positive voltage is required to create channel between drain & source.

Faster than PMOS due to higher electron mobility

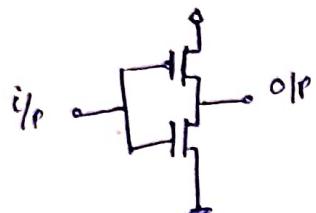
$I_D$  vs  $V_{DS}$



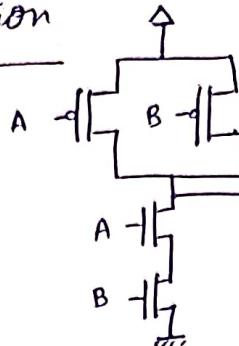
(9)

## Region of operation of MOSFET

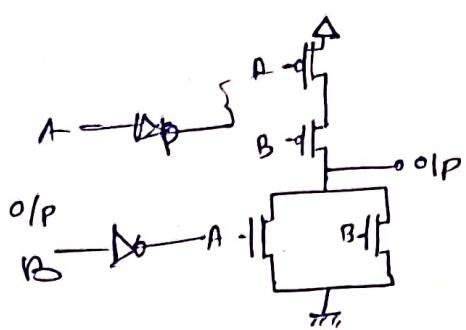
• Cut off - Ohmic - Saturation



CMOS INVERTER



CMOS NAND



CMOS NOR

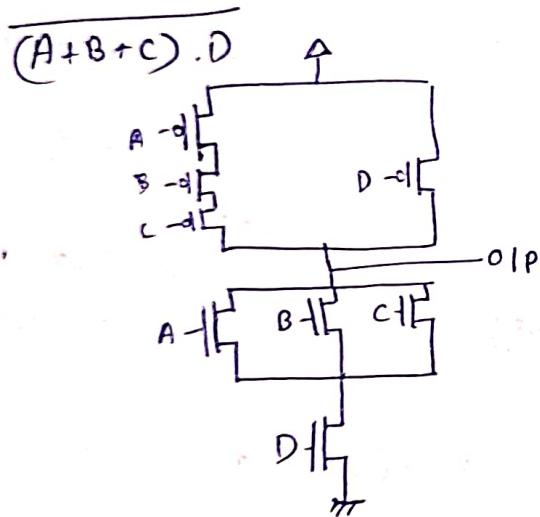
	pullup OFF	pullup ON
Pull-down OFF	Z (float)	I
OFF	0	X (crowbar) → Short circuit

$$\begin{array}{ll}
 A \ B & \overline{A+B} = Y \\
 0 \ 0 & 1 \\
 0 \ 1 & 0 \\
 1 \ 0 & 0 \\
 1 \ 1 & 0
 \end{array}
 \quad
 \begin{array}{l}
 \overline{A+B} \Rightarrow A \cdot B \\
 0 \\
 0 \\
 0 \\
 1
 \end{array}$$

micro wind 2

with Spice

Dsh 2

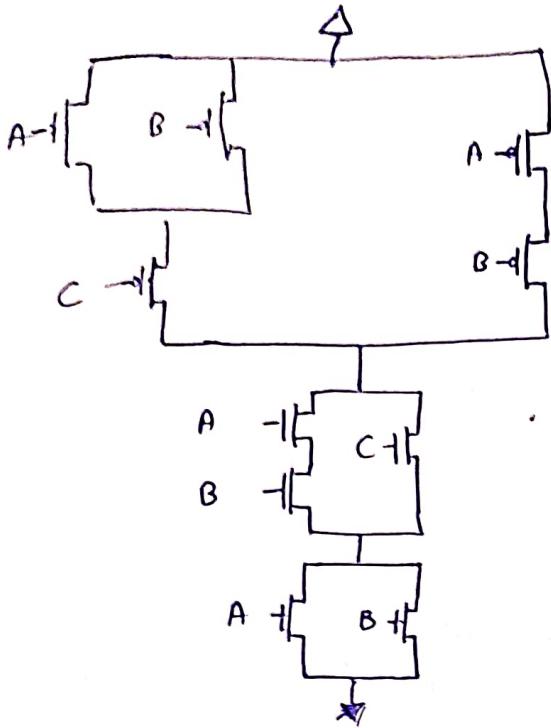


Lab 01

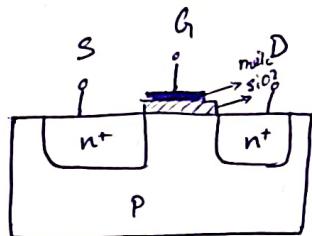
- $Y = \overline{A}$
- NAND, NOR
- $Y = \overline{ABC+D}$
- $Y = \overline{(AB+C)} \cdot D$
- $Y = \overline{AB+C} \cdot \overline{(A+B)}$

Half Adder → Full Adder  $\Rightarrow$  ALU

$\hookrightarrow$  ADD  
 SUB  
 AND  
 OR



14-12-2024  
MOSFET  $\rightarrow$  Metal oxide semiconductor FET  
 $\downarrow$  replaced with  
polysilicon gate



4-terminal device  $\rightarrow$  gate, source, drain, body.  
 gate, body  $\rightarrow$  conductors.  
 $\downarrow$  can be interdigitate  
 $\downarrow$  usually tied to ground.  
 $\downarrow$  insulators  
 $\downarrow$  Ebene more model (BJT) EAC

Source-body, drain body diodes are OFF  $\Rightarrow$  Reverse bias.

OFF  $\Rightarrow$   
reverse bias.

ON  $\Rightarrow$   
channel formation by induced charges

Accumulation  
Depletion  
Inversion.

Terminal voltage

$$V_{GS}, V_{GD}, V_{DS} = V_D - V_S = V_{GS} - V_{GD}$$

Operating region

cutoff - ohmic - saturation

Speed of operation  $\rightarrow C_{\text{ox}} \cdot I_{\text{ds}} \rightarrow I = C \frac{dV}{dt} \Rightarrow dt = C_0 \frac{dV}{I}$

$C = \frac{\epsilon A}{d}$        $\epsilon$  permittivity  
 A area  
 $d \rightarrow$  thickness of dielectric

Carrier velocity

$$E = V_{\text{ds}}/L \quad \rightarrow \text{length}$$

$$V = \mu E \quad \begin{matrix} \downarrow \\ \text{mobility} \end{matrix}$$

Drain Current  $I_{\text{ds}} = \frac{Q_{\text{channel}}}{t} \Rightarrow I_{\text{ds}} = \beta (V_{\text{gs}} - V_t - \frac{V_{\text{ds}}}{2}) V_{\text{ds}}$

$$I_{\text{ds}} = 0 ; V_{\text{gs}} < V_t$$

$$\begin{cases} \text{Saturation} \\ \text{Region} \end{cases}$$

$V_{\text{ds}} < V_{\text{sat}}$   
 $V_{\text{ds}} > V_{\text{sat}}$

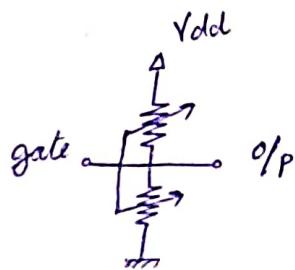
$$\beta = \mu C_{\text{ox}} \frac{W}{L} \quad \begin{matrix} \rightarrow \text{width} \\ \rightarrow \text{length} \end{matrix}$$

$$I_{\text{ds}} = \frac{\beta}{2} (V_{\text{gs}} - V_t)^2 \quad [\text{no } V_{\text{ds}}]^*$$

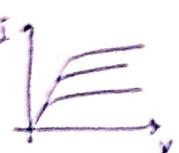
15-12-2024

Inverter Analysis

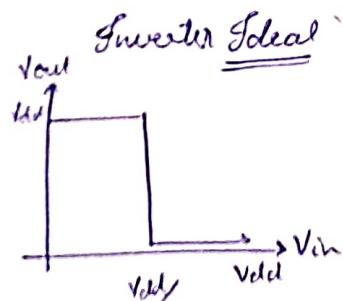
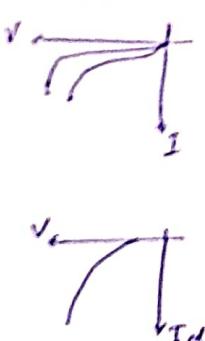
MOSFET  $\rightarrow$  Varactor model



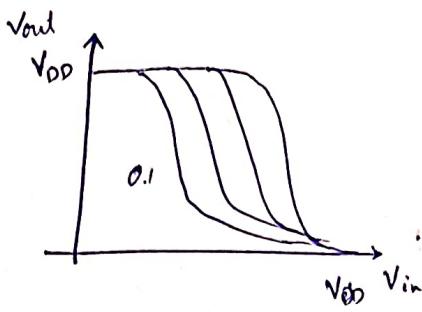
Pmos



Nmos



$$\beta = \mu C_o \frac{W}{L} \quad \underline{\beta \text{ ratio effect}}$$



$$\frac{\beta p}{\beta n} = r$$

un-skew  $\rightarrow r=1$

hi skew  $\rightarrow r > 1$

low skew  $\rightarrow r < 1$

Noise Margin minimum HIGH, maximum LOW

Both at  $i/p < o/p$

Noise margin

$$HIGH = O/p_H - i/p_H$$

$$LOW = O/p_L - i/p_L$$

Power Instantaneous Power, Energy, Average Power.

$$P(t) = I(t) V(t)$$

$$E = \int_0^T P(t) dt$$

$$P_{avg} = \frac{E}{T} = \frac{1}{T} \int_0^T P(t) dt$$

Power Degradation

- Static power
- Dynamic power.

Total power Dissipation

- Active Power
- Standby power
- Sleep mode

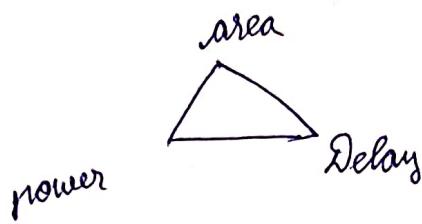
Capacitance

gate capacitance, wire capacitance

Voltage & frequency

17-12-2024

## Delay



} for a some process mode  
} this cannot be changed

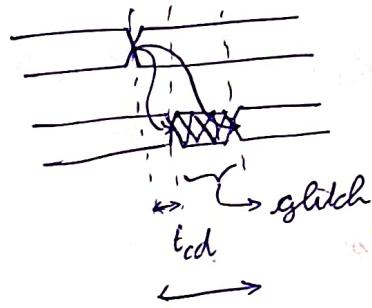
→ propagation delay. ( $t_{pd}$ )

\* max time from i/p crossing 50% to o/p crossing 50%.

→ contamination delay ( $t_{cd}$ )

\* min time from i/p crossing 50% to o/p crossing 50%.

$$t_{cd} \leq t_{pd}$$



→ rise time ( $t_r$ ) 20% to 80%. time taken  $t_{pd}$

→ fall time ( $t_f$ ) 80% to 20%. time taken

→ edge rate ( $t_{rf}$ ) avg of  $t_r = t_f \Rightarrow t_{rf} = \frac{t_r + t_f}{2}$

→ setup time ( $t_s$ ) min time data should be stable before clk arrives

→ hold time ( $t_h$ ) min time data should be stable after clk arrives

→ slack → difference between required and arrival time.

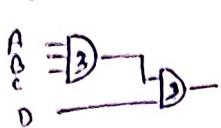
positive slack → (required) → meets timing.

negative slack → timing not met.

BC547  
BC548  
SL100

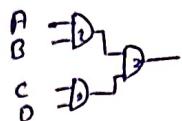
2 i/p AND gate  
A=2  
 $=D-$

area required 2 units / 2 i/p Gate  
3 " 3 "  
 $Y = ABCD$



$$A=5 \quad D=5$$

$\Rightarrow$  min area



$$A=6 \quad D=4$$

$\Rightarrow$  min delay

Critical path  $\rightarrow$  longest path need to compute the output.

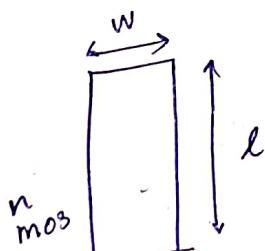
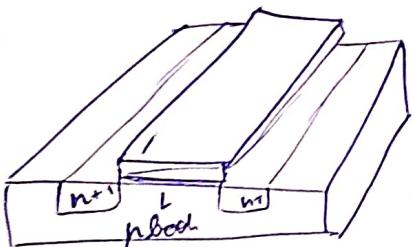
- $\rightarrow$  architectural / micro-architectural level (number of pipeline)
- $\rightarrow$  logic level (Experiment based, experience, logic synth tools)
- $\rightarrow$  circuit level (transistor sizing, alternative CMOS logic styles)
- $\rightarrow$  layout level (wire length reduction, parasitic component reduction, compact layout)

Data path subsystem design  $\rightarrow$  area (vs) delay

$\rightarrow$  optimizing for area, (or) delay (or) power

no of i/p  
fan-in, fanout  
sink capacity

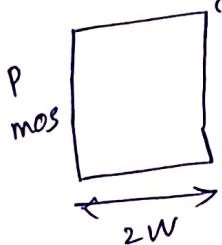
$\rightarrow$  gain in BJT MOSFET (Gm) (count)  
 $\rightarrow$  from conductance gfs (S)



$$\mu_n = 0.135 \text{ m}^2/\text{volt}\cdot\text{sec}$$

$$\mu_p = 0.048 \text{ m}^2/\text{volt}\cdot\text{sec}$$

$$\mu_n \approx 3 \mu_p$$



$\rightarrow$  twice the width  
 $\rightarrow$  to compensate the difference in mobility characteristics

$$C = \frac{EA}{d}$$

Dynamic CMOS, Pass transistor, Complementary pass transistors

minimum transistor count  $\approx$  inversion speed

reduces capacitive load  
on i/p

$t_{rise} > t_{fall}$   $\rightarrow$  for similarly doped n PMOS have high  $\sigma$

$\Rightarrow R$  than NMOS

Parasitic capacitance

Network theory  
Van Varkenbous

Capacitance of Inverter

6 → some are shorted

$$\Rightarrow C_{out} = C_{db} + C_{sb} + C_{wire} + C_{gs}$$

drain - bulk +  
source - bulk +  
wire +  
gate source +

$$I_C = C \frac{dV}{dt}$$

$$V_C = \frac{1}{C} \int_0^t i_C dt$$

first order RC model

$$- \frac{R}{C} \frac{I}{T}$$

$$V_{ss} \rightarrow V_{dd} - F$$

$$V_{out} = V_{dd} (1 - e^{-\frac{t}{RC}}) \quad T = RC$$

$$t_{pd} = 0.69 RC$$

Sizing of inverter

• Carrier Mobility Difference.  $\mu_n \approx 3 \mu_p$

• Drive strength matching. [PMOS less efficient]  $\rightarrow$  width increased.

NAND vs NOR  $\rightarrow$  cost  $\rightarrow$  flash, SD, Intel EEPROM.

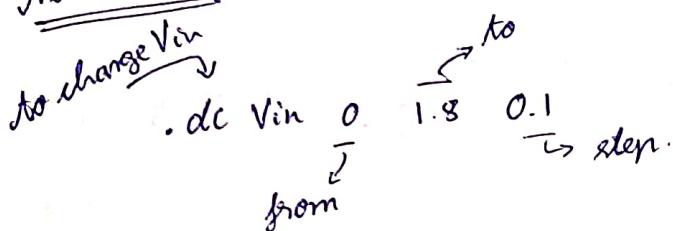
Drain current of MOSFET in saturation region.

for equal current from PMOS & NMOS

twice  
PMOS is made double  
the width

$$I_d = \frac{\mu_n C_{ox} W}{2} \frac{V_{ds} - V_{th}}{L}^2$$

Noise analysis.



ngspice

plot  $v_{out}$   $v_{in}$



plot  $\underline{\text{deriv}}(v_{out})$   
↳ derivative

let  $gain = abs(\underline{\text{deriv}}(v_{out})) >= 1$

⇒ to plot as 'oi'

plot gain  
↳ change

low side noise margin

0.7

upper side noise margin

0.95

$\frac{W}{L} = 3.5$ req
mech [2]

so noise margin  
not symmetrical

## Delay analysis

$$V_{in} = \mu \text{sec}(0.18 \quad 0 \quad .3n \quad .3n \quad 6.6n \quad 5)$$

dc  $\frac{V_{in}}{I}$  2.81m

trans 0.2n 10n

setplot  $\rightarrow$  last plot available  
ngence setplot trans

$\rightarrow$  to measure propagation delay ( $t_{ph}$ )

meas trans  $V_{out50}$  when  $V_{in} = 0.9$   $\frac{\text{RISE} = 2}{\text{fall time of } 1.8} \rightarrow$  to take second rising pulse

$\rightarrow$  similarly

meas trans  $V_{out50}$  when  $V_{out} = 0.9$  FALL = 2

$\rightarrow$  to calculate difference

$$\text{let } t_{ph\text{HL}} = V_{out50} - V_{in50}$$

propagation delay  $\downarrow$

high to low plot  $t_{ph\text{HL}}$

point  $\rightarrow$  change pulse 0.1 that changes ( $t_{ph}$ )

$$\text{let } V_{out10} = .18$$

$$\text{let } V_{out90} = 1.6$$

$\rightarrow$  measure from 10% to 90%

meas from  $t_{on10}$  when  $V_{out} = 0.18$

$$\text{RISE} = 1$$

meas from  $t_{off90}$  when  $V_{out} = 1.6$

$$\text{RISE} = 1$$

give time

$$\text{let } t_r = t_{90} - t_{10}$$

point  $t_r$

To reduce tr power of supply can be increased

- increase size → width {Wf}
- reduce power
- reduce load capacitance → cap  $0.5 \mu F - 2 \mu F$

parameters in no

→ again, again measure  $t_r$ ,  $t_f$

Power analysis

trans

pulse C

display

→ to measure power

measure from current  $\int_{20}^{40}$  vdd  $\pm$  branch

from =  $20n$  to =  $40n$   
 $e^{-09}$   $e^{-09}$

→ calculate power intermediate

let power\_inte = curr\_inte \* Vdd

print power\_inte

→ average power

let power\_avg = power\_inte /  $20e^{-09}$

print power\_avg

→ reducing load capacitance reduce power.

18-12-2024

Gate & diffusion capacitance, equivalent RC circuits

$$R = \frac{L}{\mu_n C_{ox} W}$$

gate  $\rightarrow$  proportional to width

not diffusion capacitance

$\hookrightarrow$  associated with source & drain region.

$\hookrightarrow$  depends on size of source & drain region.

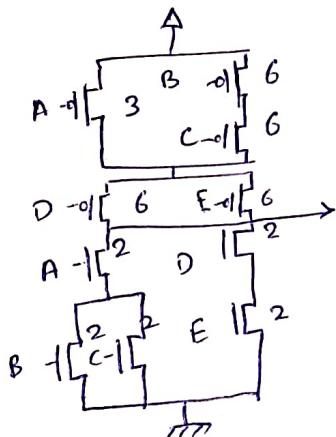
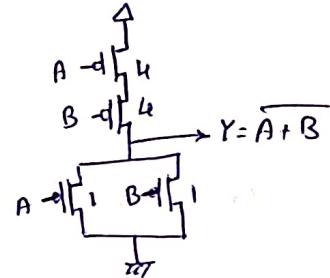
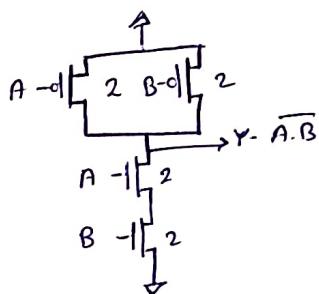
### \* Transistor sizing

NAND offers less delay

NAND uses transistor small size

\* NOR occupies more area

$$A(C+B+C) + DE$$



### PMOS sizing

$$2R/k + 2R/k + 2R/k = R$$

### NMOS sizing

$$2R/k = R$$

PMOS k is given by  $2R/k$

worst case path to V<sub>DD</sub> 1. ECB } 2. DCB }  $2R/k + 2R/k + 2R/k = R$

$$\Rightarrow k=6$$

for All B

$$2R/k = 2R/k_B + 2R/k_C \quad \text{where } k_B, k_C = 6$$

$$2R/k = 4R/6$$

$$\Rightarrow k=3$$

NMOS k is given by  $R/k$

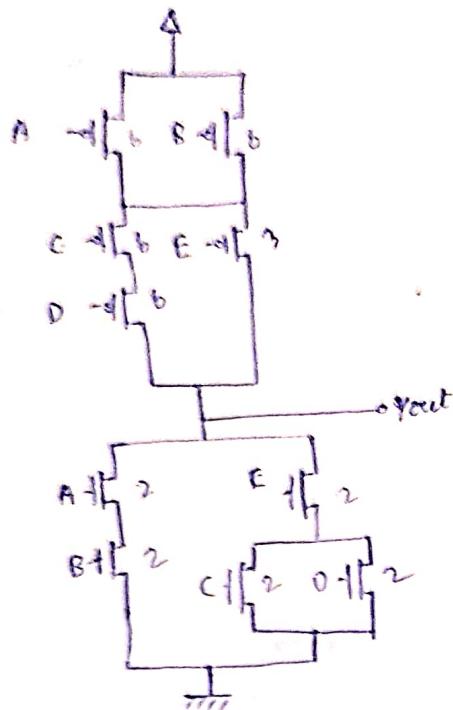
worst case path

$$\begin{cases} AB \\ AC \\ DE \end{cases}$$

$$R/k + R/k = R$$

$$\Rightarrow k=2$$

$$AB + E(C+D)$$



PMOS  
 $R \leq 2R/k$

$$\text{Wideneck } \left. \begin{array}{l} AC \\ BC \end{array} \right\} \frac{2R}{k} + \frac{2R}{k} + \frac{2R}{k} = R$$

$$\frac{6}{k} = , \Rightarrow k=6$$

$$\frac{2R}{k_E} = \frac{2R}{6} + \frac{2R}{6} + \frac{2R}{6} \Rightarrow k_3$$

NMOS  
 $R \leq 2R/k$

$$\frac{R}{k} + \frac{R}{k} = R \Rightarrow \frac{2R}{k} = R \Rightarrow k=2$$

### RC delay model

$$\text{case 1} \rightarrow \text{factor}, t_f, t_{fj} \Rightarrow 84 \text{ ps}$$

$$\text{case 2} \rightarrow d_1 + d_2 + d_3 \Rightarrow 36 \text{ ps} < 84 \text{ ps}$$

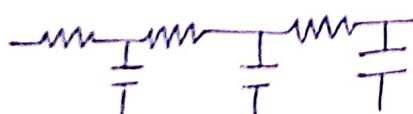
case 3 →

2	4	8	16	32	54
1	2	4	8	16	$\frac{27}{14}$ ps $\approx 19$

$\boxed{\text{RC}}$

### Elmore delay model

→ ON transistor are modeled as resistor  
→ Pullup, Pulldown modeled as RC ladder



Delay components  $t_{pd} = t_p + t_f$

parasitic delay, effort delay

↳ depends on load  
↓

load dependent delay

fan out delay

19-12-2024

→ Effort  
↓  
logical  
electrical

Logical effort  $(g)$  → measure gate

drive strength relative to  
inverter

Parasitic delay

Gate	No. of i/p	Logical effort
NAND	n	1
NOR	n	$(n+2)/3$
Tri-state MUX	2n	$(2n+1)/3$
XOR, XNOR	2n	2

Electrical effort ( $F_{out}, h$ )

Ratio of capacitance of load to  
input capacitance of gate

$t_f = g \cdot h \cdot g$  → logical  $\times$  electrical  
electrical

$$g = \frac{\text{Input capacitance of gate}}{\text{Input capacitance of inverter}}$$

$$h = \frac{\text{Input capacitance of gate (load)}}{\text{Input capacitance of gate (in)}}$$

## CMOS fabrication

- Both n-channel (nMOS) & (pMOS) build on same substrate
- special regions are required to accommodate nMOS, pMOS
  - these regions well (or) tub
  - p-well in n & vice versa

## Steps

1. n-well & channel stop region.
2. Grow field oxide &  
gate oxide
3. Deposit & pattern polysilicon layer.
4. Implant source & drain region  
substrate contact
5. Create contact windows, deposit & pattern metal layer.

## Design Rules

→ geometrical specifications

Layout → Topview

→ stick diagram → dimensions not mentioned.

different masks are made for layers

## need for design rules

Better yield, better reliability, profitability, production Si waffer

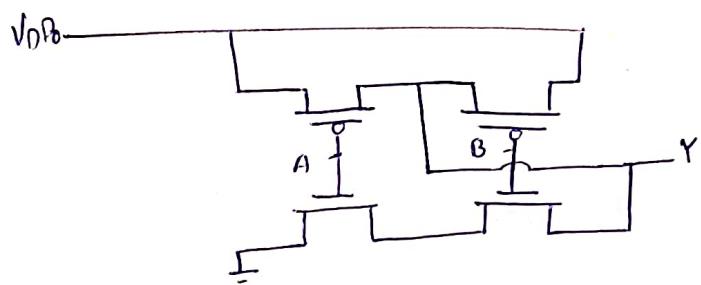
if design rule not followed

non-functional, design large silicon area, can fail functioning

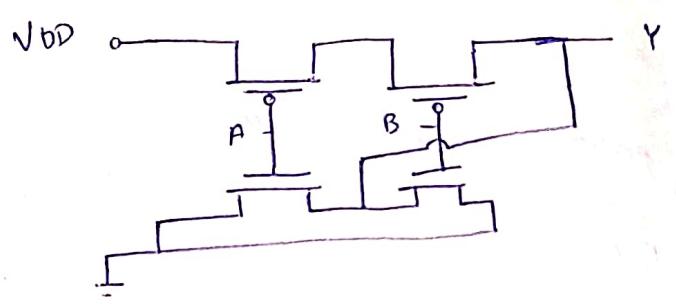
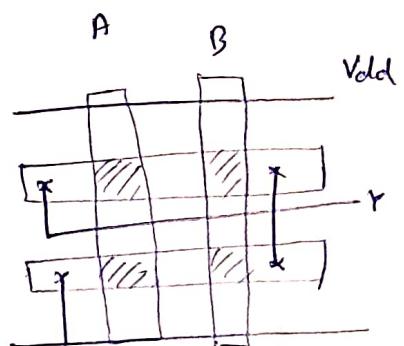
Colour codes → layers

Stick diagram

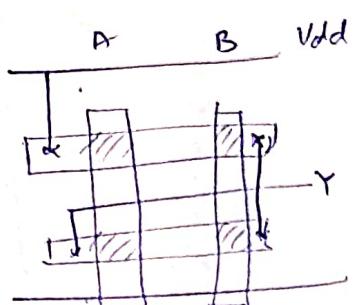
CMOS, Basic steps.



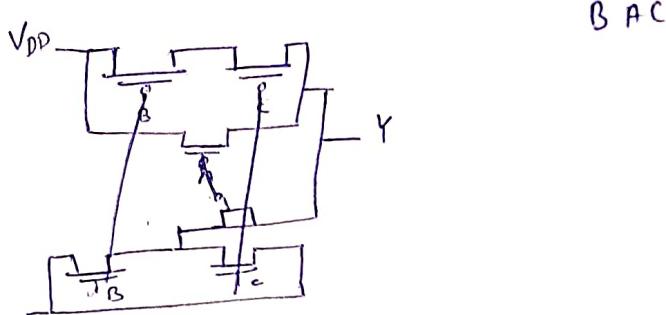
NAND



NOR



EXOR



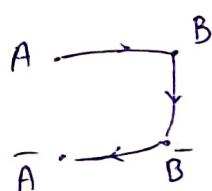
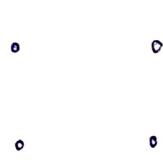
B A C

→ Eulerian path

$$Y = AB + \bar{A}\bar{B}$$

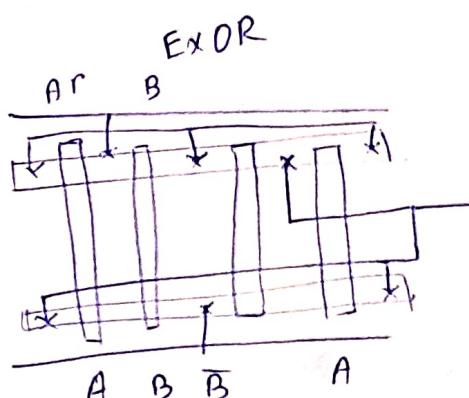
$$= \overline{AB + \bar{A}\bar{B}}$$

→ 4 transistors  $\Rightarrow$  4 nodes.



Eulerian path

$$\bar{A} B \bar{B} \bar{A}$$



EXOR

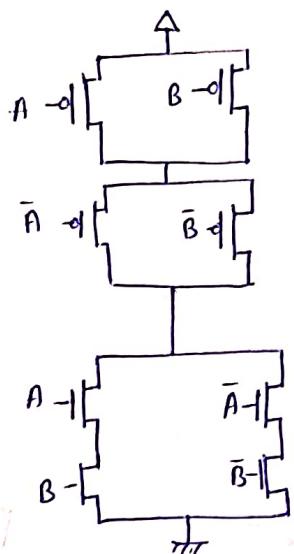
Eulerian path

$$\bar{A} B \bar{B} \bar{A}$$

## Stick diagram EXOR

Step 1 write in whole complement  $Y = \overline{AB} + \overline{\bar{A}\bar{B}}$

Step 2 circuit



Step 3 Draw node

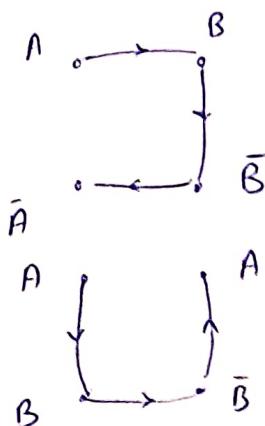
$A$        $B$

$\bar{A}$        $\bar{B}$

$A$        $\bar{A}$

$B$        $\bar{B}$

Step 4 Draw path that traverses through edge only once

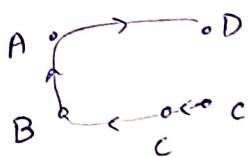
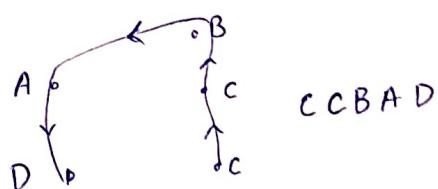
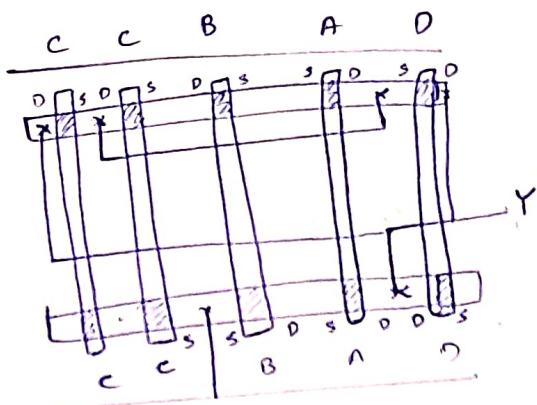
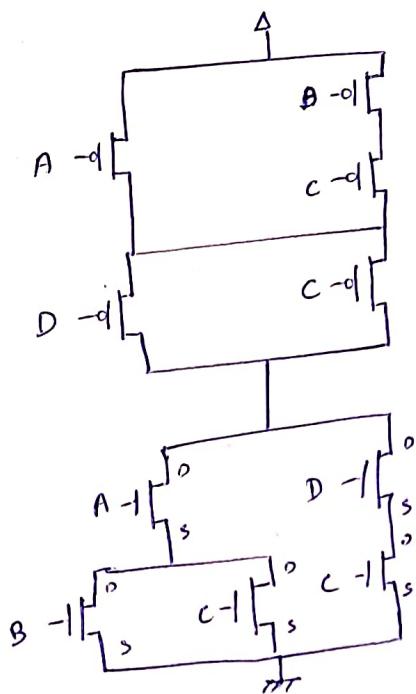


$AB\bar{B}\bar{A}$

path to be same for both pull up & pull down

step 5 Draw stick diagram with the order & connect the source, drain, substrate output

$$\overline{A(B+C)} + DC$$



20.12.2024

## Pull-down & Transmission gate

### Advantages of static CMOS

- Good noise margin

- Fast & low power

- Insensitive to device variation

- Easy to design

- widely supported in CAD tools

- Readily available in standard cell

→ manual circuit design is often done through double pumping

→ complex function with low logical effort.

→ smaller PMOS reduce, power, area & delay.

AOI Gate AND, OR, INVERTER → comparison of different

What makes circuit fast?

- Low resistance

- High current

Pull-down

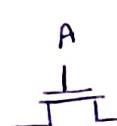
NMOS - strong<sup>0</sup>

PMOS - strong<sup>1</sup>

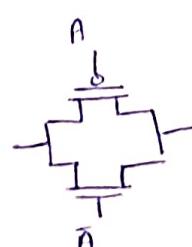
$(A + B).C$

$A + B$

Transmission gate



Level restorer to be used  
for weaker  
weaker



## Multiple file, Microwind - MOS Layout.MSL

21-12-24

### Transmission gate logic

XOR gate & inverter

### Technology scaling

Increased computational power, reduced power consumption, improved speed = performance, cost efficiency, Increased device functionality, enhanced portability & miniaturization.

→ Pno 25°C  
Tidle

### Scaling types

- Constant field, ◦ Constant voltage, ◦ Generalized scaling
  - channel length, → improve performance
  - oxide thickness

(Dennard scaling)

- dopings scaled
  - high power density
  - increased leakage
  - increased thermal issues

Improves speed, reliability

### Scalers influence

- Diminishing returns
- End of Dennard Scaling (BJT)
- Raising fabrication complexity & cost
- Physical & Quantum limit.

Xschem Sky 130

Xschem magic ngspice

Fin FET Technology (Not in Book)

Fin FET is a 3D transistor, overcomes limitation of PLANAR CMOS  
thin, vertical silicon fin, for controlled enhancement. It  
forms channel with gate wrapped around

→ Increase in leakage & gate control

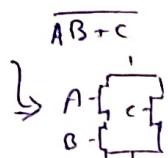
1. New materials

2. New process

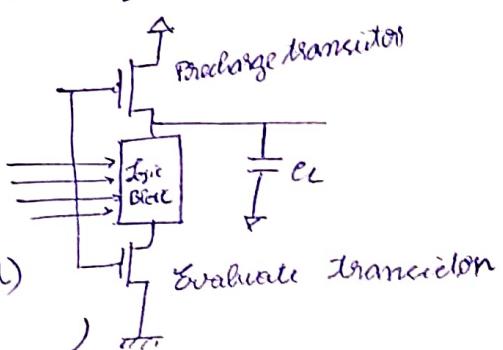
3. New construction

- ultra thin body
- double gate
- nanowire

Dominic Logic Circuits - Dynamic Logic circuits. → (Only pull down)



Dynamic CMOS cannot be  
controlled directly by single clk



NORA → logic

O/p (a static invert required)  
→ Da

⇒ Implements non-inverting logics

Key parameters for Design success

Performance, die size (area), Time to design, Verification & testability.

Design principle

Hierarchy, Regularity, Modularity, Locality.

For LVS

→ removal of voltage source,

. ends } needed  
. end

→ make subcircuit

X1 Vout Vin GND Vdd cmos-invert.

. subckt cmos-inverter Vout Vin GND net1

tb\_spice ⇒

→ edit to have instance <

. tb include cmos-inverter.spice

XVI Vin XINV AB Vdd GND cmos-invert.

.end.

22-12-2024

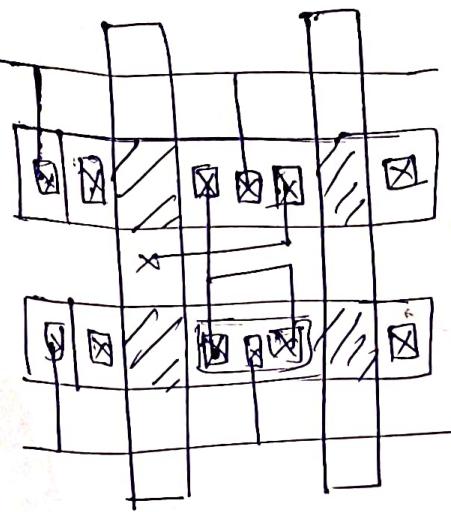
Memory architecture

Word line, bit line to access, types

SRAM, DRAM

not process compatible with CMOS

with CMOS



Memory cell 6T

VDD

GND

A

B

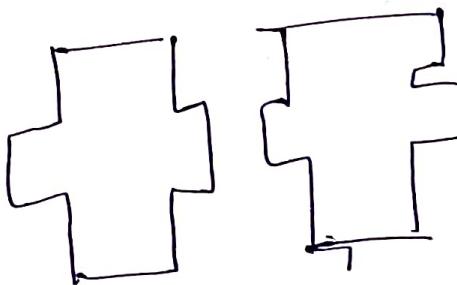
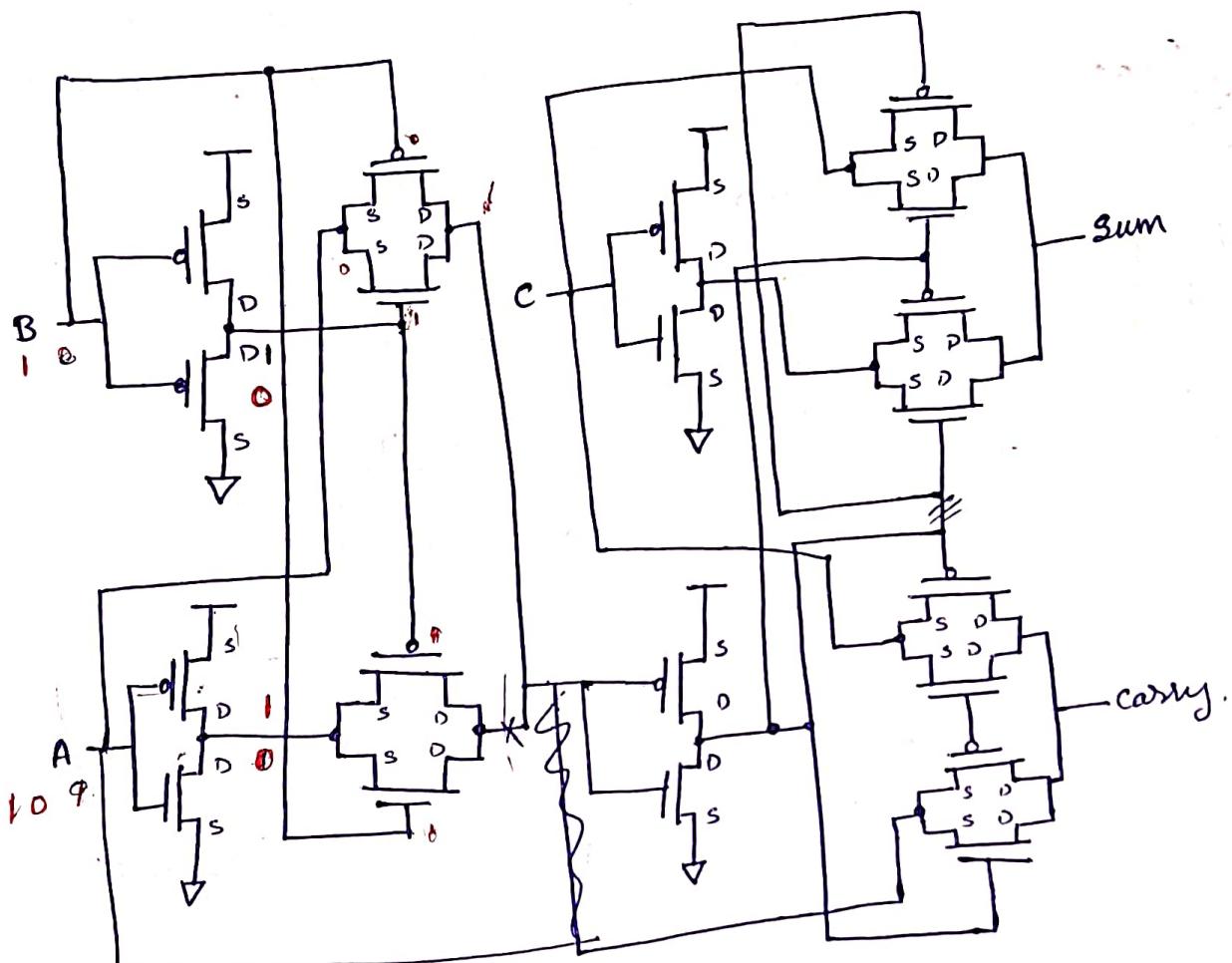
$c_{in}$  → full small

$C_{OUT}$  → full Capital



## Full adder.

20 Transistor



A	B	X
0	0	0
0	1	1
1	0	1
1	1	0