05-12-2024

Mock Interview

```
always @(posedge clk or negedge reset) begin
    q_out <= !din;
end
```

->

```
always @(posedge
```

```
  10010
  01101 ->
      1
+ -----
  01110
```

× default value

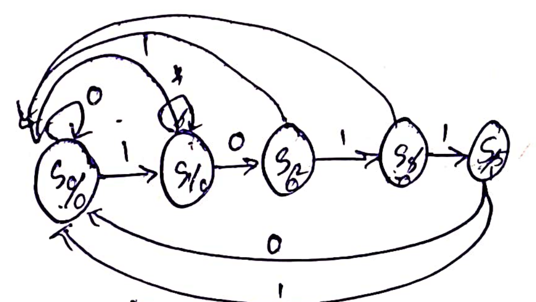
× wire

Reg.

```
class Base;
    function display ;
        $display (" base   ")
end_class
class Derived extends Base ;

    function display ;
        $display (" derived. ");
end class
```

1011 (5) ->



-> Verilog

-> SV

-> UVM

Feedback

-> Confiden ✓

-> Verilog -> Basic default wire reg.

Project

-> protcol -> 6m training.

RTL

DB

DFT

Skills.

Programming languages.

Scripting languages.

RTL design verification methodology : UVM

Protocol :

Synth tool : Vivado, Quartus, YOSYS

Simulation tool : Questa, Verilator,

Experience

Project

Education Qualification

PGDVLSI

Bachelor BE EEE.

→ tool experience

language, methodology

remove, unnecessary.

verification

understanding

⇒ experience

RTL, Design, Verification, Synthesis → UVM, FPGA (Xilinx)

Managing team × Team player → Project.

Electrical Engineer, PGDiploma VLSI, CDAC

⇒ Project (Description)

⇒ 2 only.

Tool | Synthesis | Simulation

Core skill

- - -

Portfolio

Resume → different - Pdf generation
↳ or delete upload

Project & skill update

System Bus

AXI (Adv. extensible Interface) —
CHI (Coherent bus Interface)

—

AHB ->

Memory

SRAM,
DDR, HBM

CSR -> Control & status register

Arbiter.

SoBC

UCI - Universal chiplet interconnect.

PS/2

Gayal
Prathic ->
Harshit
Charan → the Indian
Trivath -> no-eye contact with all
Kanhtu
DOGE ×
Omkar -> 'AR'
Poorwa

DDR [Single, Burst]

PCI, PCIe

USB

NVME

SATA

AXI

AHB

Ethernet

HDMI

Networking

KPI → Power
Area
Frequency.

Nvidia
- grasshopper
- NV link.
Infiniband (Ethernet alternative)

Arbitration (Avoid collision)

PS/2 → Key PS PS/2 Keyboard /

PAM4 → Signals

BOBP → CAN → Single wire

Storing in memory.

Design for testability.

Race condition
→ sampling & update

FSM - 3 logic block

assertion → system verilog constraint.

δ-cycle → delta cycle

Visualizer ⇒ wlnf.
gdb → to be used.