2	3	7	8	4	9
4	9	9	4	6	1
8	7	3	2		
6	1	1	6		

Boat

Downstream speed (D) - Speed of stream + Boat speed

Upstream speed (U) - Speed of stream - Boat speed

Speed of boat in still water - $\frac{D+U}{2}$

Speed of stream - $\frac{D-U}{2}$

Clock

$\theta = \left| \frac{11m - 30h}{2} \right|$

$\frac{a+x}{b+x} > \frac{a}{b}$ iff $a<b$

Mixture

$P \times \left[1 - \frac{R}{P}\right]^n$

P - pure
R - replacement
n - no of replacement

CI

$A = P\left(1+\frac{r}{n}\right)^{nt}$

$CI - SI = 3\frac{PR^2}{100^2} + \frac{PR^3}{100^3}$

AP

$a_n = a + (n-1)d$

$S_n = \frac{n}{2}[a + a_n]$

GP

ar^{n-1}

$a(1-r^n)/(1-r)$

n - natural numbers → $\frac{n(n+1)}{2}$

n - odd numbers → n^2

$^nP_r = \frac{n!}{(n-r)!}$

$^nC_r = \frac{n!}{(n-r)!\,r!}$

All possible combination of words with letter given taken all at a time

$\frac{n!}{n_1!\,n_2!\ldots}$

n - no of letters
n_1 - no of time first repeat
n_2 - no of time sec repeat

Propability of getting 53 Sunday 1/7 normal year 2/7 leap year.

Perfect number 6, 28, 496 ... sum of its prime factor.

Twin prime $((6n-1), (6n+1))$ → except (3,5)

Verilog

gate level modeling not preferred
VHDL

evaluated RHS - Active region
update LHS - NBA region

PAIN ORP

$display - active
$monitor - reactive, postponed
$strobe - postponed
assign - Active
Blocking - Active
#0 - Inactive
primitive - Active (evaluated)

3-FF
$q\_out = t_2$
$t_2 = t_1$
$t_1 = d_{in}$

2FF
$q\_out = t_2$
$t_1 = d_{in}$
$t_2 = t_1$

1FF
$t_1 = d_{in}$
$t_2 = t_1$
$q\_out = t_2$

time - 64 bit
integer - 32 bit
realtime - 64 bit
real - 64 bit

function - one (or) more inputs
- blocking assignments only

table → non-synthesizable

$setup (D1, clk, tsu);
$setuphold (Oreference_event, dataevent, tsu, th);

Race condition avoided using NBA

=> full connection delay
=> parallel connection delay

Assign - continuous
Always - concurrent

nmos (out-pin, d_in, control_signal)
cmos (out_pin, d_in, control_p, control_p)

0-9 mod10 counter

buff (out, in) i/p x/z → o/p x

wait
↓
level sensitive

@ (posedge)
both
0 → (x,z,1)
level, edge (x or z) → 1

#(delay)
#(rise, fall)
#(rise, fall, turn off)
#(min : typ : max)

== with x & z
↳ output 'x' if i/p has 'x'

Operator precedence - Arithmatic, Relational, Equality, reduction, logical, conditional

/ 1
Unary Binary
+ - ! a (* % + -

System Verilog

Interface in Module, program
Program in module (read only)
(rea)

Declaration spaces, - where each can be initialized & exceptions

function can have output & inout
- should have at least one input
- executes in zero simulation time

input - changes taken in
output - changes drive out
inout - both ways.

fork ... join varieties.

packed [ ] <var[ ]>, unpacked <var>[ ][ ]
↳ recomended only to be used in sim

associative array [*]
-> exception class object

get(), peek() -> blocking

program -> Reactive region

integer, int ->
↓ 4state ↓ 2state

Virtual interface -> to connect with classes

test bench structure. formal verification assersion, property, implication operators

polymorphism
compile time - overloading
run time - overriding (class)

Subsequent cycle <- |=> -> non-overlap
Same cycle <- |-> - overlapping.
[*5] - 3 cycles
- delay.
##[:]
for to

mailbox #(type) name = new(size);

and, or, intersect
within
constrain dist {100:=1, 200:=2}

BA, NBA -> Synthesis.

Assertion evaluated - observed
sampled - pre-pond

Event queue

class is -> public (default)

UVM

p- sequencer- userdefined UVM_MEDIUM - default verbosity

m- sequencer- generic

build_phase } - top-down
final

reset, config, main, shutdown } parallel

driver - active component

static components - DUT, Interface TLM 2.0 socket

cpredo - middle ?

_do sequence rand_send

create
start
rand
finish

analysis import → broadcasts

→ create, send, start, finish

factory override cannot be done on components

Subscriber . analysis_export sequence_item → transient entity

HDLSS

No of registers with BA

NBA to avoid Synth Sim mismatch

GDS Graphic Database System II

NGD Native generic database → netlist of primitive gates

NCD ~~read~~ ~~contain~~ data

UPF unified power format

UCF user constraint file

ISE Integrated Synthesis Environment

↓ software

Translation RTL → Netlist Intermediate Representation

DFT, ATPG

light sleep → memory remains ON

Clock

create_clock -period 4 -waveform {0 2}

Clock gating

set_clock_gating_check

Cycle based simulation → glitches are not detected

false path → set_false_path -from -to

multi cycle path → set_multicycle_path -setup -from -to

report_timing

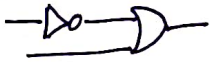
Control path → 2FF level synchronizer, MUX

Data path → FIFO

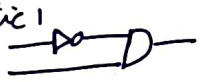
STA, FIFO depth calc

Hazard

Static 0



Static 1



Dynamic

14 ILA, VIO

Clock skew

set_clock_uncertainty

Flattening - Hierarchal to single line

Translation -

Optimization -

HDL → IR → Gate level netlist

↓ Translation ↓ Optimization

Read HDL → Elaboration → Translation → Optimization → Technology Mapping

→ constraint checking → Netlist generation.

CMOS

Avoid IR drop
- Decap
- Power plan
- decrease Metal length

Post Routed Design - Hold is fixed

End cap - avoid damage at end

Abutted design - No gap between blocks

Distributing cells - avoid routing congestion

Search & Repair - DRC remove

Solution to antena effect
- Diode insertion
- more gate area better

Power routing - pre routing -

area of conducting layer to gate area -> Antena ratio

scan chains does not have critical path

uncertainity is more in setup.

cross talk - shielding nets, connect to VSS
- reducing space

NAND - gate preferred during design.

< metal, > resistance

more in number
clk in middle metal

fixed circuit
HARD macro - only timing information, no fn known

SOFT not fixed ckt, timing & function known.

After final routing there can be setup & hold violation, hold fixed after CTS

Guard ring -> reduce latch up problem, clk buff - better drive strength

CTO - buffering, gate sizing.

better timing
↳ LVT used, HVT not perffered

Logical DRC avoid shorts info

Reduce dynamic power - reduce voltage during, reduce load capacitance

wire model of transistor, resistors & diodes.

$\beta_p/\beta_n = r$
r>1 high skew > ON time
r=1 unskew
r<1 low skew > OFF time

Pseudo NMOS - PMOS gates pull up

Domino circuit only non-inverting

Sizing
PMOS - k -> $2R/k$ + ... = R
NMOS - k -> R/k + ... = R

DRAM - precharge

SRAM fabricated with CMOS 6T-memory cell

Logical Effort
NAND (n+2)/3
NOR (2n+1)/3

Flash memory hot carrier

PMOS V_t -ve NMOS V_t +ve

const V scaling
- improve performace
- improve power density
- increase leakage thermal issue

field scaling (Denard scali
- channel length
- oxide thickness
- doppping
+ improves speed & reliability

DIBL - Drain Induced barrier l
tf - max current density
lef - capacitance table
Buffer - decrease dela
HVT - reduce static
LVT - better timing power
Halo - buff & ino
macro - placed on corne
cell to IO
CTS - 0 clk skew
@placement ↳ NO AOI cell
↑
HFNS - load balance
BIST - manufactur fault

global skew - diff between shortest path & longest path.

clk gating - reduces dynamic power
- use isolation cells

CRPR - Clock reconvergence pessimism removal

Jitter deviation of clk from ideal positi

light sleep -> Memory remains ON

Soft blockage - only inverter & buff

PFDV

Template class, RTTI

Vector

Queue

auto - stack - garbage value

extern - } data section 0

static - } data section 0

register - CPU reg - garbage value

nl, wc, diff, grep -v -> exclusion

-w -i

-l -R

-c

? - exit status

$ - last value

Set { } -> not indexed

List [ ]

Tuple ( ) - immutable, order

Dictionary { }

15.4 Zigbee
15.7 Lifi

System Architecture

0 uni, 1 multi, ff broadcast

MAC - 48 bit

CISC 8028T - FPU

Superscalar - 2 instruction per clock

Branching, Jump Policy

VLIW - Very large instruction word

DRAM - precharge, refresh

SRAM - fabricated along with CMOS - 6T

PCI-E voltage

CXL J

SLI → NVIDEA Link

Compute express link

6.0 → PAM 4 3.3 V

↳ Pulse amplitude modulation

x 1.0

↓

500 MB/s

QoS → Virtual Channels

→ Traffic Class.

e 110 → 2.5 GT/s 250 MB/s

PAM4

PCIe 6

GDDR 6

400G → ba

USB

PID - 8 bit, ADD

low speed D - 1.5kΩ to Vcc

high speed D + 1.5kΩ to Vcc

differential signaling

NRZI → PAM4

Ethernet

differential signaling : NRZ - I

3 ethernet

802.11 Wifi

15 Bee

z - 1G

ae - 10G

ba - 40G/10

-1T

PAM-4

CD/CSMA/CD

FPGA

DIL - Delay Latch loop

MMCM, Mixed mode clk merger.

PMCD . Phase matched clock dividers

DCM

ILA,

PAM3

GDDR 7