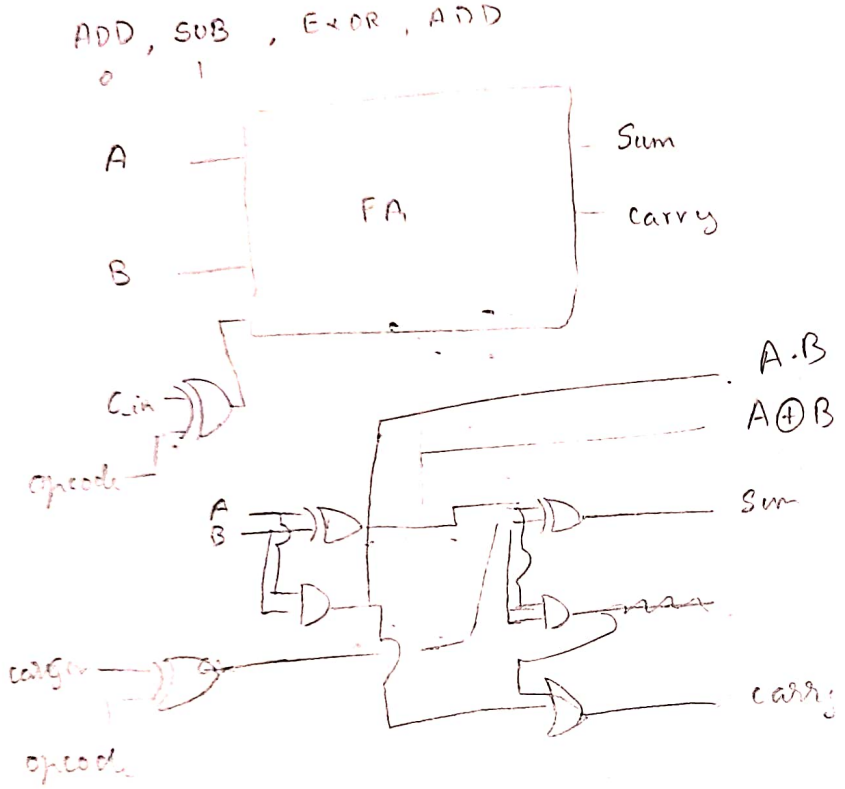
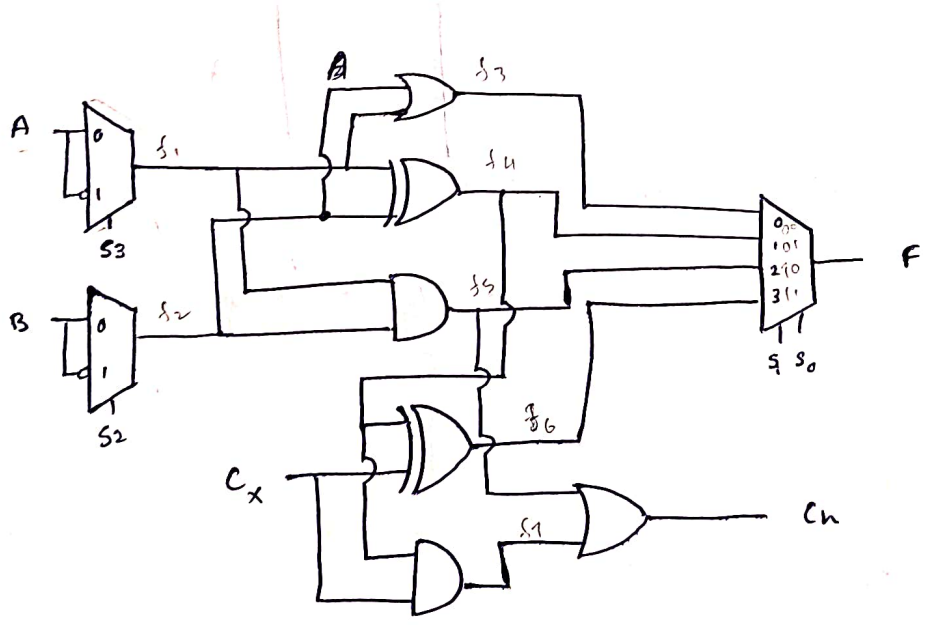
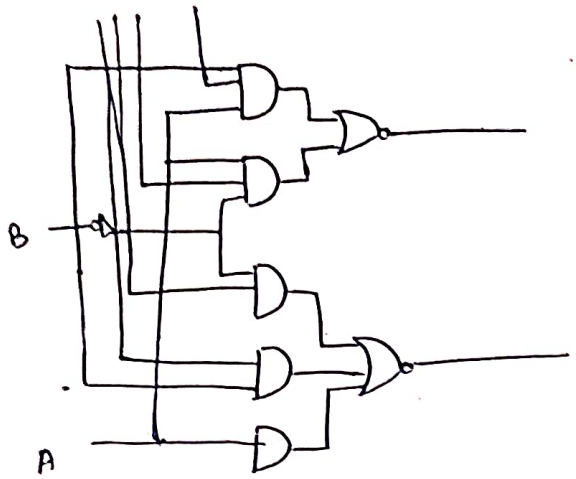
	Text editor	Tools	
	micro	Vivado	IEEE 1800:
open-xc7	VScode	Quartus	VHDL 93
	Sublime text	Yosys	

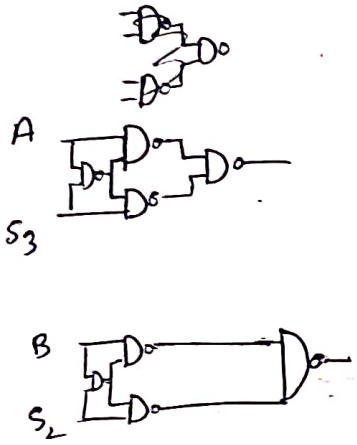
74-181 ⇒ bit slicable ALU

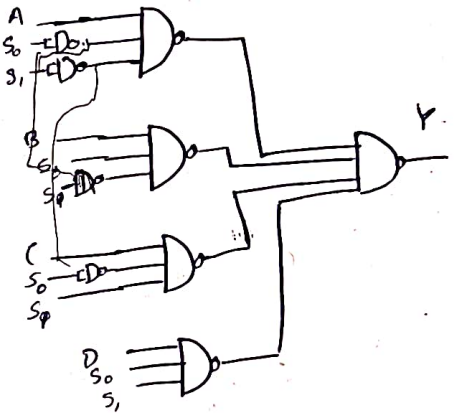




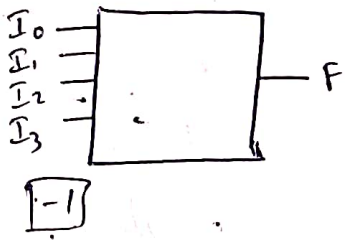


MAX10
ICE40 → LE
Artix → LC





LE → Logic Element



-1 ↓ speed programs.

XC7 ↓ Artix 7

35t → 35k cells
- extension cell within 32k LUT

cgp → package type
238 SMD - 238 pin.

→ 100 MHz

Carry look ahead adder.

$\frac{n}{2}(n+1)$ AND, n OR gate

ALU - 1 bit

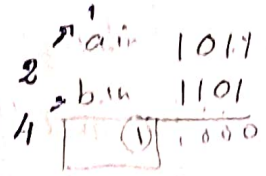
a_in - [+ −]

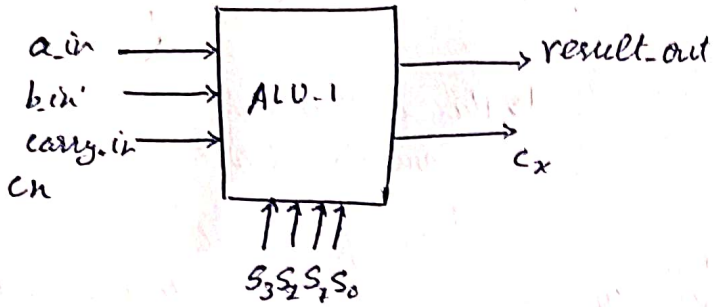
b_in - 1 & 1

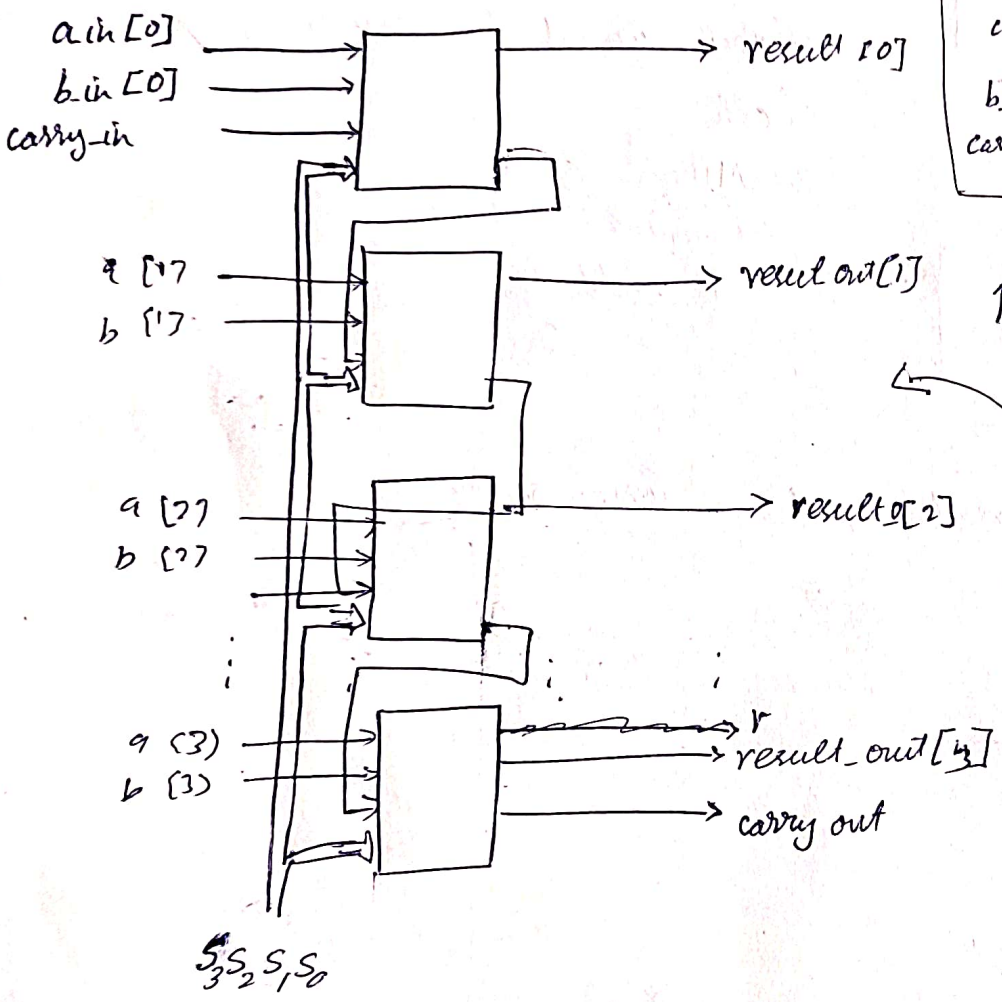
carry_in

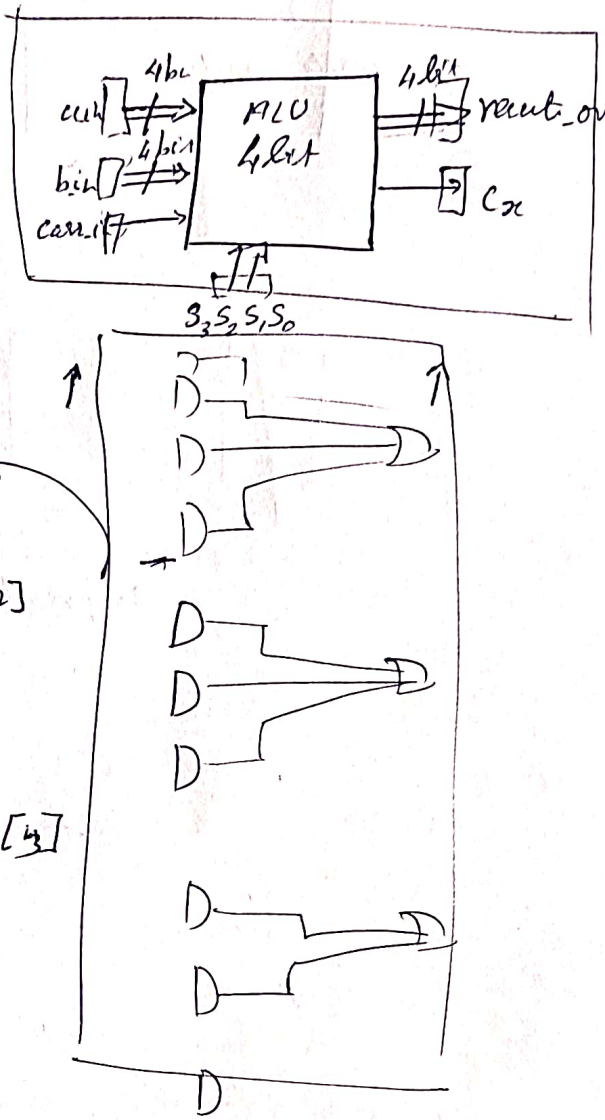
result_out

carry_out









Advantage

→ less time

Disadvantage

→ increase complexity

→ adds more gates to design

→ n - bits

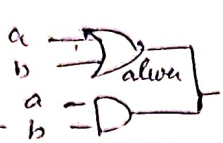
$\frac{n(n+1)}{2}$ AND n - OR

Run Linter.

↳ avoid multidriver.

↳ no-connected nets

↳ latch infer



⇒ ✓ Synthesis

```
reg d_reg;
wire c;
```

Timing constrain file

⇒ Add source → clk.xdc

↳ write constrain file.

↳ generate.

↳ Clock wizard.

→ ☑ clk

→ 200 MHz

→ select signals

→ intial condition.

... ... Finish.

↳ Run synthesis.

Constrain wizard

↳ before finish

☑ view timing constrain

☑ Create timing summary report

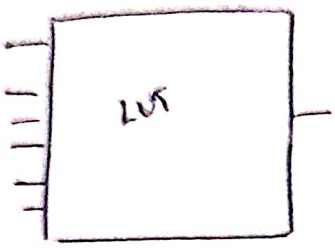
☐

☐

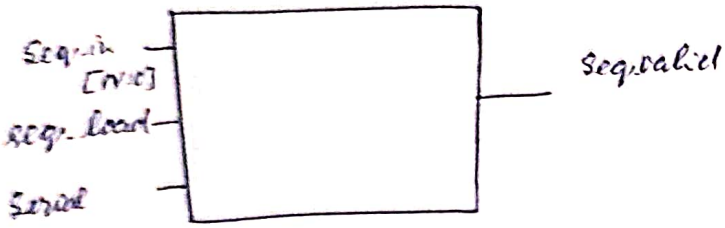
⇒ Generate report ⇒ Timing report

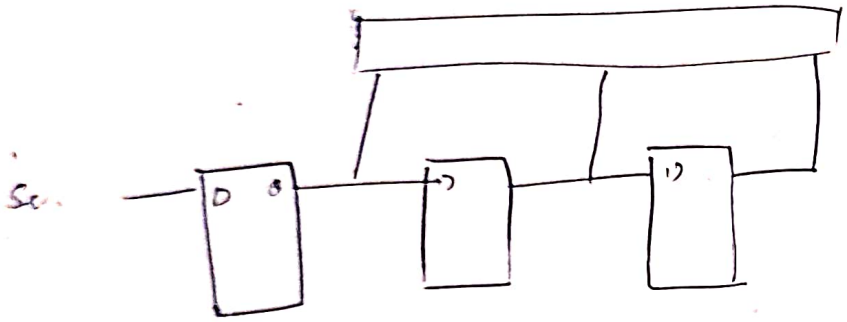
use of case: ⇒ optimise for ALU

LFFR - Linear feed forward register.



Q: 8b





5A5A5A

6×4

0101 1010 ×3

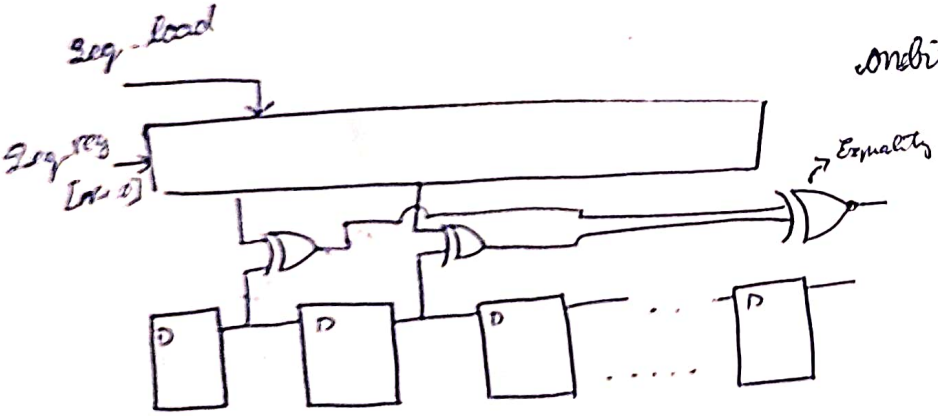
1-
0-

~~x d2~~

x d2 d2 d → 1
0

↓

→



circular right shift.

~~D~~ → 1
[DW-1]

↓ glitch → cross coupled NAND inverter.

$I_b = 0$

BJT ⇒ oscillate

$I_g = 0$

MOSFET ⇒ stick
to a stat

9.19.1

(a) transitional state $\begin{cases} 0 \to 1 \\ 1 \to 0 \end{cases}$ $\Rightarrow$ floating — NO internal PULL UP / PULL-DOWN resistor in FPGA gates

MOSFET $\Rightarrow$ can be used to implement

but, generates impulse response. $\mapsto$

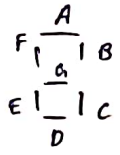
VHDL $\Rightarrow$ 9 state variable.

Verilog $\Rightarrow$ 4 state variable $\Rightarrow$ That cannot account for floating state in a BJT

$\hookrightarrow$ commercial design the use MOSFET so does not have to account for.

Metastability avoided by registring o/p

BCD $\Rightarrow$ 7 segment.



	B_3	B_2	B_1	B_0	A	B	C	D	E	F	G
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	0	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	1	1	0	0