17.05.2024

Digital Electronics

HEX	Decimal	Octal	Binary
		0	0
0	0	1	1
1	1	2	
2	2	3	
3	3	4	
4	4	5	
5	5	6	
6	6	7	
7	7		
8	8		
9	9		
A			
B			
C			
D			
E			
F			

(eg)

Weighted code — BCD (Binary coded decimal) → Each decimal digit represented by 4 digit binary number

Non-weighted code — XS-3, Gray code
- XS-3 (Excess 3) → sequential code, self-complementing code
- Gray code → cyclic code

- BCD
  0 → 9 [0000 → 1001] weights 8421
- XS-3
  Decimal → BCD $\xrightarrow{+0011}$ XS-3
- Gray code
  Binary EX-OR of next - next bit vice versa

K-map.

INDMBK

Adder, subractor, BCD -> Excess-3, Parallel adder, Subrator.

Encoder, decoder, musc

Latch, Flipflop

Combinational & Sequential circuit

Register & counter

maven -> ping design, verfication

9-10 -ram

C-digital

AND , OR , NOT ->

parity generation

Mux, Encoder,
- 2->1, 4->1
- Implement Boolean Function ->

- Sequential

Latch, Flip Flop -> T, D
- edge triggering, level
- D

Registers, shift registers, Counter

- Finite State machine model

More machine,

- Timing,
  - -> setup time, hold time (Metastability)
- Maximum operating 'f' of Flipflop
- Delay, probagation delay
  - -> gate delay, wire delay

propabation delay, line delay

Memory

SRAM , DRAM ⟶ Capacitors

↳ Transistors

- require, constant power
- periodic refresh of power
- faster than DRAM
- greater storage than DRAM
- use less power to perform
- low power consumption
- faster access speeds
- used in speed sensitive cache

× less memory capacity

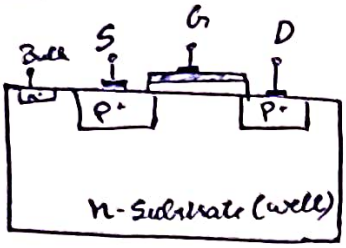
× high manufacturing cost

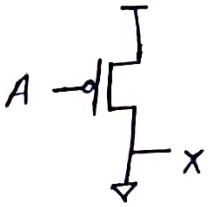
× complex design

main memory.

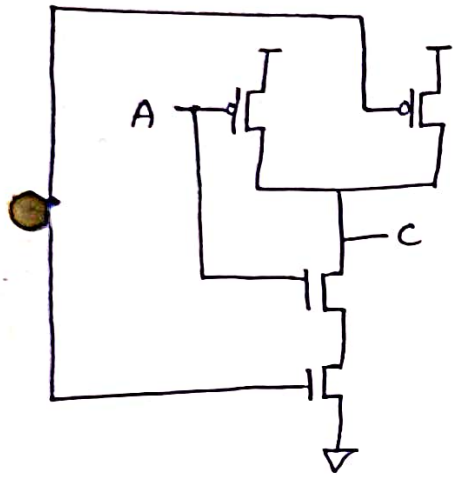
cache,

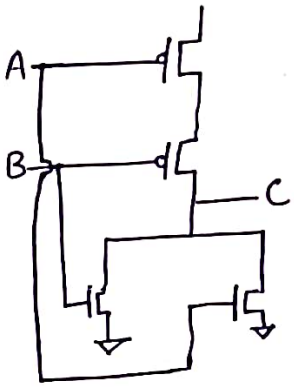
PMOS → polysilicone
→ oxide





A	X
0	1
1	0





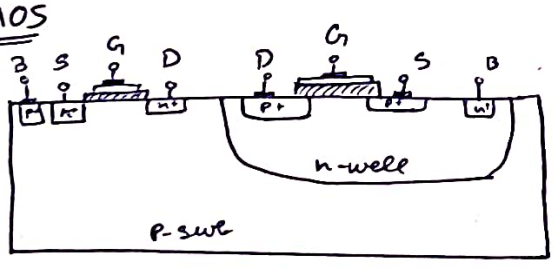
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

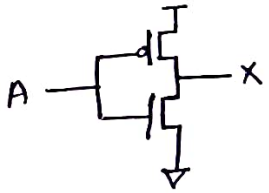
⇒ NAND

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

⇒ NOR

CMOS





A	X
0	1
1	0

Binary → Decimal

00 → 0
01 → 1
10 → 2
11 → 3

1010 → ?

$(1\times2^3)(0\times2^2)+(1\times2^1)+(0\times1)$

$8+2=\boxed{10}$

10010 ↙

$2^4+2 \Rightarrow \boxed{18}$

11011 ↙

$2^4+2^3+2+1 \Rightarrow \boxed{27}$

Decimal → Binary

75 : 2	37 R 1	⇒ 1001011
37	18 R 1	↑
18	9 R 0	↑
9	4 R 1	↑
4	2 R 0	↑
2	1 R 0	↑
1	0 R 1	

Addition → 00 + 01 = 01 ; 01 + 01 = 10 ; 01 + 10 = 11

Subtraction → 01 − 01 = 00 ; 11 − 01 = 10 ; 10 − 01 = 01

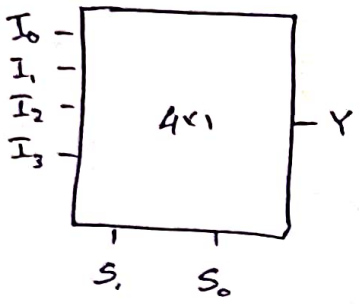
$2' = 1' + 1$

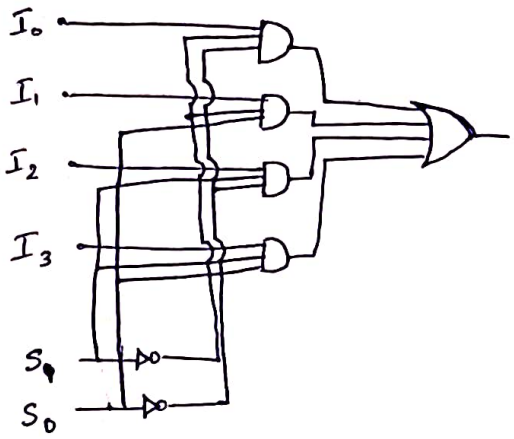
$-(\quad) = +(2's)$

Sign magnitude form 0 - positive

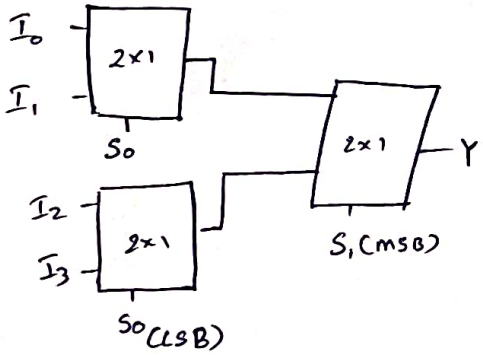
1 - negative

Multiplexer





S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



Encoder

$2^n \rightarrow n$

Octal → Binary

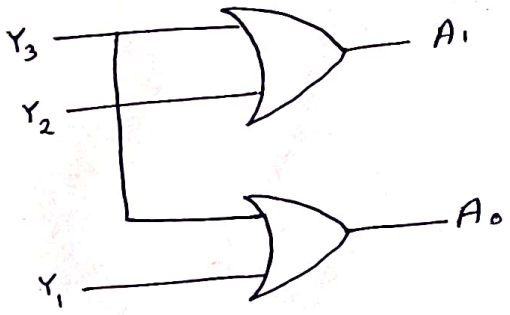
Decimal → BCD

4:2 Encoder

Y_3	Y_2	Y_1	Y_0	A_1	A_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

$A_1 = Y_3 + Y_2$

$A_0 = Y_2 + Y_1$



8:3

$A_2 = Y_7 + Y_6 + Y_5 + Y_4$

$A_1 = Y_7 + Y_6 + Y_3 + Y_2$

$A_0 = Y_7 + Y_5 + Y_3 + Y_1$

Priority encoder

Y_3 -> Highest priority

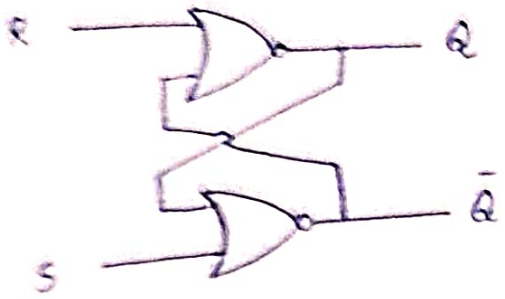
Y_3	Y_2	Y_1	Y_0	A_1	A_0	V
0	0	0	0	x	x	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	01	x	x	1	0	1
1	x	x	x	1	1	1

$A_1 = Y_3 + Y_2$

$A_0 = Y_3 + Y_2' Y_1$

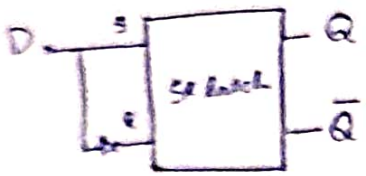
Latch

SR Latch

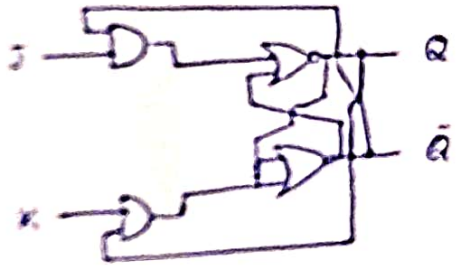


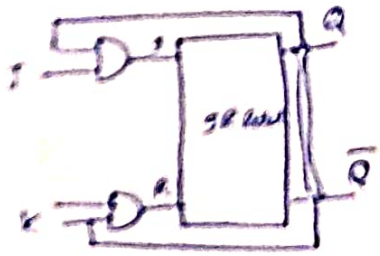
S	R	Q	$\bar{Q}$
0	0	Latch	Latch
0	1	0	1
1	0	1	0
1	1	0	0

D Latch



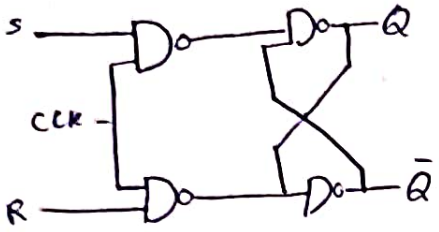
JK Latch





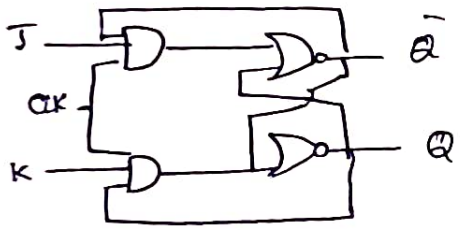
Flip Flop

S R Flipflop



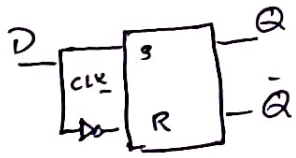
S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

J K Flipflop



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

D - Flip Flop



D	Q_n	Q_{n+1}
	x	D

Types of triggering

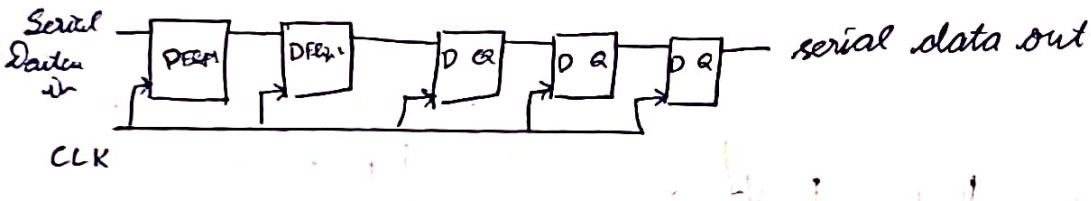
edge triggering ->

level triggering ->

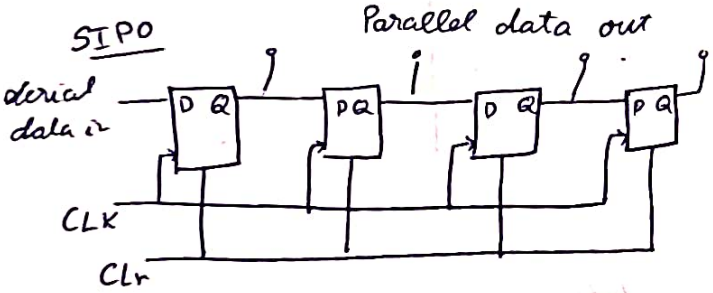
Register, Shift register, counter

- SISO
- SIPO
- PISO
- PIPO
- Bi directional
- universal
- Shift Register counter

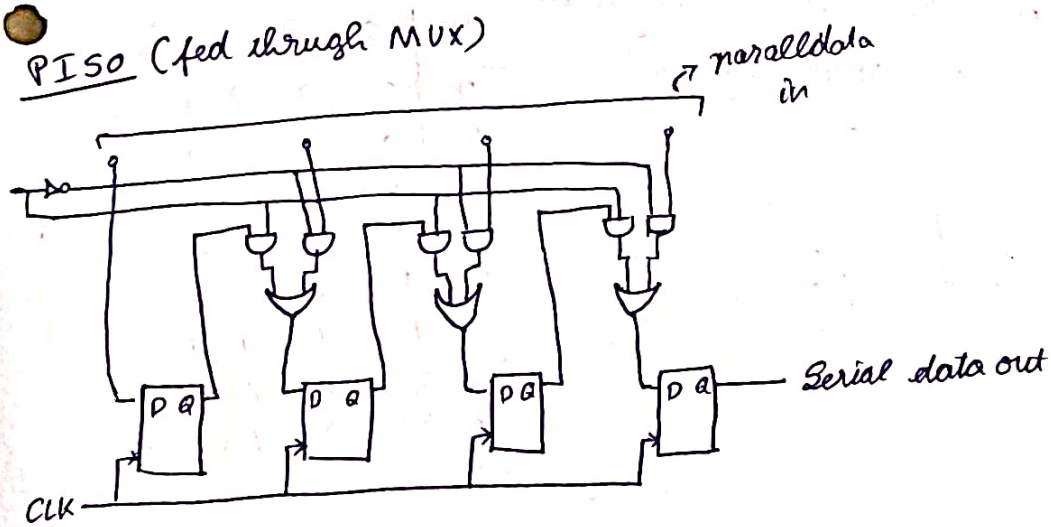
SISO



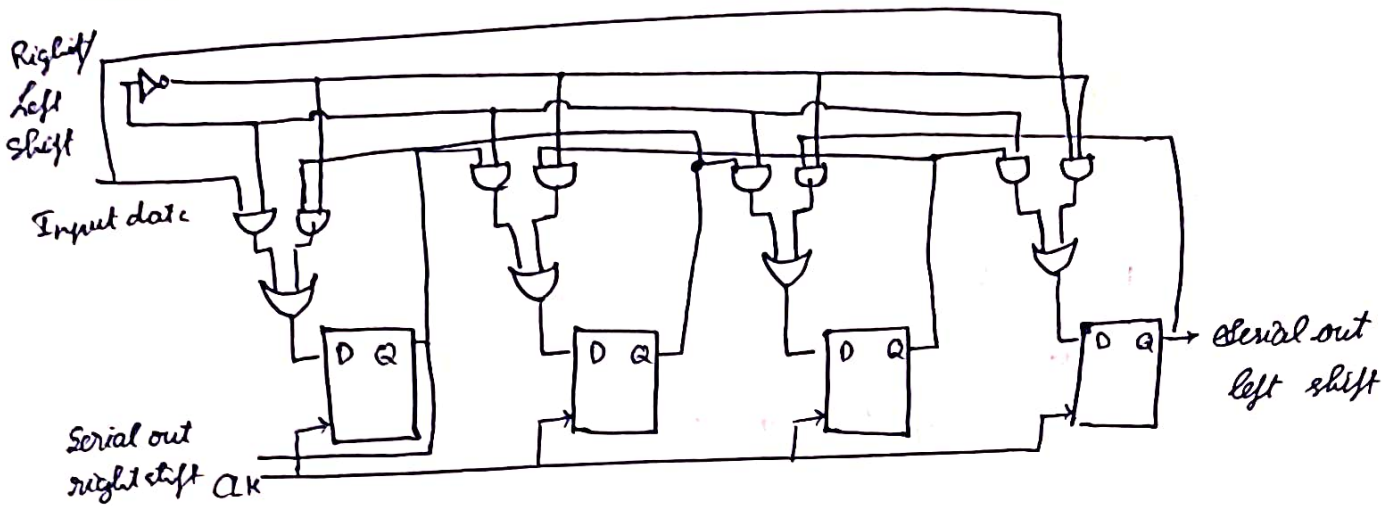
SIPO



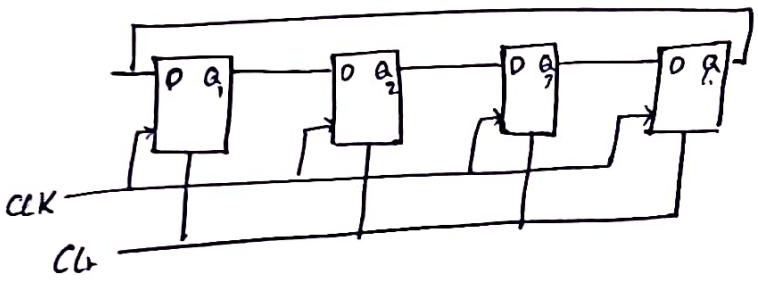
PISO (fed through MUX)



Bi-directional shift register



Ring Counter

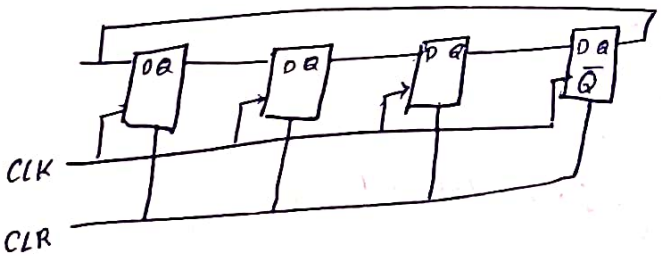


CLK	Q_1	Q_2	Q_3	Q_4
0	1	0	0	1
1	1	1	0	0
2	0	1	1	0
3	0	0	1	1

Johnson Counter

n-stage yeild 2n state

$\overline{Q}$ of last stage feed back



CLK	Q_1	Q_2	Q_3	Q_4
0	0	0	0	1
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1

21-06-2024

Clock

skew - time difference for a clock signal to arive at two different registers

delay - time taken by clock to reach sink from clk source

glitch -

jitter - fluctuations in the timing of clock edges

hold time -

metastability -

Control signal - CLK, Clr

Data signal -

$m \times 10^{-3}$

$k \times 10^{3}$

x

$n \times 10^{-9}$

$f \times 10^{-15}$

Timing

setup time - time duration that input must be stable

hold time - minimum time the input must be stable after triggering of clk

Max f of Flip Flop -

propagation delay

gate delay - circuit component, signal processing.

wire delay - distance travelled, transmission medium

signal speed

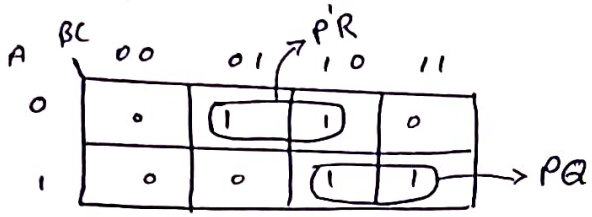
I^2C - 100 kbit/s - standard mode
400 kbit/s - fast mode
1 Mbit/s - fast mode plus
3.4 Mbit/s - high speed mode

Combinational circuit

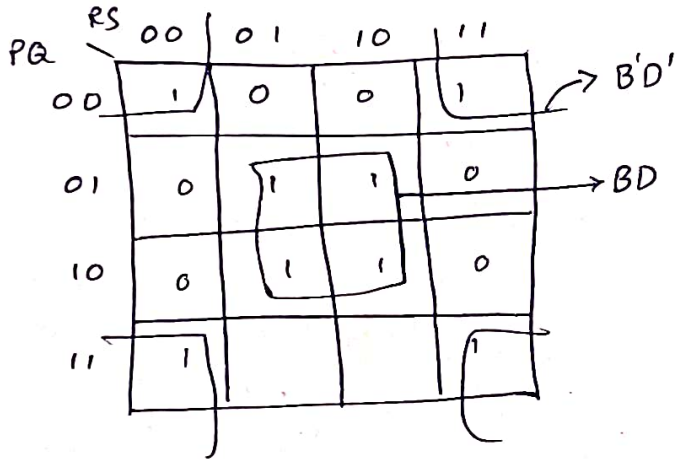
K-map

Sum of products

$Z = \sum P, Q, R (1, 3, 6, 7)$

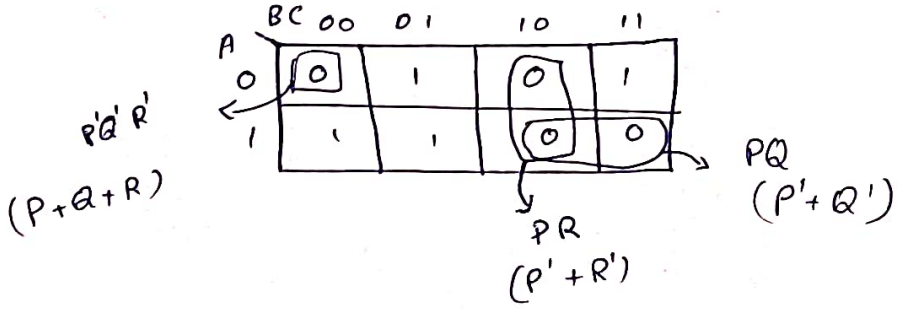


$Z = \sum A, B, C, D (0, 2, 5, 7, 8, 10, 13, 15)$



Product of Sum

F P, Q, R (0, 3, 6, 7)



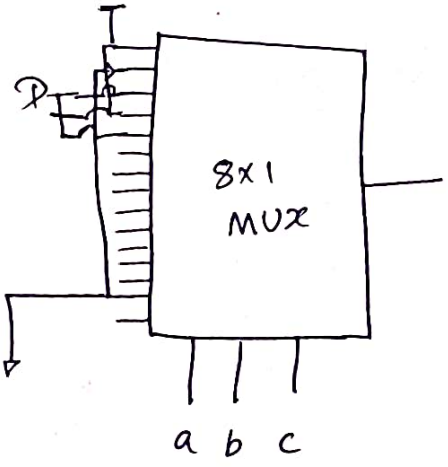
$= (P' + Q')(P' + R')(P + Q + R)$

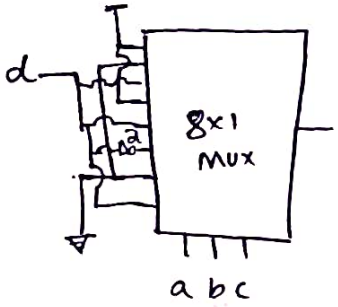
Implement function $f(a,b,c,d) = \Sigma(0,1,5,6,7,9,10,15)$

8:1 MUX a, b, c as select line

a	b	c	d	f_L
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

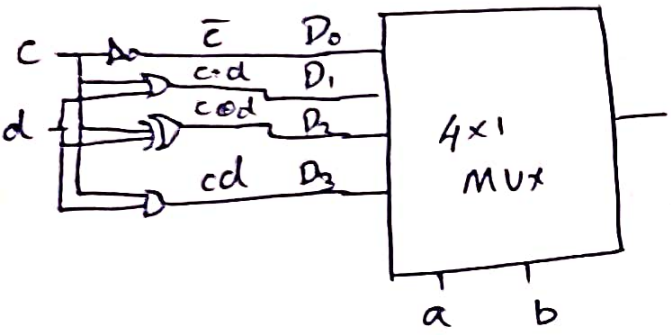
	$\bar{d}$	d	
D_0	(0)	(1)	1
D_1	2	3	0
D_2	4	(5)	d
D_3	(6)	(7)	1
D_4	8	(9)	d
D_5	(10)	11	$\bar{d}$
D_6	12	13	0
D_7	14	(15)	d





$f(a,b,c,d) = \Sigma(0,1,5,6,7,9,10,15)$

d		$\bar{c}\bar{d}$	$\bar{c}d$	$c\bar{d}$	cd	
	D_0	(0)	(1)	2	3	$\rightarrow \bar{c}$
	D_1	4	(5)	(6)	(7)	$\rightarrow d+c$
	D_2	8	(9)	(10)	11	$\rightarrow c \oplus d$
	D_3	12	13	14	(15)	$\rightarrow dc$



Finite state machine

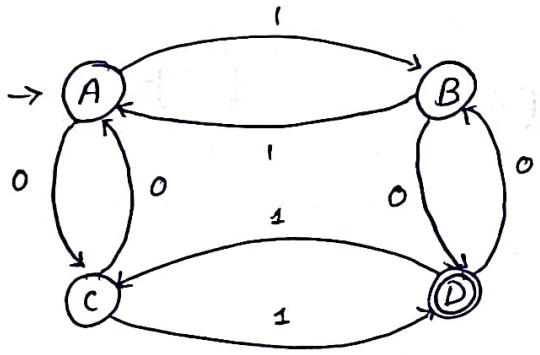
- State Transition diagram
- state table
- State equations

Finite automata

- FA with output
  - Moore Machine
  - Mealy machine
- FA without output
  - DFA — Deterministic finite automata
  - NFA — Non-deterministic Finite automata
  - ϵ-NFA

Deterministic finite automata

Deterministic finite automata



Q - Set of all states — $\{A, B, C, D\}$

Σ - inputs — $\{0, 1\}$

q_0 - start state / initial state — A

F - set of all final states — $\{D\}$

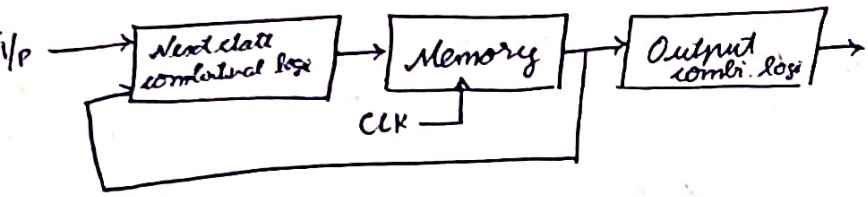
δ - transition function from $Q \times \Sigma \Rightarrow Q$

	0	1
A	C	B
B	D	A
C	A	D
D	B	C

Moore state machine

-> not depended on input

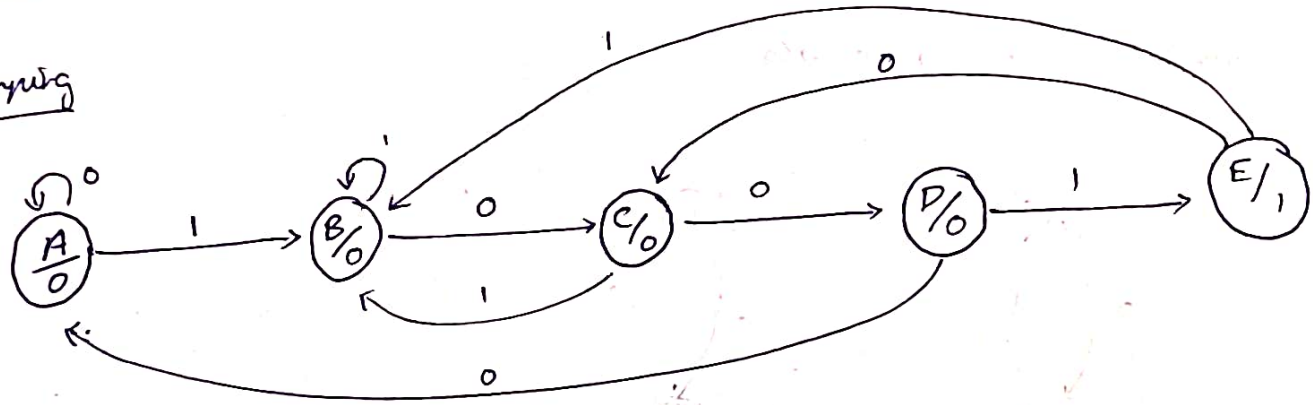
-> o/p is the fn of present state only



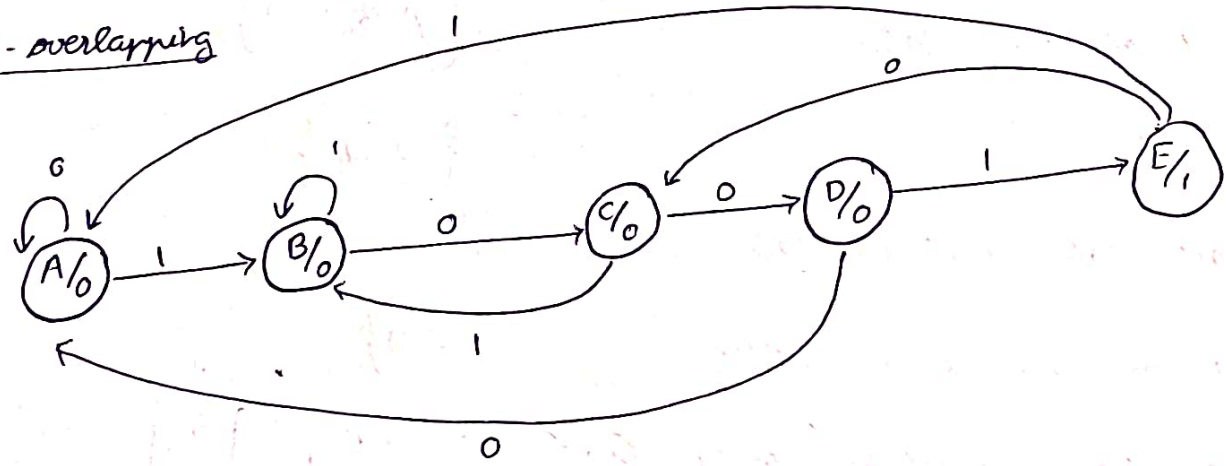
Sequence detector

1001

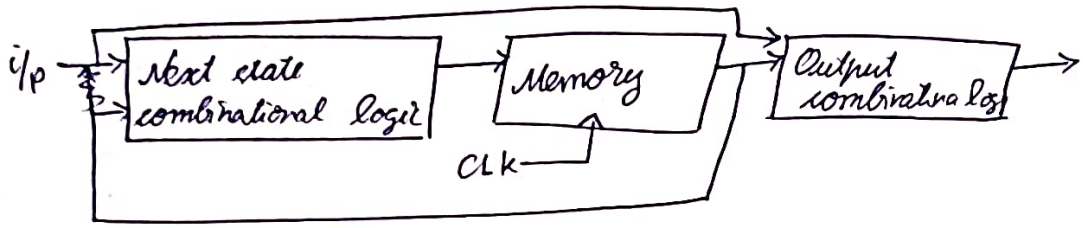
overlapping



non - overlapping



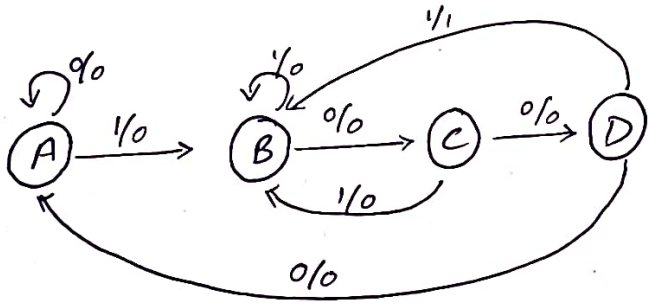
Mealy state machine



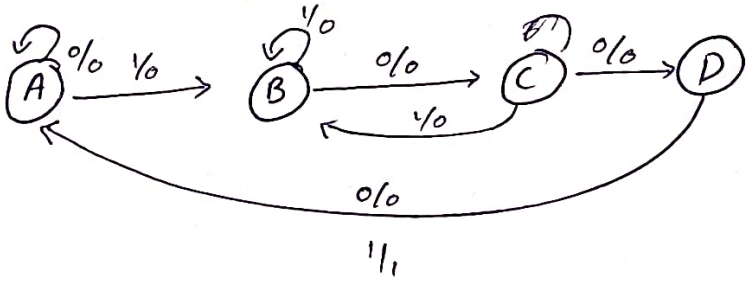
Sequence detector

1001

overlaping



non - overlaping



Maximum operating 'f' of flipflop.

f_{max}

MIPS Architecture

8 bit program counter

add, sub, and, or, slt, addi, beq, j, lb, sb

HDL

Verilog - Civilian

VHDL - Defence

Dot-bus pass over a cell is also used in cell

SPICE model -> not for high complex chip.

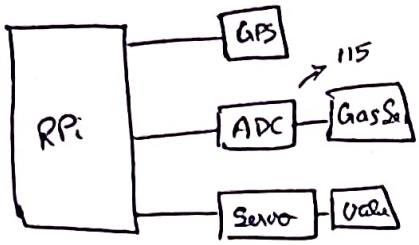
usually functionality tested -> Design rule checker

-> Electrical rule checker

NMOS, PMOS, enhancement MOS, depletion MOS

Threshold, I_D-V_D characteristics

I_D-V_G Transfer characteristics



if Gas sensor > threshold
send notification

if Gas sensor > dangerous value
cut valve.

→ Front end → 7m → 63k → 74k → 59k → 5k

coding →
→ C, C++, C

→ Back end → 6m

desit
→ DSP, PD

Battery, controller

Techning → Repair, →

Voidea →
→ extension.

Full or no load → even with Bt

→ cable, o/p thyristors.

First Visual inspection

1. MOSFET → diagnosis.

2. Relays. →

Embedded

VLSI

Design Test

Verilog

- Verification
- Timing
- Test
- Logic Synthesis

HDL

27

0	0	1
1	0	1
0	1	1
1	1	0

→ NAND

29. $XY + X'Z + YZ$

$\rightarrow XY + X'Z + YZ$

$XY + (X' + Y)Z$ ↘ $Y(X + Z) + X'Z$.

$\rightarrow XY + X'Z$

30. $\bar{A}C(\bar{A}BD)' + A'BC'D' + AB'C$

$\bar{B}C + \bar{A}B\bar{D} + A\bar{C}\bar{D}$

$B'C + A'D'(B + C')$

31 $F(A, B, C, D) = D(A + B) + \bar{B}'D$

21. octal to binary 7263

7 2 6 3

1 1 1 0 1 0 1 1 0 0 1 1

22. sum of binary numbers

$$\begin{array}{r} 11000111000 \\ 00111001111 \\ \hline 11111111111 \end{array}$$

$$+256+128+64+32+16+8+4+2+1$$

$$2^{10}-1 = 1023$$

23.

$2^{'}$ 10101100

01010011

-1

01010010

$64+16+2 = 82$

24. 12547 no of bits required to represent in BCD

16. Group of flipflops, used to store information are called - registers

20. The error in an ADC is often termed as

25. Which of the following is the fastest logic family.

error correcting code.

1 Typical instruction type

- Arithmetic, Branch, Data transfer, Logic & bit-oriented logic

2. Addressing modes

- Implied / Implicit, Stack, Immediate, Direct, Indirect, Register direct, Register indirect, Relative addressing, Indexed Base Register, Auto-Increment, Auto-decrement.

3. Stack - used for storing return address when a functio is called

Stack segment is used to store interupt & subroutine return address register.

Laws of Boolean Algebra

- Commutative
- Associative
- Distributive
- Identity
- Involution
- Absorption
- De Morgan's theorem

Copy constructor →

Private constructor →

Default constructor.

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$	0 (0)	1 (1)	0 (2)	1 (3)
$\bar{A}B$	0 (4)	1 (5)	0 (6)	1 (7)
$A\bar{B}$	0 (8)	1 (9)	0 (10)	1 (11)
AB	0 (12)	1 (13)	0 (14)	1 (15)

$A'D + BD + B'D$

- $\bar{A}C\,\overline{(\bar{A}BD)} + \bar{A}B\bar{C}\bar{D} + A\bar{B}C$

$\bar{A}C$

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

$\bar{A}C(\overline{\bar{A}BD}) + \bar{A}B\bar{C}\bar{D} + A\bar{B}C$

0	0	0	0
0	0	0	0
1	0	0	1
1	0	0	1
0	1	0	1
0	0	0	0
1	0	0	1
0	0	0	0
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0

$\bar{A}\bar{D}(B+C) + \bar{B}C$

0	0	0	0
0	0	0	0
1	0	1	1
0	1	1	1
1	1	0	1
0	1	0	0
1	1	0	1
0	1	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	1	1
0	0	1	1
0	1	0	0
0	1	0	0
0	0	0	0

1. C - set, get Serial Baud

2. D - control

3.