# CMOS Lab

→ ngspice, gaw ⇒ manual

.tf → freqn region.

Voltage source start with V

.tran

.dc

.op

MOSFET $V_{DS}$ $I_D$ ⇒ transfer characteristics. (GAW, ngspice)

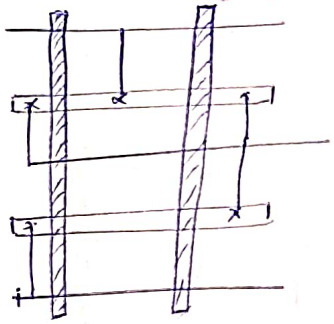
↳ setplot, display.

Inverter W/L

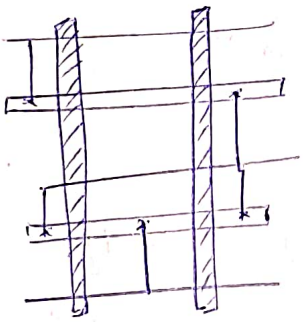
" "

$t_r$, $t_f$ $t_s$, $t_n$

NAND



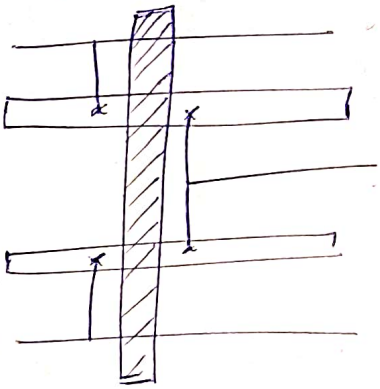
NOR

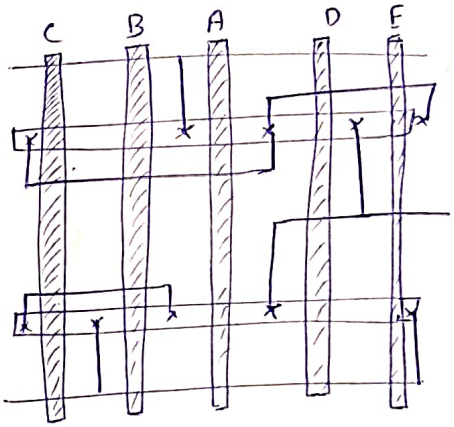


→ magic script

$\overline{A(B+C)+DE}$

Inverter.





## delay analysis.

.tran 0.01n 200n

.meas tran rise_time TRIG V(Y.out) VAL = 0.18 ↗ 10% of 1.8

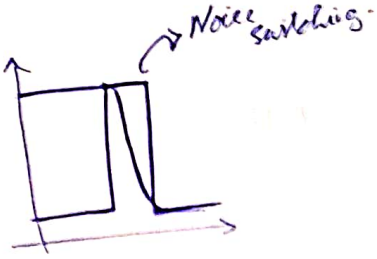
+ RISE = 1 TARG V(Y.out) VAL = 1.62 RISE = 1

fall time 1.62 -> 0.18

tphl ain 0.9 Y-out 0.9

tchl ain 0.9 1.62.

## noise analysis.




gain = (abs(deriv(vout))) >= 1) * 1.8

↳ given change (sudden) ↓ scaling factor

## power analysis .tran 0.01n 40n (add capacitor load)

measure tran current integ Vdd Branch from = 20ns to = 40ns

↳ Integrating current from 20ns to 40ns

$$P = \int_{20n}^{40n} V \, dI$$

→ (gaw)

→ VTC, Noise analysis, delay analysis, power consumption

→ Spice [presentation]

→ NMOS,

VI characteristic.


nmos
VI chara.


plot - Vds #1 branch

dc Vds 0 1.8 .1m Vgs 0 2 .5

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Stick Diagram

Layout

Magic Netlist (spice), ...)

NG spice netlist

Wave form.

Schematic

netlist

ng spice commands.

wave form

• ngspice manual, presentation

◦ magic script [NAND, NOR, INV]

⇓

spice ⇐ test bench ⇒ custom circuit load script.

modular in magic ↵

◦ execute all

⇐ ◦ tcl script.

dump < > name.

erase label-