04-12-2024

HDLSS

Synth tool inferences

- Priority mux, parallel mux
- inference of latch (un-intencional)
-
-
-

Linter

- multi driver
- un-intencional latch
- clock domain crossing

DFT

- ATPG
-
-
-
-

1. Multiplexer using tristate buffer.

```
out = (sel == 1'b0) ? in0 : 1'bz
out = (sel == 1'b1) ? in1 : 1'bz
```

2. Timing statements in Verilog @(posedge <->)
   @(negedge <->)
   @(--)

3. Truncation

a	b	Sum	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

a, b

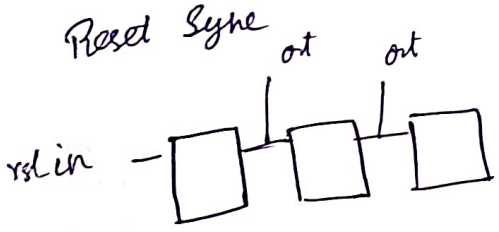
Sum = a+b x → carry will be truncated

{carry, sum} = a+b

0 - 0001
1 - 0010

enum

	sm	
IDLE = 2'b00	2'b00	4'b0000
START = 2'b01	2'b01	4'b0010
RUN = 2'b10	2'b11	4'b0100
era = 2'b11	2'b10	4'b1000



fmax → max operable

fopp → max

min & max delay in logic ckt.

Timing analysis

-> Run Linter

-> Select clock.

-> generate timing report.

Implementation

-> IO Planing

-> Utilization report (synthesis)

Design

Simulation -> Functional

Synthesis -> Behavioral simulation

Implementation ↓

I/O Port mapping -> .xdc

wrapper file

Run Linter

Timing constraint ->

Timing report

-> negative slag

by changing 'freq'

Power report

->

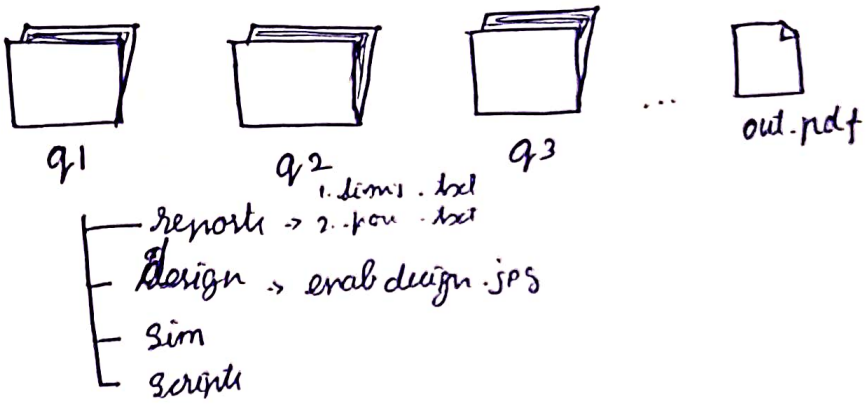
Utilization

10:30 – 12:30

	15 min	question reading
10:45	15 min ±5	design
10:55	10 min ±5	testbench
11:05		report generation, [constraint changing & rest]

→ Task based test bench, $display, always-ff, always-comb

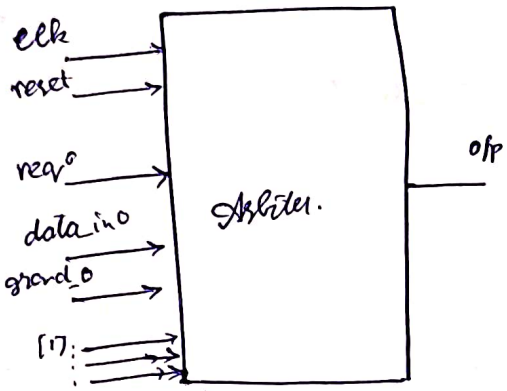
→ Design Patterns.

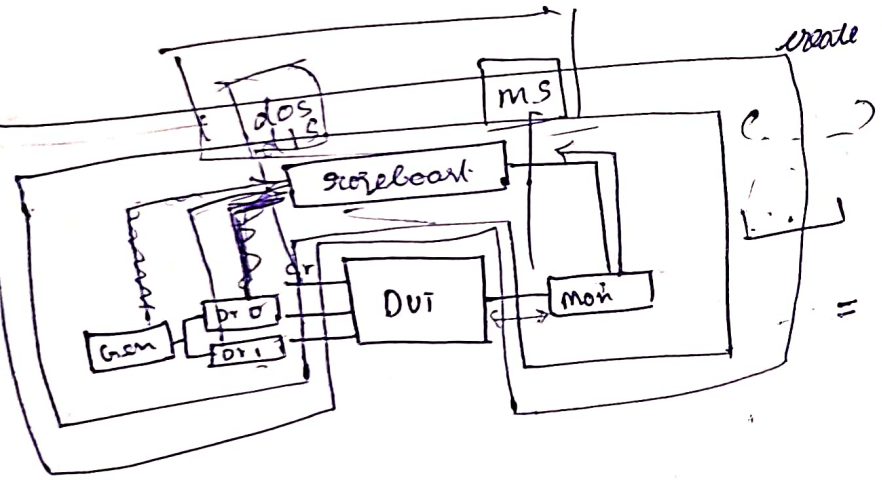


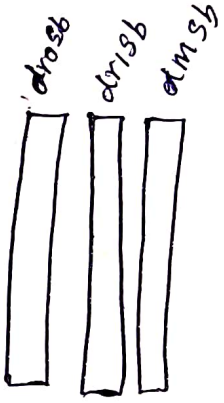
V
oop

- Problem solver.

- fork join ~~any~~ none
- fork join
- fork join any.os.

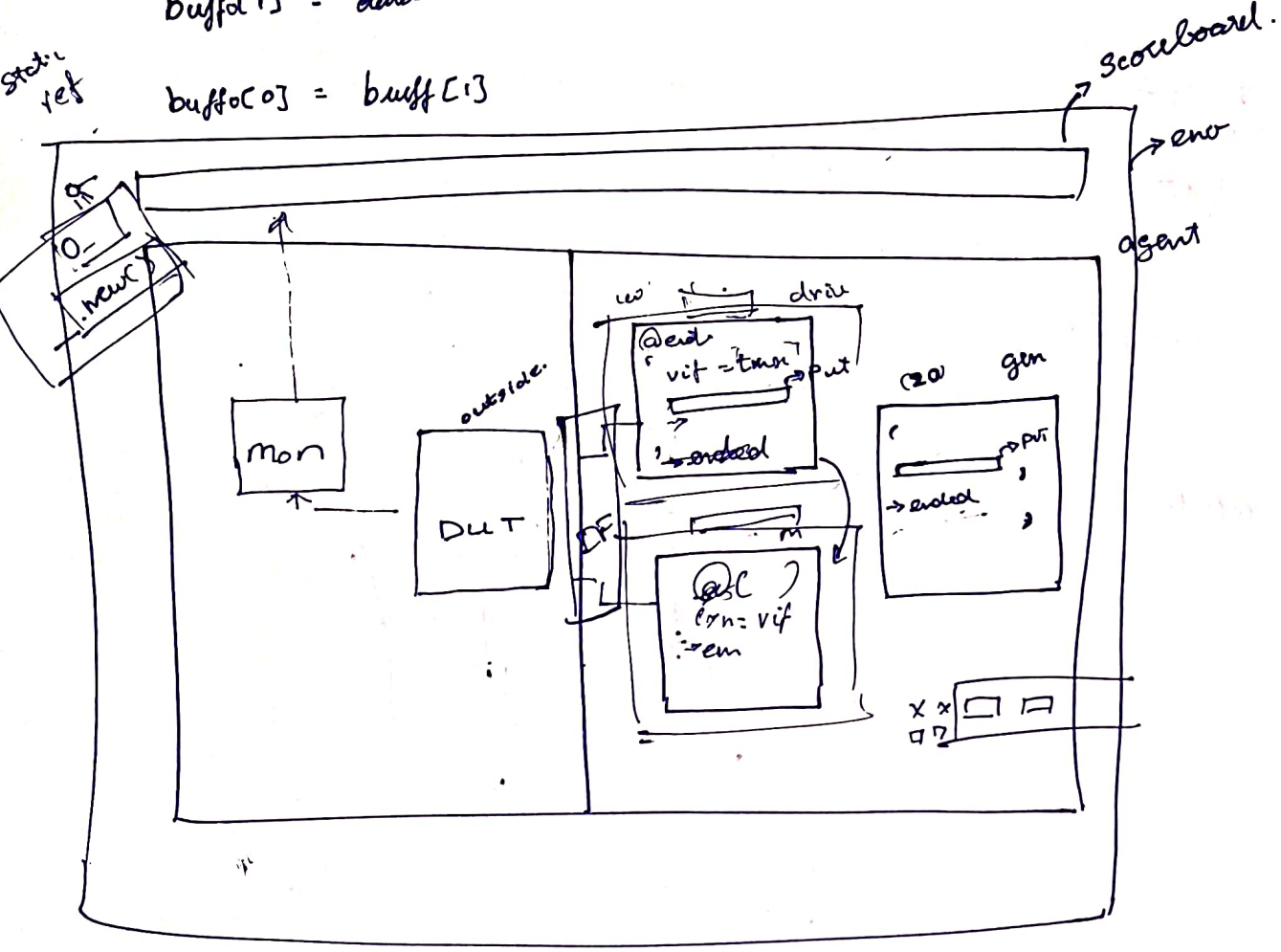


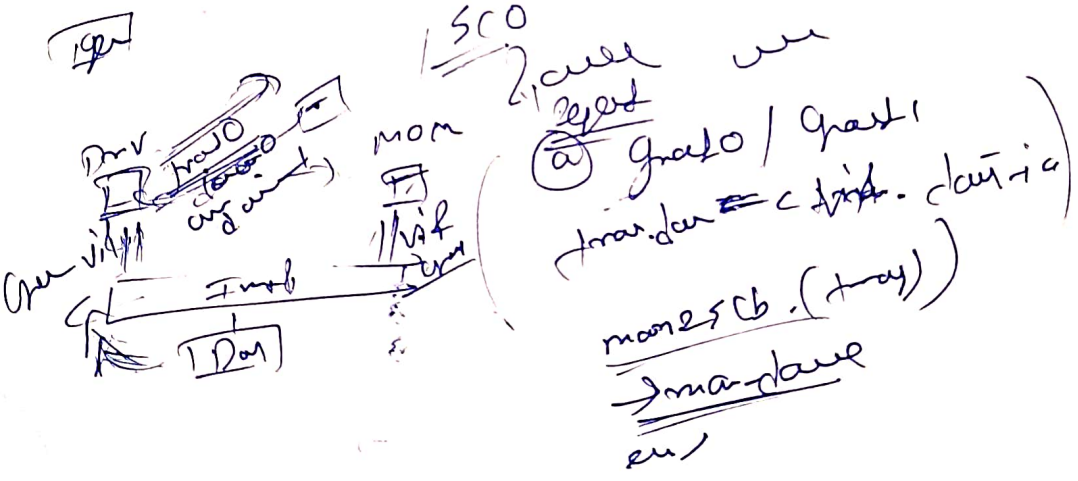




buff[1] = data

buff[0] = buff[1]





Build, connect, run ⇒

name . this.name.

$display ('$time ');

event (or) semaphore

mailbox

virtual interface

clocking