UVM → System Verilog · Base class library

- Connecting Environment to DUT
- Transactions
- Sequence & Tests
- Monitors & Subscribers
- Reporting

-> Constrained random, coverage driven verification

- Transaction level communication, layered sequential stimulus, Standardized messaging, Register layer (adv)

Checkers -> to check expected op reached.

Functional coverage →

↻ Header, payload, checksum.

05-12-2024

Mock Interview

always @(posedge clk or negedg reset) begin

q_out <= din;

end

->

always @(posedge ,

10010
01101 ->
+ 1
01110

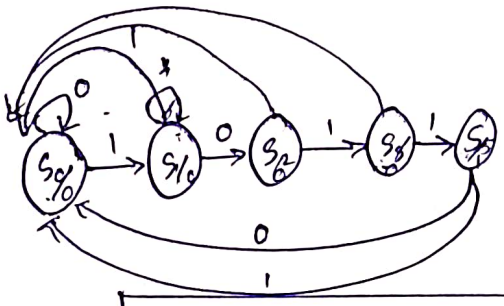
* default value
* wire
Reg.

class Base;

function display >:
$ display (" base ")
end_class
class Derived extends Base;

function display ;
$ display (" derived. ");
end class

1011 (5) ->



Feedback
-> confiden ✓
-> Verilog -> Basic default wire reg.

-> Verilog
-> SV
-> UVM

Project
-> protcol -> 6m training.

RTL
DB
DFT

23-11-2024

→ Vijay

Top Down → rather than opp.

State Machine →

phrasing (finite operator) in compailer.

quintuple

Σ - input alphabet → set of indivisible unit

Γ - output alphabet

S - set of states → history of i/ps - that are relavant

δ - function that maps. $\Sigma \times S \to S$ → cartesian product → set of orderd pair. → maps i/p set to o/p set

ω - function that maps $\Sigma \times S \to \Gamma$

Language.

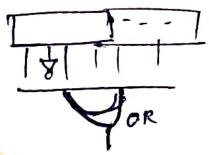
BNF - Backus Naur Form.

grep → global regex parser.

{Fullname ::== firstname, middlename }

firstname ↓ token

Shift Reduce Parsing



Child eats

Child eats an apple

LALR(1)

↳ Look ahead

tokens are shifted in

↓

Rule match } → syntax match, schematic match

↓

Reduce

↳ shift/reduce conflict } context free grammar

reduce/reduce conflict

Sanskrit ?

• Abstract syntax tree

Sanskrit - sound or letter.

Error-correction codes. RS (544, 514)

Cache → LRU
→ MFU
→ FIFO

Galois Fields.

Set → Group → Ring → Field → Polynomial → Vector Space

with, within

07-12-2024

Software for automating tasks. → Synth
→ Simulation
→ GDS error check

Algebra → a set with operation & rules.

Langauge

- Symbols, not-Symbols (empty space)
- Strings, ~~words~~ → meaning full string
- Lexecon – set of meaningful word
- ~~Words~~ Sentence –
- Stanza –
- Grammer → set of rules in a lang
- token – read till space
- pharsing – extracting meaning from it.
  - → Scanner - lexical analyzer.
  - → Lookup engine → Symbol table (CAM - Content addressable memory)
  - → Syntatic analyzer → checks with predefined rules.
  - → Sematic analyzer → checks for valid constructs
  - → AST → ~~ph~~ parsers stores in ←

Program

AT&T → lex
↳ flex GNU
→ yacc →
↳ bison

↳ LALR1
↳ look ahead 1 parser

Bad grammer

→ ambiguity in grammer.

Compiler

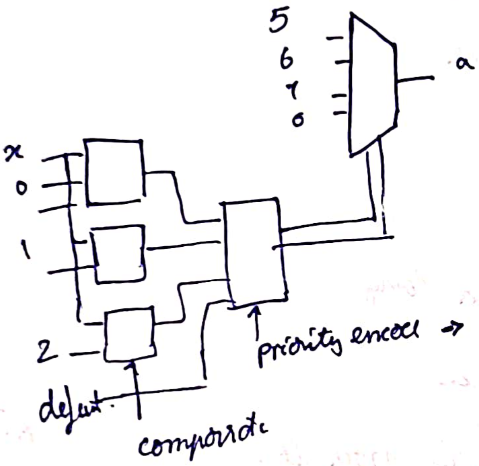
→ translation from one to other   C → assembly
.V → .C

Language.
Lisp → Emacs Lisp.
↳ unambigious grammer

Verilog constructs **Combinational circuit**

assign Y = (a & b) | c;

—
```
if (x==0)
   a<=5;
if (x==1)
   a<=6;
if (x==2)
   a<=7;
else
   a<=a;
```



priority encoder → compare with all least priority before match,

—
```
case (x)
  ---
  ---
  ---
endcase
```

⇒ Infers parallel mux (regular)

Sequential circuit

always @ (posedge clk) ______
↓
Sync / async reset
↓ ASIC (pref)   ↓ FPGA's

use of begin end everywhere → edit code { best case syntax error; worst case error in Silicon.

// comments → why? part to explain

→ don't comment the operation.

function, task

loop → for, generate

class ✗

} → using don't provide 1→1 mapping with netlist inferred, create a layer of abstraction

ECO → Engineering change order (change made to silicon dye after implementation done)

↳ using spare gate, wire

→ Final netlist usually single bit instead of bus [n:0]

DDR [Single / Burst] Networking

PCI, PCIe

USB

NVME

SATA

AXI

AHB

Ethernet

HDMI

KPI → Power
Area
Frequency.

Nvidia
- grasshopper
- NV link.

Arbitration (Avoid collision)

PS/2 → Key PS PS/2 Keyboard /

PAM4 → Signals

BOBD → CAN → Single wire

Storing in memory.

Design for reliability.

FSM - 3 logic Block

assertion → system verilog constraint.

Race condition
→ sampling & update

S-cycle → delta cycle

Visualizer ⇒ wlwf.
gdb → to be used.

Portfolio

Resume → different - Pdf generation
↳ or static upload

Project & skill update

System Bus

AXI (Adv. extensible Interface) —
CHI (Coherent bus Interface)

—

AHB ->

Memory

SRAM,
DDR, HBM

CSR -> Control & status register

Arbiter.

SoC

UCI - Universal chiplet interconnect.

PS/2

Jayant
Prathic ->
Harshit
Charan → the Indian
Trinath -> no-eye contact with all
Ekansh
DOGE ×
Omkar -> 'AA'
Poorva