07-11-2024 System Architecture (Ethernet, FPGA architecture)

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Ethernet IEEE 802.3

LAN, WAN

Network switching
- → Circuit switching - dedicated channel
- → Packet switching - information transmitted in packets.

Network Topologies
- → bus, star, ring, mesh...
- extended star, fat tree / Clos, Hyper cube (→ makes)] Direct & Indirect network
- → 1D mesh, Torus
- 2D
- 3D

Bandwidth vs Throughput
- → header / footer
- → ack
- → error correction

⇓ actual data rate (Carefull)

→ 10 Mbs
→ 1 bit / clk

Ethernet
- → seamless performance (10/100/1G)
- → Price / performance
- → Interoperability
- Scalability.

1500
1024

PAM-4 signaling

Network layers: A P S T N D P — Software / I Hardware — Hardware

TCP/IP: T N
Ethernet: D P

0 → unicast
1 → multicast
ff:ff:ff: → broadcast

MAC
OUI
CDAC
00:A2:22:xx:xx:xx

Hub vs switch

Ethernet Frame

→ switching frequency & voltage of operation.
→ level → Ethernet

10 Base T +2.5 V - -2.5 V
100 BaseTx +1 V - -1 V

CSMA/CD -

TCP → flow control (using acknowledge)

Slot time 512 bits times → [to avoid to <foc collision]

$2^8 \cdot 2$

$\frac{512 \text{ bits} = 64 \text{ bytes (B)}}{10 \text{ Mbps}}$

$51.2 \mu s$

100 giga
→ 448 byte as padding

burst time | 1500 bytes | → max can be

slot time | 512 bytes | → min req

Full-duplex

→ CSMA/CD - no longer relevant (seperate dedicated lines used)

→ flow control needs to be implemention.
→ pau flow control, credit flow contra

Ethernet connector. → RJ45, SFP, ...

Coding → Manchester Coding (10Mbps) '1' '0' select 4b→5b mapping what to choose
→ 4b→5b (100 Mbps)
→ 8b→10b (1 Gbps)
→ 64b→66b (10 Gbps)
→ Running disparity.

NRZI, NRZ-L
reduce transition
maintain balance
→ scrambler or another coding mode at receiver to decode

Auto-negotiating → MDIO, MDC (similar to I_2C) Ma
data clk

Control register. → memory pinning
↳ DMA to map physical address, virtual address.

Switch architecture → crossbar.
↳ arbiter

→ store & forward
→ cut through.
→ worm hole

~~12-11-2024~~.

Programable Logic Device - FPGA

PROM, PAL → PLA

I/O Buff → Current amplifier
↓
unity gain amplifier.

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↳ Functionality can be implemented in → Logic gates
→ NAND (or) NOR gates
→ ROM to model

40 i/ps ⟶ 2^{40} o/p

40 i/ps ⟶ 56 o/p [Implemented in xilinx CPLD]

- 4 i/p LUT ⇒ cascaded to get req i/p

- Faster FPGA tend to slower than faster CPLD for small design

- Interconnects in FPGA
  - Route through logic [implemented by tool]

FPGA vendor ←
Atmel →

Virtex-II, Pro, Pro X ← Architecture.

Virtex-4

IOB → Single ended, Differential, Tristate ⟶ Ground bounce
HP → High performance HD
HR → High range

Single port memory → tristate Buff
→ protection circuit, weak keeper (multi-bus access)

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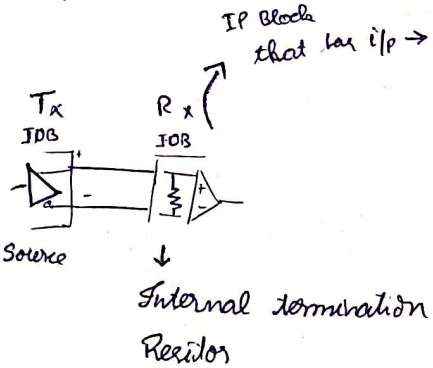
Differential buffer → instantiation to be placed
① → Same bank
② → Adjacent pins (to have high CMRR)



High Speed PCB Design

Nelco, Rogers → instead of Fiber Reinforced

Latch, FF, DDR. → in o/p side

ISERDE 53 ⟶ Bit slip (to begin transmission.)

Configurable Logic Block

SLICE, SLICEM + memory (Distributed RAM / Shift register)

- LUT
- Flip Flop
- Arithmatic & carry chain
- Multiplexers.

→ Relationally Placed Macro

Latch → to be instanciated not by synth tool only.

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→ Morris Manno → Latched design

Block RAM, clocking, DSP, interconnect.

Metastability in → Flip flop → Gates → Transistors → Cutoff ↓ Saturation

Innertial delay & Transport delay.

↓

min time for the gate that signal need to be stable.

36 bit → 1K 32 bit + 4 bit for parity.

↓ one for 1 byte

↳ Tool can infer a Block RAM,

↳ Recomended to use desired macro

[problem with to so design needs to be changed]

↓

macro

⟶ P-block constrain

↓

placement

512 x 44 FIFO →

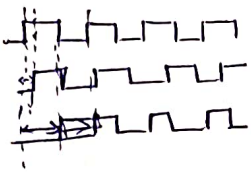
DSP - Digital Signal Processing.

Scaling & addition →

< resource intensive (comparator) used instead
>

MMCM & Blocking

DLL → Delay Locked loop



PLL
↓
recreates clk

DLL
↓
compensate clk
(de-skew)

↓

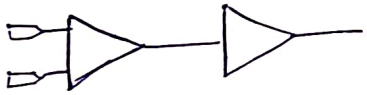
DCM →

↓ Synthesis from clk

PMCD →
(Phase matched clk divider)

↓

MMCM
(Mixed mode clk mgmt.)



POST → at lower clk if OK that need not be high frequency designed.

① →

② → Shifted to higher clk for design.

AC/DC switching characteristics. ⇒ frequency range

- PLL recreates clk ⇒ removes jitter filter.

Routing Matrix

→ Switching elements, delay ⇒ Not known to synthesis tool.

Configuration

FLASH, JTAG (Single JTAG)

(master)
/slave

Debugging, Readback (Chip scope)

-> ILA core

Xilinx	Altera
CLB	→
Slice	→ ALM
IOB	→ IOE

Factory programmed FPGA

Xilinx - Easy path → } certain parts not tested
Altera - Hard copy → }

→ Structured ASIC pre-fabricated, layer fused to fix functionality.