→ Reference, for data types (standard) | Edcation

→ ML → matrix multiplication use. C to document | Report

-> Block diag. (paper)

-> Different Multiplier, Adder (design, speed, area, power compar) | Edcation

→ Research paper

→ ParametrisedIP | D

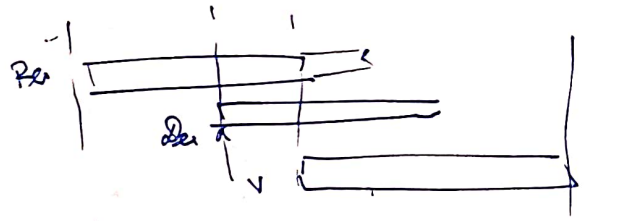
→ i/o Through GPIO

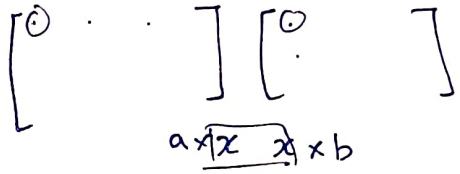
To write to Block RAM,

compare Block RAM, extract from BRAM

→ Limitation of matrix dimention to data type

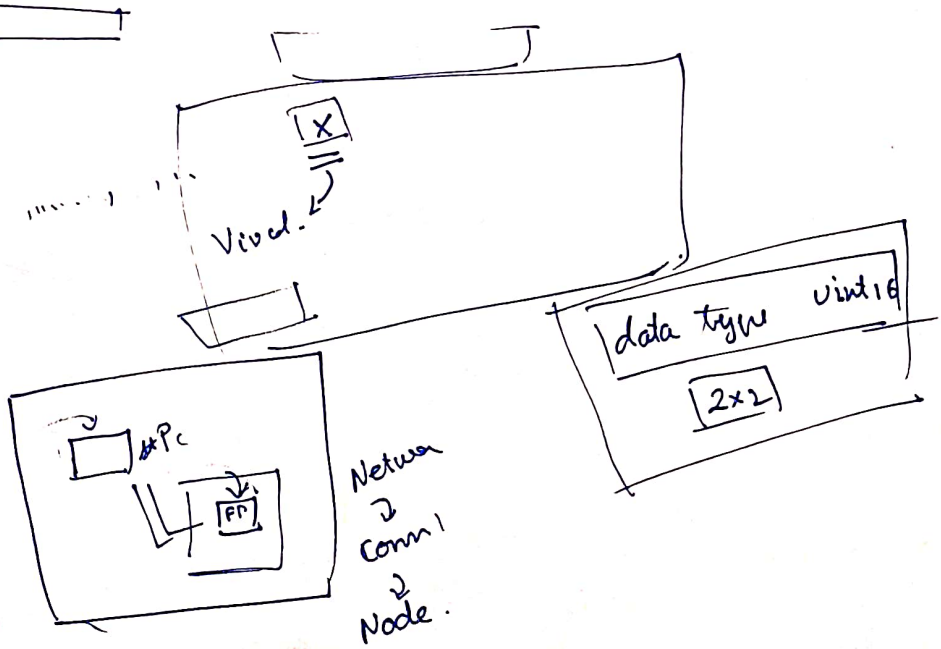
bottleneck. | Dr Report -




Mul, Addition,

Param



'This' pointer to handle of class

&

Skye Chip.

⇒ Embedded Design

⇒ RTL, DV, Analog Design

⇒ DFT

⇒ pre / post silicon validation

⇒ STA,

⇒ SV, UVM

1. Generate BRAM input, expected output

2. Calculate / compute & compare

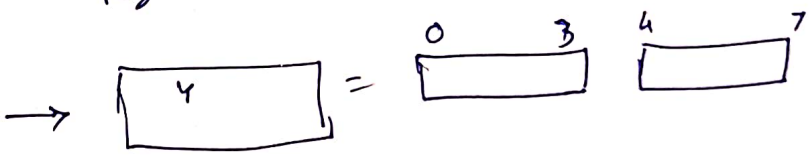
3. Set output compare match or not

2×2 2×2

0x 0 : 3 } A
0x 1 : 4
0x 2 : 6
0x 3 : 7
0x 4 - 9
5 : } B
6 :
7

5
9
10
11

reg




3×3 3×3

0
1
2
3
4
5
6
7
8
} A

( Expected Y == )

match <= 1'b1;

done <=

next

$$\begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}_{2\times2} \begin{bmatrix} b_{11} & b_{12} \\ b_{21} & b_{22} \end{bmatrix}_{2\times2} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$$

## Normal matrix multiplication

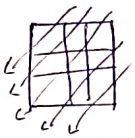
| | Multiplication | Addition | |
|---|---|---|---|
| $3 \times 3 \longrightarrow$ | 27 | 18 | 45 |
| | $n^3$ | $(n-1)n^2$ | |

$a + (n-1)d$

$1 + 3n - 3$

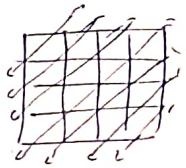
$3+1$

4



$5+(n-1)$

7

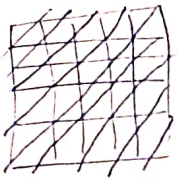


$7 + 3$

$4+(3)$

10

$n+$



$9+4$

13

## Systolic array

| | | | |
|---|---|---|---|
| $3 \times 3 \longrightarrow$ | 7 | 7 | 14 |
| | $3n-2$ | $3n-2$ | $6n-4$ |

$n+5$