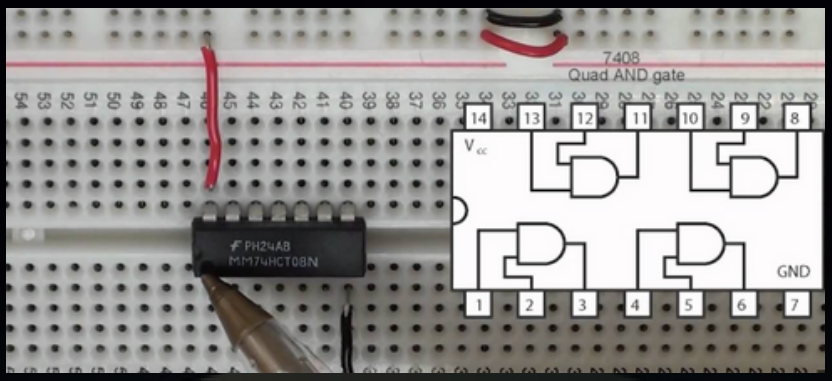
Logic Gates

Papers Dock

COMPUTER SCIENCE 9618 PAPER 3

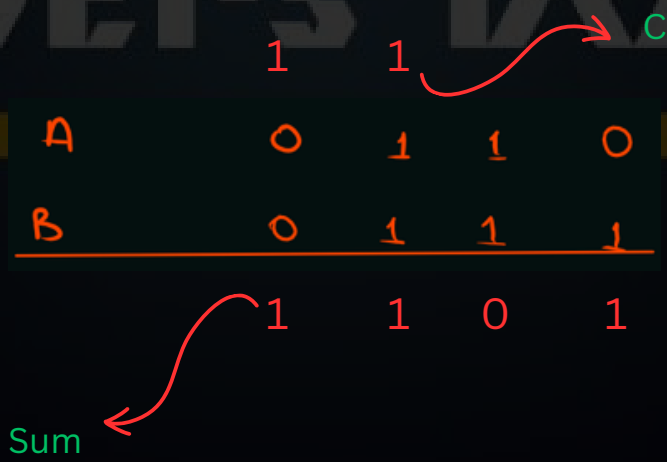
Logic Gates

Logic gates are basic building blocks in digital circuits that perform logical operations like AND, OR, and NOT. They are widely used in industries such as electronics, telecommunications, and automation for designing microprocessors, control systems, and data processing units.



ADDERS

- Used in Electronics
- Digital Circuit that performs addition of number
- Present in ALU (Arithmetic Logic Unit)



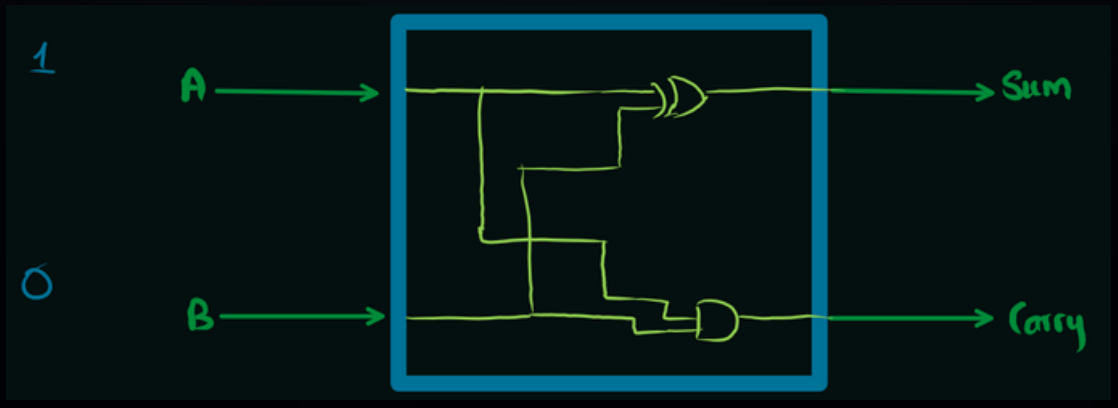
- If we are adding only two bits then we use half adder.
- If we are adding multiple bits then we use full adder.

HALF ADDER

- Addition of Two Bits
- Half adder will not add carry

Truth Table Half Adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

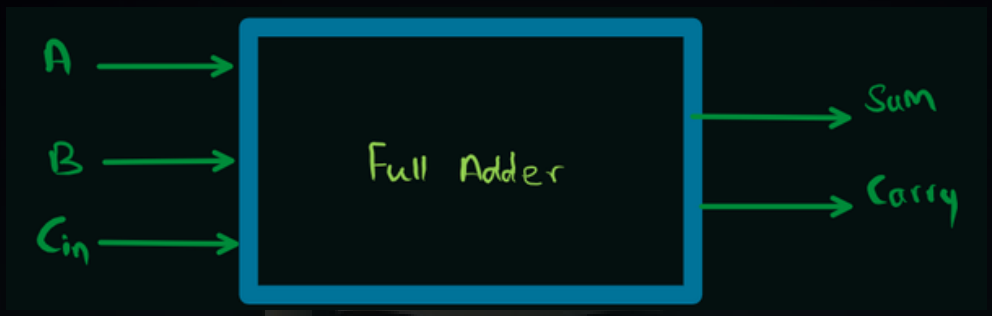


Problems in Half Adder

- **Basically we have to consider carry while adding, so that's not possible in Half Adders. For that purpose, you have to use full adder.**

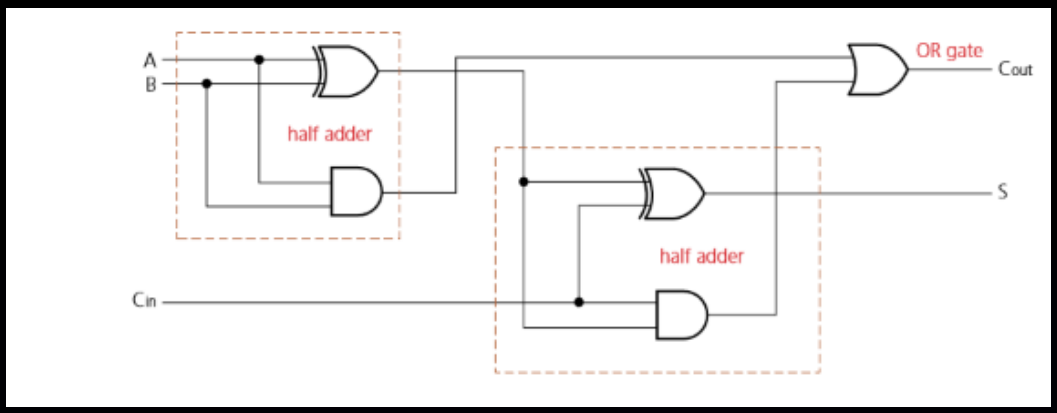
FULL ADDER

- **Adds three bits**
- **Not able to add complete nibble**



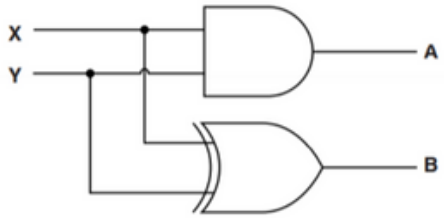
Truth Table Full Adder

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Exam Style Questions

4 (a) (i) Complete the truth table for this logic circuit.



Input		Output	
X	Y	A	B
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

[2]

(ii) State the name given to this logic circuit.

Half Adder ..... [1]

(iii) Name the labels usually given to **A** and **B**.

Label **A** Carry .....

Label **B** Sum .....

Explain why your answers are more appropriate for the **A** and **B** labels.

A basically represents carry part of the addition of 2 bits .....

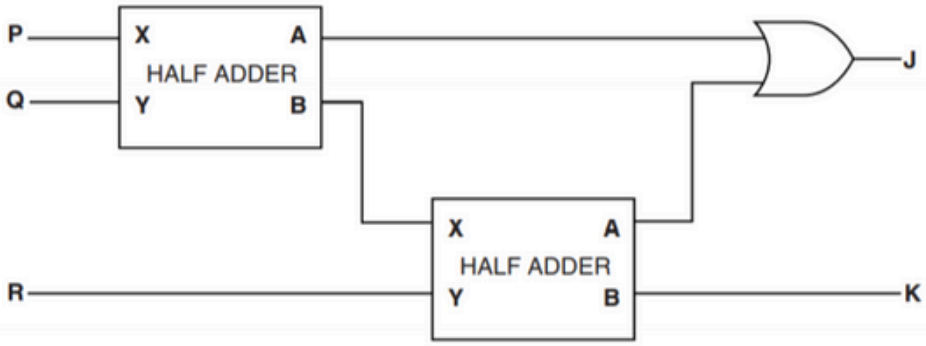
B basically represents sum part of the addition of 2 bits .....

..... [4]

5 (a) (i) A half adder is a logic circuit with the following truth table.

Input		Output	
X	Y	A	B
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

The following logic circuit is constructed.



Complete the following truth table for this logic circuit.

Input			Working space	Output	
P	Q	R		J	K
0	0	0		0	0
0	0	1		0	1
0	1	0		0	1
0	1	1		1	0
1	0	0		0	1
1	0	1		1	0
1	1	0		1	0
1	1	1		1	1

[2]

(ii) State the name given to this logic circuit.

Full Adder ..... [1]

(iii) Name the labels usually given to **J** and **K**.

Label **J** Carry (out) .....

Label **K** Sum .....

Explain why your answers are appropriate labels for these outputs.

J represents carry out part of the binary addition of 3 bits .....

K represents sum part of the binary addition of 3 bits .....

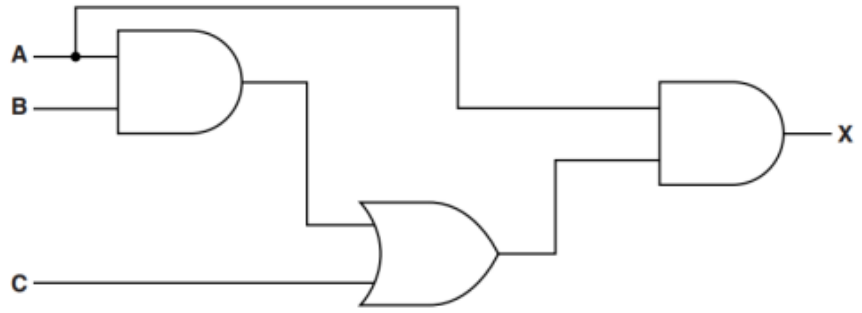
.....

..... [4]

Boolean Expression

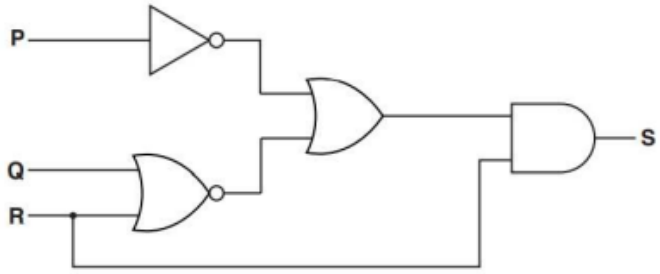
A AND B	$A \cdot B$
A NAND B	$\overline{A \cdot B}$
A OR B	$A + B$
A NOR B	$\overline{A + B}$
NOT A	$\overline{A}$
A XOR B	$A \oplus B$

(b) (i) Write the Boolean expression corresponding to the following logic circuit:



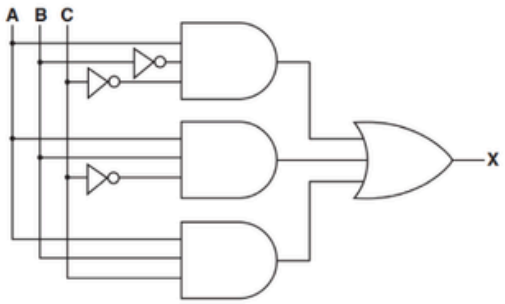
((A.B)+C).A ..... [2]

3 A logic circuit is shown:



(a) Write the Boolean algebraic expression corresponding to this logic circuit:

S = $\overline{((\overline{Q+R})+\overline{P})}.R$ ..... [4]



A	B	C	Working space	X
0	0	0		0
0	0	1		0
0	1	0		0
0	1	1		0
1	0	0		1
1	0	1		0
1	1	0		1
1	1	1		1

[2]

Karnaugh Map

Karnaugh map is graphical representation that provides a systematic method for simplifying the boolean expression.

Case 1 : Writing Expression By Trace Table As Sum of Product

INPUT			OUTPUT
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Step 1 : Mark Rows With Output 1

Step 2 : Use Sum Of Products And Write (A or $\bar{A}$) (B or $\bar{B}$)

3 (a) A Boolean algebraic expression produces the following truth table.

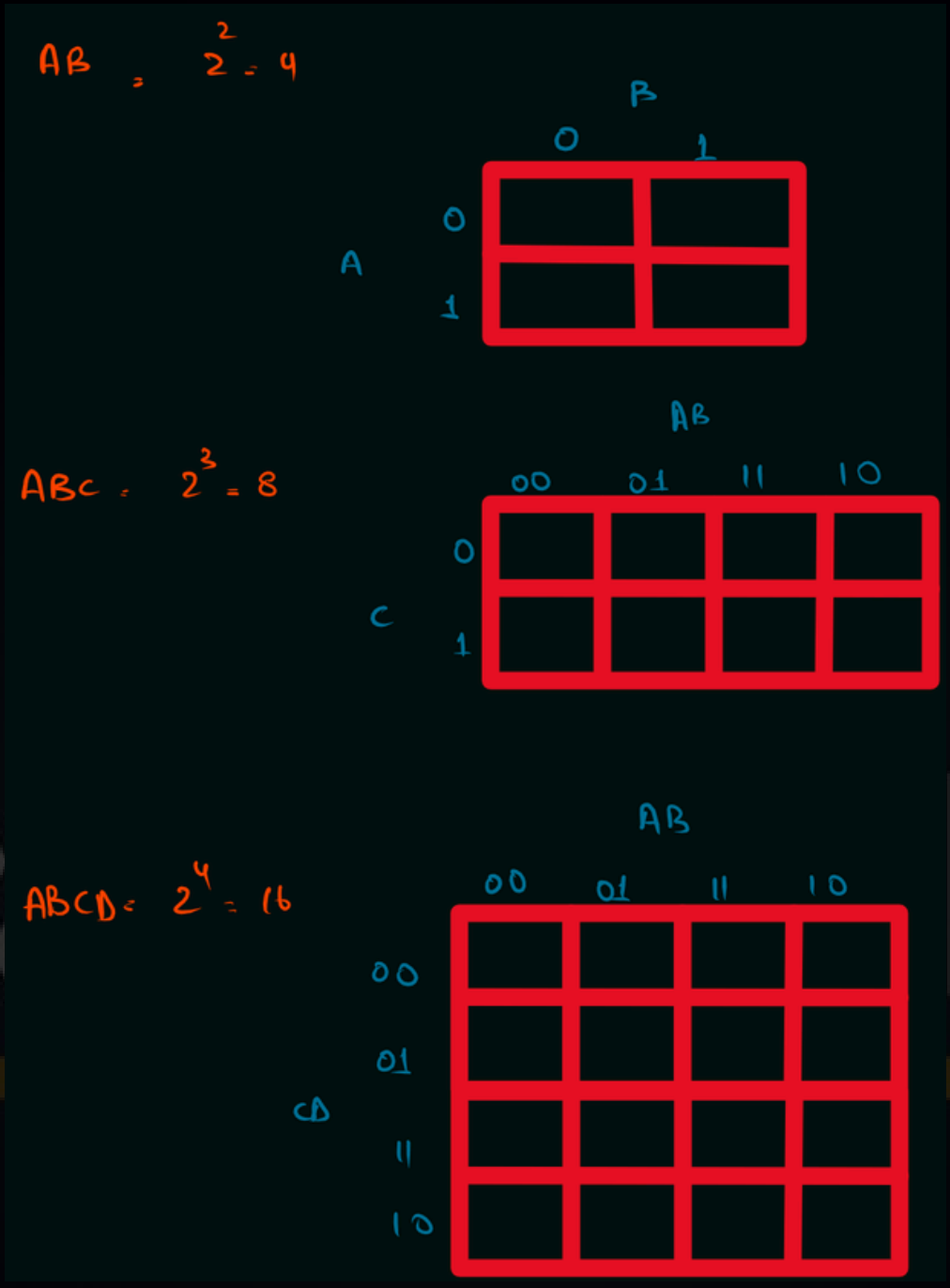
INPUT			OUTPUT
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

(iii) Write the simplified sum-of-products Boolean expression for the truth table.

X = $\bar{A}.\bar{B}.\bar{C} + \bar{A}.\bar{B}.C + \bar{A}.B.\bar{C} + \bar{A}.B.C + A.\bar{B}.\bar{C} +$ $A.\bar{B}.C$ [2]

Case 2 : Filling / Constructing K-MAP by Trace Table

Number of cells depends on the number of inputs
2^n = cells where n is the no of inputs



INPUT			OUTPUT
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

AB

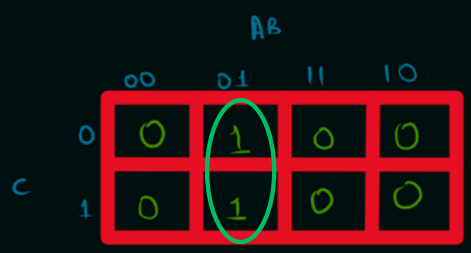
C \ AB	00	01	11	10
0	1	0	0	0
1	1	1	1	1

Case 3 : Simplifying Boolean Expression

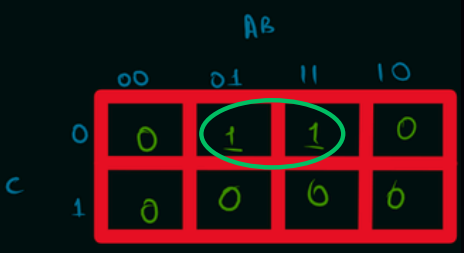
Looping → Adjacent 1
Equation using these loops

Rules For Looping

① Adjacent 1 are enclosed in a circle.



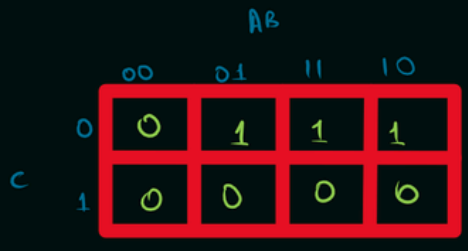
Vertical loop



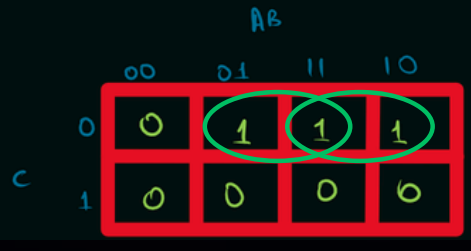
Horizontal loop

② Number of 1's in a particular loop.

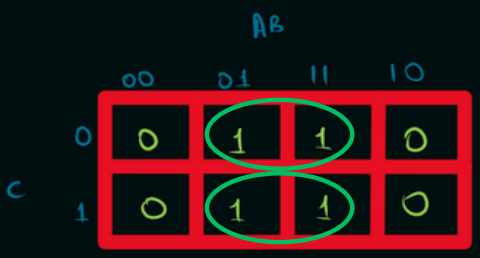
2 4 8 16 32 64 128



③ Overlapping Rule.



④ Group / loop of 1 should be as large as possible.



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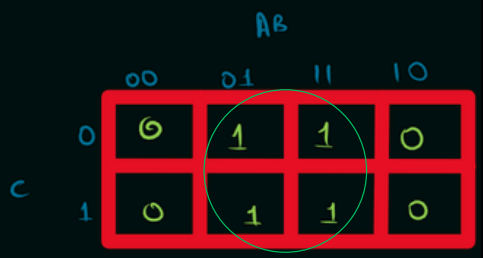
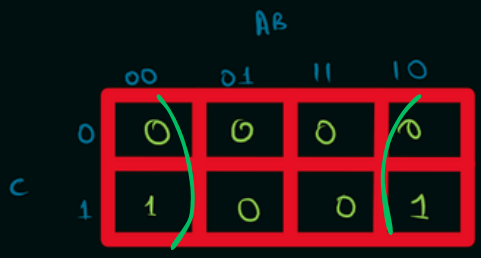
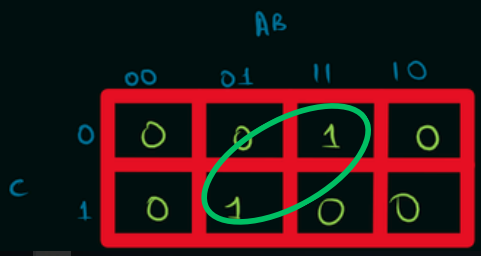


✓

⑤ 1's in corner are considered as adjacent.



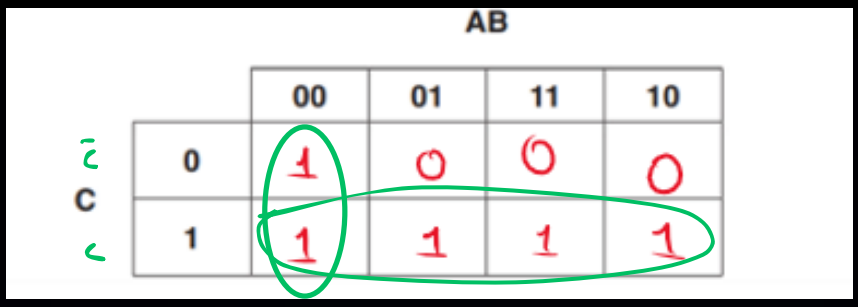
⑥ Diagnol looping is not allowed



✗

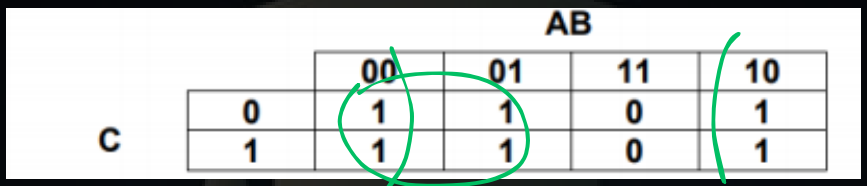
Making Equation From K-Map

Note : Loops are getting added . Look for constant value



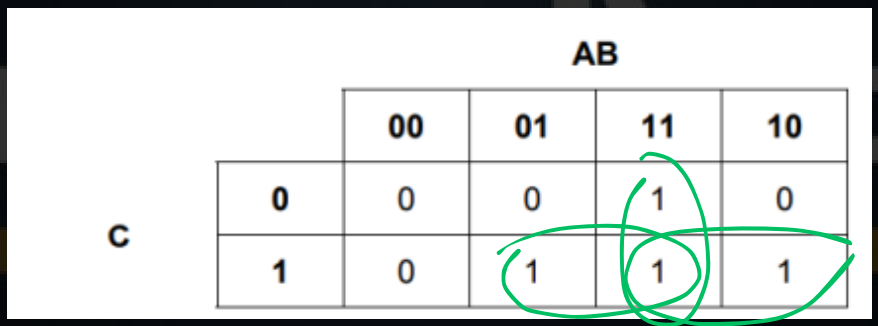
C \ AB	00	01	11	10
0	1	0	0	0
1	1	1	1	1

$\bar{A}.\bar{B} + C$



C \ AB	00	01	11	10
0	1	1	0	1
1	1	1	0	1

$\bar{A}.\bar{B}$



C \ AB	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$B.C + A.C + A.B$

Boolean Algebra

Laws Of Boolean Algebra

1) Commutative Law

Order Does Not Matter

$A + B = B + A$
$A \cdot B = B \cdot A$

2) Associative Law

$A + (B + C) = (A + B) + C$
$A \cdot (B \cdot C) = (A \cdot B) \cdot C$

3) Distributive Law

$A \cdot (B + C) = (A \cdot B) + (A \cdot C)$
$(A + B) \cdot (A + C)$

common will come out and will be added into the product of remaining two.

4) Idempotent Law

$A \cdot A = A$
$A + A = A$

5) Null Law

$0 \cdot A = 0$
$1 + A = 1$

6) Identity Law

$1 \cdot A = A$
$0 + A = A$

7) Inverse Law

$A \cdot \bar{A} = 0$
$A + \bar{A} = 1$

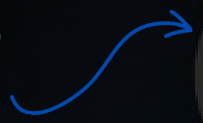
8) Absorption Law

$A + (A \cdot B) = A$
$A \cdot (\bar{A} + B) = A$
$A + (\bar{A} \cdot B) = A + B$
$\bar{A} + (A \cdot B) = \bar{A} + B$

9) Demorgan's Law

$\overline{A \cdot B} = \bar{A} + \bar{B}$

$\overline{A + B} = \bar{A} \cdot \bar{B}$



10) Double Compliment Law

$\bar{\bar{A}} = A$

$A = \bar{\bar{A}}$

Simplifying Boolean Expression

Case 1 : $A + B + \bar{A} + \bar{B}$

Associative law : $A + \bar{A} + B + \bar{B}$

Inverse law : $1 + 1$

$= 1$

Case 2 : $\bar{A} \cdot A + \bar{A} \cdot B + A \cdot B + B \cdot \bar{B} + A \cdot A \cdot A + A \cdot A \cdot \bar{B}$

Inverse law : $0 + \bar{A} \cdot B + A \cdot B + 0 + A \cdot A \cdot A + A \cdot A \cdot \bar{B}$

Identity law : $\bar{A} \cdot B + A \cdot B + A \cdot A \cdot A + A \cdot A \cdot \bar{B}$

Idempotent law : $\bar{A} \cdot B + A \cdot B + A + A \cdot \bar{B}$

Distributive law : $B \cdot (\bar{A} + A) + A (1 + \bar{B})$

Inverse law : $B \cdot (1) + A (1 + \bar{B})$

Null law : $B(1) + A(1)$

Identity law : $B + A$

Case 3 $A \cdot B \cdot C + \bar{A} + A \cdot \bar{B} \cdot C$

Associative law : $A \cdot B \cdot C + A \cdot \bar{B} \cdot C + \bar{A}$

Distributive law : $(A \cdot C) \cdot (B + \bar{B}) + \bar{A}$

Inverse law : $(A \cdot C) \cdot (1) + \bar{A}$

Identity law : $(A \cdot C) + \bar{A}$

Associative law : $\bar{A} + (A \cdot C)$

Absorption : $\bar{A} + C$

$A = \bar{\bar{A}}$

CASE 4 : $A \cdot \bar{B} \cdot \bar{C} + A \cdot B \cdot \bar{C} + A \cdot B \cdot C$

$(A \cdot \bar{C})(\bar{B} + B) + A \cdot B \cdot C$ (Distributive law)

$(A \cdot \bar{C})(1) + A \cdot B \cdot C$ (Inverse law)

$(A \cdot \bar{C}) + A \cdot B \cdot C$ (Identity law)

$A \cdot \bar{C} + A \cdot B \cdot C$ (Distributive law)

$A \cdot (\bar{C} + (B \cdot C))$

$A \cdot (\bar{C} + B)$ (Absorption law)

CASE 5 : $A \cdot \bar{B} \cdot \bar{C} + A \cdot B \cdot \bar{C} + A \cdot B \cdot C$

(Idempotent law) : $A \cdot \bar{B} \cdot \bar{C} + A \cdot B \cdot \bar{C} + A \cdot B \cdot \bar{C} + A \cdot B \cdot C$

(Distributive law) : $(A \cdot \bar{C}) \cdot (\bar{B} + B) + (A \cdot B) \cdot (\bar{C} + C)$

(Inverse law) $(A \cdot \bar{C}) \cdot (1) + A \cdot B \cdot (1)$

(Identity law) $(A \cdot \bar{C}) + (A \cdot B)$

(Distributive law) $A \cdot (\bar{C} + B)$

$(\bar{A} + \bar{C})(\bar{B} \cdot D + B + \bar{D})$ $\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D + \bar{A} \cdot B \cdot \bar{C} \cdot \bar{D}$

CASE 6: $\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D + \bar{A} \cdot \bar{B} \cdot C \cdot D + \bar{A} \cdot \bar{B} \cdot C \cdot \bar{D} + \bar{A} \cdot B \cdot \bar{C} \cdot \bar{D}$

$\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D + \bar{A} \cdot \bar{B} \cdot C \cdot D + \bar{A} \cdot \bar{B} \cdot C \cdot \bar{D} + \bar{A} \cdot B \cdot \bar{C} \cdot \bar{D} + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D}$

$(\bar{A} \cdot \bar{B} \cdot \bar{C}) \cdot (\bar{D} + D) + (\bar{A} \cdot \bar{B} \cdot C)(D + \bar{D}) + (\bar{A} \cdot \bar{C} \cdot \bar{D}) \cdot (B + \bar{B})$

$\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot (1) + (\bar{A} \cdot \bar{B} \cdot C)(1) + (\bar{A} \cdot \bar{C} \cdot \bar{D}) \cdot (1)$

$\bar{A} \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot \bar{B} \cdot C + \bar{A} \cdot \bar{C} \cdot \bar{D}$

$(\bar{A} \cdot \bar{B}) \cdot (\bar{C} + C) + \bar{A} \cdot \bar{C} \cdot \bar{D}$

$(\bar{A} \cdot \bar{B}) \cdot (1) + \bar{A} \cdot \bar{C} \cdot \bar{D}$

$\bar{A} \cdot \bar{B} + \bar{A} \cdot \bar{C} \cdot \bar{D}$

$\bar{A} \cdot (\bar{B} + (\bar{C} \cdot \bar{D}))$

CASE 7 : $\overline{(\bar{W} + X) \cdot (Y + \bar{Z})}$

$\overline{(\bar{W} + X)} + \overline{(Y + \bar{Z})}$

$(\bar{\bar{W}} \cdot \bar{X}) + (\bar{Y} \cdot \bar{\bar{Z}})$

$(W \cdot \bar{X}) + (\bar{Y} \cdot Z)$

Flip Flop

Combination Circuit

Output depends on input

Sequentlal Circuit

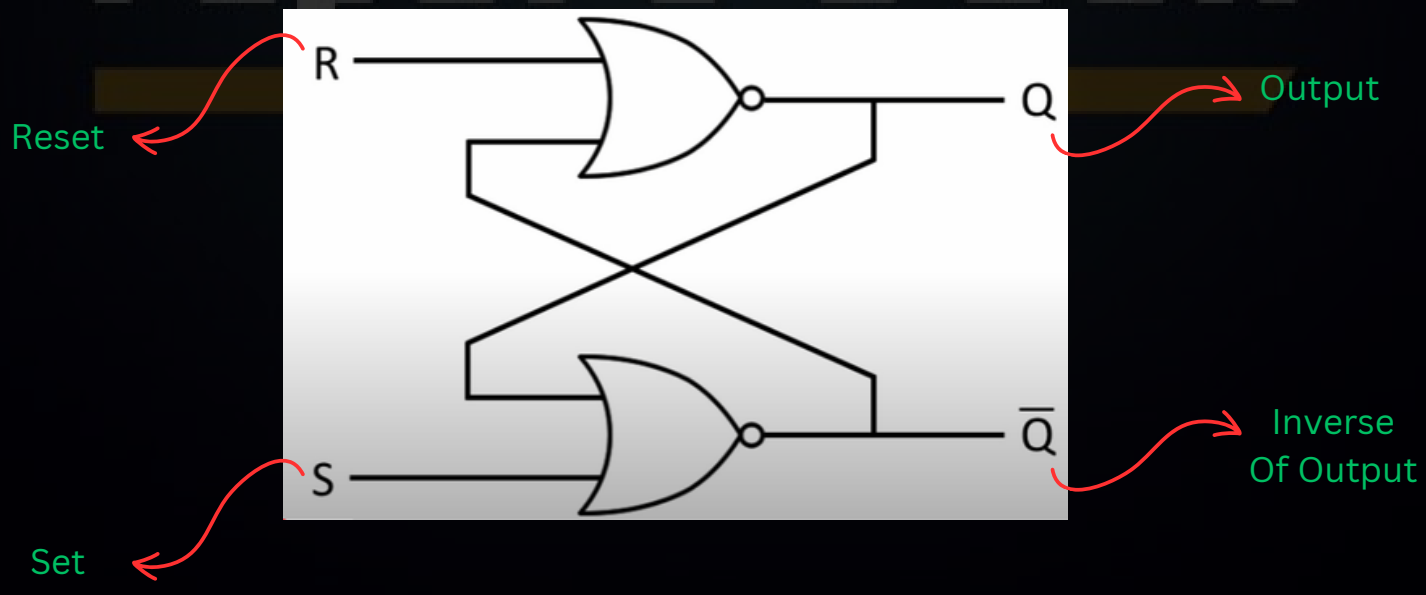
Output depends on the output of previous value

Flip flops are circuits used in digital electronics to store information / Binary Data

Describe the role of Flip Flops in Computer ?

- A flip flop can either store a 0 or a 1
- Computers uses bits to store data.
- Flip Flops can therefore be used to store bits of data.
- Memory can be created from flip flops.

SR NOR Gate Flip Flop



	S	R	Q	$\overline{Q}$
Initially	1	0	1	0
S changed to 0	0	0		
R changed to 1	0	1		
R changed to 0	0	0		
S and R changed to 1	1	1		

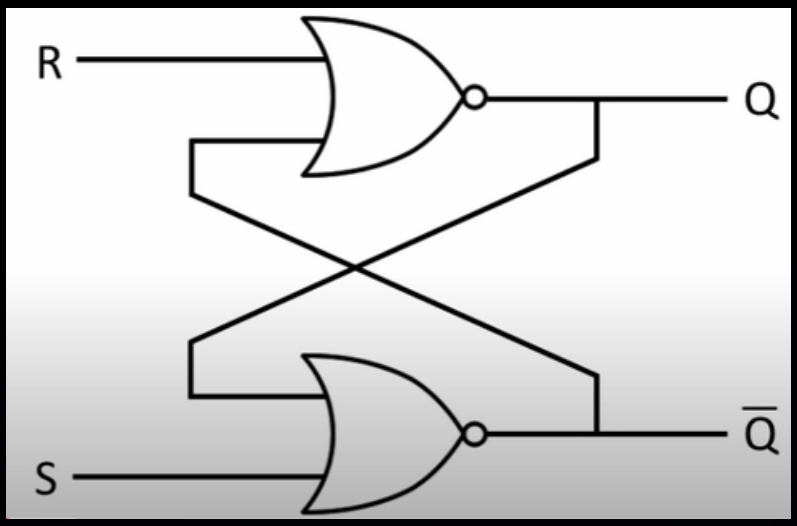
How SR NOR Gate Flip Flop works ?

There are 4 different states

- Set (S): When the Set input is activated (S = 1 and R = 0), the flip-flop stores a 1.
- Reset (R): When the Reset input is activated (R = 1 and S = 0), the flip-flop stores a 0.
- Hold State: If both inputs are 0 (S = 0, R = 0), the flip-flop holds its previous state, meaning it keeps storing the same value as before.
- Invalid State: If both S and R are 1, it's an invalid state for an SR flip-flop, leading to unpredictable behavior, so this condition is generally avoided.

Why do we need Hold State ?

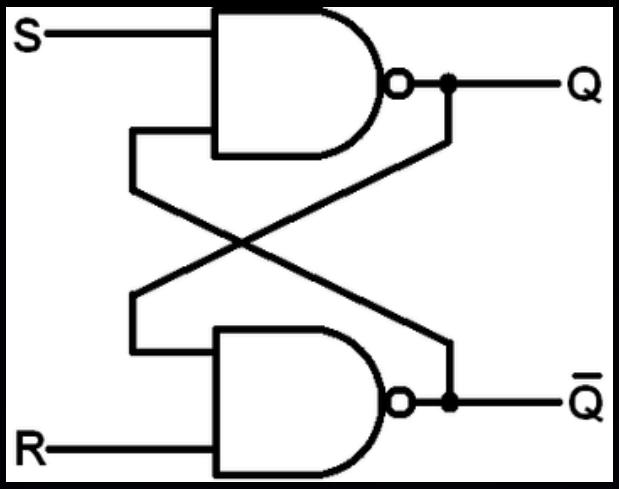
In digital circuits, sometimes we want to keep the current value unchanged until a new command is given. Without the hold state, the flip-flop would constantly need new inputs to maintain the stored value, making it impractical as a memory element.



	S	R	Q	$\overline{Q}$
Initially	1	0	1	0
S changed to 0	0	0	1	0
R changed to 1	0	1	0	1
R changed to 0	0	0	0	1
S and R changed to 1	1	1	0	0

Whenever the input of S AND R is 1 at the same time then the value on Q and $\bar{Q}$ will be 0 which is not possible as $\bar{Q}$ is the inverse of Q.

SR NAND Gate Flip Flop



	S	R	Q	$\overline{Q}$
Initially	1	0	0	1
R changed to 1	1	1	0	1
S changed to 0	0	1	1	0
S changed to 1	1	1	1	0
S and R changed to 0	0	0	1	1

How SR NAND Gate Flip Flop works ?

There are 4 different states

- Set (S' = 0, R' = 1): When the Set input is activated (S' = 0 and R' = 1), the flip-flop stores a 1.
- Reset (S' = 1, R' = 0): When the Reset input is activated (R' = 0 and S' = 1), the flip-flop stores a 0.
- Hold State (S' = 1, R' = 1): If both inputs are 1 (S' = 1 and R' = 1), the flip-flop holds its previous state, meaning it keeps storing the same value as before.
- Invalid State (S' = 0, R' = 0): If both S' and R' are 0, it's an invalid state for a NAND SR flip-flop. This state is generally avoided to prevent unpredictable behavior.

(ii) One of the combinations in the truth table should not be allowed to occur.

State the values of S and R that should not be allowed. Justify your choice.

S = 0 R = 0

Q and Q have the same output and they should be compliment of eachother due to which flip flop becomes unstable

[3]

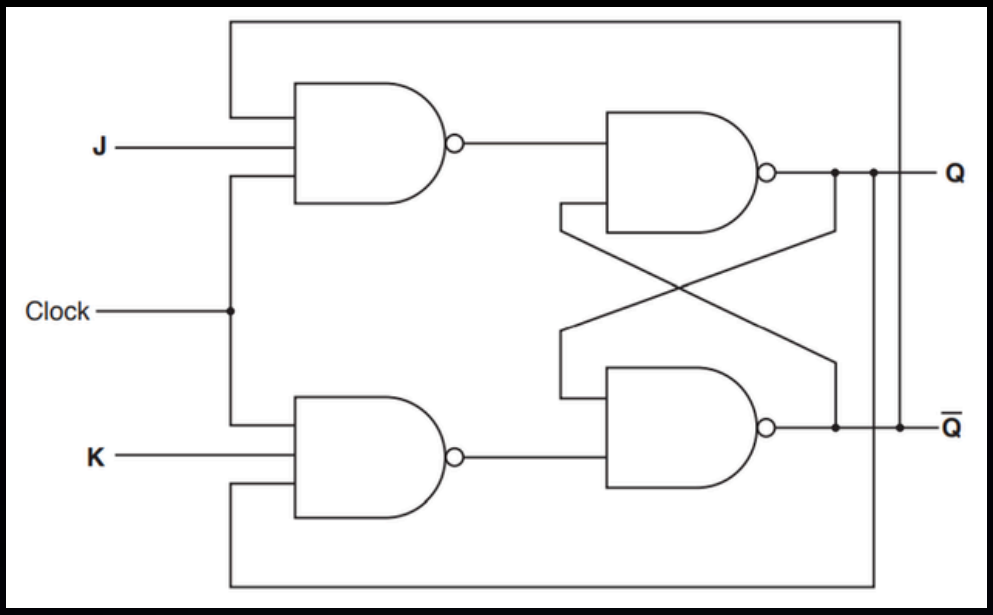
What are the two problems in S-R flip flop ?

Problem 1: One combination of S and R is there on which Q and $\bar{Q}$ have same value although they should be inverse of each other.

Problem 2: Input may not arrive at the same time

Note: Whenever the value of Q and $\bar{Q}$ becomes same the flip flop becomes unstable. Flip flop has only two stable states.

JK Flip Flop



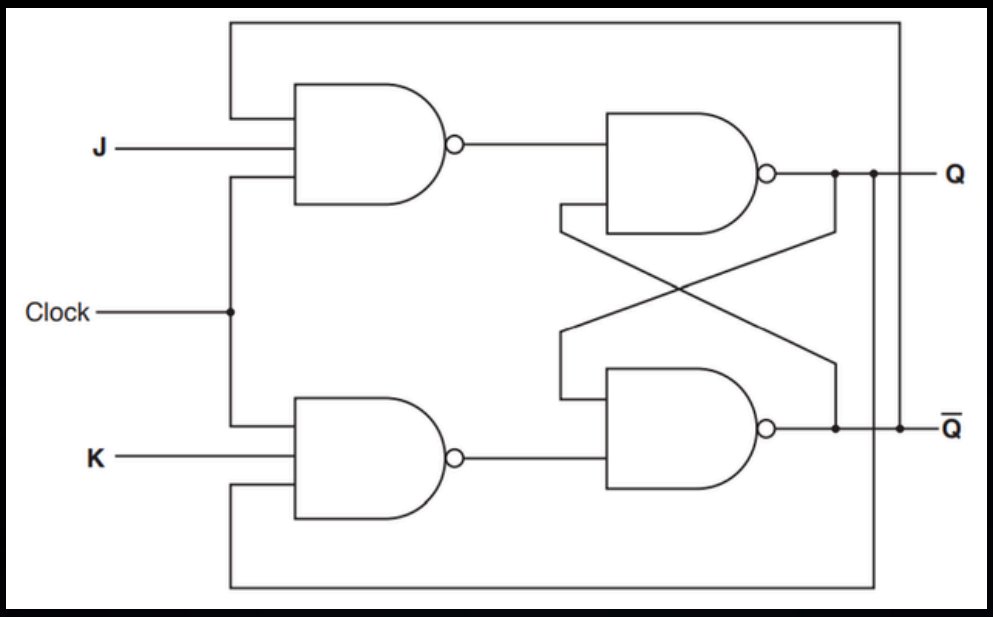
Explain why the JK flip flop is an improvement on the SR flip flop ?

- SR flip flops has an invalid combination of S and R
- SR flip flop inputs may not arrive at the same time.

- JK flip flops does not allow for Q and $\bar{Q}$ to have the same value. All four combinations of values for J and K are valid.
- JK flip flop incorporates a clock pulse for synchronization.

What are the advantage of JK flip flop?

- All four possibilities are valid
- Unstable state is avoided
- Flip flop is stable



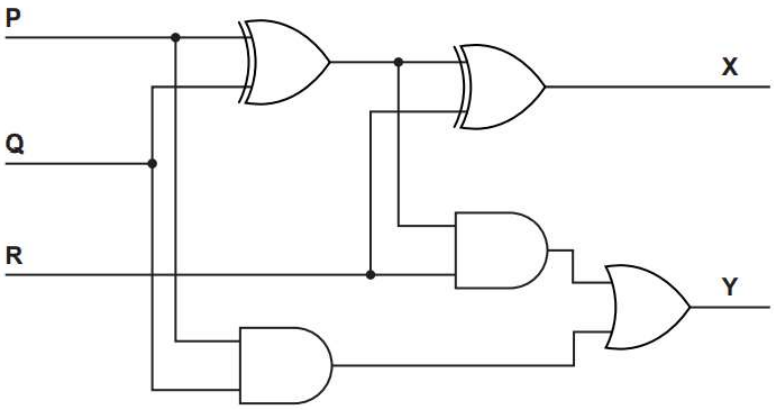
(i) Complete this truth table for the JK flip-flop.

J	K	Clock	Working space	Initial values		Final values	
				Q	$\overline{Q}$	Q	$\overline{Q}$
0	0	1		1	0	1	0
0	0	1		0	1	0	1
0	1	1		1	0	0	1
0	1	1		0	1	0	1
1	0	1		1	0	1	0
1	0	1		0	1	1	0
1	1	1		1	0	0	1
1	1	1		0	1	1	0

Logic Gates

Question 1

4 **(a)** Write the Boolean algebraic expressions for the following logic circuit.



X = ...

.....

Y = ...

.....

[5]

(b) The logic circuit given in **part (a)** is a full adder.

(i) Give the purpose of outputs **X** and **Y** in this circuit.

X .....

Y .....

[2]

(ii) Give the use of the input **R** in this circuit.

..... [1]

Question 2

4 The following truth table represents a logic circuit with three inputs and two outputs.

INPUT			OUTPUT	
A	B	C	X	Y
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(a) Write the Boolean expressions for the truth table as sum-of-products.

X = ...

.....

Y = ...

.....

[4]

(b) Complete the Karnaugh Maps (K-maps) for the truth table.

OUTPUT X

C \ AB	00	01	11	10
0				
1				

OUTPUT Y

C \ AB	00	01	11	10
0				
1				

[2]

(c) The K-maps can be used to simplify **one** of the expressions in **part (a)**.

(i) Draw loop(s) around appropriate group(s) of 1s to produce an optimal sum-of-products for the single output table that can be simplified in **part (b)**. [3]

(ii) Write the simplified sum-of-products expressions for this output from **part (c)(i)**.

..... [3]

(d) Identify the common logic circuit given by the truth table in **part (a)**. Give the use of each output.

Logic circuit .....

Use of **X** .....

Use of **Y** .....

[3]

Question 3

4 The following truth table represents a logic circuit with three inputs and two outputs.

INPUT			OUTPUT	
A	**B**	**C**	**X**	**Y**
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	0	0
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

(a) Write the Boolean expressions for the truth table as sum-of-products.

X = ...

Y = ...

[3]

(b) Complete the Karnaugh Maps (K-maps) for the truth table.

OUTPUT X

C \ AB	00	01	11	10
0				
1				

OUTPUT Y

C \ AB	00	01	11	10
0				
1				

[2]

(c) The K-maps can be used to simplify **one** of the expressions in **part (a)**.

(i) Draw loop(s) around appropriate group(s) of 1s to produce an optimal sum-of-products for the single output table that can be simplified in **part (b)**. [2]

(ii) Write the simplified sum-of-products expressions for this output from **part (c)(i)**.

..... [2]

Question 4

5 Complete these statements about flip-flops.

A flip-flop is a ..... .

It has ..... stable states.

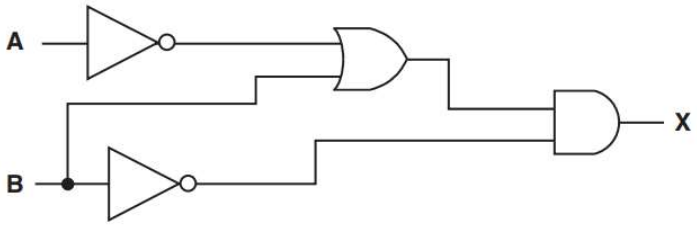
A flip-flop is used for ..... .

There are different types of flip-flop, for example ..... and ..... .

[5]

Question 5

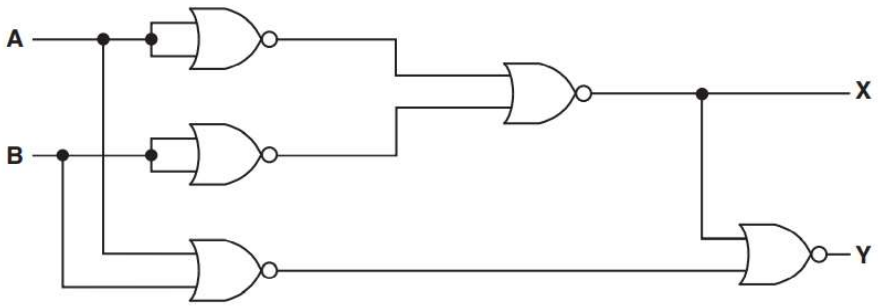
3 **(a)** The following logic circuit can be simplified to use only one gate.



Give the name of this single gate.

..... [1]

(b) **(i)** Complete the truth table for the logic circuit.



A	B	Working space	X	Y
0	0			
0	1			
1	0			
1	1			

[2]

(ii) Give the name of the logic circuit that has this truth table.

..... [1]

(iii) Give the uses for outputs **X** and **Y**.

X .....

Y .....

[2]

(c) Consider the following Boolean algebraic expression:

$$\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot D + \overline{A} \cdot \overline{B} \cdot C \cdot D + \overline{A} \cdot \overline{B} \cdot C \cdot \overline{D} + \overline{A} \cdot B \cdot \overline{C} \cdot \overline{D}$$

Use Boolean algebra to simplify the expression. Show your working.

Working .....

.....

.....

.....

.....

.....

.....

.....

.....

Simplified expression ..... [5]

Question 6

3 **(a)** A Boolean algebraic expression produces the following truth table.

INPUT			OUTPUT
A	**B**	**C**	**X**
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

(i) Complete the Karnaugh Map (K-map) for the truth table.

		AB			
		00	**01**	**11**	**10**
C	**0**				
	1				

[1]

The K-map can be used to simplify the expression that produced the truth table in **part (a)**.

(ii) Draw loops around appropriate groups of 1s in the K-map to produce an optimal sum-of-products. [2]

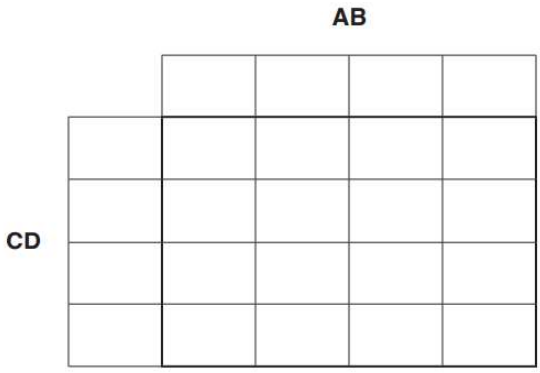
(iii) Write the simplified sum-of-products Boolean expression for the truth table.

X = ... [2]

(b) A logic circuit with four inputs produces the following truth table.

INPUT				OUTPUT
A	**B**	**C**	**D**	**X**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

(i) Complete the K-map for the truth table.



[4]

(ii) Draw loops around appropriate groups of 1s in the K-map to produce an optimal sum-of-products. [2]

(iii) Write the simplified sum-of-products Boolean algebraic expression for the truth table.

X = ... [2]

Question 7

4 A Boolean expression produces the following truth table.

INPUT			OUTPUT
A	**B**	**C**	**X**
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

(a) Write the Boolean expression for the truth table as a sum-of-products.

X = ... [2]

(b) Complete the Karnaugh Map (K-map) for the truth table above.

		AB			
		00	**01**	**11**	**10**
C	**0**				
	1				

[1]

The K-map can be used to simplify the expression in **part (a)**.

(c) Draw loops around appropriate groups in the K-map in **part (b)** to produce an optimal sum-of-products. [2]

(d) Write, using your answer to **part (c)**, a simplified sum-of-products expression for the truth table.

X = ... [2]

Question 8

2 **(a)** A Boolean expression produces the following truth table.

INPUT			OUTPUT
A	**B**	**C**	**X**
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

(i) Write the Boolean expression for the truth table by applying the sum-of-products.

X = ...

..... [3]

(ii) Complete the Karnaugh Map (K-map) for the truth table in **part (a)**.

		AB			
		00	**01**	**11**	**10**
C	**0**				
	1				

[1]

The K-map can be used to simplify the function in **part (a)(i)**.

(iii) Draw loop(s) around appropriate groups in the table in **part (a)(ii)**, to produce an optimal sum-of-products. [2]

(iv) Write, using your answer to **part (a)(iii)**, a simplified Boolean expression for your Karnaugh map.

X = ... [2]

(b) Simplify the following expression using De Morgan's laws. Show your working.

$$\overline{(\overline{W} + X) \bullet (Y + \overline{Z})}$$

.....

.....

.....

.....

.....

..... [3]

Question 9

4 **(a)** A Boolean expression produces the following truth table.

INPUT			OUTPUT
A	**B**	**C**	**X**
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

(i) Write the Boolean expression for the truth table as a sum-of-products.

X = ...[2]

(ii) Complete the Karnaugh Map (K-map) for the truth table in **part (a)(i)**.

C \ AB	00	01	11	10
0				
1				

[1]

The K-map can be used to simplify the function in **part (a)(i)**.

(iii) Draw loop(s) around appropriate group(s) of 1s to produce an optimal sum-of-products for the table in **part (a)(ii)**. [2]

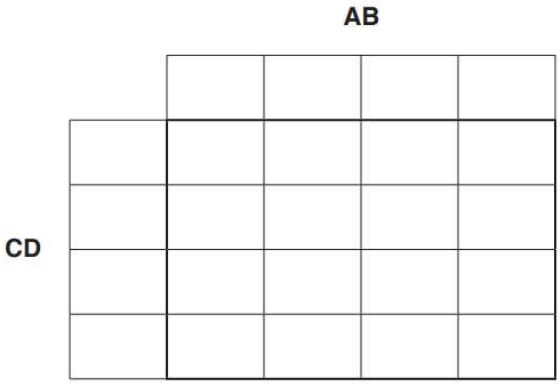
(iv) Write the simplified sum-of-products expression for your answer to **part (a)(iii)**.

X = ...[2]

(b) A logic circuit with four inputs produces the following truth table.

INPUT				OUTPUT
A	**B**	**C**	**D**	**X**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

(i) Complete the K-map that corresponds to the truth table.



[4]

(ii) Draw loop(s) around appropriate group(s) of 1s to produce an optimal sum-of-products for the table in **part (b)(i)**. [2]

(iii) Write the simplified sum-of-products expression for your answer to **part (b)(ii)**.

X = ...[2]

Question 10

4 **(a)** A Boolean expression corresponds to the following truth table.

INPUT			OUTPUT
A	**B**	**C**	**X**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(i) Write the Boolean expression for the truth table by applying the sum-of-products.

X = ...[2]

(ii) Complete the Karnaugh Map (K-map) for the truth table.

C \ AB	00	01	11	10
0				
1				

[1]

(iii) The K-map can be used to simplify the expression in **part (a)(i)**.

Draw loop(s) around appropriate groups of 1s in the table in **part (a)(ii)** to produce an optimal sum-of-products. [3]

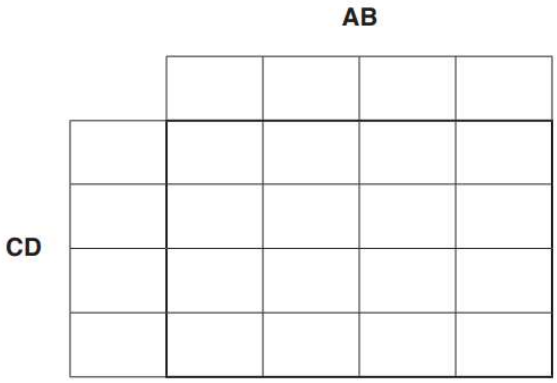
(iv) Write the simplified sum-of-products expression for your answer to **part (a)(iii)**.

X = ...[3]

(b) A logic circuit with four inputs produces the following truth table.

INPUT				OUTPUT
A	**B**	**C**	**D**	**X**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

(i) Complete the K-map that corresponds to the truth table.



[4]

(ii) Draw loop(s) around appropriate groups of 1s in the table in **part (b)(i)** to produce an optimal sum-of-products. [2]

(iii) Write the simplified sum-of-products expression for your answer to **part (b)(ii)**.

X = ...[2]

Question 11

3 **(a)** Consider the following Boolean expression.

$$A \cdot \overline{B} \cdot \overline{C} + A \cdot B \cdot \overline{C} + A \cdot B \cdot C$$

Use Boolean algebra to simplify the expression.

.....

.....

.....

.....

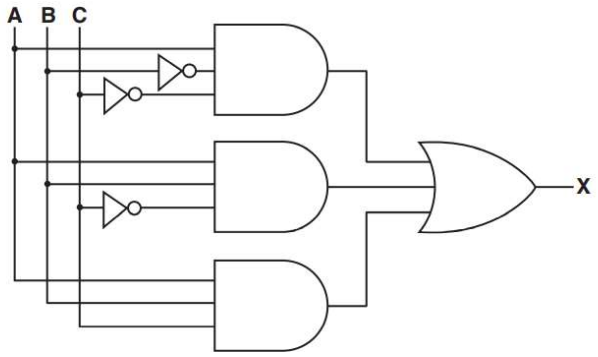
.....

.....

.....

.....[4]

(b) (i) Complete the truth table for the following logic circuit.



A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[2]

(ii) Complete the Karnaugh Map (K-map) for the truth table in **part (b)(i)**.

		AB			
		00	01	11	10
C	0				
	1				

[1]

(iii) Draw loops around appropriate groups of 1s in the table in **part (b)(ii)** to produce an optimal sum-of-products. [2]

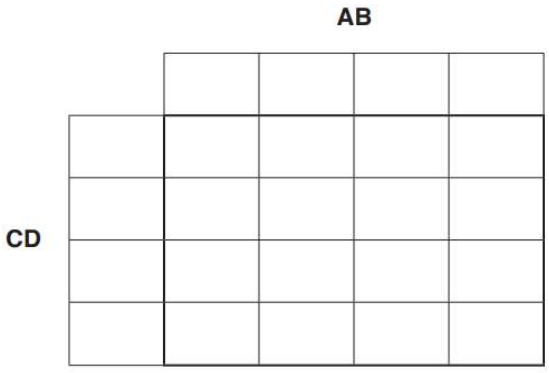
(iv) Using your answer to **part (b)(iii)**, write a simplified sum-of-products Boolean expression.

X = ...[2]

(c) The truth table for a logic circuit with four inputs is shown.

INPUT				OUTPUT
A	**B**	**C**	**D**	**X**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

(i) Complete the K-map for the truth table in **part (c)**.



[4]

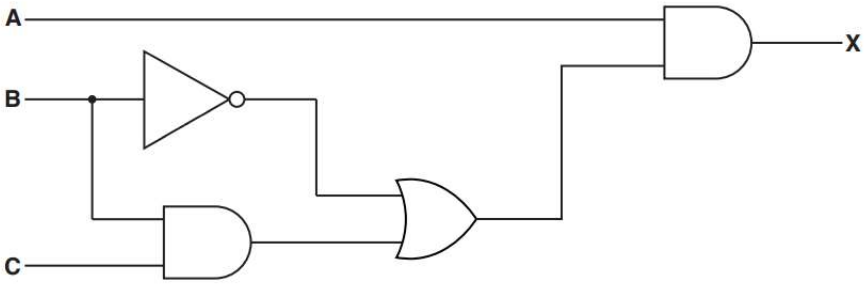
(ii) Draw loops around appropriate groups of 1s in the table in **part (c)(i)** to produce an optimal sum-of-products. [2]

(iii) Using your answer to **part (c)(ii)**, write a simplified sum-of-products Boolean expression.

X = ...[2]

Question 12

3 Consider the following logic circuit, which contains a redundant logic gate.



(a) Write the Boolean algebraic expression corresponding to this logic circuit.

X = ...[3]

(b) Complete the truth table for this logic circuit.

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[2]

(c) **(i)** Complete the Karnaugh Map (K-map) for the truth table in **part (b)**.

		AB			
		00	**01**	**11**	**10**
C	**0**				
	1				

[1]

The K-map can be used to simplify the expression in **part (a)**.

(ii) Draw loop(s) around appropriate groups to produce an optimal sum-of-products. [2]

(iii) Write a simplified sum-of-products expression, using your answer to **part (ii)**.

X = ...[2]

(d) One Boolean identity is:

$$A + \overline{A}.B = A + B$$

Simplify the expression for X in **part (a)** to the expression for X in **part (c)(iii)**. You should use the given identity.

.....

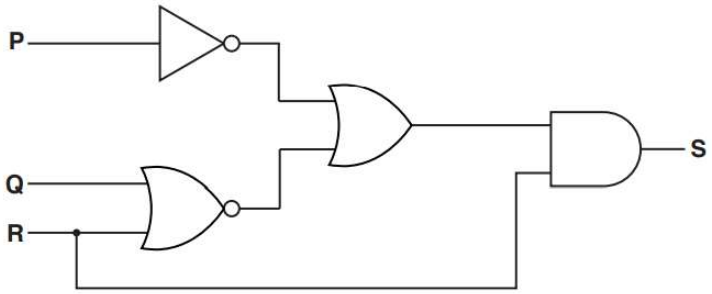
.....

.....

.....[2]

Question 13

3 A logic circuit is shown:



(a) Write the Boolean algebraic expression corresponding to this logic circuit:

S = ...[4]

(b) Complete the truth table for this logic circuit:

P	Q	R	Working space	S
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[2]

(c) **(i)** Complete the Karnaugh Map (K-map) for the truth table in **part (b)**.

		PQ			
		00	**01**	**11**	**10**
R	**0**				
	1				

[1]

The K-map can be used to simplify the function in **part (a)**.

(ii) Draw loop(s) around appropriate groups to produce an optimal sum-of-products. [1]

(iii) Write a simplified sum-of-products expression, using your answer to **part (ii)**.

S = ...[1]

(d) One Boolean identity is:

$$(A + B) . C = A . C + B . C$$

Simplify the expression for S in **part (a)** to the expression for S in **part (c)(iii)**.

You should use the given identity and De Morgan's Laws.

.....

.....

.....

.....

.....

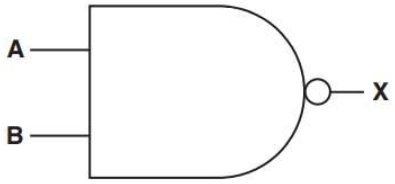
.....

.....

.....[3]

Question 14

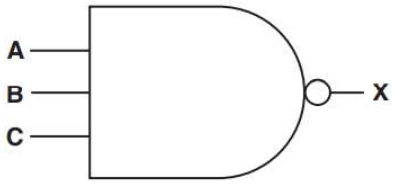
5 (a) (i) Complete the truth table for this 2-input NAND gate:



A	B	X
0	0	
0	1	
1	0	
1	1	

[1]

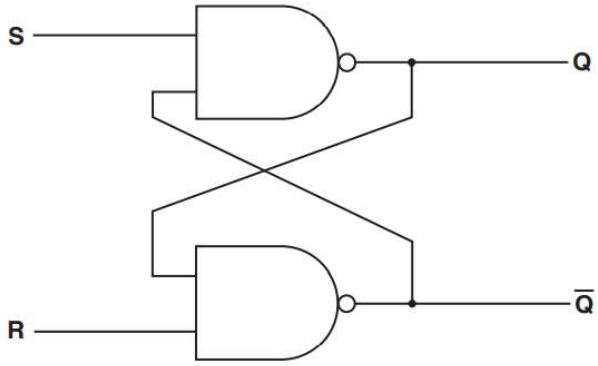
(ii) Complete the truth table for this 3-input NAND gate:



A	B	C	X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

[1]

(b) A SR flip-flop is constructed using two NAND gates.



(i) Complete the truth table for the SR flip-flop:

	S	R	Q	$\overline{Q}$
Initially	1	0	0	1
R changed to 1	1	1		
S changed to 0	0	1		
S changed to 1	1	1		
S and R changed to 0	0	0	1	1

[3]

(ii) The final row in the table in **part b(i)** shows that the output for both **Q** and $\overline{Q}$ is 1.

Explain why this is a problem.

.....

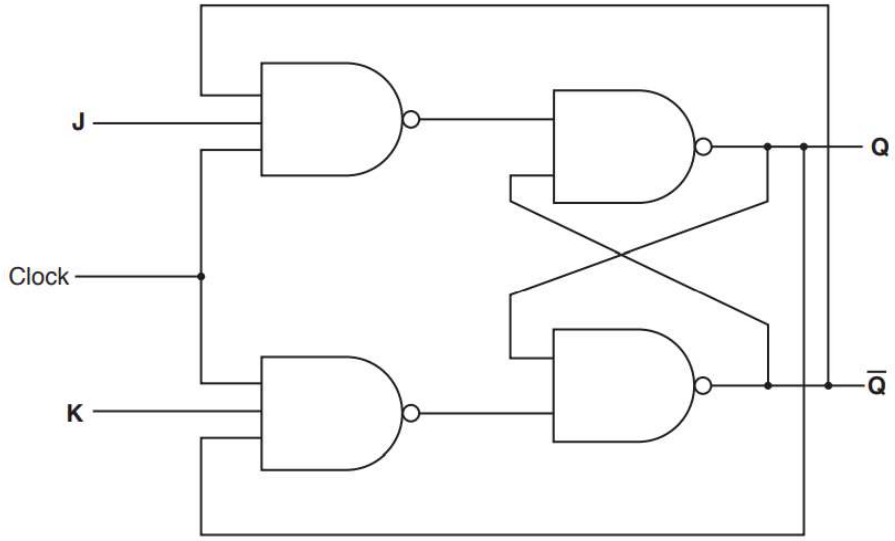
.....

.....

..... [2]

(c) Another type of flip-flop is the JK flip-flop.

A JK flip-flop is constructed as follows:



(i) Complete this truth table for the JK flip-flop.

J	K	Clock	Working space	Initial values		Final values	
				Q	$\overline{Q}$	Q	$\overline{Q}$
0	0	1		1	0	1	0
0	0	1		0	1	0	1
0	1	1		1	0	0	1
0	1	1		0	1	0	1
1	0	1		1	0		
1	0	1		0	1		
1	1	1		1	0		
1	1	1		0	1		

[4]

(ii) Explain why the JK flip-flop is an improvement on the SR flip-flop.

.....

.....

.....

..... [2]

(d) Explain the role of flip-flops in a computer.

.....

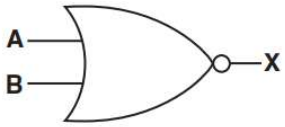
.....

.....

..... [2]

Question 15

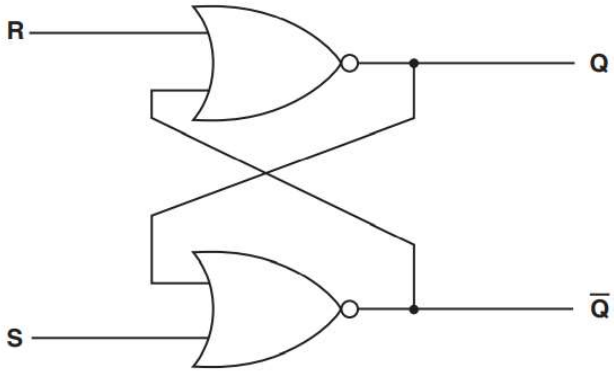
5 **(a)** Complete the truth table for this NOR gate:



A	B	X
0	0	
0	1	
1	0	
1	1	

[1]

A SR flip-flop is constructed using two NOR gates.



(b) Complete the truth table for the SR flip-flop:

	S	R	Q	$\overline{Q}$
Initially	1	0	1	0
S changed to 0	0	0		
R changed to 1	0	1		
R changed to 0	0	0		
S and R changed to 1	1	1		

[4]

Another type of flip-flop is the JK flip-flop. The JK flip-flop is an improvement on the SR flip-flop.

(c) (i) The JK flip-flop has three inputs. Two of the inputs are the Set (J) and the Reset (K).

State the third input.

.....[1]

(ii) There are **two** problems with the SR flip-flop that the JK flip-flop overcomes.

State each problem and state why it does not occur for the JK flip-flop.

Problem 1 .....

.....

.....

.....

Problem 2 .....

.....

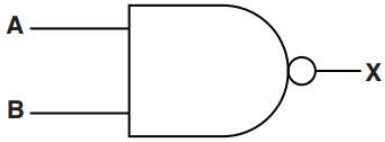
.....

.....

[4]

Question 16

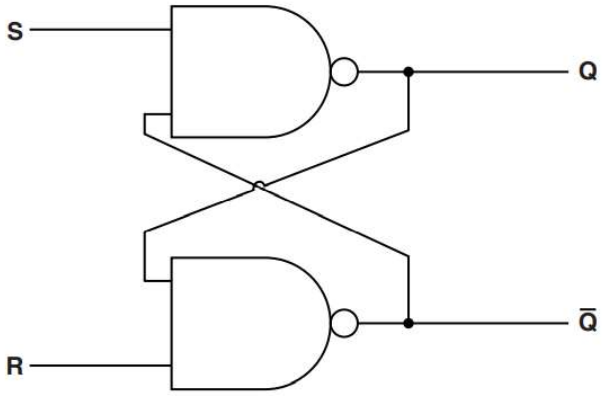
5 **(a)** Complete the truth table for this NAND gate:



A	B	X
0	0	
0	1	
1	0	
1	1	

[1]

A SR flip-flop is constructed using two NAND gates.



(b) (i) Complete the truth table for the SR flip-flop.

	S	R	Q	$\bar{Q}$
Initially	1	0	0	1
R changed to 1	1	1		
S changed to 0	0	1		
S changed to 1	1	1		
S and R changed to 0	0	0		

[4]

(ii) One of the combinations in the truth table should not be allowed to occur.

State the values of S and R that should not be allowed. Justify your choice.

S = ... R = ...

.....

.....

.....

.....[3]

Another type of flip-flop is the JK flip-flop.

(c) (i) Give one extra input present in the JK flip-flop.

.....

.....[1]

(ii) Give **one** advantage of the JK flip-flop.

.....

.....[1]

(d) Describe the role of flip-flops in a computer.

.....

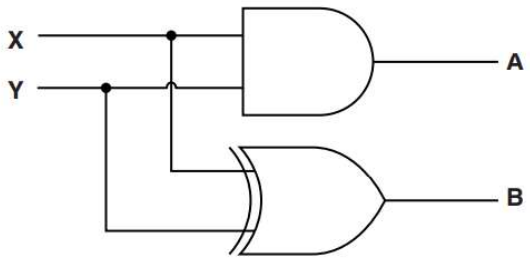
.....

.....

.....[2]

Question 17

4 **(a)** **(i)** Complete the truth table for this logic circuit.



Input		Output	
X	Y	A	B
0	0		
0	1		
1	0		
1	1		

[2]

(ii) State the name given to this logic circuit.

..... [1]

(iii) Name the labels usually given to **A** and **B**.

Label **A** .....

Label **B** .....

Explain why your answers are more appropriate for the **A** and **B** labels.

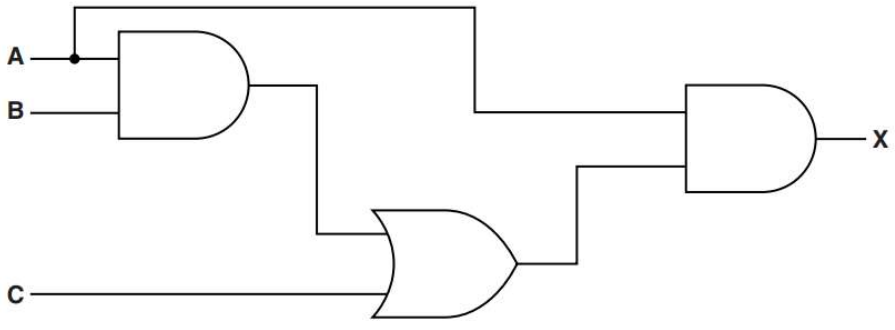
.....

.....

.....

..... [4]

(b) **(i)** Write the Boolean expression corresponding to the following logic circuit:



..... [2]

(ii) Use Boolean algebra to simplify the expression that you gave in **part (b)(i)**.

Show your working.

.....

.....

.....

.....

.....

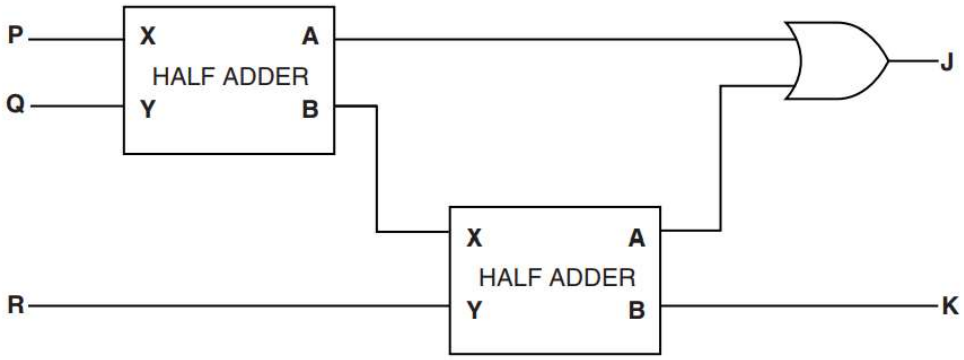
..... [3]

Question 18

5 **(a)** **(i)** A half adder is a logic circuit with the following truth table.

Input		Output	
X	**Y**	**A**	**B**
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

The following logic circuit is constructed.



Complete the following truth table for this logic circuit.

Input			Working space	Output	
P	**Q**	**R**		**J**	**K**
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

[2]

(ii) State the name given to this logic circuit.

..... [1]

(iii) Name the labels usually given to **J** and **K**.

Label **J** .....

Label **K** .....

Explain why your answers are appropriate labels for these outputs.

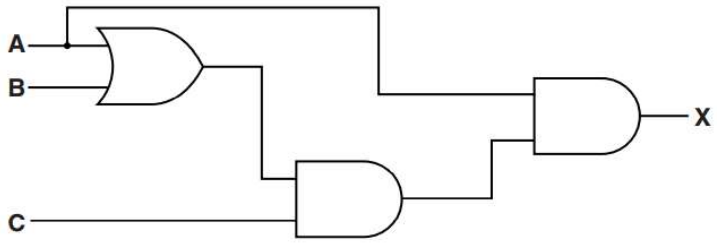
.....

.....

.....

..... [4]

(b) (i) Write down the Boolean expression corresponding to the following logic circuit:



..... [2]

(ii) Use Boolean algebra to simplify the expression given in **part (b)(i)**.

Show your working.

.....

.....

.....

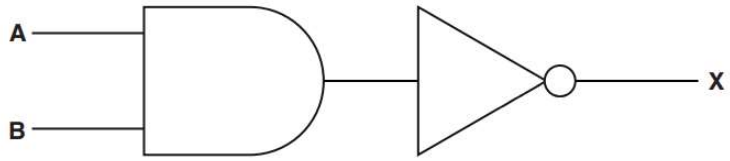
.....

.....

..... [4]

Question 19

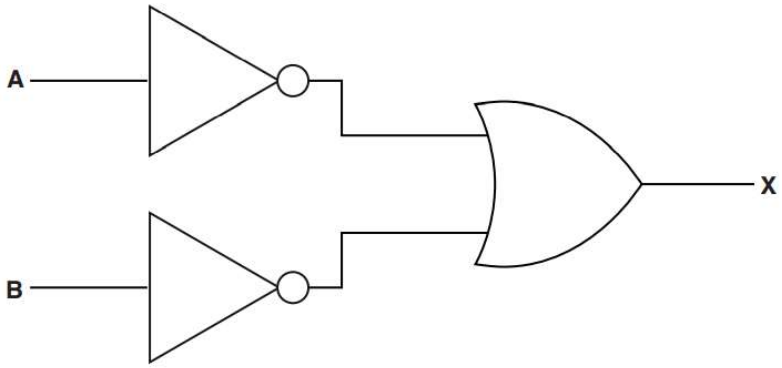
4 (a) (i) Complete the truth table for this logic circuit:



A	B	Working space	X
0	0		
0	1		
1	0		
1	1		

[1]

(ii) Complete the truth table for this logic circuit:



A	B	Working space	X
0	0		
0	1		
1	0		
1	1		

[1]

(b) A student decides to write an equation for **X** to represent the full behaviour of each logic circuit.

(i) Write the Boolean expression that will complete the required equation for **X** for each circuit:

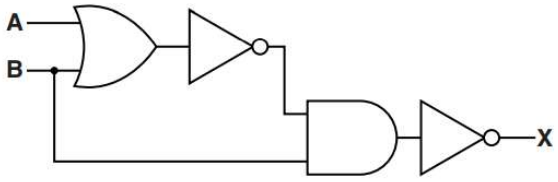
Circuit 1: **X** = ...

Circuit 2: **X** = ...[2]

(ii) Write the De Morgan's Law which is shown by your answers to **part (a)** and **part (b)(i)**.

.....[1]

(c) Write the Boolean algebraic expression corresponding to the following logic circuit:



.....[3]

(d) Using De Morgan's laws and Boolean algebra, simplify your answer to **part (c)**.

Show all your working.

.....

.....

.....

.....

.....

.....[3]

Question 20

5 (a) (i) Complete the Boolean function that corresponds to the following truth table.

INPUT			OUTPUT
A	**B**	**C**	**X**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

$X = \overline{A} \cdot B \cdot C +$ .....[3]

The part to the right of the equals sign is known as the sum-of-products.

(ii) For the truth table above complete the Karnaugh Map (K-map).

		AB			
		00	**01**	**11**	**10**
C	**0**				
	1				

[1]

The K-map can be used to simplify the function in **part(a)(i)**.

(iii) Draw loop(s) around appropriate groups of 1's to produce an optimal sum-of-products. [2]

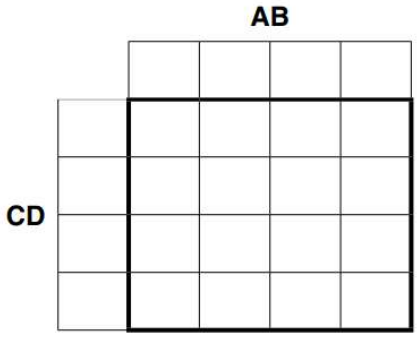
(iv) Using your answer to **part (a)(iii)**, write the simplified sum-of-products Boolean function.

X = ...[2]

(b) The truth table for a logic circuit with four inputs is given below:

INPUT				OUTPUT
A	**B**	**C**	**D**	**X**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

(i) Complete the K-map corresponding to the truth table above.



[4]

(ii) Draw loop(s) around appropriate groups of 1's to produce an optimal sum-of-products. [2]

(iii) Using your answer to **part (b)(ii)**, write the simplified sum-of-products Boolean function.

X = ...[2]

Question 21

5 (a) (i) Complete the Boolean function that corresponds to the following truth table.

INPUT			OUTPUT
P	**Q**	**R**	**Z**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

$Z = P \,.\, \overline{Q} \,.\, \overline{R} +$ .....[3]

The part to the right of the equals sign is known as the sum-of-products.

(ii) For the truth table above complete the Karnaugh Map (K-map).

		PQ			
		00	**01**	**11**	**10**
R	**0**				
	1				

[1]

The K-map can be used to simplify the function in **part(a)(i)**.

(iii) Draw loop(s) around appropriate groups of 1's to produce an optimal sum-of-products. [2]

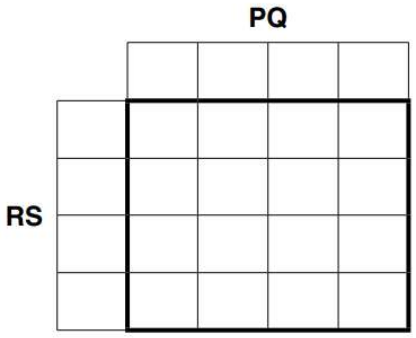
(iv) Using your answer to **part (a)(iii)**, write the simplified sum-of-products Boolean function.

Z = ...[1]

(b) The truth table for a logic circuit with four inputs is given below:

INPUT				OUTPUT
P	**Q**	**R**	**S**	**Z**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

(i) Complete the K-map corresponding to the truth table above.



[4]

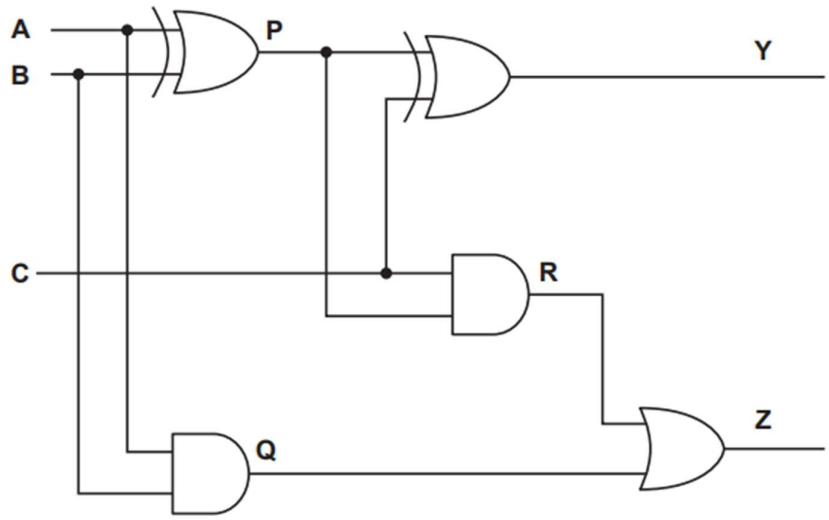
(ii) Draw loop(s) around appropriate groups of 1's to produce an optimal sum-of-products. [2]

(iii) Using your answer to **part (b)(ii)**, write the simplified sum-of-products Boolean function.

Z = ...[2]

Question 22

7 The diagram shows a logic circuit.



(a) Complete the truth table for the given logic circuit. Show your working.

Inputs			Working space			Outputs	
A	B	C	P	Q	R	Y	Z
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

[3]

(b) State the name of the logic circuit.

..... [1]

(c) Write the Boolean expressions for the two outputs **Y** and **Z** in the truth table as sum-of-products **and** state the purpose of each output.

Y = ...

Purpose .....

Z = ...

Purpose .....

[4]

Question 23

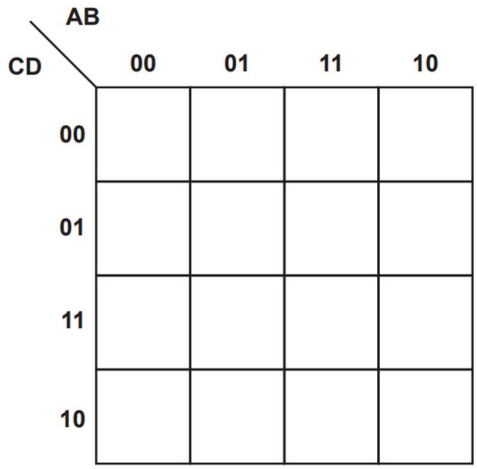
7 **(a)** Write the Boolean expression that corresponds to the given truth table as a sum-of-products.

INPUT				OUTPUT
A	**B**	**C**	**D**	**Z**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Z = ...

..... [3]

(b) (i) Complete the Karnaugh map (K-map) for the given truth table.



[2]

(ii) Draw loop(s) around appropriate group(s) of 1s in the K-map to produce an optimal sum-of-products. [2]

(iii) Write the Boolean expression from your answer to **part b(ii)** as a simplified sum-of-products.

Z = ...

..... [2]

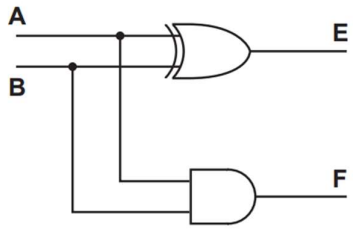
(iv) Write the simplified Boolean expression for your answer to **part b(iii)**.

Z = ...

..... [1]

Question 24

6 A logic circuit has two inputs **A** and **B**, and two outputs **E** and **F**.



(a) Complete the truth table for this logic circuit.

INPUT		OUTPUT	
A	**B**	**E**	**F**
0	0		
0	1		
1	0		
1	1		

[2]

(b) (i) State the name of this logic circuit.

..... [1]

(ii) State the purpose of each output **E** and **F**.

Purpose of **E** .....

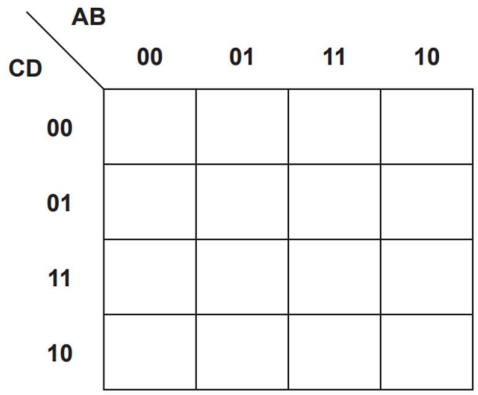
Purpose of **F** .....

[2]

Question 25

7 **(a)** Complete the Karnaugh map (K-map) for the Boolean expression.

$$Z = \overline{A}.B.\overline{C}.\overline{D} + \overline{A}.B.\overline{C}.D + A.B.\overline{C}.\overline{D} + A.B.\overline{C}.D + A.\overline{B}.\overline{C}.\overline{D} + A.\overline{B}.\overline{C}.D$$



[2]

(b) Draw loop(s) around appropriate group(s) in the K-map to produce an optimal sum-of-products. [2]

(c) Write the Boolean expression from your answer to **part (b)** as a simplified sum-of-products. Use Boolean algebra to give your answer in its simplest form.

Simplified sum-of-products

Z = ...

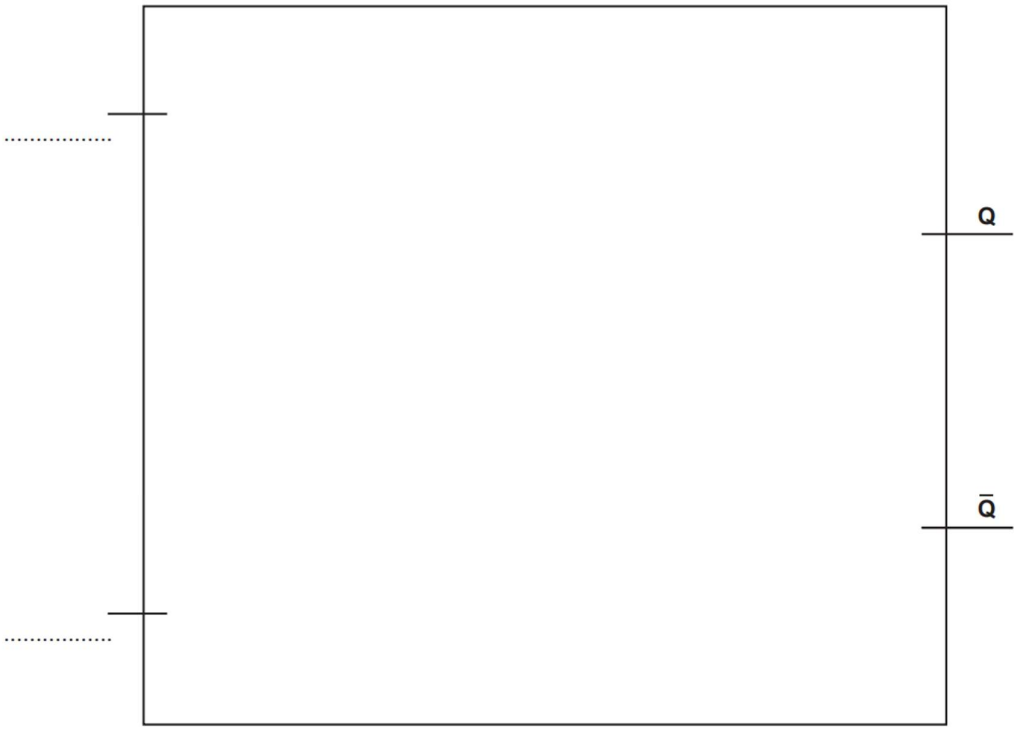
Simplest form

Z = ...

[3]

Question 26

8 **(a)** Draw a logic circuit for an SR flip-flop **and** label the inputs.



[4]

(b) State the purpose of a flip-flop.

.....

..... [1]

(c) Simplify the following expression using Boolean algebra, including De Morgan's laws.
Show your working.

$$\overline{\overline{(A.B)}.\overline{(A.C)}.\overline{(B.D)}}$$

Working .....

.....

.....

.....

.....

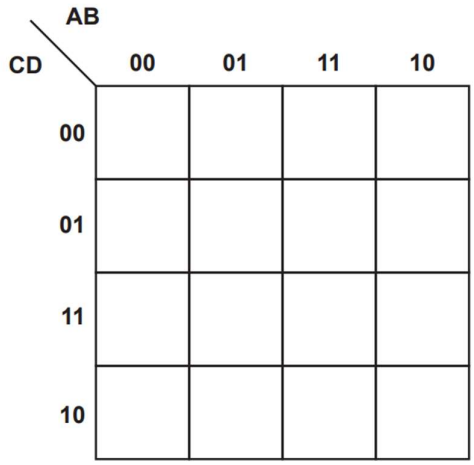
Answer .....

[3]

Question 27

7 **(a)** Complete the Karnaugh map (K-map) for the following Boolean expression.

$$Z = \overline{A}.\overline{B}.\overline{C}.\overline{D} + \overline{A}.\overline{B}.\overline{C}.D + \overline{A}.B.\overline{C}.\overline{D} + \overline{A}.B.\overline{C}.D + A.B.\overline{C}.\overline{D} + A.B.\overline{C}.D$$



[2]

(b) Draw loop(s) around appropriate group(s) in the K-map to produce an optimal sum-of-products. [2]

(c) Write the Boolean logic expression from your answer to **part (b)** as a simplified sum-of-products.

Z = ...

..... [2]

(d) Use Boolean algebra to give your answer to **part (c)** in its simplest form.

Z = ... [1]

Question 28

9 This truth table represents a logic circuit.

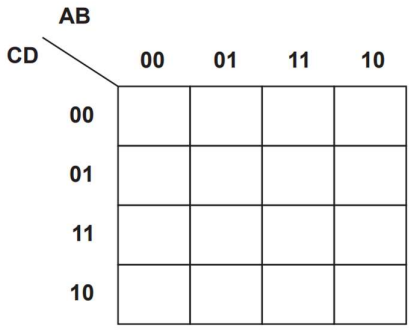
INPUT				OUTPUT
A	**B**	**C**	**D**	**Z**
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

(a) Write the Boolean logic expression that corresponds to the given truth table as the sum-of-products.

Z = ...

..... [3]

(b) Complete the Karnaugh map (K-map) for the given truth table.



[2]

(c) Draw loop(s) around appropriate group(s) in the K-map to produce an optimal sum-of-products. [2]

(d) Write the Boolean logic expression from your answer to **part (c)** as a simplified sum-of-products.

Z = ...

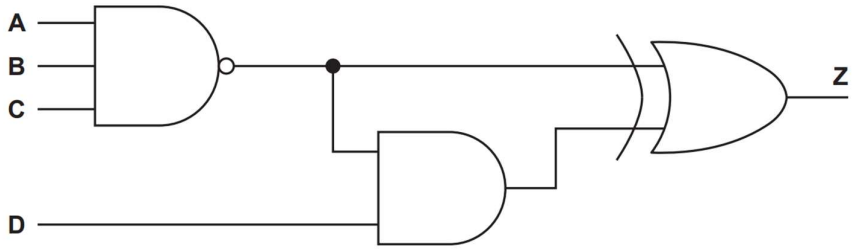
..... [2]

(e) Use Boolean algebra to give your answer to **part (d)** in its simplest form.

Z = ... [1]

Question 29

6 This diagram represents a logic circuit.



(a) Complete the truth table for the given logic circuit.

A	B	C	D	Working space	Z
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

[3]

(b) Simplify the given Boolean expression using Boolean algebra.
Show your working.

$Y = \overline{A}.\overline{B}.\overline{C}.\overline{D} + \overline{A}.\overline{B}.C.\overline{D} + \overline{A}.B.\overline{C}.\overline{D} + \overline{A}.B.C.\overline{D}$

.....

.....

.....

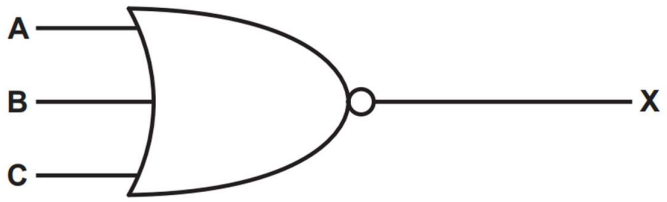
.....

.....

..... [3]

Question 30

7 **(a)** This logic circuit represents the Boolean expression: $X = \overline{A + B + C}$



Complete this truth table for the given logic circuit.

A	B	C	X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

[1]

(b) Apply De Morgan's laws to the expression: $X = \overline{A + B + C}$

X = ... [1]

(c) Simplify the following expression using Boolean algebra.

Show all the stages in your simplification.

$T = X.Y.Z + X.\overline{Y}.Z + \overline{X}$

.....

.....

.....

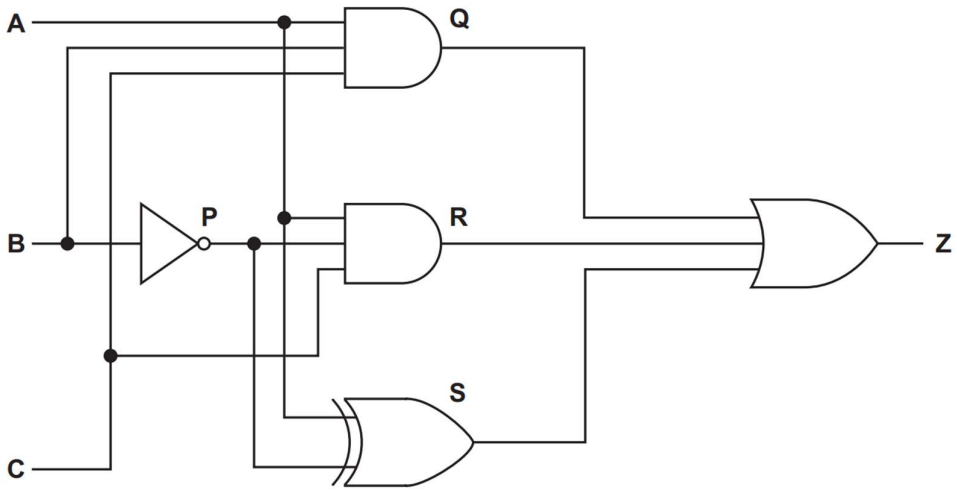
.....

.....

..... [3]

Question 31

6 The diagram shows a logic circuit.



(a) Complete the truth table for the given logic circuit.

Show your working.

			Working space				
A	**B**	**C**	**P**	**Q**	**R**	**S**	**Z**
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

[3]

(b) Write the Boolean expression that corresponds to the logic circuit as a sum-of-products.

Z = ...

.....

.....

..... [2]

(c) (i) Complete the Karnaugh map (K-map) for the Boolean expression:

$\overline{A}.\overline{B}.\overline{C} + \overline{A}.\overline{B}.C + A.\overline{B}.\overline{C} + A.\overline{B}.C + A.B.\overline{C} + A.B.C$

A \ BC	00	01	11	10
0				
1				

[2]

(ii) Draw loop(s) around appropriate group(s) in the K-map to produce an optimal sum-of-products. [2]

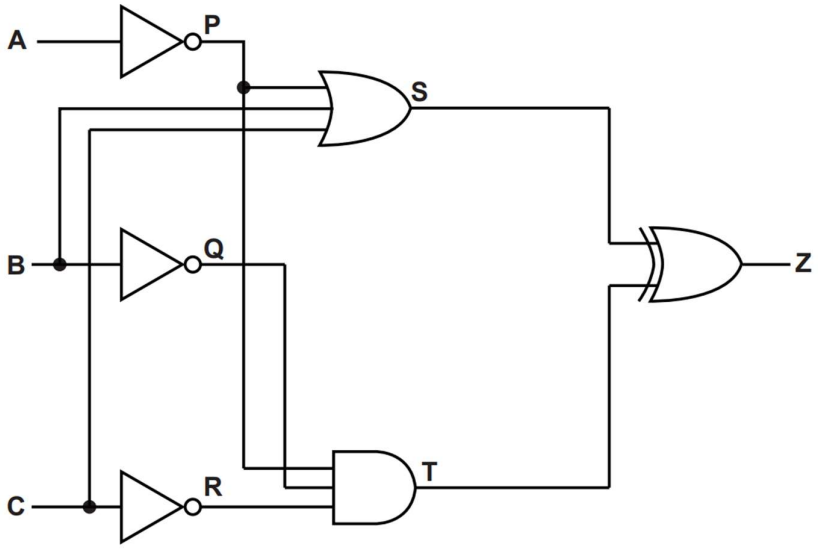
(iii) Write the Boolean expression from your answer to part **(c)(ii)** as a simplified sum-of-products.

.....

..... [1]

Question 32

6 The diagram shows a logic circuit.



(a) Complete the truth table for the given logic circuit.
Show your working.

			Working space					
A	**B**	**C**	**P**	**Q**	**R**	**S**	**T**	**Z**
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						

[3]

(b) Write the Boolean expression that corresponds to the logic circuit as a sum-of-products.

Z = ...

.....

.....

..... [2]

(c) **(i)** Complete the Karnaugh map (K-map) for this Boolean expression:

$\overline{A}.\overline{B}.\overline{C} + \overline{A}.B.\overline{C} + \overline{A}.B.C + A.\overline{B}.\overline{C} + A.B.\overline{C} + A.B.C$

A \ BC	00	01	11	10
0				
1				

[2]

(ii) Draw loop(s) around appropriate group(s) in the K-map to produce an optimal sum-of-products. [2]

(iii) Write the Boolean expression from your answer to part **c(ii)** as a simplified sum-of-products.

.....

..... [1]

Answers

Answer 1

4(a)	X = ((P XOR Q) XOR R) Y = ((P XOR Q) AND R) OR (P AND Q) or $X = \overline{(\overline{P}.Q + P.\overline{Q})}.R + (\overline{P}.Q + P.\overline{Q}).\overline{R}$ $Y = (\overline{P}.Q + P.\overline{Q}).R + P.Q$ **One** mark for correct use of XOR **One** mark for correct use of AND **One** mark for correct use of OR **One** mark for X correct **One** mark for Y correct	**5**
4(b)(i)	X: Sum Y: Carry (out)	**2**
4(b)(ii)	Carry (in)	**1**

Answer 2

4(a)	For each expression, **2** marks all products correct no incorrect products seen, **1** mark 2 or 3 products correct, max 4 $X = \overline{A}.\overline{B}.C + \overline{A}.B.\overline{C} + A.\overline{B}.\overline{C} + A.B.C$ $Y = \overline{A}.B.C + A.\overline{B}.C + A.B.\overline{C} + A.B.C$	**4**
4(b)	**One** mark for each correct K-map max 2 OUTPUT X AB C | 00 | 01 | 11 | 10 0 | 0 | 1 | 0 | 1 1 | 1 | 0 | 1 | 0 OUTPUT Y AB C | 00 | 01 | 11 | 10 0 | 0 | 0 | 1 | 0 1 | 0 | 1 | 1 | 1	**2**
4(c)(i)	**One** mark for OUTPUT X no loops OUTPUT Y **one** mark vertical loop correct **one** mark horizontal loops correct OUTPUT X AB C | 00 | 01 | 11 | 10 0 | 0 | 1 | 0 | 1 1 | 1 | 0 | 1 | 0 OUTPUT Y AB C | 00 | 01 | 11 | 10 0 | 0 | 0 | 1 | 0 1 | 0 | 1 | 1 | 1	**3**

4(c)(ii)	**One** mark for each correct product and no incorrect products max 3 A.B + B.C + A.C	**3**
4(d)	Logic circuit: Full Adder X: Sum Y: Carry	**3**

Answer 3

4(a)	For X **1** mark for all products correct For Y **2** marks for 3 products correct, no other products seen $X = \bar{A}.\bar{B}.\bar{C} + A.B.C$ $Y = \bar{A}.B.C + A.\bar{B}.C + A.B.C$	**3**
4(b)	**One** mark for each correct K-map max 2 **OUTPUT X** **AB** **C** \ **00** **01** **11** **10** **0** 1 0 0 0 **1** 0 0 1 0 **OUTPUT Y** **AB** **C** \ **00** **01** **11** **10** **0** 0 0 0 0 **1** 0 1 1 1	**2**
4(c)(i)	**One** mark for OUTPUT X no loops **One** mark for OUTPUT Y all loops correct and no others max 2 **OUTPUT X** **AB** **C** \ **00** **01** **11** **10** **0** 1 0 0 0 **1** 0 0 1 0 **OUTPUT Y** **AB** **C** \ **00** **01** **11** **10** **0** 0 0 0 0 **1** 0 1 1 1	**2**
4(c)(ii)	**One** mark for each correct product A.C + B.C	**2**

Answer 4

5	(logic) Circuit // bi-stable Two Memory // data storage // registers // storing one bit of data JK/SR/D/T SR/JK/T/D	**5**

Answer 5

<table>
<tr><td>3(a)</td><td>NOR</td><td>1</td></tr>
<tr><td>3(b)(i)</td><td>1 mark for X column, 1 mark for Y column

<table>
<tr><th>A</th><th>B</th><th>Working Space</th><th>X</th><th>Y</th></tr>
<tr><td>0</td><td>0</td><td></td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td></td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td></td><td>1</td><td>0</td></tr>
</table></td><td>2</td></tr>
<tr><td>3(b)(ii)</td><td>Half adder</td><td>1</td></tr>
<tr><td>3(b)(iii)</td><td>1 mark per bullet
∞ X is (used for) carry
∞ Y is (used for) sum</td><td>2</td></tr>
<tr><td>3(c)</td><td>1 mark per bullet for working (max 4)

$\bar{A}.\bar{B}.\bar{C}.\bar{D} + \overline{A.B}.\bar{C}.D + \overline{A.B}.C.D + \bar{A}.\overline{B.C}.\bar{D} + \bar{A}.B.\bar{C}.\bar{D}$
$= \bar{A}.\bar{B}.\bar{C}.\bar{D} + \overline{A.B}.\bar{C}.D + \overline{A.B}.C.D + \bar{A}.\overline{B.C}.\bar{D} + \bar{A}.B.\bar{C}.\bar{D} + \bar{A}.\bar{B}.\bar{C}.\bar{D}$
∞ Adding in a second copy of the first term (Use of Idempotent Law)

$= \bar{A}.\bar{B}.\left(\bar{C}.\bar{D} + \bar{C}.D + C.D + C.\bar{D}\right) + \bar{A}.\bar{C}.\bar{D}.\left(B + \bar{B}\right)$
∞ Taking $\bar{A}.\bar{B}$ and $\bar{A}.\bar{C}.\bar{D}$ outside brackets (Associative Law)

$= \bar{A}.\bar{B}.\left(\bar{C}.\left(\bar{D} + D\right) + C.\left(D + \bar{D}\right)\right) + \bar{A}.\bar{C}.\bar{D}.\left(B + \bar{B}\right)$
∞ Grouping $\bar{C}.\left(\bar{D} + D\right) + C.\left(D + \bar{D}\right)$ (Associative Law and Commutative Law)

$= \bar{A}.\bar{B}.\left(\bar{C}.(1) + C.(1)\right) + \bar{A}.\bar{C}.\bar{D}.(1)$
$= \bar{A}.\bar{B}.\left(\bar{C} + C\right) + \bar{A}.\bar{C}.\bar{D}.(1)$
$= \bar{A}.\bar{B}.(1) + \bar{A}.\bar{C}.\bar{D}.(1)$
∞ Replacing $\left(D + \bar{D}\right)$ with 1 and replacing $\left(\bar{C} + C\right)$ with 1 (Use of Complement Law)

$= \bar{A}.\bar{B} + \bar{A}.\bar{C}.\bar{D}$
∞ Reducing first four terms to $\bar{A}.\bar{B}$ and reducing last two terms to $\bar{A}.\bar{C}.\bar{D}$ (Use of Identity Law)

1 mark for correct answer
$= \bar{A}.(\bar{B} + \bar{C}.\bar{D})$</td><td>5</td></tr>
</table>

Answer 6

3(a)(i) — **1**

C \ AB	00	01	11	10
0	1	1	0	1
1	1	1	0	1

3(a)(ii) — **2**

1 mark for each correct loop

C \ AB	00	01	11	10
0	1	1	0	1
1	1	1	0	1

3(a)(iii) — **2**

1 mark per bullet point

- $\overline{A}$
- $+\overline{B}$

$X = \overline{A} + \overline{B}$

3(b)(i) — **4**

1 mark correct values and order of row and column headings

3 marks fully correct table entries (based on headings) or
2 marks table entries contain one error (based on headings) or
1 mark table entries contain two errors (based on headings)

CD \ AB	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	1	1	0	0
10	1	1	0	0

3(b)(ii) — **2**

1 mark per loop

CD \ AB	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	1	1	0	0
10	1	1	0	0

3(b)(iii) — **2**

1 mark for each bullet point

- $\overline{A}.C$
- $+ A.\overline{C}$

$X = \overline{A}.C + A.\overline{C}$

Answer 7

4(a)	**1 mark** for 3 or 4 correct products **2 marks** for all 5 correct products $X = \overline{A}.\overline{B}.\overline{C} + \overline{A}.\overline{B}.C + \overline{A}.B.C + A.\overline{B}.C + A.B.C$	**2**
4(b)	**1 mark** for correct answer AB C 00 01 11 10 0: 1 0 0 0 1: 1 1 1 1	**1**
4(c)	1 mark per correct loop AB C 00 01 11 10 0: 1 0 0 0 1: 1 1 1 1	**2**
4(d)	**1 mark** per bullet point. • $\overline{A}.\overline{B}$ • $+C$ $X = \overline{A}.\overline{B} + C$ // $X = C + \overline{A}.\overline{B}$	**2**

Answer 8

2(a)(i)	1 mark for each 2 correct products, i.e. 3 marks for 6, 2 marks for 4 or 5, 1 mark for 2 or 3 $\mathbf{X = \overline{A}.\overline{B}.\overline{C} + \overline{A}.\overline{B}.C + \overline{A}.B.\overline{C} + \overline{A}.B.C + A.\overline{B}.\overline{C} + A.\overline{B}.C}$	**3**
2(a)(ii)	1 mark for the correct K-map **AB** **C** 00 01 11 10 0: 1 1 0 1 1: 1 1 0 1	**1**
2(a)(iii)	1 mark for each correct loop **AB** **C** 00 01 11 10 0: 1 1 0 1 1: 1 1 0 1	**2**

2(a)(iv)	1 mark per bullet point: • $\overline{A}$ • $+\overline{B}$ $X = \overline{A} + \overline{B}$ // $X = \overline{B} + \overline{A}$	2
2(b)	$X = \left(\overline{(\overline{W} + X).(Y + \overline{Z})}\right)$ One mark for correct use of De Morgan's law to + • $X = \overline{(\overline{W} + X)} + \overline{(Y + \overline{Z})}$ One mark for correct use of De Morgan's law + to • $X = \overline{\overline{W}}.\overline{X} + \overline{Y}.\overline{\overline{Z}}$ One mark for correct answer • $X = W.\overline{X} + \overline{Y}.Z$	3

Answer 9

4(a)(i)	**2** marks all products correct, **1** mark 2 or 3 products correct $X = \overline{A}.B.\overline{C} + \overline{A}.B.C + A.\overline{B}.\overline{C} + A.\overline{B}.C$	2
4(a)(ii)	**1** mark for all correct bits **AB** **C** | **00** | **01** | **11** | **10** **0** | 0 | 1 | 0 | 1 **1** | 0 | 1 | 0 | 1	1
4(a)(iii)	**1** mark for each correct loop **AB** **C** | **00** | **01** | **11** | **10** **0** | 0 | (1) | 0 | (1) **1** | 0 | (1) | 0 | (1)	2
4(a)(iv)	**1** mark per bullet – allow follow through from **4(a)(iii)** ∞ $\overline{A}.B$ ∞ $+A.\overline{B}$ $X = \overline{A}.B + A.\overline{B}$	2

4(b)(i)	**1** mark per bullet max **2** ∞ Correct column headings and row headings – values only ∞ Correct column headings and row headings – order 1 mark for 2 correct rows/columns, 2 marks for 4 correct rows/columns (based on headings) max **2** **AB** **CD** **00** **01** **11** **10** **00** 0 1 1 0 **01** 0 1 1 0 **11** 0 1 0 0 **10** 0 1 0 0	**4**
4(b)(ii)	**1** mark for each correct loop **CD** **00** **01** **11** **10** **00** 0 1 1 0 **01** 0 1 1 0 **11** 0 1 0 0 **10** 0 1 0 0	**2**
4(b)(iii)	**1** mark per bullet $\bar{A}.B$ $+B.\bar{C}$ $X = \bar{A}.B + B.\bar{C}$	**2**

Answer 10

4(a)(i)	1 mark for 2 or 3 correct, 2 marks for 4 correct $X = \bar{A}.B.C + A.\bar{B}.C + A.B.\bar{C} + A.B.C$	**2**
4(a)(ii)	1 mark for the correct K-map **AB** **C** **00** **01** **11** **10** **0** 0 0 1 0 **1** 0 1 1 1	**1**
4(a)(iii)	1 mark for each loop max 3 **AB** **C** **00** **01** **11** **10** **0** 0 0 1 0 **1** 0 1 1 1	**3**

4(a)(iv)	1 mark for each pair. Allow follow through from **(iii)** ∞ A.B ∞ +B.C ∞ +A.C $X = A.B + B.C + A.C$	**3**
4(b)(i)	1 mark per bullet point max 2: ∞ Correct column headings and row headings – values only ∞ Correct column headings and row headings – order 1 mark for 2 correct rows or columns, 2 marks for 4 correct rows or columns (based on headings) **AB** **CD** **00** 0 1 1 0 **01** 0 0 1 0 **11** 0 0 1 0 **10** 0 0 1 0	**4**
4(b)(ii)	1 mark per loop **AB** **CD** **00** 0 1 1 0 **01** 0 0 1 0 **11** 0 0 1 0 **10** 0 0 1 0	**2**
4(b)(iii)	1 mark per bullet point: ∞ A.B ∞ $+B\bar{C}.\bar{D}$ $X = A.B + B\bar{C}.\bar{D}$	**2**

Answer 11

3(a)

1 mark per bullet point to max 3:

- Correct use of Idempotent law $Y = Y.Y \quad Y = Y + Y$
- Correct use of Complement law $0 = Y.\overline{Y} \quad 1 = Y + \overline{Y}$
- Correct use of Distributive law $X(Y + Z) = X.Y + X.Z$
- Correct use of Redundancy law $X.\overline{Y} + Y = X + Y$
- Correct use of identity law $X.1 = X$

1 mark for the correct answer

For example:

$X = A.\overline{B}.\overline{C} + A.B.\overline{C} + A.B.C$	Idempotent law
$X = A.\overline{B}.\overline{C} + A.B.\overline{C} + A.B.\overline{C} + A.B.C$	Distributive law
$X = A.\overline{C}.(\overline{B} + B) + A.B.(\overline{C} + C)$	Complement/Inverse law
$X = A.\overline{C} + A.B$	
$X = A.(\overline{C} + B)$	Correct answer
$X = A.\overline{B}.\overline{C} + A.B.\overline{C} + A.B.C$	Distributive law
$X = A.\overline{C}.(\overline{B} + B) + A.B.C$	Complement/Inverse law
$X = A.\overline{C} + A.B.C$	
$X = A.(\overline{C} + B.C)$	Redundancy Law
$X = A.(\overline{C} + B)$	Correct answer

3(b)(i)

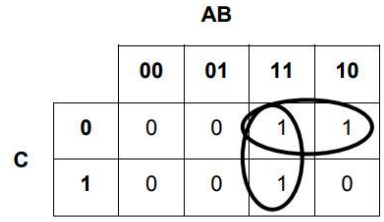
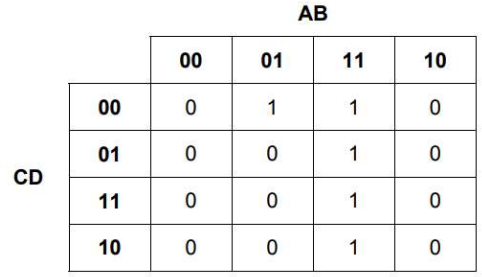
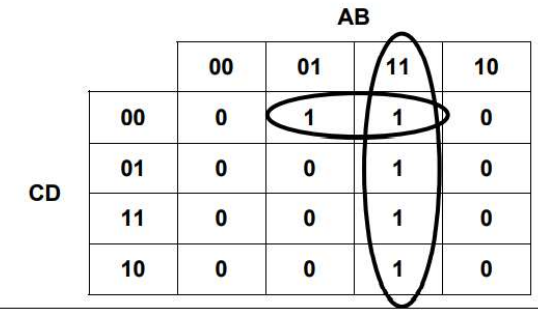
1 mark for first four as 0, 1 mark for 1011

A	B	C	X	
0	0	0	0	1 mark
0	0	1	0	
0	1	0	0	
0	1	1	0	
1	0	0	1	1 mark
1	0	1	0	
1	1	0	1	
1	1	1	1	

3(b)(ii)

1 mark for correct K-map

		AB			
		00	**01**	**11**	**10**
C	**0**	0	0	1	1
	1	0	0	1	0

3(b)(iii)	1 mark for each correct loop to max 2 
3(b)(iv)	1 mark per bullet point: • $A.\overline{C}$ • + A.B $X = A.\overline{C} + A.B$
3(c)(i)	1 mark per bullet point to max 2: • Correct column headings and row headings – values only • Correct column headings and row headings – order 1 mark for 2 correct rows or columns, 2 marks for 4 correct rows or columns (based on headings) 
3(c)(ii)	1 mark for each correct loop to max 2: 
3(c)(iii)	1 mark per bullet point: • A.B • + $B.\overline{C}.\overline{D}$ $X = A.B + B.\overline{C}.\overline{D}$

Answer 12

3(a)	$X = A.(\overline{B} + (B \,.\, C))$ B.C 1 $\overline{B}$ + B.C 1 A. 1	3

3(b)	<table><tr><th>A</th><th>B</th><th>C</th><th>Working Space</th><th>X</th></tr><tr><td>0</td><td>0</td><td>0</td><td></td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td></td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td></td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td></td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td></td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td></td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td></td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td></td><td>1</td></tr></table> 1 mark first four entries, 1 mark for the last four entries	2
3(c)(i)	<table><tr><td></td><td></td><td colspan="4">AB</td></tr><tr><td></td><td></td><td>00</td><td>01</td><td>11</td><td>10</td></tr><tr><td>C</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td></td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr></table>	1
3(c)(ii)	<table><tr><td></td><td></td><td colspan="4">AB</td></tr><tr><td></td><td></td><td>00</td><td>01</td><td>11</td><td>10</td></tr><tr><td>C</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td></td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr></table>	2
3(c)(iii)	$X = A.\overline{B} + A.C$ 1 1	2
3(d)	$X = A.(\overline{B} + (B \cdot C))$ $X = A.(\overline{B} + C)$ 1 $X = A.\overline{B} + A.C$ 1 (dependent mark – must be correct outcome from previous line)	2

Answer 13

3(a)	$S = (\overline{P} + (\overline{Q+R})) . R$ $\overline{P}$ 1 $(\overline{Q+R})$ 1 $(\overline{P}+(\overline{Q+R}))$ 1 . R (must be outside final brackets) 1 Or $\overline{P}$ 1 $(\overline{Q+R})$ 1 $\overline{P}+(\overline{Q+R})$ 1 (.....). R 1	4

3(b) — **2**

P	Q	R	Working space	S
0	0	0		0
0	0	1		1
0	1	0		0
0	1	1		1
1	0	0		0
1	0	1		0
1	1	0		0
1	1	1		0

2 marks all correct, 1 mark seven correct, 0 marks six or fewer correct

3(c)(i) — **1**

R \ PQ	00	01	11	10
0	0	0	0	0
1	1	1	0	0

3(c)(ii) — **1**

R \ PQ	00	01	11	10
0	0	0	0	0
1	1	1	0	0

3(c)(iii) — **1**

$S = \overline{P} \cdot R$

3(d) — **3**

$S = (\overline{P} + (\overline{Q+R})) \cdot R$

$S = (\overline{P} + (\overline{Q} \cdot \overline{R})) \cdot R \;//\; \overline{P} \cdot R + (\overline{Q+R}) \cdot R$ 1

$S = (\overline{P} \cdot R) + (\overline{Q} \cdot \overline{R} \cdot R)$ 1

$S = \overline{P} \cdot R + \overline{Q} \cdot 0$)

$S = \overline{P} \cdot R + 0$) 1

$S = \overline{P} \cdot R$

Answer 14

5(a)(i)		1

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

5(a)(ii) — **1**

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

5(b)(i) — **3**

	S	R	Q	$\overline{Q}$	
Initially	1	0	0	1	
R changed to 1	1	1	**0**	**1**	1
S changed to 0	0	1	**1**	**0**	1
S changed to 1	1	1	**1**	**0**	1
S and R changed to 0	0	0	1	1	

5(b)(ii) — **2**

- Q and $\overline{Q}$ have same value
- Q and $\overline{Q}$ should be complements of each other
- Flip-flop becomes unstable

1 mark for each point, **max 2**

5(c)(i) — **4**

J	K	Clock	Working space	Initial values Q	Initial values $\overline{Q}$	Final values Q	Final values $\overline{Q}$
0	0	1		1	0	1	0
0	0	1		0	1	0	1
0	1	1		1	0	0	1
0	1	1		0	1	0	1
1	0	1		1	0	**1**	**0**
1	0	1		0	1	**1**	**0**
1	1	1		1	0	**0**	**1**
1	1	1		0	1	**1**	**0**

1 mark per shaded row

5(c)(ii) — **2**

- S-R flip-flop has an invalid combination of S and R // The S_R flip flop allows both Q and $\overline{Q}$ to have the same value // S-R flip-flop inputs may arrive at different times 1
- The J-K flip-flop does not allow for Q and $\overline{Q}$ to have the same value // All four combination of values for J and K are valid // J-K flip-flop incorporates a clock pulse for synchronisation 1

5(d) — **2**

- A flip-flop can store either a 0 or a 1
- Computers use bits to store data
- Flip-flops can therefore be used to store bits (of data)
- Memory can be created from flip-flops

1 mark for valid point, **max 2**

Answer 15

5(a) — **1**

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

5(b) — **4**

	S	R	Q	$\overline{Q}$	
Initially	1	0	1	0	
S changed to 0	0	0	1	0	(1)
R changed to 1	0	1	0	1	(1)
R changed to 0	0	0	0	1	(1)
S and R changed to 1	1	1	0	0	(1)

5(c)(i) — Clock (pulse) — **1**

5(c)(ii) — **4**

Max 2 marks per problem – **max 4 marks**

Problem 1

- One combination of S and R gives NOT valid / indeterminate output // Q and $\overline{Q}$ have the same value
- The JK flip-flop does not allow for Q and $\overline{Q}$ to have the same value for any combination of inputs // $\overline{Q}$ and Q have to be complementary

Problem 2

- Inputs may not arrive at the same time
- The JK flip-flop has a clock pulse to synchronise inputs

Answer 16

5 (a)	<table><tr><th>A</th><th>B</th><th>X</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	**1**
(b) (i)	<table><tr><th>S</th><th>R</th><th>Q</th><th>$\overline{Q}$</th></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td></tr></table>	**1** **1** **1** **1**

(ii)	S = 0 R = 0 Produces Q = 1 , $\overline{Q}$ =1 // Q and $\overline{Q}$ have same value But Q and $\overline{Q}$ should be complements of each other Becomes unstable	**1** **1** **1** **1** **Max 3**
(c) (i)	Clock (pulse)	**1**
(ii)	All four possibilities are valid The 1-1 combination changes output to logical complement Unstable state avoided Invalid state cannot occur // the flip-flop is stable	**1** **1** **1** **1** **Max 1**
(d)	Memory // data storage Stores a single bit	**1** **1**

Answer 17

4 (a) (i)

Input		Output	
X	**Y**	**A**	**B**
0	**0**	0	0
0	**1**	0	1
1	**0**	0	1
1	**1**	1	0

1 mark for each correct column (A and B)

[2]

(ii) Half adder [1]

(iii) C // Carry [1]
S // Sum [1]

represents the carry part of the addition of two bits [1]
represents the sum part of the addition of two bits [1]

(b) (i) A. [1]
(A.B + C) [1]

(ii) Allow follow through from **(b)(i)**

A.(A.B+C)
= A.A.B + A.C
= A.B +A.C
= A.(B+C)

1 mark for each correct simplification line – max 2 [2]
1 mark for A.(B+C) if correct answer to part **(b)(i)** [1]

Answer 18

5 (a) (i)

Input			Working space	Output	
P	Q	R		J	K
0	0	0		0	0
0	0	1		0	1
0	1	0		0	1
0	1	1		1	0
1	0	0		0	1
1	0	1		1	0
1	1	0		1	0
1	1	1		1	1

1 mark each column

If zero marks then
6 or 7 pairs correct – 1 mark

[2]

(ii) Full adder [1]

(iii) C / Carry [1]
S / Sum [1]
represents the carry part of the addition of three bits [1]
represents the sum part of the addition of three bits [1]

(b) (i) A. [1]
(A+B).C [1]

(ii) Allow follow through from **(b)(i)**

A. ((A+B).C)
= A.(A.C + B.C)
= A.A.C +A.B.C
= A.C + A.B.C
= A.C (1 + B)
=A.C.1
= A.C

1 mark for each correct simplification line – max 3 [3]
1 mark for A.C if correct answer to part **(b)(i)** [1]

[4]

Answer 19

4 (a) (i)

Circuit 1		
A	B	X
0	0	**1**
0	1	**1**
1	0	**1**
1	1	**0**

1

(ii)	Circuit 2 A | B | X 0 | 0 | **1** 0 | 1 | **1** 1 | 0 | **1** 1 | 1 | **0**	1
(b) (i)	• circuit 1: $\overline{A.B}$ • circuit 2: $\overline{A} + \overline{B}$	1 1
(ii)	$\overline{A.B} \equiv \overline{A} + \overline{B}$	1
(c)	$\overline{\overline{(A+B)}.B}$ Mark as follows: $\overline{(A+B)}$ $.B$ bar over whole expression	 1 1 1
(d)	$\overline{\overline{(A+B)}.B}$ $= \overline{\overline{(A+B)}} + \overline{B}$ $= (A+B) + \overline{B}$ $= A + (B + \overline{B})$ $= A + 1$ $= 1$ allow f.t. from **(c)**	 1 1 1 1 1 [max 3]

Question 20

5 **(a)** **(i)** $\overline{A}.B.C +$ [1]

$A.B.\overline{C}$ [1]

$+$

$A.B.C$ [1]

(ii)

		AB			
		00	**01**	**11**	**10**
C	**0**	0	0	1	0
	1	0	1	1	0

[1]

(iii)

C \ AB	00	01	11	10
0	0	0	1	0
1	0	1	1	0

1 mark for each loop

Allow f.t. from **(ii)**

[2]

(iv) X =

A.B [1]

+ B.C [1]

Allow f.t. from **(iii)**

(b) (i)

CD \ AB	00	01	11	10
00	0	1	1	0
01	0	0	0	0
11	0	0	1	0
10	0	1	1	0

1 mark row headings

1 mark column headings

1 mark per 2 correct rows (based on headings)

[4]

(ii)

CD \ AB	00	01	11	10
00	0	1	1	0
01	0	0	0	0
11	0	0	1	0
10	0	1	1	0

1 mark for loop with two 1s

1 mark for looping the four 1s

[2]

(iii) X =

$B.\overline{D}$ [1]

+ A.B.C [1]

Answer 21

5 (a) (i)

$$Z = P.\overline{Q}.\overline{R} +$$ [1]

$$P.\overline{Q}.R +$$ [1]

$$P.Q.R$$ [1]

(ii)

R \ PQ	00	01	11	10
0	0	0	0	1
1	0	0	1	1

[1]

(iii) 1 mark each loop

R \ PQ	00	01	11	10
0	0	0	0	1
1	0	0	1	1

Allow f.t. from **(ii)** [2]

(iv)

$$Z = P.\overline{Q}$$ [1]

$$+P.R$$ [1]

Allow f.t. from **(iii)**

(b) (i) 1 mark row headings. 1 mark column headings.
1 mark per 2 correct rows (based on headings)

RS \ PQ	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	0	1	1	0
10	0	0	0	0

[4]

(ii) 1 mark for loop with two 1s; 1 mark for loop with four 1s

RS \ PQ	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	0	1	1	0
10	0	0	0	0

Allow f.t. from **(i**
–1 for each incorrect grouping, max. 2 errors [2]

(iii)

$Z = Q.S$ [1]

$+P.R.\overline{S}$ [1]

Allow f.t. from **(ii).** –1 error if more than 2 terms

[Total: 16]

Answer 22

Question	Answer	Marks
7(a)	**One** mark for working, (all three columns P, Q and R) **One** mark for each correct column Y, Z	**3**
7(b)	Full adder	**1**

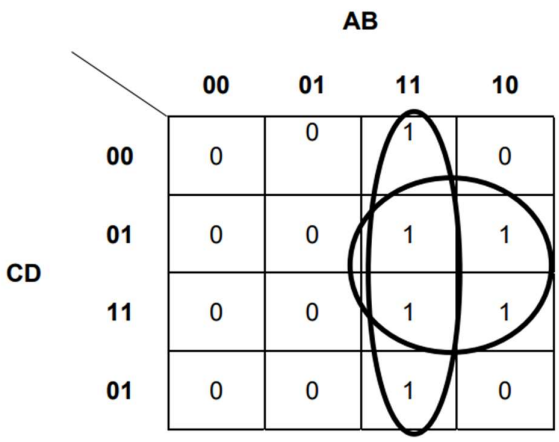
A	B	C	P	Q	R	Y	Z
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	1	0	0	1	0
0	1	1	1	0	1	0	1
1	0	0	1	0	0	1	0
1	0	1	1	0	1	0	1
1	1	0	0	1	0	0	1
1	1	1	0	1	0	1	1

7(c)	**One** mark for each point $Y = \overline{A}\ \overline{B}\ C + \overline{A}\ B\ \overline{C} + A\ \overline{B}\ \overline{C} + A\ B\ C$ Purpose: Sum bit $Z = \overline{A}\ B\ C + A\ \overline{B}\ C + A\ B\ \overline{C} + A\ B\ C$ Purpose: Carry output	**4**

Answer 23

Question	Answer	Marks
7(a)	**One** mark per two correct products **(Max 3)** **(Z =) $A\ \overline{B}\ \overline{C}\ D + A\ \overline{B}\ C\ D + A\ B\ \overline{C}\ \overline{D} + A\ B\ \overline{C}\ D +$** **$A\ B\ C\ \overline{D} + A\ B\ C\ D$**	**3**
7(b)(i)	**One** mark for every two correct rows or columns **(Max 2)**	**2**

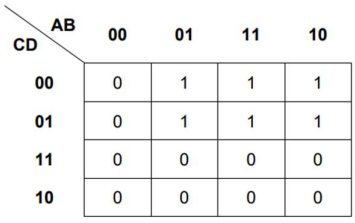
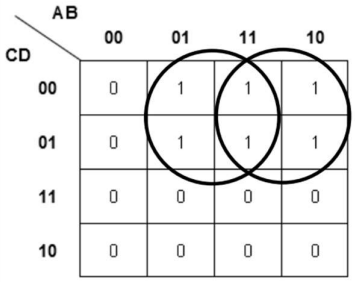
CD \ AB	00	01	11	10
00	0	0	1	0
01	0	0	1	1
11	0	0	1	1
10	0	0	1	0

7(b)(ii)	**One** mark for correct loop **(Max 2)**  	**2**
7(b)(iii)	**One** mark per correct marking point **(Max 2)** • **A B // A D** • **+ A D // + A B** **(Z =) A B + A D // A D + A B**	**2**
7(b)(iv)	**(Z =) A (B + D) // A (D + B)**	**1**

Answer 24

Question	Answer	Marks
6(a)	**1 mark** per correct output column **INPUT** **OUTPUT** **A** **B** **E** **F** 0 0 0 0 0 1 1 0 1 0 1 0 1 1 0 1	**2**
6(b)(i)	Half adder	**1**
6(b)(ii)	Purpose of E: **Sum** Purpose of F: **Carry**	**2**

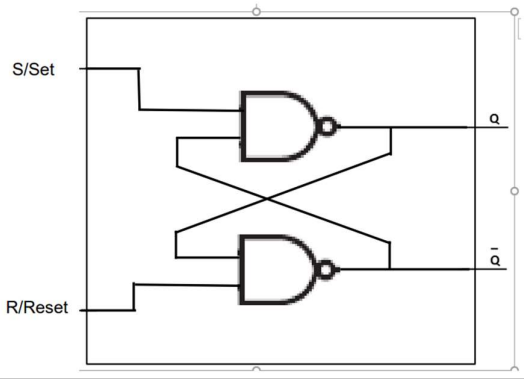
Answer 25

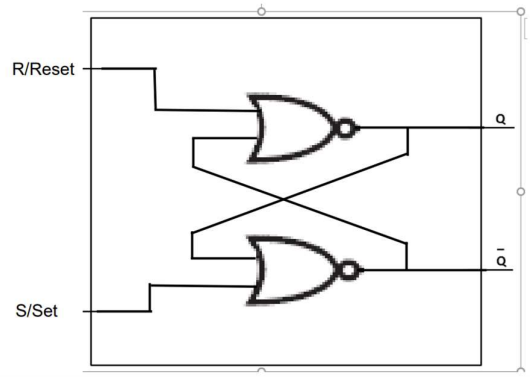
Question	Answer	Marks
7(a)	**Two** marks if no errors present **One** mark if one error present 	2
7(b)	**One** mark for correct loop **(Max 2)** 	2

CD \ AB	00	01	11	10
00	0	1	1	1
01	0	1	1	1
11	0	0	0	0
10	0	0	0	0

Question	Answer	Marks
7(c)	**One** mark for each point • Any correct Boolean term • Boolean terms and operator correct and no other terms present (Z =) $B\overline{C} + A\overline{C}$ **One** mark for simplest form (Z =) $\overline{C}\,(A + B)$	3

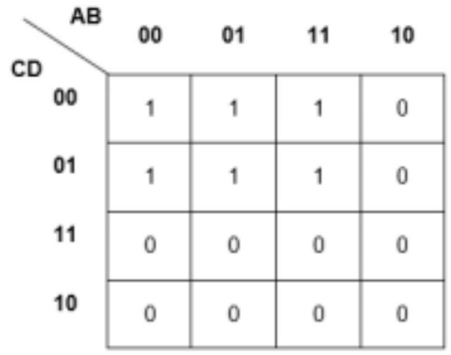
Answer 26

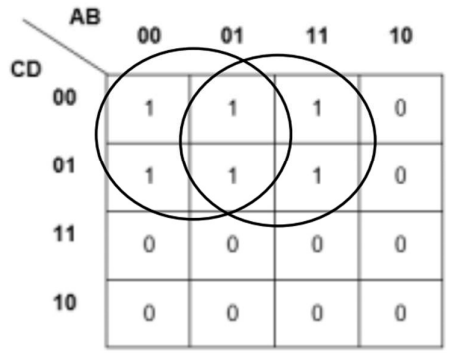
Question	Answer	Marks
8(a)	**One** mark for each point **(Max 4)** • One correct NAND or NOR gate with two separate inputs and one output • Second correct logic gate of same type as first with two separate inputs and one output • Correct connections between logic gates • Correctly labelled inputs Example answers: 	4

Question	Answer	Marks
8(a)	**Or**  	
8(b)	To store a binary digit / (single) bit.	**1**

Question	Answer	Marks
8(c)	**One** mark for each point (**Max 3**) • Correct application of De Morgan's Law • Correct application of Double Negation Law or Distributive Law • Correct answer $\overline{(\overline{A}.\overline{B})}.\overline{(\overline{A}.C)}.\overline{(B.D)}$ $\overline{(\overline{A}.\overline{B})} + \overline{(\overline{A}.C)} + \overline{(B.D)}$ [1] $(\overline{A}.\overline{B}) + (\overline{A}.C) + (B.D)$ [1] $\overline{A}.(\overline{B} + C) + B.D$ [1]	**3**

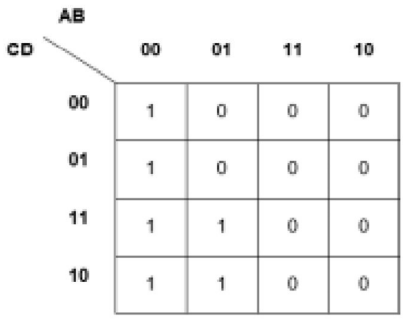
Answer 27

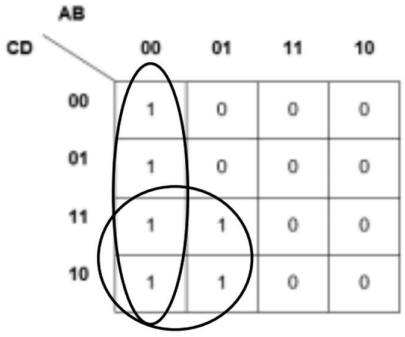
Question	Answer	Marks
7(a)	**Two** marks if no errors present **One** mark if one error present 	**2**

7(b)	**One** mark for each correct loop **(Max 2)** 	**2**

Question	Answer	Marks
7(c)	**One** mark for each mark point (**Max 2**) • Any correct Boolean term • Boolean terms and operator correct and no other terms present (Z =) $\bar{A}\bar{C} + B\bar{C}$	**2**
7(d)	**One** mark for simplest form (**Max 1**) (Z =) $\bar{C}(\bar{A} + B)$	**1**

Answer 28

Question	Answer	Marks
9(a)	**One** mark for every two correct products (**Max 3**) (Z =) $\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{A}BC\bar{D} + \bar{A}BCD$	3
9(b)	**Two** marks if no errors present **One** mark if one error present  	2

Question	Answer	Marks
9(c)	**One** mark for each correct loop **(Max 2)**  	2
9(d)	**One** mark for each mark point (**Max 2**) • Any correct Boolean term • Boolean terms and operator correct and no other terms present (Z =) $\bar{A}\bar{B} + \bar{A}C$	2

9(e)	**One** mark for simplest form (**Max 1**) (Z =) $\bar{A}(\bar{B} + C)$	1

Answer 29

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>6(a)</td><td>One mark for every shaded block of rows for column Z correct (Max 3)

<table>
<tr><th>A</th><th>B</th><th>C</th><th>D</th><th>Z</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
</table>
</td><td>3</td></tr>
<tr><td>6(b)</td><td>One mark for correct working from points (Max 2), for example:
(Y =) $\overline{A}.\overline{B}.\overline{C}.\overline{D} + \overline{A}.\overline{B}.C.\overline{D} + \overline{A}.B.\overline{C}.\overline{D} + \overline{A}.B.C.\overline{D}$
(Y =) $\overline{A}.\overline{D}.(\overline{B}.\overline{C} + \overline{B}.C + B.\overline{C} + B.C)$
(Y =) $\overline{A}.\overline{D}.(\overline{B}.(\overline{C} + C) + B.(\overline{C} + C))$
(Y =) $\overline{A}.\overline{D}.(\overline{B}.(1) + B.(1))$
(Y =) $\overline{A}.\overline{D}.(\overline{B} + B)$
(Y =) $\overline{A}.\overline{D}.(1)$

One mark for correct answer
(Y =) $\overline{A}.\overline{D}$</td><td>3</td></tr>
</table>

Answer 30

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>7(a)</td><td>
<table>
<tr><th>A</th><th>B</th><th>C</th><th>X</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td></tr>
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<tr><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td></tr>
</table>
</td><td>1</td></tr>
<tr><td>7(b)</td><td>$X = \overline{A}.\overline{B}.\overline{C}$</td><td>1</td></tr>
</table>

Question	Answer	Marks
7(c)	**(Max 2)** for correct working from points shown $(T =) X.Y.Z + X.\overline{Y}.Z + \overline{X}$ Distributive law $(T=) X.Z.(Y + \overline{Y}) + \overline{X}$ Complement law $(T=) X.Z.(1) + \overline{X}$ Identity law $(T=) X.Z + \overline{X}$ Redundancy law (to get final answer) **One** mark for correct answer $(T=) \overline{X} + Z$	3

Answer 31

Question	Answer	Marks
6(a)	**One** mark for working, all four columns P, Q, R and S **One** mark for first four rows of column Z **One** mark for second four rows of column Z	3

			Working space				
A	**B**	**C**	**P**	**Q**	**R**	**S**	**Z**
0	0	0	1	0	0	1	1
0	0	1	1	0	0	1	1
0	1	0	0	0	0	0	0
0	1	1	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	1	0	1	0	1
1	1	0	0	0	0	1	1
1	1	1	0	1	0	1	1

6(b)	**Two** marks for all five correct terms and no extras **One** mark for any three correct terms (Z =) $\bar{A}.\bar{B}.\bar{C} + \bar{A}.\bar{B}.C + A.\bar{B}.C + A.B.\bar{C} + A.B.C$	2

Question	Answer	Marks
6(c)(i)	**Two** marks if all correct **One** mark if one error present	2

A \ **BC**	**00**	**01**	**11**	**10**
0	1	1	0	0
1	1	1	1	1

6(c)(ii)	**One** mark for each correct loop **(Max 2)**	2

A \ **BC**	**00**	**01**	**11**	**10**
0	1	1	0	0
1	1	1	1	1

6(c)(iii)	A + $\underline{B}$	1

Answer 32

Question	Answer	Marks
6(a)	**One** mark for working, all five columns P, Q, R, S and T **One** mark for first four rows of column Z **One** mark for second four rows of column Z	3

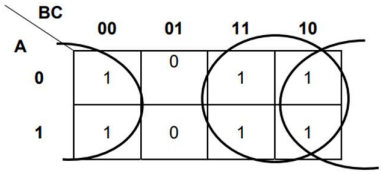
			Working space					
A	**B**	**C**	**P**	**Q**	**R**	**S**	**T**	**Z**
0	0	0	1	1	1	1	1	0
0	0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0	1
0	1	1	1	0	0	1	0	1
1	0	0	0	1	1	0	0	0
1	0	1	0	1	0	1	0	1
1	1	0	0	0	1	1	0	1
1	1	1	0	0	0	1	0	1

6(b)	**Two** marks for all six correct terms only **One** mark for any three correct terms $(Z =) \bar{A}.\bar{B}.C + \bar{A}.B.\bar{C} + \bar{A}.B.C + A.\bar{B}.C + A.B.\bar{C} + A.B.C$	2

Question	Answer	Marks
6(c)(i)	**Two** marks if all correct **One** mark if only one error present	2

A \ BC	00	01	11	10
0	1	0	1	1
1	1	0	1	1

6(c)(ii)	**One** mark for each correct loop **(Max 2)**	2



6(c)(iii)	B + $\underline{C}$	1