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Ghazi AOUSSAJI

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Design and implementation of low complexity digital pre-distortion (DPD) algorithms for multiband and multiple input multiple output (MIMO) wireless transmitters

In front of the jury :

President	: Mr. Faouzi BAHLOUL
Examiner	: Mr. Fethi MEJRI
ENIT supervisor	: Mr. Taoufik AGUILI

Research Laboratory :

SysCom

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List of Abbreviations

ACPR	Adjacent Channel Power Ratio
ADC	Analog-to-Digital Converter
ANN	Artificial Neural Network
CDMA	Code Division Multiple Access
DPD	Digital Predistortion
EVM	Error Vector Magnitude
DAC	Digital-to-Analog Converter
DECT	Digital Enhanced Cordless Telecommunications
DLA	Direct Learning Architecture
DSP	Digital Signal Processing
DUT	Device Under Test
FBMC	filter bank multicarrier
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
GSM	Global System for Mobile communication
GPS	Global Positioning System
IIR	Infinite Impulse-Response
ILA	Indirect Learning Architecture
IM3	Third -order InterModulation
IP	Intellectual Property
LTE	Long Term Evolution
LUT	Look-Up Table
MIMO	Multiple Input Multiple Output
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
TDMA	Time Division Multiple Access
VHDL	Very High Speed Integrated Circuit Hardware Description Language

Abstract

Power Amplifier is the most crucial part of wireless communication systems. Being the most power hungry element and due to its nonlinear characteristic, it will affect the transmission performance and reduce the power efficiency. Different techniques have been developed in order to solve this issue. Digital Predistortion is one of the modern solutions that has proven its performance at linearization of the PA behaviour.
During this work, Digital Predistortion has been simulated in Matlab and true Rf tests has been performed on a real transmission platform. Then DPD algorithm was also designed and implemented in VHDL.

Key Words : Power amplifier, Digital predistortion, OFDM, VHDL, Wireless communication.

Résumé

L'Amplificateur de puissance est la partie la plus cruciale des systèmes de communication sans fil. Étant l'élément qui consomme une grande partie de puissance absorbée et en raison de sa caractéristique non linéaire, il affecte les performances de transmission et réduit l'efficacité énergétique. Différentes techniques ont été développées pour résoudre ce problème. La predistortion numérique est l'une des solutions modernes qui a prouvé sa performance à la linéarisation du comportement de PA. Au cours de ce travail, la predistortion numérique a été simulée dans Matlab et des vrais testes ont été réalisés sur une véritable plateforme de transmission sans fil. Ensuite, l'algorithme DPD a également été conçu et décrit en VHDL.

Mots clés : Amplificateur de puissance, predistortion numérique , OFDM, VHDL, Telécomunication.

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General Introduction

Nowadays, in wireless communications systems, many different types of data are transmitted such as speech, emails, pictures, videos... As the demand of people is increasing for wireless applications, more and more data need to be transmitted through wireless networks.
However, the spectrum resources are limited so they must be used wisely. Advanced wireless communication techniques such as Wide Code Division Multiple Access (WCDMA) and Orthogonal Frequency Division Multiplexing (OFDM) have been developed in order to improve the spectral efficiency and allow more users to send more data with higher speed rates. he involved signals and modulation techniques are characterized by wide bandwidth and non-constant envelopes leading to a high Peak to Average Power Ratio (PAPR).Unfortunately, The signals characterized by high PAPR are very sensitive to the nonlinear characteristic of transmitter components such as Power amplifier.

The power amplifier is the key component in modern wireless transmitter. For a power amplifier, high power efficiency is a basic requirement because of the energy consumption issue. At the same time, high linearity is more and more required today, to minimize the frequency interference and allow higher transmission capacity in wideband communication systems. The more linear the transmitters, the more user channels can be fitted into the available spectrum resources. Particularly with the trend of mobile phone technology moving towards multi-band and wide-band systems, where different wireless communication standards such as global positioning system (GPS), global system for mobile communications (GSM), universal mobile telecommunications system (UMTS), Long Term Evolution (LTE),Bluetooth and wireless local area network (WLAN) are to be integrated altogether. Power amplifiers with both excellent linearity and high power efficiency are increasingly essential in the transmitters. However, it is well known that high linearity will reduce the power efficiency in power amplifiers. The best solution for this problem is using linearization techniques which consists of process the signal before transmit it to the power amplifier. As a result, linearization techniques allows power amplifiers to have both high power efficiency and high linearity.

This project is about Digital PreDistortion(DPD) design and implementation, one of the advanced techniques of power amplifier linearization. Next chapter will introduce some background of this topic. Second chapter is about DPD simulation and tests on real PA. Finally, last chapter is dedicated to VHDL implementation of the DPD algorithm.

Chapter 1

Background

This chapter is an overview of the problematic of this project, its goal and a brief presentation of the host company. An introduction to the basic knowledge of wireless telecommunication systems and transceivers is given. Section 4 introduces Power amplifier main characteristics are introduced and explained briefly.

1.1 Problematic overview

The power amplifier(PA) is a very important part in a wireless communication system. In fact, it allows the user to enhance the communication range to reach far distances(some kilometers). Unfortunately, most of power amplifiers have nonlinear properties, which become dominant in their saturation zone. On the other hand, the maximum power efficiency occurs closely their saturation zone. Ideal function of a PA is simple:

$$f(x) = a \times x \tag{1.1}$$

where a > 1, as shown in blue striped line in figure 1.1.

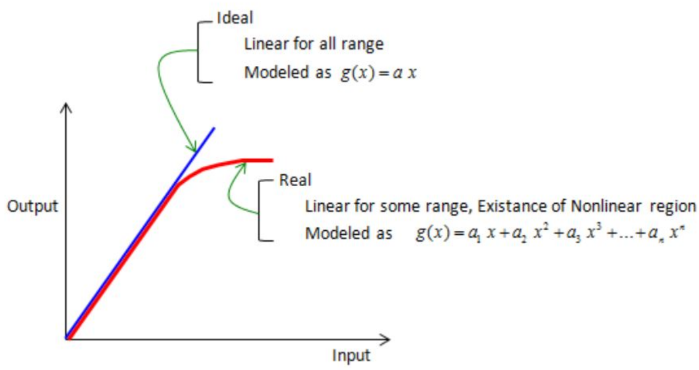

Figure 1.1: Ideal vs real power amplifier characteristic

However, nothing goes like theory. In reality, the characteristics of an amplifier goes as shown in red. In this curve, in some section you would see a straight line which is very close to ideal operation, but from some point the behavior deviates from the ideal operation.

Mathematically this non-ideal (non-linear) curve can be represented in a polynomial function. In the same time, PA is one of the major sources of power dissipation in wireless base stations. The digital predistortion(DPD) techniques makes the PA operating in a more efficient power level resulting in more energy efficient wireless networks. To address the ever increasing demand for higher data rates, the MIMO and the carrier aggregation techniques are being adopted by the current and upcoming wireless standards. The requirement for concurrent transmission over multiple bands in carrier aggregation schemes and over multiple antennas in MIMO schemes poses a great challenge to the design of feasible DPD algorithms. The multiband/MIMO DPD algorithms currently available in the literature are computationally too complex to be implemented in practice.

1.2 The aim of this work

This work aims at the design and implementation of low complexity digital predistortion (DPD) algorithms for multiband and multiple input multiple output (MIMO) wireless transmitters. The following are the work steps that should be achieved:

* Numerical simulations on Codintek's Matlab Tx and Rx OFDM transceiver chains.

* On over-the-air Codintek's MIMO SDR platform that takes into account true RF analog front-end, while still using Matlab algorithms

* Realized designs will have to be coded in VHDL, integrated to Codintek's Intellectual Property (IP) Core and tested in real-time modem operation.

1.3 Company overview : CODINTEK

This work was made in collaboration with CODINTEK company. CODINTEK is a Tunisian company providing innovative RF broadband product design services and solutions for dense communication networks. The company helps clients to deliver leading edge designs from concept to production. CODINTEK offers a family of synthesizable flexible DSP IP cores, each delivering a different balance of performance and power dissipation. In addition, the company team have the specialized skills and experience at designing wireless IOT solutions for the connected world. The company provides kits ,tools and all-in-one modules for designing smart products, for smart homes, smart cities and industry.

Figure 1.2: Codintek's logo

1.4 Wireless telecommunications systems

Wireless communications is a type of data transmission that is performed and delivered without wire connection. This term incorporates procedures of connecting and communicating between two or more devices using a wireless signal through various wireless communication technologies and devices.
The communication between two devices occurs when the destination or receiving intermediate device captures these signals, creating a wireless communication link between the sender and receiver.
Wireless communication generally works through electromagnetic signals that are broadcast by a device within the air, physical atmosphere or environment. The sending device can be a sender or an intermediate device with the ability to propagate wireless signals in order to enhance the transmission range.

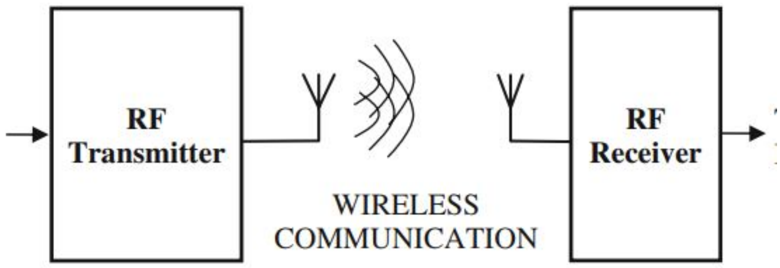

Figure 1.3: Basic view of an RF communication system

1.4.1 Transceiver

A transceiver (TRX) is a device which can transmit and receive signals. Usually, a transceiver contains both a transmitter and a receiver. However, if the transmitter and receiver only share a common housing and nothing else, the device is called a transmitter-receiver. Transceivers are extremely important in the history of technology, as they have paved the way for many inventions such as two-way radios, mobile phones and the internet.

There are two main types of radio transceivers: full duplex and half duplex.
Half-duplex transceiver can transmit data only in one direction, when a radio transceiver is transmitting the message, the receiver portion is disabled. As both the parts share the same components, including the same antenna, the parts cannot transmit and receive signals at the same time. Thus, receiving and transmitting can not be done simultaneously, even though sometimes both operations may take place at the same frequency. An example of use of such a system is two-way radios, also known as walkie-talkies, which use push to talk functions.

In full-duplex transceivers, the transceiver can receive signals during transmissions. However, in such transceivers, the transmitter and receiver work at completely different frequencies. This disallows any kind of signal interference to occur. Many modern devices, including mobile phones and devices using satellite communication, use this technology.

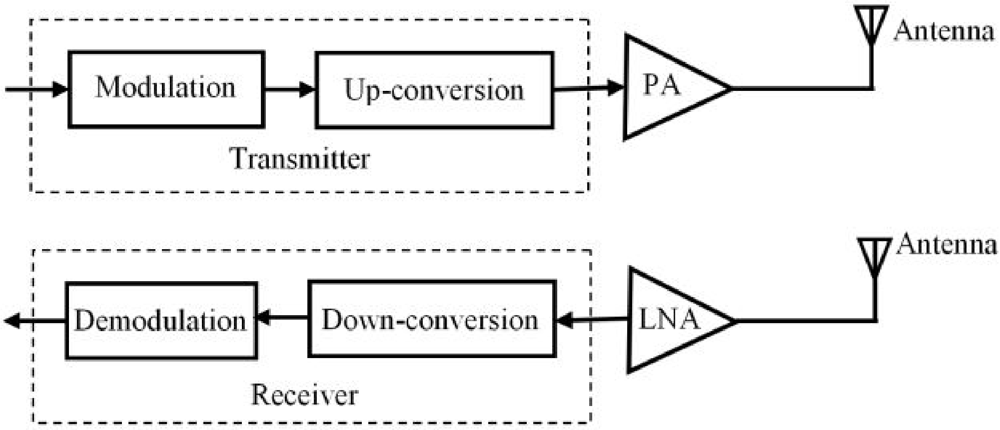

Figure 1.4: Transceiver

Modern digital communications transceivers are generally composed of a Medium Access Control (MAC) layer managing the access to the medium between different users in a network and the quality of service seen by each, and a PHY (Physical Layer) which is responsible for the transfer of information across the medium (wireless channel, cable, optical fiber, etc.). The PHY can be decomposed into two blocks:

* The digital baseband (DBB) which is located between the MAC and the analog front-end (AFE). The baseband transmission path encodes the bits provided by the MAC, generates the data symbols to be sent across the medium, and finally performs the digital modulation. The reception path demodulates the data and provides a decoded bit stream to the MAC. Generally, the transmission requirements are well specified by the standards (channel coding, modulation, etc.), whereas the algorithms used in reception (channel estimation/equalization, synchronization, etc.) can vary from one implementation to another.

* The RF AFE is connected to the DBB. The RF transmit path converts the DBB signal to analog and frequency up-converts to RF. The receiver frequency down-converts the RF signal to baseband, filters out any interferers, and finally converts the signal to DBB.

1.4.2 Different modulation techniques

They represent techniques adopted by communication standards such as time-division multiple-access (TDMA) and code-division multiple-access (CDMA) are competing technologies for OFDM. Another competing technique, filter bank multicarrier (FBMC), has evolved with the advances in OFDM systems. For 3G systems, the cellular industry has generally adopted CDMA, despite the evolution of TDMA. However, both techniques are well suited for narrow-band systems and can provide roughly the same degree of spectral efficiency, while using the same processing blocks (turbo codes, higher-order modulation, adaptive modulation and coding, etc...) [Praveen kumar Singya, 2017].

Modulation techniques adopted by various wireless standards		
GSM	General Packet Radio service (GPRS), Enhanced Data for Global Evolution (EDGE)	First digital cellular scheme. Great success in GSM. Enhancement being designed for GSM/EDGE.
CDMA	CDMA2000 1x Evolution (1xEV), 1x Evolution data only (1xEV-DO), 1x Evolution data and voice (1xEV-DV), Wide-band CDMA (WCDMA), High-Speed Packet Access, IEEE 802.11b	Commonly adopted by various 3G networks. Efficient modulation technique; widely preferred by various wireless systems.
OFDM	IEEE 802.11a/g/n/ac, digital video broadcasting (DVB), WiMAX (IEEE 802.16), IEEE 802.22, 3GPP-LTE, LTE-Advanced.	Efficient solution for broadcast systems, broadband radio systems, and high peak data rates in large blocks of spectrum. Flexible spectrum usage. Basis for most of the 4G systems (LTE and WiMAX) and WLAN. One of the possible solutions for the next-generation wireless communication standards (5G)
FBMC	Telecommunication Industry Association digital radio technical standard, cognitive radio	Preferred in cognitive radio. Considered a dominant contender for 5G. Based on FBMC; four alternative waveforms identified by 5GNOW.

Table 1.1: Modulation techniques adopted by various wireless standards

1.4.3 Orthogonal Frequency Division Multiplexing

OFDM stands for Orthogonal Frequency Division Multiplexing. It is a variation of FDM technique in which sub-carriers are closely spaced to have an efficient utilization of the provided bandwidth. OFDM sub-carriers carry different data in parallel simultaneously to achieve higher data rate. [wirless world, 2012]
OFDM transmitter uses complex modulation techniques to increase the data carrying capacity. For example, 16-QAM modulation maps 4 bits to a complex symbol. This complex symbol is carried by only one subcarrier of an OFDM symbol. In OFDM transmission, multiple sub-carriers are transmitted with each carrying different data symbols to increase the data rate. The figure 1.6 below represents the basics of the OFDM transmission chain.

OFDM modulation is a bit complex technique. But, it allows an efficient use of frequency spectrum and resistance to frequency selective fading.

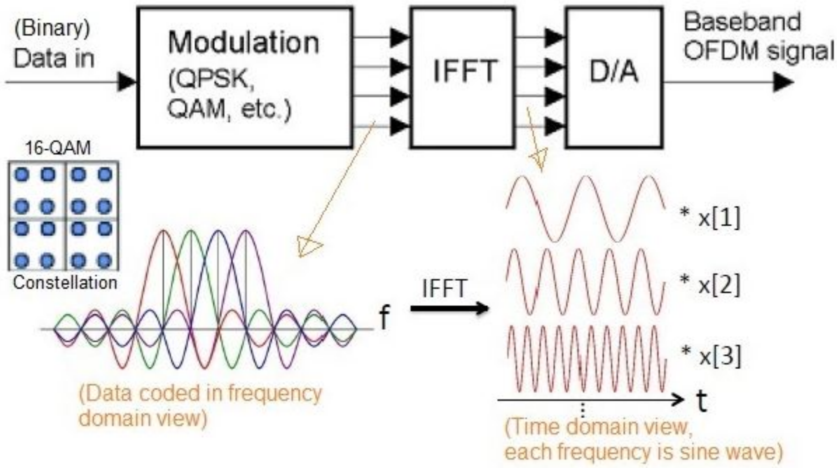

Figure 1.5: OFDM scheme

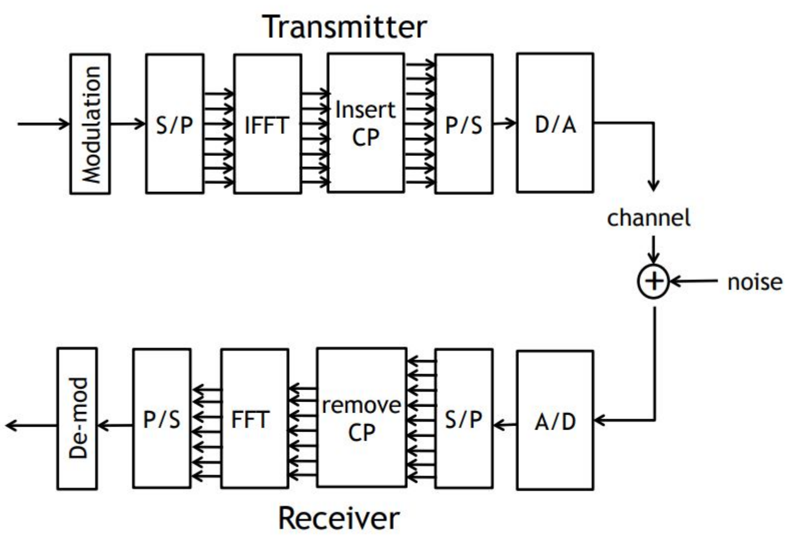

Figure 1.6: ODFM basics

1.5 Power Amplifier

An amplifier receives a signal from an input source and provides a scaled version of the signal to an output device such as an antenna or to another amplifier stage. The main factors are usually linearity, gain, and efficiency. Being the most power hungry element in the transmission systems, Power amplifier efficiency is the most crucial matter to be resolved. There has been considerable industrial interest in producing Radio Frequency (RF) PAs with good linearity and power efficiency. These two contradictory requirements can be composed by using external circuitry to linearize an efficient amplifier. Ideally, linearity is the ability of an amplifier to maintain equal gain for any input signal. But, this is not true in practice, especially for higher input power levels. PAs must be linear to minimize interference and spectral regrowth. However, PAs have an inherent nonlinear behavior and are considered the main reason of distortions in RF transmitters [FG, 2016].

1.5.1 Gain

The power gain of a PA is the ratio of output to input power, and is usually measured in decibels. The power gain of a PA in dB (decibel) is given by:

$$G(db) = 10log\left(\frac{Pout}{Pin}\right) \tag{1.2}$$

Pin is the input power and Pout is the output power.

1.5.2 Bandwidth

The bandwidth(BW) of an amplifier is the range of frequencies for which the amplifier delivers acceptable performance. A well-accepted metric for acceptable performance is the half power points (i.e., frequencies where the power is half of its peak value) on the output. Hence, the BW can be defined as the difference between the lower and upper half power points of the gain transfer function of the system as illustrated in the figure 1.7 below. This BW is also called the 3-dB BW.

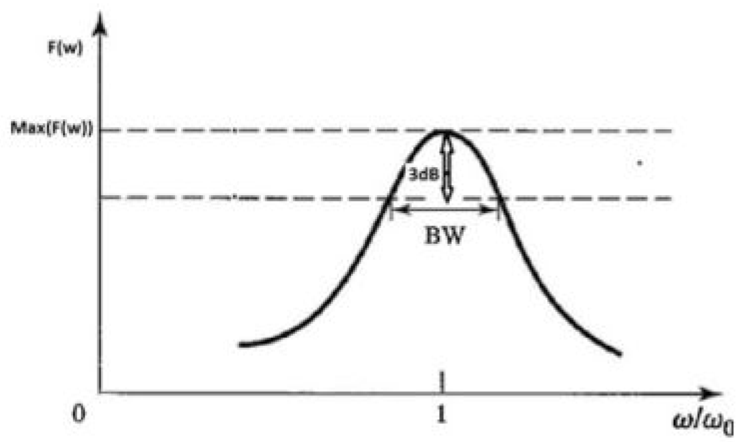

Figure 1.7: 3 dB bandwidth illustration of the frequency dispersive system

1.5.3 Noise Figure

The noise factor (F) is a metric that gives an indication of noise added by the circuit. The noise factor is defined as the input signal-to-noise ratio (SNRin) divided by the output SNR (SNRout), which is given by

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{1.3}$$

1.5.4 Power Efficiency

Power efficiency of PA is most concerned by researchers in modern wireless communication system. It is because that it directly affects the power efficiency of whole transmitter. Commonly, the power efficiency of PA can be estimated by Power Added Efficiency (PAE). PAE, which involves PA input signal power, is expressed as

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \eta \left(1 - \frac{1}{g}\right) \tag{1.4}$$

where Pin and Pout denote the input and output powers of PA, respectively, PDC denotes supplied DC (Direct Current) power, and $g = \frac{P_{out}}{P_{in}}$ is linear gain.

1.5.5 P1dB

The 1 dB compression point (P1dB) is a measure of amplitude linearity. The gain of an amplifier goes down when its output reaches saturation. The P1dB point is the input power that causes the gain to decrease 1 dB from the normal expected linear gain plot. It is the point where the amplifier goes into compression and becomes nonlinear. Similarly, the saturation power, $P_{sat[dB]}$, corresponds to the maximum power that the PA can deliver and often corresponds to 3-5 dB gain compression from the small-signal gain. Operation above this point should not occur to avoid signal clipping and strong distortions. Figure 1.8 below illustrates the P1dB, maximum saturation and 3 dB saturation points for a typical PA.

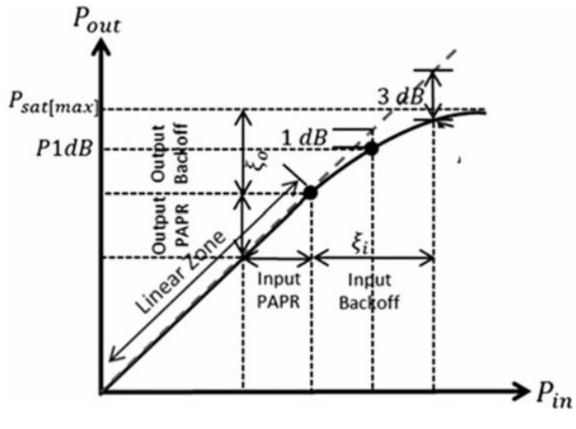

Figure 1.8: Typical $P_{in}P_{out}$ characteristic of a PA

1.5.6 Third-Order Intercept Point

Similar to Psat and P1dB, there are other device parameters that specify the nonlinearity of the PA. In general, the nth-order intercept point, IIPn, is the intersection between the extended linear gain of the PA and the linearly extended gain of the nth-order intermodulation distortions. This can be seen in the figure 1.9 below.

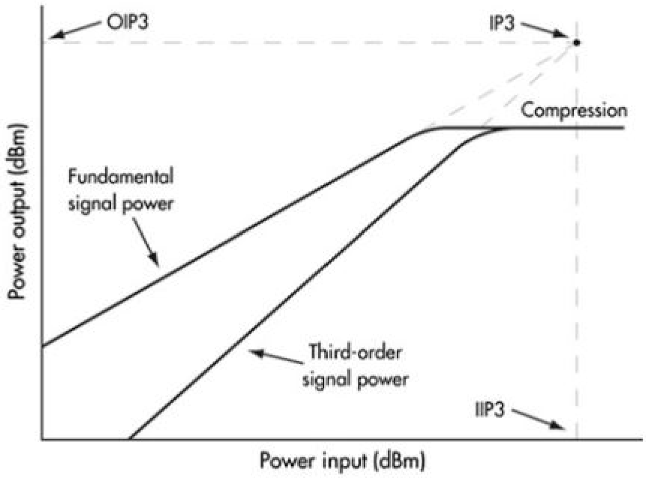

Figure 1.9: Third order intercept piont

1.5.7 PAPR

Peak-to-average power ratio (PAPR) is the ratio between the peak power P_{peak} (related to peak amplitude) and the average power P_{avg} (related to mean amplitude) of a modulated signal, x(t). It is also called crest factor and is given by

$$PAPR(dB) = 10log\left(\frac{max(|x(t)|^2)}{mean(|x(t)|^2)}\right) = 10log\left(\frac{P_{peak}}{P_{avg}}\right) \tag{1.5}$$

1.6 Conclusion

This chapter was a brief introduction for the background needed to start working on the current subject. Before starting working on such project some basic terms and concepts must be defined. Next chapter will be about digital predistortion.

Chapter 2

Digital predistortion

There is a various techniques for power amplifiers linearisation, digital predistortion is a modern technique that allows the reduce of nonlinearity while still working on the baseband processing. There is also other techniques performed on the analog front-end which are out of the scoop of this work.

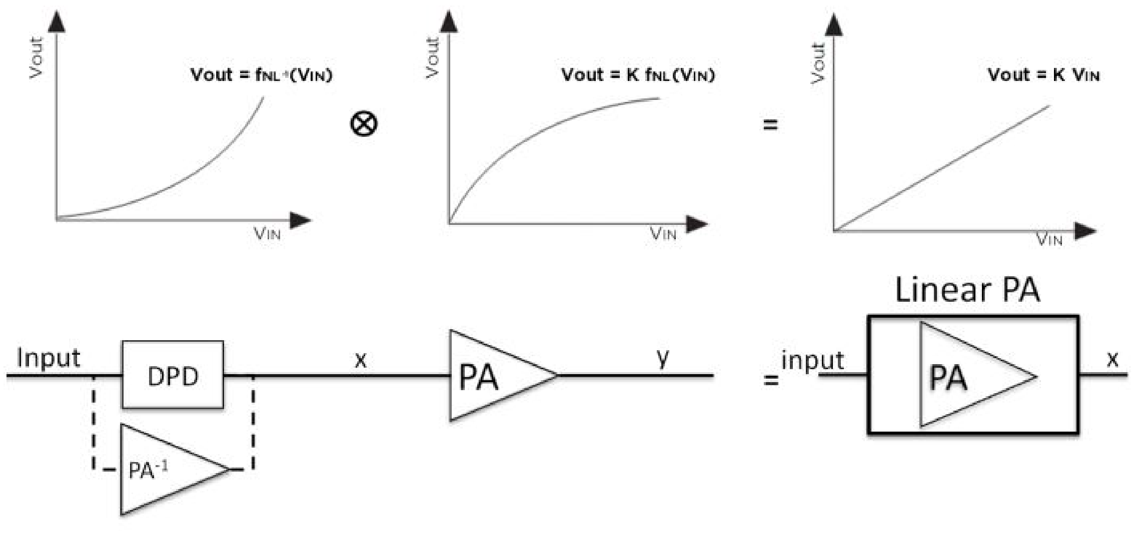

Figure 2.1: Digital predistortion principe

The DPD is based on introducing a nonlinear function in the baseband part of the transmitter. This Function generates additional distortion that are out of phase to those introduced by the PA. The DPD corrects the power and phase level of a primary input signal in order to get a linear amplification. The cascaded system DPD+PA linearity relies on the DPD ability to produce complementary nonlinearities in magnitude and phase to the PA ones. Hence, Digital predistortion success requires proper choice of the predistortion function and accurate PA behavior modeling.

2.1 Digital predistortion overview

Digital Predistortion Algorithm can be classified into two main categories:

- Static DPD is the simple architecture where the predistortion bloc is estimated offline(in lab tests). Once estimated,the DPD engine and can not be changed.

- Adaptive DPD includes an additional part that estimates the DPD bloc instantaneously and adapts it to the current situation. For sure, this type will give more performance then the static DPD.

While it is easy to implement on hardware, static DPD is less efficient for multivariable dynamic systems.On the other hand adaptive DPD is more precise and efficient in PA model extracting but when still more complex to implement.

2.2 Popular DPD

A lot of DPD techniques have been proposed in the literature and research papers. The most used implementation methods are classified into three main categories: Look-Up Table (LUT) based DPDs, Neural network(NN) based DPDs and model based DPDs (called also polynomial based DPDs).

2.2.1 LUT based DPD

LUT based DPD is a basic method for implementing DPD technique. It is a simple and efficient technique. The values of desired predistorted signals are stored in the memory units as a table. The table is indexed by the amplitude of the input signal, then the predistorted signal is extracted.
The core of LUT based DPD is the table used to generate the predistorted signal. The important task is to properly construct a LUT which represents the inverse function of the PA.

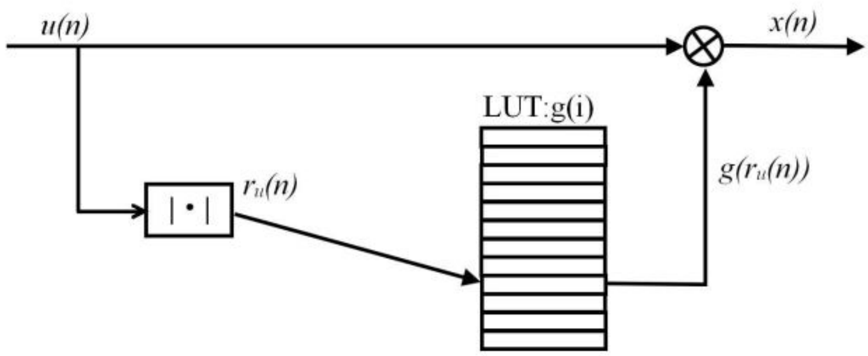

Figure 2.2: Structure of complex-gain LUT-based predistorter

2.2.2 Neural network based DPD

Artificial Neural Network (ANN) has an excellent capability to accurately approximate nonlinear functions.It has been proven that a feed forward ANN with a single hidden layer and nonconstant, bounded and monotone-increasing continuous activation functions, can approximate any nonlinear function with any desired error [HUSH et HORNE, 1993]. Hence, ANN can be used to model a PA and its predistorter.
The model of a single neuron mathematical expression is given by :

$$y = F(\omega x + b) \tag{2.1}$$

Where x and y are the input and output of the neuron, respectively, w is the weight value, b is the bias value, and F is the activation function. Figure 2.3 shows a generic structure of a recurrent neural network. Because neural network has a strong ability of learning

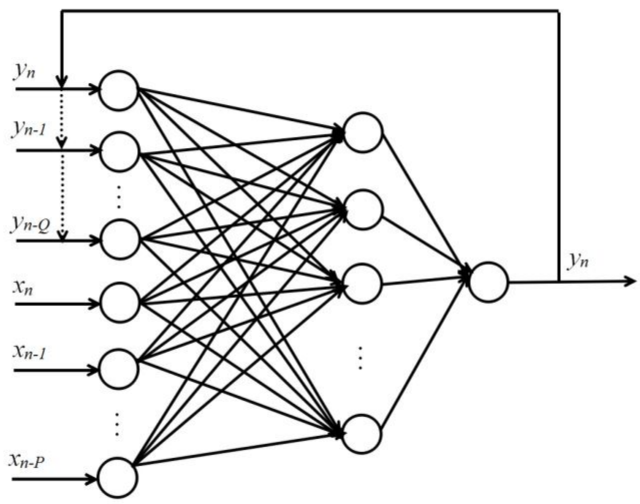

Figure 2.3: Structure of a recurrent neural network

and imitation, the neural network based DPDs can obtain good linearization performance. However, the training of the neural network is complex and time-consuming. The hardware implementation of the neural network is not easy in practical applications.Hence, It will not be considered as a solution for our problematic.

2.2.3 Model based DPD

Model based DPDs also called polynomial based DPDs, are mostly used for the linearization of PA.Similarly, the predistorter is also a nonlinear system. For memoryless system, the polynomial model can be used to model the predistorter. Both PA and DPD are modeled by a polynomial function. For memoryless system, the polynomial model is function of current sample only . For memory system, polynomial model is a function of the current sample and N previous samples (N here is called memory depth).

2.2.3.1 Two tones test

Two tones test is a simple theoretical modeling that helps to represent the effect of PA nonlinearity on the frequency spectrum. Say that the PA is modeled as:

$$Y(t) = a1 \times x(t) + a2 \times x^2(t) + a3 \times x^3(t) + a4 \times x^4(t) + a5 \times x^5(t) \tag{2.2}$$

Considering the following signal composed of tow tones :

$$x(t) = A \times cos(\omega_1 t) + A \times cos(\omega_2 t) \tag{2.3}$$

Substituting 2.6 in 2.5 gives :

$$\begin{aligned} Y(t) = a1 &\times [A \times cos(\omega_1 t) + A \times cos(\omega_2 t)] \\ &+ a2 \times [A \times cos(\omega_1 t) + A \times cos(\omega_2 t)]^2 \\ &+ a3 \times [A \times cos(\omega_1 t) + A \times cos(\omega_2 t)]^3 \\ &+ a4 \times [A \times cos(\omega_1 t) + A \times cos(\omega_2 t)]^4 \\ &+ a5 \times [A \times cos(\omega_1 t) + A \times cos(\omega_2 t)]^5 \end{aligned} \tag{2.4}$$

The resulting harmonic and intermodulation products are listed in the table of Appendix A

the even-order products cause less concern than the odd-order products, since they are out of band and can be filtered out easily. The two-tone test output spectrum close to the carriers is shown in the next figure 2.4.

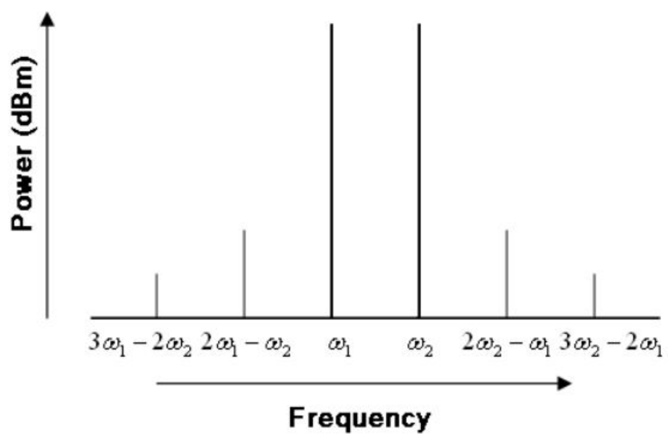

Figure 2.4: Two tone test output spectrum

Hence, one can conclude that even order products are not very important in Pa modeling since their effect is less important compared to the odd order products. This is an interesting result that well help making Digital predistortion algorithm less complex and more easy to implement on hardware platforms.

2.2.3.2 Memory effect

Power Amplifiers exhibit memory effects. It means that Pa output depends not only on current input signal but also history of the input and output signal. There are two different types of memory effects:

- Short term memory effects that takes place on a time scale close to the carrier frequency. It is generally due to the presence of the reactive components presence in the network(capacitors, inductors).

- Long term memory effect which takes place on a time scale close or smaller than the signal bandwidth. This effect is caused by thermal effect, charge trapping effects and DC self biasing [Mkadem, 2014].

2.3 Conclusion

This chapter presented the DPD process and some of its popular varieties and how they work. In the next chapter we will talk about the Simulations and tests that has been performed.

Chapter 3

Simulation and Tests

After identifying the problematic and main topic terms, we start digging deeper into the non linearity effects and how to compensate it using DPD algorithm. This chapter is about the problematic modeling on Matlab and test results on the true RF platform.

3.1 Matlab modeling

As a first step, the predistortion algorithm should be modeled and tested. Furthermore, applying DPD on OFDM signal requires some additional operations such as digital up converting and filtering. All this and lots more can be done perfectly on Matlab®

Figure 3.1: Matlab

Matlab is a computing environment and proprietary programming and modeling language developed by MathWorks company. MATLAB allows the manipulation of matrix , plotting of functions, implementation of sophisticated algorithms and interfacing with other programs written in other programming languages such as C, C++ and Python.

3.1.1 Interpolating

Applying DPD requires a higher frequency resolution (comparing to the transmission chain without DPD). In other word, sampling rate must be higher. For example, in order to apply a third order DPD, frequency resolution must be three times at least the original one. This is a direct consequence of Shannon Sampling Theorem :

> If a continuous time signal contains no frequency components higher than W hz, then it can be completely determined by uniform samples taken at a rate fs samples per second where $fs \geq 2W$

To fulfill this condition we need to use digital to analogue converter(DAC) in transmitter part and analogue to digital converter (ADC) with high sampling rate. For example, applying a third order DPD on OFDM signal with 20Mhz bandwidth will require converters with 120Msps. Converters with such sampling rates are quiet expansive. Fortunately, one of the often used process in DSP can solve this issue.Interpolation means adding some additional samples to the original signal in order to increase the sampling rate without modifying or destructing it or adding other information.On of the easiest techniques is 'Zero padding', which consists of inserting zeros between samples.

3.1.1.1 Interpolating with a factor of 2

Before interpolating, we have a simple OFDM signal. the next figure 3.2 shows the PSD of the original signal:

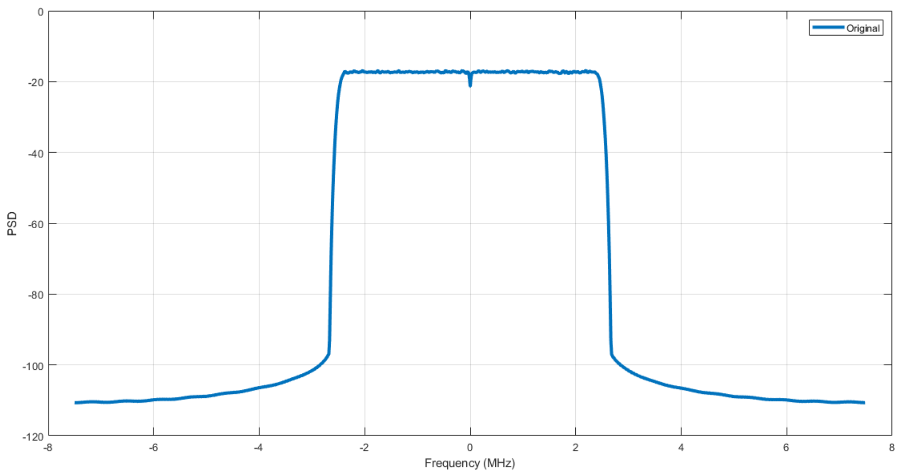

Figure 3.2: Original signal before interpolation

Zero padding this signal in time domain by a factor of 2 will give us the next PSD shown in the following figure 3.3: Time domain zero padding is a simple way to improve frequency resolution[Lindsten, 2010] but it introduces periodic replications of the original spectra. The original signal has more frequency resolution but one half of the original spectra was added on the left and an other half on the right of the original. These added parts should be filtered.

3.1.1.2 Interpolating with a factor of 3

Similarly to the previous subsection, but with an interpolating factor of there, the original signal was upsampled in time domain.
The PSD of the upsampled signal shows the central original spectra with two other replications on the left and right sides.
Hence, we can conclude that upsampling enhances the frequency resolution but it adds replications on the adjacent bands. Those replications must be filtered. Since we still working in base band digital processing, filtering must be also digital.

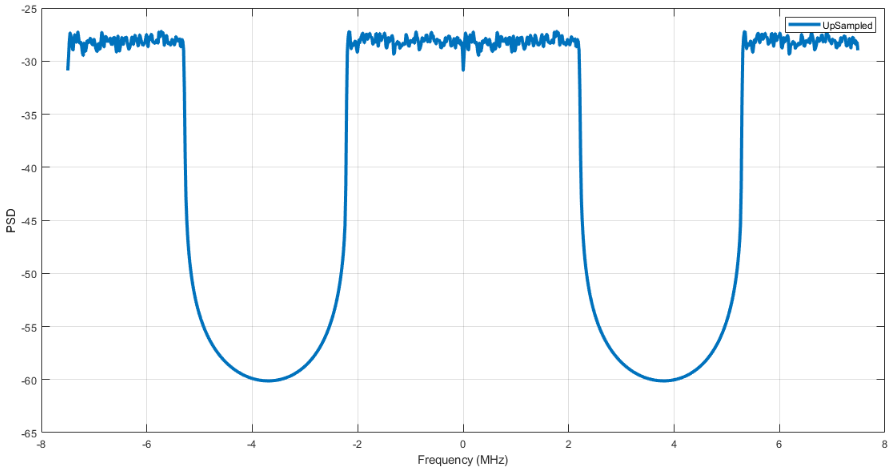

Figure 3.3: PSD of upsampled signal by a factor of 2

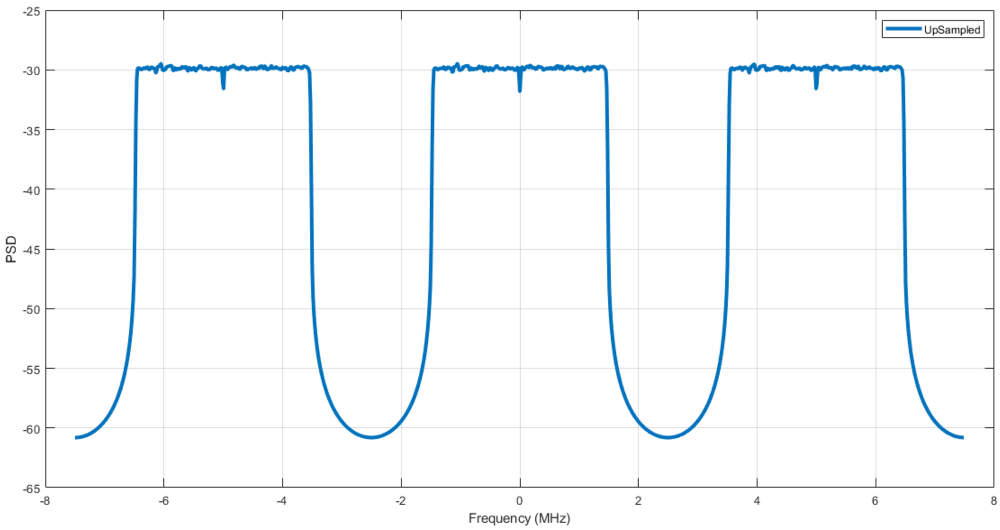

Figure 3.4: Periodic replications due to interpolation

3.1.2 Filtering

The next step of interpolation is filtering in order to eliminate the replications. In digital signal processing, filtering is a very important process. In fact, there are two types of digital filters, Finite Impulse Response filters (FIR) and Infinite Impulse Response filters(IIR). In our case, we choose FIR filters because of its linear phase property which implies that the phase is a linear function of frequency. It ensures that signals of all frequencies are delayed by the same amount of time, hence, eliminating the possibility of phase distortion.

Fir filter can be mathematically expressed as follow:

$$y(n) = \sum_{0}^{M-1} b_k x(n-k) \tag{3.1}$$

Designing a FIR filter can be done easily with Matlab's filter designer with a customized number of coefficients. This feature can provides also the magnitude and phase response of the designed filter and can generate its Matlab script and coefficients. Passing the up sampled (interpolated) signal, with an upsampling rate of 3, through the designed filter with 64 taps gives the results shown in figure **??**.

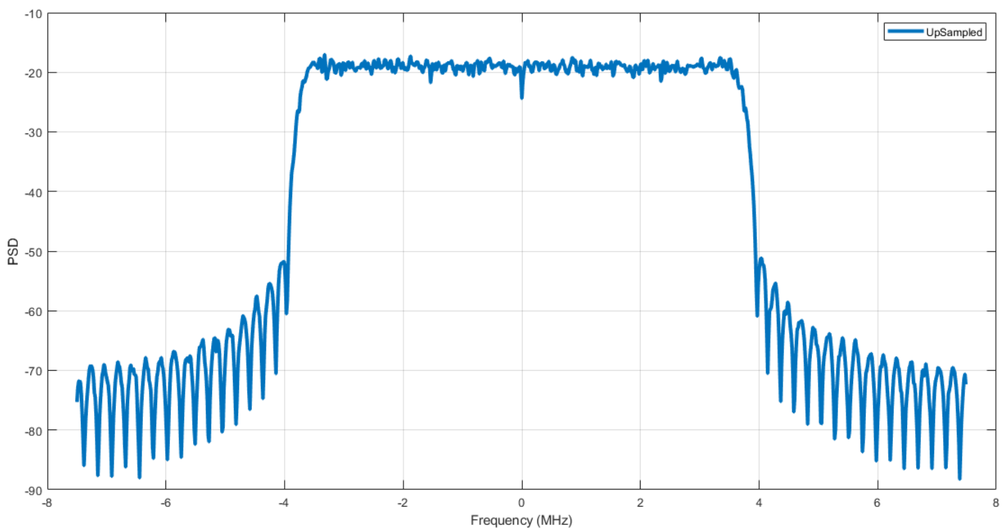

Figure 3.5: PSD of 64 taps FIR filter output

This is the output of a symmetric FIR filter with 64 coefficients. To get better filtering performance we need a big number of coefficients but note that this will make its hardware implementation more complex.

Next figure 3.6 shows the PSD of a 128 taps FIR filter :

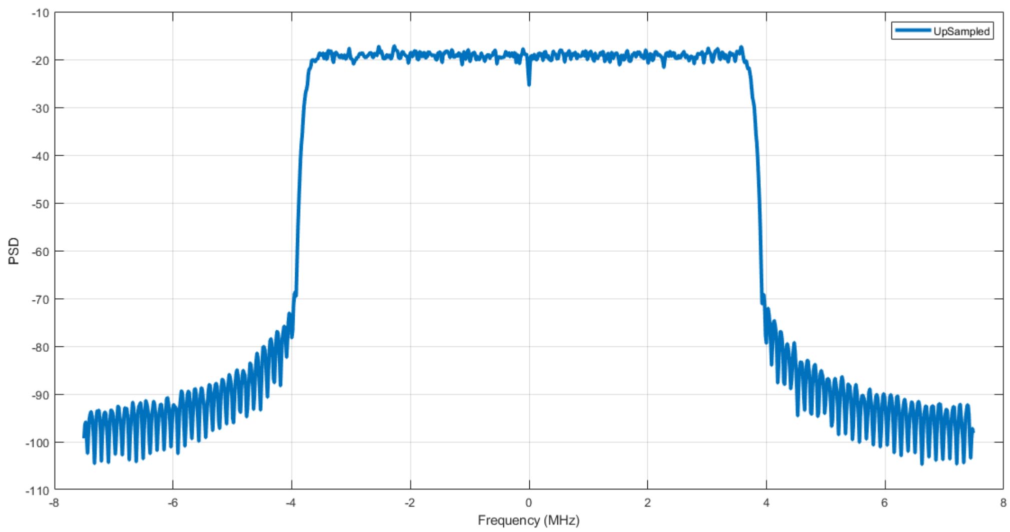

Figure 3.6: PSD of a 128 taps FIR filter output

We can observe that the replications are more attenuated compared to the previous filter. The next figure 3.7 shows the magnitude response (blue) and phase response (red) of the designed filter.

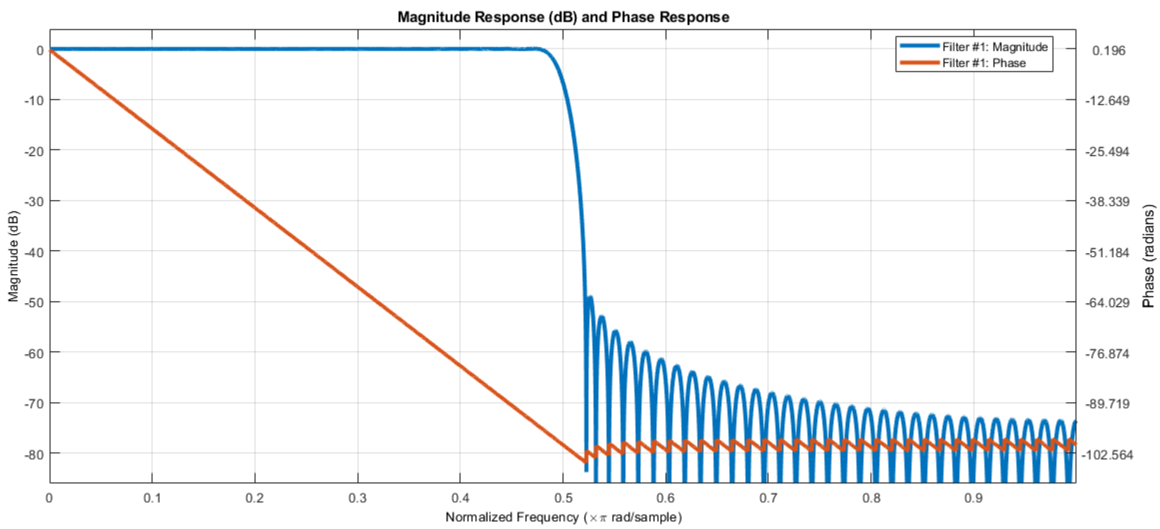

Figure 3.7: Magnitude and Pahse response of 128 taps filter

In hardware implementation ,usually number of taps is limited to 32 which can be reduced to 16 in our case thanks to symmetric FIR filter (this will be more explained in the next chapter) .

3.1.3 Power amplifier effects

After generating the OFDM signal, interpolation and filtering, the power amplifier must modeled in order to test its effects. In fact, there is a lot of models types for the PA in the literature. We will consider the polynomial only because of its simplicity. Modeling a PA with a polynomial equation will be done on Matlab by creating a matrix of coefficients. In real implementation of DPD, PA coefficients must be determined by real tests. Several combinations of coefficients and memory depth was tested and compared for memory and memoryless PA models.

3.1.3.1 Memoryless PA model

first, we will test a memoryless PA model, with odd order terms only, that can be expressed as:

$$y(n) = \sum_{i=1}^{k} c_k x(n) \|x(n)\|^{2i} \tag{3.2}$$

Generating an OFDM signal and pass it through the PA model gives the next results shown in figure 3.8:

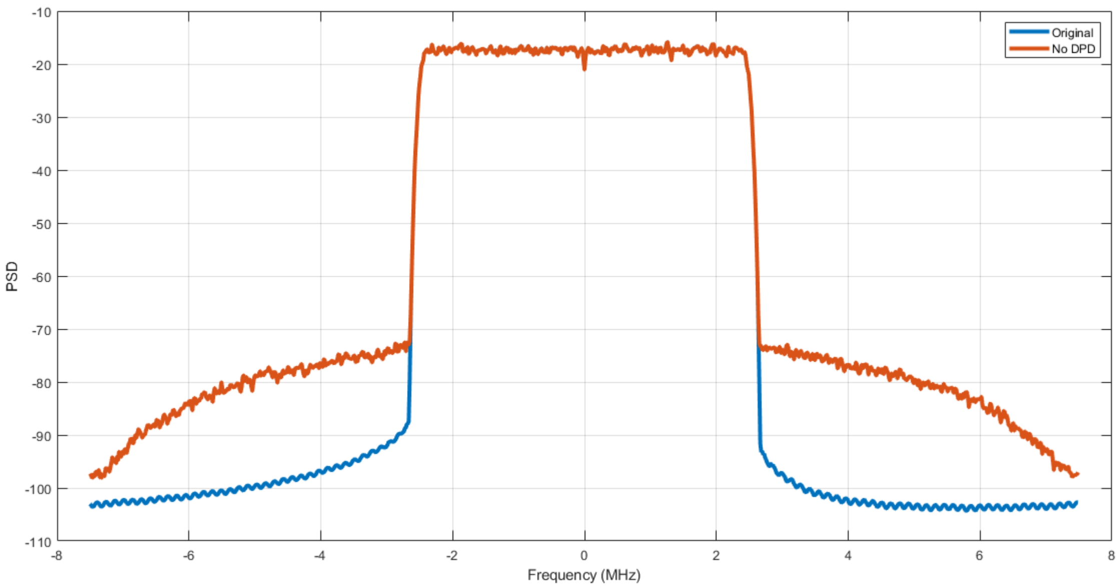

Figure 3.8: Memoryless PA model output

The figure 3.8 illustrates the power spectrum density of the original signal(in blue) and the PA output signal(in red).This model of PA have four complex coefficients which means it considers up to the seventh order term(only odd). One can observe that the PA non-linearity caused the spectral regrowth of the output signal. Second observation is that this spectral regrowth is symmetric on the right and left adjacent bands. Eventually, this out of band distortion will affect the transmission performance and cause issues when we talk about Spectral mask.

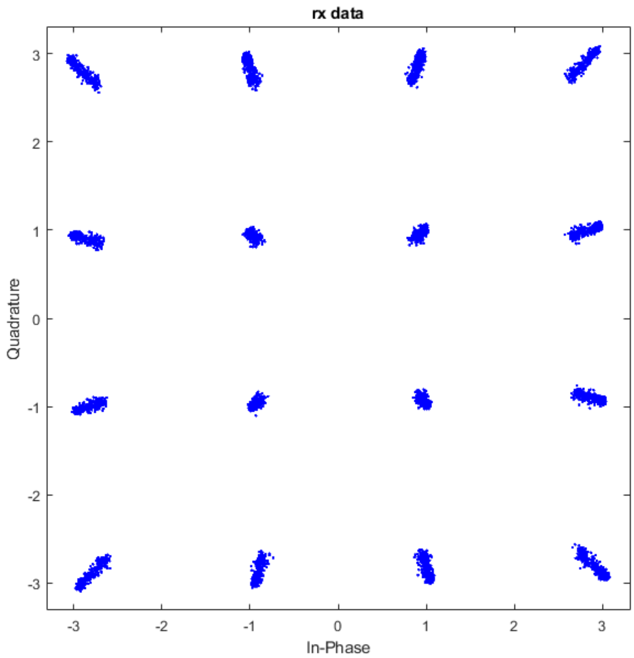

Figure 3.9: Scatterplot of the TX and RX signal

This figure 3.9 shows the effect of the PA nonlinearity on the constellation diagram which can be measured by the Error Vector Magnitude(EVM) indicator.
This is the constallation of a 16QAM modulated signal. It shows that the symbols tend to migrate to the center of diagram.

3.1.3.2 Memory PA model

Considering now the memory effect in the model of the PA. Mathematical equation describing the PA model will be as follows:

$$y(n) = \sum_{j=0}^{m} \sum_{i=1}^{k} c_{k,j} x(n-j) \|x(n-j)\|^{2i} \tag{3.3}$$

Now, keeping the seventh order and considering a memory depth of three, we pass the same OFDM signal through the new PA model.
Memory effect add spectrum asymmetry in frequency domain and the dispersion of constellation in time domain [Feng, 2015].
The figure 3.10 above shows the PSD of the original siganl and the output of the memory PA model. We can observe that more distortion is added to PA impairments due to memory effect.
The scatterplot confirms the previous deduction. More distortion is added to the constellation diagram and the symbols are dispersed in circular forms.

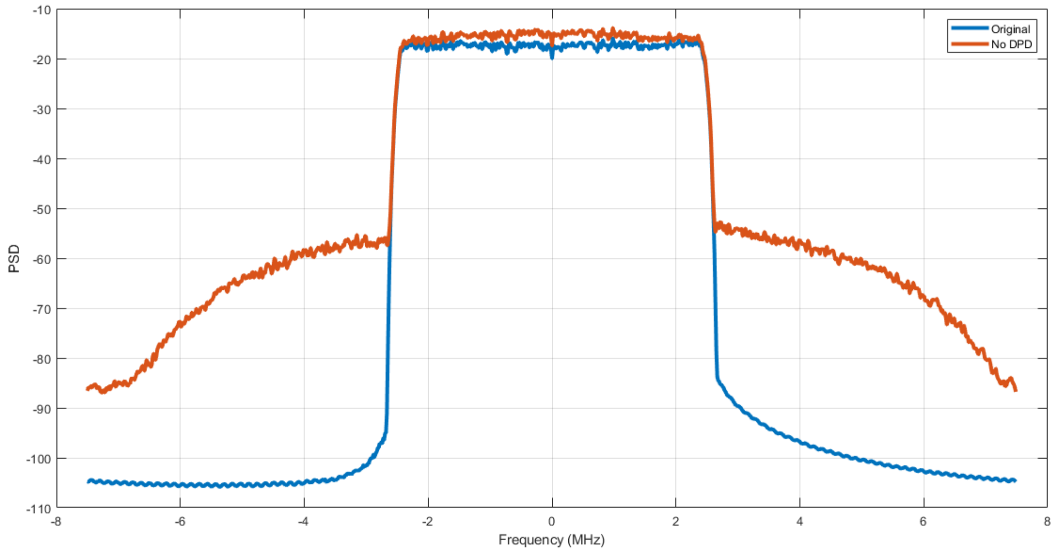

Figure 3.10: Memory PA output

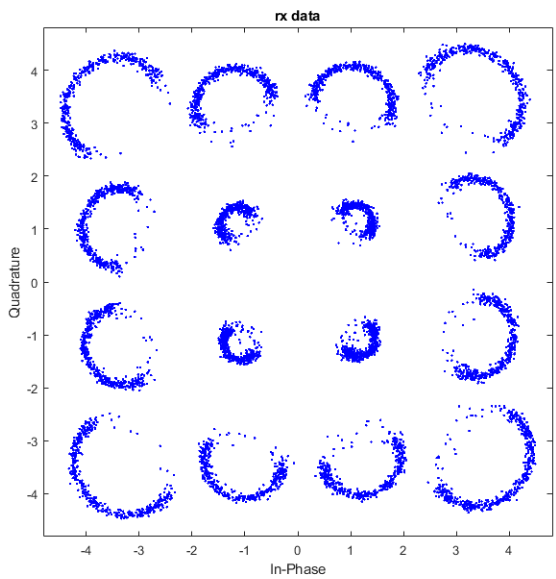

Figure 3.11: Scatterplot of the TX an RX signal

3.1.4 Digital predistortion

After identifying the RF impairments caused by the PA nonlinearity, we should now simulate the DPD and test its efficiency. As discussed in the previous chapter, DPD is used in the PA linearization. There are two methods for DPD coefficients extraction : direct and indirect learning architectures.

3.1.4.1 Direct learning architecture

The block diagram of DLA is illustrated in figure 3.12:

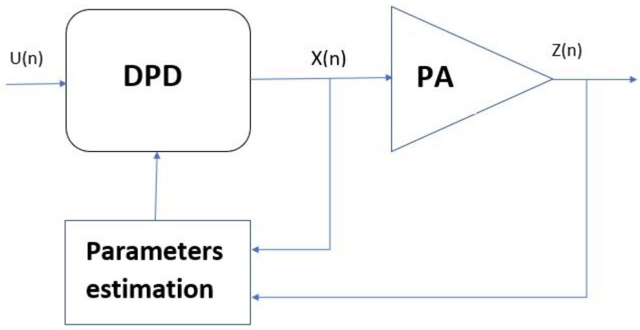

Figure 3.12: DLA bloc diagram

In DLA, the determination of the PD needs two steps. First, the model of PA's behavior needs to be predefined. The coefficients cpq are extracted by LS method which is explained in Appendix B. Secondly, the identified model of the PA is reversed for the determination of the DPD.

3.1.4.2 Indirect learning architecture

This architecture consists of calculating the desired output signal from the input one, then estimating the predisposed input signal that gives the desired one. Identifying the DPD coefficient can be done by passing the distorted input and the desired output signals through the Least Mean Squares(LMS) algorithm. Both methods was tested but ILA

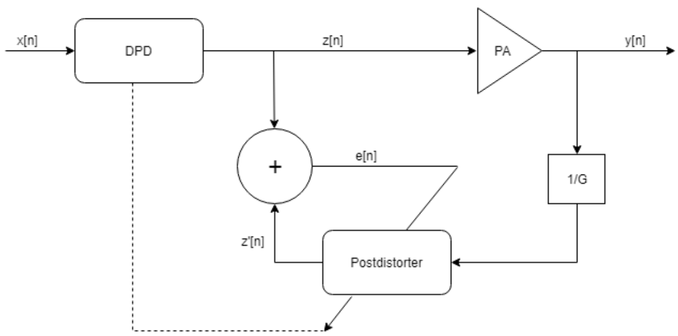

Figure 3.13: Indirect learning architecture

showed more interesting result's. In fact, it allows a great accuracy and more flexibility.

3.1.4.3 DPD effect

To see the memory effects on DPD and PA model. We test the four possible model combination cited below.

Memoryless PA model and memoryless DPD model We well start by simulating the memoryless PA and DPD models. Considering the nonlinearty order of 7 for both and working on the same input OFDM signal.

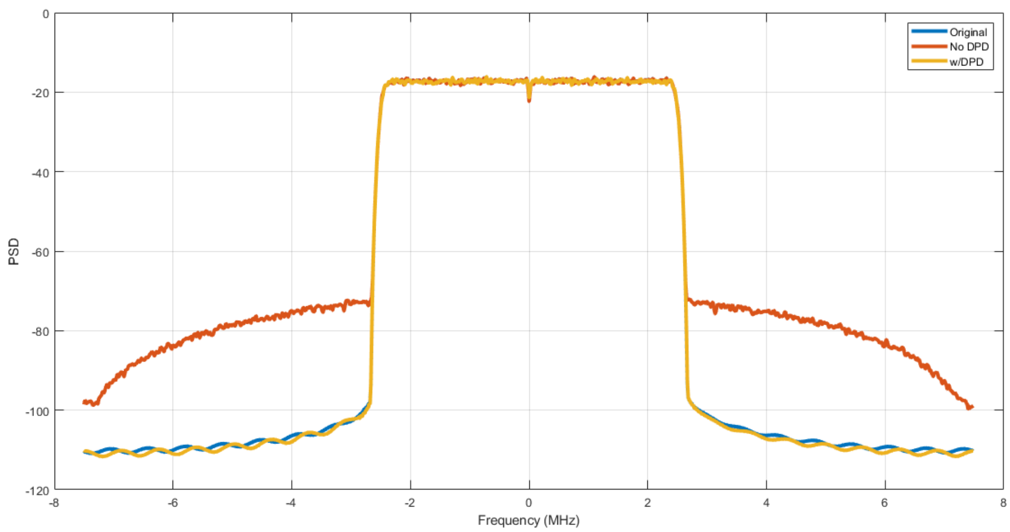

Figure 3.14: Memoryless PA and DPD simulation result

Memoryless PA model and memory DPD model Now keeping the same PA model and using a memory DPD model. The output results are shown in the figure 3.15.
In this situation, DPD memory model has no additional better effect. In fact, we can observe that there is some non symmetry added to the PA output of the predistorted signal. Hence, one can conclude that using a memory model for a PA with low memory effect has no real importance.

Memory PA model and momeoryless DPD model We consider now a memory model of the PA, with 4 as memory depth, and start with a memoryless DPD model. The results are shown in the figure 3.16.
The output of the PA with DPD and without DPD are almost equal. There was no enhancements in term of spectral regrowth. In other words, using a memoryless DPD model in order to linearize a PA with remarkable memory effect has no sens.

Memory PA model and memory DPD model finally, we test memory model for both PA and DPD. The result is shown in figure 3.17.
Obviously, the memory DPD model has an important effect in linearizing the PA behavior. Hence, one can conclude that DPD is certainly able to improve the power

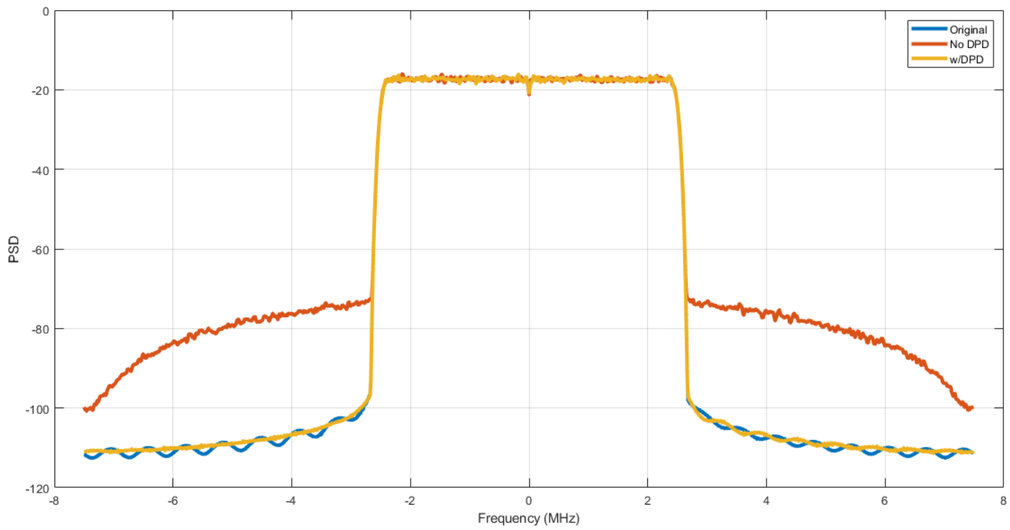

Figure 3.15: Memoryless PA and memory DPD result

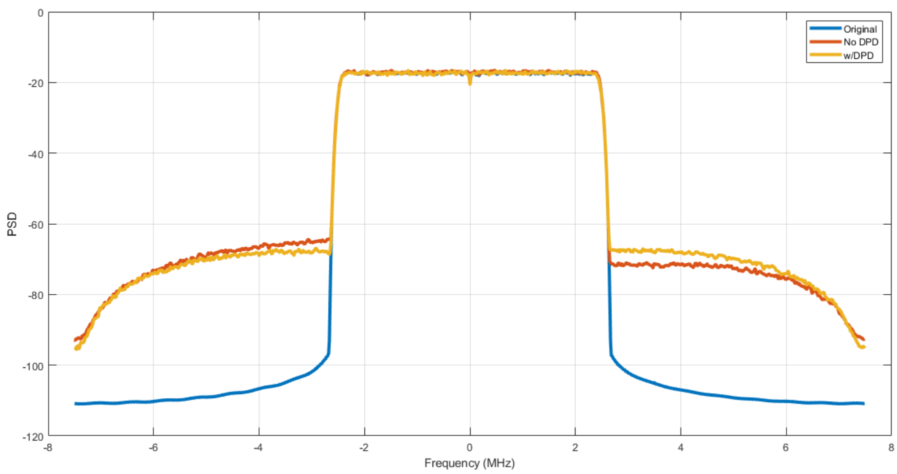

Figure 3.16: Memory PA and memoryless DPD results

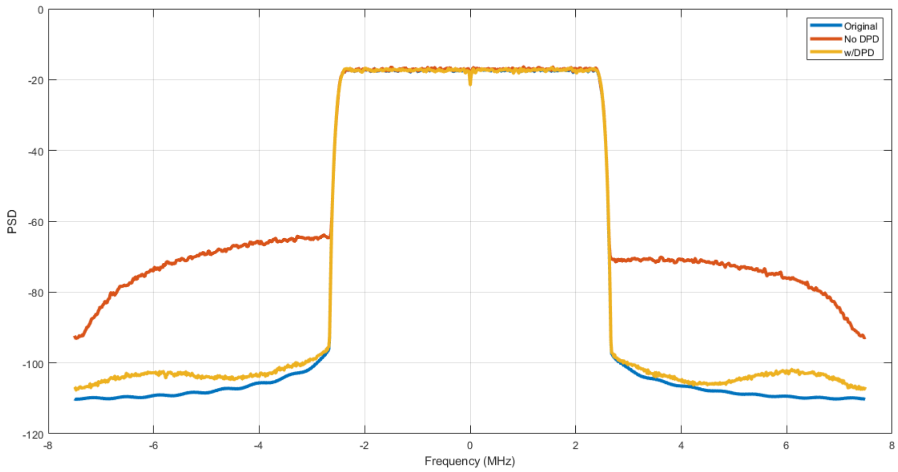

Figure 3.17: Memory PA and DPD model results

amplifying process performance. For a low memory effect PA, a memoryless DPD will be enough to linearize its behavior. On the other hand, PAs with a remarkable Memory effect must be anticipated by a memory DPD model.

3.1.5 Conclusion

In this section, Interpolation process has been presented and its effect of increasing the frequency resolution has been highlighted. Fir filter was also explained and filters with different number of taps was tested. In section 3.1.3 PA different models has been introduces and radio frequency impairments was presented. In the next section, PA+DPD cascaded system was highlighted with memory and memoryless combinations and its performance was discussed. PA with high memory effect need to be used with DPD engine with memory model. On the other hand, adding a memory model DPD to a Pa with low memory effect will add no enhancement.
Once having simulated the PA and the DPD, true tests must be performed in order to confirm the previous results. Next section will be about the real tests that have been made.

3.2 Tests on CODINTEK's platform

Simulation results must be confirmed with tests on a real platform. In this section, The platform MRP-A200 and the power amplifier that we used in the tests will be presented. Then tests results will be discussed.

3.2.1 MRP-A200 PLATFORM

The MRP-A200 is designed to modulate, transmit and receive data over wireless medium. The modulation uses 20MHz bandwidth is carried over 5GHz unlicensed band.

Figure 3.18: MRP-A200 platform

This platform main Features are:

- ARM Cortex-M3 Processor with embedded flash FPGA
- High rate Full duplex RF transceiver operates at 5 GHz unlicensed band
- Single 12V Power supply
- RJ45 for 10/100Mbits Ethernet
- Programmable clock generator
- On-board high-efficiency DC-DC converters

The platform can be connected to the PC through the Ethernet port. It can be configured and controlled with Matlab. After, configuration, OFDM signal can be sent to the platform and stored into a memory embedded stack. Since the platform have two transceivers, One of them can be configured as a transmitter and the other as a receiver.

3.2.2 SKYWORKS power amplifier

The SKY85724-11 is a highly integrated, 5 GHz front-end module (FEM) incorporating a 5 GHz single-pole, a 5 GHz low-noise amplifier (LNA) with bypass, and a 5 GHz power amplifier (PA) intended for mobile/portable 802.11ac applications and systems [Solutions, 2016].
In order to protect the transceivers from high power signal, the transmitter signal must be attenuated with some special attenuators.

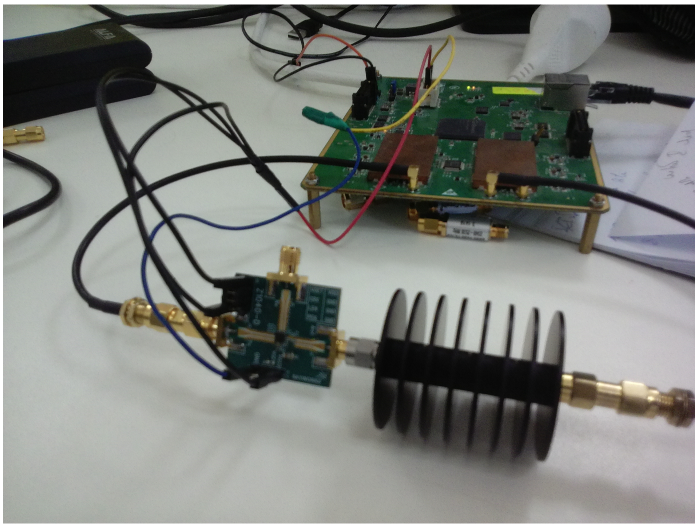

Figure 3.19: Power amplifier with attenuator

Figure 3.20: RF attenuator

3.2.3 Work environment

The testing process starts from my laptop where the signal is generated,interpolated, and sent to the MRP platform. Once stored into the ram of the platform, then these steps are followed :

1. The output of the transmitter is connected to the input of the receiver. Once triggered, the the stored signal is sent from the transmitter to the receiver and stored into its ram. The stored signal will be treated on Matlab in order to estimate the PA Model.

2. The output of the transmitter is connected to a spectrum analyzer in order to visualize the spectra of the PA output. This scenario is used once the PA model is extracted and the signal is predistoretd with the estimited DPD.

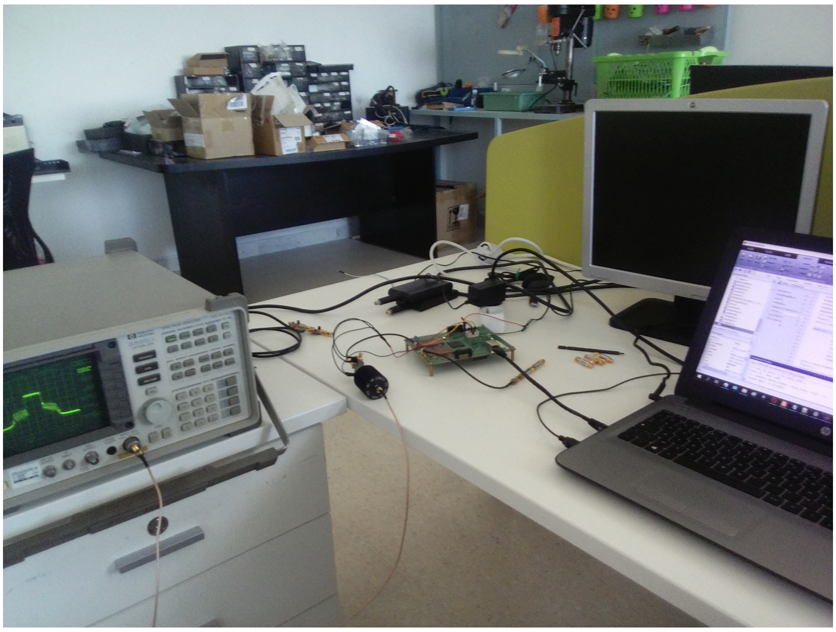

Figure 3.21: Work environment

3.2.4 Experimental results

In a first step, OFDM signal was passed through the PA and received frame was used in order to estimate the PA coefficients. Then the signal was predistorted and retransmitted. I used a spectrum analyzer in order to visualize the output spectrum of the PA output with/without predistotion. The following figure 3.22 is a picture of the spectrum analyzer showing the spectra of the PA output with/ without predistortion.
The figure 3.22 shows that the predistorted signal comes out with lower spectral regrowth. In this case, DPD effect is not very obvious because non linear zone of this power amplifier is already small so there was not too much to be linearized.

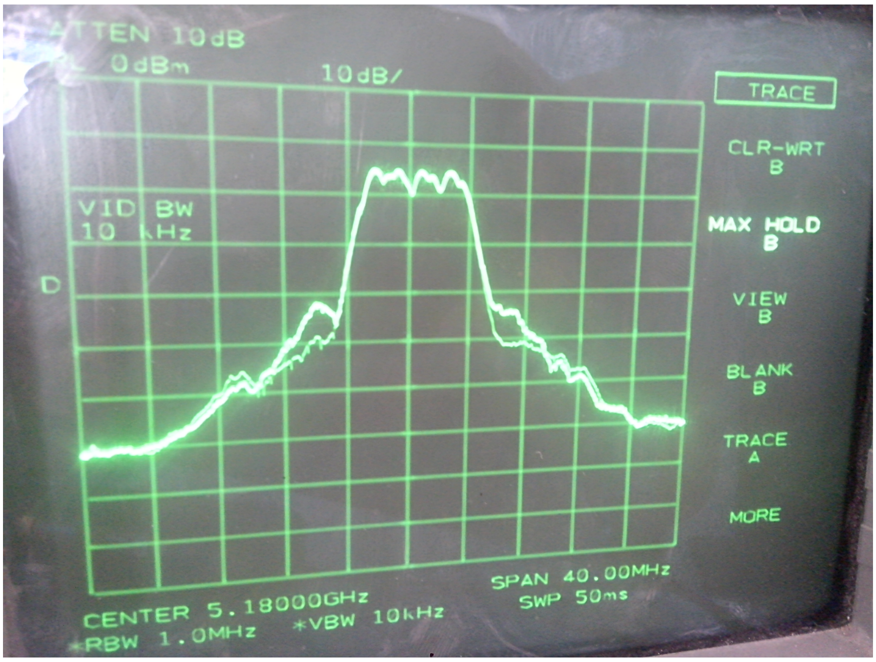

Figure 3.22: PA output with/without DPD

3.2.5 conclusion

This chapter presented DPD simulation and tests on true power amplifier results. First, PA coefficients was estimated then DPD model was extracted. OFDM signal was predistorted and passed through the PA. Output results was visualized on a spectrum analyzer and DPD effects was discussed. Hence, DPD algorithm has shown its performance on real RF tests.

Next chapter will be about implementation of tested algorithm in VHDL.

Chapter 4

Digital front end implementation

Digital front end is the top level of the zero padding, filtering and DPD bloc combined together. Zero padding with filtering forms the Digital Up Converter(DUC).
In this chapter, VHDL implementation of Digital front end will be presented. The main architecture will be highlighted. Then the internal blocs will be explained.

4.1 Digital front end architecture

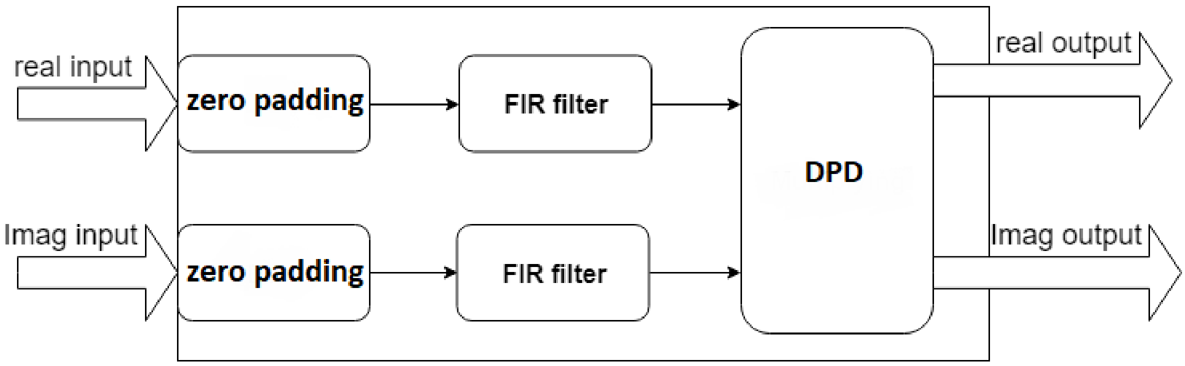

Figure 4.1: Digital front end main architecture

Since the input signal is composed of real part and imaginary part, two parallel internal digital up converters(interpolation blocs) are needed. DPD can't be separated since real output is function of both real and imaginary input, and so does the imaginary output.

4.2 Designing steps

When designing the Digital front end, some steps must be followed in order to make this process easier and more efficient. First, the bloc must be written and verified on QuestaSim. Then the output signal of the designed bloc is saved in a txt file. On the other hand, Matlab will generate the equivalent signal, read the txt file and compare both results. If the results are equal then design is valid ,else, it must be reviewed.

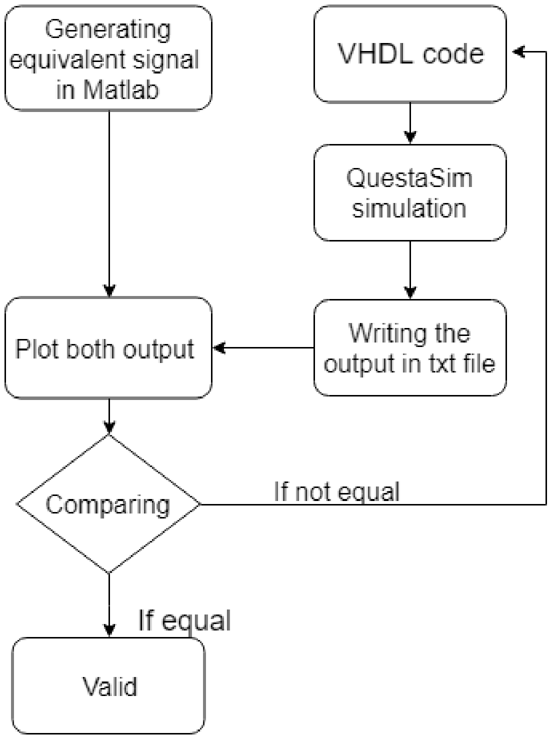

Figure 4.2: Designing steps

4.3 Zero padding

Digital up converter has a simple principe : adding zeros between samples. Zero padding is widely used in digital signal processing in several domains. This technique will increase the number samples and hence, the frequency resolution. Yet, its implementation is not as simple as it appears. The major complexity in its design is avoiding lost of data. The Digital Up Converter (DUC) is sensitive to two clock domain which means that a First In First Out (FIFO) memory bloc is needed. Interpolating is to pop one sample from the FIFO on a one reading clock rising edge and zeros for n(order on interpolation) other clock rising edges. The sensitivity to more then one clock domain is huge dilemma in hardware designing.

4.4 Asynchronous FIFO pointers

This issue was solved by adding an extra bit to the reading and writing pointers. If the Most Significant Bits (MSBs) of the two pointers are different, it means that the write pointer has wrapped one more time that the read pointer. If the MSBs of the two pointers are the same, it means that both pointers have wrapped the same number of times.

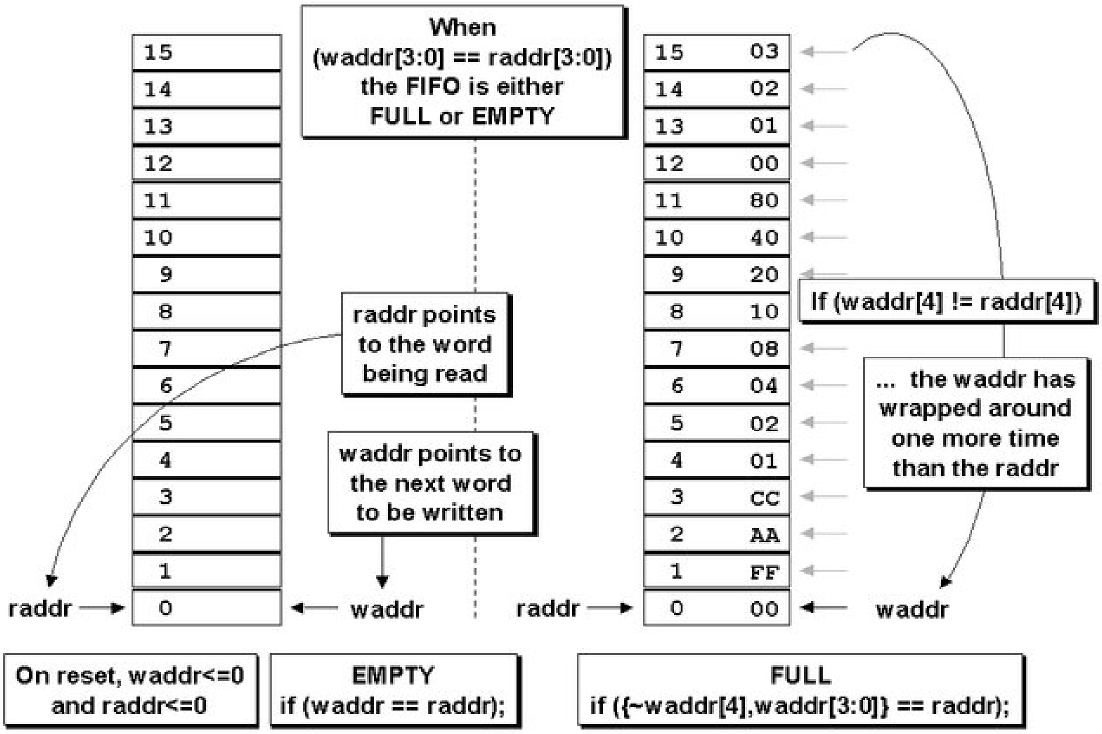

Figure 4.3: FIFO full and empty conditions [Cummings, 2002]

4.5 FIR filter

The finite impulse response filter is used in many digital signal processing systems to perform signal preconditioning, band selection, low-pass, decimation/interpolation, filtering, and video convolution functions.

4.5.1 Conventional FIR Application

Filtering in digital signal processing is a convolution product. Figure 4.4 below shows a conventional 8-tap FIR filter architecture. This filter has eight registers(8 bit data width)

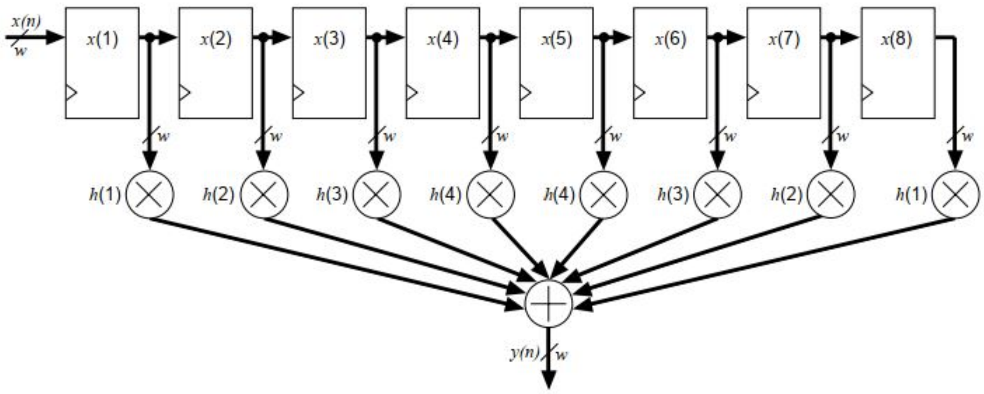

Figure 4.4: Conventional FIR Application

arranged in a configuration of a shift register. This is the easiest way to implement a FIR filter on a hardware platform. Yet, one can see that 8 taps only will cost 8 multiplying blocs.

4.5.2 Optimized FIR filter

For a linear phase response FIR filter, the coefficients are symmetric around the center values. This symmetry allows the symmetric taps to be added together before multiplying them by the coefficients. Considering the symmetry, we can lower the number of multiplies from eight to four, which reduces the DSP blocs required to implement the filter [ALTERA, 1998].

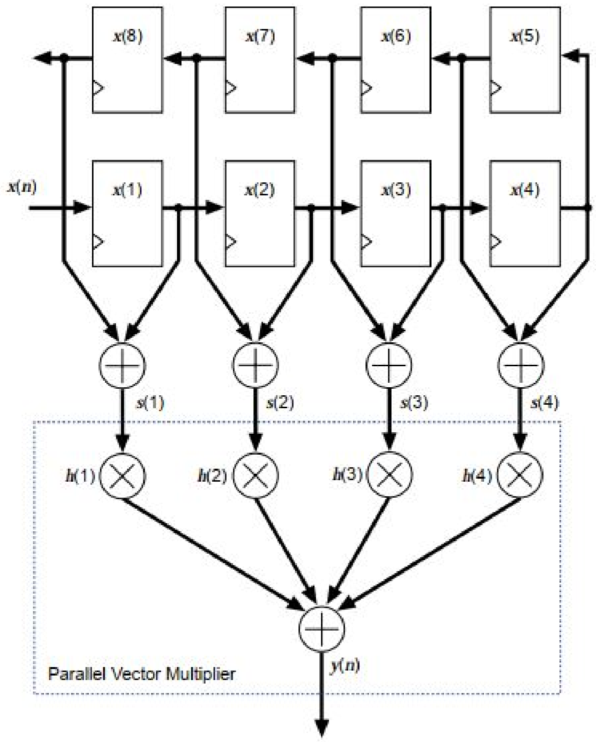

Figure 4.5: Optimized FIR filter architecture

4.6 DPD

DPD bloc is the most complicated one. In fact, since the input data and the coefficients are both complex, the main multiplying operation must be divided into many sub multiplication operations. Implemented design is a third order only polynomial equation as expressed below:

$$Output = C1 * Input + C3 * Input * \|Input\|^2 \tag{4.1}$$

Say that $Input = A + iB$, $C1 = a1 + ib1$ and $C3 = a3 + ib3$ then 4.1 will be:

$$Output = (a1 + ib1) * (A + iB) + (a3 + ib3) * (A + iB) * \|A + iB\|^2 \tag{4.2}$$

First, one important optimization can be done considering that :

$$\|A + iB\|^2 = (A + iB) * (A - iB) = A^2 + B^2$$

This property of complex numbers allows us to avoid calculating the modulus of the the input signal.
Hence, the final output signals will be as follow:

$$Re = (a1 + a3(A^2 + B^2))A - (b1 + b3(A^2 + B^2))B \tag{4.3}$$

$$Im = (b1 + b3(A^2 + B^2))A + (a1 + a3(A^2 + B^2))B \tag{4.4}$$

We can note that some bloc can be reused. Total number of multiplications is 8 and total number of adding is 6.

4.7 Digital front end top level

After finishing the design of the main blocs and testing them, comes the step of gathering them under a top level in order to construct a Digital front end. The top level will be composed of two zero padding blocs , tow FIR filters and a DPD bloc. The top level was designed with multiple coefficients and tested following the designing steps mentioned previously and the output of the VHDL design and Matlab script was equal.

4.8 Synthesis and implementation in Vivado

Vivado is software provided by XILINX company that allows Synthesis and implementation of hdl designs. We used it in order to verify that our design is implementable and to get it's complexity. Figure 4.6 shows the elaborated design schematic.

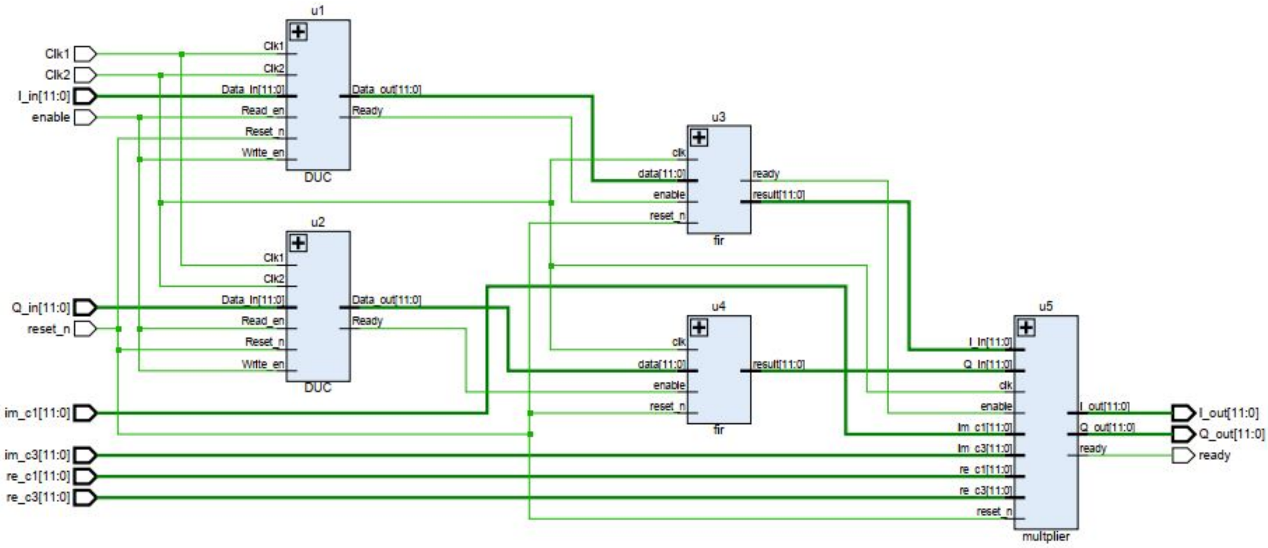

Figure 4.6: Elaborated design schematic

The complexity of the design was also given by the software in figure 4.7. Note the FPGA target was chosen with large number of logic blocs and DSP blocs. In most cases logic resources are limited and their use must be optimized.

Name	Slice LUTs (134600)	Slice Registers (269200)	Slice (33650)	LUT as Logic (134600)	LUT as Memory (46200)	LUT Flip Flop Pairs (134600)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
DPD	623	905	318	607	16	159	40	101	2
u1 (DUC)	73	53	35	65	8	43	0	0	0
u2 (DUC_0)	72	53	32	64	8	43	0	0	0
u3 (fir)	209	386	131	209	0	26	16	0	0
u4 (fir_1)	208	384	114	208	0	20	16	0	0
u5 (multplier)	62	28	20	62	0	26	8	0	0

Figure 4.7: Design complexity

last, we also get the time report which will give the maximum clock speed that can be accepted by the design.

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	14.671 ns	Worst Hold Slack (WHS):	0.082 ns	Worst Pulse Width Slack (WPWS):	19.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	1588	Total Number of Endpoints:	1588	Total Number of Endpoints:	946

All user specified timing constraints are met.

Figure 4.8: Time report

4.9 conclusion

This chapter was about VHDL implementation of static digital predistortion algorithm. First, zero padding bloc was designed with an asynchronous FIFO having two clocks signals sensitivity. Then, FIR filter design with 32 taps was explained and an optimized version was highlighted. DPD bloc design was also described and complex numbers multiplication was developed briefly. Gathering and connecting the mentioned blocs under the digital front end was the next step. Finally, the synthesis and implementation of the whole design in Vivado was presented followed by its complexity and timing report.

General conclusion

In wireless communication system, power amplifier is a very important component. Its inherent nonlinearity and memory effects lead to the in-band and out-of-band distortions and affect the power efficiency. Baseband digital predistortion is one of the most promising methods for compensating the distortions.

In this work, a preliminary introduction of the wireless communication domain was given with a detailed description of the PA characteristics. DPD popular techniques was also highlighted and model based DPD was chosen to work with during this project.
Baseband digital predistortion algorithm for linearizing power amplifiers with and without memory effects was simulated and tested on Matlab. True tests was also performed on a real power amplifier and using CODINTEK transmission platform. Spectra of the output signal was visualized on a spectrum analyzer and DPD enhancment was presented.

In addition, the DPD algorithm was implemented in VHDL and the design was tested and compared to Matlab equivalent algorithm. Synthesis and implementation was performed in Vivado and design complexity was highlighted.

As a future work, the design will be elaborated, and implemented on FPGA. After testing it's performance, we should focus on reducing it's complexity.

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Appendix A

Order	Terms	a_1V	a_2V^2	a_3V^3	a_4V^4	a_5V^5
Zero	DC		1		9/4	
First	ω_1	1		9/4		25/4
	ω_2	1		9/4		25/4
Second	$2\omega_1$		1/2		2	
	$2\omega_2$		1/2		2	
	$\omega_1 \pm \omega_2$		1		3	
Third	$3\omega_1$			1/4		25/16
	$3\omega_2$			1/4		25/16
	$2\omega_1 \pm \omega_2$			3/4		25/8
	$2\omega_2 \pm \omega_1$			3/4		25/8
Fourth	$4\omega_1$				1/8	
	$4\omega_2$				1/8	
	$3\omega_1 \pm \omega_2$				1/2	
	$3\omega_2 \pm \omega_1$				1/2	
	$2\omega_1 \pm \omega$				3/4	
Fifth	$5\omega_1$					1/16
	$5\omega_2$					1/16
	$4\omega_1 \pm \omega_2$					5/16
	$4\omega_2 \pm \omega_1$					5/16
	$3\omega_1 \pm 2\omega_2$					5/8
	$3\omega_2 \pm 2\omega_1$					5/8

Table 4.1: Two tone intermodulation products up to fifth order[Xiao, 2009]

Appendix B

LMS method is an adaptive algorithm based on gradient method. Its cost function is defined by minimizing the mean square error, as follows:

$$\epsilon = E\{|e(n)|^2\} \tag{4.5}$$

where e(n) is the error between the desired output and actual output. The error is defined by :

$$e(n) = d(n) - y(n) \tag{4.6}$$

$$y(n) = x^T(n)w(n) \tag{4.7}$$

where d(n) is the desired output, y(n) the actual output, x(n) the system input sequences, w(n) the weight function and $(.)^T$ transpose operation. The update of the weight is given by:

$$w(n+1) = w(n) + \mu e(n)x(n) \tag{4.8}$$

where μ is the step which controls the convergence speed. In LMS algorithm, the iteration is run, until a set of acceptable weight values are achieved such that the cost function ϵ is small enough.