Graehme Blair Drew Hasse EECS 355 Lab 2: Combinational Divider Simulation Results

Three simulations were run. Two divider test (32bit/16bit) and one comparator test (4bit).

The test cases for the comparator were hard coded.

Numbers for the divider tests were read in from a text file in the pattern:

Dividend

Divisor

And then passed to the divider component.

4 bit comparator input:

```
DINL_stimulus : process is

begin

DINL_tb <= "00000";

wait for 10 ns; DINL_tb <= "00110";

wait for 10 ns; DINL_tb <= "01010";

wait for 10 ns; DINL_tb <= "11110";

wait for 10 ns; DINL_tb <= "01000";

wait;

end process;

DINR_stimulus : process is

begin

DINR_tb <= "0001";

wait for 10 ns; DINR_tb <= "0000";

wait for 10 ns; DINR_tb <= "0010";

wait for 10 ns; DINR_tb <= "0111";

wait for 10 ns; DINR_tb <= "1000";

wait;

end process;

end architecture behave;
```

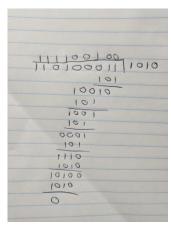


Figure 1 Binary Long Division by Hand

Waveform output:

-🔷 /comparator_tb/DINL_tb	00000	00000	00110	01010	11110	01000
- <pre>-<pre>/comparator_tb/DINR_tb</pre></pre>	0001	0001	0000	0010	0111	1000
/comparator_tb/DOUT_tb	0000	0000	0101	1000	0111	0000
/comparator_tb/isGreaterEq_tb	0					

16 bit divider simulation input: Output: 12 / 4 = 3 -- 0 16 / 2 = 8 -- 0 1000 / 0 = 1000 -- 0 OVERFLOW 12 / 7 = 1 -- 5 25000 / 250 = 100 -- 0 12 / 9 = 1 -- 3 3200 / 52 = 61 -- 28 58346 / 127 = 459 -- 53 12345 / 123 = 100 -- 45 9876 / 102 = 96 -- 84

Waveform output:

waveronn output.							
≨ 1 →	Msgs						
/divider_tb/start_tb	0						
-/ /divider_tb/dividend_tb	0000000000001100	000000000000110	0	0000000000001000	00	000000111110100	0
+	00000100	00000100		00000010		00000000	
	0000000000000011	0000000000000000001	1	000000000000000000000000000000000000000	00	000000111110100	0
/divider_tb/remainder_tb	00000000	00000000		00000000		00000000	
/divider_tb/overflow_tb	0						
10000000000001100	01100001101010	00	100000000000011	00			
100000111	111111010	33	00001001				
00000000000000001	00000000011001	.00	000000000000000	01			
00000101	00000000		00000011				

32 bit divider simulation input: Output:

1000000 / 2500 = 400 -- 0

12300 1000009 / 4598 = 217 -- 2243

1000009 1000009 / 4598 = 217 -- 2243

4598 3200000 / 24501 = 130 -- 14870

24501 3490000 / 9 = 387777 -- 7

3490000 9 123456 / 9876 = 12 -- 4944

123456 4543245 / 6475 = 701 -- 4270

9876

4543245 63665742 / 567 = 112285 -- 147 6475

63665742 27538530 / 9852 = 2795 -- 2190

567 27538530 6575097 / 45 = 146113 -- 12

Waveform output:

9852 6575097 45

<pre>/divider_tb/start_tb</pre>	0							
/divider_tb/dividend_tb	0000000000011	0000000000	000111101000010	0100	00000000	001000110	000101001	0100
/divider_tb/divisor_tb	0000100111000100	0000100111	1000100		00110000	000001100)	
/divider_tb/quotient_tb	000000000000000	0000000000	00000000000000000001	1001	00000000	00000000	00000000	0111
→ /divider_tb/remainder_tb	000000000000000000000000000000000000000	0000000000	000000		0010011	11101000		
/divider_tb/overflow_tb	0							
<u> </u>								
		<u>. </u>						
(00000000000001111010000100100.	[00000000011000	001101010000	000 10000000	00011010	10100000	01101		
(00000000000001111010000100100. (0001000111110110	(00000000011000			00011010		01101		
	01011111101101	01	0000000	00000100	1			
0001000111110110	01011111101101	01 00000000000000000000000000000000000	0000000	00000 100 000000 10	1 11110101			
0001000111110110 100000000000000000000	(00000000000000000000000000000000000	01 00000000000000000000000000000000000	0000000	00000 100 000000 10	1 11110101			
0001000111110110 000000000000000000000	(00000000000000000000000000000000000	01 00000000000000000000000000000000000	0000000	00000 100 000000 10	1 11110101			