NIST College
BScCSIT
First Semester
Digital Logic Lab Sheet
2017

Lab 1

Title: To be familiar with the basic gates.

***Objectives*:**

i) To verify experimentally the truth table of two inputs AND gate.
ii) To verify experimentally the truth table of two inputs OR gate.
iii) To verify experimentally the truth table of one input NOT gate.
iv) To construct 3 input AND gate using 2 inputs AND gate and so it's truth table with verification.
v) To construct and verify 4 inputs OR gate using 2 inputs OR gate.
vi) To verify and understand the output of NOT gate putting it into series of 2 and 3.

LAB 2

Title: To be familiar with Universal Gates and De-Morgan's Theorem

Objectives:

1. To verify the NAND Gate with 2 inputs.
2. To verify the NOR Gate with 2 inputs.
3. To verify the NAND Gate with 3 inputs.
4. To verify the NOR Gate with 3 inputs.
5. To verify De-Morgan Theorems
6. To evaluate the Universal property of NAND gate
    i. Construct and verify NOT gate using NAND gates.
    ii. Construct and verify AND gate using NAND gates.
    iii. Construct and verify OR gate using NAND gates.
    iv. Construct and verify NOR gate using NAND gates.

7. To evaluate the Universal Property of NOR gate
    i. Construct and verify NOT gate using NOR gates.
    ii. Construct and verify AND gate using NOR gates.
    iii. Construct and verify OR gate using NOR gates.
    iv. Construct and verify NAND gate using NOR gates.

LAB 3

Title: To be familiar with Exclusive gates

Objectives:

1. To construct and verify 2 input XOR gate.
2. To construct and verify 2 input XOR gate by implementation of basic gates.
3. To construct and verify 2 input XOR gate using only 2 input NAND gates.
4. To construct and verify 3 input XOR gate.
5. To construct and verify 2 input XNOR gate.
6. To construct and verify 2 input XNOR Gate by implementation of basic gates.

LAB 4

Title: To be familiar with Adder and Subtract

Objectives:

1. To construct and verify half adder circuit.
2. To construct and verify half subtract circuit.
3. To construct and verify half adder and subtract in one circuit.
4. To construct and verify full adder circuit.
5. To construct and verify full subtract circuit.
6. To construct and verify full adder and subtract in one circuit.

Lab 5

Title: To be familiar with decoder, encoder, multiplexer and de-multiplexer

Objectives:

1. To construct and verify 2-4-line decoder.
2. To construct and verify octal to binary encoder.
3. To construct and verify 4-1 multiplexer.
4. To construct and verify 1:4 de-multiplexer.
5. To construct and verify 8:1 multiplexer
6. To Construct and verify 1:8 demultiplexer.

Lab 6

Title: To be familiar with latches and flip-flop

Objectives:

1. To investigate the operation of NOR latch.
2. To investigate the operation of NAND latch.
3. To investigate the operation of T- latch.
4. To investigate the operation of C/K R-S latch.
5. To investigate the operation of Master Slave R-S latch.

LAB 7

Title: To be familiar with flip flops

Objectives:

1. To construct and verify J-K flip-flop using gates.
2. To verify S-R flip-flop
3. To verify J-K flip-flop.
4. To verify D flip-flop.
5. To verify T flip-flop.
6. To verify master-slave flip-flop.

LAB 8

Title: To be familiar with Counter

Objectives:

1. To construct and verify MOD 4 ripple up asynchronous counter
2. To construct and verify MOD 8 ripple up asynchronous counter.
3. To construct and verify MOD 16 ripple up asynchronous counter.
4. To construct and verify MOD 16 ripple asynchronous down counter.
5. To construct and verify above objectives using synchronously.
6. To construct and verify the Decade counter.

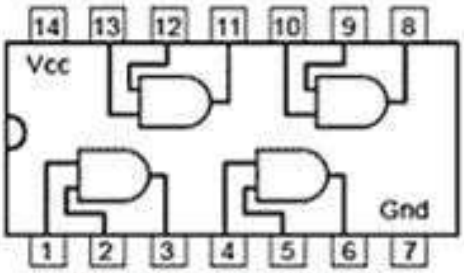
LAB 9

Title: To be familiar with Shift Register

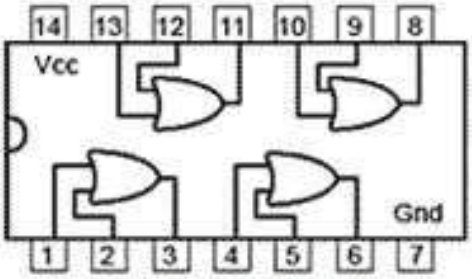
Objectives:

1. To construct and verify SISO shift register.
2. To construct and verify SIPO shift register.
3. To construct and verify PISO shift register.
4. To construct and verify PIPO shift register.
5. To construct and verify RING counter.
6. To construct and verify Jhonson counter.

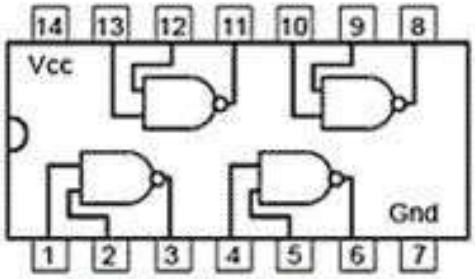
Pin configuration of different TTL IC



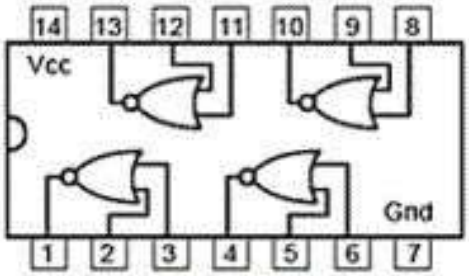
7408 Quad 2 input AND Gates



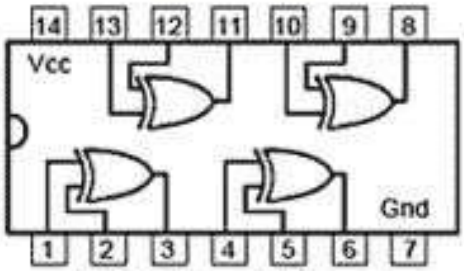
7432 Quad 2 input OR Gates



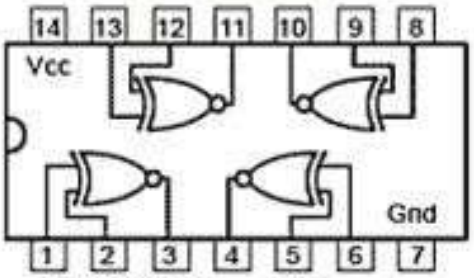
7400 Quad 2 input NAND Gates



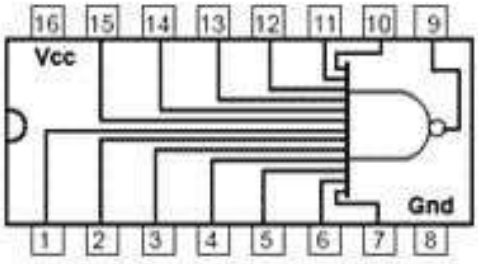
7402 Quad 2 input NOR Gates



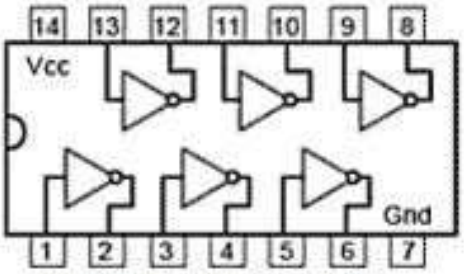
7486 Quad 2 input XOR Gates



747266 Quad 2 input XNOR Gates



74133 Single 13 input NAND Gate



7404 Hex NOT Gates (Inverters)

What should lab sheet content?

1. Cover page
2. Title
3. Objective
4. Theory
5. Observation
6. Conclusion

Note:

Lab sheet should be done in A4 paper. All diagrams, tables and figures should have drawn using pencil and scale with neat and clean labelling.