Digital Integrated Circuit

Unit-9

Transistor Transistor Logic (TTL)

- Introduced in 1964 by Texas Instruments
- Widely used family of digital devices.
- Fast, inexpensive, and easy to use.
- Uses active-low and active high signals
- Types:
  - Standard
  - High-speed
  - Low power
  - Schottky, and
  - Low-power Schottky

- Open collector and tristate devices → backbone of modern computer and digital systems; used to build buses
- Other digital family mostly used in CMOS → has very low power dissipation, so used in battery-powered equipment such as pocket calculators, digital wristwatches, and portable computers.

Switching Circuits

- Semiconductor devices used in digital integrated circuits include
  - diodes
  - bipolar junction transistors (BJTs), and
  - metal-oxide semiconductor field-effect transistor (MOSFETs)
- Mostly used TTL families : 7400 and 74LS00
- Mostly used CMOS families: 74C00 and 74HC00
- Basic elements used to construct these circuits are:
  - resistors
  - didoes, and
  - BJTs

The Semi conductor Diode

- Semi conductor diode sometimes called a *pn* junction
- Behaves like a one-way switch.

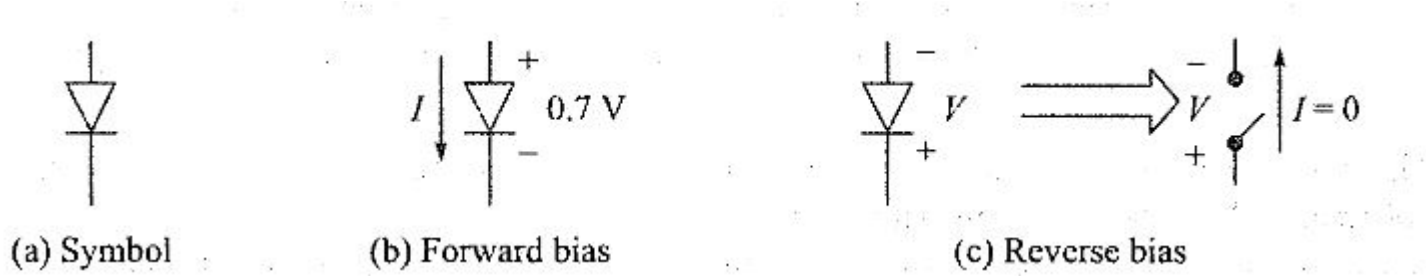


Figure: Semiconductor Diode

➢ When forward-biased, the diode conducts current, and the voltage across the diode terminals is about 0.7V.

➢ When reverse biased, the diode will not conduct current; the diode will acta like a open switch. The voltage across the diode terminal depends on the external circuits.

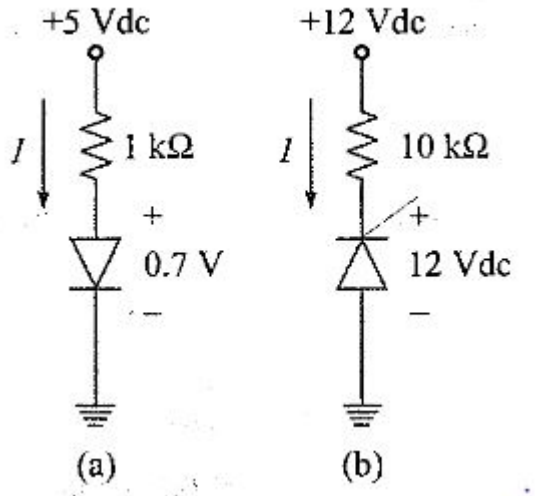
Q. For each diode in figure, determine whether the diode is forward or reverse biased. Determine the diode current I in each case.

Solution

(a) The current direction is from +5 Vdc to ground, and thus the diode is forward-biased. The voltage across the diode terminals is 0.7 Vdc, and the diode current is found as

$$I = (5 - 0.7)/1\ \text{k}\Omega = 4.3/1\ \text{k}\Omega = 4.3\ \text{mA}$$

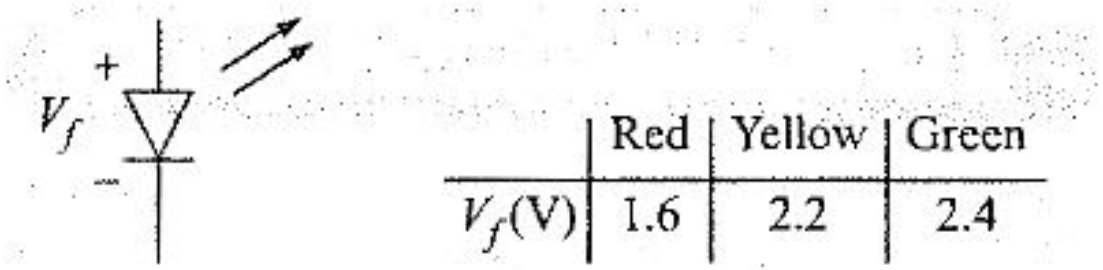
(b) The current direction is from +12 Vdc to ground, thus the diode is reverse-biased. The diode current is then $I = 0.0$ mA. There is no voltage across the 10-kΩ resistor, and thus the voltage across the diode terminals is 12 Vdc.



Figure

LEDs

- LED = light emitting diode
- The arrows indicate light emission capability.
- When forward biased, it emits light in the visible spectrum and is thus used as an indicator.
- The voltage across the diode terminals when forward biased in greater than 0.7V. V_f varies with color of the emitted light.
- The color of the emitted light depends on the element added to the semiconductor material during manufacturing.



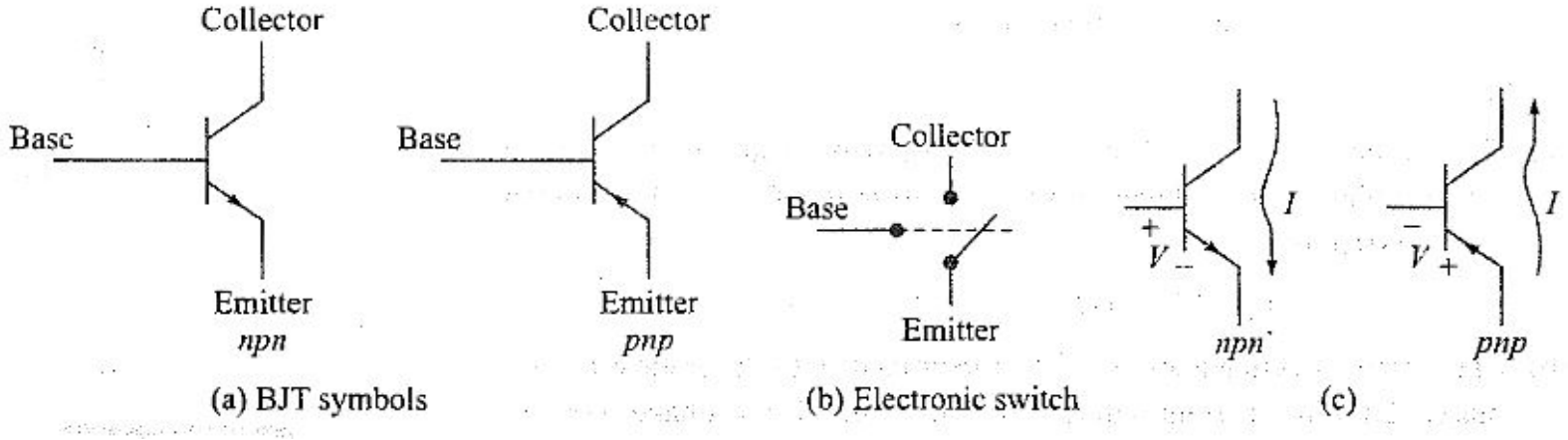
	Red	Yellow	Green
V_f(V)	1.6	2.2	2.4

(b) Typical forward voltages

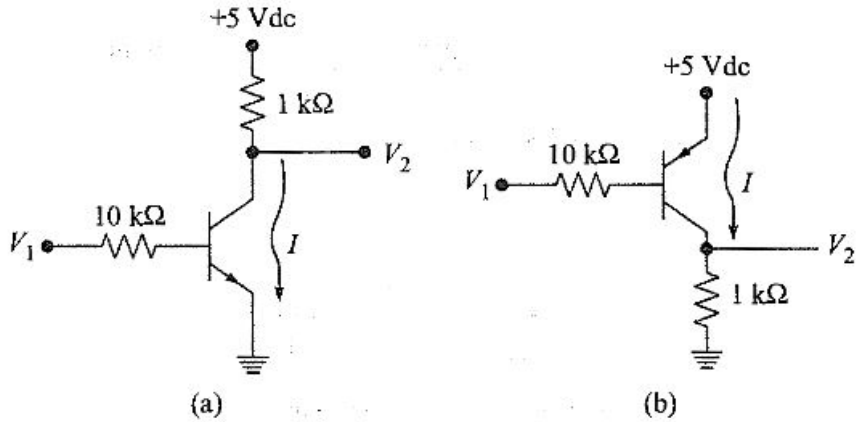
Figure: LED symbol and forward biased voltage for different color

Bipolar Junction Transistor (BJT)

- Available in two polarities: npn and pnp.
- BJT terminals: collector, emitter and base.
- BJT behaves as switch, by applying a voltage between base and emitter.
- When V_{BE}=0, the switch is off → no current between Collector and emitter; the transistor is off.
- When V_{BE}=V volt, the switch is ON → current between Collector and emitter; the transistor is ON. The voltage between emitter and collector (across a closed switch) is zero!
- For the npn, the base must be more positive than the emitter. The opposite is true for pnp.



Q. Determine the current I and the voltage V_2 for the circuit given below if i) V_1= 0 Vdc and ii) v_1= +5 Vdc



Solution

a. $V_1 = 0$ Vdc. There is no current in the 10-kΩ resistor. Thus the voltage base-emitter is zero. The BJT is off (switch is open). The BJT current and the current in the 1-kΩ resistor is zero. The voltage V_2 is +5 Vdc.

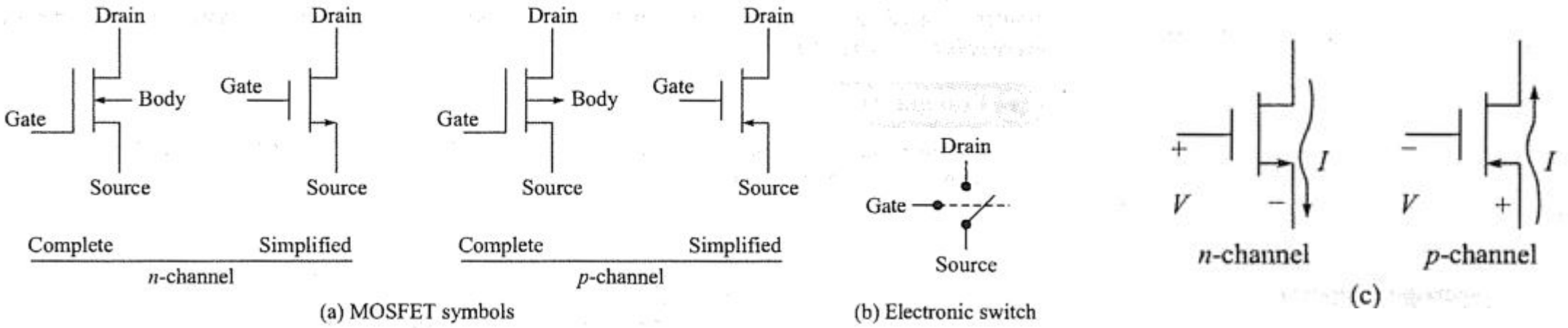
$V_1 = +5$ Vdc. The base is more positive than the emitter—the BJT is on (switch is closed). V_2 is zero. The BJT current is $I = 5$ mA.

b. V_1 is 0 Vdc. The base is more negative than the emitter—the BJT is on (switch closed), V_2 is +5 Vdc. The BJT current is $I = 5$ mA.

V_1 is +5 Vdc. There is no current in the 10-kΩ resistor. The base is at +5 Vdc, and so is the emitter. Thus the voltage base-emitter is zero, and the BJT is off (switch open). The current $I = 0$ mA, and $V_2 = 0$ Vdc.

MOSFETs

- Available in two polarities: n-channel and p-channel
- Operate in “depletion” or “enhancement” mode devices.
- MOSFETs terminals: *gate, source and drain*.
- Behaves as switch, by applying a voltage between gate and source.
  - When V_{GS}=0, the switch is open; no current is allowed between source and drain; the transistor is off.
  - When V_{GS}=V volt, the switch is closed; current is allowed between source and drain; the transistor is on. The voltage between source and drain (across a closed switch) is zero!.
- For the n-channel transistor, the gate must be more positive than the source. The opposite is true for the p-channel transistor.



Complementary Metal-Oxide-Semicondutor (CMOS) FETs

- NMOS ICs → ICs constructed entirely with n-channel MOSFETs.
- PMOS ICs → ICs constructed entirely with p-channel MOSFETs.
- CMOS ICs → IC constructed using both n-channel and p-channel; n-channel and p-channel MOSFETs are complementary devices. Examples: 74C00 and 74HC00 families.
- A CMOS is an inverter
  - V_1=0 Vdc, Q_n is off and Q_p is on. V2 = +5 Vdc.
  - V_1=+5 Vdc, Q_n is on and Q_p is off. V2 = 0 Vdc.
- In steady state (while not switching), one of the transistors is always off. So, current I = 0 mA.
- When switching between states, both transistors are on for a very short time because of the rise or fall time of V_1. this is the only time when current is non zero.
- CMOS is used in application where dc power supply current must be held to a minimum-watches, pocket calculators, etc.
- If the input V1 = +5 Vdc/2=2.5 Vdc, direct short occurs between + 5 Vdc and ground.

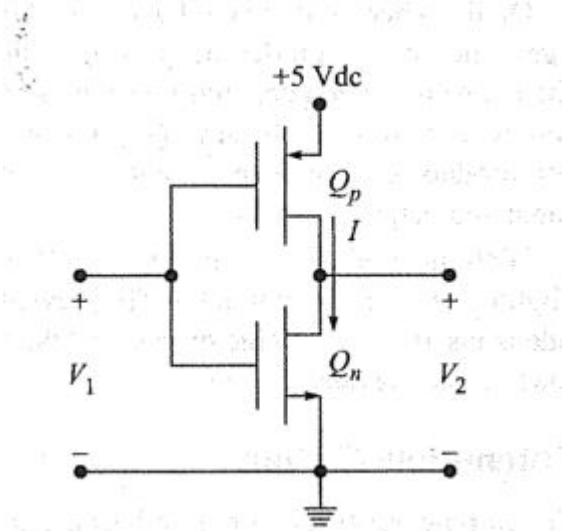


Figure: CMOS Inverter

7400 TTL

Standard TTL

- Figure: TTL NAND gate
- The multiple emitter input transistors is typical of gates and other devices in the 7400 series.
- Each emitter acts like a diode, therefore, Q_1 and the 4-KΩ act like a 2-input AND gate. The rest of the circuit inverts the signal so that the overall circuit acts like a 2-input NAND gate.
- The output of transistor (Q_3 and Q_4) form totem-pole connection (one npn in series with another).
  - With it, either the upper or lower transistor is on.
  - When Q_3 is on, the output is high; when Q_4 is on, the output is low.

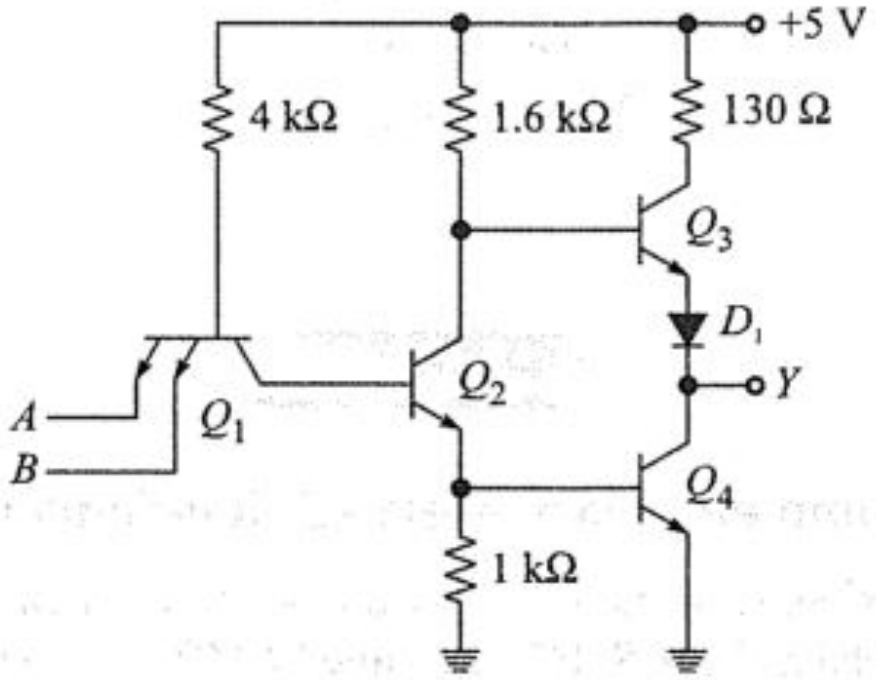


Figure: Two input TTL NAND gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Figure: Truth Table

- If A or B are low, the base of Q_1 is pulled down to approximately 0.7 V. this reduces the base voltage of Q_2 to almost zero. Therefor, Q2 cuts off. With Q_2 open, Q_4 if off, and the Q_3 base is pulled high. The emitter of Q_3 is only 0.7 V below the base, and thus the Y output is pulled up to a high voltage.
- When A and B are both high voltages, the emitter diode of Q_1 stop conducting, and the collector diode goes into forward conduction. This forces Q_2 to turn on. In turn, Q_4 goes on and Q_3 turns off, producing a low output.
- Without diode in D_1 in the circuit, Q_3 will conduct slightly when the output is low. To prevent this, the diode is inserted; its voltage drop keeps the base-emitter diode of Q_3 reverse biased. In this way, only Q_4 conducts when the output is low.

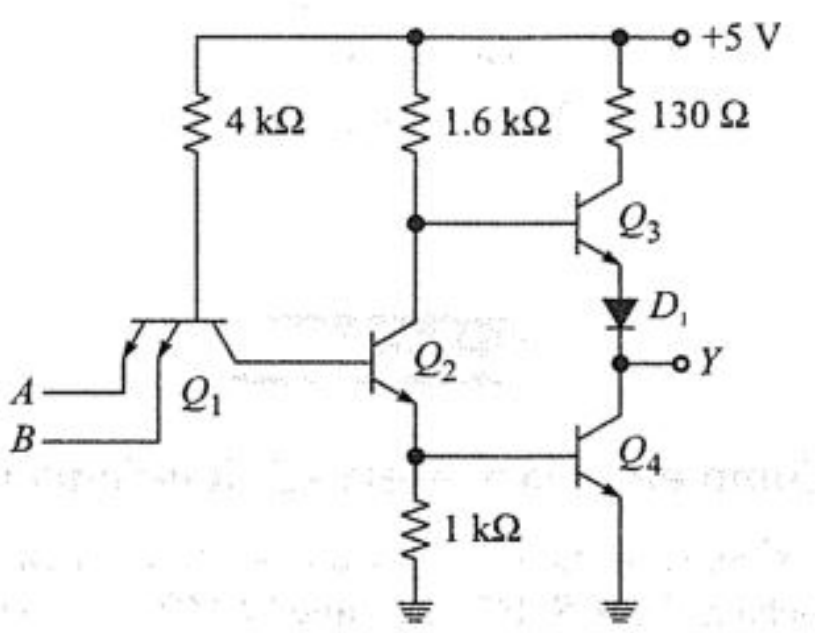


Figure: Two input TTL NAND gate

Propagation delay time

- ➢ The time it takes for the output of a gate to change after the inputs have changed.
- ➢ The propagation delay time of TTL gate is approximately 10 ns.

Power dissipation

- A standard TTL gate has power dissipation of about 10 milliwatt (mW).
- It may vary from this value because of signal levels, tolerances etc. but on average it is 10 mW.

Device Number

Device Number	Description
7400	Quad 2-input NAND gates
7402	Quad 2-input NOR gates
7404	Hex Inverter
7408	Quad 2-input AND gates
7410	Triple 3-input NAND gates
7411	Triple 3-input AND gates
7420	Dual 4-input NAND gates
7421	Dual 4-input AND gates
7425	Dual 4 input NOR gates
7427	Triple 3-input NOR gates
7430	8-input NAND gate
7486	Quad 2-input XOR gates

5400 Series

7400 series

- Temperature range of 0 to 70^{o}C
- Supply range: 4.754 to 5.25 V.
- Adequate for commercial application

5400 series

- Temperature range: -55 to 125^{o}C
- Supply range: 4.5 to 5.5 V
- Developed for military applications
- Rarely used for commercial because of high cost

Hight speed TTL

- By decreasing the resistance a manufacture can lower the time the internal time constants; this decreases the propagation delay time.
- Smaller resistance however increases power dissipation.
- This design variation is known as high speed TTL.
- Device number: 74H00, 74H02, so on.
- Power dissipation: approximately 22mw
- Propagation delay: approximately 6ns

Low-Power TTL

- By increasing the internal resistance a manufacture can reduce the power dissipation of TTL gates. This design variation is known as low-power TTL.
- Device are numbers 74L00, 74L02 and so on.
- This devices are slow because of large internal time constants and has propagation delay time of bout 35 ns.
- Has power dissipation of bout 1 mW.

Schottky TTL

- Problem with standard TTL, high-speed TTL and low-power TTL→ saturation delay time.
  - ➢ In these types, the transistor are switched with on with excessive current, causing a surplus of carriers to be stored in the base. When you have to switch a transistor from on to off, you have to wait for the extra carriers to flow out of the base. This delay is referred as saturation delay time.
- Schottky TTL reduces saturation delay time.
- Has forward voltage of 0.25 to 0.4 V → prevents saturation from saturating fully. This virtually eliminates saturation delay time, which means better switching speed.
- Devices are numbers as 74S00, 74S02,and so on.

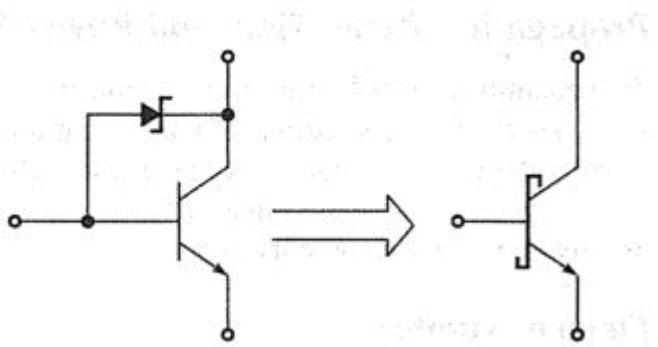


Figure: Schottky Diode

Low-Power Schottky TTL

- By increasing internal resistance and using Schottky diode, there comes a compromise between low power and high speed: Low-power Schottky diode.
- Devices are numbered as 74SL00, 74SL02, so on.
- Power dissipation: around 2 mW
- Propagation delay time: around 10 ns.

TTL Parameters

- Floating Inputs
- Worst-Case Input voltages
- Worst-Case Output voltages
- Profiles and Windows
- Sourcing and Sinking
- Noise Immunity
- Standard Loading

Floating Inputs

- When TTL input is high, the emitter current is nearly zero. (fig. a)
- When TTL input is *floating* (unconnected, fig. b), no emitter current is possible because of the open circuit. Therefore, a floating TTL input is equivalent to a high output.

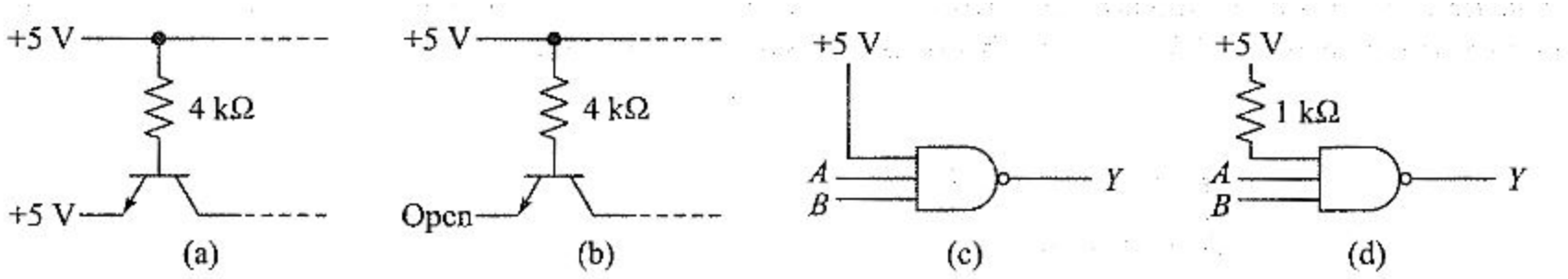


Figure: a) High input, b) Open is equivalent to high input, c) Direct connection to supply voltage, d) High input through a pull-up resistor

Worst-Case Input Voltages

- Figure shows a TTL inverter with an input voltage of V_i and an output voltage of V_o.
- When V_i=0 V, it is in low state and designated as V_{IL}. It can range from 0 V to 0.8 V. So, worst case low input $V_{IL,\ max}$=0.8 V.
- If $V_i > V_{IL,\ max}$, the output state is unpredictable.
- High state input voltage, V_{IH} ranges from 2 to 5 V. So, worst case high input $V_{IL,\ min}$=2 V.
- When $V_i < V_{IH,\ min}$, the output state is unpredictable.

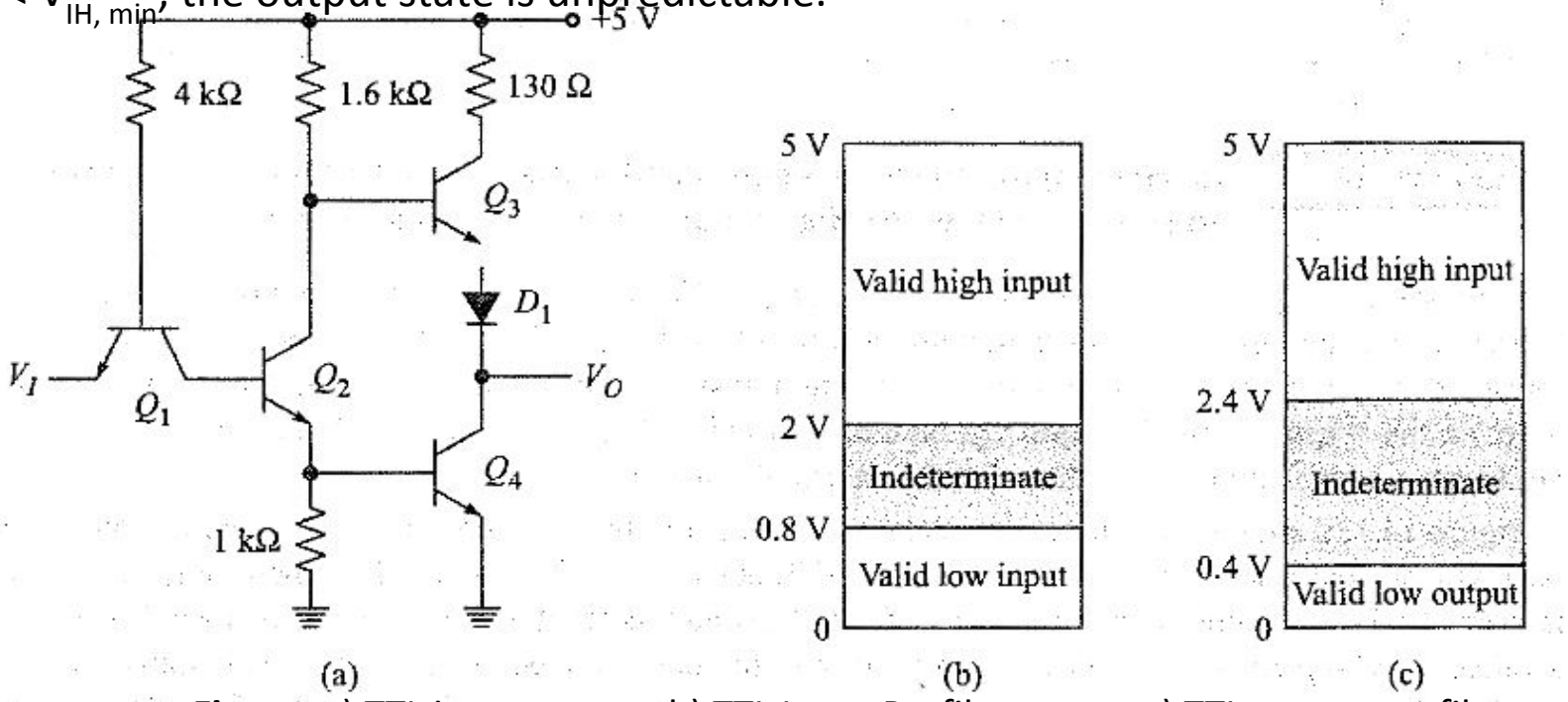


Figure: a) TTL inverter b) TTL Input Profile c) TTL output profile

Worst Case Output voltage

- Ideally, the low output sate is 0 V and the high output state is 5 V. because of internal voltage drop inside TTL devices, we cannot achieve these values.
- When the output voltage is low, Q_4 is saturated and has a small voltage drop across it. With TTL devices, any output voltage from 0 to 0.4 V is considered as a low output and designated as V_{OL}.
- When the output is high, Q_3 acts as emitter follower. Because of the voltage drop across Q_3, D1, and 130Ω resistor, the output voltage will be less than supply voltage. With TTL devices, the high-state output voltage is designated V_{OH} and has a value between 2.4 to 3.9 V. so V_{OH}, worst case high output min=2.4 V
- Any output between 0.4 and 2.4 V is indeterminate under worst-case conditions.

Profile and windows

- The input characteristic of figure a and output characteristic of figure b are called TTL input profile and TTL output profile respectively. Each rectangular area in figure can be thought as window.
- There is a low window(0 to 0.8V), an indeterminate window (0.8 to 2.0 V), and high window (2.0 to 5.0 V) in input profile. Similar in output profile.

Values to Remember (worst case values)

- $V_{IL, max}$ = 0.8 V
- $V_{IH, min}$ = 2 V
- $V_{OL, max}$ = 0.4 V
- $V_{OH, min}$ = 2.4 V

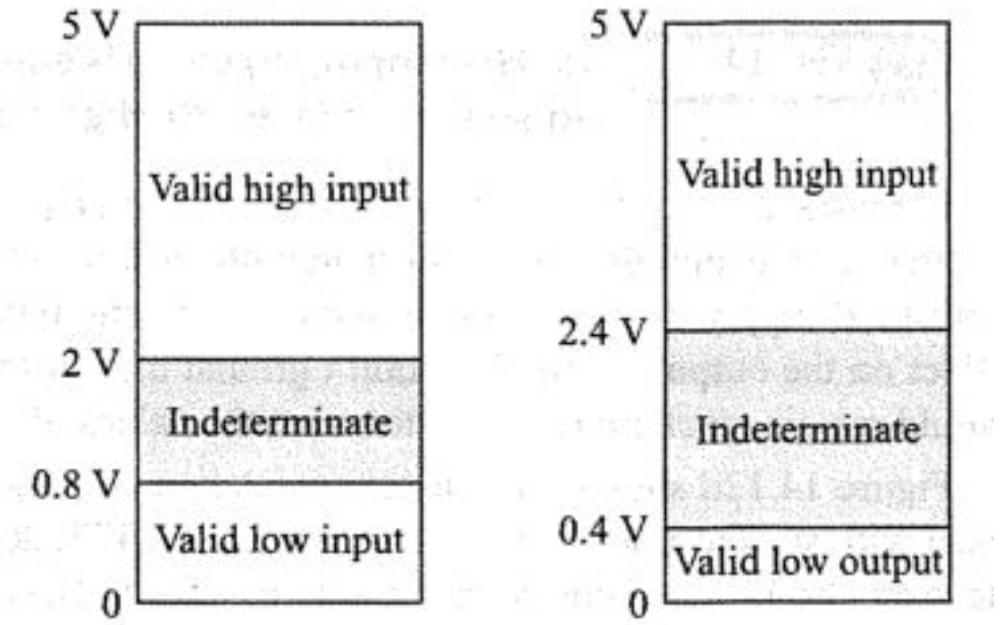
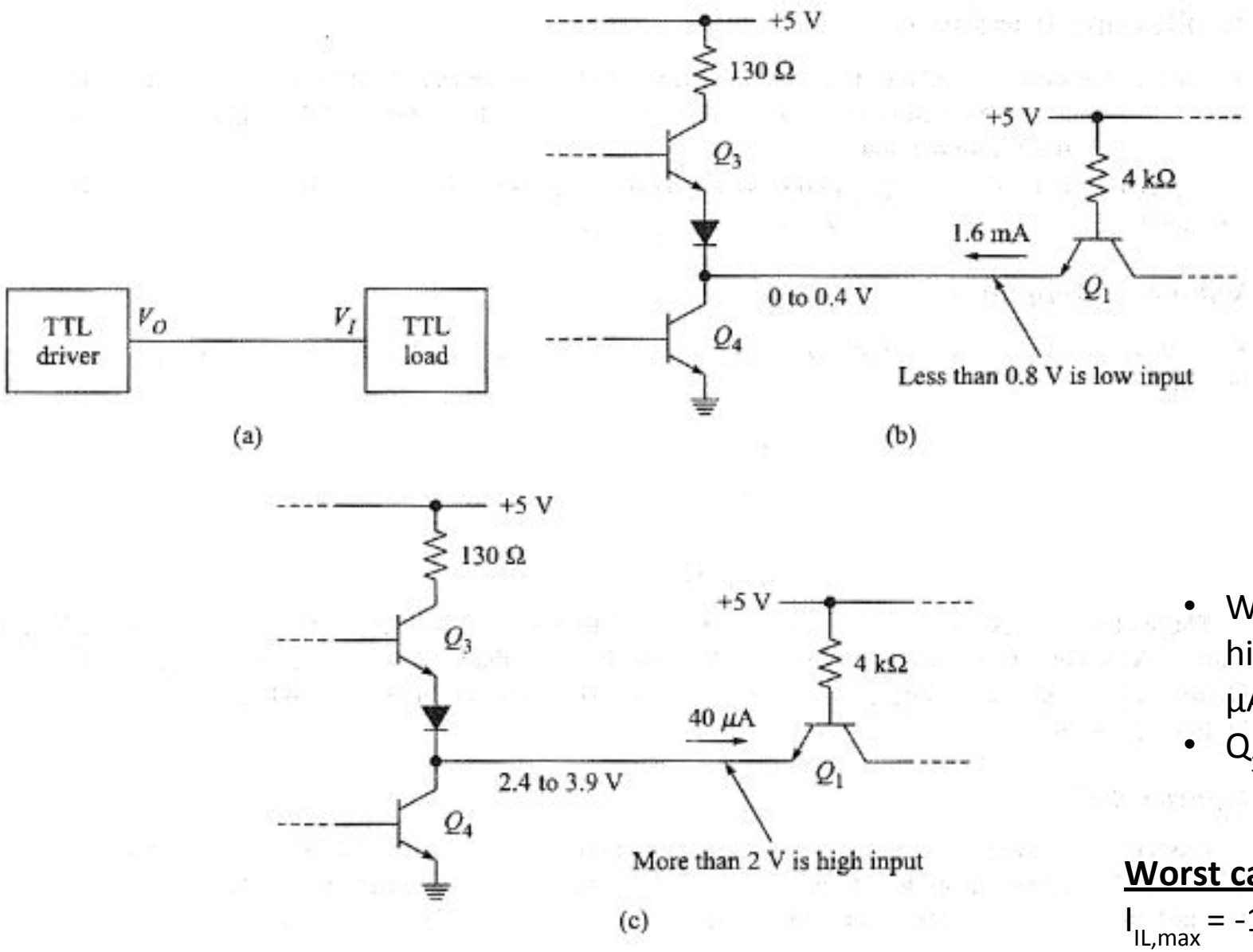


Figure: a) TTL Input Profile b) TTL Output Profile

Compatibility

- TTL devices are compatible because the low and high output window fit inside the low and high input windows.
- Therefore, the output of any TTL devices is suitable for driving the input of another TTL devices.
- Figure below shows one TTL device driving another. The first device is called a *driver* and the second is a *load*.



- When standard TTL output is low, an emitter current of around 1.6 mA exits in the direction shown.
- Because it is saturated, Q_4 acts like *current sink*.

- When the standard TTL output is high, a reverse emitter current of 40 μA exits in the direction shown.
- Q_3 is acting *as current source*.

Worst case input currents

$I_{IL,max}$ = -1.6 mA $I_{LH,max}$ = 40 μA

Figure: Sinking and sourcing current

Noise Immunity

- In worst case, there is a difference of 0.4 V between the driver output voltages and required load input voltage. For instance, the worst case values are:
  - ➢ $V_{OL, max} = 0.4$ V
  - ➢ $V_{IL, max} = 0.8$ V
- Similarly, the worst case high values are
  - ➢ $V_{OH, min} = 2.4$ V
  - ➢ $V_{IH, max} = 2$ V
- In either case, the difference is 0.4 V. This difference is called noise *immunity*. It represents built in protection against noise.

Why do we need protection against noise?

- The connecting wires between a TTL driver and load is equivalent to a small antenna that picks up stray noise signals.
- In worst case
- $V_{IL}=V_{OL} + V_{noise} = 0.4\ V + V_{noise}$
- $V_{IH} = V_{OH}-V_{noise} = 2.4\ V – V_{noise}$
- The TTL load has an input that is on the verge of being unpredictable in a noisy environment. The slightly additional noise voltage may produce a false change in the output state of the TTL load.

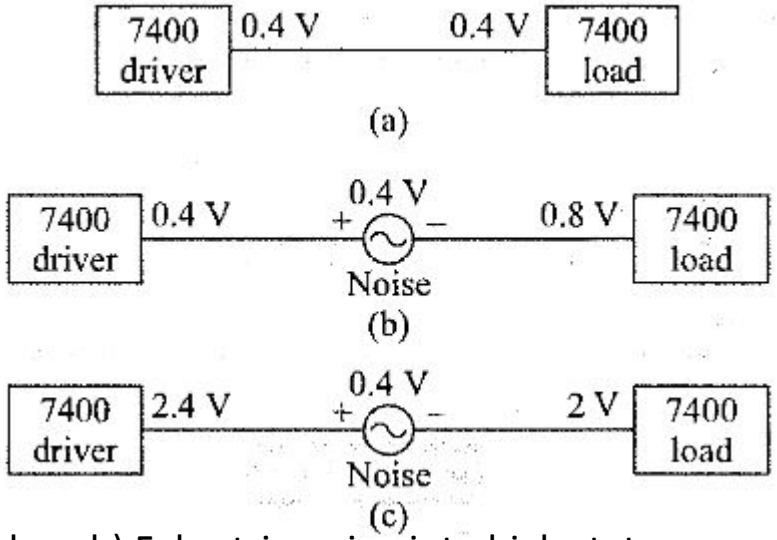


Figure: a) TTL driver and load b) False triggering into high state, c) False Triggering into low state

Standard Loading

- A TTL device can source current (high output) or sink current (low output).
- $I_{OL,\ max}$ = 16 mA
- $I_{OH,\ max}$ = -400 µA
- $I_{IL,\ max}$ = -1.6 mA
- $I_{IH,\ max}$ = 40 µA
- Since, the maximum output currents are 10 times larger than the input currents, we can connect up to 10 TTL emitters to any TTL output.

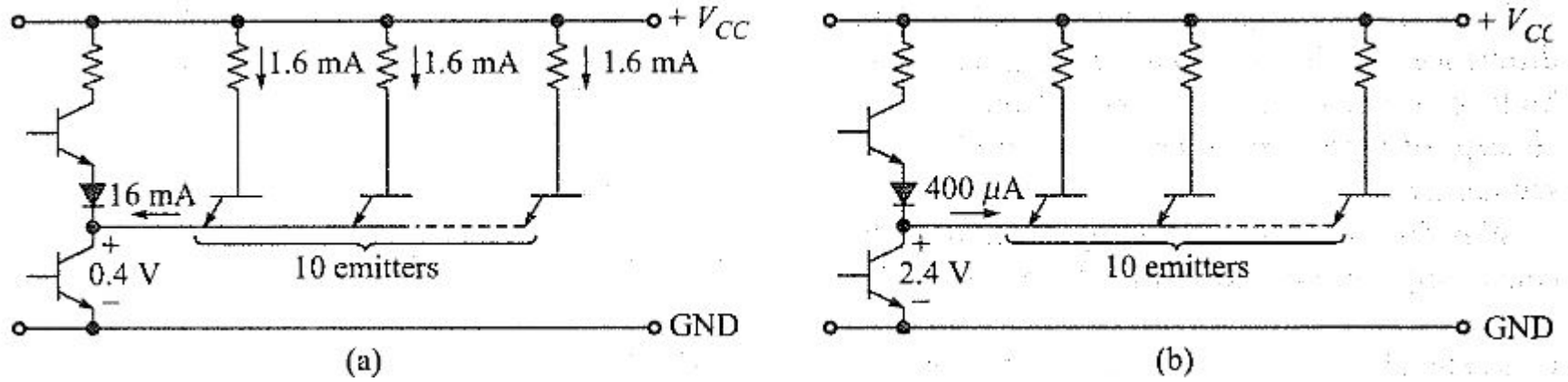


Figure: a) Low-state fanout b) High-state fanout

Fan-out is a term that defines the maximum number of digital inputs that the output of a single logic gate can feed.
Fan-in is a term that defines the maximum number of digital inputs that a single logic gate can accept

TTL Driver	*TTL Load*				
	74	*74H*	*74L*	*74S*	*74LS*
74	10	8	40	8	20
74H	12	10	50	10	25
74L	2	1	20	1	10
74S	12	10	100	10	50
74LS	5	4	40	4	20

Table: Fanouts

TTL Overview

NAND Gates

- The backbone of the 7400 series.
- All devices in this series are derived from the 2-input NAND gate.
- To produce 3-, 4-, and 8- input NAND gates, the manufacture uses 3-, 4-, and 8- emitter transistors.
- Least expensive devices in 7400 series

NOR Gates

- Here, Q5 and Q6 have been added to basic NAND gate design.
- Since Q2 and Q6 are in parallel, we get the OR function, which is followed by inversion to get the NOR function.
- When A and B are both low, the bases of Q1 and Q5 are pulled low; this cuts off Q2 and Q6. then Q3 acts as an emitter-follower, and we get a high output.
- If A or B is high, Q1 and Q5 are cut off, forcing Q2 or Q6 turn on. When this happens, Q4 saturates and pulls the output down to a low voltage.
- With more transistors, a manufacture can produce 3- and 4-input NOR gates. (Note: A TTL 8-input NOR gate is not available.)

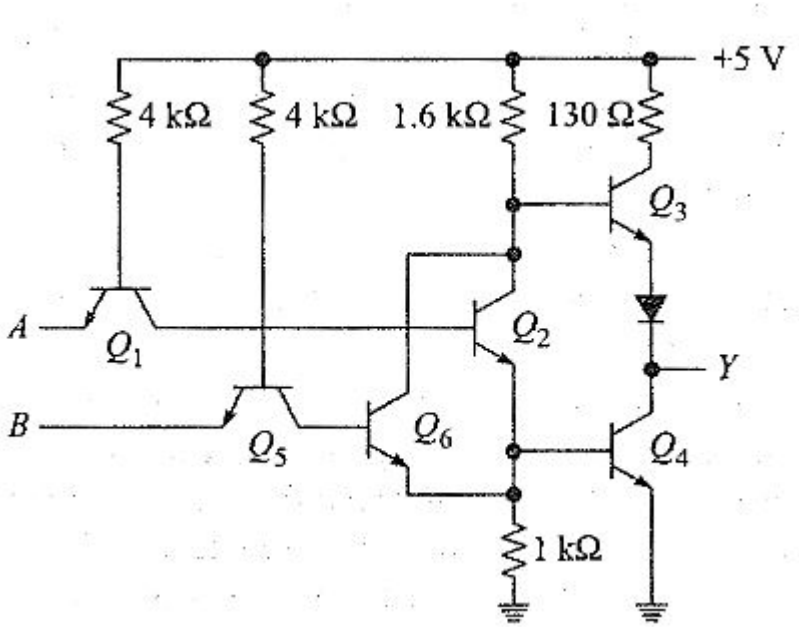


Figure: TTL NOR gate

AND and OR gates

- To produce the AND function, another inverting stage is inserted in the basic NAND gate design. The extra inversion converts the NAND to an AND gate.
- The available NAND gates are: 7408 (quad 2-input), 7411 (triple 3-input), and 7421 (dual 4-input).

- Similarly, another inverting stage can be inserted in the NOR gate to get OR gate.
- The only available TTL OR gate is the 7432 (quad 2-input).

Buffer Drivers

- ALL IC buffer can source and sink more current than standard TTL.
- Example: 7347 is a quad 2-input NAND buffer.
- Each gate has following worst case currents:

$$I_{IL} = -1.6\ mA \quad I_{IH} = 40\ \mu A$$
$$I_{OL} = 48\ mA \quad I_{OH} = -1.2\ mA$$

- The input currents are the same as those of 7400, but the output current are 3 times as high. That means, it can drive heavier loads. In other words, the fanout of a 7437 is 3 times that of 7400.

Open-Collector Gates

- Some TTL devices have an *open-collector output*. That is, they use only the lower transistor of a totem-pole pair.

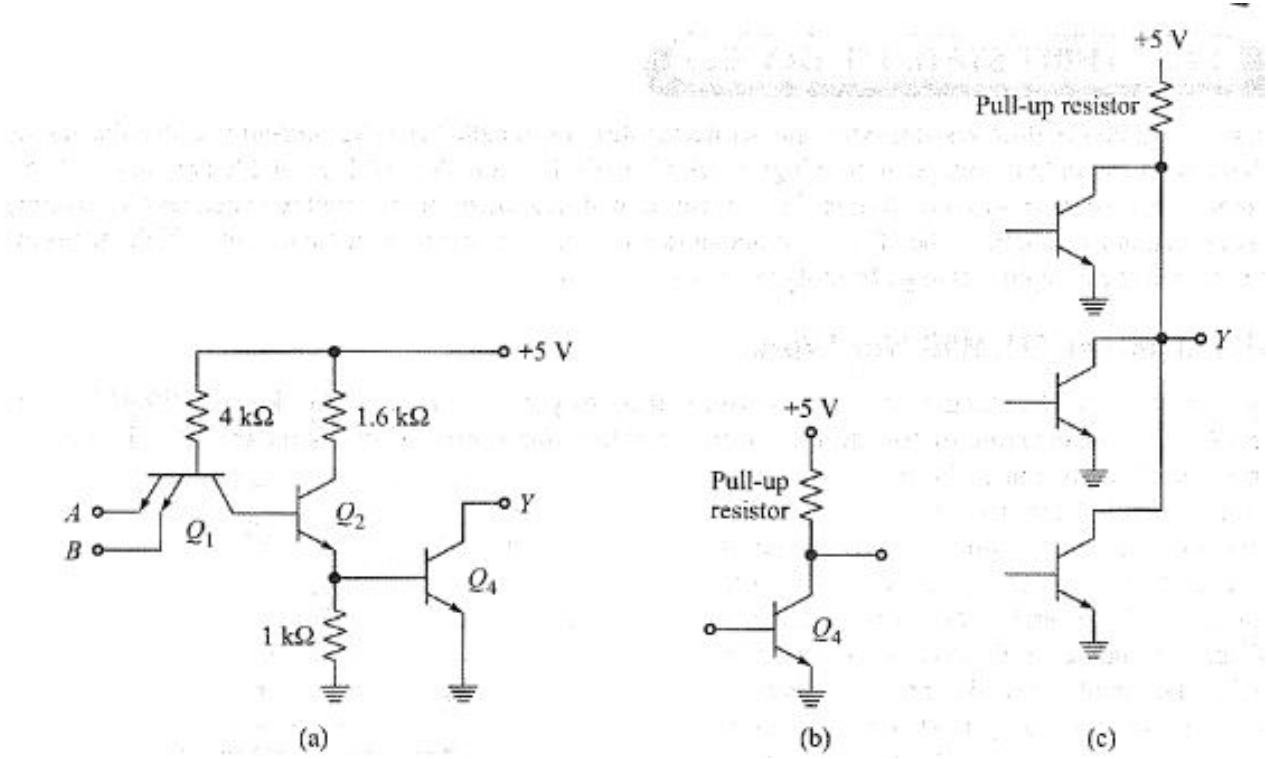


Figure: Open-collector TTL a) Circuit, b) Pull-up resistor, c) Open-collector outputs connected to a common pull-up resistor

- Because the collector of Q4, is open, a gate like this will not work properly until you connect an external pull-up resistor.

- The outputs of open-collector gates can be wired together and connected to a common pull-up resistor as in figure c above. (3 TTL devices connected to the pull-up resistor). This is known as *wire-OR* (some called in wire-AND).
- Disadvantages of open-collector gates: slow switching speed → worst when the output goes from low to high.
- Using active pull-up, which uses the modified totem-pole output to speed up the charging of stray output capacitance, switching time can improve.

Three-state TTL Devices

- Using a common pull-up resistor with open-collector devices is called *passive pull-up* because the supply voltage pulls the output voltage to the high level when all the transistor are cut off.
- *Active pull-up* is the modified from of totem-pole output to overcome the disadvantage of passive pull-up.

Why standard TTL will not work?

- Trying to wire-OR standard TTL gates will destroy one or more devices.
- In given figure, two output of pins of two standard TTL devices are connected.
- If the output of the second device is low, Q_4 is on and appears like a short circuit.
- If at the same time, the output of Q_1 is high, then Q_1 acts like as an emitter follower that tries to pull the output voltage to high level.
- Since, Q_1 and Q_4 are both conducting heavily, only 130Ω remains between the supply voltage and ground. The final result is an excessive current that destroys one of the TTL devices.

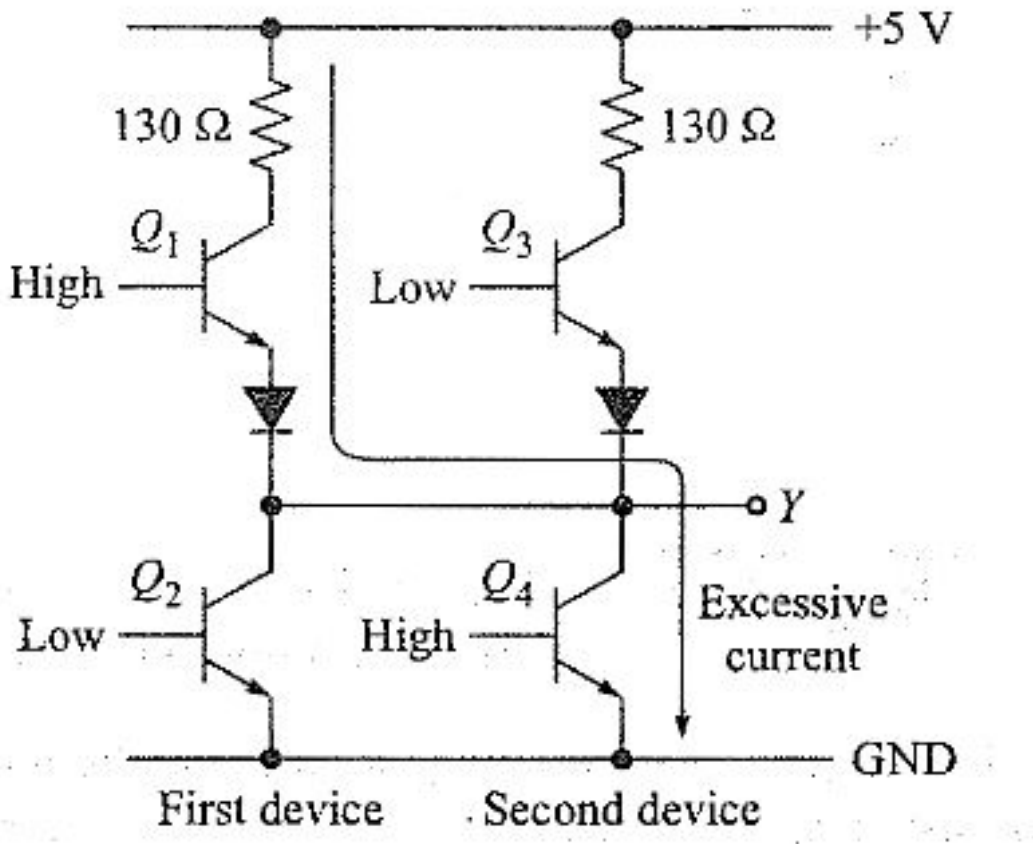


Figure: Direct connection of TTL outputs produces excessive current

Low Disable Input

- Three-state totem-pole outputs directly without destroying any devices and, avoids the loss of speed that occurs with open-collector devices.
- When DISABLE is low, the base and collector of Q_6 are pulled low →cuts off Q_7 and Q_8. therefore, the second emitter of Q_1 and the cathode of D_1 are floating. For this condition, the rest of circuit acts as inverter:
  - ➢ a low A input forces Q_2 and Q_5 to cut off, while Q_3 and Q_4 turn on, producing a high output.
  - ➢ a high a input forces Q_2 to turn on, which drives Q_5 on and produce a low output.

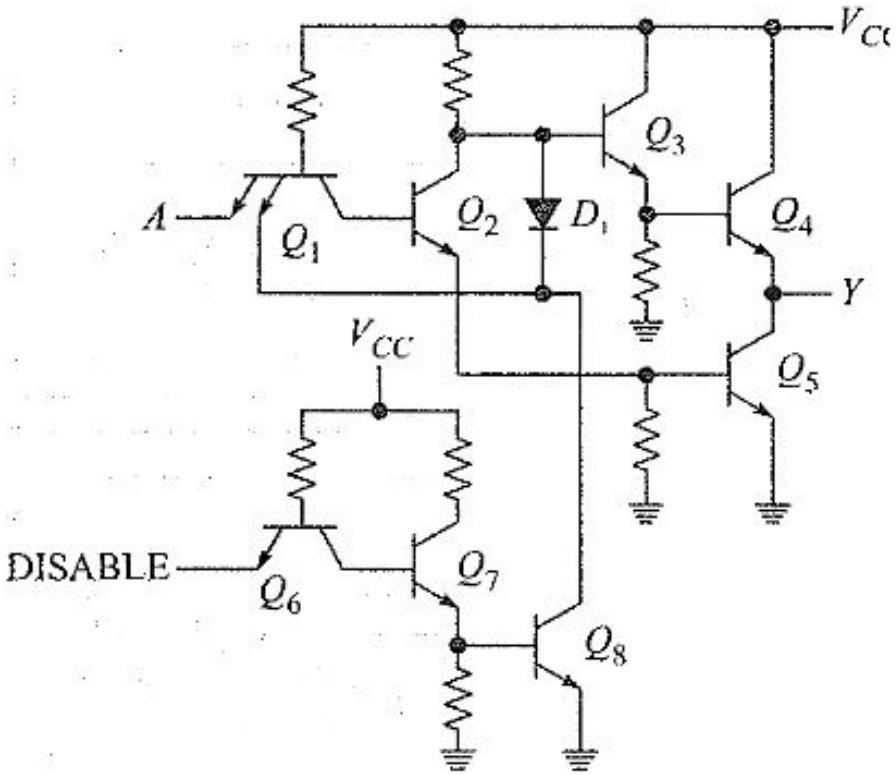


Figure: Three-State Inverter

DISABLE	A	Y
0	0	1
0	1	0
1	X	High Impedance

High DISABLE Input

- When DIABLE is high, the base and collector of Q_6 go high, which turns on Q_7 and Q_8. Ideally the collector of Q_8 is pulled to ground. This causes the base and collector of Q_1 to go low, cutting Q_2 and Q_5.
- Also Q_3 is off because of the clamping action of D_1 i.e. the base of Q_3 is only 0.7 V above ground, which is insufficient to turn on Q_3 and Q_4.
- With both Q_4 and Q_5 off, the y output is floating. Ideally, this means the Thevenin impedance looing back into the Y approaches infinity,

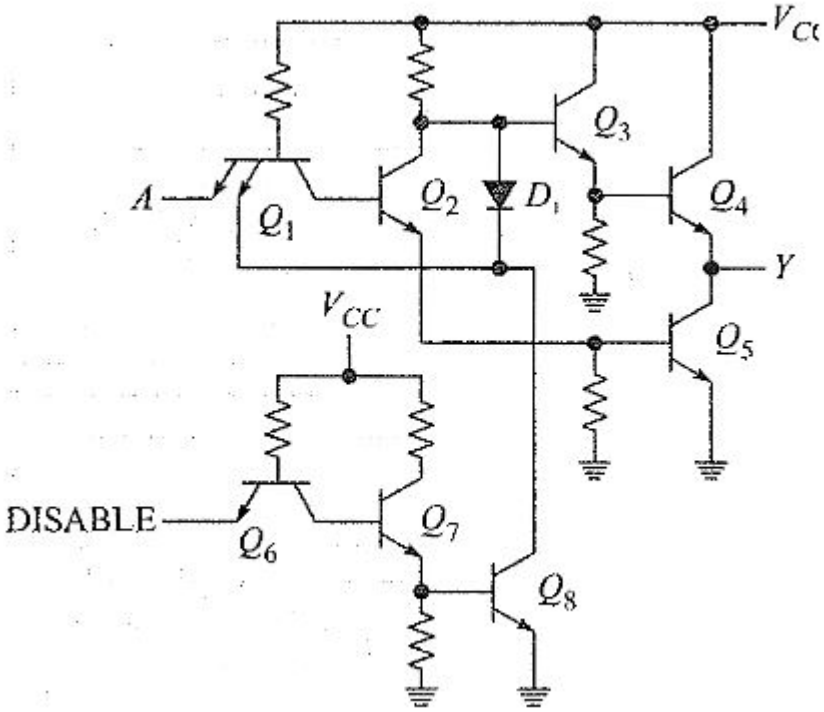


Figure: Three-state Inverter

Three-state Buffer

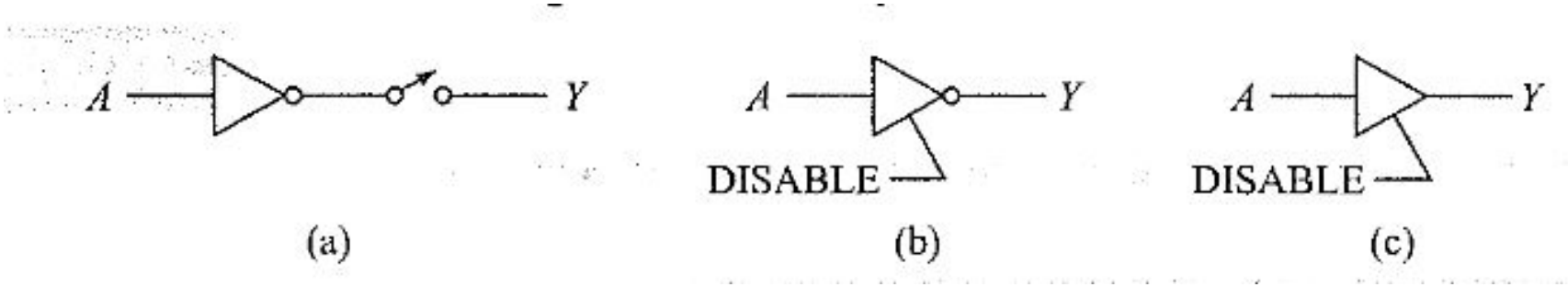


Figure: Three-state logic diagrams: a) Equivalent circuit of inverter, b) Logic symbol of inverter, c) Logic symbol of buffer

- 74365 is an example of a commercially available three-state hex non-inverting buffer.
- Used in organizing digital components around a bus.

External Drive for TTL Loads

- To drive a TTL load with an external source, need to satisfy the TTL input requirements for voltage and current.
- For standard TTL,
  - ➢ in the low state, an input voltage between 0 and 0.8 v with a current of around 1.6 mA.
  - ➢ in the high state, the voltage has to be from 2 to 5 v with current of around 40 µA.

Switch drive

- With switch open, the input is pulled up to +5 V. in worst case, 40 µA current exist. So voltage appearing at the input pin, V_i = 5 V –(40 µA)(1 kΩ) = 4.96 V, which is well above minimum requirement of 2 V, which is fine because it means that the noise immunity is excellent.

- When switch is closed, the input is pulled to ground. In worst case, the input current is 1.6 mA. This sink creates no problem because it flows through the closed switch to ground. The noise immunity is fine because the input voltage if 0 V, well below the maximum allowable value of 0.8 V.

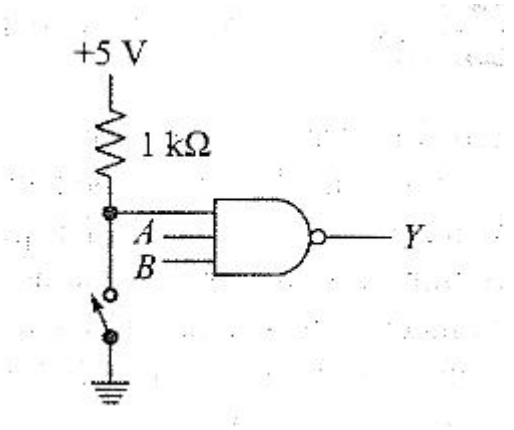


Figure: Switch Drive for TTL Input

Transistor Drive

- When Vi is low, the transistor if off and is equivalent to an open switch. Then the TTL input is pulled to +5V through resistance of 1 kΩ.
- When V_i is high, the transistor is on and is equivalent to a closed switch. In this case, it easily sinks the 1.6 mA of input current.
- The transistor inverts the control signal V_i. The double inversion produces an in-phase control signal at the TTL input.

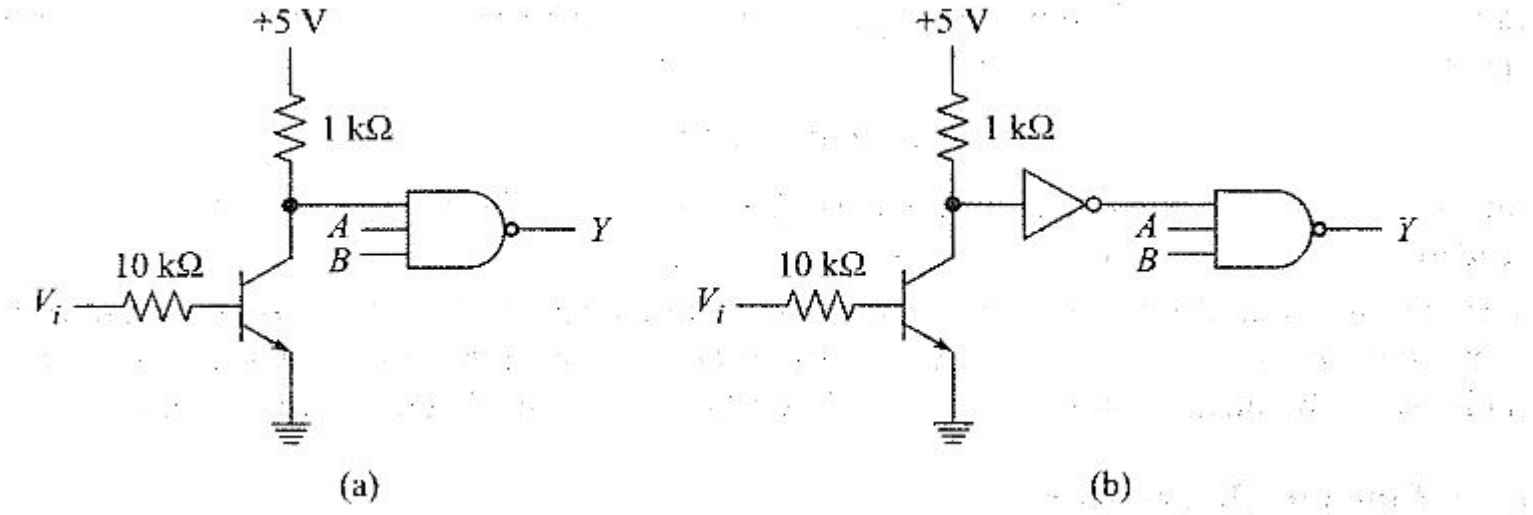


Figure: a) Transistor drive for TTL input, b) Inverter eliminates transistor inversion

TTL Driving External Loads

- Because standard TTL can sink up to 16 mA, TTL driver can be used to control an external load such as relay, LED, etc.
- When the TTL output is high, there is no load current.
- But when the TTL output is low, the lower end of R_L is ideally grounded. This set up a load current of approximately $I_L = 5\ V / R_L$
- Since standard TTL can sink a maximum of 16 mA, the load resistance is limited to a minimum value of about
- $R_L = 5\ V / 16\ mA = 312\Omega$.

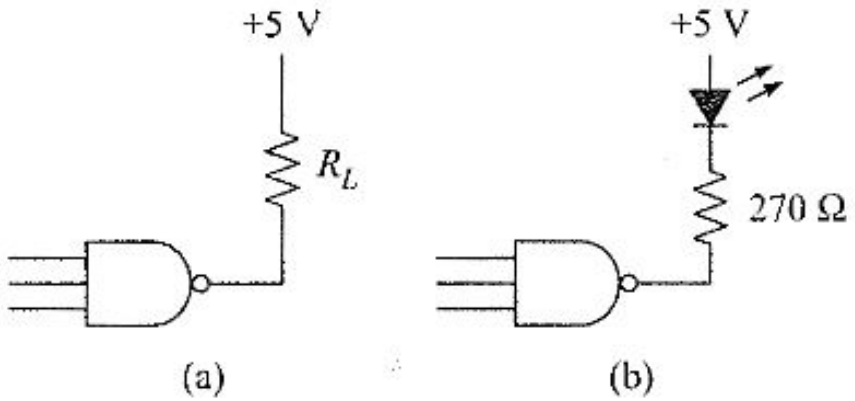


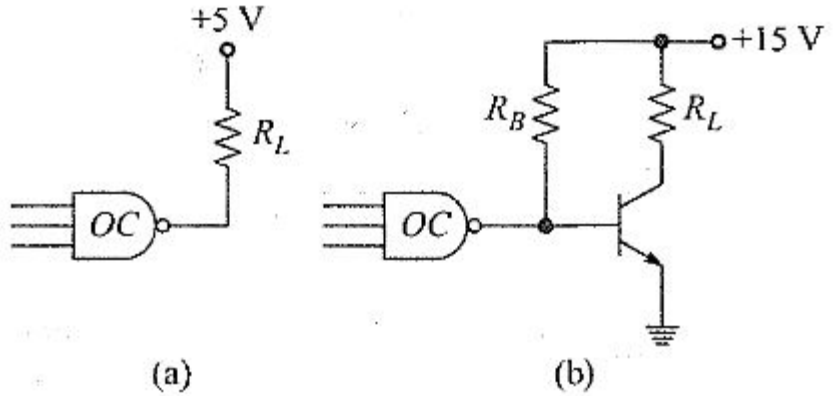
Figure: a) TTL output drives load resistor, b) TTL output drives LED

Driving an LED

- When TTL output is high, the LED is off.
- When the TTL output is low, the LED lights up. If the output voltage drop is 2 V, the LED Current is:
- $I_L = (5\ V - 2V)/270\Omega = 11.1\ mA$.

Supplying Voltage Different from + 5V

- Use open collector TTL Devices
- Since open-collector device can sink a maximum of 16 mA, the minimum load resistance in figure a is 1 kΩ.
- Use external transistor to get more than 16 mA load current.



- When the open-collector device has a low output, the external transistor goes off and the load current is zero.
- When the open-collector device has a high output, the external transistor goes on and the load current is maximum..

74C00 Series

- National Semiconductor pioneered the 74C00 series
- Compatible with TTL devices of similar number. For instances, the 74C00 is quad 2-inut NAND gates, the 74C02 is quad 2-input NOR gate and so on.
- Contains a variety of small-scale integration (SSI) and medium-scale integration (MSI)
- Useful too build battery-powered equipment

CMOS NAND Gate

- Q_1 and Q_2 form one complementary connection; Q_3 and Q4 form another.
- A low A will close Q_1 and open Q_2; a high A input will open Q_1 and close Q_2.
- Similarly, a low B input will open Q_3, and close Q_4; a high B input will close Q_3 and open Q_4.
- The Y output is pulled up to the supply voltage when either Q_1 or Q_4 is conducting.
- The output is pulled to ground only when Q_2 and Q_3 are conducting.

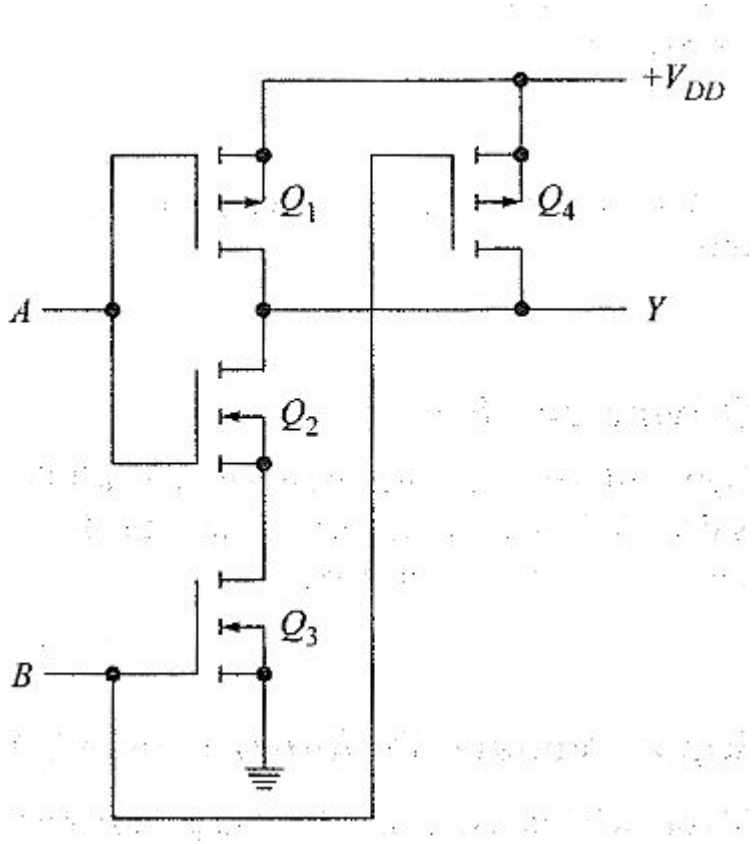


Figure: A CMOS NAND Gate

A	B	Y
Low	Low	High
Low	High	High
High	Low	High
High	High	Low

- Case 1: Here A and B is low. Because A is low, Q_1 is closed. Therefore Y is pulled high through the small resistance of Q_1.

- Case 2: Now A is low and B is high. Since A is still low, Q_1 remains closed and Y stays in the high state.

- Case 3: The A input is high and the B is low. Because B is low, Q_4 is closed. This pulls Y up to the supply voltage through the small resistance of Q_4.

- Case 4: The A is high, and the B is high. When both inputs are high, Q_2 and Q_3 are closed, pulling the output to ground.

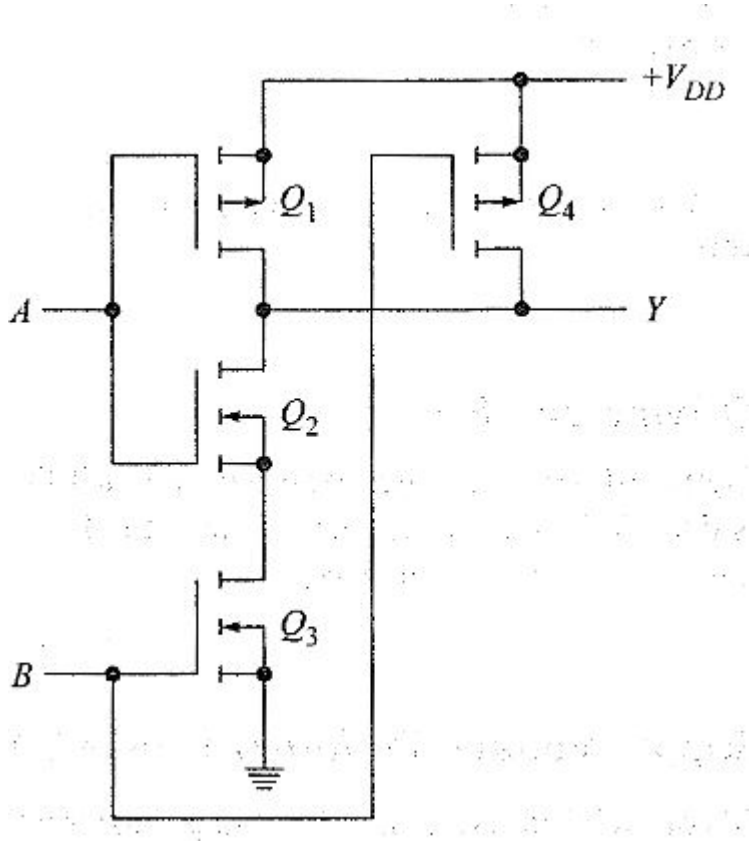


Figure: A CMOS NAND Gate

A	B	Y
Low	Low	High
Low	High	High
High	Low	High
High	High	Low

NOR Gate

- The output goes high only when Q1 and Q2 are closed. The output goes low if either Q3 or Q4 is closed.

<u>The four possible cases are:</u>

- Case 1: The A is low, and the B is low. For both inputs low, Q_1 and Q_2 are closed. Therefore, Y is pulled high through the small resistance of Q_1 and Q_2.
- Case 2: The A is low, and the B is high. Because B is high, Q_3 is closed, pulling the output down to ground.
- Case 3: The A is high, and the B is low. With A high, Q_4 is closed. The closed Q_4 pulls the output low.
- Case 4: The A is high, and the B is high. Since A is still high, Q_4 is closed and the output remains low.

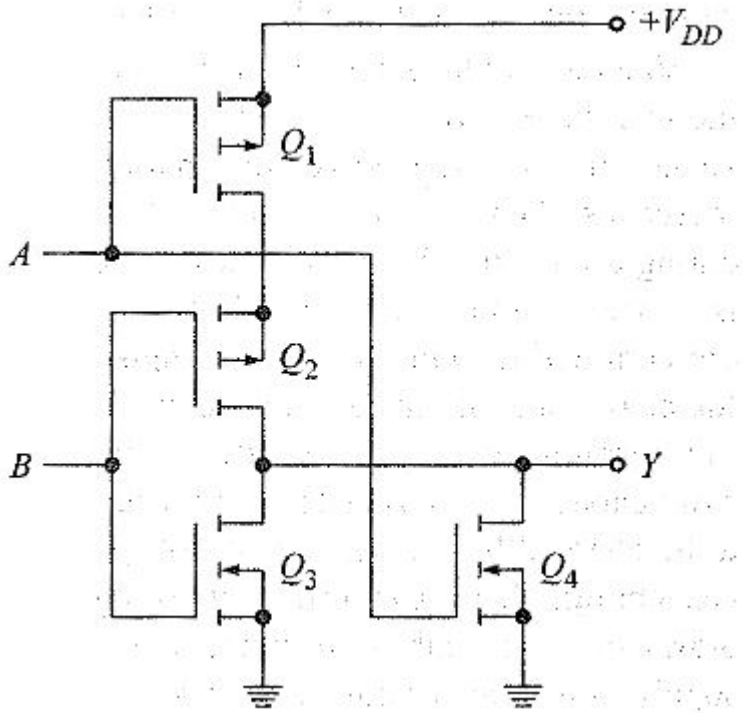


Figure: CMOS NOR Gate

A	B	Y
Low	Low	High
Low	High	Low
High	Low	Low
High	High	Low

Propagation Delay Time

- Propagation delay time t_p is approximately 25 to 100ns, with exact value depending upon the power supply voltage and other factors.

- When two or more CMOS gates are cascaded, the propagation delay time of each gates are added together to get total.

CMOS Characteristics

- 74C00 works over temperature range of -40 to + 85oC and over a supply range of 3 to 15 V.

Floating Inputs

- ➢ Setup a possible noise problem,
- ➢ Produce excessive power dissipation
- ➢ Because of insulated gates, a floating input allows the gate voltage to drift into the linear region, causing excessive current flow through push-pull stages.

Easily damaged

- Because of the thin layer of silicon dioxide between the gate and substrate, CMOs devices have a very high input resistance, approximately infinite.
- The insulating layer is kept as thin as possible to give the gate more control over the drain current.
- Because of this layer is so thin, it is easily destroyed by excessive gate voltage.
- One way to protect against overvoltages is to include diodes across the input.

Transfer Characteristic of a CMOS Inverter

- When the input voltage is low state, the output voltage is in the high state.
- As the input voltage increases, the output remains in the high state until a threshold is reached.
- Somewhere near an input voltage $V_{cc}/2$, the voltage greater than $V_{cc}/2$ holds the output in the low state.
- This transfer characteristic is an improvement over TTL because:
  - ➢ The indeterminate region is much smaller
  - ➢ Noise immunity if 45 percent of $V_{cc}/2$
  - ➢ The logic swing between the low and high output states approximately equals the supply voltage.

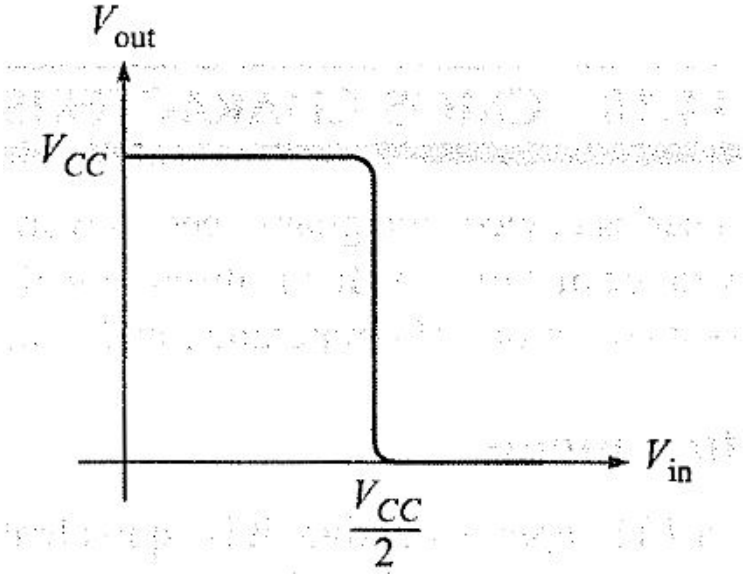


Figure: Transfer Characteristic of a CMOS gate

Compatibility

- CMOS devices are compatible with one another because the output of any CMOS device can be used as the input to another CMOS device.

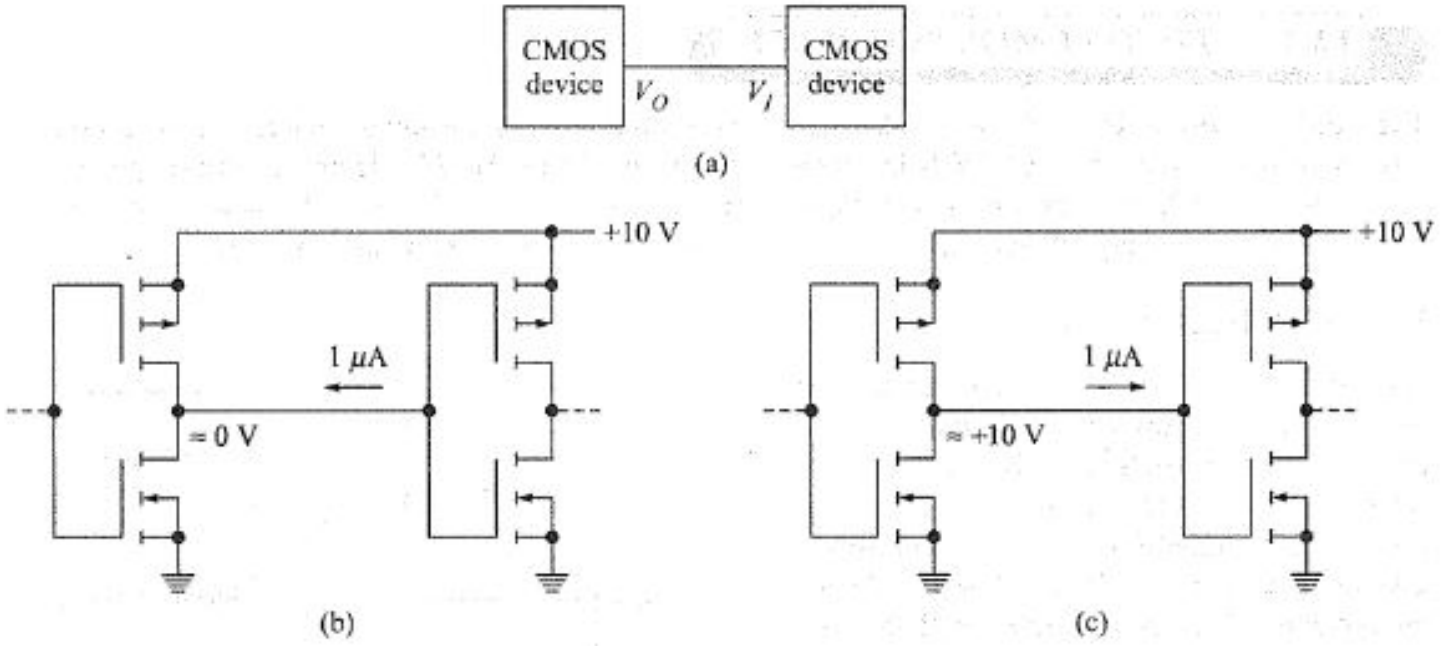


Figure: a) output of CMOS device an drive input of another CMOS device,
b) Sink currentc) source current

Worst-case input currents for CMOS devices:

$I_{IL,\ max}$ = 1 μA $I_{IH,\ max}$ = 1 μA

$I_{OL,\ max}$ = 10 μA $I_{OH,\ max}$ = -10 μA

Fanout: 10

TTL-To-CMOS Interface

- The word interface refers to the way a driving device is connected to a loading device.
- TTL devices need a supply voltage of 5 V, while CMOS devices can use any supply voltage from 3 to 15 V.
- Because the supply requirements differ, several interfacing schemes may be used.

Interfacing at supply voltage 5 V

- There is no problem with TTL low-state window (0 to 0.4 V) because it fits inside the CMOS low-state window (0 to 1.5 V). This means, the CMOS load always interprets the TTL low-state drive as a low.
- The problem is in the TTL high state. Need to do something extra to make the two different devices compatible. → standard solution is to use a pull up resistor between TTL driver and the CMOS load as shown in figure below.

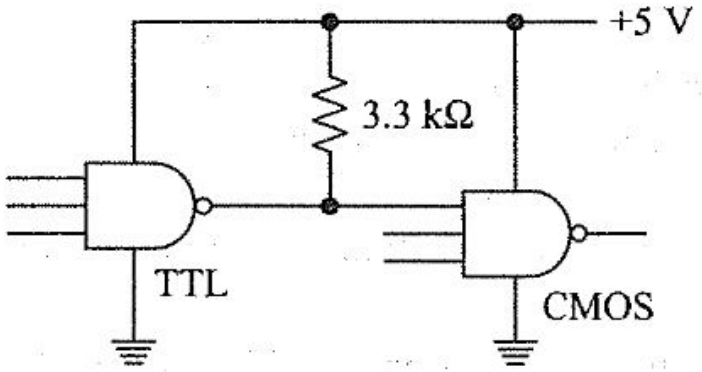


Figure: TTL driver and CMOS load

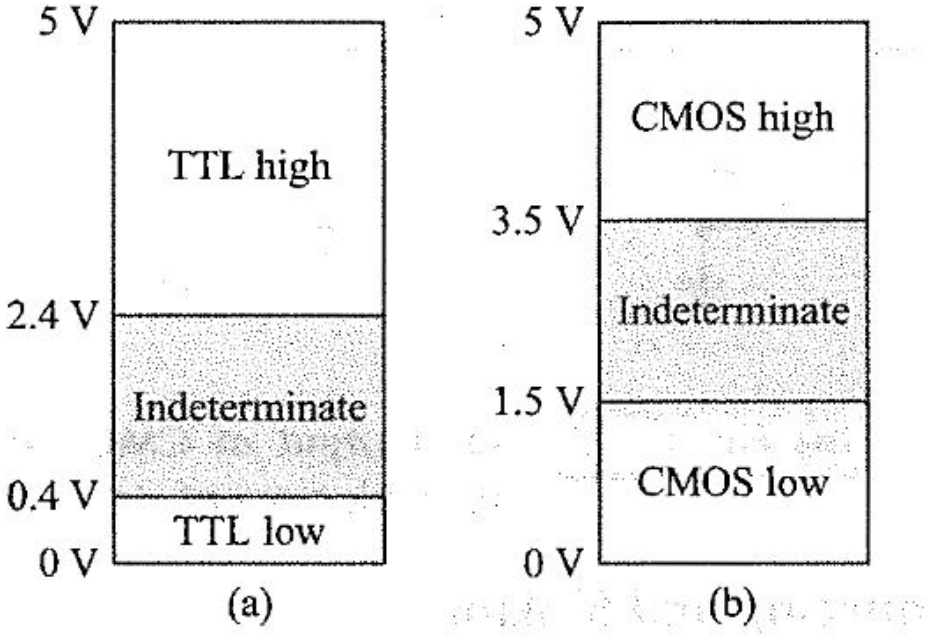
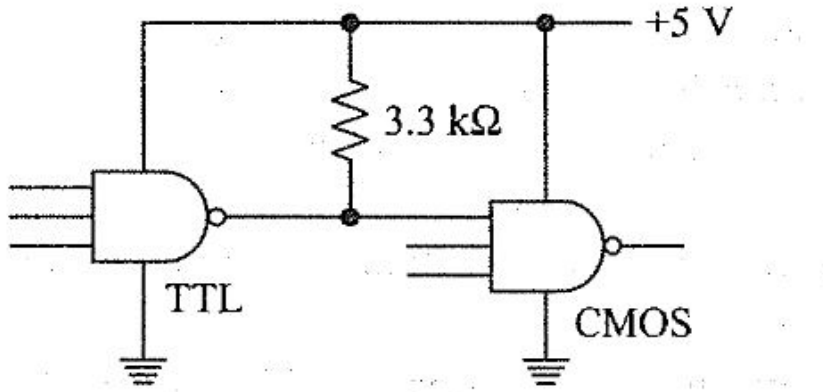


Figure: a) TTL output profile
b) CMOS input profile

- When TTL output is low, the lower end of the 3.3 kΩ is grounded. Therefore, the TTL driver sinks a current of roughly I = (5 V/3.3 kΩ) = 1.52 mA.
- When TTL output is high, the output voltage is pulled up to +5 V
- In worst case, $I_{OL, max}$ = 16 mA and supply voltage can be as high as 5.25 V, so minimum resistance is
- R_{min} = (5.25 V/16 mA) = 328Ω
- The standard value is 330 Ω → use this if switching speed is critical.
- In many application, a pull-up resistance of 3.3 kΩ is fine.



Different supply voltage

- CMOS performance deteriorates at lower voltages because the propagation delay time increases and the noise immunity decreases.
- So, CMOS devices is better to run with supply voltage between 9 and 12 V.

- When TTL output is low, the supply voltage is pulled to ground with I_{sink} = (12 V/6.8 kΩ) = 1.76 mA.
- When TTL output is high, the open-collector rises passively to +12 V; this produces slower switching action than before.
- For instance, with gate capacitance of 10 pF, the pull-up time is RC = (6.8 kΩ) (10pF) = 68 ns.
- If this is a problem , reducing pull up resistor to its minimum allowable value of

  R_{min} = (12 V) / (16 mA) = 750 ohm

  Pull-up time constant decrease to RC = (750 Ω) (10 pF) = 7.5 ns

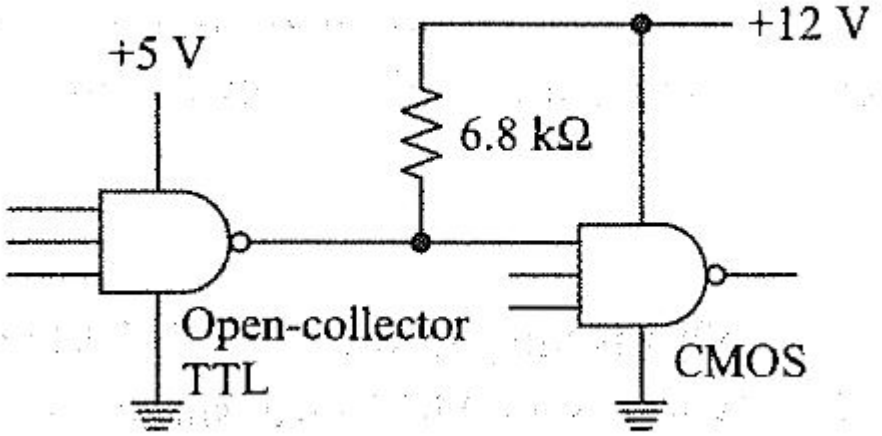


Figure: open-collector TTL driver allows higher CMOS supply voltage

CMOS Level Shifter

- The input stage of the chip uses a supply voltage of +5V, while the output stage uses +12 V. In other words, the input stage interfaces with TTL, and the output stage interfaces with CMOS.

- A standard TTL device drives the level shifter, producing active TTL pull up to at least +2.4 V. the voltage can be pull up beyond this, causing valid high-state input to the level shifter.
- Since, the output of the level shifter connects to +12 V, it has better propagation delay time and noise immunity. Due to this, level shifter is used between TTL driver and CMOS load.

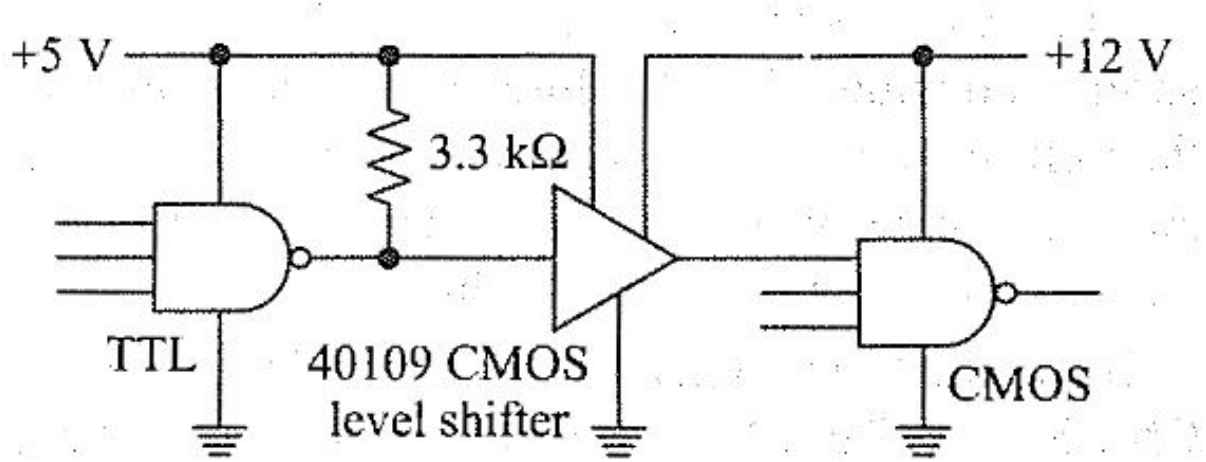


Figure: CMOS level shifter allows the use of 5-V and 12-V supplies

CMOS-To-TTL-Interface

- We have to make sure that the CMOS low-state output is always less than 0.8 V, the maximum allowable TTL low-state input voltage.
- Also, the CMOS high-state output must always be greater than 2 V, the minimum allowable TTL high-state input voltage.

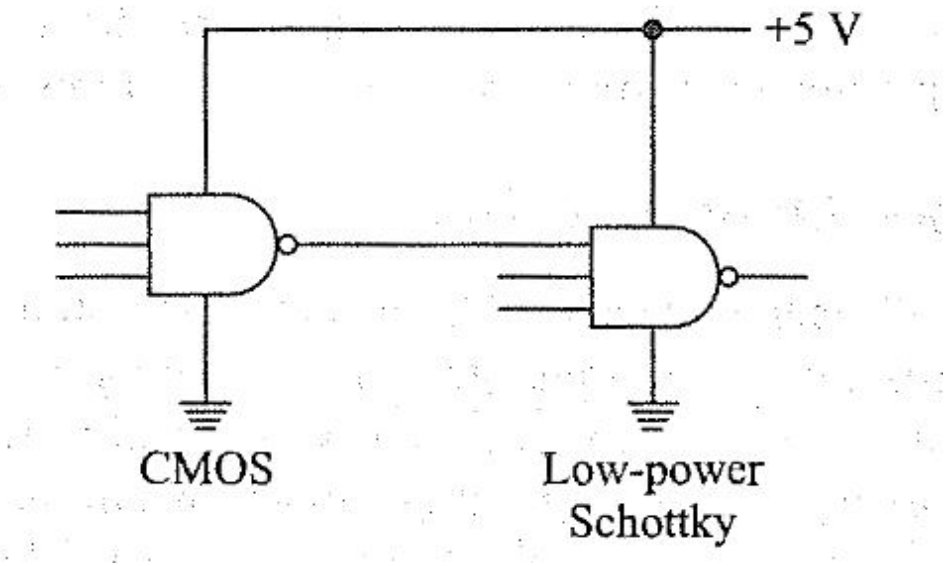


Figure: CMOS driver and low power Schottky TTL Load

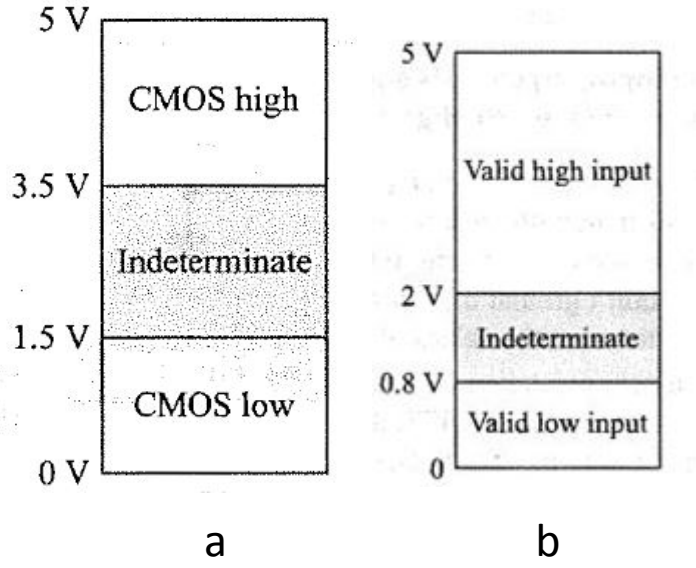
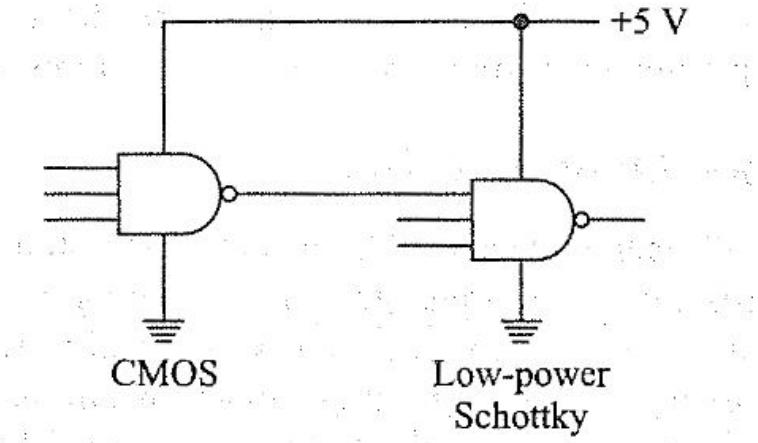


Figure: a) CMOS input profile b) TTL input profile

Supply Voltage at 5 V

- Use +5 V as the supply voltage for the driver and the load
- Low power Schottky device has the worst-case input currents:
- $I_{IL,max}$=-360 µA $_{ILH,max}$ = 20 µA
- Worst case-output currents for CMOS driving TTL:
- $I_{OL,max}$ = 360 µA $I_{OH,max}$ = -360 µA
- This tells us that a CMOS driver can sink 360 µA in the low state, exactly the input current for a low-power Schottky TTL devices. On the other hand, the CMOS driver can source 360 µA, which is more than enough to handle the high-state input current (only 20 µA). So the sink current limits the CMOS/TTL fanout to 1.



Using CMOS Buffer

- The CMOS driver now directly connects to a CMOS buffer, ac a chip with larger output currents. For instance, a 74C902 is a hex buffer, or six CMOS buffers in a single package. Each buffer has the worst-case output currents: $I_{OL,max}$ = 3.6 mA µA $I_{OH,max}$ = 800 µA
- Since a standard TTL load has a low-state input current of 1.6 mA and a high-state input current of 40 µA, a 74C902 can drive two standard TTL Loads. So the CMOS/TTL fanout is 2

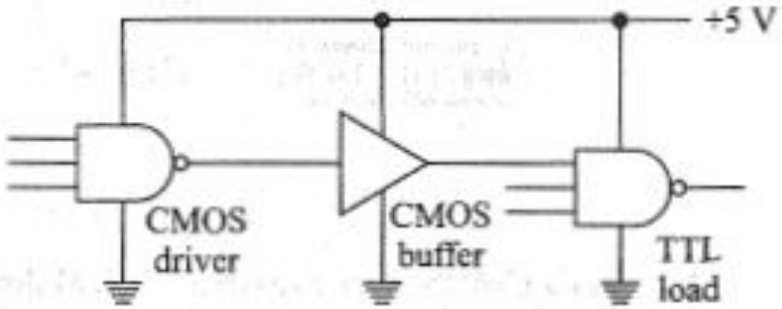


Figure: CMOS buffer can drive standard TTL load

Different supply voltage

- CMOS buffer like 74C902 can use a supply voltage of 3 to 15 V and an input voltage of -0.3 to 15 V.
- The input voltage can be greater than the supply voltage without damaging the device. For instance, a high-state input of +12 V can be used even though the supply voltage is only +5 V.

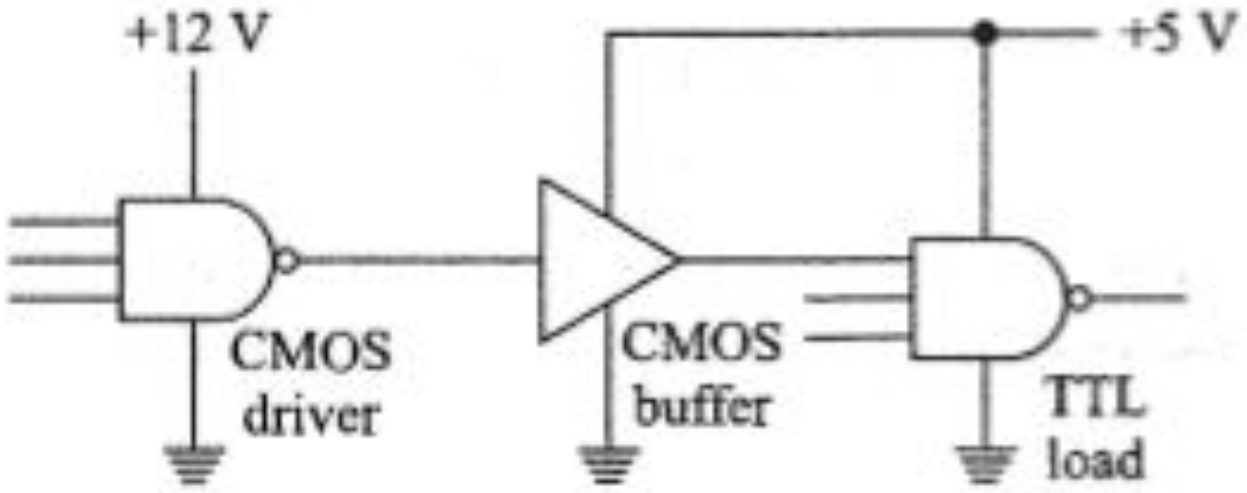


Figure: CMOS driver runs better with 12-V supply

Open-Drain Interface

- Open-drain devices have an output stage consisting only of sink MOSFET. 74C906 is a hex open-drain buffer.
- CMOS driver and CMOS buffer run off +12 V, except for the open-drain output which provides the TTL interface.

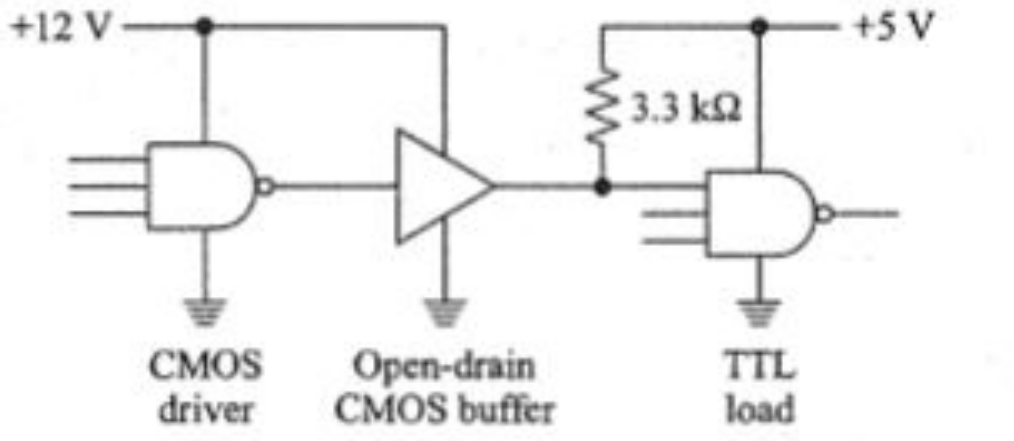


Figure: Open-drain CMOS buffer increases sink current.