Asynchronous Sequential Circuit

Introduction

- Asynchronous sequential circuit, also called Event Driven Circuit does not have any clock to trigger change of state.
- States changes are triggered by change in input signal i.e. the Circuit behavior is determined by signals at any instant in time and the order in which input signals change.

Where we use Asynchronous sequential circuits??

- These are used when speed of operation is important. As they are independent of internal clock pulse, they are operate quickly. so they are used in Quick response circuits.
- Used in the communication between two units having their own independent clocks.
- Used when we require the better external input handling.

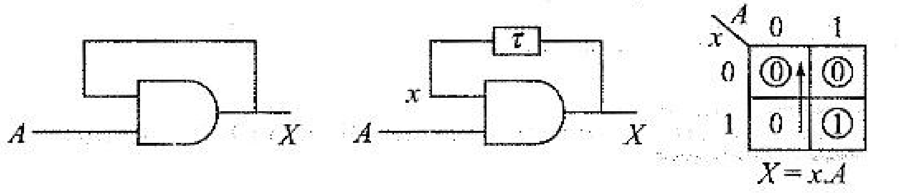
DRAWBACKS:

- Asynchronous sequential circuits are more difficult to design.
- Though they have a faster performance, their output is uncertain

Analysis of Asynchronous Sequential Circuit

AND Gate

- The two input AND gate with output feedback as one input is shown figure (a).
- The circuit is redrawn as shown in figure (b) that includes the effect of propagation delay of the gate say (τ), the finite time after which gate reacts to input.
- Thus, if X is current output obtained following logic relation and x is the feedback output we write, x=X(t-τ).
- In the given truth table (state table), encircled state indicate stable conditions of the circuit.



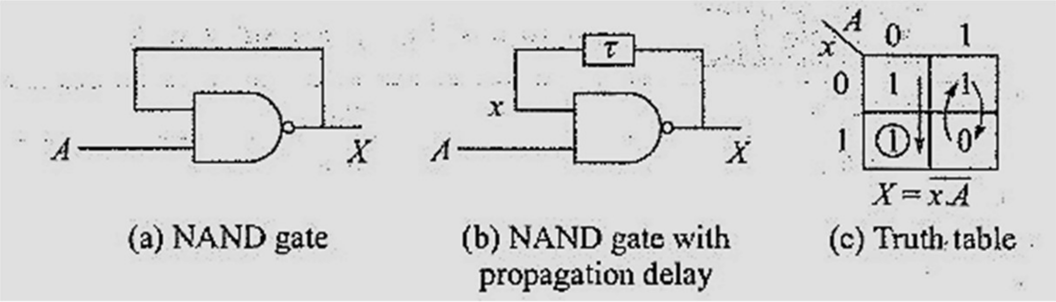
x \ A	0	1
0	⓪	⓪
1	0	①

(a) AND gate (b) AND gate with propagation delay (c) Truth table

- For any state, if $x=X$ then the circuit is stable and if $x \neq X$, if is unstable

NAND Gate

- For A=1 there is no stable state and x=X’ for both x=0 and x=1. Thus there is oscillation between x=0 and A=1 and x=1 and A=1 state.



(a) NAND gate

(b) NAND gate with propagation delay

x \ A	0	1
0	1	1
1	1	0

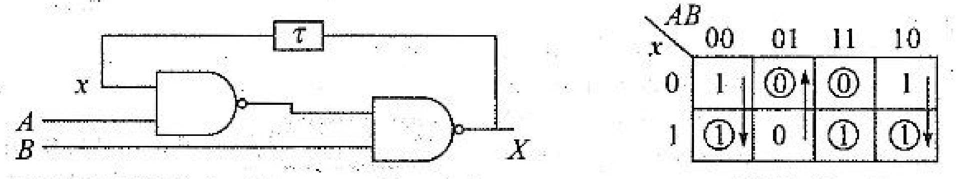
$X = \overline{xA}$

(c) Truth table

Figure: Two input NAND gate with output feedback

Two Input NAND Latch

- Constraint to be followed in asynchronous circuit:
- Though there can be more than one input feeding the circuit, *at a time only one input variable can change*. The other input can change only when the circuit is stabilized following the previous input change. The time required the circuit is in the order of propagation delay of gate i.e. in nanosecond order.
- Similarly, if there are two or more output variables *only one output variable can change at any time instant*, as propagation delays in different paths are different.



(a) NAND latch with propagation delay

x \ AB	00	01	11	10
0	1 ↓	⓪ ↑	⓪	1 ↓
1	①	0	①	①

(b) Truth table

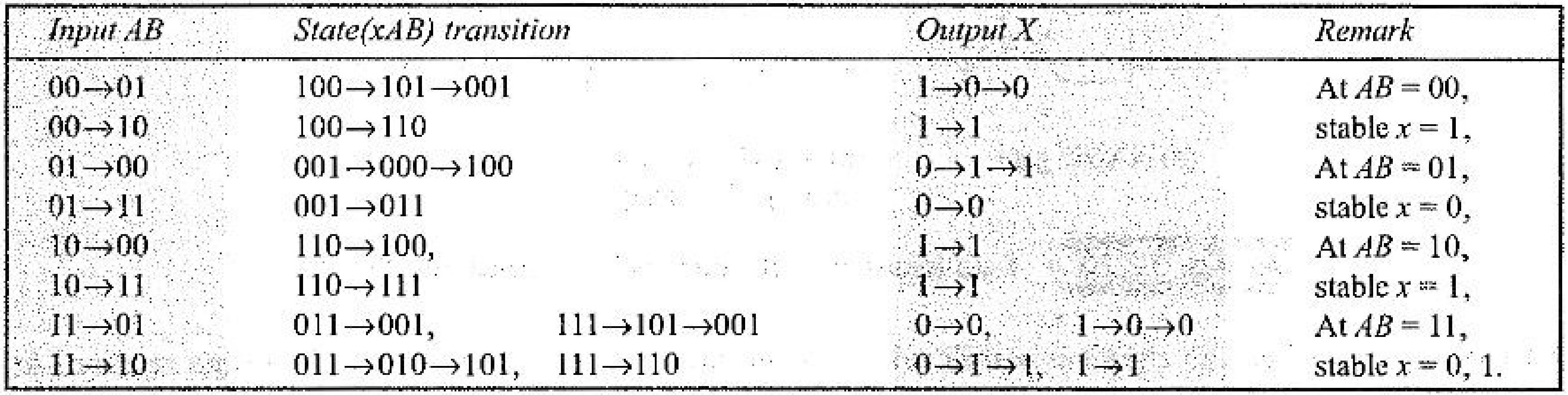
- ➢ for any given combination of x, a, B if X=x, the circuit is stable otherwise not. Stable states are encircled and arrows show the movements from the transient states,

Figure: Two input NAND Latch

For each input combination the circuit has at least one stable state and this stable state will be the starting point of our discussion in each case.

- **Input AB change from 00 to 01**: The circuit move from xAB=100, a stable position to xAB=101 which is unstable then moves to xAB=001, a stable sate that has output 0. therefore, a 00→01 transition in AB has output X making 1→0 transitions.
- **Input AB changes from 00 to 10**: the circuit from xAB=100, a stable position to xAB=110, another stable state has output 1. therefore, a 00→10 transition in AB does not alter the value of output X=1.
- Note that AB cannot change from 00 to 11 as there will be finite delay. Thus, the transition path of AB is either 00 →01→11 (then output changes as 1→0→0) or 00→10→11 (output changes as 1→1→1) depending upon on which A or B changes earlier. Therefore, output is 0 or 1 depending upon intermediate value and in asynchronous design such transitions are not allowed.

Transition Table of NAND Latch



Input AB	*State(xAB) transition*	*Output X*	*Remark*
00→01	100→101→001	1→0→0	At $AB = 00$,
00→10	100→110	1→1	stable $x = 1$,
01→00	001→000→100	0→1→1	At $AB = 01$,
01→11	001→011	0→0	stable $x = 0$,
10→00	110→100,	1→1	At $AB = 10$,
10→11	110→111	1→1	stable $x = 1$,
11→01	011→001, 111→101→001	0→0, 1→0→0	At $AB = 11$,
11→10	011→010→101, 111→110	0→1→1, 1→1	stable $x = 0, 1$.

Analyze the given Mealy Model asynchronous sequential circuit

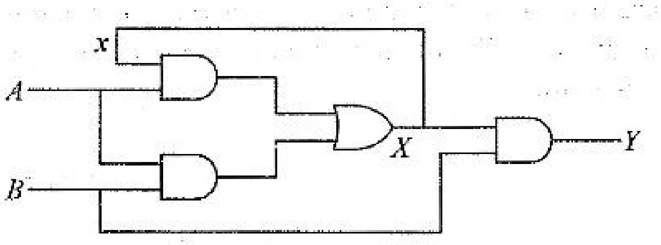
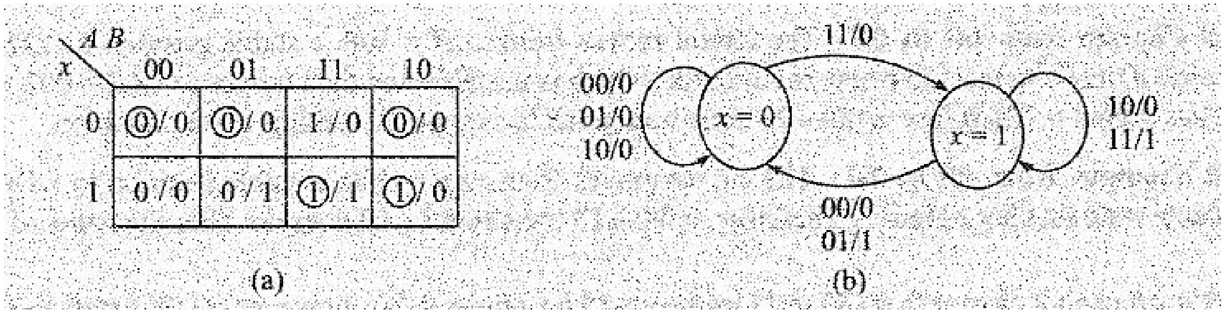


Figure: An asynchronous sequential circuit: Mealy model

- Consider x=X(t-τ) where τ is the cumulative propagation delay from input side up to X.
- Stable states are encircles when X=x.
- Two stable sates x=0 and x=1.
- For all possible combination of xAB we get X and Y following logic relation shown in the circuit.
- Prepare k-map and state diagram.



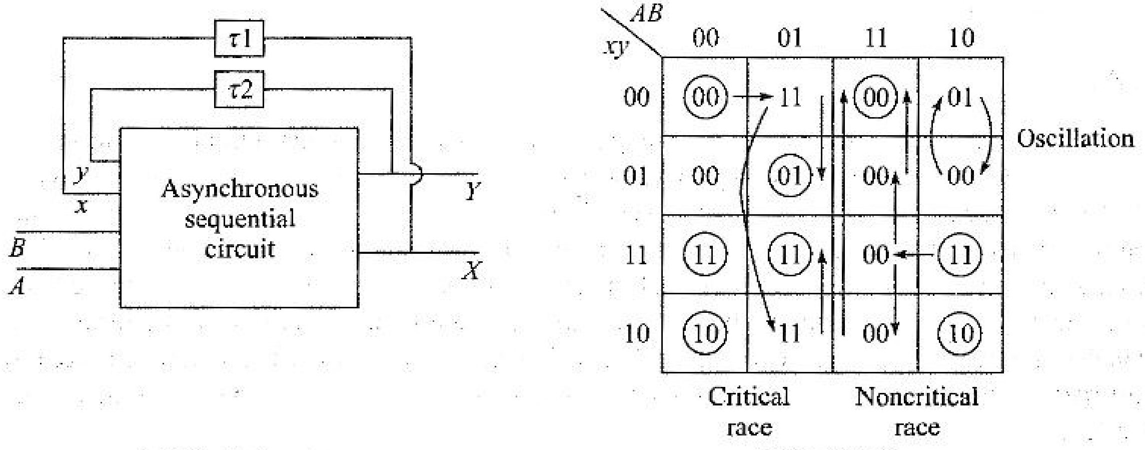
x \ AB	00	01	11	10
0	0/0	0/0	1/0	0/0
1	0/0	0/1	1/1	1/0

a) Karnaugh map, b) state diagram for asynchronous circuit given

Problems with Asynchronous Sequential Circuits

- Oscillation
- Critical race
- Hazards

- Consider an asynchronous sequential circuit with two inputs A and B and two outputs, X and Y.
- Both the outputs are fed back to the input side in the form of x and y but with different propagation delays. Thus x and y cannot change simultaneously but with time delays τ1 and τ2 respectively and we can write x=X(t-τ1) and y=Y(t-τ2).
- The stable states are encircled in the circuit where xy=XY. But there are certain major problems with this truth table.



xy \ AB	00	01	11	10
00	00	11	00	01
01	00	01	00	00
11	11	11	00	11
10	10	11	00	10

(a) Block diagram

(b) Truth table

Figure: Block diagram and truth table of 2 input , 2 outputs asynchronous circuit

Oscillation

- Consider, the stable state xyAB=0000, where x=X and y=Y. if the input AB changes from 00 to 10, the circuit goes to xyAB=0010 state and then output XY=01. This is transient because xy$\neq XY$. After time τ2, y take the value of Y=1 and the circuit goes to xyAB=0110 where output XY=00. This again is transient state and after another propagation delay of τ2, the circuit goes through xyAB=0010. thus the circuit oscillates between state 0010 and 0110 and the output Y oscillates between 0 an 1 with time gap τ2. In asynchronous sequential circuits for any given input, transitions between two unstable states like these are to be avoided to remove oscillation.

Critical Race

- This occurs when an input change tries to modify more than one output.
- Consider stable state xyAB=0000.Now, if AB changes to 01 the circuit moves to xyAB=0001 where XY=11. Now depending which of τ1 and τ2 is lower, xy moves from 00 to either 01 and 10.
- If τ1 is lower, x changes earlier and the circuit goes to xyAB=1001 which is a unstable state with output XY=11. the circuit next moves to state xyAB=1101 which is a stable state and final output is XY=11.
- If τ2 is lower, y changes earlier and the circuit goes to xyAB=010, a stable state and final output is 01.
- Thus, depending upon on propagation delays in feedback path, the circuit settles at two different states generating two different set of outputs. Such a situation is called critical race condition and is to be avoided in asynchronous sequential circuit.

- Race can be non-critical too, in which case its presence does not pose any problem for the circuit behavior.
- Consider stable state xyAB=1110. if the input AB changes to 11, the circuit goes to xyAB=1111 where output XY=00.
- Again depending of propagation delays xy becomes either 01 and 10. if xy=01, then the circuit moves to xyAB=0111 and then to 0011 and settles there. If xy=10 then the transition path is 1111→1011→0011.
- In both cases final state is 0011 and output is 00.
- Since, the race condition does not lead to two different state it is termed as non-critical race.

Hazards

- Static and dynamic hazards causes malfunctioning of asynchronous sequential circuit.
- Situations like Y=A+A’ and Y=AA’ are to be avoided for any input output combination with the help of hazards covers in truth table.
- Other problem →essential hazards→ occurs when change in input does not reach one part of the circuit while from other part one output fed back to the input side becomes available→avoided by adding delay, by adding gates that does not change the logic level, in the feedback path.

Design of asynchronous sequential circuit

The problem:

- A digital logic circuit is to be designed that has two inputs A, B and one output X. X goes high if at A=1, B makes a transitions 1→0. X remains high as long as this A=1, B=0 are maintained. If any of A or B changes at this time output X goes low. It becomes high again when at A=1, B goes from 1 to 0.
- Solution

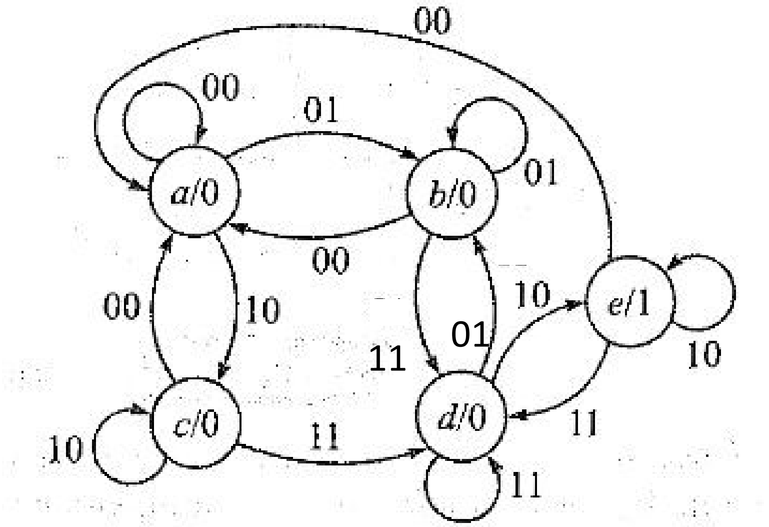
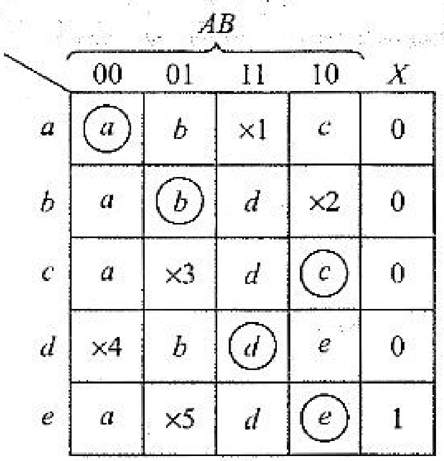


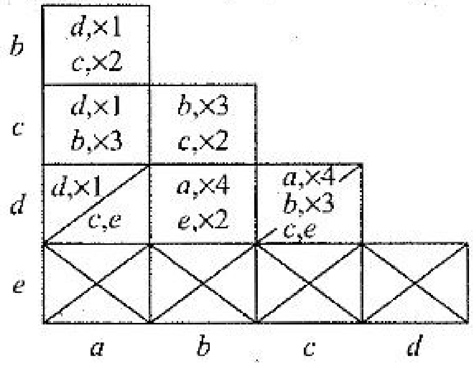
Figure: State diagram of the problem using Moore model

- Primitive table or primitive flow table or flow table



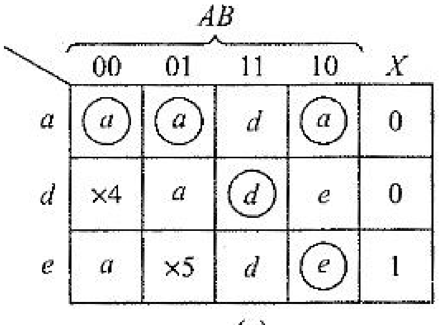
	AB 00	01	11	10	X
a	ⓐ	b	×1	c	0
b	a	ⓑ	d	×2	0
c	a	×3	d	ⓒ	0
d	×4	b	ⓓ	e	0
e	a	×5	d	ⓔ	1

State Reduction using implicant table



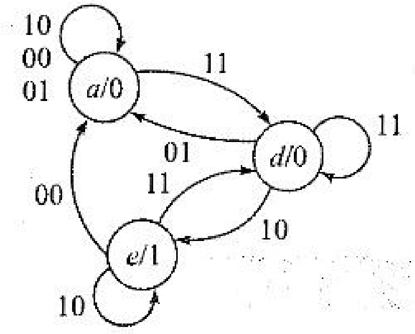
b	d,×1 c,×2			
c	d,×1 b,×3	b,×3 c,×2		
d	d,×1 c,e	a,×4 e,×2	a,×4 b,×3 c,e	
e	☒	☒	☒	☒
	a	b	c	d

Reduced state table and state transition diagram



	AB 00	01	11	10	X
a	ⓐ	ⓐ	d	ⓐ	0
d	×4	a	ⓓ	e	0
e	a	×5	d	ⓔ	1

(a)

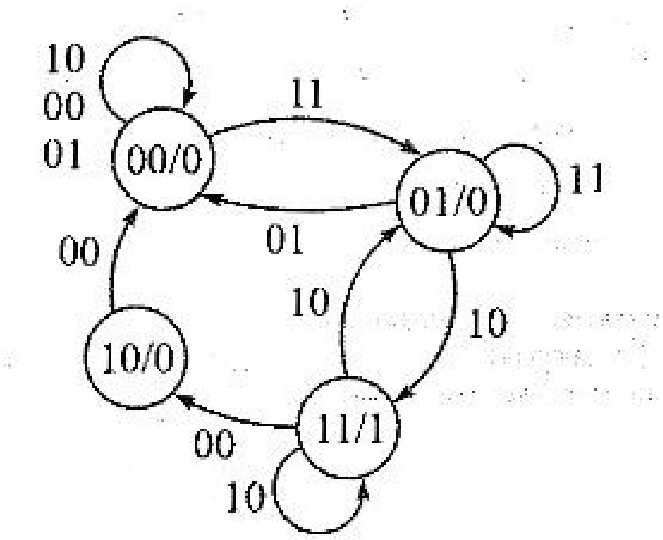


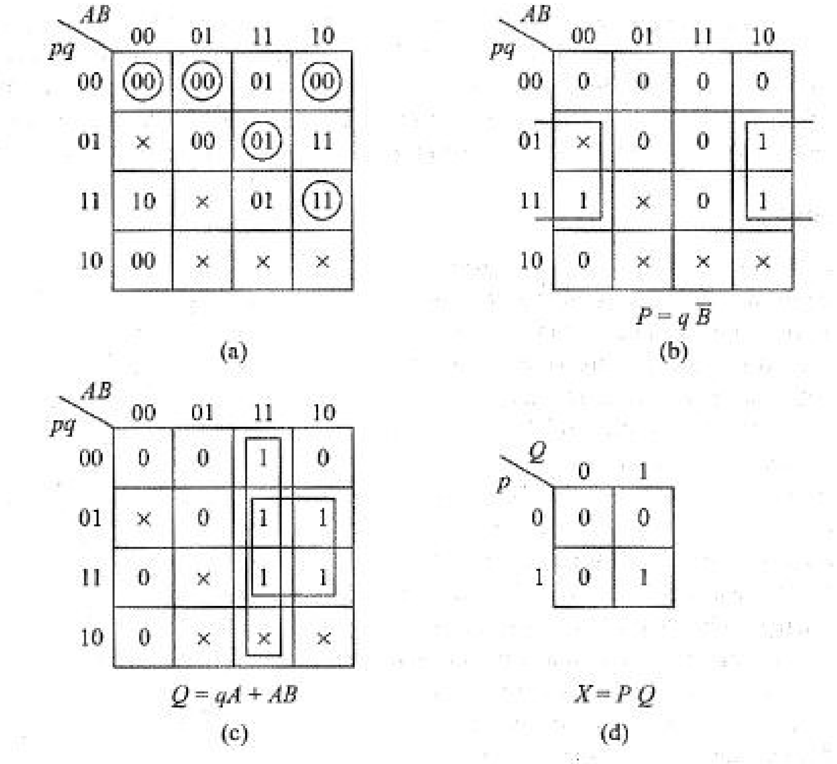
(b)

State assignment

- a:00
- d:01
- e:11
- Ø : 10 →dummy state

Modified state transition diagram





pq \ AB	00	01	11	10
00	00	00	01	00
01	×	00	01	11
11	10	×	01	11
10	00	×	×	×

(a)

pq \ AB	00	01	11	10
00	0	0	0	0
01	×	0	0	1
11	1	×	0	1
10	0	×	×	×

$P = q\overline{B}$

(b)

pq \ AB	00	01	11	10
00	0	0	1	0
01	×	0	1	1
11	0	×	1	1
10	0	×	×	×

$Q = qA + AB$

(c)

p \ Q	0	1
0	0	0
1	0	1

$X = P\,Q$

(d)

a) Reduced state diagram b) to d) k-map and design equations

- We represent state variable by P and Q, the corresponding feedback variables are represented by p and q respectively.
- We use Karnaugh map to get expression of sate variables P and Q as a function of input A, B and feedback variables p and q.
- The equation of output is generated from P and Q

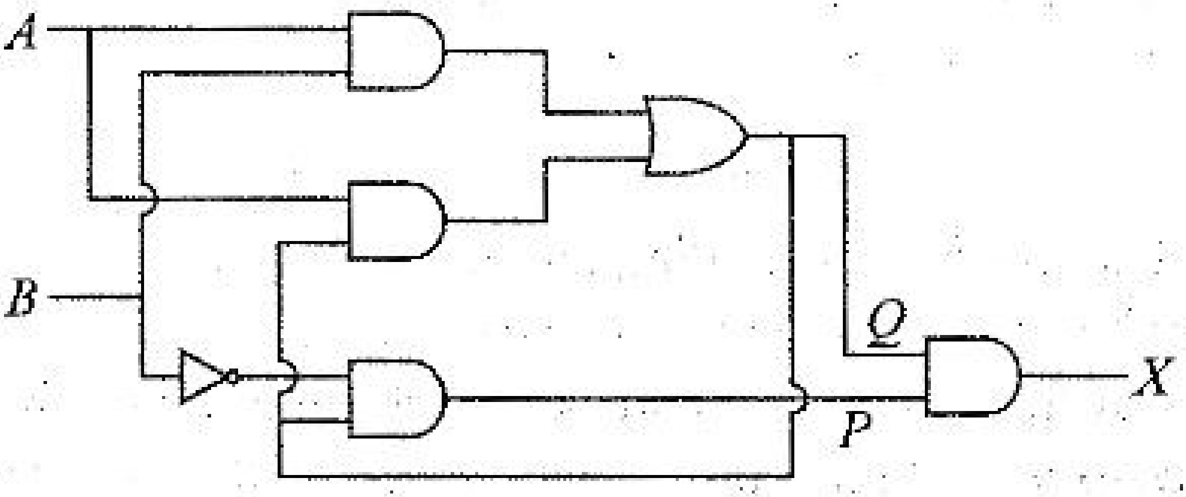


Figure: Circuit diagram of given problem