# Static and Dynamic Hazards

**Static-1 Hazard**

- This type of hazard occurs when *Y = A + A'* type of situation appears for a logic circuit for certain combination of other inputs and A makes a transition 1 → 0.
- An A+A' condition should always generate 1 at the output, i.e. static-1.
- But the NOT gate output takes finite time to become 1 following 1→0 transition of A.
- Thus for the OR gate there are two zeros appearing at its input for that small duration, resulting a 0 at its output. The width of this zero is in nanosecond order and is called a glitch.
- For combinational circuit, it may go unnoticed but in sequential circuit, more particularly in asynchronous sequential circuit it may cause major malfunctioning.

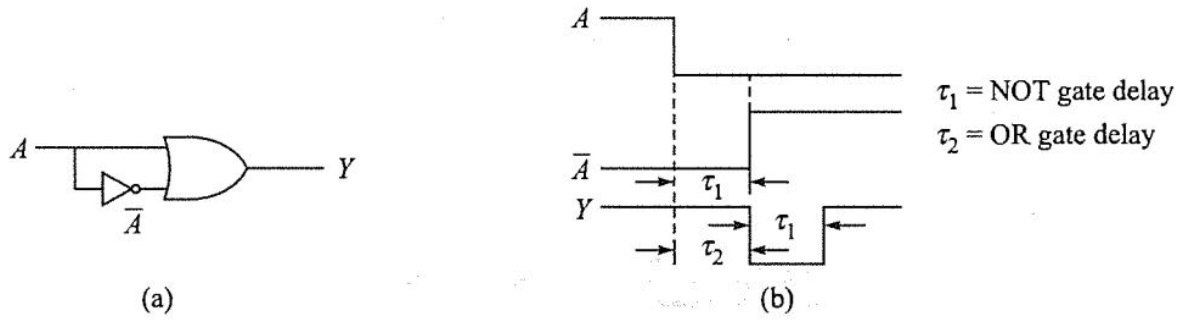


**Figure**: Static-1 Hazard

Solution to Static-1 Hazard

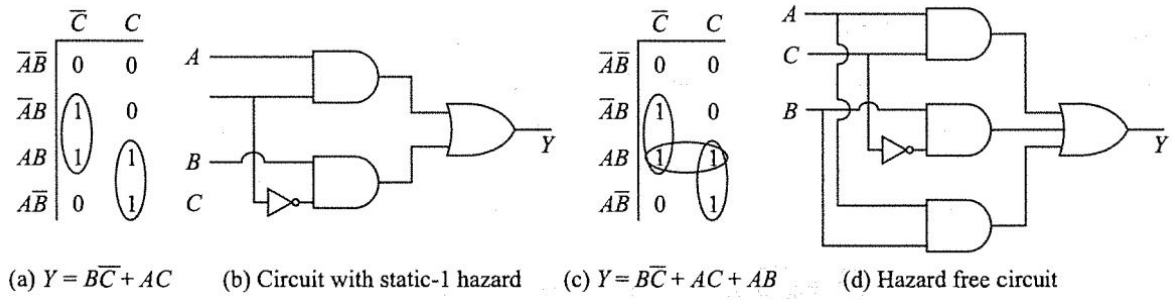


**Figure**: Static-1 hazard and its cover

- In the figure above (b) , when B =1, and A = 1, and then C makes transition 1→0, it produces glitch (satic-1 hazard).
- Consider another grouping as in figure (c), it includes one additional term AB.
- This corresponding circuit though require more hardware than minimal representation, is hazard free.
- The additional term AB ensures Y = 1 for A=1 and B=1 through the third input of final OR gate and a 1→0 transition at C does not affect output.

Again, a NAND gate with A and A' connected at its input for certain input combination will give static-1 hazard when A makes transition 0→1 and require hazard cover.

**Static-0 Hazard**

- This type of hazard occurs when *Y = A.A'* kind of situation occurs in a logic circuit for certain combination of other inputs and A makes a transition 0→1.
- An A.A' condition should always generate Oat the output, i.e. static-0.
- But the NOT gate output (Fig. below (a) ) takes finite time to become 0 following a 0→ 1 transition of A.
- Thus for final AND gate there are two ones appearing at its input for a small duration resulting a 1 at its output (Fig below b). T
- This Y= 1 occurs for a very small duration (few nanosecond) but may cause malfunctioning of sequential circuit.

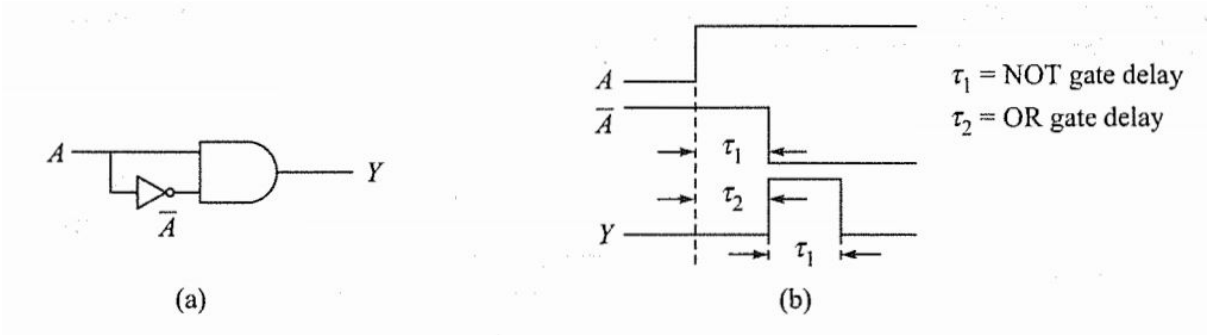


**Figure**: Static-0 Hazard

Solution to Static-0 Hazard

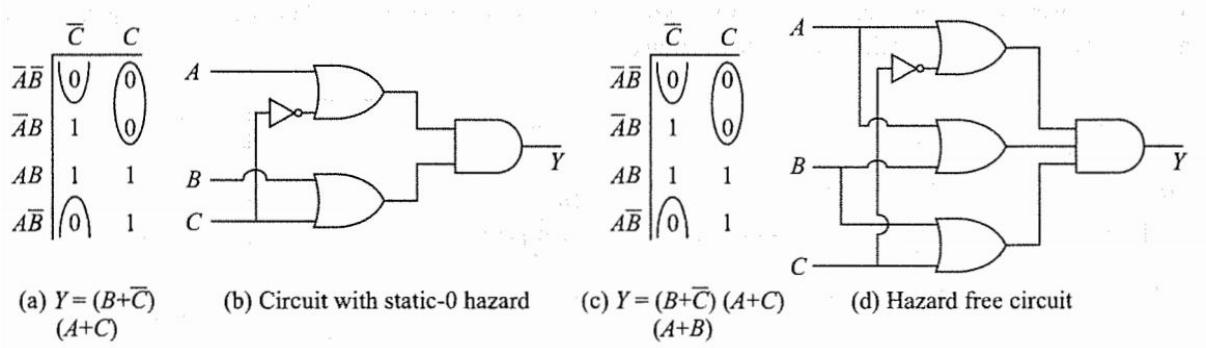


**Figure**: Static-0 and its cover

- If figure above , if B=0, A=0 and C makes transition 0→1, there will be static-0 hazard occurring at the output.
- To prevent this, we add one additional group, i.e. one more sum term (A+B) an shown in figure above d.
- The additional term (A+B) ensures Y=0 for A=0, B=0 through the third input of final AND gate and a 0→1 transition at C does not affect output.

Also, a NOR gate with A and A' connected at its input for certain input combination will give static-0 hazard when A makes a transition 1→0 and require hazard cover.

**Dynamic Hazard**

- Dynamic hazard occurs when circuit output makes multiple transitions before it settles to a final value while the logic equation asks only for one transition.
- An output transition designed as 1→0 may give 1→0→1→0 when such hazard occurs and a 0→ 1 can behave like 0→1→0→1.
- The output of logic equation in dynamic hazard degenerates into Y = A +A'A or Y = (A+A').A kind of relations for certain combinations of the other input variables. This occur in multilevel circuits having implicit satic-1 and/or static-0 hazards.