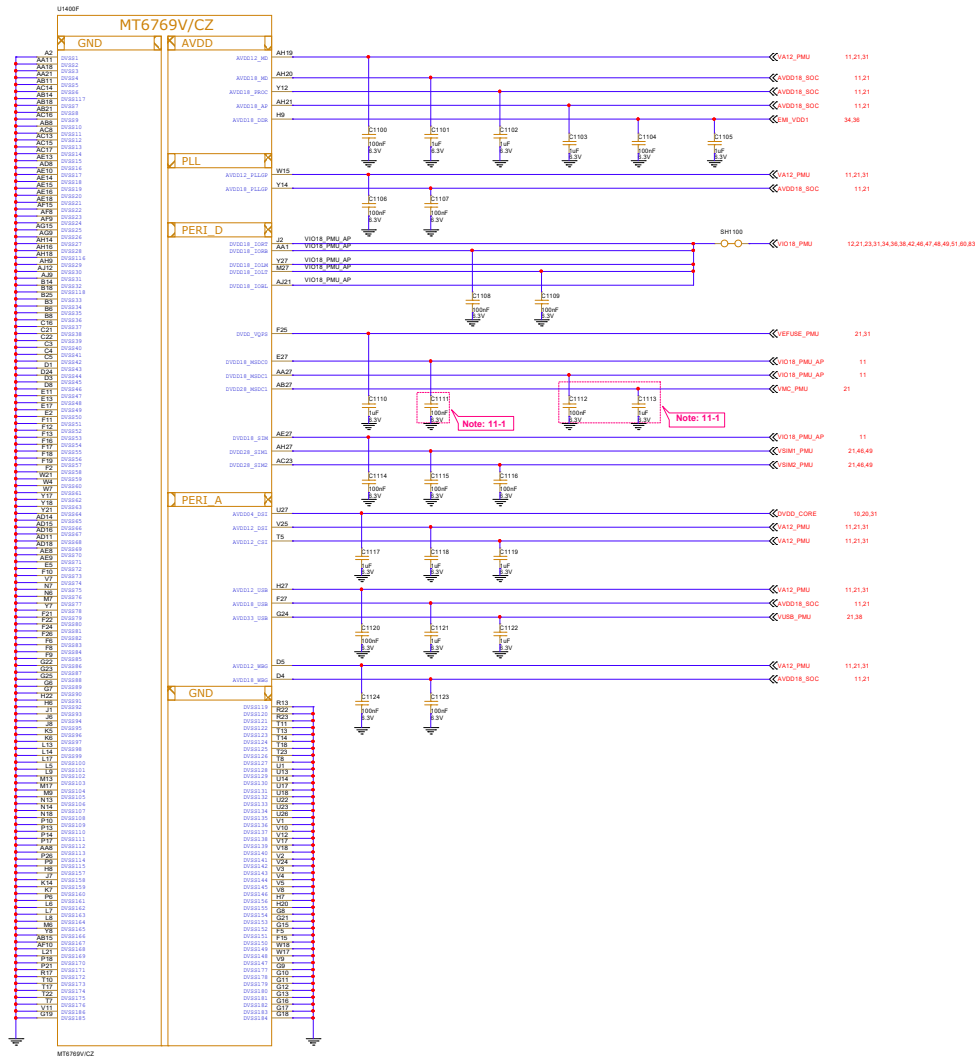


LAMU_MB_DISCRETE_DDR_NOCA_V0D3_0704
1. 变更ICD连接器型号;
2. 删除PD_VDD_VSYS供电兼容(删除R3820);
3. 变更Flicker_I2C, 增加R4825,R4826;
4. ALPS_VDD输入锁定为VSYS;
5. AP增加一组SCP_I2C0(GPIO15/GPIO16);
6. AP删除ANT_ID(GPIO79);
7. T5901,T5902封装变更为DFN1006-2L;

LAMU_MB_DISCRETE_DDR_NOCA_V0D4_0802
1. 删除PD_VCONN对地1K电阻(R3832);
2. B5701,B5702变更为0402封装;
3. R2400变更为短路块SH2401;
4. R2406变更为短路块SH2402;
5. R3600变更为短路块SH2402;
6. 删除R3701,R3721,R3723,R3821,R4602,R4608,R4603;
7. 删除R4607, 增加TP4603;
8. R4634变更为短路块SH4601;
9. R4812,R4813,R4814改短路块;
10. R5402,R5403替换为短路块;
11. R5404,R5405替换为短路块;
12. R2403,R2404变更为短路块;
13. R5301,R5302替换为短路块;
14. 删除R5004,R5008;
15. R4106,R4107,R4114替换为短路块;
16. R4110变更短路块;
17. R4117,R4118,R4119变更为短路块;
18. PA_ADS兼容设计, 增加R4212,R4211

TINNO			
RESCNO		Xingjun.Yu	
TITLE		LAMU_MB	
PAGE		01_CHANGELOG_B0	
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	1 OF 100

TINNO			
DESIGNED		Xingjun Yu	
TITLE		LAMU_MB	
PAGE		02_CHANGELOGT_MF	
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	2 OF 100

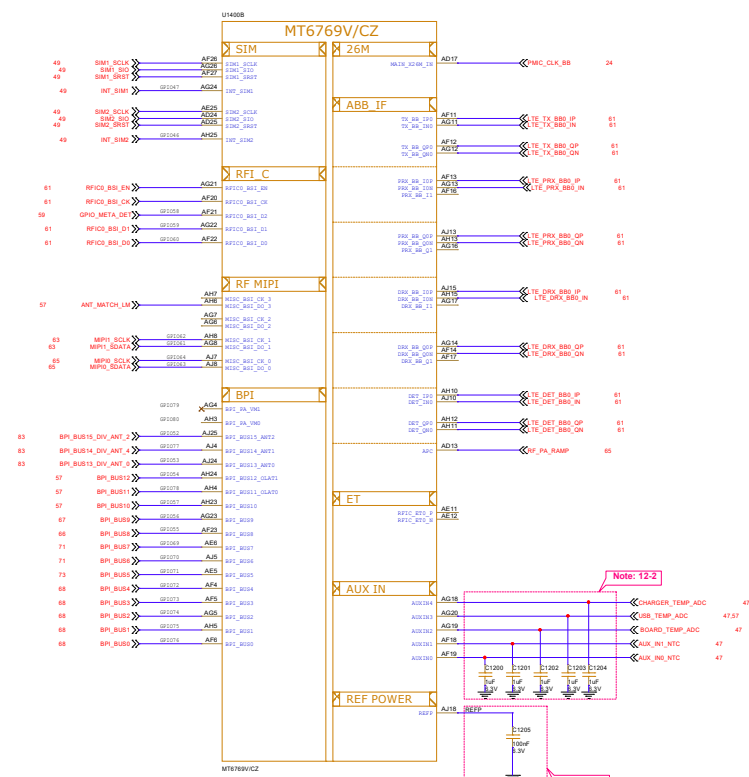
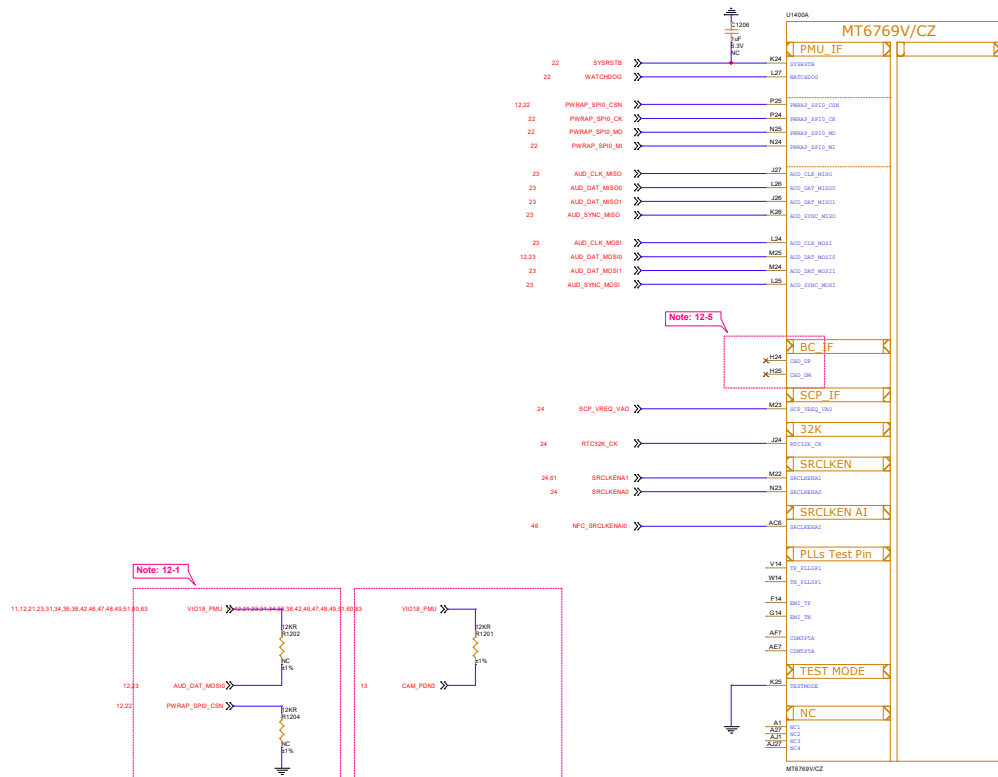


Schematic design notice of '11_BB_POWER_IO' page:

Note 11-1: C1111 closed DVDD18_MSDC0 150ml

Note 11-2: C1112 closed DVDD18_MSDC1 150ml
C1113 closed DVDD28_MSDC1 150ml

TINNO				
REVISION		Xinglan Ye		
TITLE		LAMBDA		
PAGE		11_BB_POWER_IO		
SIZE	D	REV	V1.0	
DATE	Thursday, October 31, 2024	SHEET	11	OF 100



Schematic design notice of "12_BB_1" page:

Note 12-1: PWRAP_SPI0_CSN' and 'AUD_DAT_MOSIO' are bootstrap pins to select which interface will be the JTAG pin out

PWRAP_SPI0_CSN	AUD_DAT_MOSIO	AP JTAG Mode	IO JTAG Mode
H (Default)	L (Default)	N/A	N/A
H	H (by external PU)	SPI0 + EINT8	SPI2 + SPI3
L (by external PD)	L	SPI0 + EINT8	N/A
L (by external PD)	H (by external PU)	N/A	N/A

Note 12-2: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

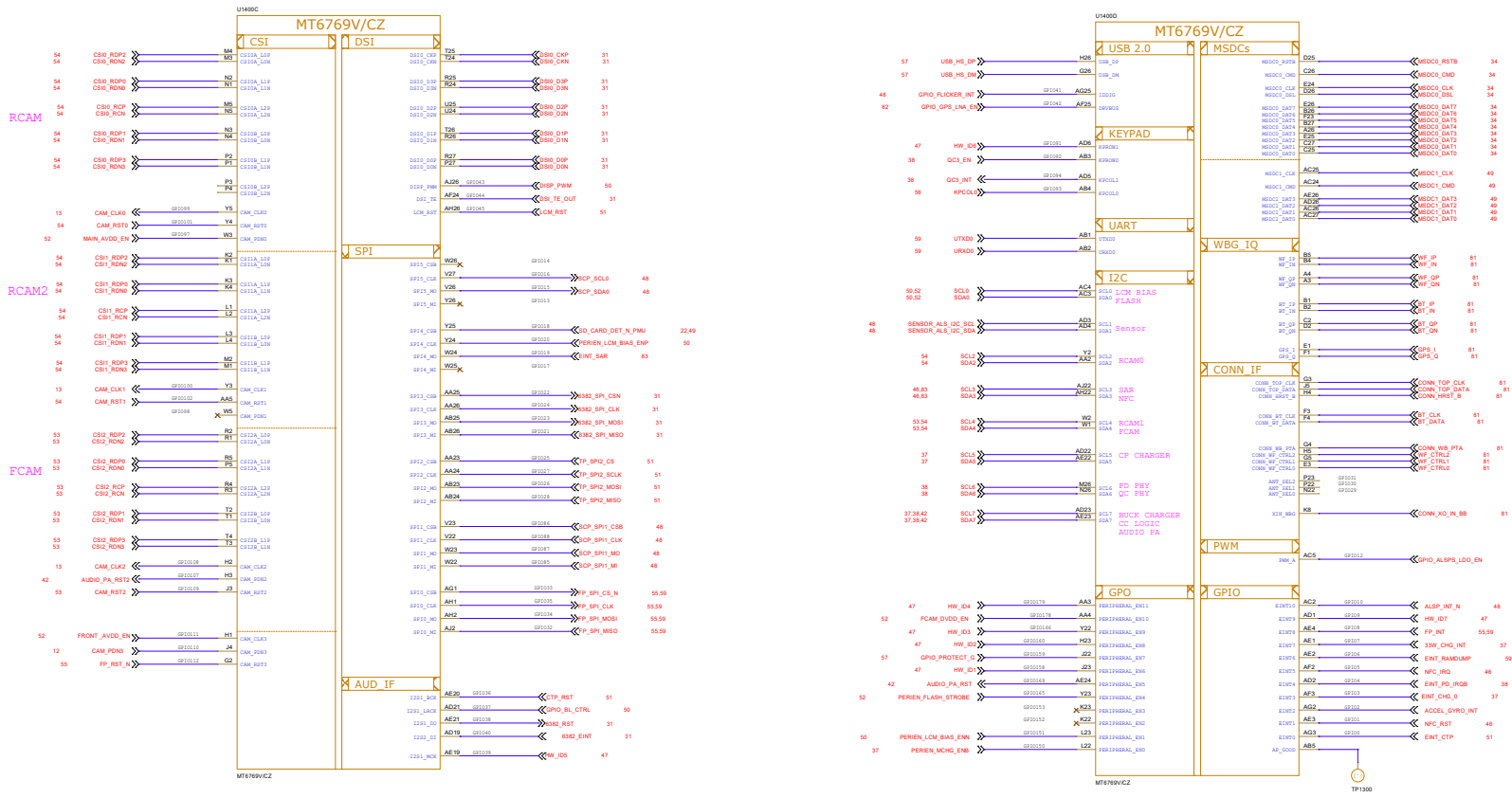
Note 12-3: The de-coupling cap. for REFP (AJ18 ball) have to be placed as close to BB as possible.

Note 12-4: HW pin for DDR type feature in bootstrap (refer to BB HW design Notice)

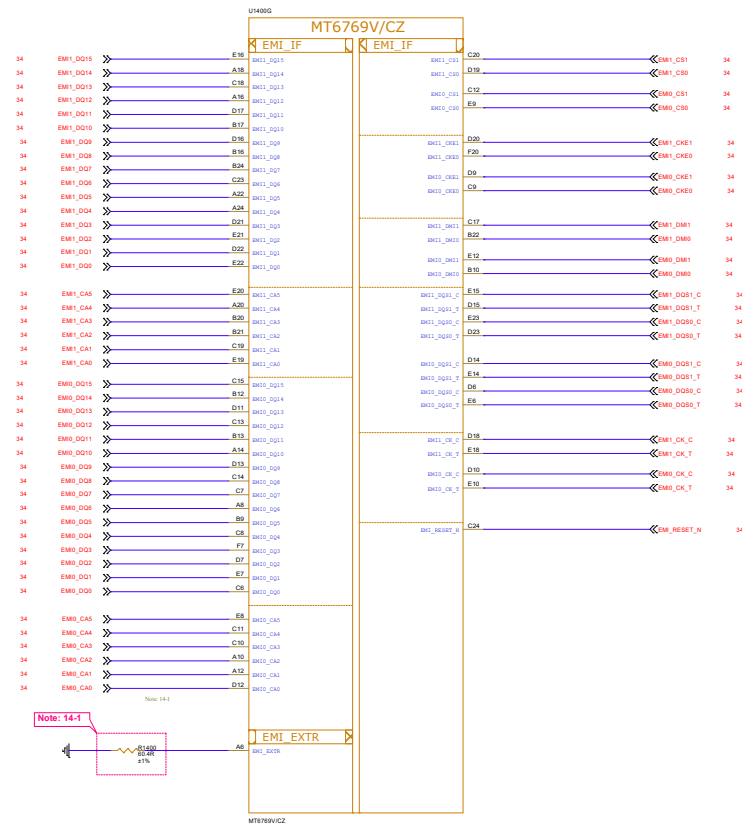
AUD_SYNC_MISO	AUD_CLK_MISO	CAM_PDN3	PMIC 6358 voltage	DDR Type
default=PD	default=PD	default=PD	VDRAM1 / VDRAM2	DDR
No ext. pull	No ext. pull	No ext. pull	1.25v / 0.6v	LP4X eMCP
No ext. pull	12K pull to VIO18	No ext. pull	0v / 1.8v	Reserved
12K pull to VIO18	No ext. pull	No ext. pull	1.25v / 0v	LP3 eMCP
12K pull to VIO18	12K pull to VIO18	No ext. pull	1.25v / 1.8v	Reserved
No ext. pull	No ext. pull	12K pull to VIO18	1.25v / 0.6v	Discrete LP4X

Note 12-5: Charger must have D+/D- pin for charger type USB detection.
Charger must have at least 500mA USB current for All charger type.

TINNO			
DESIGNED	Xingjun Ye		
TITLE	LAMB_M6		
PAGE	12_BB_1		
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	12 OF 100



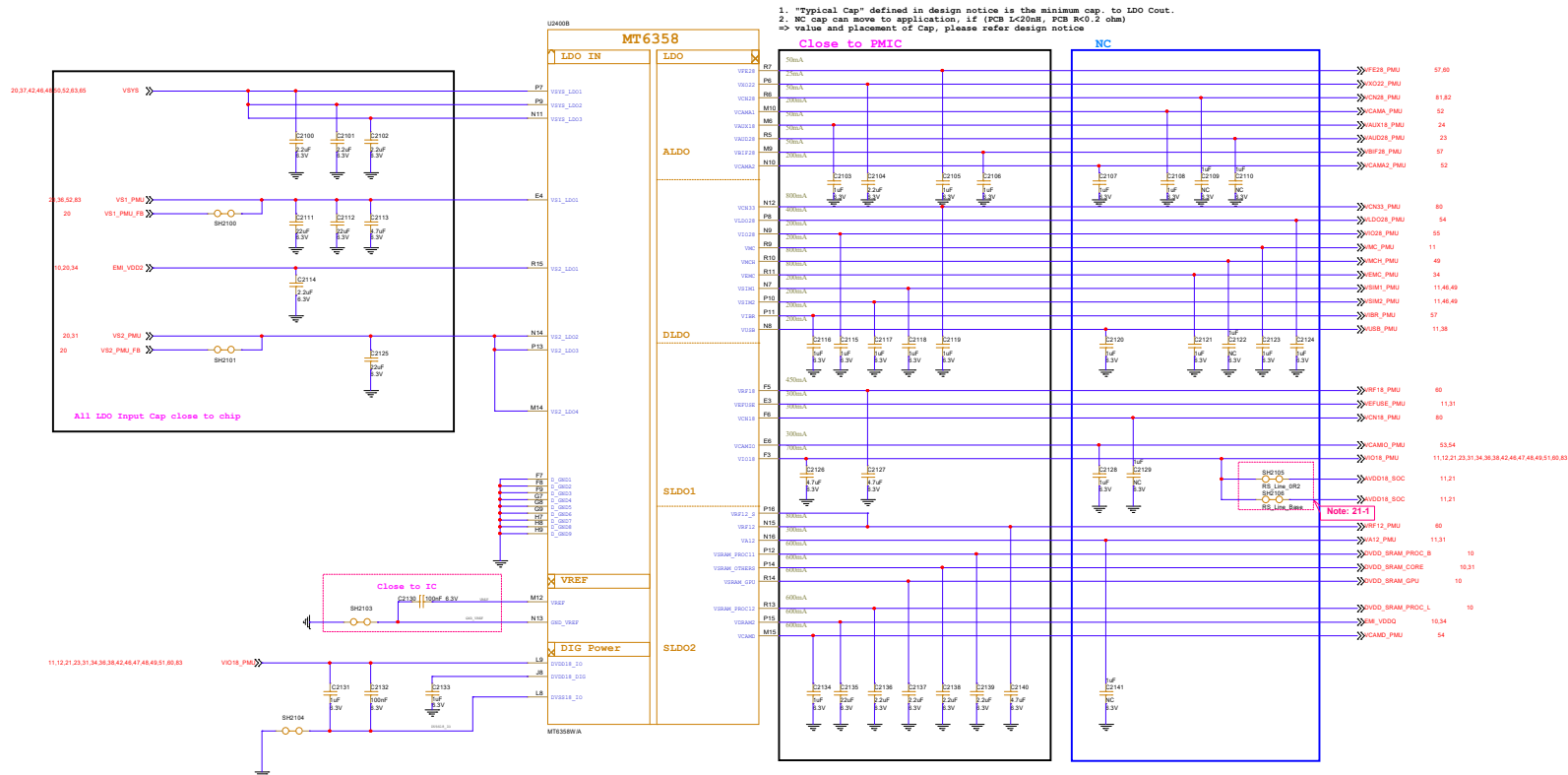
TINNO				
REVISION		Xingjun.Yu		
TITLE		LAMB_LB		
PAGE		13_08_2		
SIZE	0	REV	V1.0	
DATE	Thursday, October 31, 2024	SHEET	13	OF 100



Schematic design notice of '14_BB_3' page.

Note 14-1: R4001 please select 60.4 ohm (1%) resistor

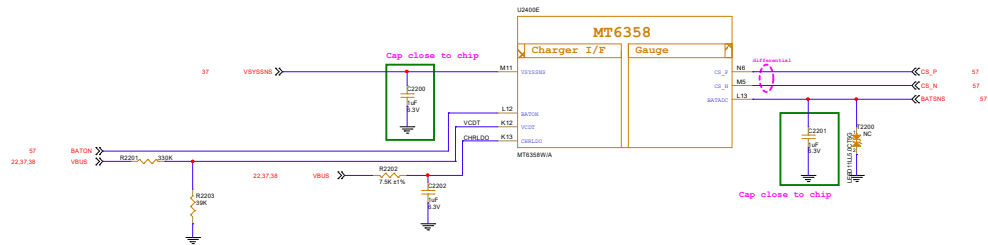
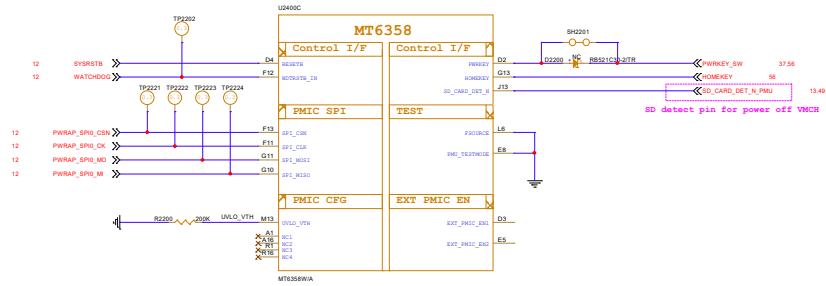
TINNO				
REVISION		Xingjun.Yu		
TITLE		LAMB_M0		
PAGE		14_BB_3		
SIZE	D	REV	V1.0	
DATE	Thursday, October 31, 2024	SHEET	14	OF 100



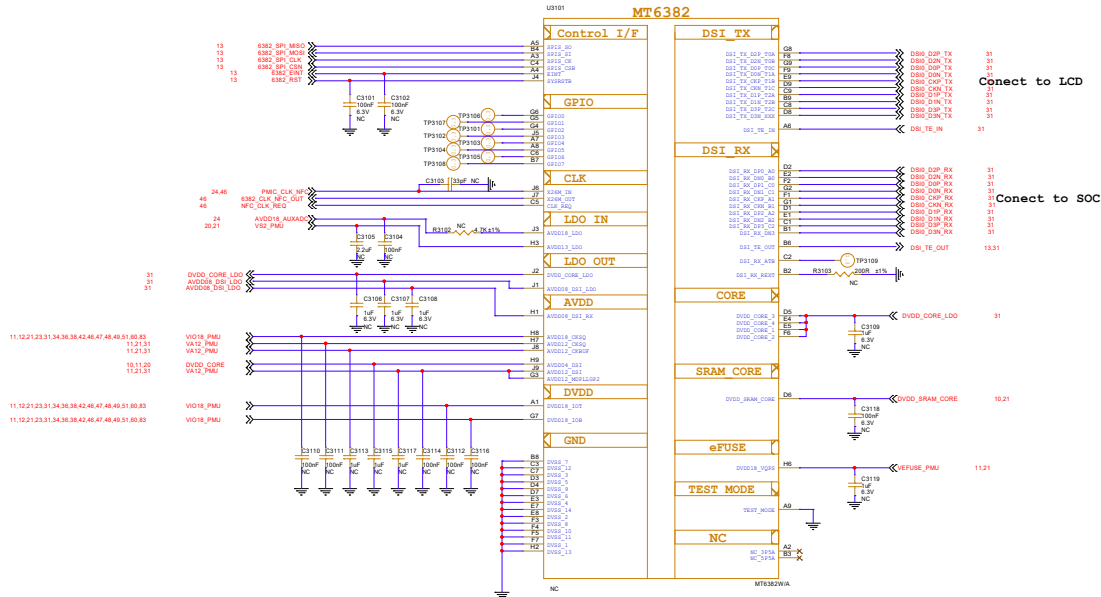
Schematic design notice of "21_POWER_MT6358-LDO" page.

Note 21-1: Please set SH2101 close to C2132, making star connection between VIO18_PMU and AVDD18_SOC near to LDO cap. C2132
 Please also refer to MT6358 design notice for further detail design information

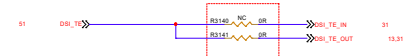
TINNO			
RESCHN2	Xingjun.Yu		
TITLE	LAMB_LB		
PAGE	21_POWER_MT6358-LDO		
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	21 OF 100



TINNO			
DESIGNER	Xingjun.Yu		
TITLE	LAMBDA		
PAGE	22_POWER_MT6358-I/F		
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	22 OF 100



如果使用MT6382，貼R3140；
如果不用MT6382，貼R3141。



MT6382 Power Ball	GR(MT6382)
AVDD08_DS1_LDO (LDO output)	Supply AVDD08_DS1_RX
DVDD_CORE_LDO (LDO output)	Supply DVDD_CORE
DVDD08_DS1_RX	By internal LDO
AVDD08_DS1_RX	By internal LDO
DVDD_SRAM_CORE	DVDD_SRAM_CORE(VSRAM_OTHERS)
DVDD18_IOT	
DVDD18_I08	VI018_PMU
DVDD18_CK5Q	V52_PMU
AVDD12_CK5Q	VA12_PMU
AVDD12_DS1	
AVDD12_MDLIGP2	
AVDD18_LDO	VALM18_PMU
AVDD18_LDO	V52_PMU
AVDD12_CK5Q	VA12_PMU
DVDD18_VQPS	VEFUSE_PMU
AVDD04_DS1	DVDD_CORE(VCORE)
X2M_IN	X2_EXT
X2M_OUT	X

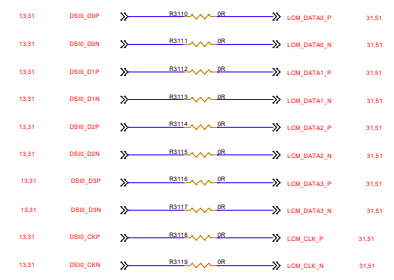
Connect to SOC Connect to 6382 RX



Connect to 6382 TX Connect to EMI

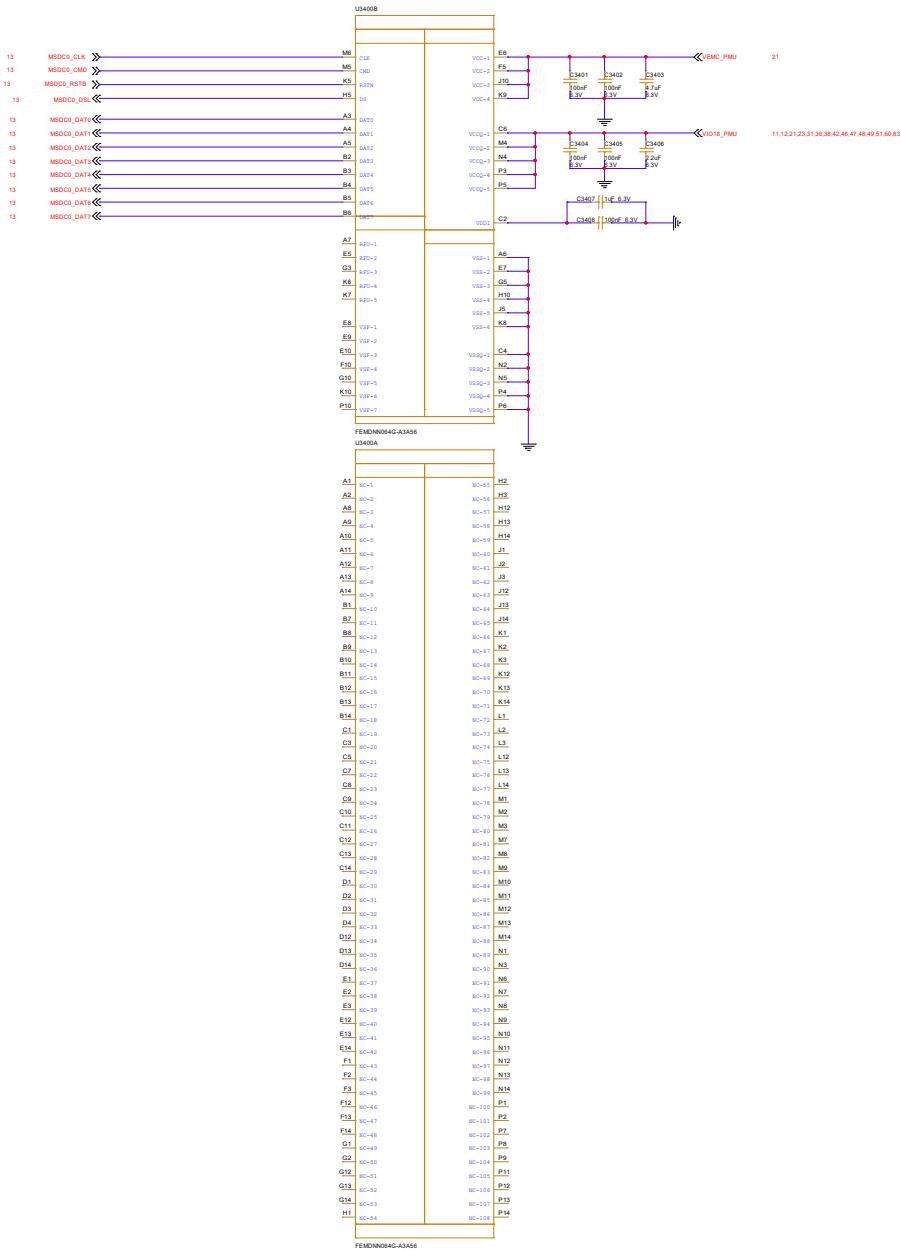


Connect to SOC Connect to EMI

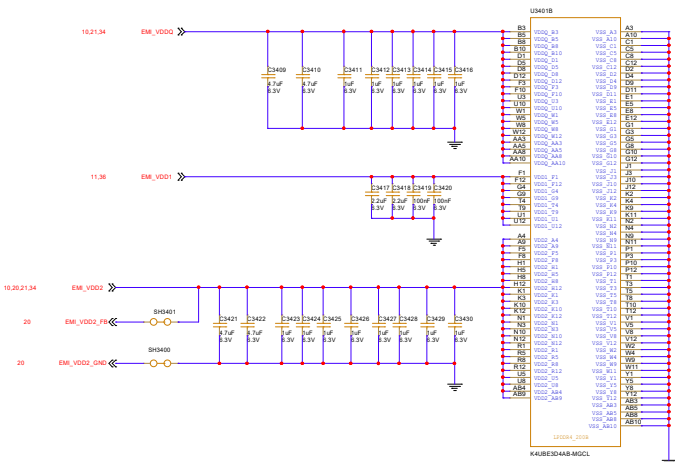


TINNO			
REVISION	Xingjun.Yu		
TITLE	LAMB_06		
PAGE	31_MT6382		
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	31 OF 100

eMMC5.1---32GB

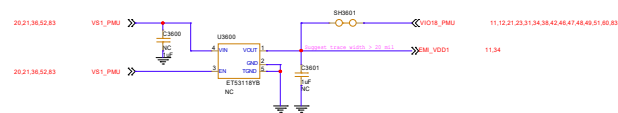


VCC-C3403	VCCQ-C3406	VDDIO-C3407
宏芯宇	4.7uF	4.7uF
正波龙	2.2uF	2.2uF
		1uF



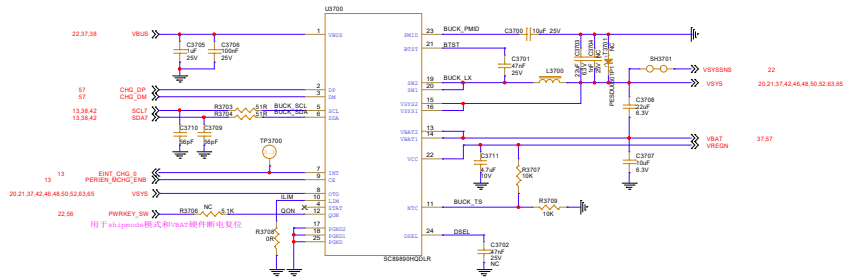
TINNO			
REVISION	Xinglin Ye		
TITLE	LAMBUR		
PAGE	34_OBSCURE_D0RXX		
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	34 OF 100

Ext. EMI_VDD1 for LPDDR4X VDD



TINNO			
DESIGNED		Xingjian.Yu	
TITLE		LAMU_MB	
PAGE		38_POWER_EXT	
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	36 OF 100

CHARGE_10W&15W_W/PP

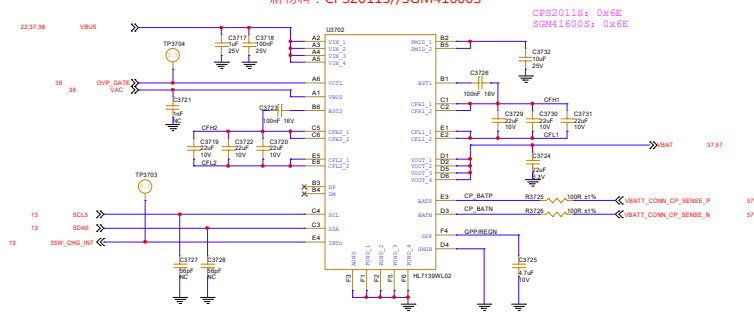


SGM41542/SGM41543D/SC89890H compatible design

Option_15W	C3702	R3708	R3700	C3708
SGM41542	NC	NC	NC	NC
SGM41543D	NC	NC	NC	22uF
SC89890H	47uF	0R	NC	22uF

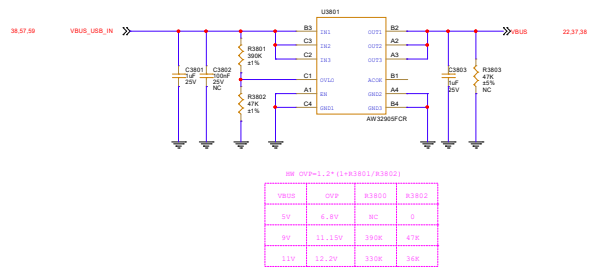
CHARGE_33W_CP0

新物料：CPS2011S/SGM41600S

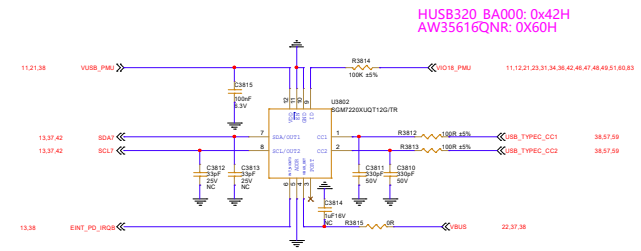


CPS2011S: 0x6E
SGM41600S: 0x6E

OVP IC

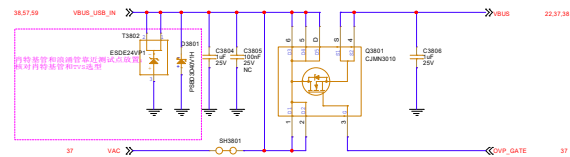


CC LOGIC



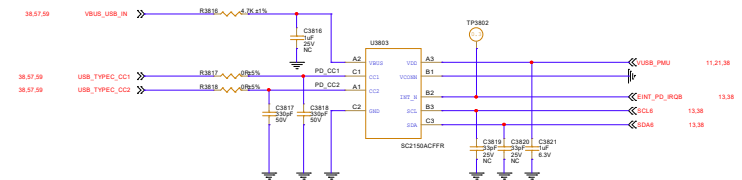
MOS OVP

Without WLC

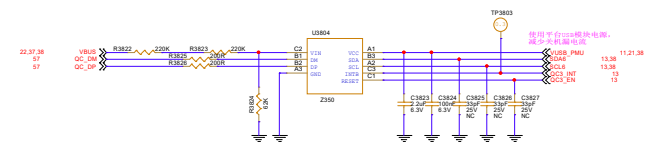


PD PHY

U3803:贴片使用EG09-SC2150-001//SC2150PCFFR

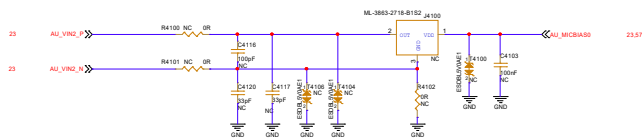


QC PHY

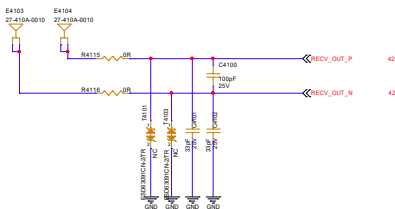


TINO			
DESIGNED		Xingjian Yu	
TITLE		LABU_MB	
PAGE		38_OVP_PD_OC_PHY	
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	38 OF 100

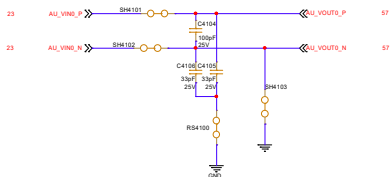
Sub MIC



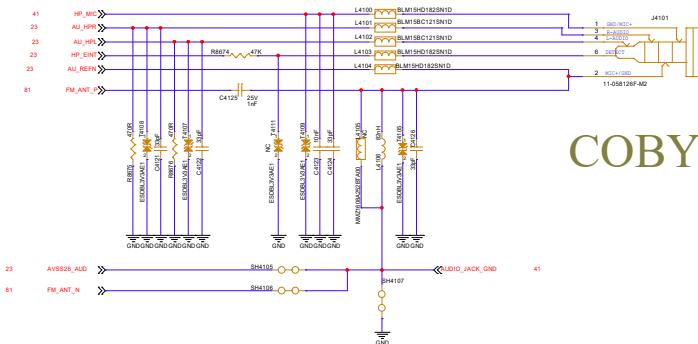
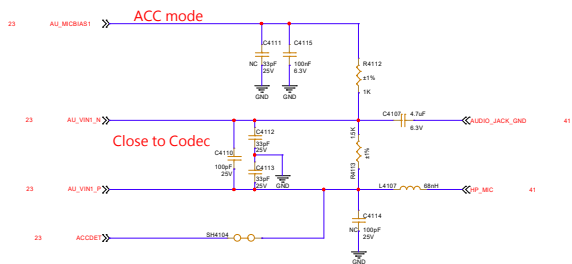
Handset Receiver



Main MIC



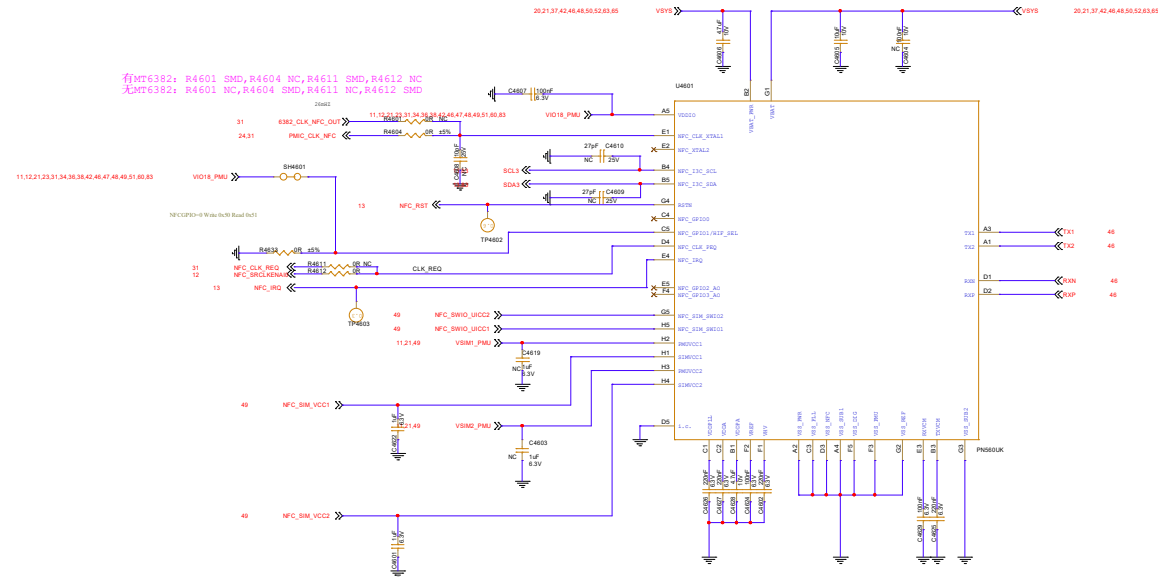
Headset Mic



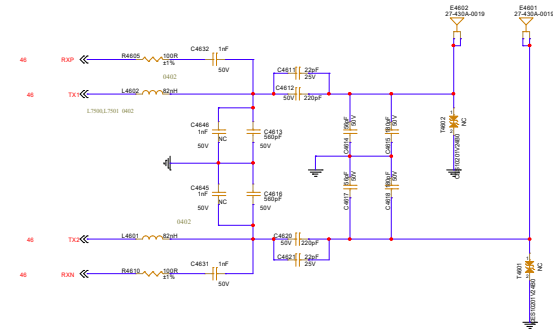
COBY-P352CE


TINNO			
REVISION		Xingjun.Yu	
TITLE		LAMEL_MIS	
PAGE		41_AUDIO	
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	41 OF 100

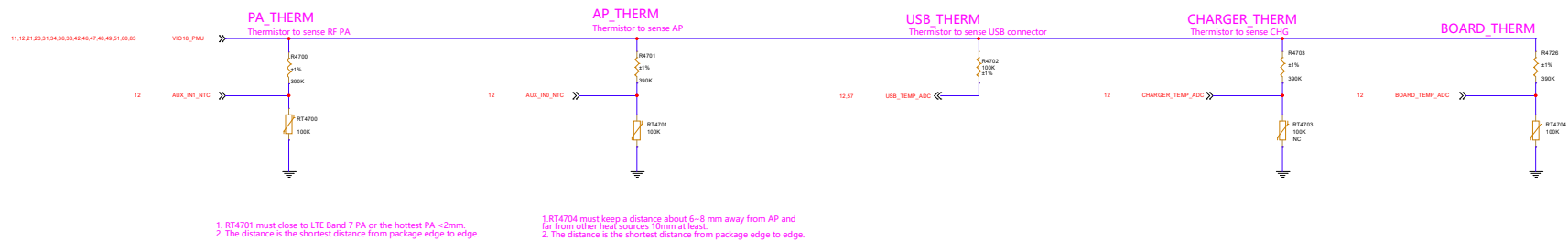
NFC PN560UK Circuit



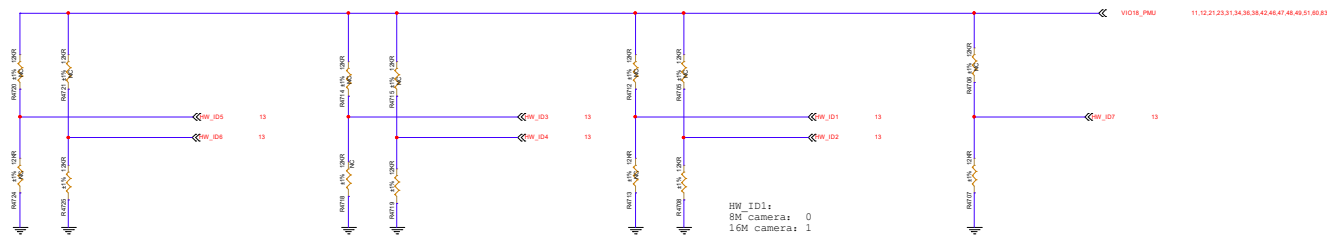
NFC antenna interface



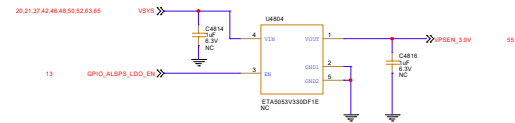
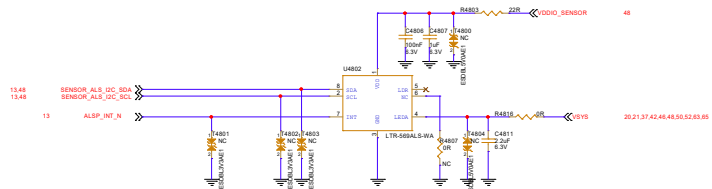
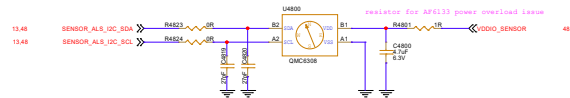
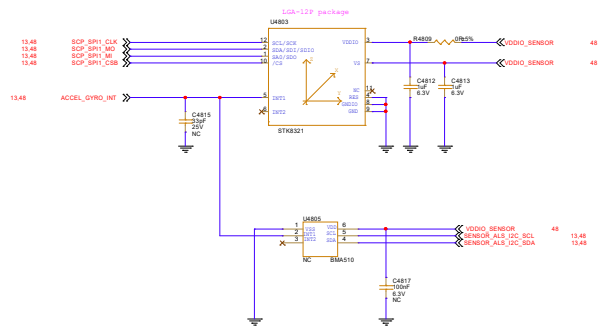
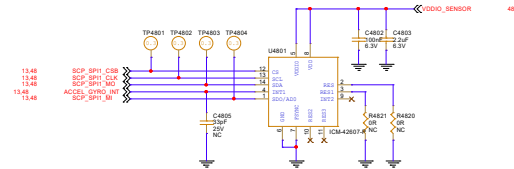
				
DESIGNED		Xingjian Yu		
TITLE		LAMU_MB		
PAGE		46_NFC		
SIZE	D	REV	V1.0	
DATE	Thursday, October 31, 2024	SHEET	46	OF 100



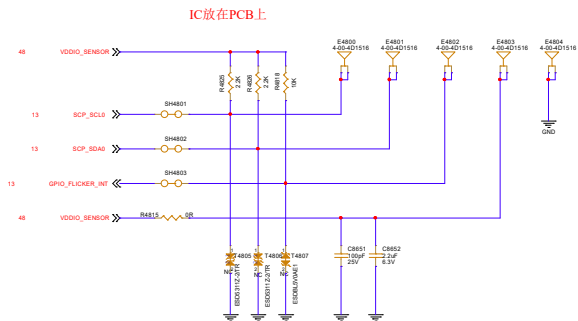
HW ID



TINNO			
DESIGNER		Xinglan.Yu	
TITLE		LAMBDA	
PAGE		47_THERMAL_HW_ID	
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	47 OF 100

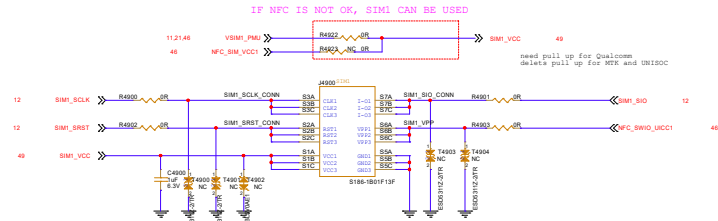


如客户无特殊要求，可以和指纹电源共用，注意核对电压和过流能力

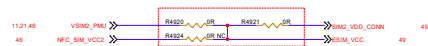


				
DESIGNED		Xingjian Yu		
TITLE		LAMU_MB		
PAGE		48_SENSOR		
SIZE	D	REV	V1.0	
DATE	Thursday, October 31, 2024	SHEET	48 OF	100

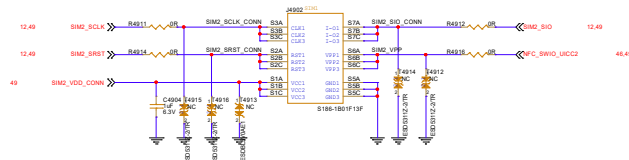
SIM1



```
有NFC无ESIM: R4920 NC,R4921 SMD,R4924 SMD
有NFC有ESIM: R4920 NC,R4921 NC,R4924 SMD
无NFC无ESIM: R4920 SMD,R4921 SMD,R4924 NC
无NFC有ESIM: R4920 SMD,R4921 NC,R4924 NC
```

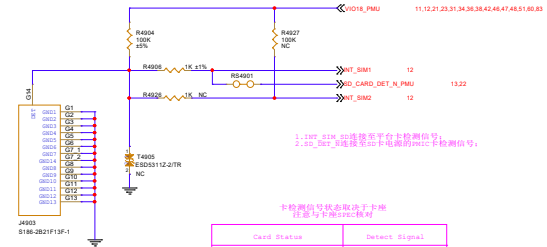
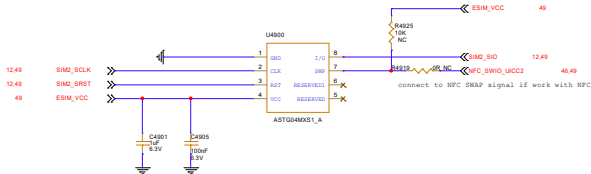


SIM2



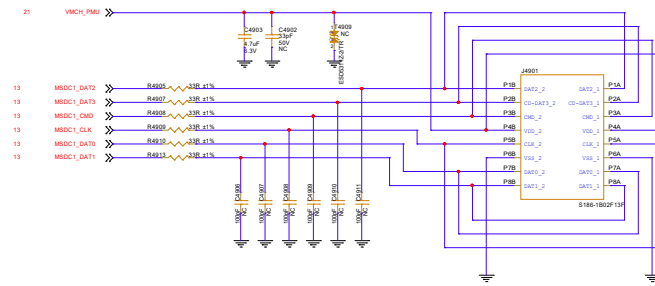
eSIM

U4900 PN is ASTG04MXS1, not is ASTG04MXS1_A
If U4900 is ASTG04MXS1_A, R4919 and R4925 must SMD

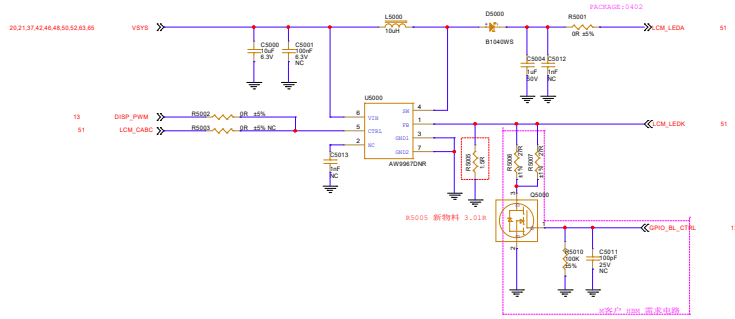


Card Status	Detect Signal
Card Not Installed	0
Card Installed	1

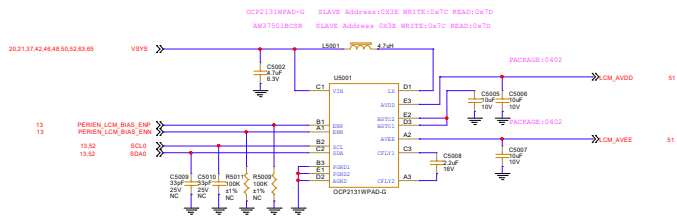
SD CARD



LCD BL DRIVER

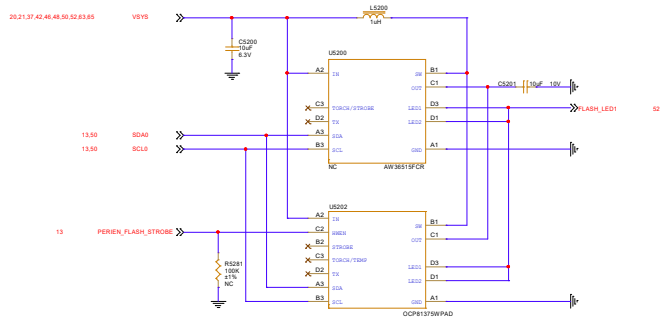


LCD BIAS DRIVER

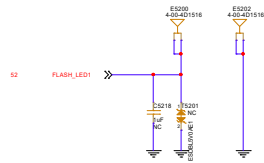


FLASH DRIVER

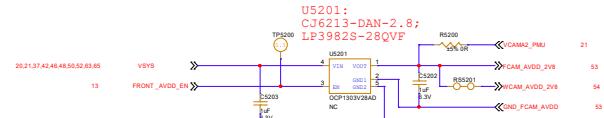
Dual Independent for Flash 2.0A and Torch 0.5A



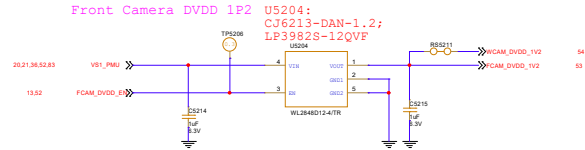
FLASH LED



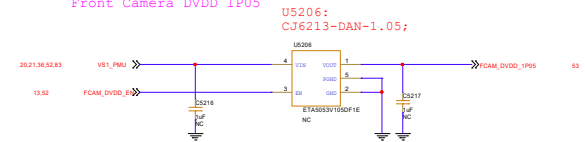
Front Camera AVDD



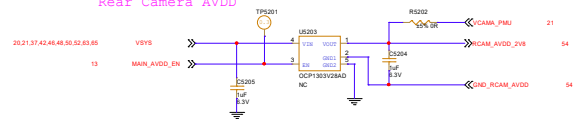
Front Camera DVDD 1P2



Front Camera DVDD 1P05



Rear Camera AVDD

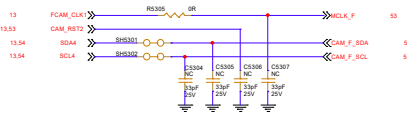
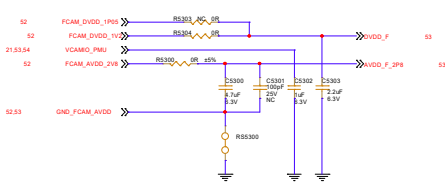
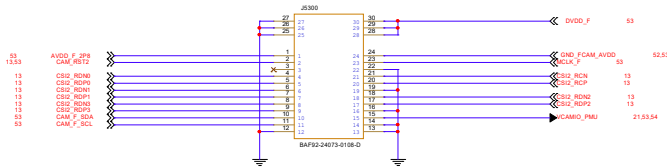


TINNO				
REVISION		Xinglan.Yu		
TITLE		LAMB_M8		
PAGE		S2_LDO_FLASH		
SIZE	D	REV	V1.0	
DATE	Thursday, October 31, 2024	SHEET	S2 OF	100

FRONT CAMERA CONNECTOR

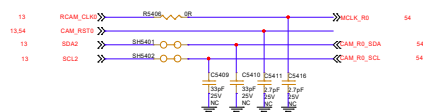
32M F

FRONT CAM	Sensor	AVDD	DVDD	DOVDD	APVDD	I2C
32M	GC32E1	2.8V Max 55mA	1.2V Max 120mA	1.8V Max 5mA	/	Sensor: 0x20 (W) 0x21 (R) EEPROM: 0xA2 (W) 0xA3 (R)

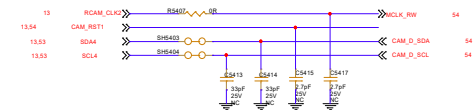
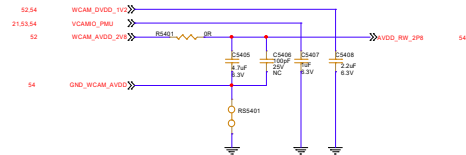


50M/32M AF

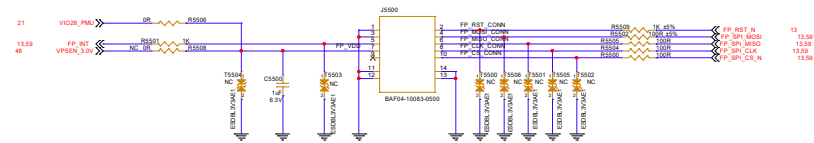
Pin 1 to 16 connection diagram for the GB309-243-HEB-E 10000 component. The component is shown as a yellow rectangle with pins 1 through 16 on the left and pins 27 through 34 on the right. Pin 1 is connected to VCC400_FPMU. Pin 2 is connected to AVDD_RIS_278. Pin 3 is connected to CAM_RIS_15. Pin 4 is connected to CSB_RIS_16. Pin 5 is connected to CSB_RIS_17. Pin 6 is connected to CSB_RIS_18. Pin 7 is connected to CSB_RIS_19. Pin 8 is connected to CSB_RIS_20. Pin 9 is connected to CSB_RIS_21. Pin 10 is connected to CSB_RIS_22. Pin 11 is connected to CSB_RIS_23. Pin 12 is connected to CSB_RIS_24. Pin 13 is connected to CSB_RIS_25. Pin 14 is connected to CSB_RIS_26. Pin 15 is connected to CSB_RIS_27. Pin 16 is connected to CSB_RIS_28. Pin 27 is connected to DSD_RIS_14. Pin 28 is connected to DSD_RIS_15. Pin 29 is connected to DSD_RIS_16. Pin 30 is connected to DSD_RIS_17. Pin 31 is connected to DSD_RIS_18. Pin 32 is connected to DSD_RIS_19. Pin 33 is connected to DSD_RIS_20. Pin 34 is connected to DSD_RIS_21. The component is labeled GB309-243-HEB-E 10000.



8M FF

[illegible]

FINGERPRINT CONNECTOR



屏下指纹需连接至小板上，e20器件可删除

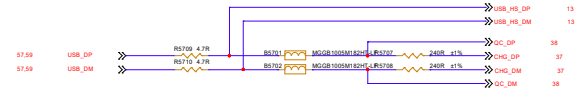
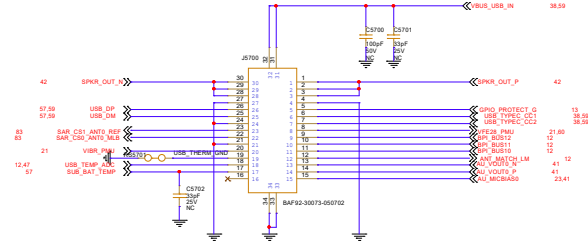
TINNO			
DESIGNED		Xinglan.Yu	
TITLE		LAMB_M6	
PAGE		55_FP	
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	55 OF 100



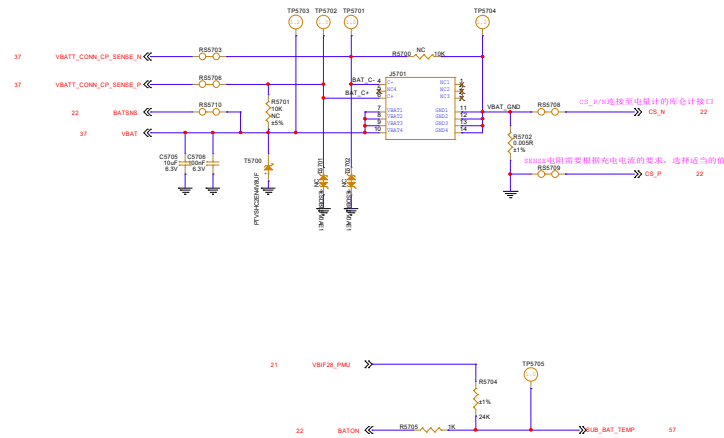
SUB BOARD CONNECTOR

MTK/UNISOC平台

J5700: EI01-BAF923-000



BATTERY CONNECTOR

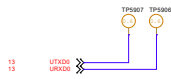


TINNO				
REVISION		Xinglan.Yu		
TITLE		LAMBDA		
PAGE		ST_BAT_CONN_SUB_BOARD		
SIZE	D	REV	V1.0	
BATK	Thursday, October 31, 2024	SHEET	57	OF 100

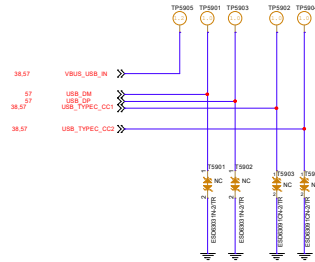
RAMdump



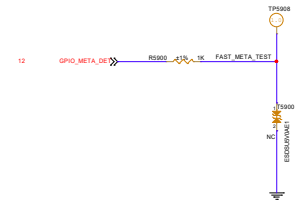
UART



USB



Fast META



Mark



PCB板和PCB标签

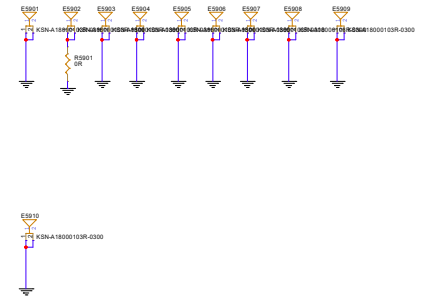


屏蔽件

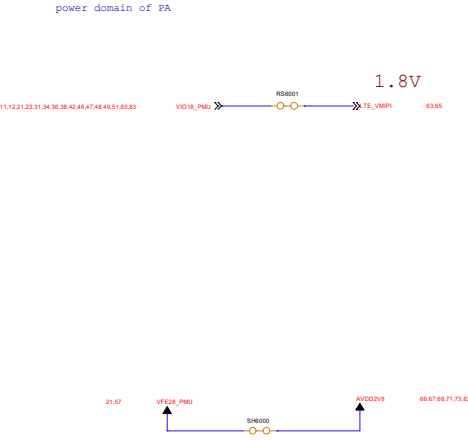
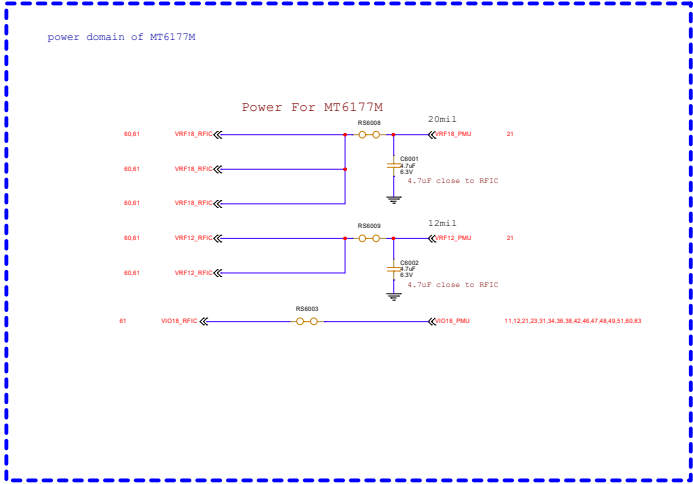
屏蔽罩根据pcb实际堆叠确认类型、数量及尺寸

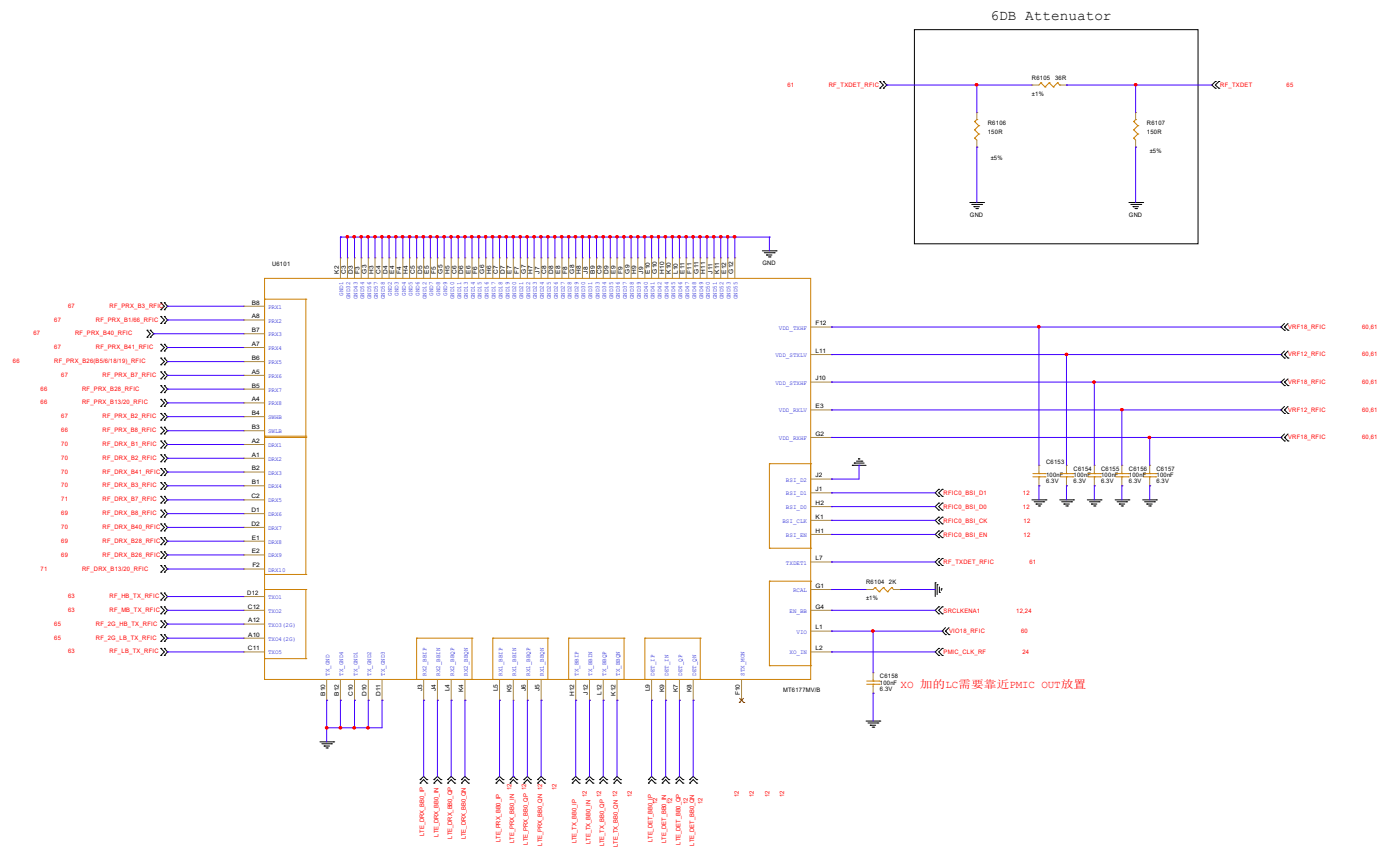


Top



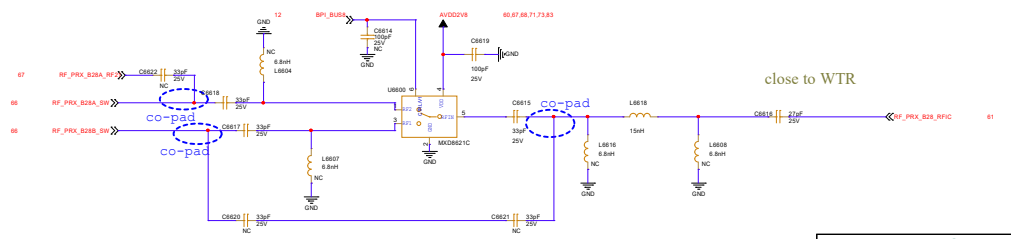
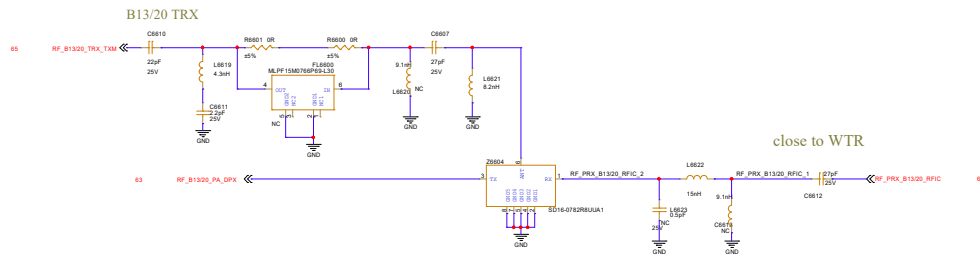
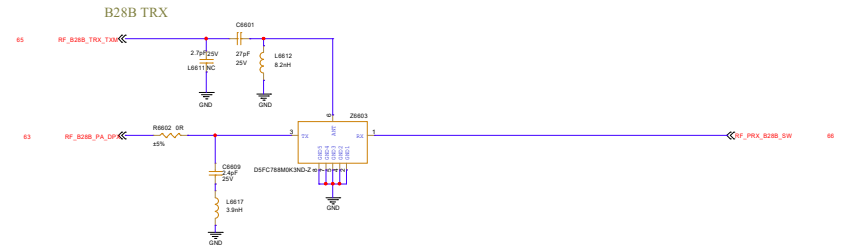
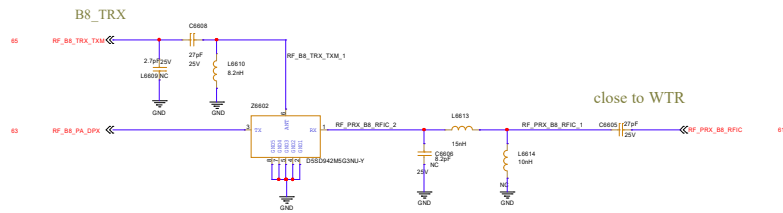
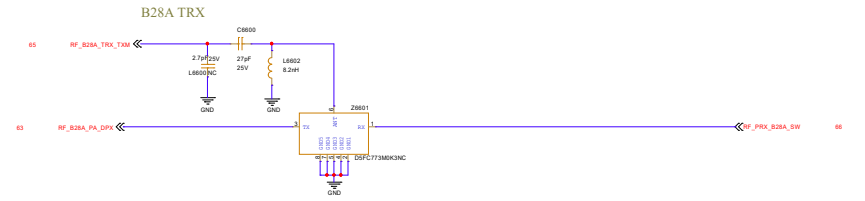
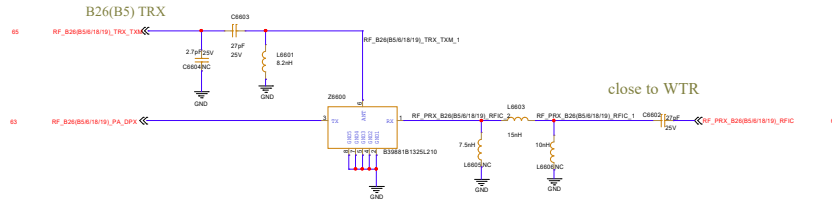
TINO			
DESIGNED		Xingqian Yu	
TITLE		LAMU_MB	
PAGE		50_TP_GND_SHIELDING_MARK	
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	50 OF 100



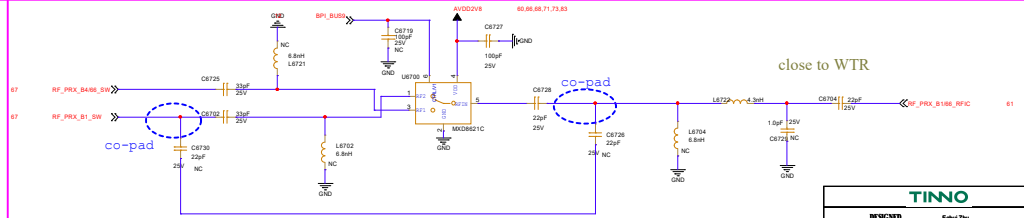
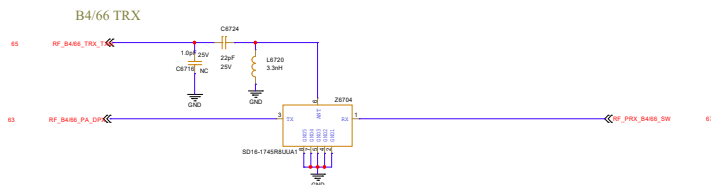
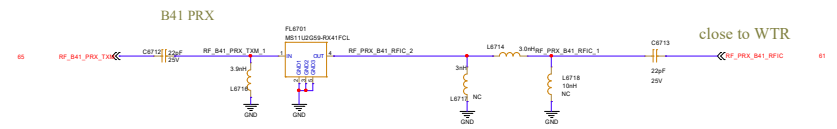
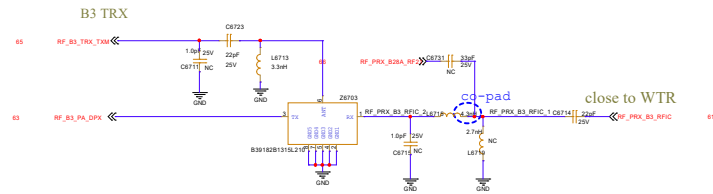
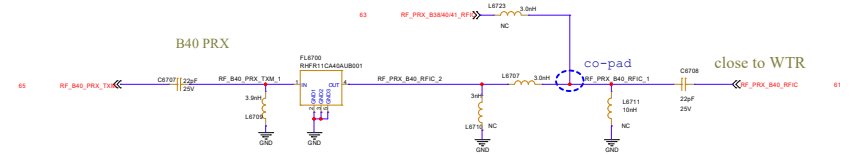
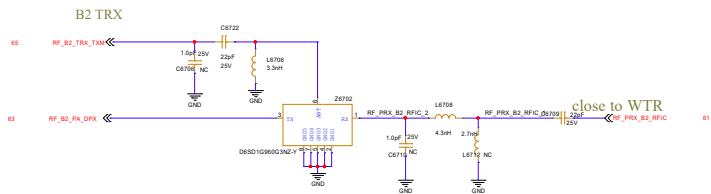
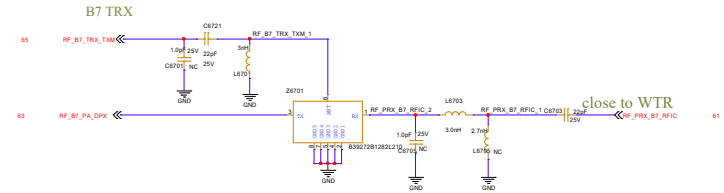
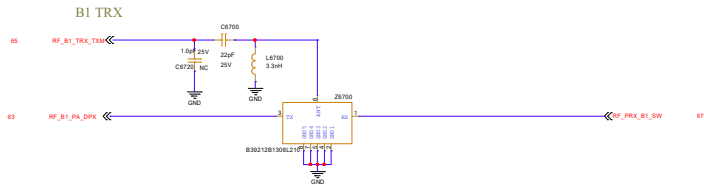


BOARD_ID2	GPIO 122	WCN Clock
	0	TCXO+DCXO/TSX(WIFI only)
	1	TSX

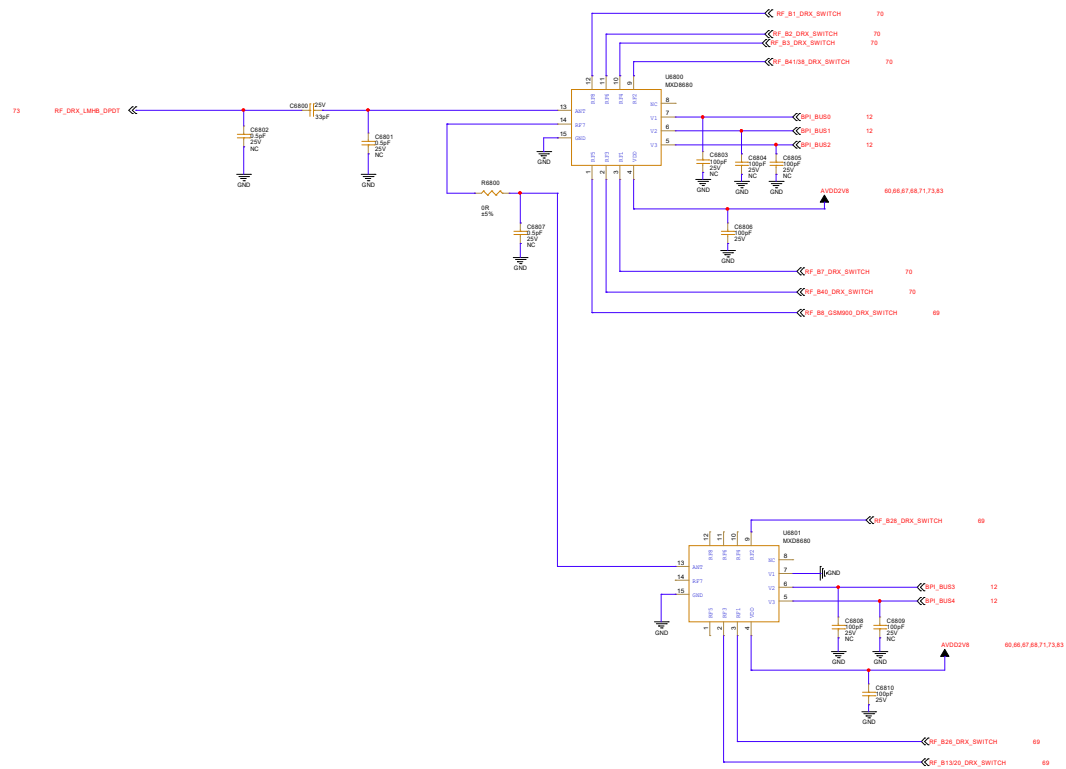
TINNO			
DESIGNER	Fahad Zuo		
TITLE	LAMBDA		
PAGE	81_TRANSCIVER_JOMPER		
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	61 OF 100



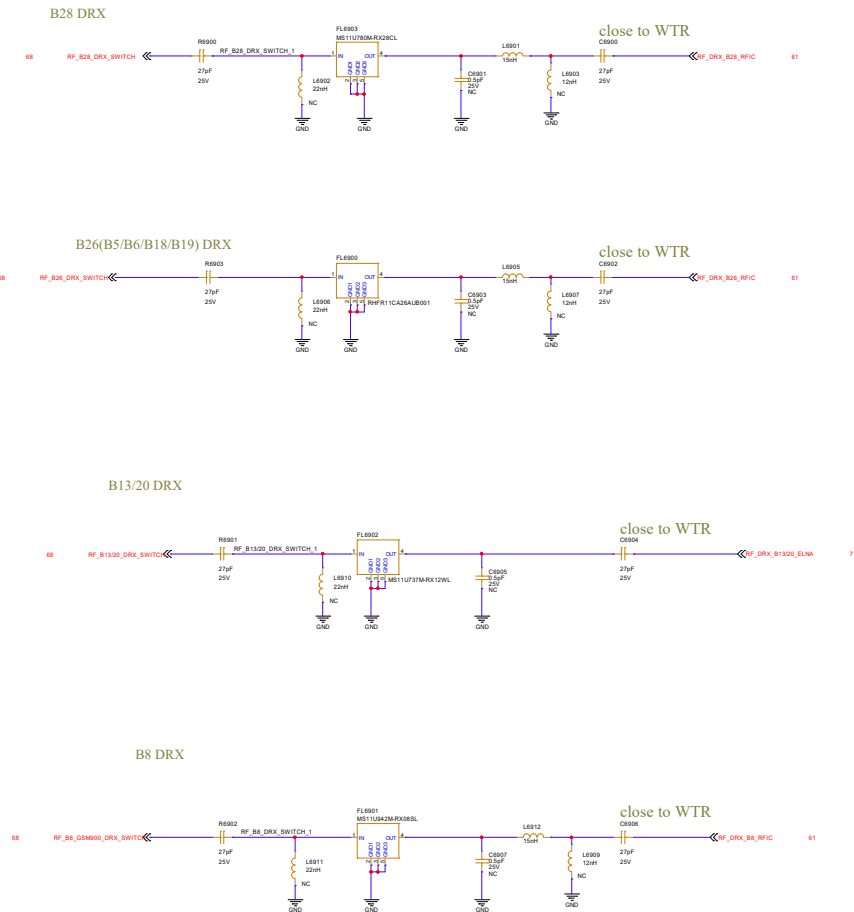
TINNO				
REVISION	Fahad.Zhu			
TITLE	LAMBDA			
PAGE	86_RF_TRX_LB			
SIZE	D	REV	V1.0	
DATE	Thursday, October 31, 2024	SHEET	68	OF 100



TINNO				
DESIGNED	Fahad Zuo			
TITLE	LAMBDA			
PAGE	RF_TRX_MW			
SIZE	D	REV	V1.0	
DATE	Thursday, October 31, 2024	SHEET	67	OF 100

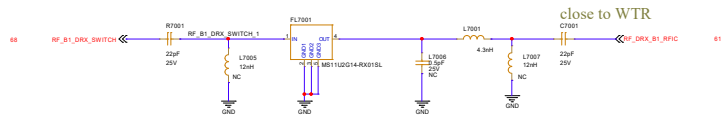


TINNO			
DESIGNER		Fahad Zuo	
TITLE		LAMB_M8	
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SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	68 OF 100

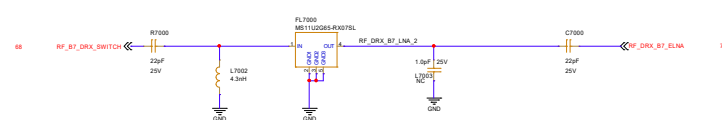


TINNO			
REVISION		Folio: 2/2	
TITLE		LAMELLE	
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SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	69 OF 100

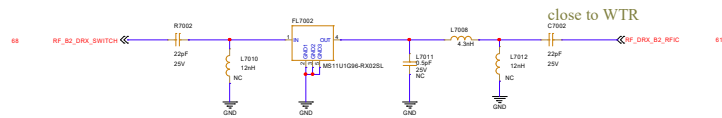
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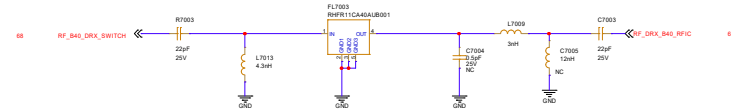
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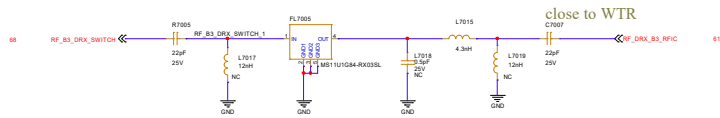
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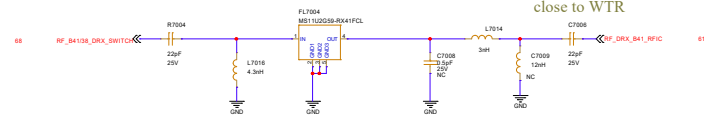
B40 DRX



B3 DRX

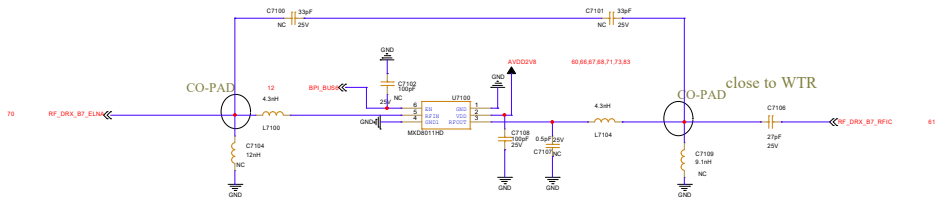


B41 DRX

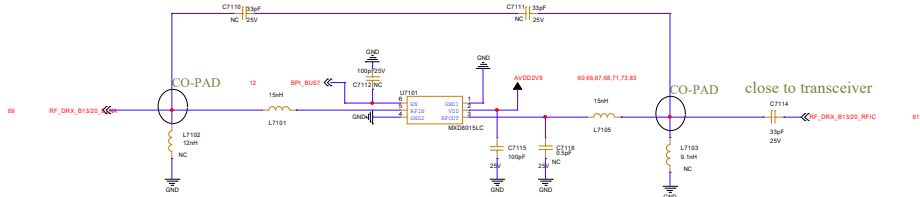


TINNO			
REVISION		Fahad.Zhu	
TITLE		LAMBDA	
PAGE		70_DRX_FILTER_MMB	
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	70 OF 100

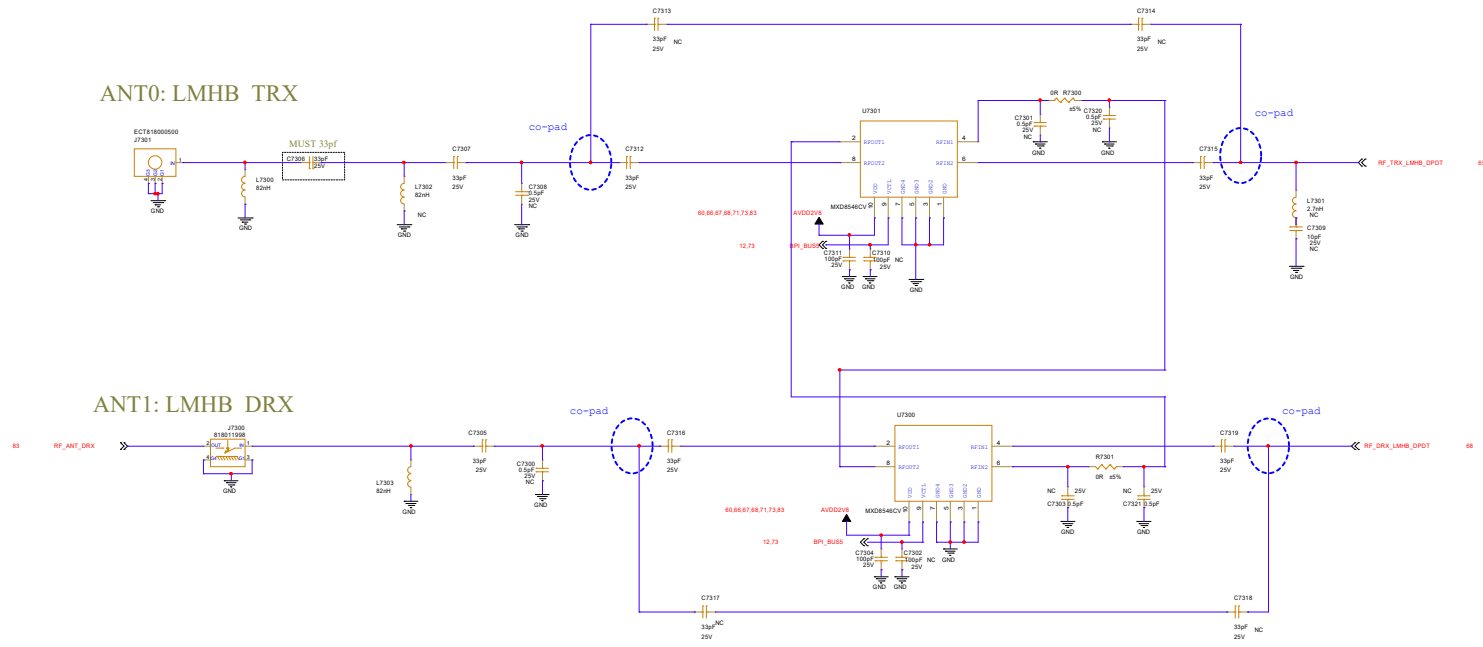
B7_DRX LNA

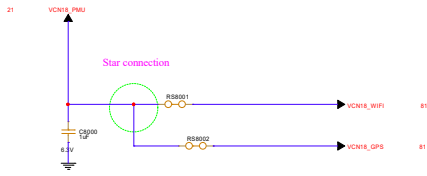
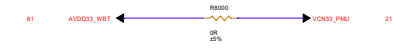


B20_DRX LNA



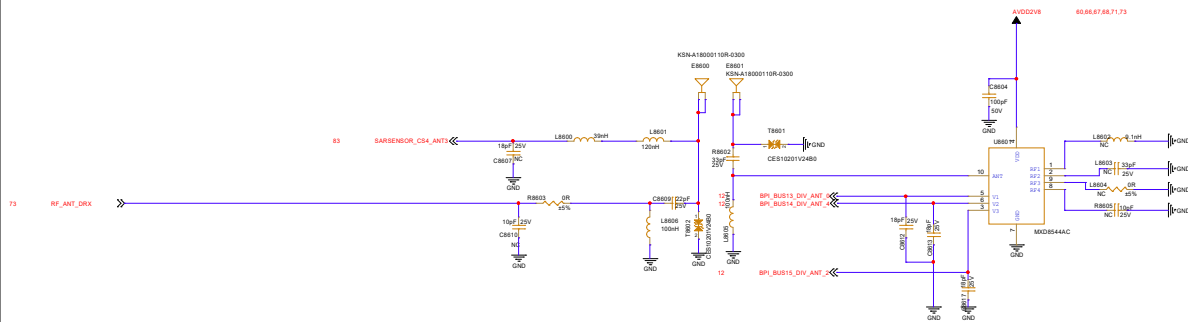
TINNO			
DESIGNED	Fahad Zuo		
TITLE	LAMBDA		
PAGE	71_RF_LNA		
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	71 OF 100



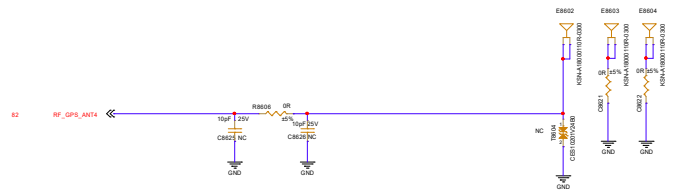


TINNO			
DESIGNED		Felix Zhu	
TITLE		LAMA_MB	
PAGE		85_WCH_PWR	
SIZE	D	REV	V1.0
DATE	Wednesday, October 26, 2023	SHEET	85 OF 109

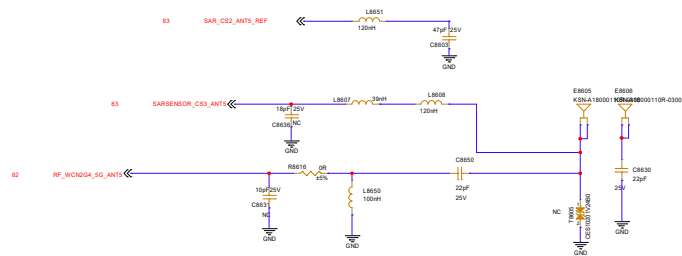
ANT3: LMHB DRX



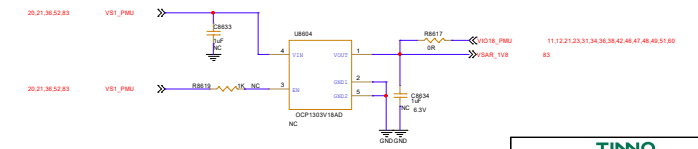
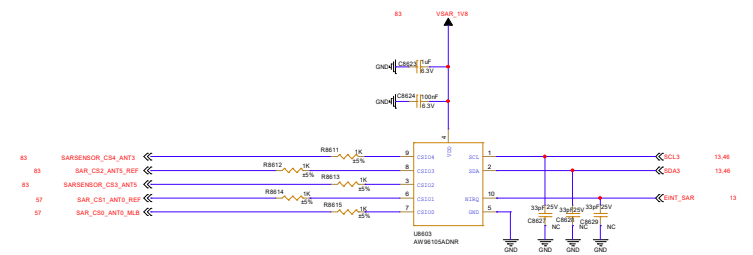
ANT4: GPS



ANT5: WCN_2.4G/5GWIFI_BT

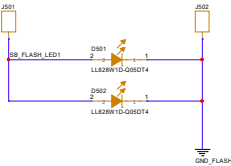


SAR Sensor IC
AW96105ADNR



TINNO			
DESIGNED		Chu Xiao	
TITLE		LAMU_MB	
PAGE		86_ANT	
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	83 OF 109

FLASH



TINNO			
DESIGNED		Xinglin.Yu	
TITLE		LAMB_FLASH	
PAGE		100_SUB_FLASH	
SIZE	D	REV	V1.0
DATE	Thursday, October 31, 2024	SHEET	105 OF 109