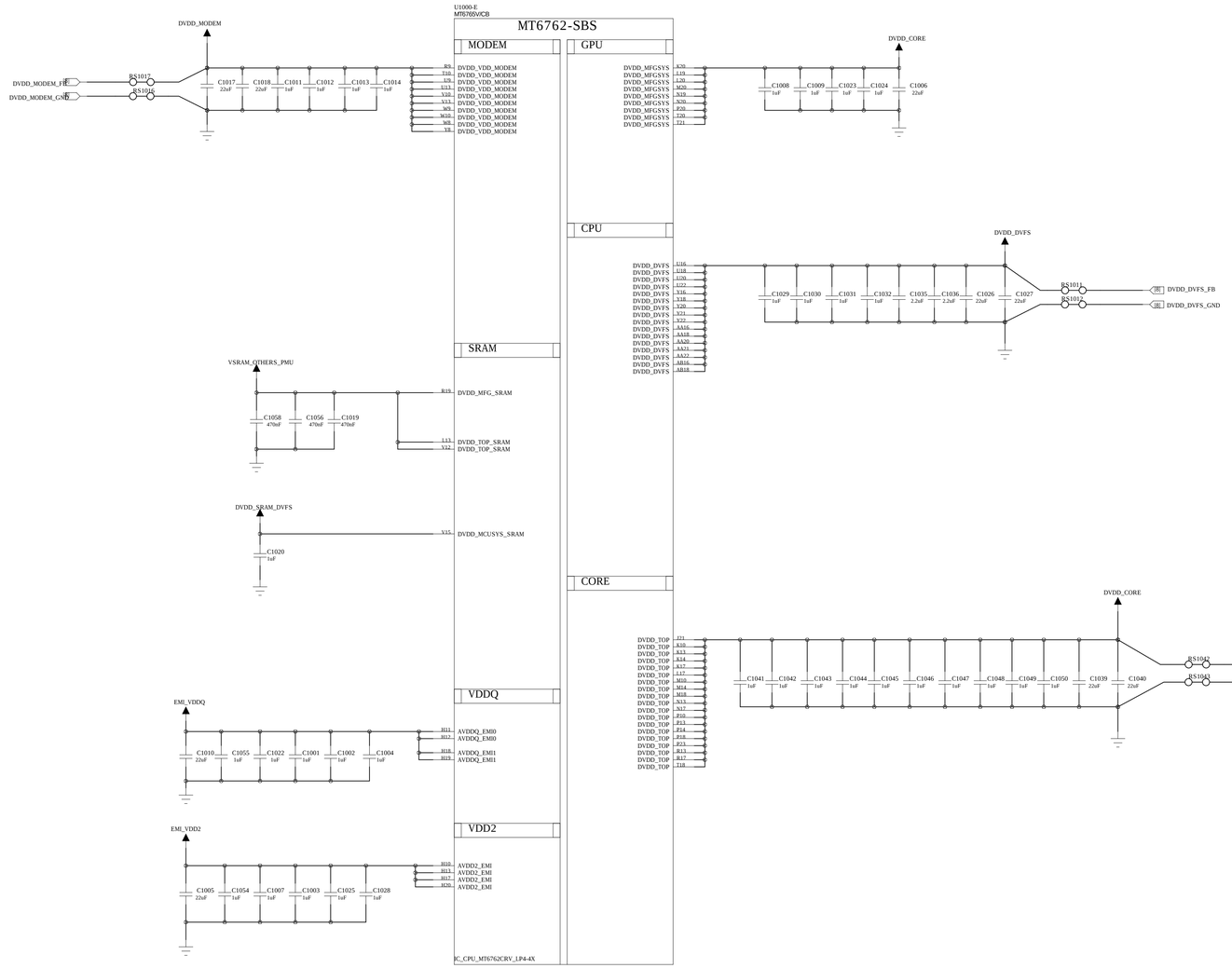
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



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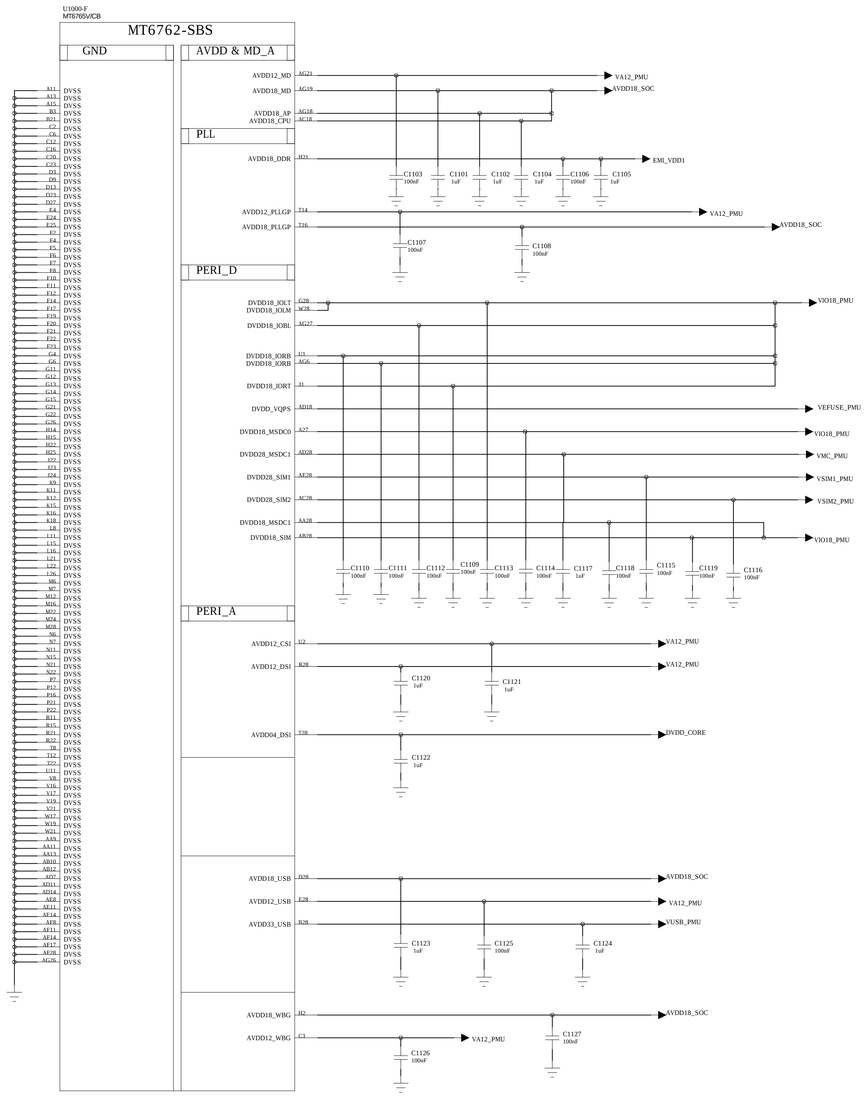
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: MT6765	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: P410	SIZE: D
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: P410	REV: V1.0
		SCALE: <Scale>	SHEET: 2 OF 33

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



Schematic design notice of "11_BB_POWER_IO" page.

Note 11-1: C4101 closed DVDD18_MSDC0 150mil

Note 11-2: C4302 closed DVDD28_MSDC1 150mil

Note 11-3: C4301 closed DVDD18_MSDC1 150mil

DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: MT6765	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: P410	SIZE: D
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: P410	REV: V1.0
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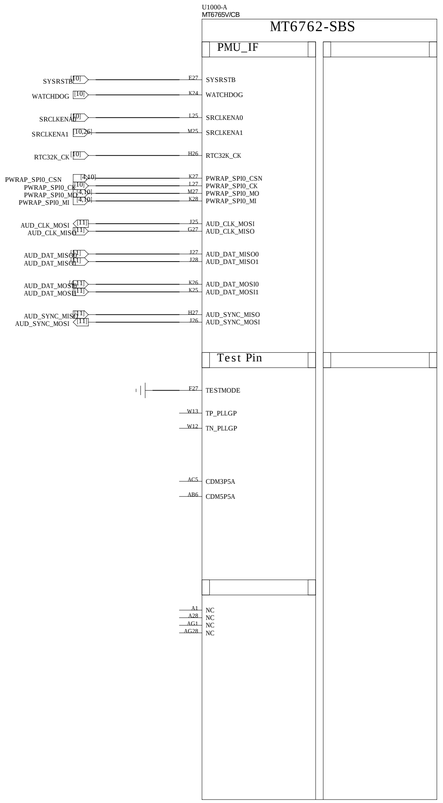
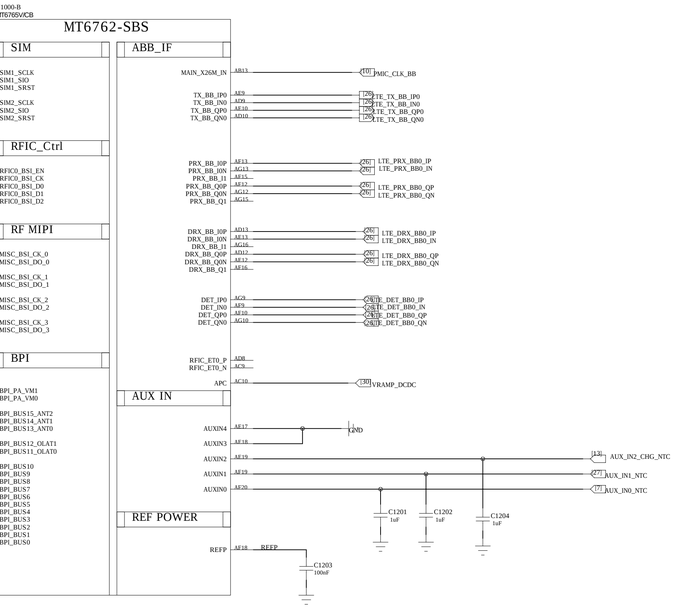
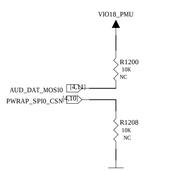
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

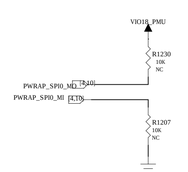






"PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pin to select which interface will be the JTAG pin out.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	JTAG Function	
default=PU	default=PD	AP_JTAG	MD_JTAG
HI	LO	N/A	N/A
HI	HI (by ext. PU)	SPI0+EINT8	SPI1+SPI3
LO (by ext. PD)	LO	SPI0+EINT8	N/A
LO (by ext. PD)	HI (by ext. PU)	MSDC1	N/A

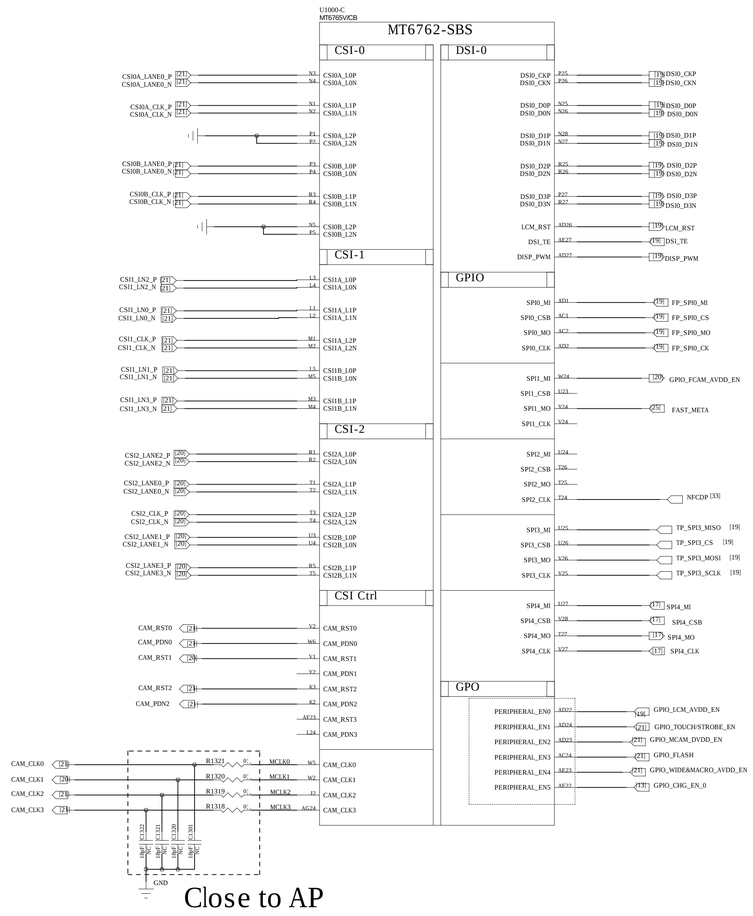


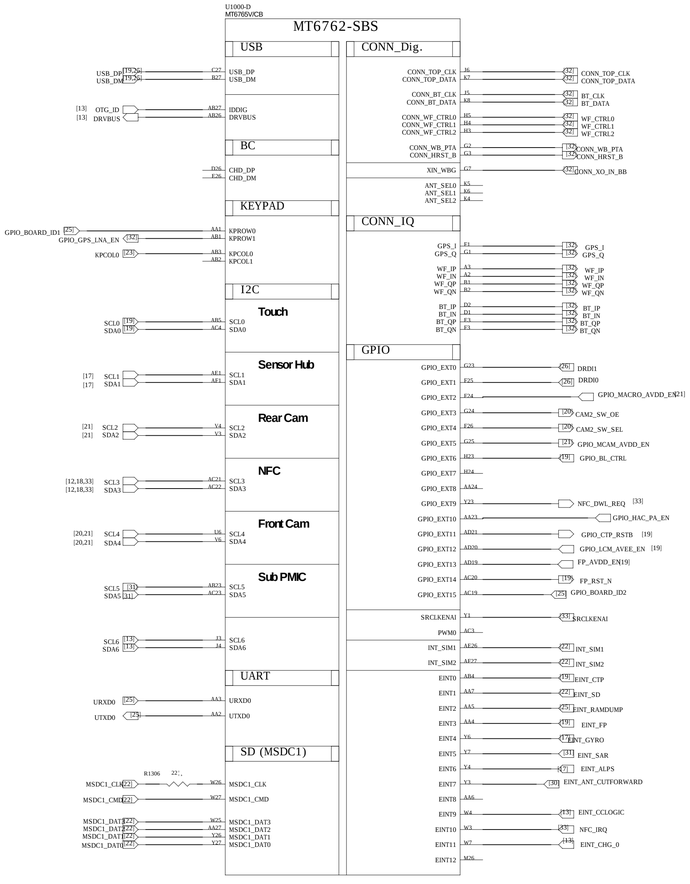
Note 12-4: PWRAP_SPI0_MI / PWRAP_SPI0_MO is DDR type feature in bootstrap

PWRAP_SPI0_MI	PWRAP_SPI0_MO	Booting interface	
default=PU	default=PD	DDR	MSDC0 pin mux
LO (by ext. PD)	LO	LPDDR3	follow LPDDR3 Ref SCH.
LO (by ext. PD)	HI (by ext. PU)	N/A	N/A
HI	LO	LPDDR4X	follow LP4X/LP4 Ref SCH.
HI	HI (by ext. PU)	LPDDR4	follow LP4X/LP4 Ref SCH.

DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno	
		TITLE: MT6765	
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: P410	SIZE: D
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: P410	REV: V1.0
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 4 OF 33

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



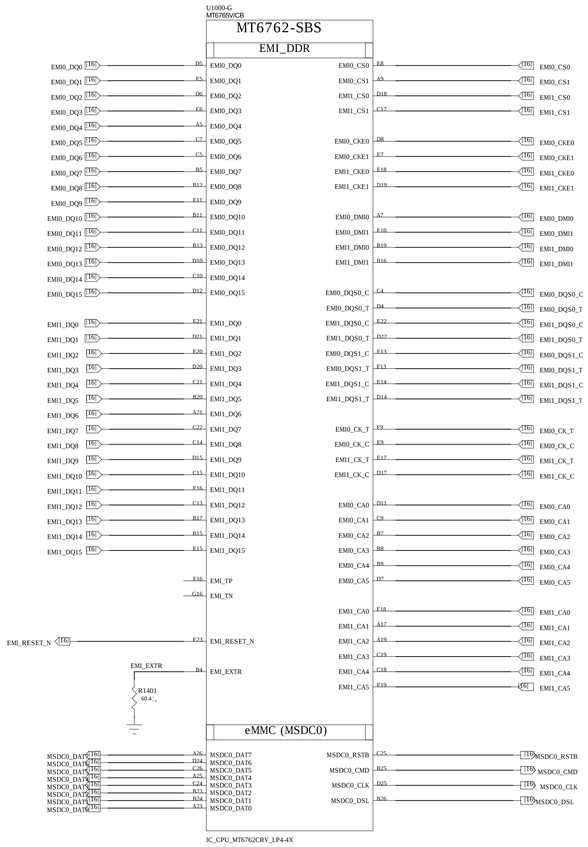


Schematic design notice of "13_BB_2" page.

Note 13-1: The enable pin of acoustic or optoelectronic devices (e.g. SPK AMP/Backlight/Charger OCP/OVP) suggest to use Peripheral_EN[0:5]
If use other GPIOs as enable pin, suggest to reserve 0201 NC to GND

COMPANY: Tinno			
TITLE: MT6765			
DRAWN: Marshall	DATED: 2018-09-22A		
CHECKED: <Checked By>	DATED: <Checked Date>		
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>		
CODE: P410	SIZE: D	DRAWING NO: P410	REV: V1.0
SCALE: <Scale>	SHEET: 56 33		

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



Schematic design notice of "14_BB_3" page.

Note 14-1: R4001 please select 60.4 ohm (1%) resistor

Note 14-2: Please check eMCP LP3 and eMCP LP4X/LP4 pin mux

DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno	
		TITLE: MT6765	
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: P410	SIZE: D
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: P410	REV: V1.0
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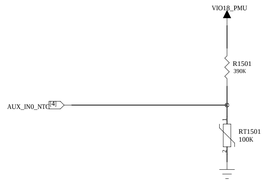
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



Thermistor to sense AP temperature

1. NTC1501must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.
2. The distance is the shortest distance from package edge to edge.

DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno			
		TITLE: MT6765			
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: P410	SIZE: D	DRAWING NO: P410	REV: V1.0
QUALITY CONTROL: <QC By>	DATED: <QC Date>				
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 33	

Schematic design notice of "20_POWER_MT6357_Buck"

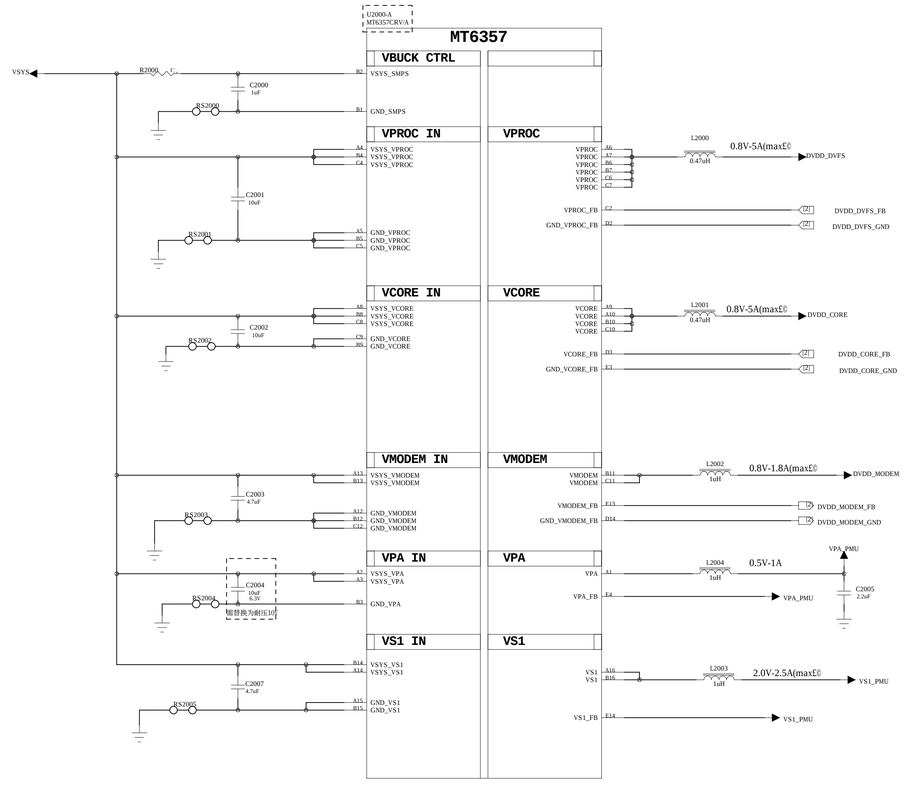
Note 20-1: C2005, please choose 0402 size

Note 20-2: PMIC Part number notice for MT6765/62/61 platform

MTK Platform	PMIC
MT6765 / 62	MT6357 CRV
MT6761	MT6357 MRV

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

MTK Platform	PMIC
MT6765/62	MT6357CRV
MT6761	MT6357MRV



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QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: P410 / SIZE: D / DRAWING NO: P410 / REV: V1.0	
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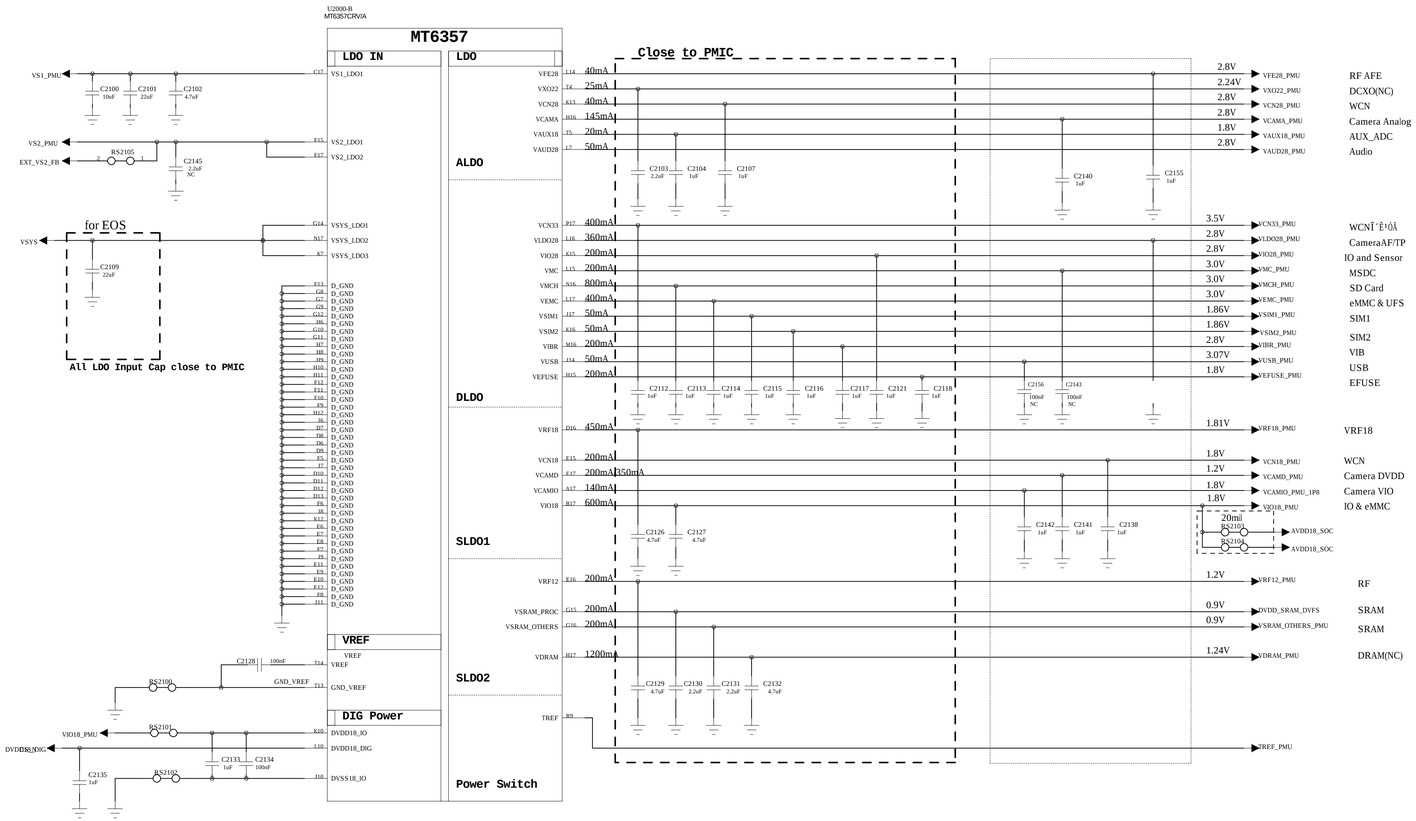
LTR	ECO NO:	APPROVED:	DATE:



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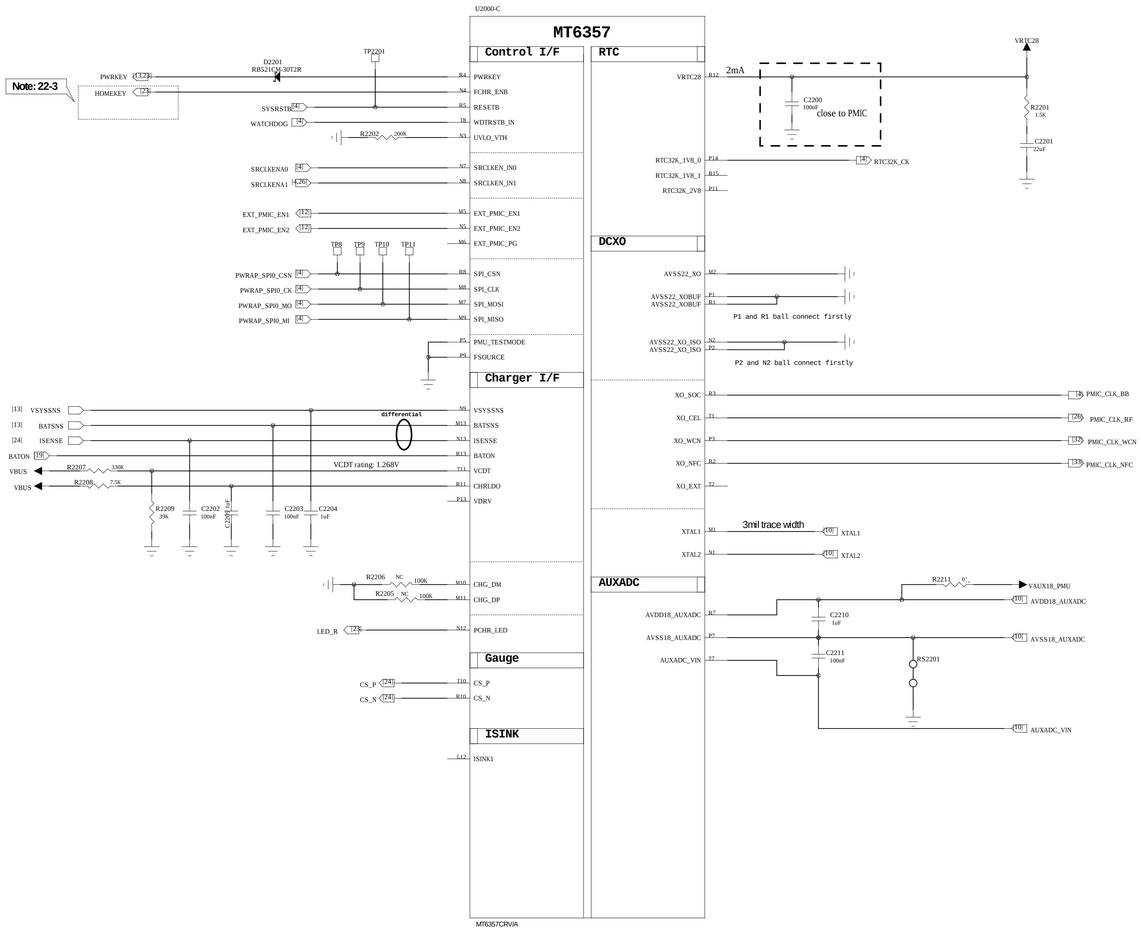
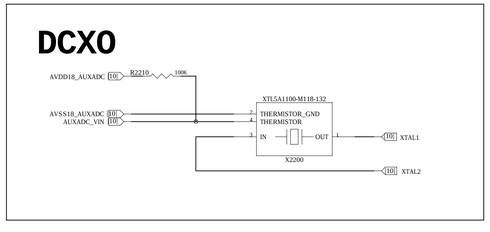
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: P410	SIZE: D
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: P410	REV: V1.0
		SCALE: <Scale>	SHEET: 33

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Design Noice

	With Power Path	Without Power Path
ISENSE	VBAT(Charger output)	Rsns(L side)
BATSNS	VSYS(Charger output)	Rsns(VBAT side)
VSYSSNS	VSYS(Charger output)	VBAT(Con)





Schematic design notice of "22_POWER_MT6357-IF"

Note 22-1:	Please implement 2520 & 2016 Size TMS PCB co-layout. Please refer to MT6762_MT6357 Co-Clock Design Notice for co-layout guide
Note 22-2:	1. Please Connect P1 and R1 ball first and then to GND 2. Please Connect P2 and N2 ball first and then to GND 3. Please connect DCXO GND to main GND by independent L1-2 GND via.;
Note 22-3:	DO NOT connect it through L1 GND Let floating if disable HOMEKEY function
Note 22-4:	Please follow MT6762_MT6357 Co-Clock Design Notice for Layout guide of VAUX18, then R8101 can use 0 ohm to replace BEAD.
Note 22-5:	Please connect to battery connector

COMPANY: Tinno			
TITLE: MT6765			
DRAWN: Marshall	DATED: 2018-09-22A		
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: P410	SIZE: D
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: P410	REV: V1.0
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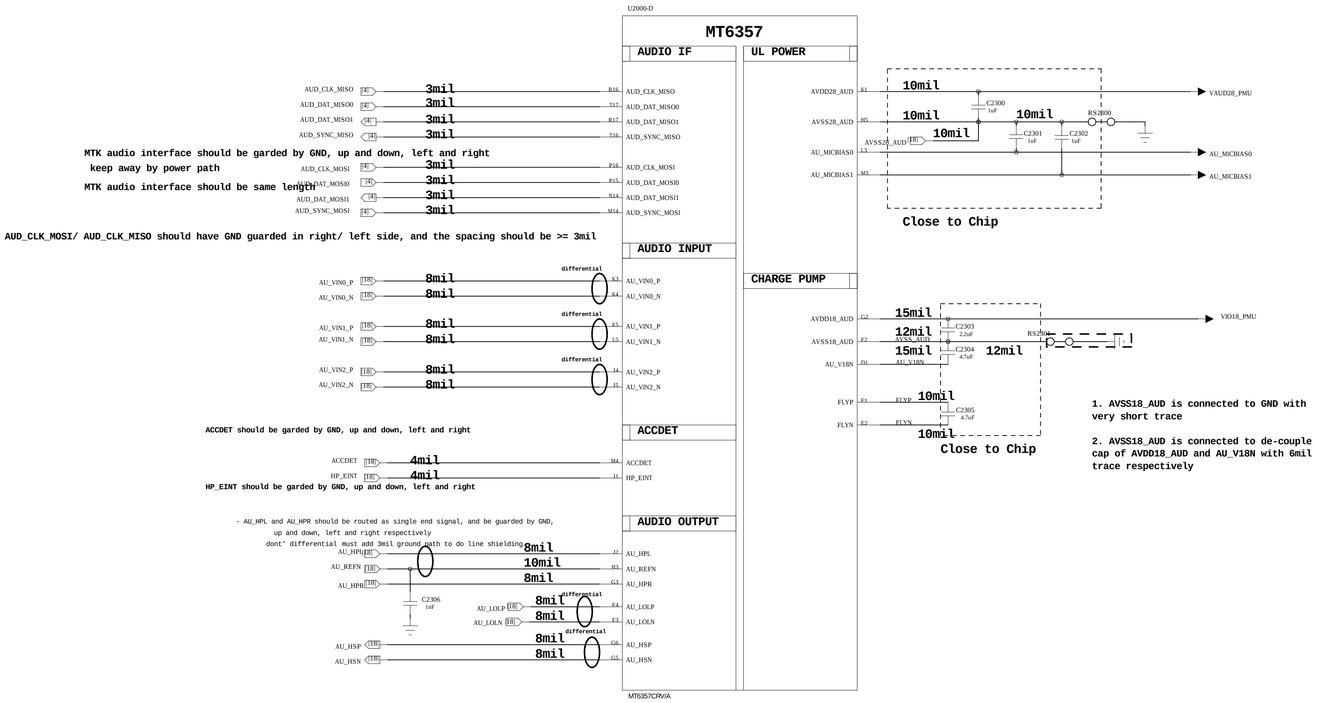
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



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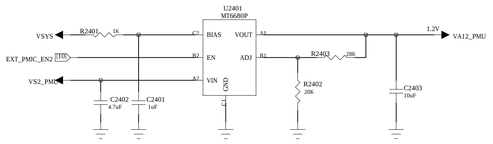
		SCALE: <Scale>	SHEET: 33

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

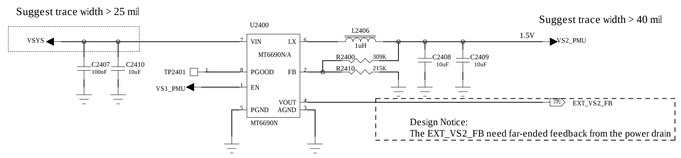
LDO for VA12



0.5V*(1+R2403/R2402)

Ext. Bulk for VS2

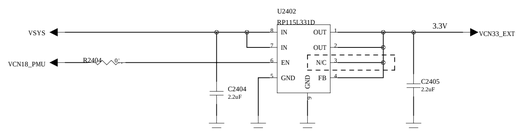
For Low Power Perfemance



0.6V*1+R2400/R2410)

LDO for VCN33

Suggest trace width > 25 mil

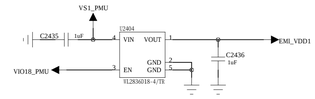


Schematic design notice of "28_POWER_ThirdParty-Power"

Note 28-1:	VA12 Layout placement please close to AP
Note 28-2:	VS2 Buck Layout placement please close to PMIC MT6357
Note 28-3:	VCN33 LDO Layout placement please close to MT6631

LPDDR4X VDD1 1.8V LDO

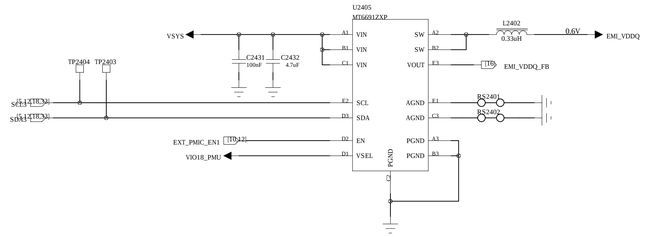
Suggest trace width > 20 mil



Ext. buck LP4/4X VDDQ 1.125V/0.6V

If use LPDDR4, NC U2802 and peripheral components
MT6691ZXP/A / Ext. buck LP4X VDRAM(VDDQ)
I2C address: 0x50 (Write:0xA0, Read:0xA1)

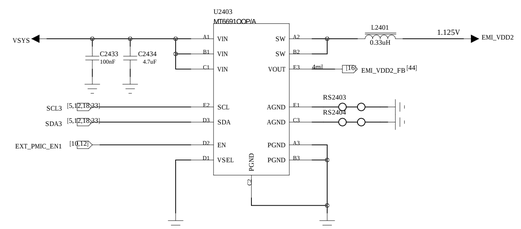
Suggest trace width > 25 mil



Ext. buck LP4/4X VDD2 1.125V

MT6691OOP/A / Ext. buck LP4X VDRAM (VDD2)
I2C address: 0X57 (Write:0xAE, Read:0xAF)

Suggest trace width > 50 mil



Schematic design notice of "28_POWER_ThirdParty-Power"

Note 28-1:	VA12 Layout placement please close to AP
Note 28-2:	VS2 Buck Layout placement please close to PMIC MT6357
Note 28-3:	VCN33 LDO Layout placement please close to MT6631
Note 28-4:	MT6691ZXP/A and MT6691OOP/A Buck Layout Placement please close to LPDDR4X
Note 28-5:	U2810 LDO Layout Placement Please close to LPDDR4X VDD1 power ball
Note 28-6:	For EMI_VDD2_FB and EMI_VDDQ_FB, please follow MMD rule

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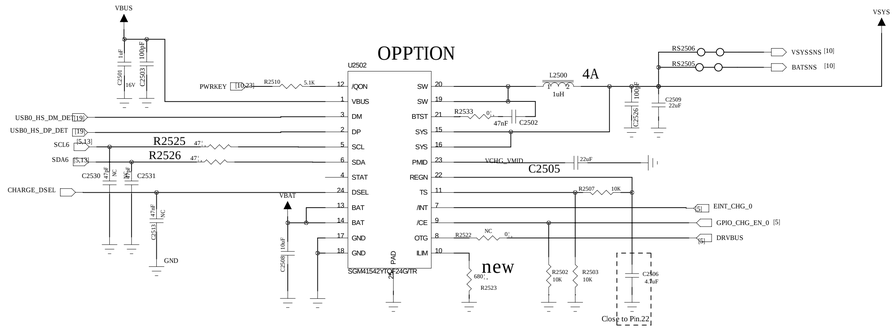
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: MT6765	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: P410	SIZE: D
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: P410	REV: V1.0
		SCALE: <Scale>	SHEET: 32 33

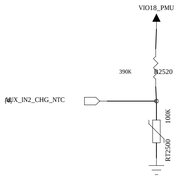
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

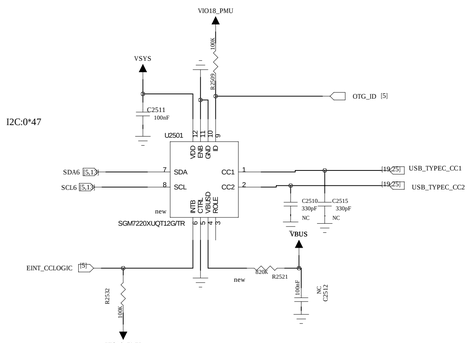
CHARGE_9V*2A

I2C ADDR:0x6B

L2501,L2502,R2501,R2504 CLOSE TO Connector!!!







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			TITLE:	MT6765	
DRAWN: Marshall	DATED: 2018-09-22A		CODE: P410	SIZE: D	DRAWING NO: P410 / REV: V1.0
CHECKED: <Checked By>	DATED: <Checked Date>				
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

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CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: MT6765	
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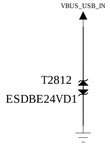

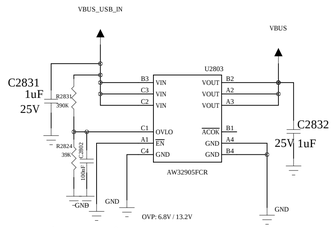

Vbus in:4.75V to 10.5V

µ÷½ÚOVPµçÑ¹£»13.2V

DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno			
		TITLE: MT6765			
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: P410	SIZE: D	DRAWING NO: P410	REV: V1.0
QUALITY CONTROL: <QC By>	DATED: <QC Date>				
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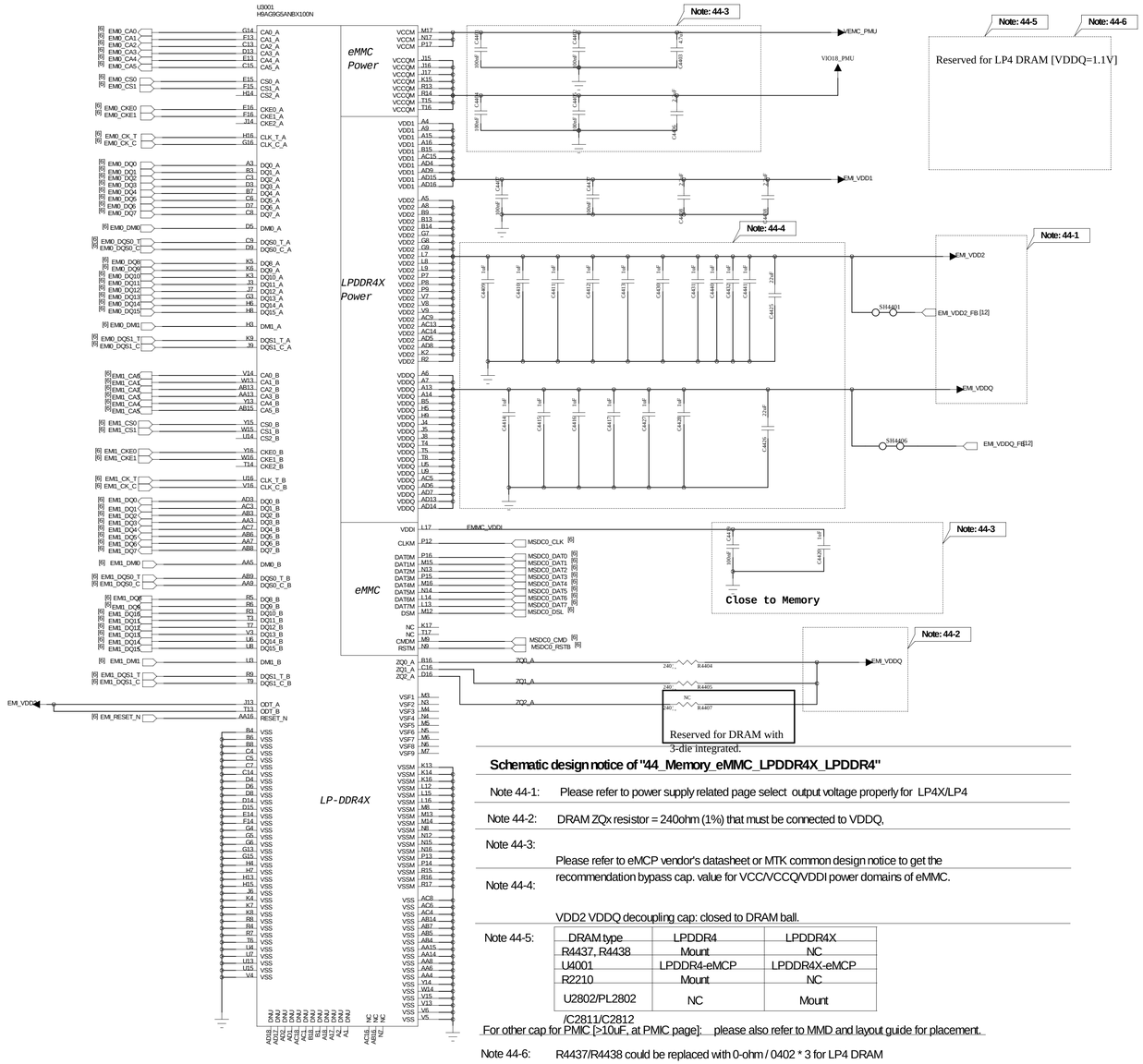


Schematic design notice of "44_Memory_eMMC_LPDDR4X_LPDDR4"

Note 44-1: Please refer to power supply related page select output voltage properly for LP4X/LP4

Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ.

Note 44-3:

Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

Note 44-4:

VDD2 VDDQ decoupling cap: closed to DRAM ball.

Note 44-5:

DRAM type	LPDDR4	LPDDR4X
R4437, R4438	Mount	NC
U4001	LPDDR4-eMCP	LPDDR4X-eMCP
R2210	Mount	NC
U2802/PL2802	NC	Mount

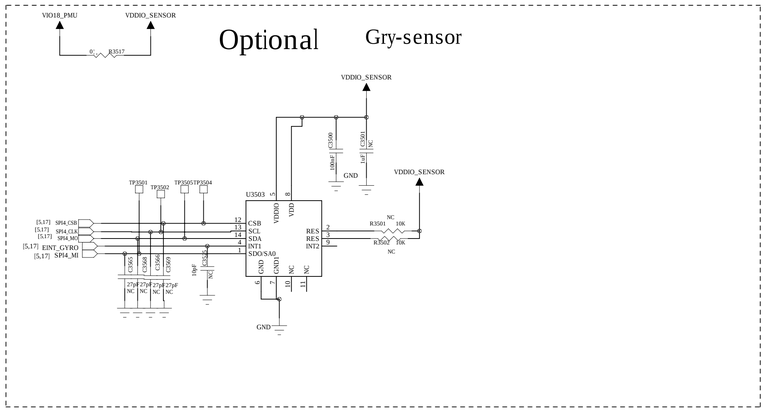
/C2811/C2812

For other cap for PMIC [>10uF, at PMIC page]: please also refer to MMD and layout guide for placement.

Note 44-6: R4437/R4438 could be replaced with 0-ohm / 0402 * 3 for LP4 DRAM

DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno	
		TITLE: MT6765	
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: P410	SIZE: D
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: P410	REV: V1.0
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 16 33

G+Gyro Sensor

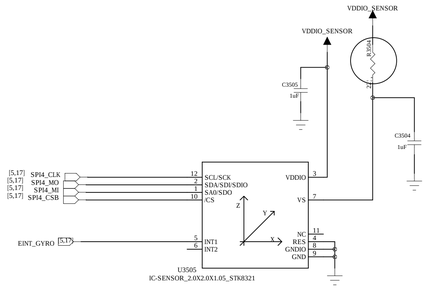


Note: 77-4

Accelerometer- Sensor

0824: Check SCH

	SA0=0	SA0=1
STK8321	0X0F	0X1F
LIS2DOC	0X30W/0X31R	0X32W/0X33R



E-Compass

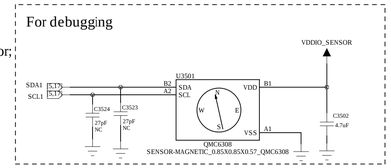
E-Compass

QMC6308	0x2C//58H(W)/59(R)
AKM09918	0x0C

Note: 77-1

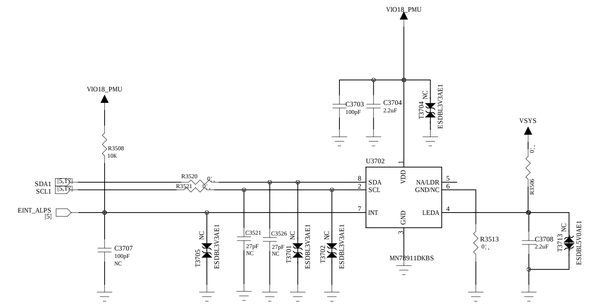
zwt0831: near P/L sensor;

Note: 77-6



Proximity Sensor charge

STK33562	0¡Á46



Baro Sensor

Baro(BMP380) I2C address : 7h'76 (SDO pin tied to GND)

Schematic design notice of "77_PERI_SENSORS_MEMs_ALS/PS" page.

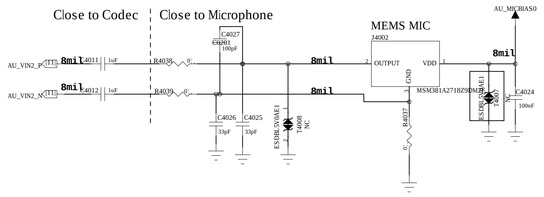
Note 77-1:	[M sensor] Keep a minimum distance of 15mm from power ICs / PCB traces of more than 100mA / magnet component. Check HW design notice for more detail
Note 77-2:	[A+G] For optmized GPS performance, please check HW design notice for Sensor selection guide
Note 77-3:	[A+G] MUST use SPI for optmized sensor hub performance **DO NOT USE i2C**
Note 77-4:	[A+G] Suggest choose sensor support FIFO watermark interrupt otherwise we cannot support Hifi-sensor, daydream VR. And Sensor-location accuracy will become worse.
Note 77-5:	[Baro] Reserve Baro sensor for LPPe feautre (Must for North America Operator / NA SKU)
Note 77-6:	DO NOT share Sensor hub i2C to other non-SCP device
Note 77-7:	Interrupt pin of MEMS sensor must be assign to ball EINT[12:0]

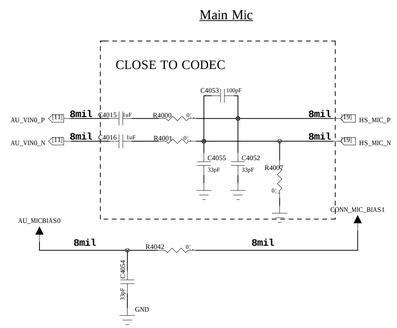
REVISION RECORD

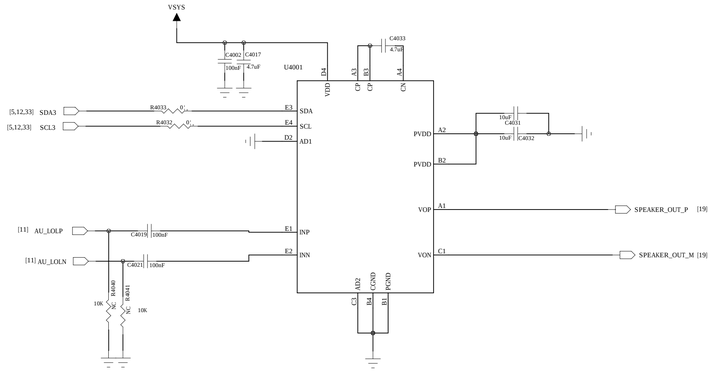
LTR	ECO NO:	APPROVED:	DATE:

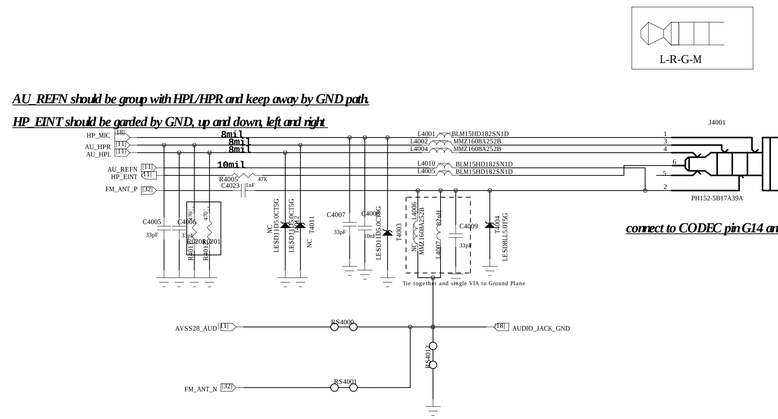
DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: MT6765	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: P410 / SIZE: D / DRAWING NO: P410 / REV: V1.0	
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 33

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



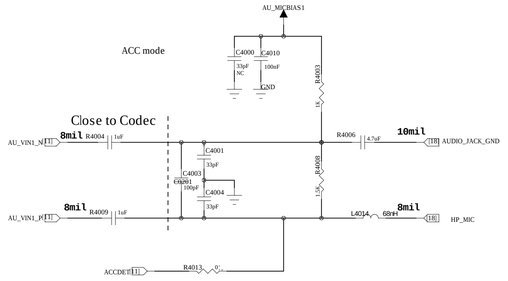






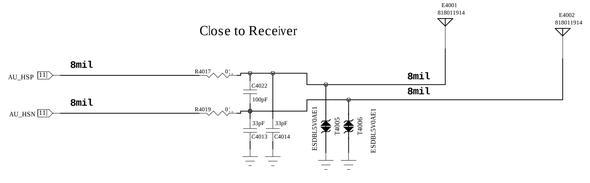
COBY-P352CE

Headset Mic



	DCC	ACC
R4004	0R	1uF
R4009	0R	1uF
R4003	NC	1K
R4008	NC	1.5K
R4002	2.5K	NC
R4006	0R	4.7uF
R4013	NC	0R

Handset Receiver

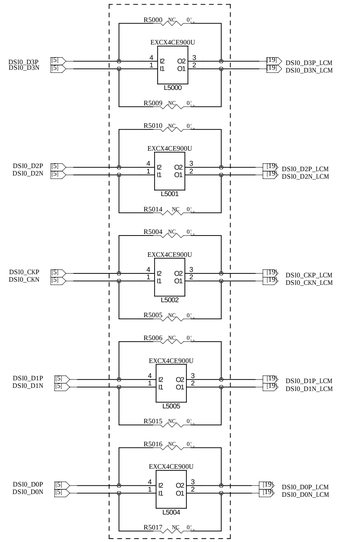


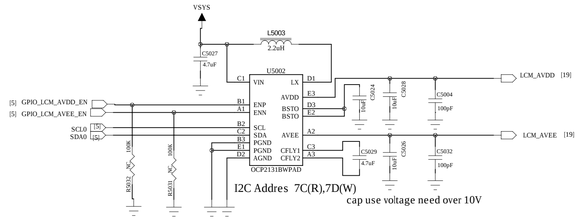
COBY-P352CE

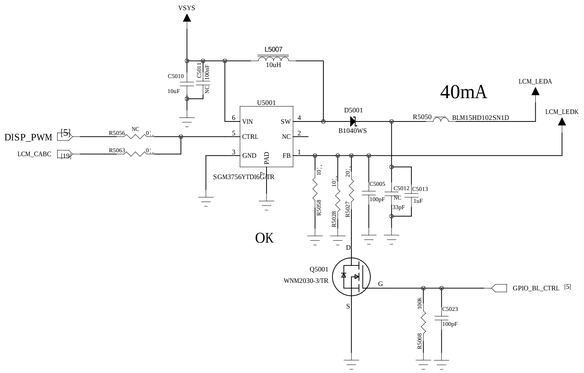
COMPANY: Tinno					
TITLE: MT6765					
DRAWN: Marshall	DATED: 2018-09-22A				
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: P410	SIZE: D	DRAWING NO: P410	REV: V1.0
QUALITY CONTROL: <QC By>	DATED: <QC Date>				
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 18 33	

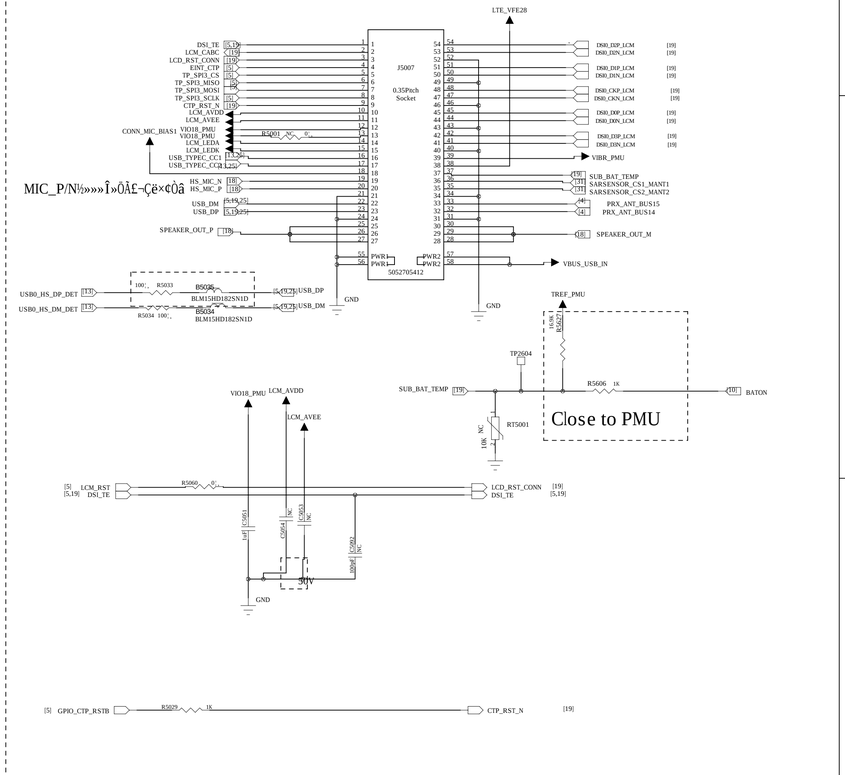
COBY-P352CE

LCD Connector

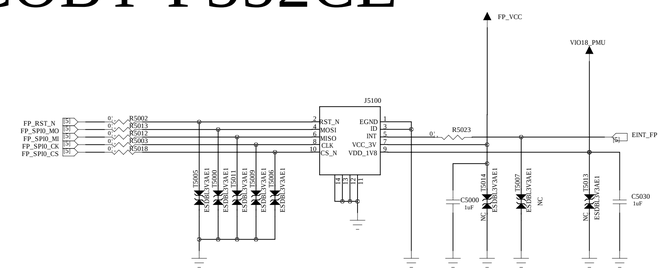






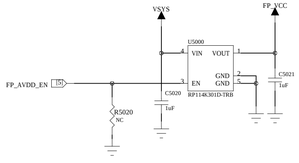


COBY-P352CE



Fingerprint Connector

1	GND
2	RST
3	ID(GND)
4	MOSI
5	INT
6	MISO
7	VDD2V8
8	CLK
9	DOVDD1V8
10	CS
11	GND
12	GND
13	GND
14	GND



DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: MT6765	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: P410	SIZE: D
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: P410	REV: V1.0
		SCALE: <Scale>	SHEET: 33

REVISION RECORD

LTR	ECO NO:	APPROVED:	DATE:

FRONT-CAMERA
8M: 4 lane

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

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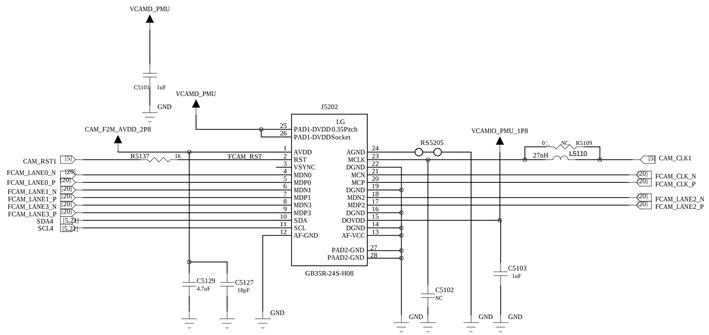
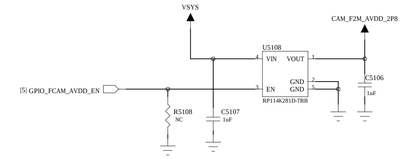
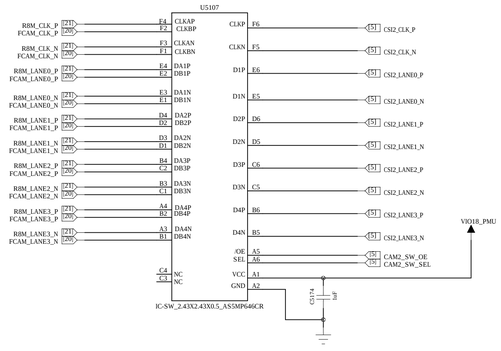
	AVDD	DVDD	DOVDD	ID	I2C
S5K4H7YX03	2.7~2.9 V(2.8V)	1.14~1.26V(1.2V)	1.7~1.9V(1.8V)	NC	0X20(W)/0X21(R)



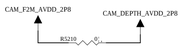




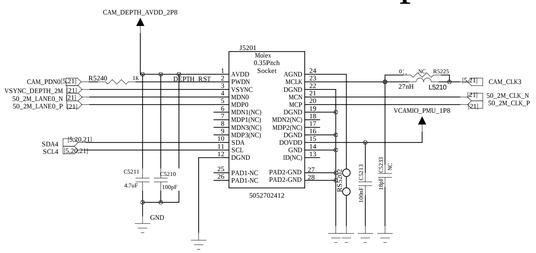
SEL	CE	function	
LOW	LOW	MIPI TO A	
HIGH	LOW	MIPI TO B	
X	HIGH	clock and data ports high impedance	

I2C Address

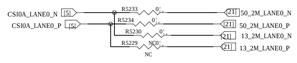
DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno	
		TITLE: MT6765	
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: P410	SIZE: D
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: P410	REV: V1.0
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 30 33

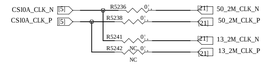


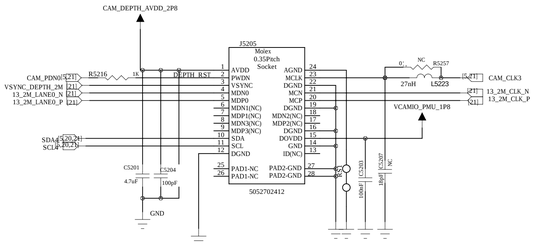
2M FF-Depth Side-¹²ÓÃ8MÎ»ÖÃ



R12,R17,R22,R25 Close to J5201 !!!!







2M FF-Depth Side-50M

Camera LDO

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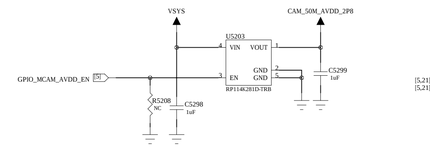
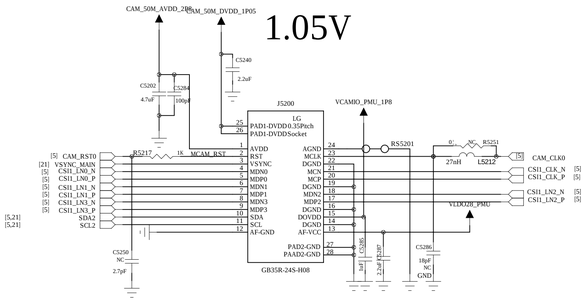
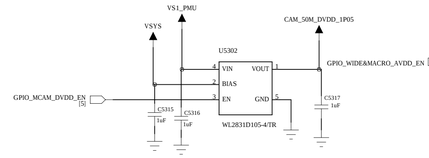
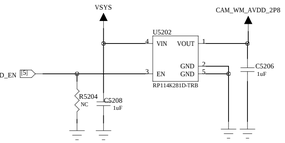
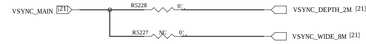
Main-CAMERA 50M/13M





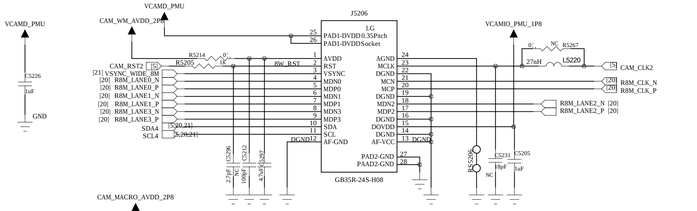


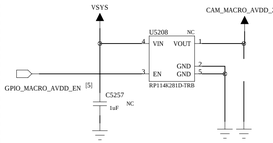


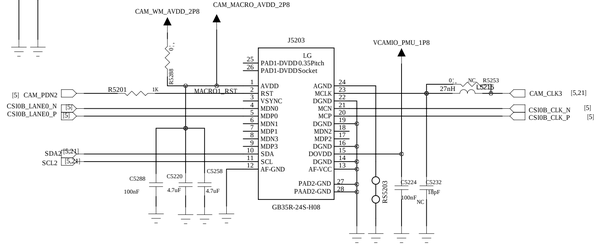


8M: WIDE

	AVDD	DVDD	DOVDD	ID	I2C
S5K4H7YX03	2.7~2.9 V(2.8V)	1.14~1.26V(1.2V)	1.7~1.9V(1.8V)		0X5A(W)/0X5B(R)

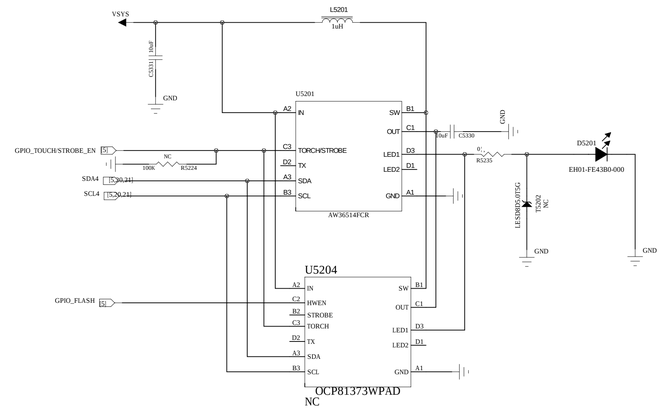






2M FF-Macro

Rear CAM Flash LED

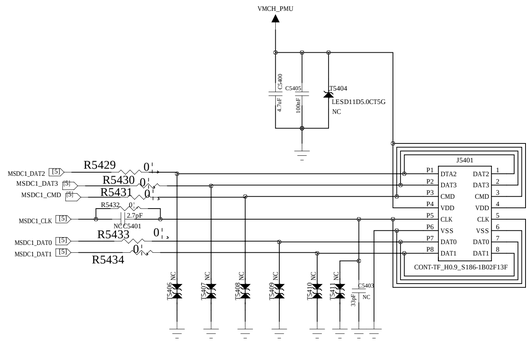


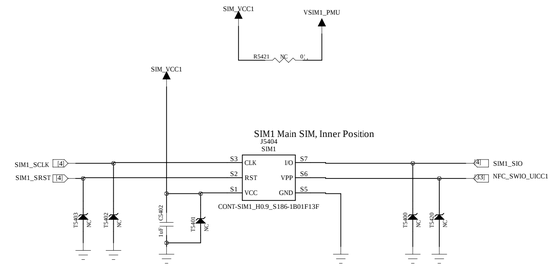
	AVDD	DVDD	DOVDD	I2C
GC5035	2.7V-3.0V	1.15V-1.3V	1.7V-3.0V	W:0x7E R:0x7F

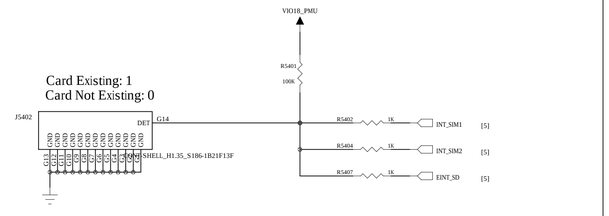
DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: CAMERA MT6765	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: P410	SIZE: D
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: P410	REV: V1.0
		SCALE: <Scale>	SHEET: 31 33

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

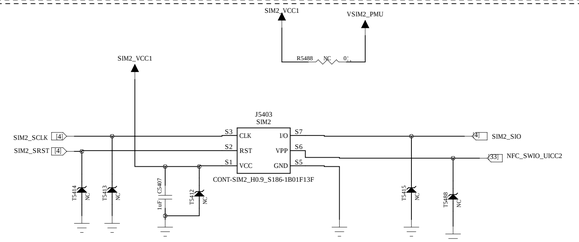
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:







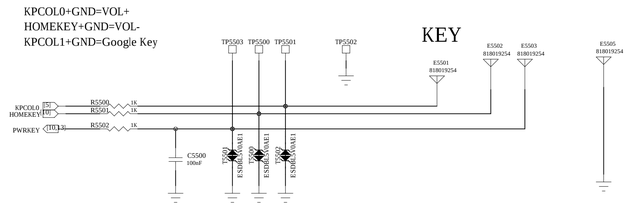
SIM Card 2



DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno	
		TITLE: MT6765	
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: P410	SIZE: D
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: P410	REV: V1.0
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 32 33

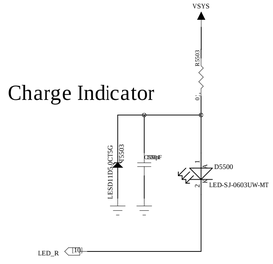
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

MP Test point



COBY-P720AE

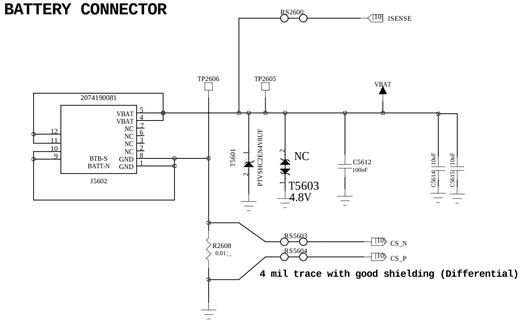
Charge Indicator



COMPANY: Tinno					
TITLE: MT6765					
DRAWN: Marshall	DATED: 2018-09-22A	CODE: P410	SIZE: D	DRAWING NO: P410	REV: V1.0
CHECKED: <Checked By>	DATED: <Checked Date>				
QUALITY CONTROL: <QC By>	DATED: <QC Date>				
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 28 33	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

BATTERY CONNECTOR



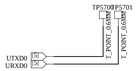
DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno			
		TITLE: MT6765			
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: P410	SIZE: D	DRAWING NO: P410	REV: V1.0
QUALITY CONTROL: <QC By>	DATED: <QC Date>				
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 34 33	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Debug Test Point

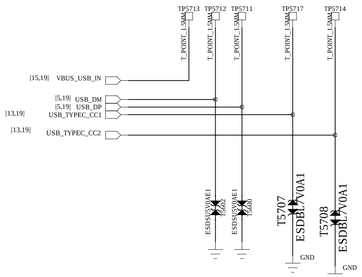
RAM dump

UART



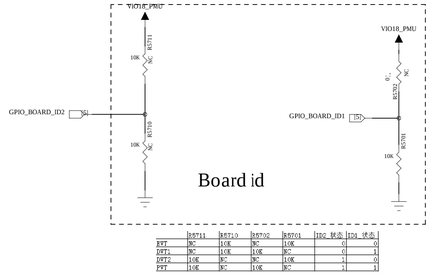
Fixture Test Point

USB



Batery
Refer to Page 26

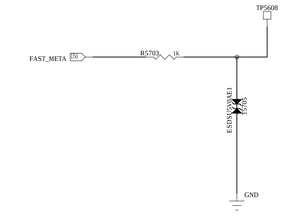
CTP
Refer to Page 56



	R5711	R5710	R5702	R5701	ID2 电压	ID1 电压
EVT	NC	10K	NC	10K	0	0
DVT1	NC	10K	10K	NC	0	1
DVT2	10K	NC	NC	10K	1	0
PVT	10K	NC	10K	NC	1	1

Key
Refer to Page 55

Fast META



Mark

shielding can

BB

PDN

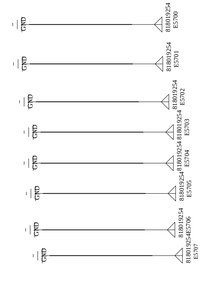
RF

4G_PA

WCN

Metal Grounding

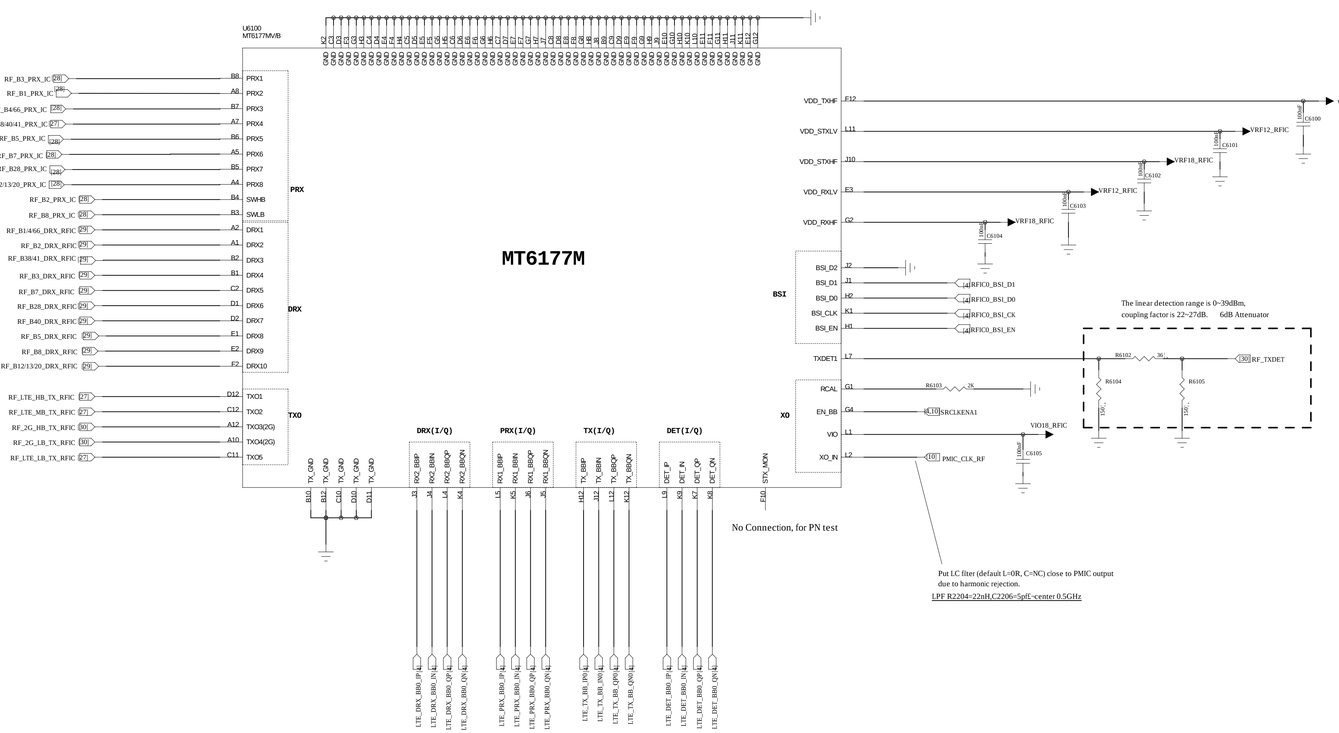
Top

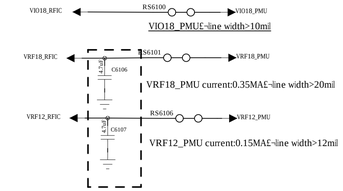


Bottom

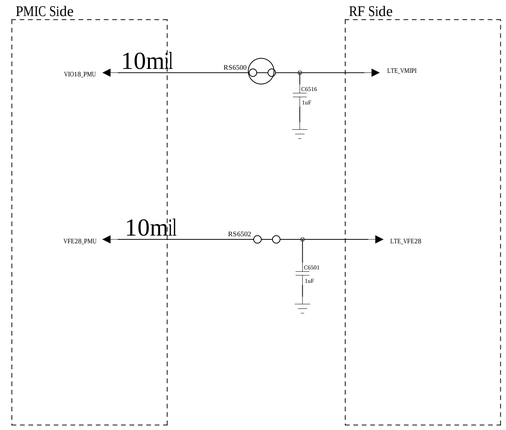
DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno	
		TITLE: MT6765	
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: P410	SIZE: D
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: P410	REV: V1.0
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 35 33

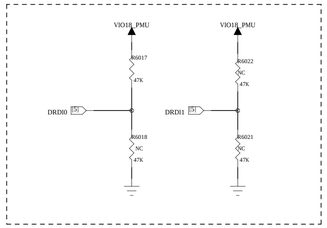
REVISION RECORD			
LTR:	ECO NO:	APPROVED:	DATE:





PMIC to RF power net transfer





DRDI

SKU	R6017	R6018	R6022	R6021
EU	47K	NC	NC	NC
LA	NC	47K	NC	NC
AP	NC	NC	47K	NC

DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno			
		TITLE: MT6177			
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: P410	SIZE: D	DRAWING NO: P410	REV: V1.0
QUALITY CONTROL: <QC By>	DATED: <QC Date>				
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 26 33	

Main RF TRX Switch

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

CO-lay	C6243	C6247
B4	NC	33pF
B41	33pF	NC

Band	RX
B40(pin37)	TRX1(pin41)
B41(pin39)	TRX2(42) pin33,pin35

CO-lay	C6248	C6245	C6239	C6242
B40_HBRX	NC	33pF	33pF	NC
B40_TXM	NC	33pF	NC	33pF
B28B	33pF	NC	NC	NC

VPA_PMU width>60mil;(min width=20mil,length<=100mils)
VCC1>=10mil;VCC2>=50mil
VPA_PMU PA side load C 6.2UF+-5%

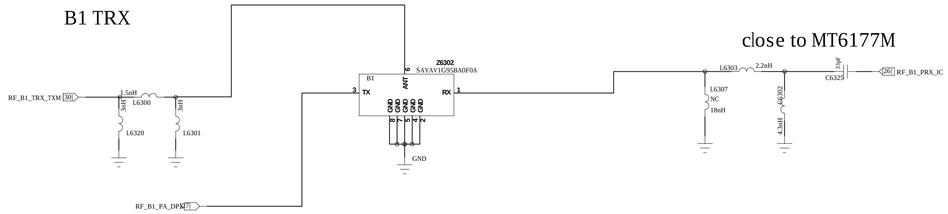
Close to PA

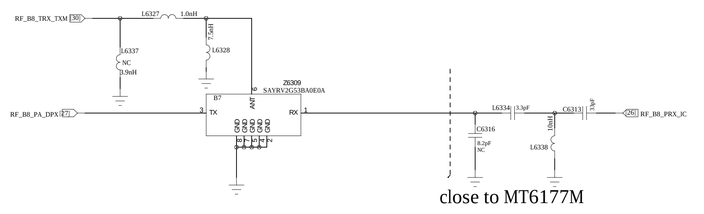
Thermistor / To sense board level temperature

Thermister have to be placed as close to B7&B1 PA as possible, routing with ground guard.
RT900 close to PA , and located in the same layer

close to MT6177M

COMPANY:	Tinno		
TITLE:	MT6765		
DRAWN: Marshall	DATED: 2018-09-22A	CODE: P410	SIZE: D
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: P410	REV: V1.0
QUALITY CONTROL: <QC By>	DATED: <QC Date>	SCALE: <Scale>	SHEET: 27 33
RELEASED: <Released By>	DATED: <Release Date>		





REVISION RECORD			
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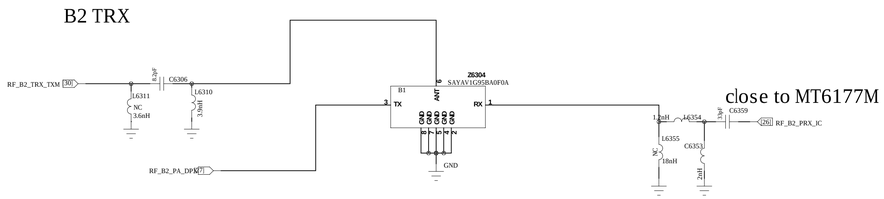
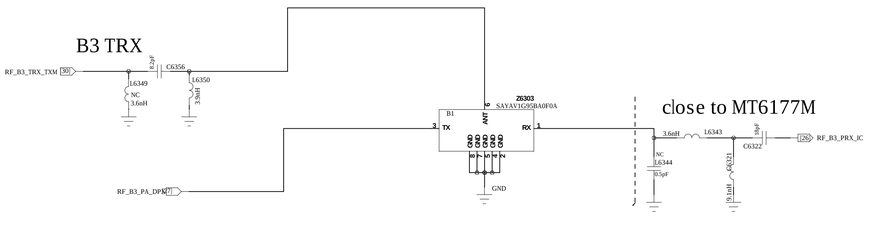
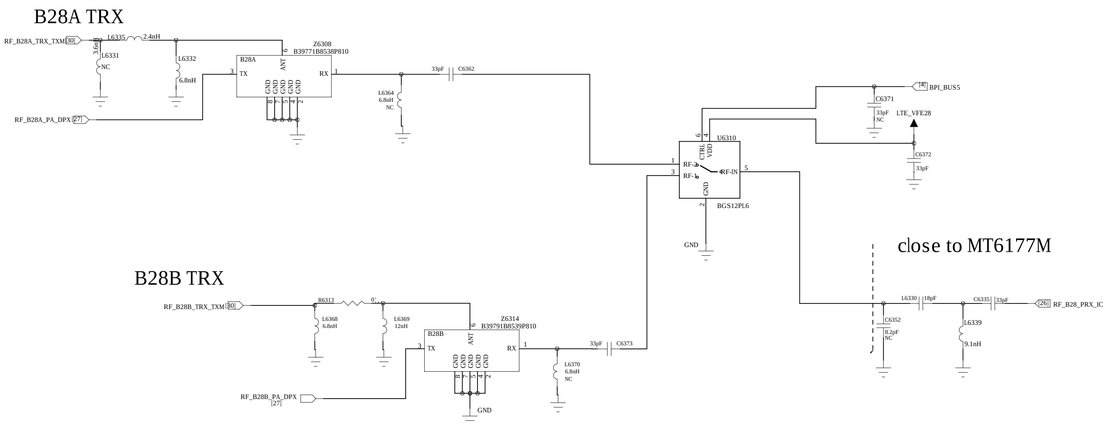
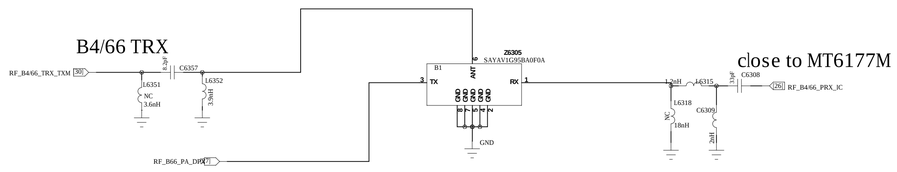
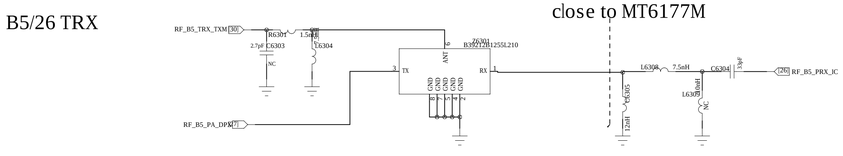
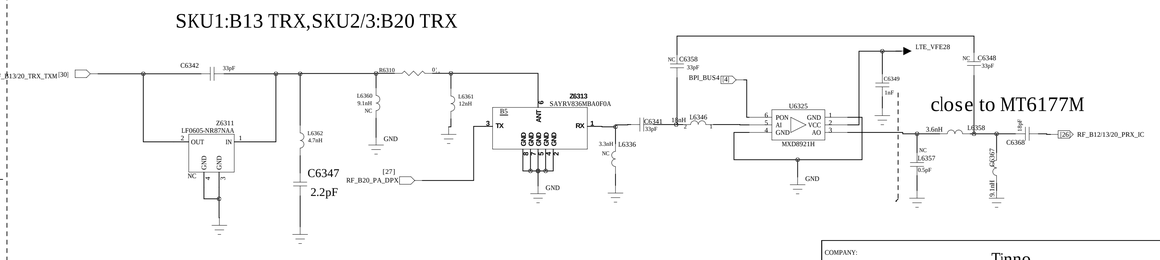


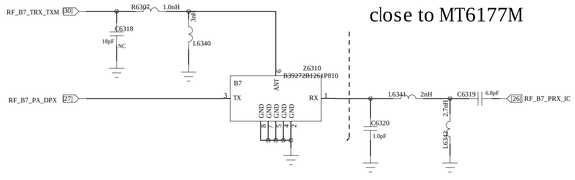








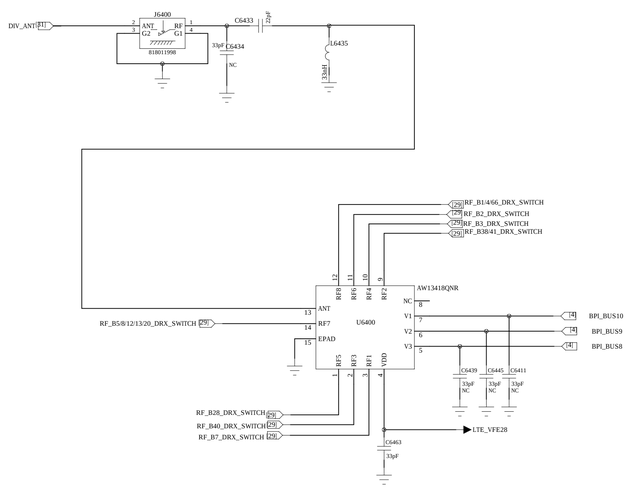


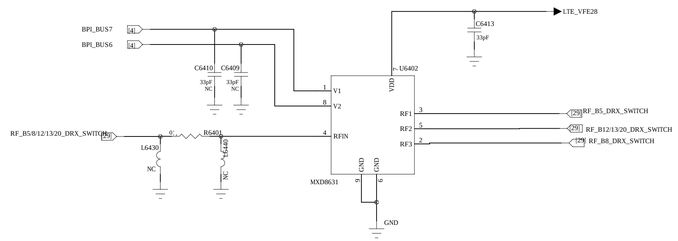


COMPANY:	Tinno
TITLE:	
DRAWN: Marshall	DATED: 2018-09-22A
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

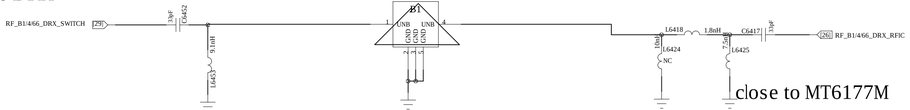
CODE:	SIZE:	DRAWING NO:	REV:
P410	D	P410	V1.0

SCALE: <Scale> SHEET: 28 33





B1/4/66 DRX



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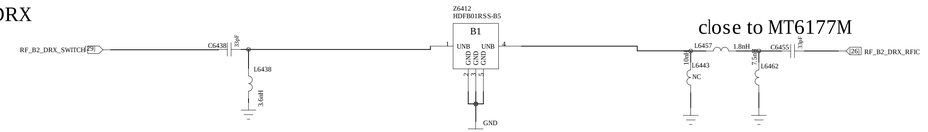

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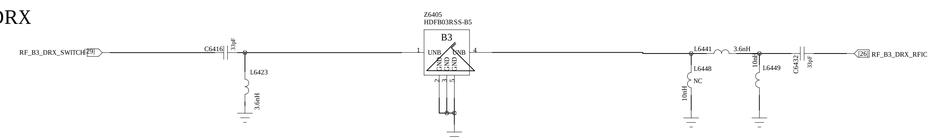
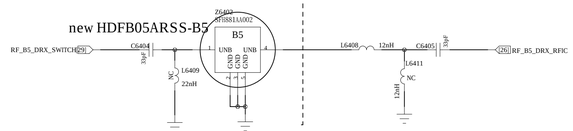
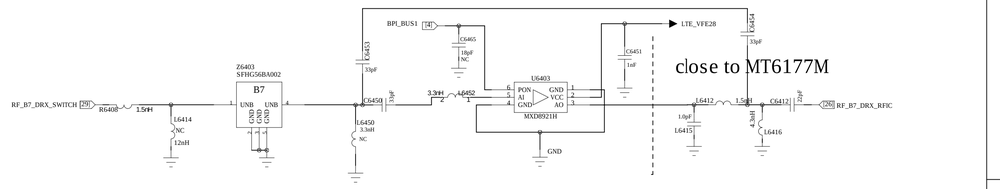
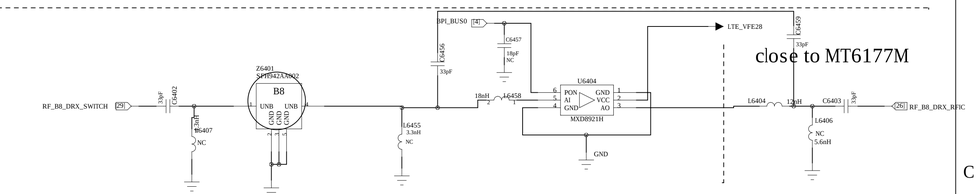




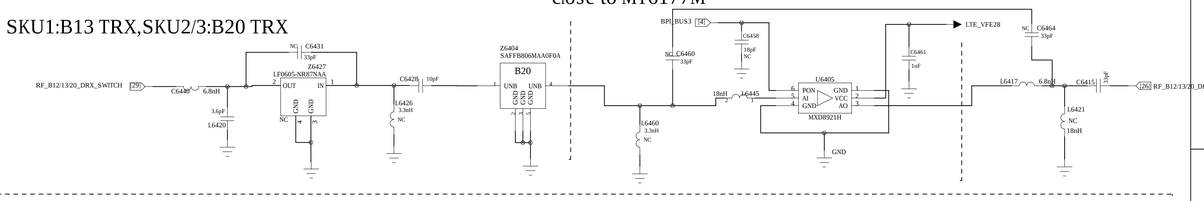
B7 DRX



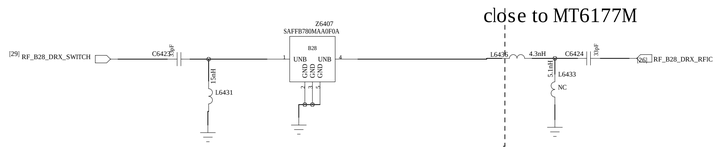
B8 DRX



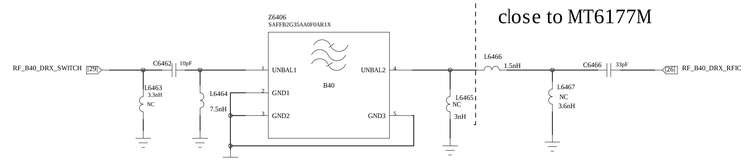
SKU1:B13 TRX,SKU2/3:B20 TRX



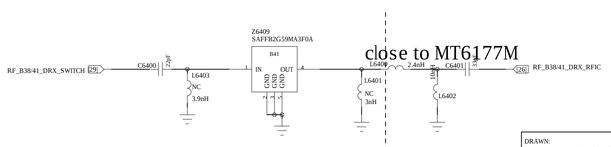
B28 DRX



B40 DRX



B41 DRX



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DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: MT6765	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: P410	SIZE: D
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: P410	REV: V1.0
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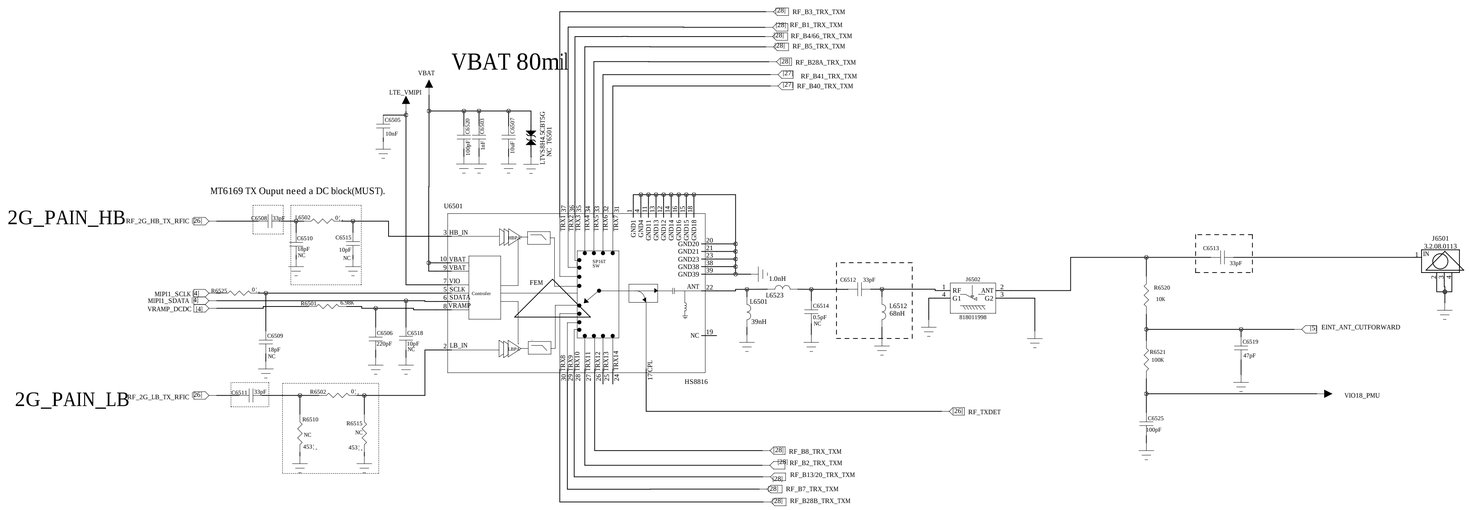

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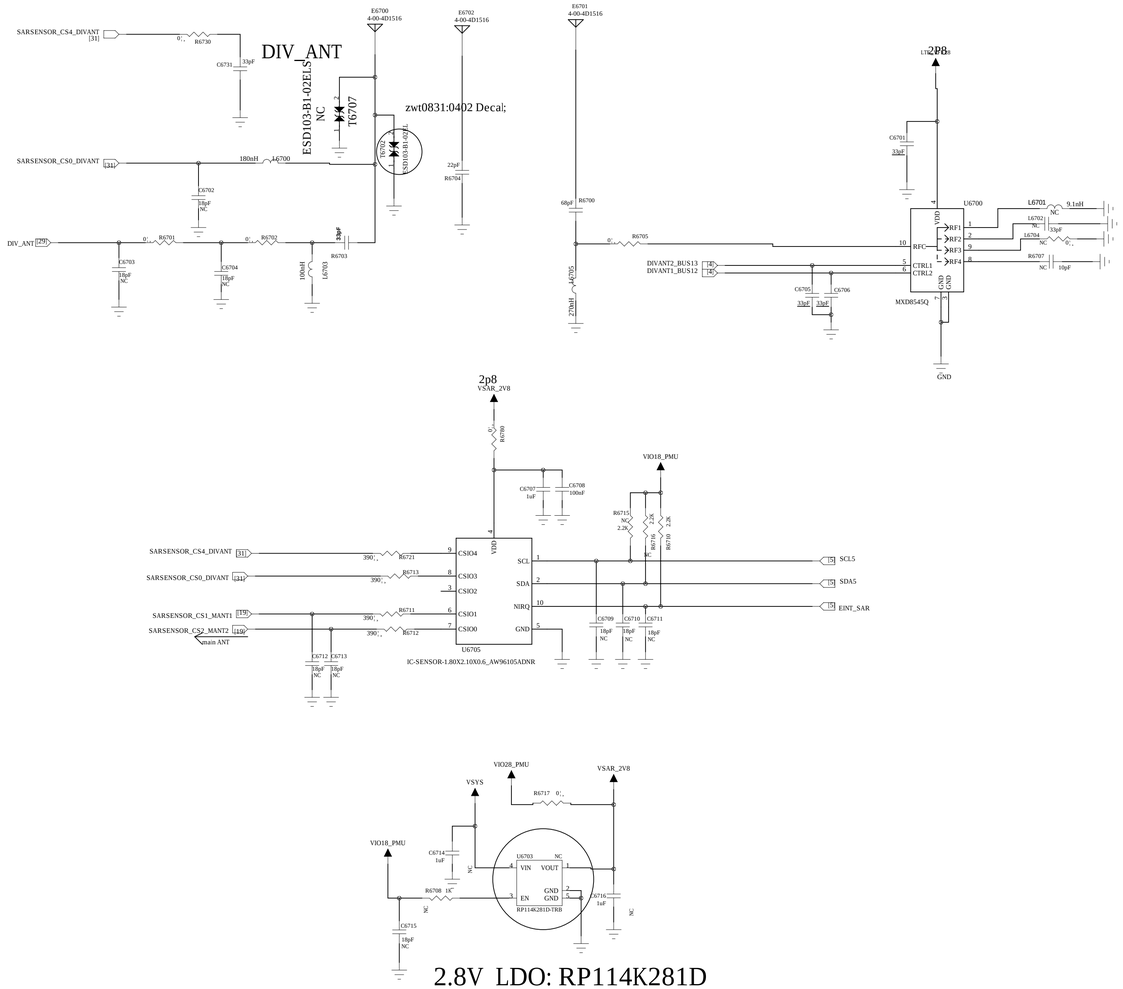

2.8V LDO: RP114K281D

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CHECKED: <Checked By>	DATED: <Checked Date>	CODE: P410	SIZE: D
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RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 33

WCN ANT & Filter

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Close to Antenna

Close to MT6631

GPS xLNA

Close to ANT

LNA selected

matching value depends on

MT6631N

DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: RF_PWR_ET_APT	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: P410	SIZE: D
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: P410	REV: V1.0
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REVISION RECORD			
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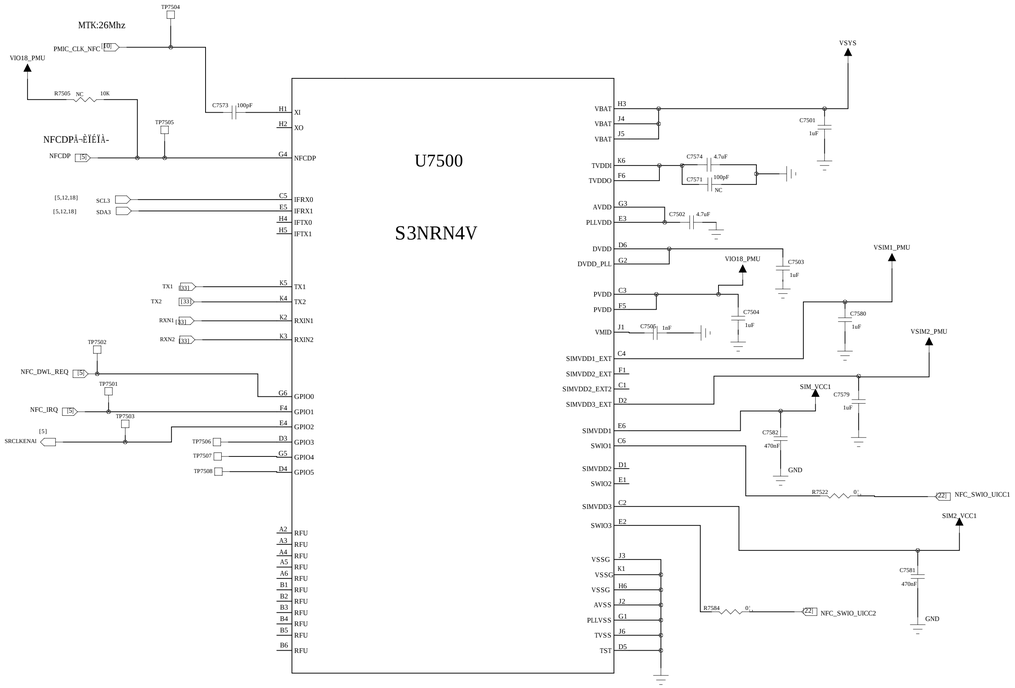

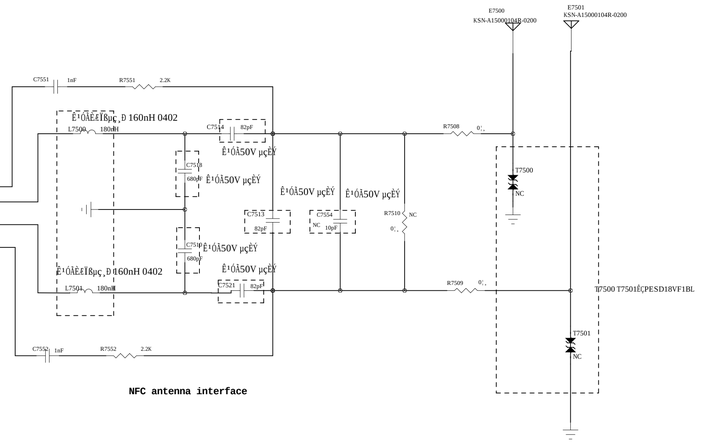

NFC antenna interface

DRAWN: Marshall	DATED: 2018-09-22A	COMPANY: Tinno	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: MT6765	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: P410	SIZE: D
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: P410	REV: V1.0
		SCALE: <Scale>	SHEET: 33 33