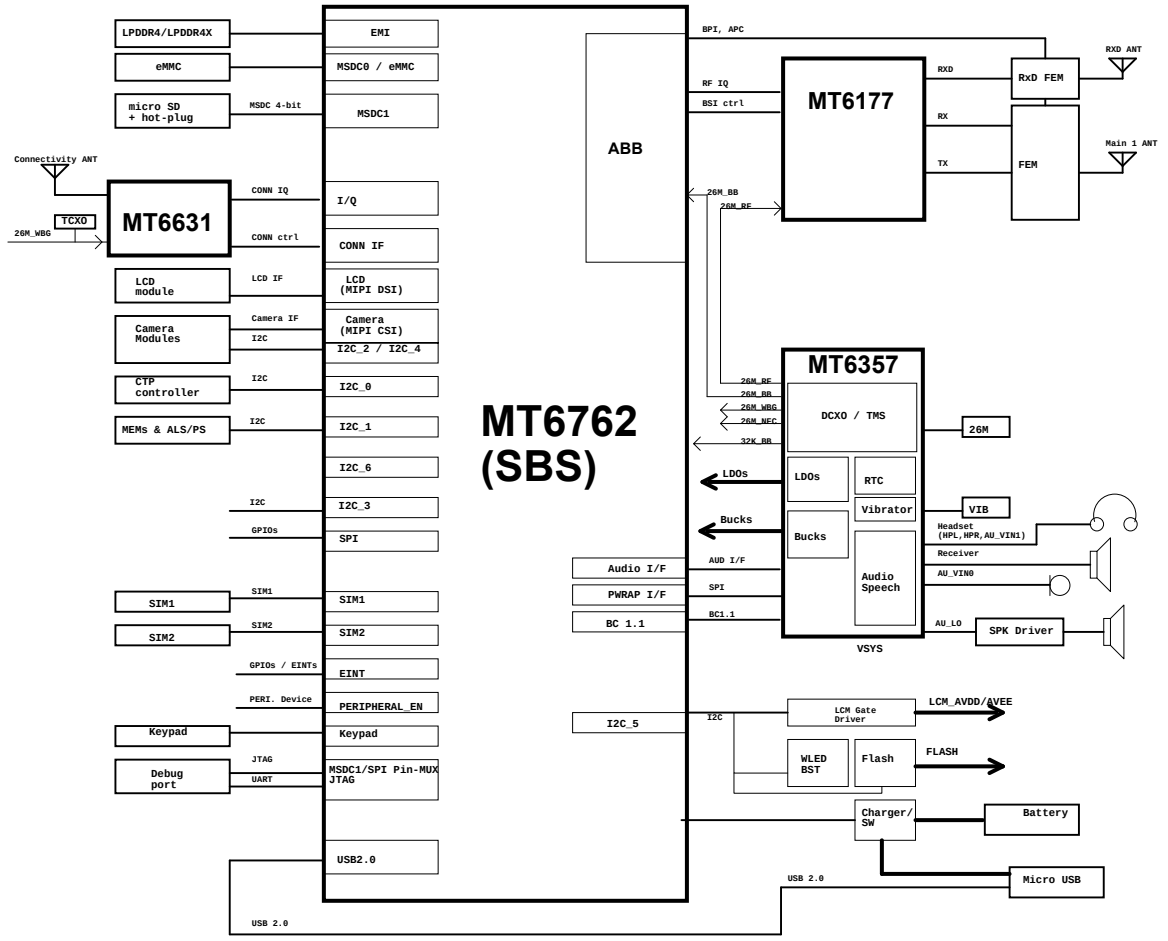
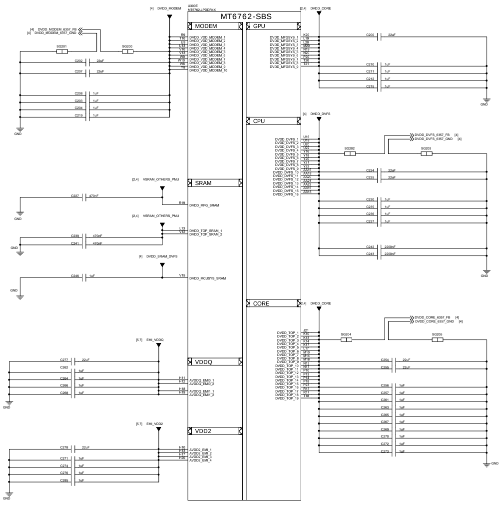
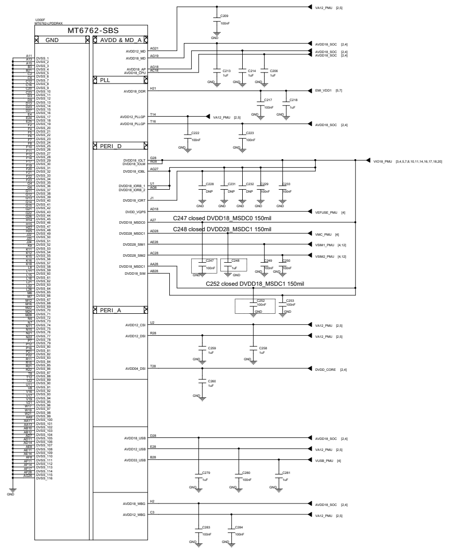


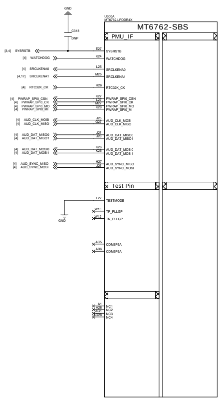
ONTIM Technologies Ltd.		ontim
Title: M6200		Size: A3
Functionality: BB Block Diagram		Ver: P0
Date: Friday, July 24, 2020	Sheet 1 of 24	

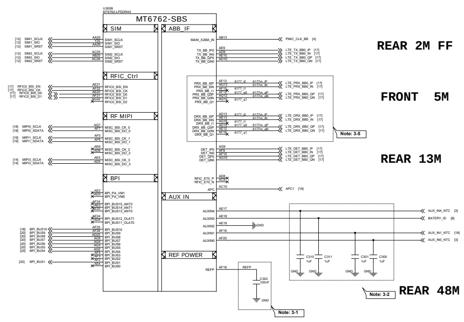
base MT6762 ref-SCH

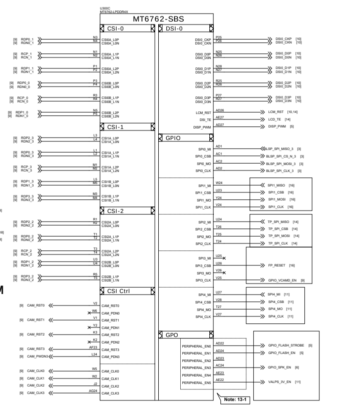


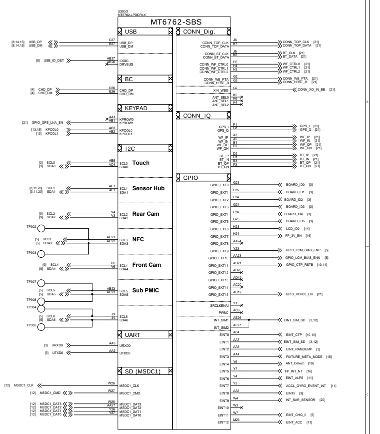


base MT6762 ref-SCH









Schematic design notice of "12_BB_1" page.

Note 3-1: The de-coupling cap. for REFP (AF18 ball) have to be placed as close to BB as possible.

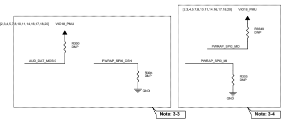
Note 3-2: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

Note 3-3: "PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pin to select which interface will be the JTAG pin out.

	PWRAP_SPI0_CSN	AUD_DAT_MOSI0	JTAG Function	
	default=PU	default=PD	AP_JTAG	MD_JTAG
USE CASE	HI	LO	N/A	N/A
	HI	HI (by ext. PU)	SPI0+EINT8	SPI1+SPI3
	LO (by ext. PD)	LO	SPI0+EINT8	N/A
	LO (by ext. PD)	HI (by ext. PU)	MSDC1	N/A

Note 3-4: PWRAP_SPI0_MI / PWRAP_SPI0_MO is DDR type feature in bootstrap

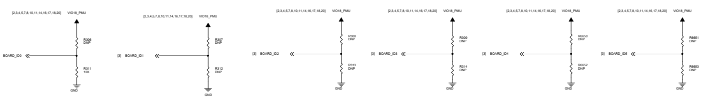
	PWRAP_SPI0_MI	PWRAP_SPI0_MO	Booting interface	
	default=PU	default=PD	DDR	MSDC0 pin mux
USE CASE	LO (by ext. PD)	LO	LPDDR3	follow LPDDR3 Ref SCH.
	LO (by ext. PD)	HI (by ext. PU)	N/A	N/A
	HI	LO	LPDDR4X	follow LP4X/LP4 Ref SCH.
	HI	HI (by ext. PU)	LPDDR4	follow LP4X/LP4 Ref SCH.

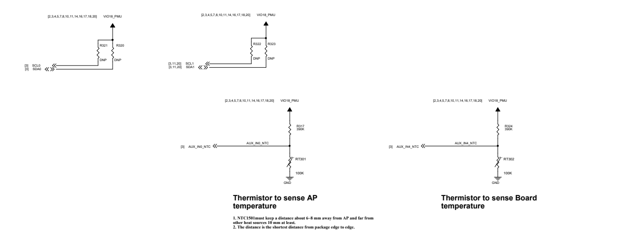


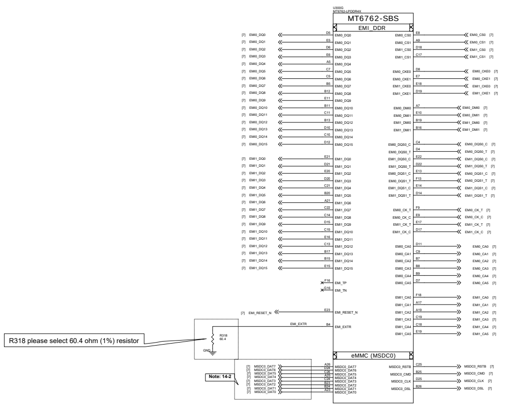
Note 12-5: Please set unused IQ pins in NC

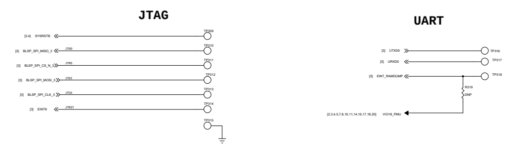
Schematic design notice of "13_BB_2" page.

Note 13-1: The enable pin of acoustic or optoelectronic devices (e.g. SPK AMP/Backlight/Charger OCP/OVP) suggest to use Peripheral_EN[0:5]
If use other GPIOs as enable pin, suggest to reserve 0201 NC to GND

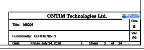




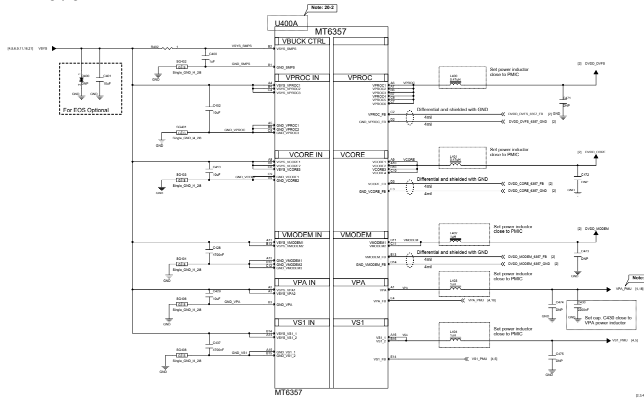


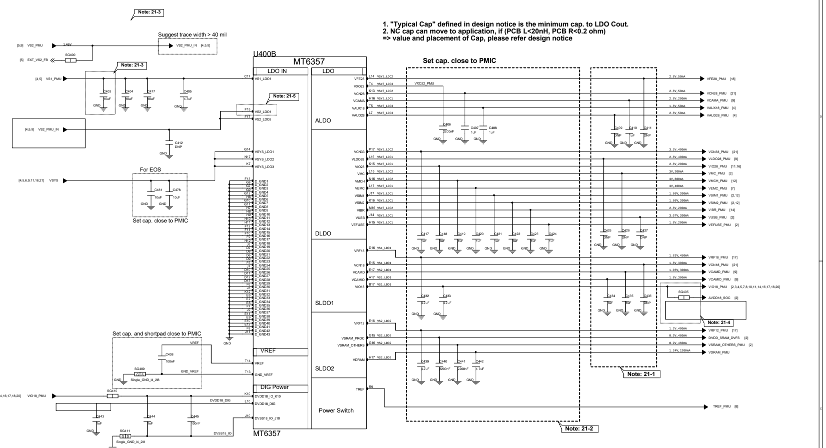


Note 14-2: Please check eMCP LP3 and eMCP LP4X pin mux



base MT6762 ref-SCH





Schematic design notice of "20_POWER_MT6357_Buck"

Note 20-1: C2040, please choose 0402 size

Note 20-2: PMIC Part number notice for MT6765/62/61 platform

MTK Platform	PMIC
MT6765 / 62	MT6357CRV
MT6761	MT6357MRV

Schematic design notice of "21_POWER_MT6357_LDO"

Note 21-1: If these power trace can meet LDO layout constraint, these CAP can be NC or removed. Please refer to MT6357 design notice.

Note 21-2: Output cap range please follow MT6357CRV LDO design notice

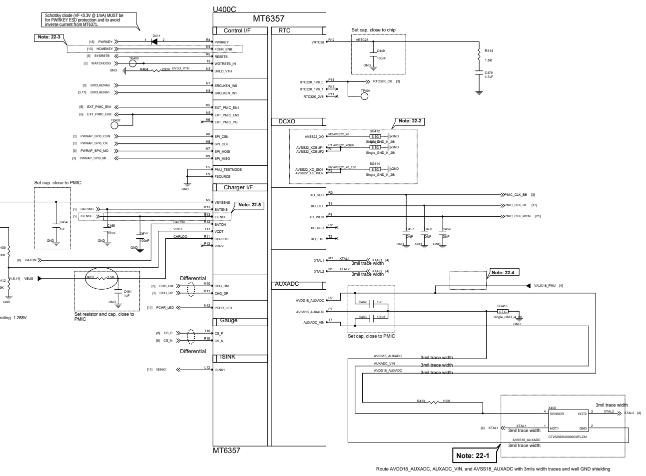
Note 21-3: Ext Buck BOM option

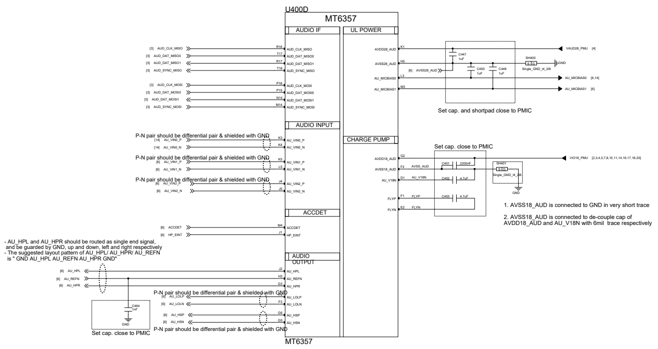
	Ext. buck option	
	w/ EXT VS2 Buck	w/o EXT VS2 Buck
C403	10uF(0402)	22uF(0603)
R420	0-ohm , 0603	NC
R401	NC	0-ohm , 0603

Note 21-4: Please set SG405 and SG407 close to C433, making star connection among VIO18_PMU, AVDD18_SOC, and EMI_VDD1 near to LDO cap. C433

Please also refer to MT6357 design notice for further detail design information

Note 21-5: Please connect VS2_LDO1(F15) to VS1_PMU if voltage applied to VCAMD(E17) >= 1.3 V





Schematic design notice of "22_POWER_MT6357-IF"

Note 22-1: Please implement 2520 & 2016 Size TMS PCB co-layout.
Please refer to MT6762_MT6357 Co-Clock Design Notice for co-layout guide

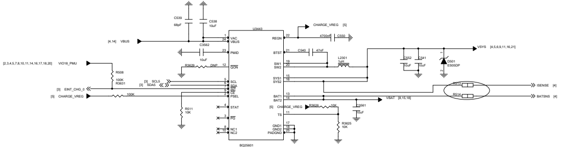
Note 22-2:
1. Please Connect P1 and R1 ball first and then to GND
2. Please Connect P2 and N2 ball first and then to GND
3. Please connect DCXO GND to main GND by independent L1-2 GND via.; DO NOT connect it through L1 GND

Note 22-3: Let floating if disable HOMEKEY function

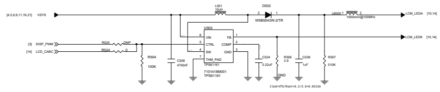
Note 22-4: Please follow MT6762_MT6357 Co-Clock Design Notice for Layout guide of VAUX18, then R411 can use 0 ohm to replace BEAD.

Note 22-5: Please connect to battery connector

Charger

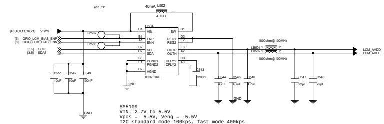


LCM Backlight LED driver



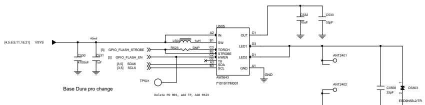
```
AW9962E
VIN: 2.7V to 5.5V
Fpwm = 10-100KHz, Dpwm= 0.3-100%, tMIN_ON=50ns
```

LCD Bias



```
SM5109
VIN: 2.7V to 5.5V
Vpos =  5.5V, Veng = -5.5V
I2C standard mode 100kps, fast mode 400kps
I2C 7bits-address: 0x3E
NT50358ACG/J
VIN: 2.5V to 5.5V
Vpos =  5.5V, Veng = -5.5V
I2C standard mode 100kps, fast mode 400kps
I2C 7bits-address: 0x3E
```

Flash LED 5V Boost



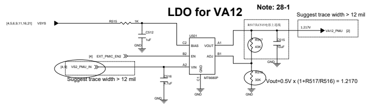
AW3643
VIN:2.7V to 5.5V
400kHz I2C address: 0X63 (Write:0xC6, Read:0xC7)

SY7806
VIN:2.7V to 5.5V
400kHz I2C address: 0X63 (Write:0xC6, Read:0xC7)

base MT6762 ref-SCH

LDO for VA12

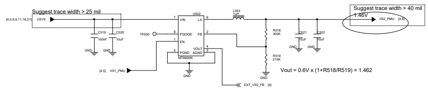
Note: 28-1



base MT6762 ref-SCH

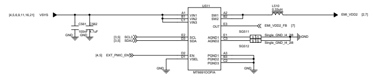
Ext. Bulk for VS2

Note: 28-2



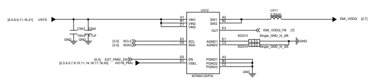
Ext. buck LPDDR4X/LPDDR4 VDRAM

MT6691OOP/A / Ext. buck LP4X/LP4 VDRAM (VDD2)
I2C address: 0X57 (Write:0xAE, Read:0xAF)

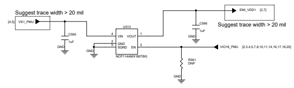


Ext. buck LPDDR4X VDDQ

MT6691ZXP/A / Ext. buck LP4X VDRAM(VDDQ)
I2C address: 0x50 (Write:0xA0, Read:0xA1)

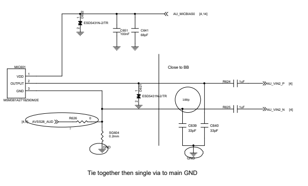


LPDDR4X/LPDDR4 VDD1 1.8V LDO

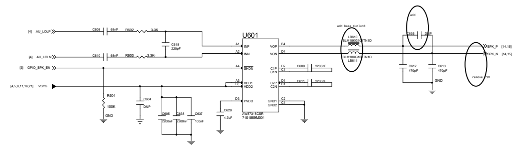


Schematic design notice of "28_POWER_ThirdParty-Power"	
Note 28-1:	VA12 Layout placement please close to AP
Note 28-2:	VS2 Buck Layout placement please close to PMIC MT6357
Note 28-3:	VCN33 LDO Layout placement please close to MT6631

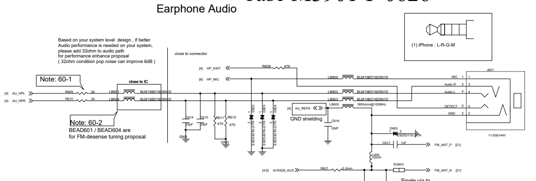
Handset 2nd Microphone



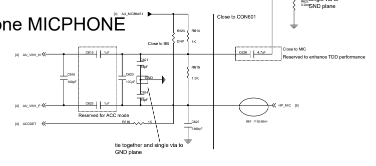
SPEAKER base M3901-P 0626



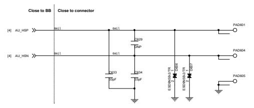
Earphone Audio base M3901-P 0626


Based on your system level design, if better Audio performance is needed on your system, please add 32ohm to audio path for performance enhance proposal (32ohm condition pop noise can improve 6dB)
Note: 60-1
close to IC
close to connector
Note: 60-2
BEAD601 / BEAD604 are for FM-desense tuning proposal
GND shielding
(1) iPhone : L-R-G-M
Single via to GND plane

Earphone MICPHONE

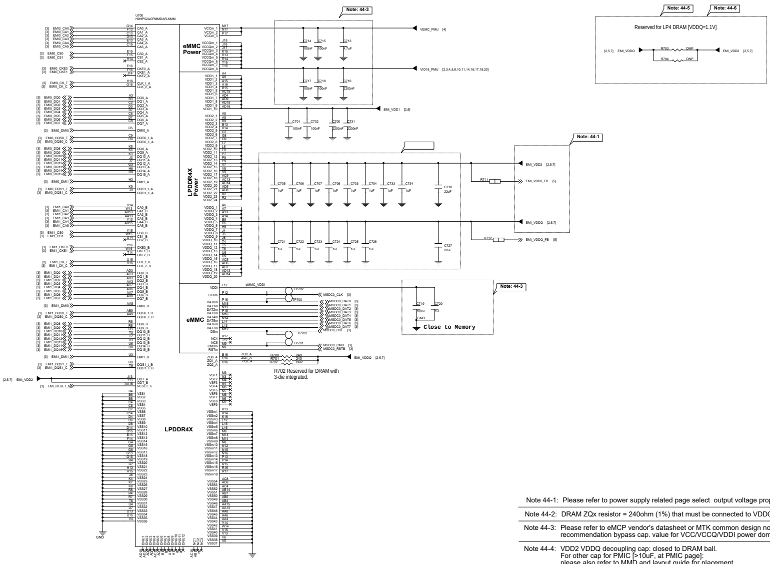


EAR PIECE



ONTIM Technologies Ltd.	
Title: M6206	Size E
Functionality: BB AUD	Ver P0
Date: Friday, July 24, 2020	Sheet 6 of 24

This page base MT6762_LPDDR4/4X reference SCH



Note 44-1: Please refer to power supply related page select output voltage properly for LP4X/LP4

Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ,

Note 44-3: Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

Note 44-4: VDD2 VDDQ decoupling cap: closed to DRAM ball.
For other cap for PMIC [>10uF, at PMIC page]:
please also refer to MMD and layout guide for placement.

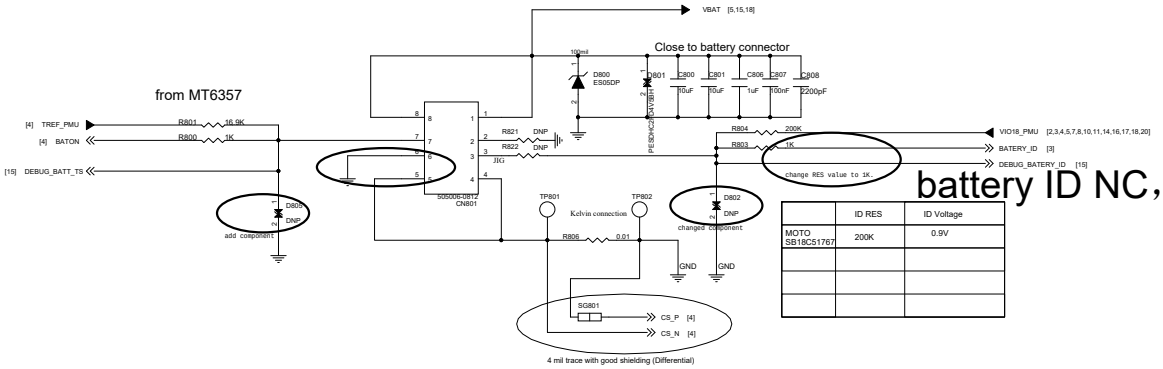
Note 44-5:

DRAM type	LPDDR4	LPDDR4X
R703, R704	Mount	NC
U700	LPDDR4-eMCP	LPDDR4X-eMCP
R6649	Mount	NC
U512/L511 /C563/C564	NC	Mount

Note 44-6: R703/R704 could be replaced with 0-ohm / 0402 * 3 for LP4 DRAM

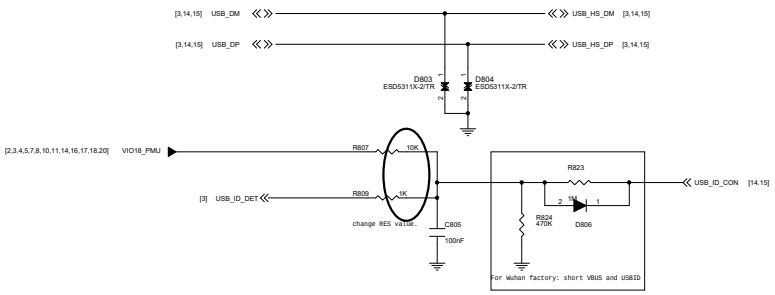
This page base M3901-P 0626

BATTERY CONNECTOR



battery ID NC，delete?

	ID RES	ID Voltage
MOTO SB18C51767	200K	0.9V



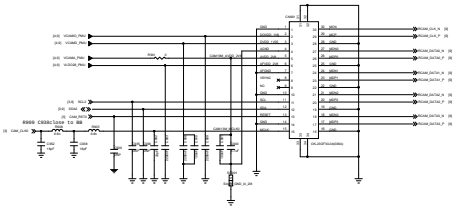
ONTIM Technologies Ltd.	
Title: M6206	Size: C
Functionality: BB VBAT&USB	Ver: P0
Date: Friday, July 24, 2020	Sheet 8 of 24

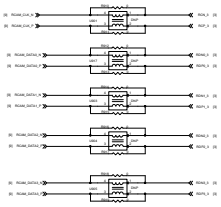
Page09:Rear-CAM-13M,2M
Front-CAM-5M

Dual CAM
Rear-Main-AF Camera 13M

RST0 MCLK0 I2C2

Rear camera SHINETECH(SKOL5XX03-FGX5) I2C address: (Write:0x20, Read:0x21)
AF driver xxxx I2C address (Write:0xxx, Read:0xxx)

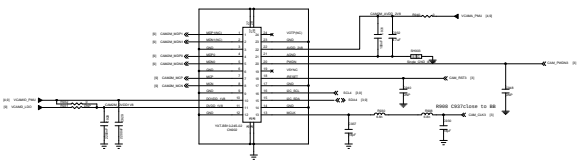


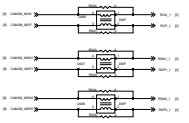


Dual CAM
Rear-Slave-FF Camera 2M Macro

RST3 MCLK3 I2C4
PWDN3

Rear camera Union image(ST-ZNAK57FF-V1) I2C address: (Write:0x20, Read:0x21)

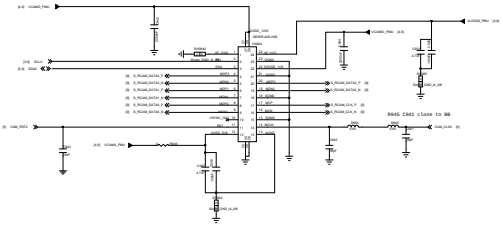


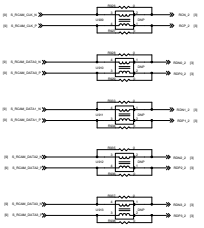


Single CAM

POWN2 MCLK2 I2C2

Main Camera 48M
I2C address:0x20(W),0x21(R)
I2C driver IC 0x18(W),0x19(R)
I2C EEPROM 0xB0(W),0xB1(R)

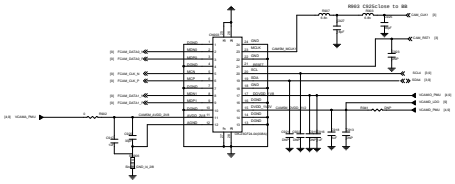


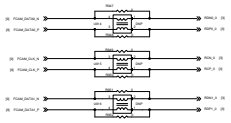


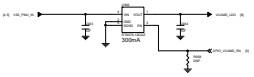
Front-FF-5M Camera

RST1 MCLK1 I2C4

Front camera xxxx(xxxx) I2C address: (Write:0x50, Read:0x51)



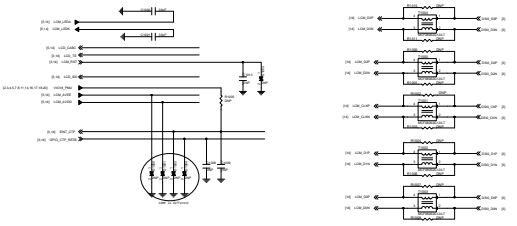




ONTIM Technologies Ltd.

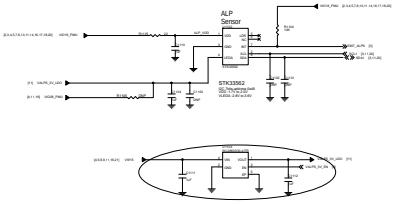
This page base M3901-P 0626

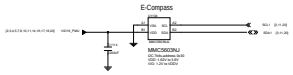
LCM Connector

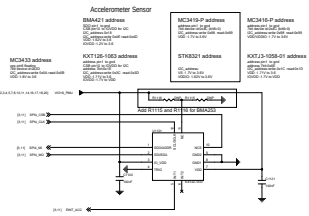


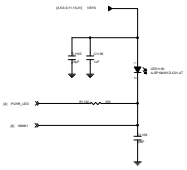
GT1151 I2C address: 0X5D (Write:0xBA, Read:0xBB)
or 0x14 (Write:0x28, Read:0x29)

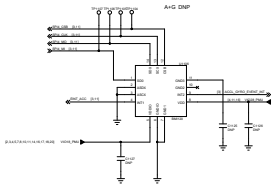
This page base M3901-P 0626

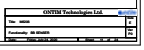




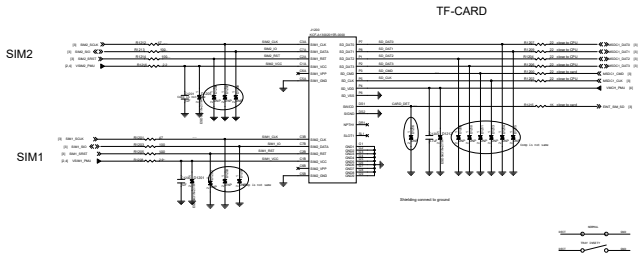






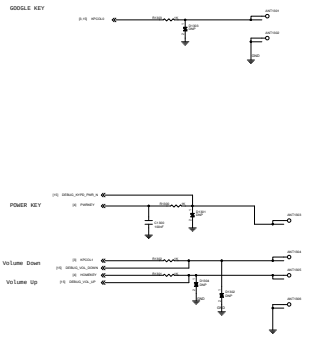


SIM and TF

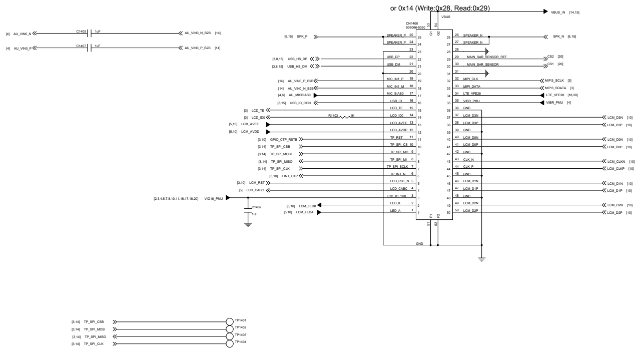


KEY base M3901-P 0626

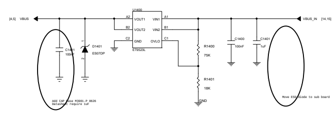
Volume Up : HOME Key / GND
Volume Down : KPCOL1/GND
DO NOT put pull-up resistor on PWRKEY



LCM Connector

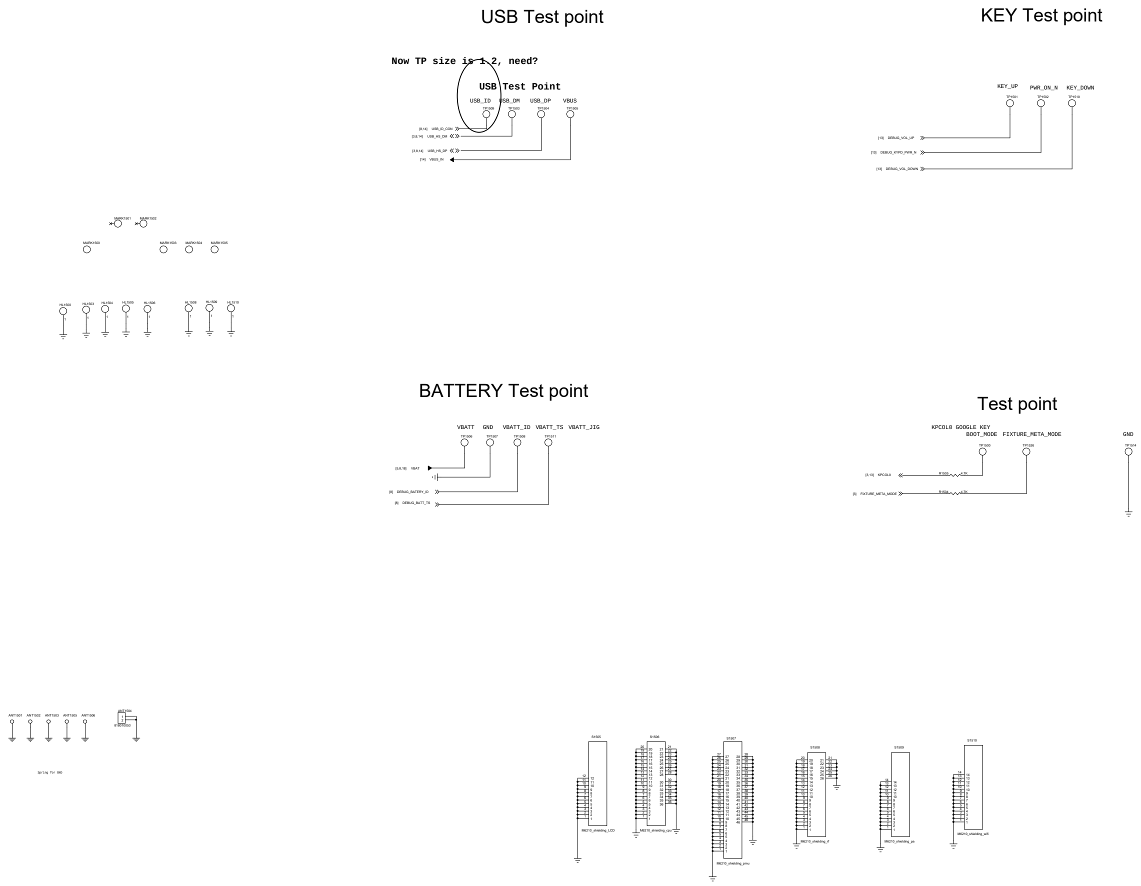


OVP



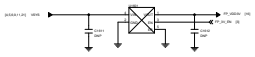
VIN_OVLO=VOVLO_TH x (1+R1/R2) = 1.2 * (1 + 75/18) = 6.2

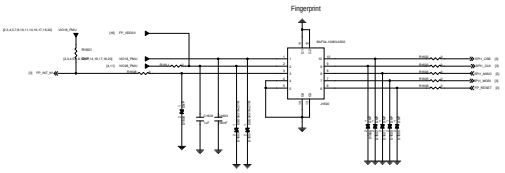
ONTIM Technologies Ltd.	
Title: M6206	Size E
Functionality: BB OVP&CON	Ver P0
Date: Friday, July 24, 2020	Sheet 14 of 24

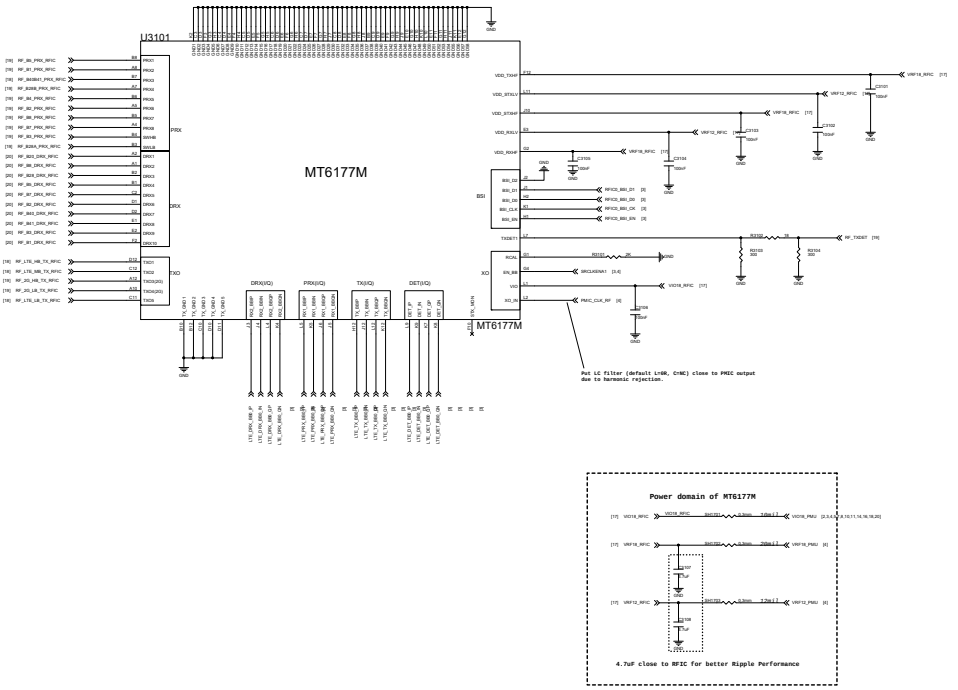


ONTIM Technologies Ltd.	
Title: M6206	Size E
Functionality: BB TEST POINT	Ver P0
Date: Friday, July 24, 2020	Sheet 15 of 24

This page base M3901-P 0626

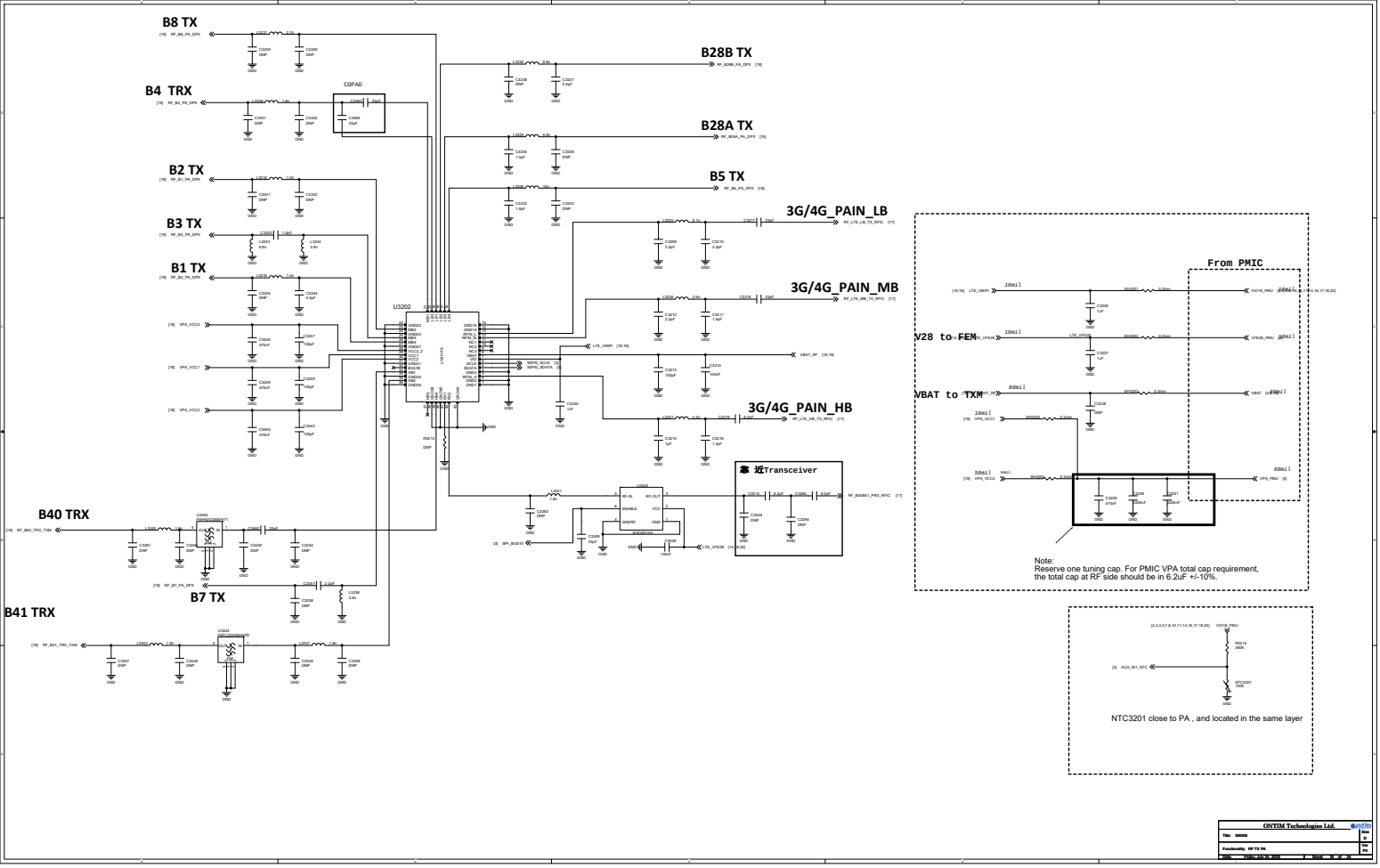


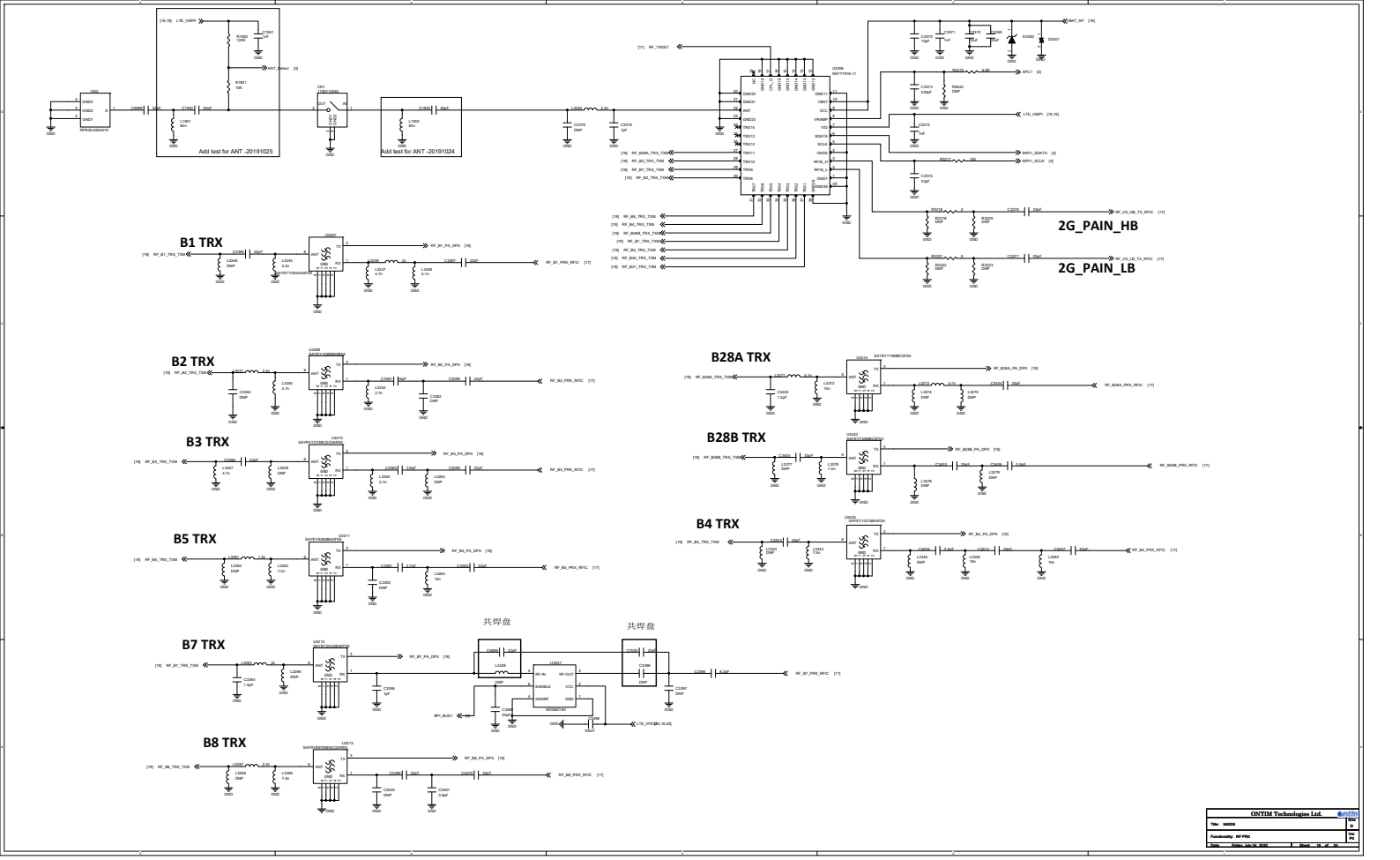




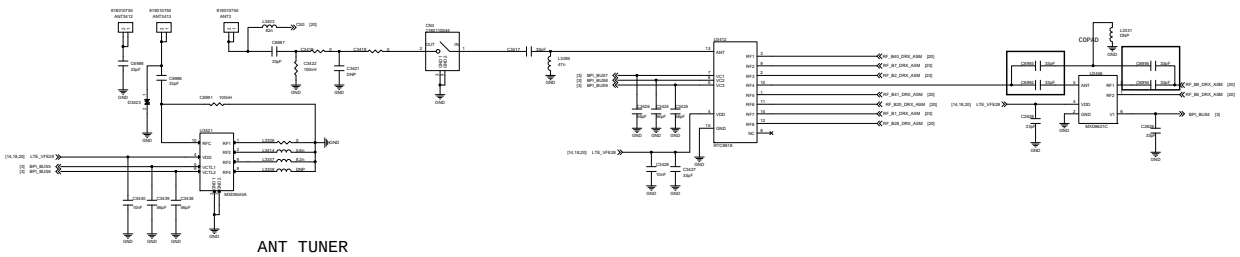
RF MT6177

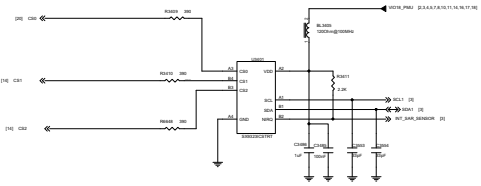
ONTIM Technologies Ltd.	
Title: MA208	Size: B
Functionality: RF MT6177	Ver: P0
Date: Friday, July 24, 2020	Sheet 10 of 46

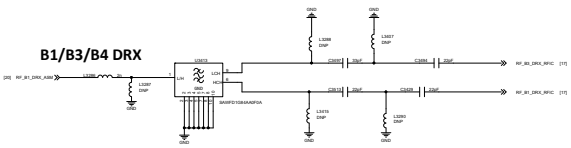

B8 TX
B4 TRX
B2 TX
B3 TX
B1 TX
B40 TRX
B7 TX
B41 TRX
B28B TX
B28A TX
B5 TX
3G/4G_PAIN_LB
3G/4G_PAIN_MB
3G/4G_PAIN_HB
COPAD
U3202
Transceiver
From PMIC
V28 to FEM
VBAT to TXM
Note:
Reserve one tuning cap. For PMIC VPA total cap requirement,
the total cap at RF side should be in 6.2uF +/-10%.
NTC3201 close to PA , and located in the same layer
ONTIM Technologies Ltd.

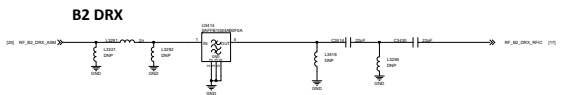


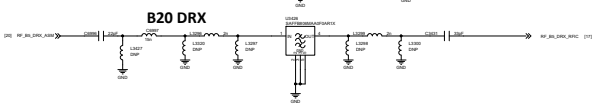
ONTIM Technologies Ltd.	
Title: M8309	Size: D
Functionality: RF PRX	Rev: V0
Date: Friday, July 24, 2020	Sheet 19 of 34

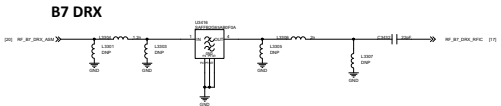


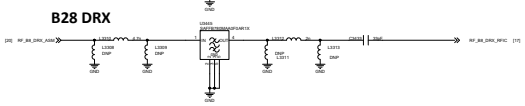


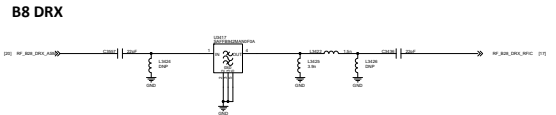


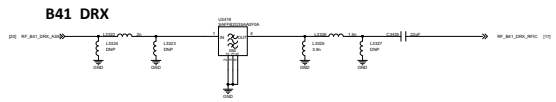


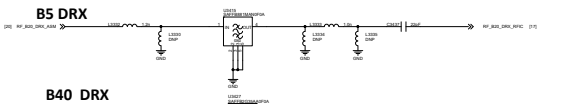


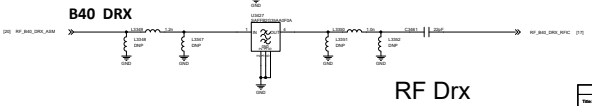






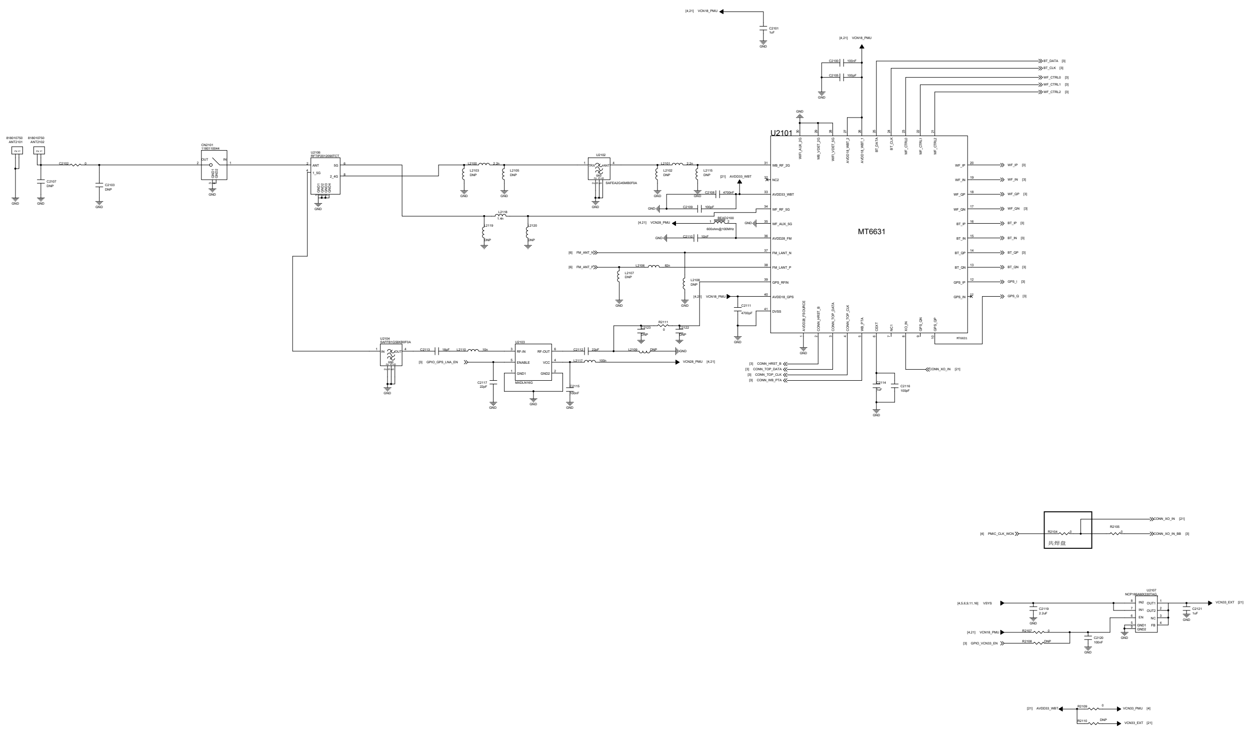






RF Drx

ONTIM Technologies Ltd.



ONTIM Technologies Ltd.	
Title: M6206	Size E
Functionality: RF WCN	Ver P0
Date: Friday, July 24, 2020	Sheet 21 of 24