

# SCHEMATIC,MAIN,84350\_1\_15

REV:	V10
FILE #:	001.84350_1_15
DOCUMENT NO.:	84350_1_15_20220216_0000
DEPARTMENT:	EE
DESIGNER:	PenghangLi
DATE:	Tuesday, February 15, 2022
Sheet	1 of 102

Revision History

REV	DESCRIPTION
A	

Board Change History

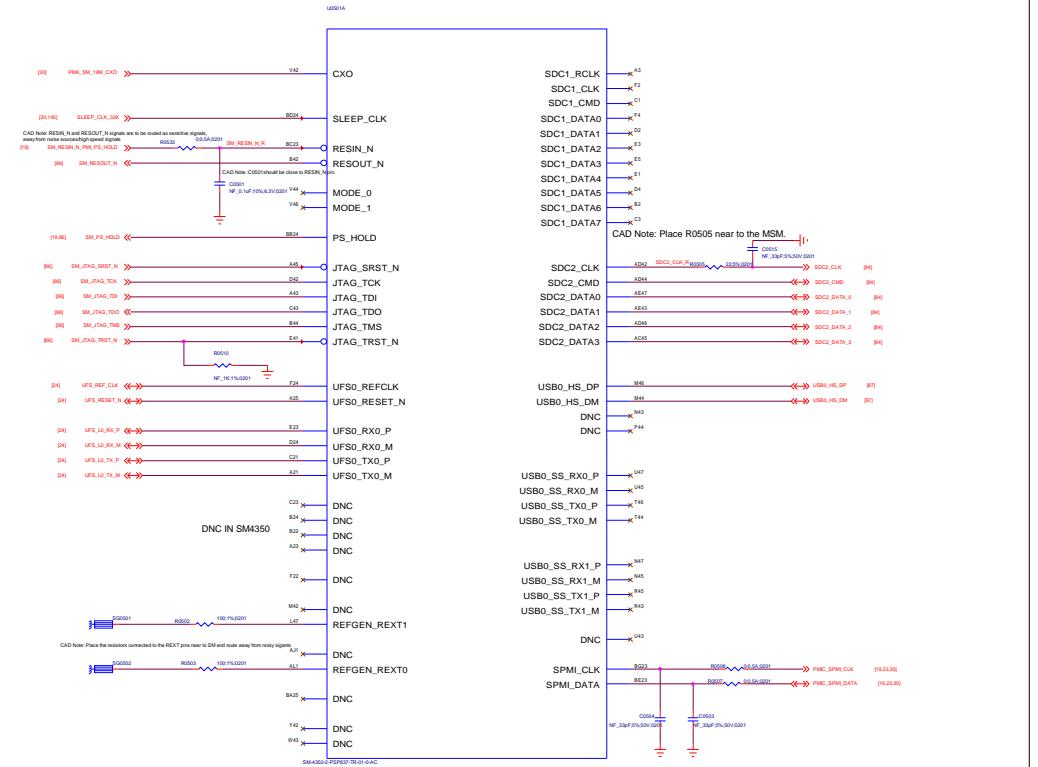
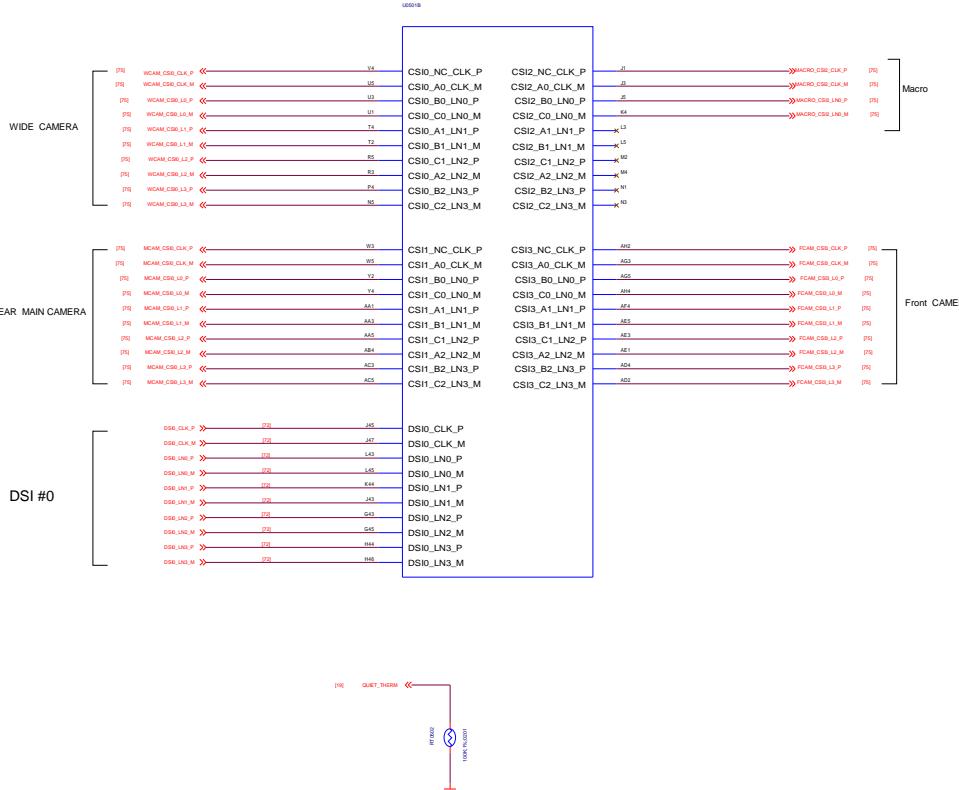
SCHEMATIC MCN	HW VERSION	REVISION	DESCRIPTION OF CHANGE

REVISION HISTORY2

## BLOCK DIAGRAM

004.BLOCK DIAGRAM	REV: V10
DOCUMENT NO:	84868_1_H_2022016_0009
DEPARTMENT:	Design
DESIGNER:	Nageswara
WINGTECH	Printed: Monday, December 26, 2022 Sheet 1 of 122

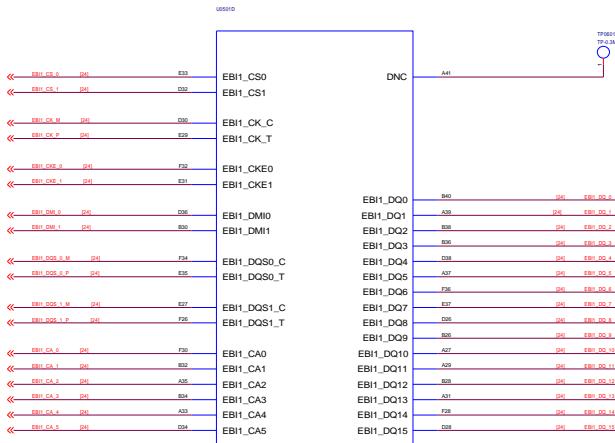
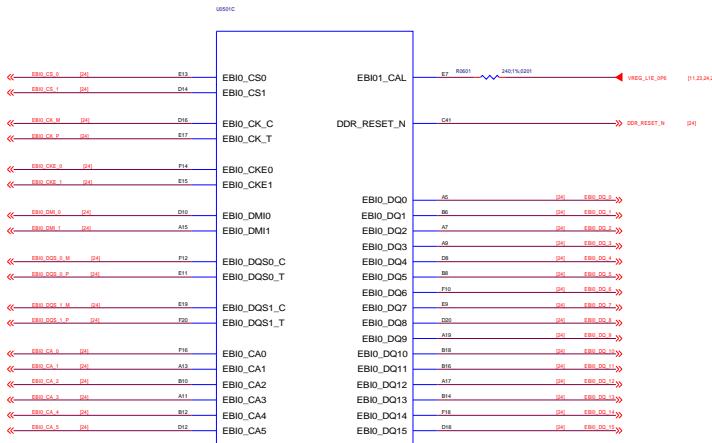
- The CSI group can be split into two lanes:
  - CSI lane mapping when a 4-lane interface is configured as 2-lane plus 1-lane interface
    - DCLK => DCLK\_A
    - DLNG => DLNG\_A
    - DLNT => DLNT\_A
    - DLNB => DLNB\_B
    - DLND => DCLK\_B
  - CSI lane mapping when a 4-lane interface is configured as 1-lane plus 3-lane interface
    - DCLK => DCLK\_A
    - DLNG => DLNG\_A
    - DLNB => DLNB\_B
    - DLND => DCLK\_B



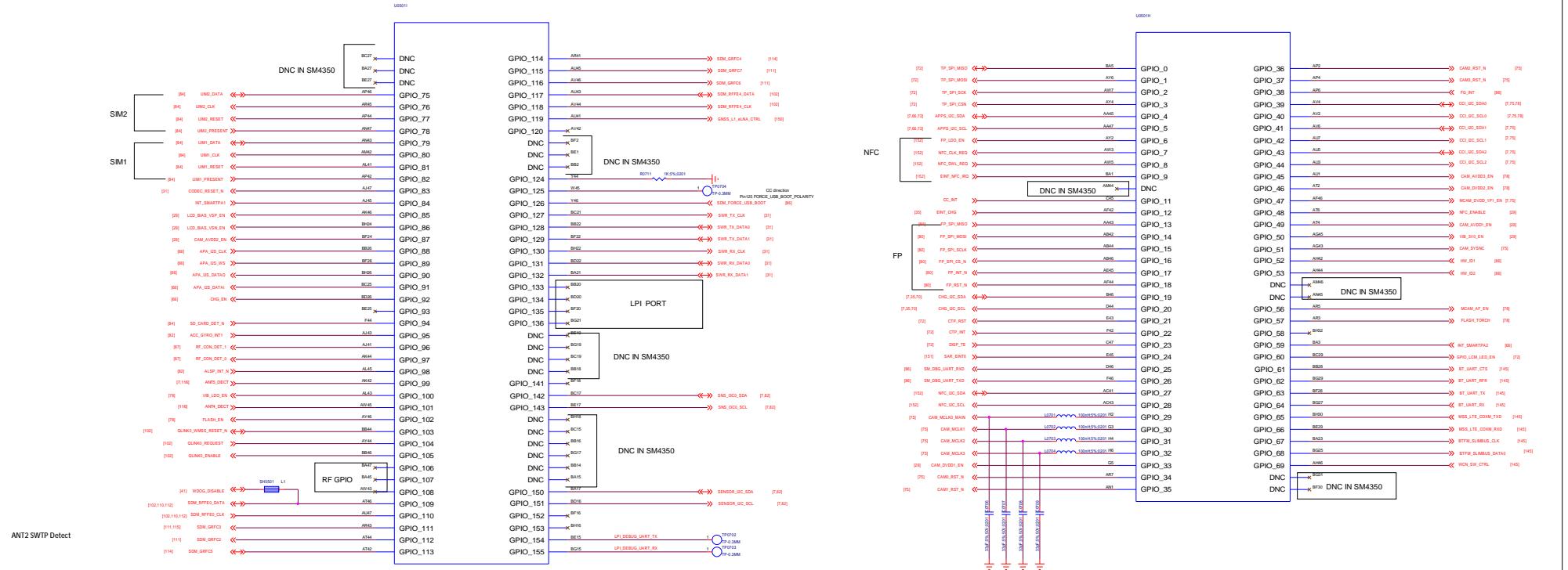
SM4350\_Control\_CSI\_DSI

Title	005.SM4350_CONTROL_CSL_DSI	EST:	V10
DOCUMENT NO.:	SM4350_1_16_20220216_0059	Size:	Custom
DEPARTMENT:	EE	DESIGNER:	Ningguo





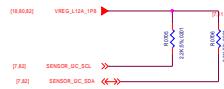
## SM6350\_LPDDR4x



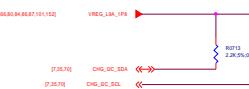
Audio PA \ Backlight\ LCD bias\SAR



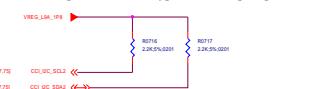
M Sensor\ PS&ALS



Charging IC\Fuelgauge \CC



CAM WIDE\CAM MACRO



FlashDriver\Front CAM



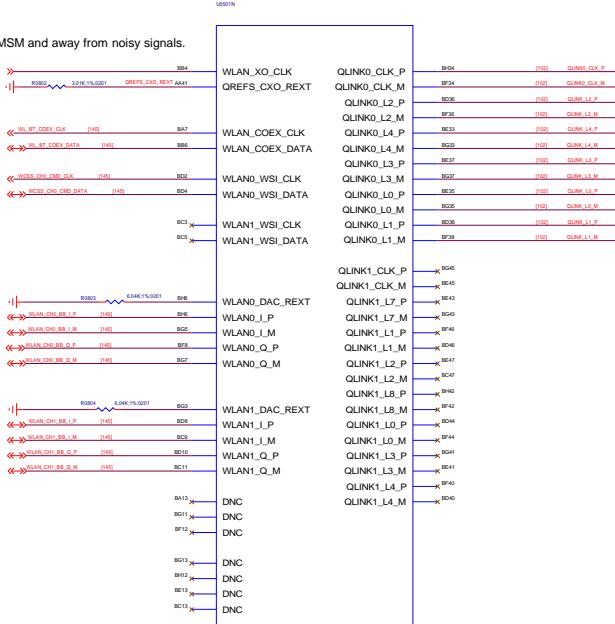
MAIN CAM



A+G Sensor I3C



CAD NOTE: Keep the resistors on the MSM REXT pins near to MSM and away from noisy signals.



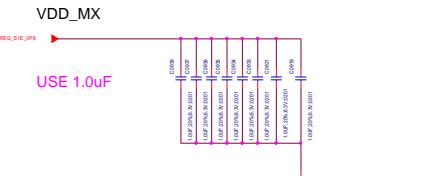
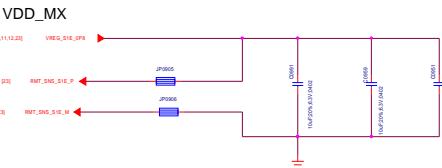
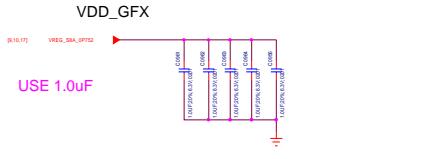
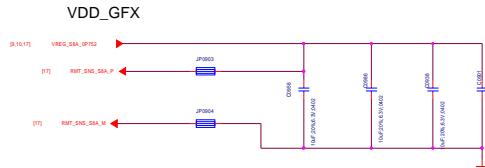
SM6350\_WLAN/Qlink

Title	<b>008.SM4350_WLAN_QLINK</b>	REV. V10
DOCUMENT NO.	S84350_1_16_20220216_9559	Size Custom
DEPARTMENT:	BB	DESIGNER: Negusus
<b>WINGTECH</b>		
Date:	Monday, December 06, 2021	Sheet 8 of 120

# PM6350 FTS Bucks

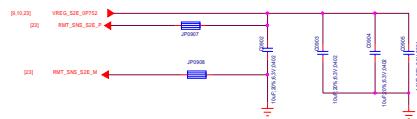
# PM6150A FTS Bucks

For LP4x VDD2

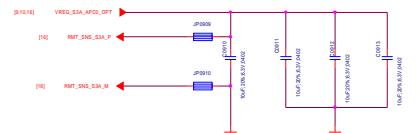


## SM4350\_Power Capacitor

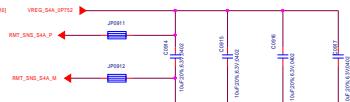
VDD\_CX



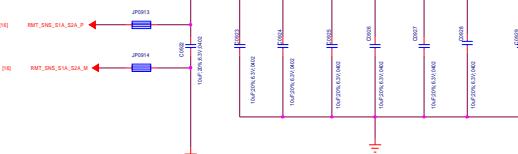
VDD\_APPC0



VDD\_APPC1



VDD\_MODEM



USE 1.0uF



USE 1.0uF

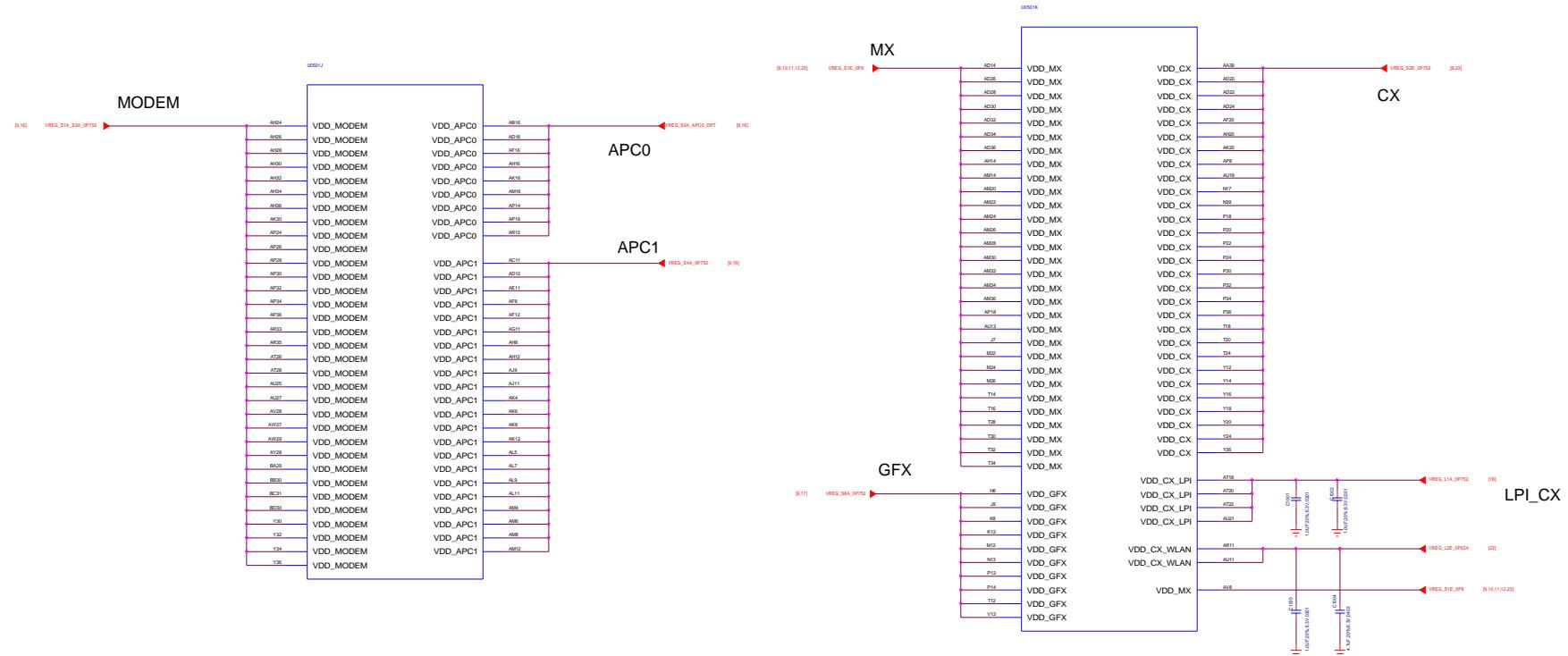


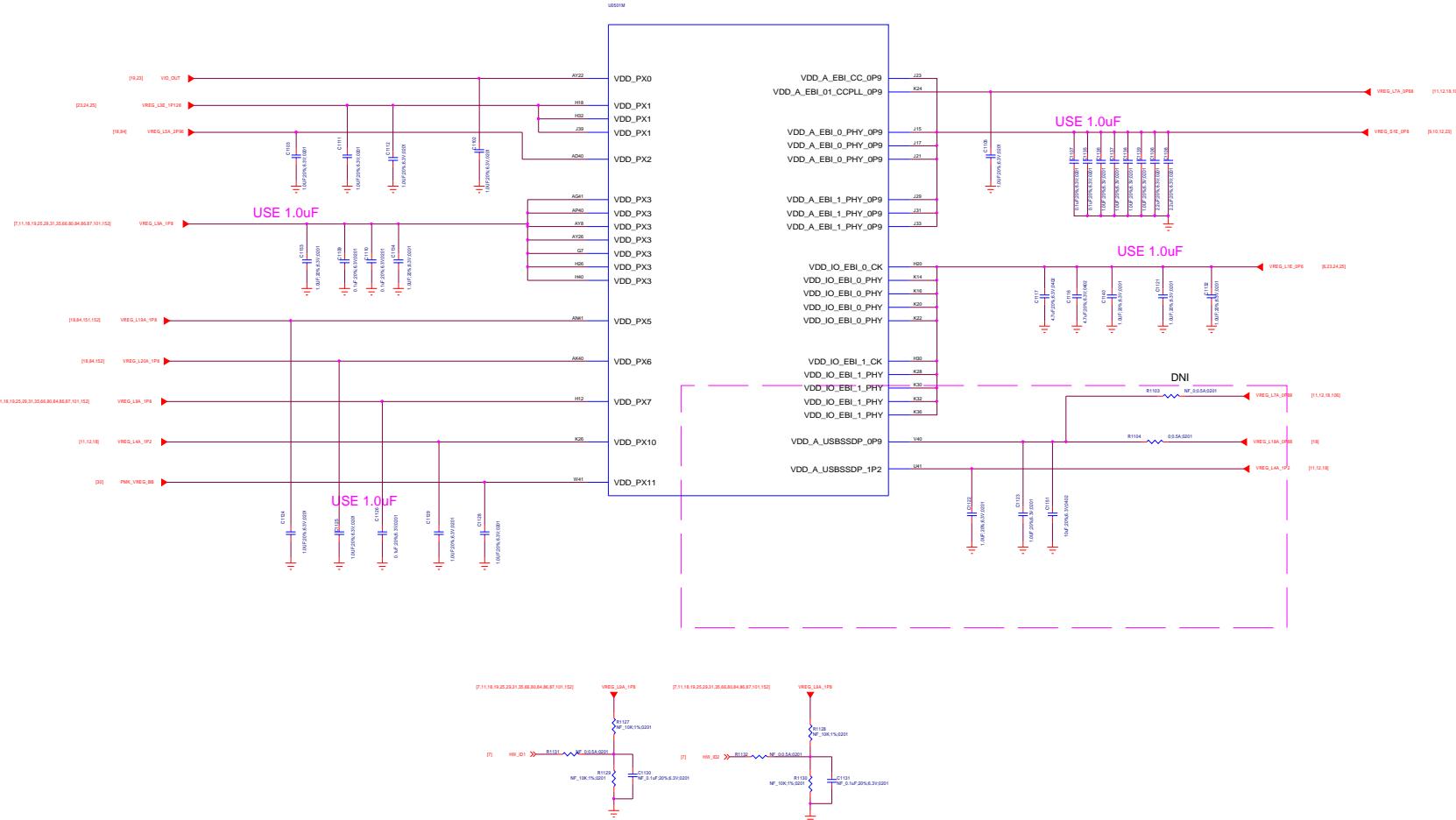
USE 1.0uF



USE 1.0uF

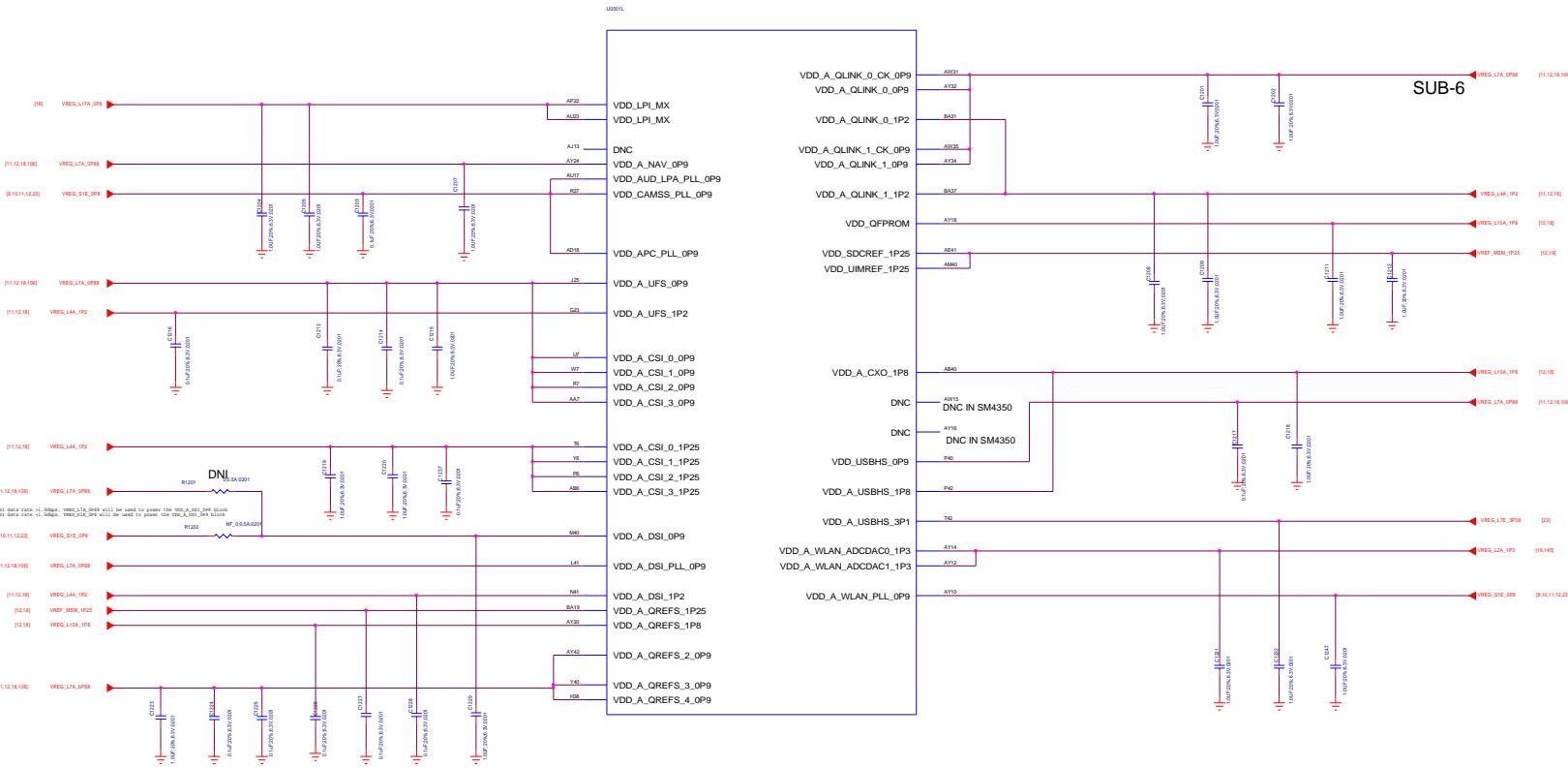






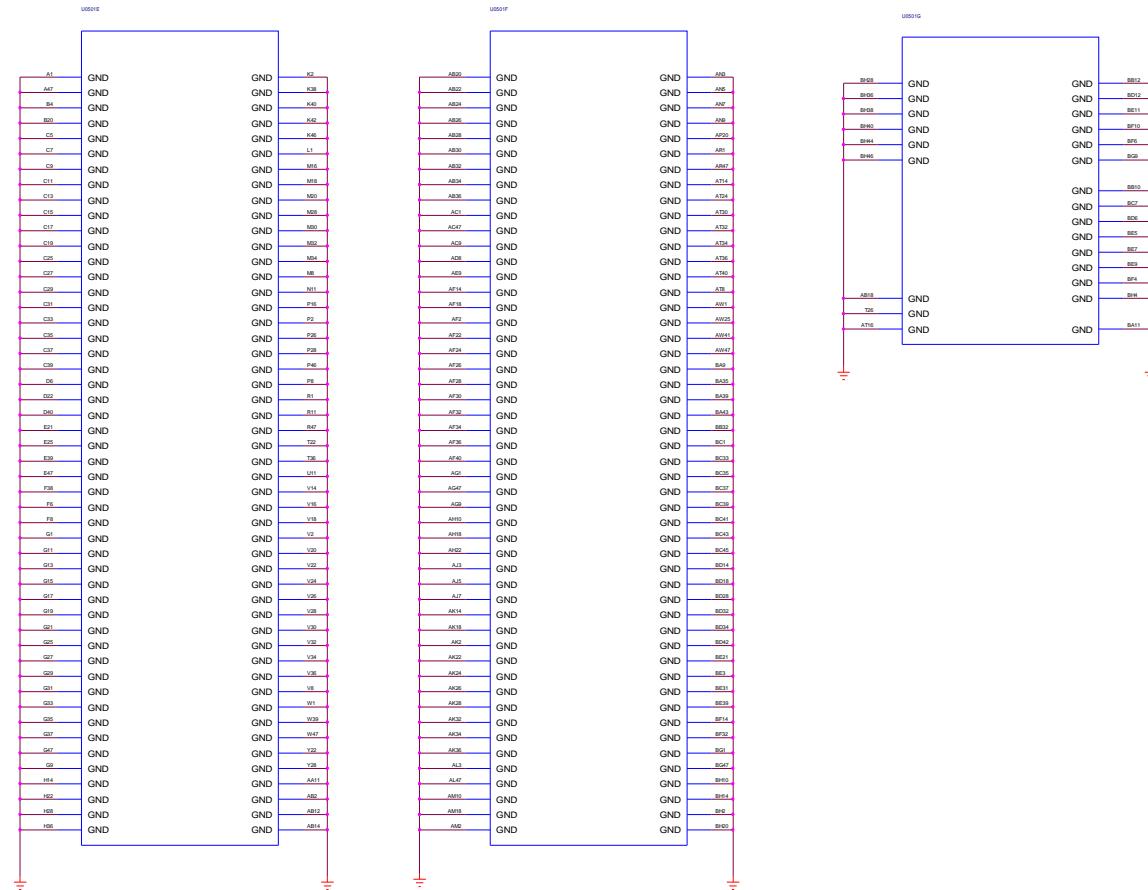
SM6350\_Power2 of 3

Title:	<b>011.SM4350 POWER2</b>	REV: V10
DOCUMENT NO.:	<b>SB4350_1_16_24220216_0058</b>	Size: Custom
DEPARTMENT:	<b>BB</b>	DESIGNER: <b>Nigamrao</b>
<b>WINGTECH</b>		
Date:	Monday, December 06, 2021	Sheet 11 of 152

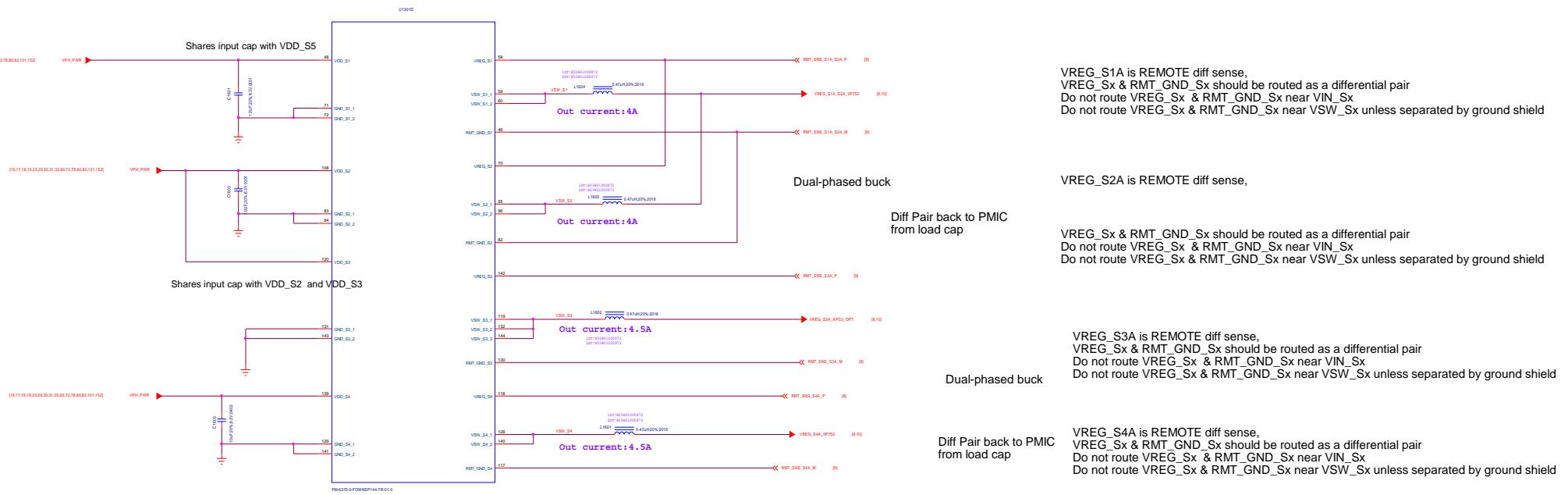


SM6350\_Power3 of 3

Title	<b>012.SMA4350_POWER3</b>	REV. V10
DOCUMENT NO.	SMA4350_1_16_20220216_0929	Size Custom
DEPARTMENT:	EE	DESIGNER: Nagashima
<b>WININGTECH</b>		
Date:	Monday, December 06, 2021	Sheet 12 of 150



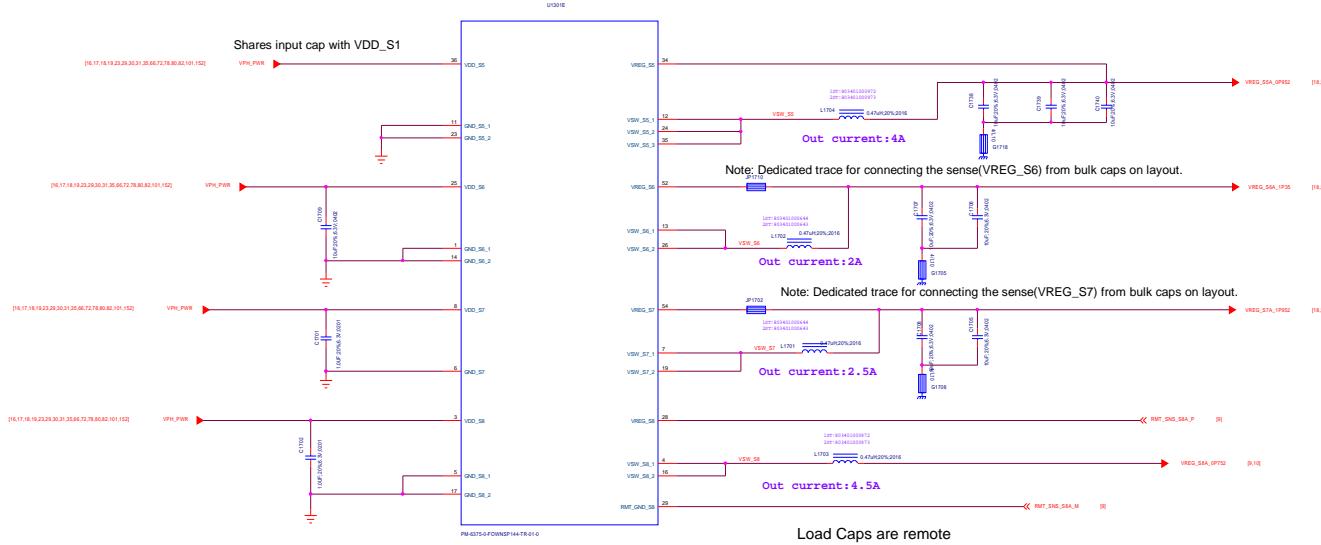
SM6350\_Ground



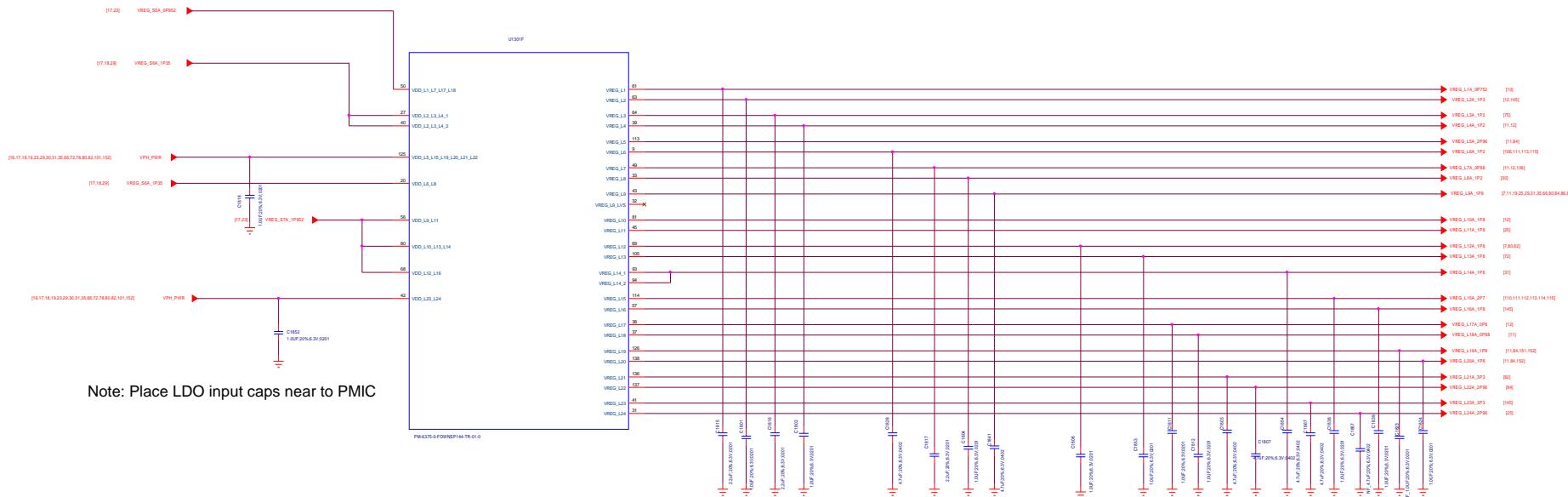
Place Cin as close to PMIC as possible to achieve this requirement.

Loop inductance from (VIN\_Sx to Cin + Cin to GND\_Sx) must be < 3nH

S1A-2A:	FTS510	0.8V default	8000mA Ipeak	8110.00mA APC
S3A-4A:	FTS510	0.8V default	8000mA Ipeak	8480mA CX, MODEM
S5A:	HFS510	0.912V default	4000mA Ipeak	3620.00mA EBI, MX, nLDO
S6A:	HFS510	1.352V default	2000mA Ipeak	1560mA LDO
S7A:	HFS510	2.04V default	2500mA Ipeak	2350mA LDO
S8A:	FTS510	1.128V default	4000mA Ipeak	1790mA LDO, LPDDR4x



PM6125\_Bucks\_S5-S8



Note: Place LDO input caps near to PMIC

LDO L5/L9/L10/L11/L12/L13/L14/L15/L16/L19/L20/L21/L22/L23/L24 is the Pseudo-capless LDO, so can dni CAP in BOM

## PSEUDO CAPLESS LDOs

PSEUDO CAFELESS EDOS

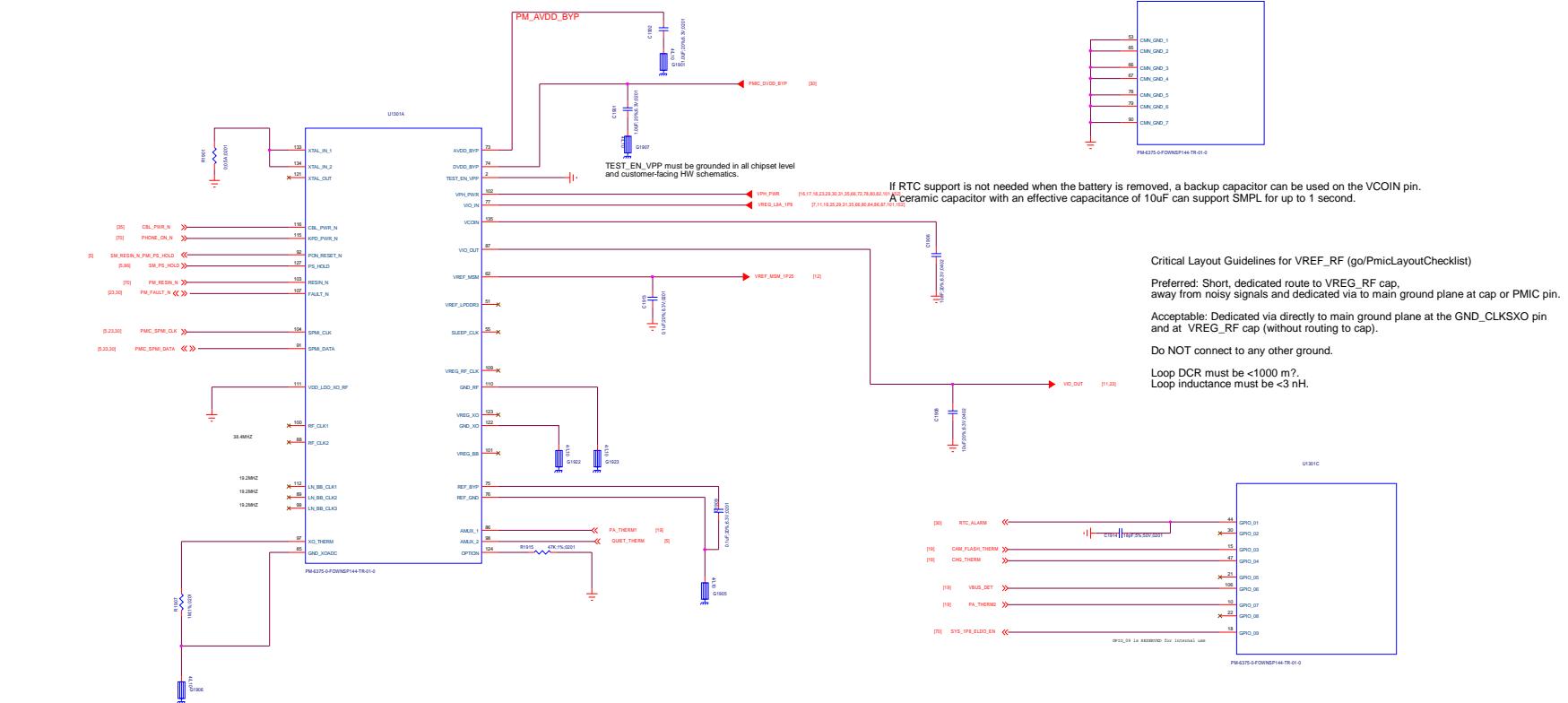
For CAPLESS LDOs: If decaps on the load side do not add up to LDO spec, then install the cap close to the PMIC

Layout Note:  
No trace shall be present in at least two immediate layers below XTAL.

Route XTAL IN/OUT trace with  
length between 3mm and 10mm

AVDD\_BYP should be routed  
away from noisy traces

Trace from pin to cap and ONE dedicated via from cap to main ground plane.  
DCR < 200mOhm and ESL < 10nH  
Do NOT connect to any other ground.



Placement/Layout Note:  
VREG\_RF Cout should be placed close to the PMIC  
Can be prioritized over VREG\_XO Cout placement

Short dedicated route to VREG\_RF/XO cap

Dedicated via directly to main ground plane at the capacitor

Dedicated trace from REF\_BYP to cap.

Dedicated via to main ground plane right under PMIC pin (REF\_GND)

As close to the PMIC as possible

REF\_BYP and REF\_GND should be

routed away from noisy traces

SPMI\_CLK & SPMI\_DATA should be routed away from noisy traces

Route signals as a diff pair as much as possible

GND\_XOADC

Skinny trace to XTAL components ground.

One dedicated via to main ground place as close to PMIC pin as possible

Critical Layout Guidelines for Clocks (go/PmicLayoutChecklist)

Coupling to any RFCLK or LNBBCLK output from each aggressor should be < 50 fF.

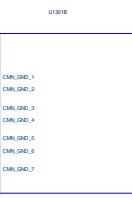
1. SMPTE components (Buck, Boost, Charger)

2. VSW\_Sx traces (Buck, Boost, Charger)

3. All other RFCLK, LNBBCLK

4. Any high speed digital signal

5. Any other noisy signals



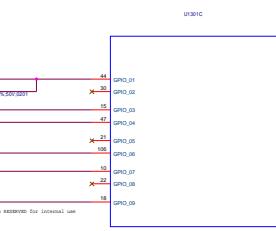
Critical Layout Guidelines for VREF\_RF (go/PmicLayoutChecklist)

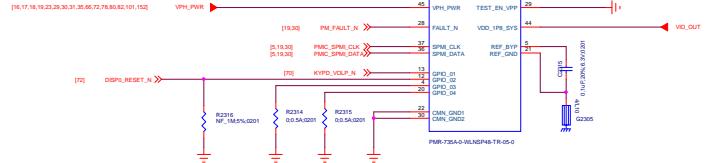
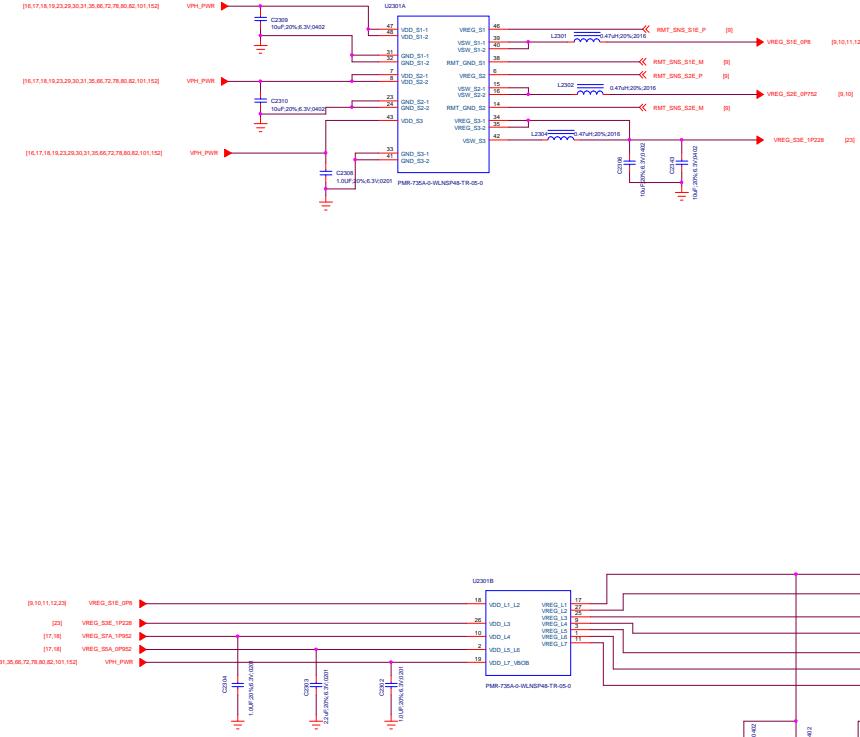
Preferred: Short, dedicated route to VREG\_RF cap,  
away from noisy signals and dedicated via to main ground plane at cap or PMIC pin.

Acceptable: Dedicated via directly to main ground plane at the GND\_CLKSXO pin  
and at VREG\_RF cap (without routing to cap).

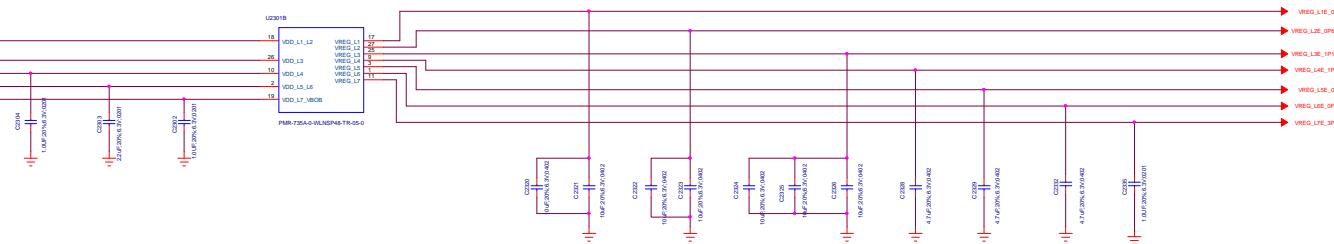
Do NOT connect to any other ground.

Loop DCR must be < 1000 m<sup>2</sup>.  
Loop inductance must be < 3 nH.





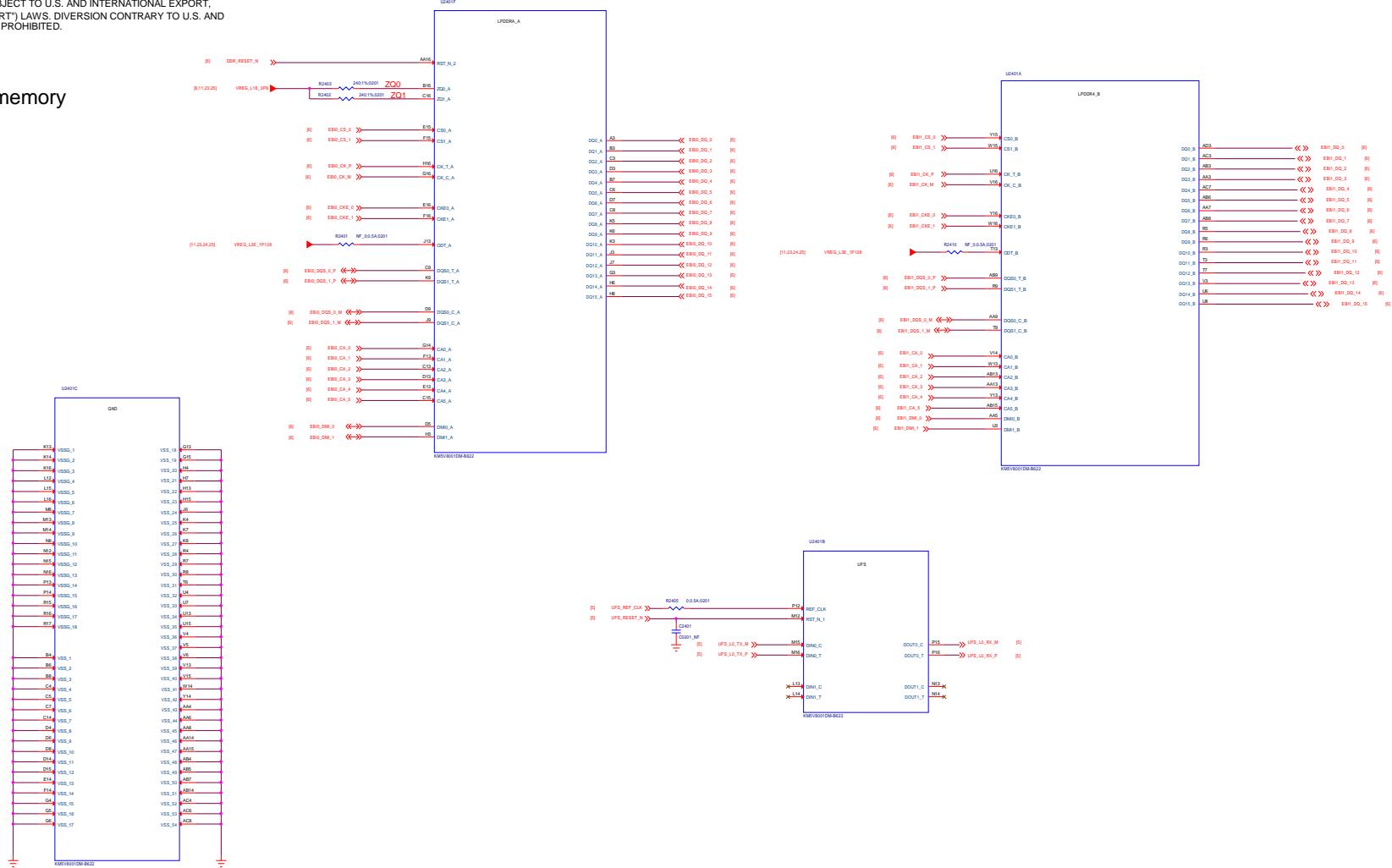
REF\_BYP and REF\_GND should be routed away from noisy traces



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REVISIONS			
LTR.	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		

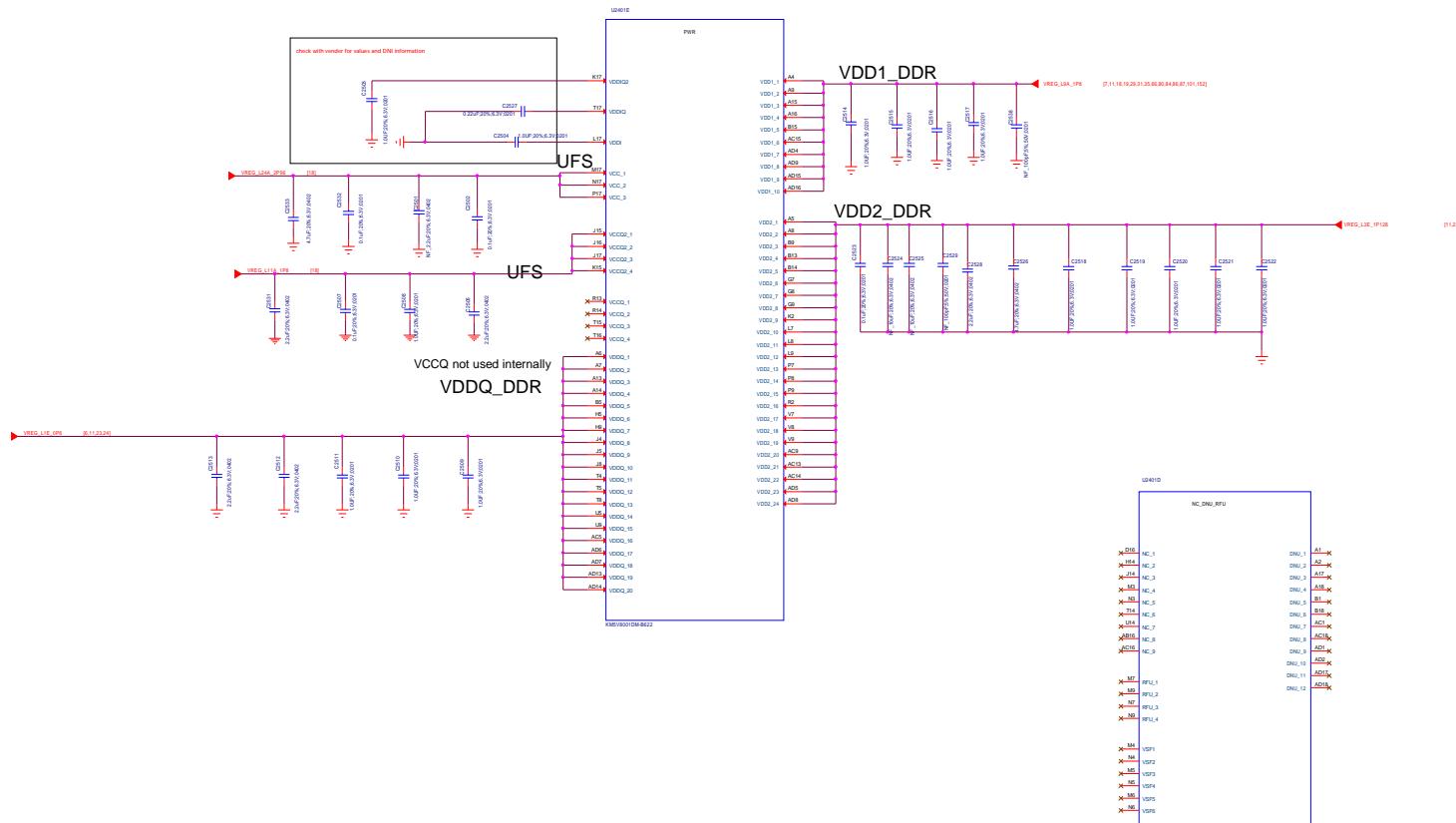
Pls near to the memory



PIs use memory in PVL list

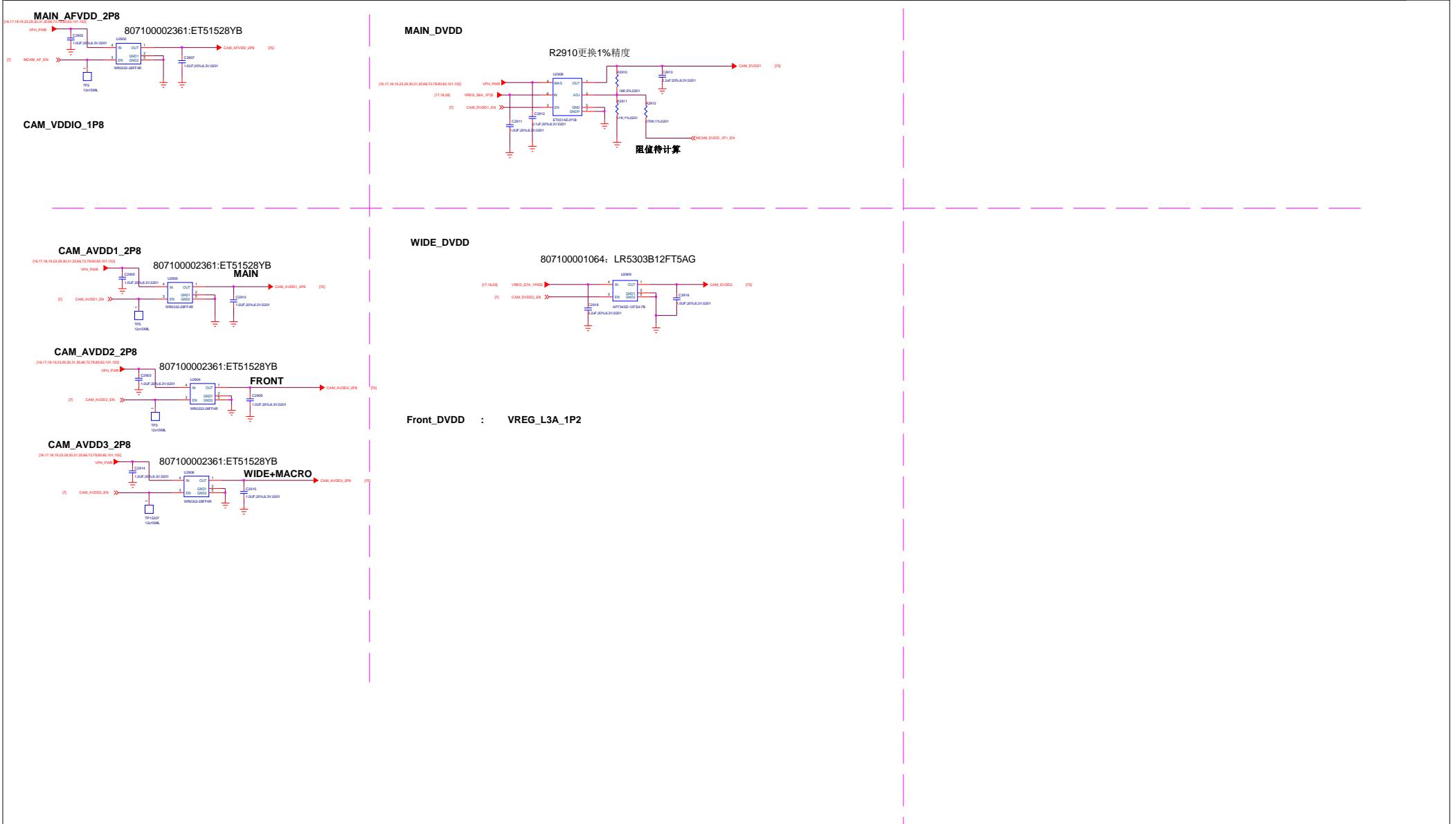


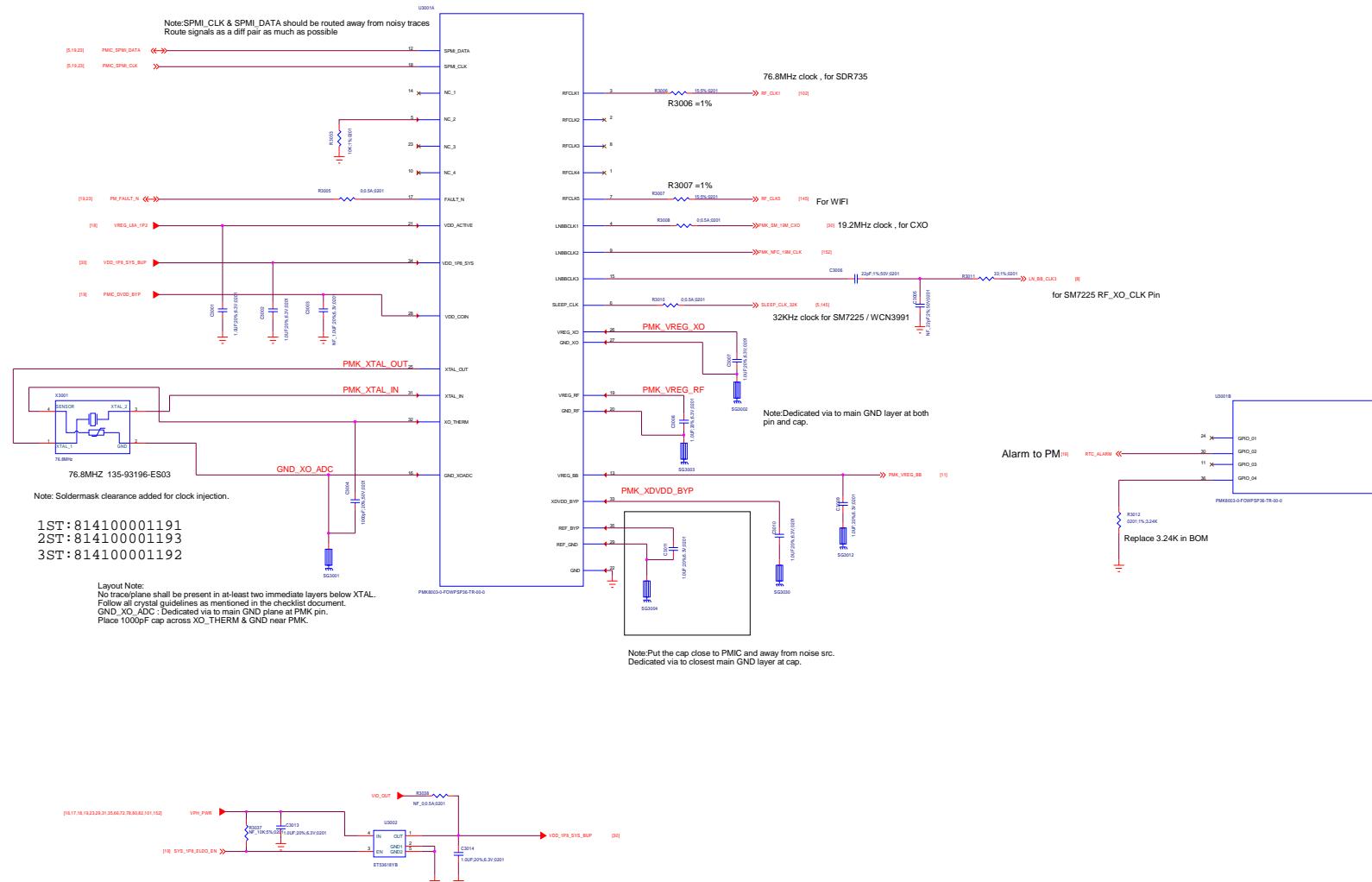
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## eMCP\_POWER

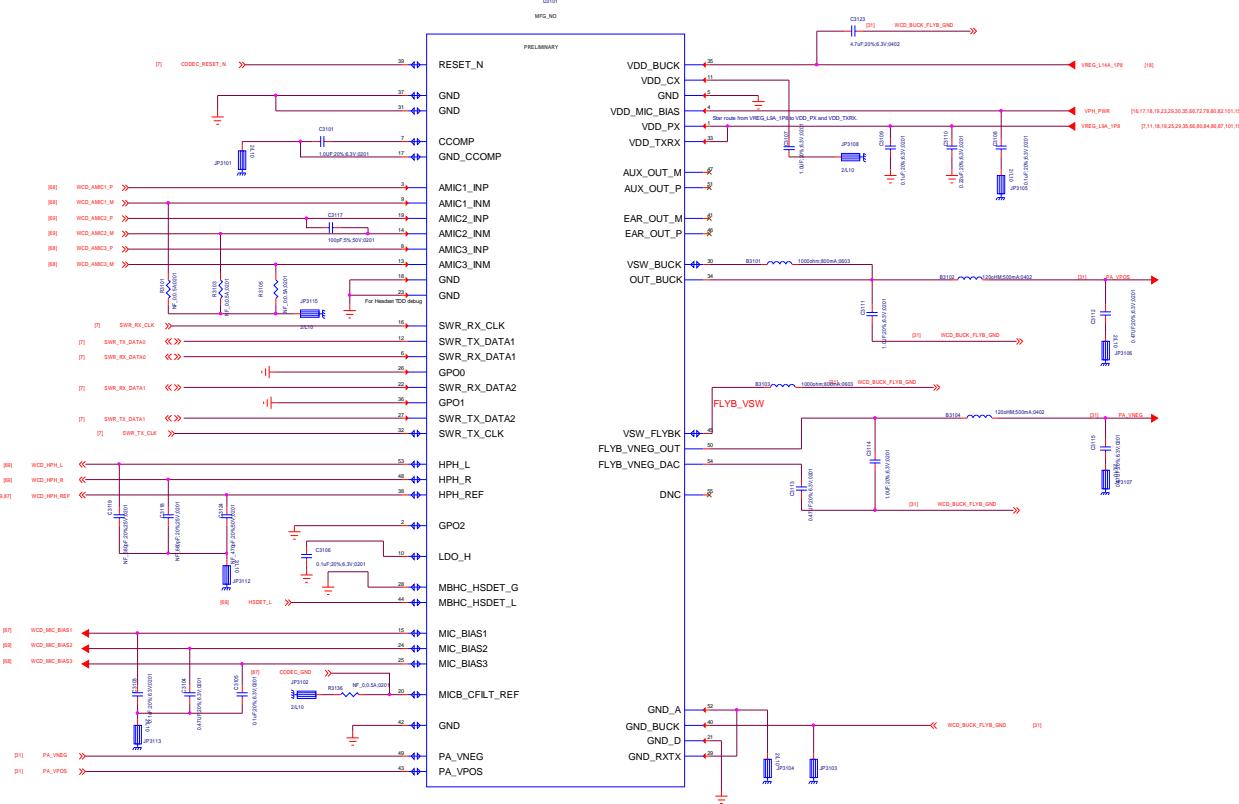
File Page Name = 025.UMCP\_POWER'10  
DOCUMENT NO.: Design Name = 584250\_1\_16\_20220210\_0805 Custom  
DEPARTMENT: DESIGNER = zhangheping  
  
date: Page Modify Date = Monday, December 05, 2022 25 of 102





PMK8003 CLK

File	<b>030.PMK8003_TIMEX</b>	Ext:	V10
DOCUMENT NO:	SB4350_1_16_20220216_0058	Size	Custom
DEPARTMENT:	EE	DESIGNER:	Ningxiao
<b>NINGTECH</b>		Date: Monday, December05, 2021	
		Sheet	30
		of	152

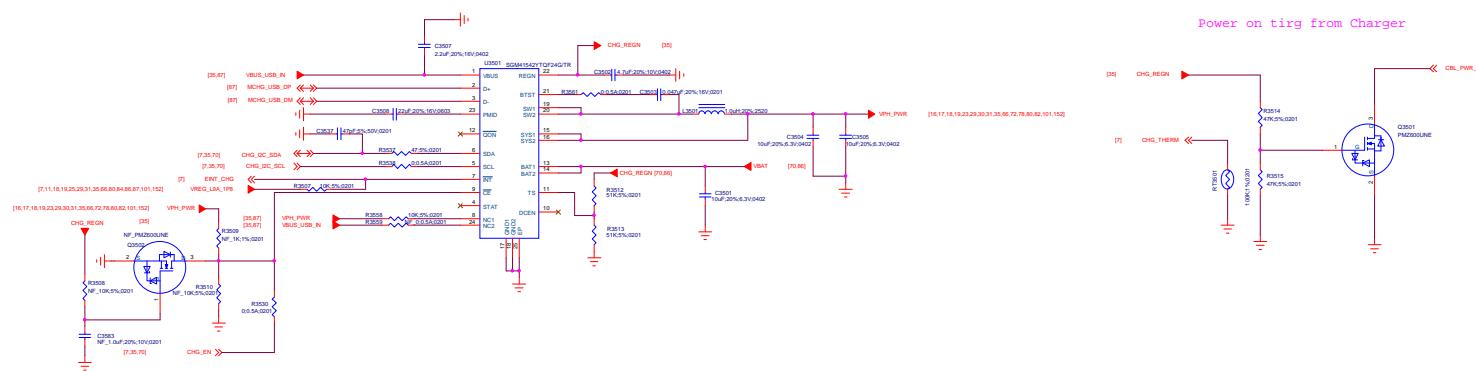


NOTE:B3101-B3104 Can't change to other PN.Otherwise will cause receiver TDD issue.

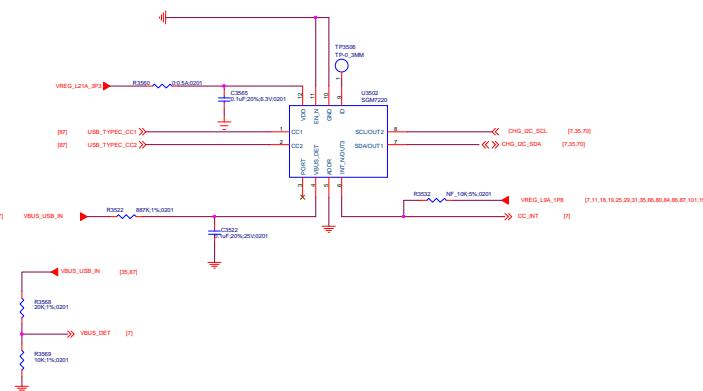
AUDIO\_CODEC\_WCD9370

## 35\_Charger

### Charger



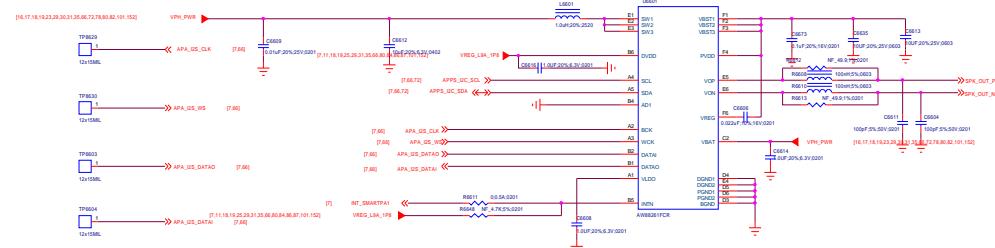
### CC logic



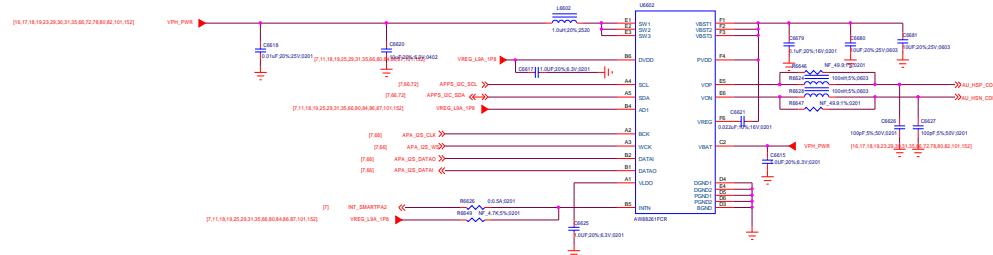
035_Master Charger		REV: V10
DOCUMENT NO.:	SB4500_1_16_20220116_8659	Sheet D
DEPARTMENT:	EE	DESIGNER: Ningwei
REV:		WINGTECH

Printed: Tuesday, December 21, 2021 Sheet 20 of 152

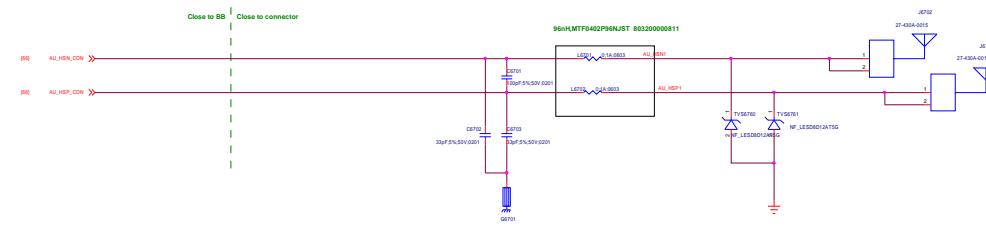
# 066\_SPK



FOR REC



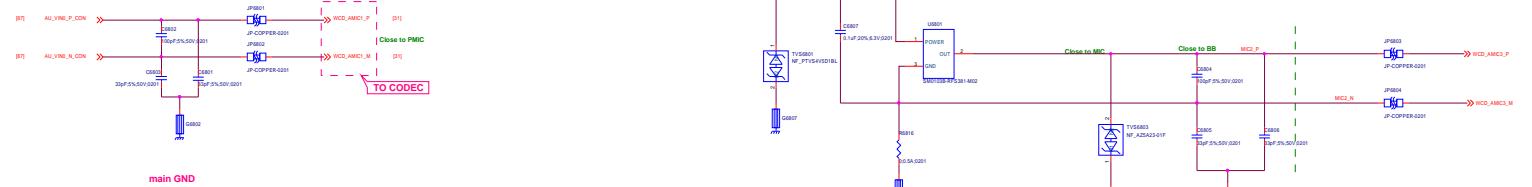
## Receiver

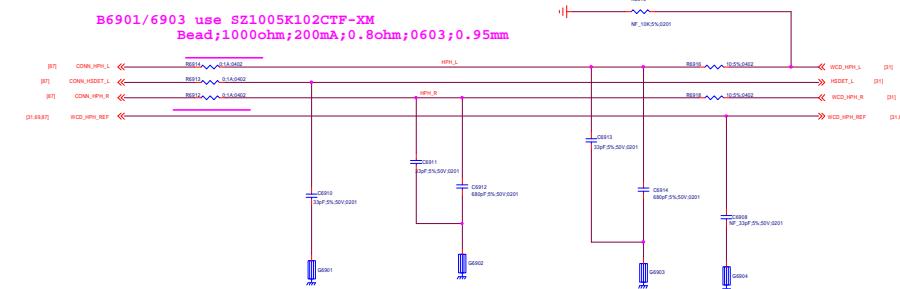
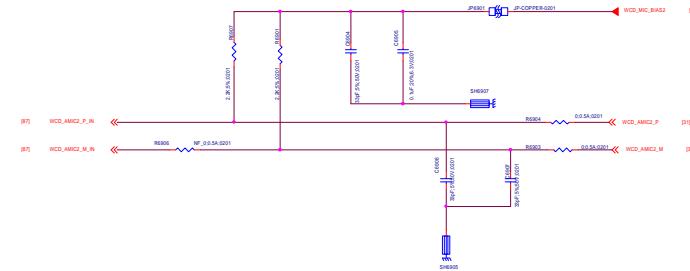


## AUX MIC

## MAIN MIC

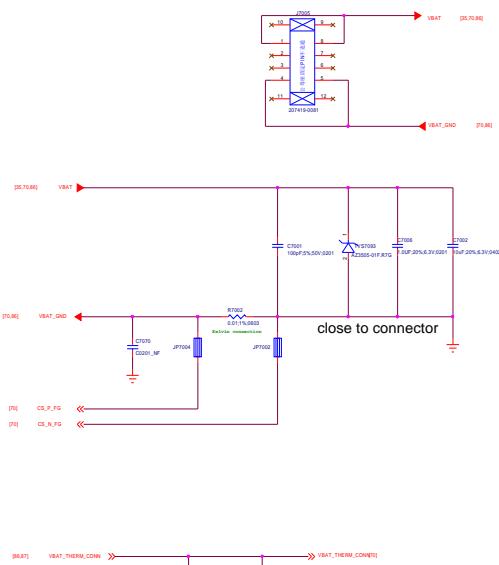
### second Microphone



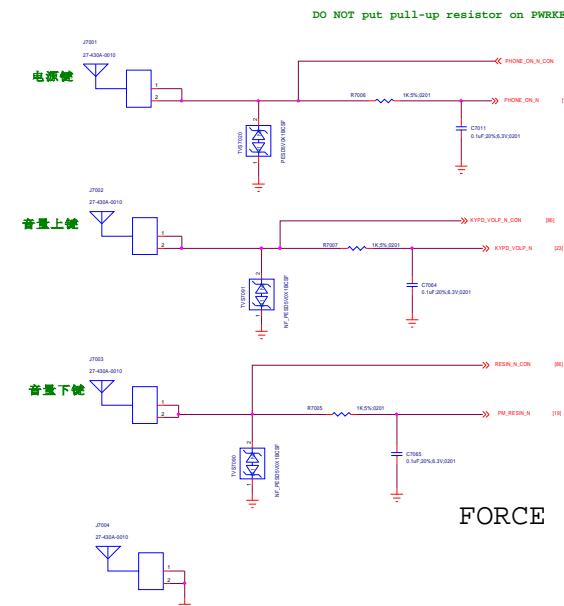


# 070\_Battery/Sidekey

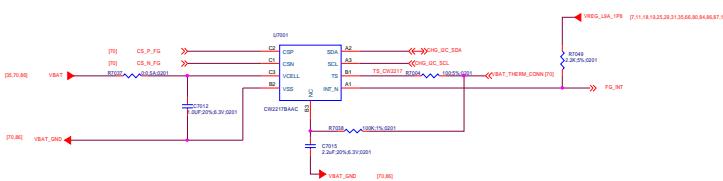
## BATTERY MASTER CONNECTOR



## POWER KEY / VOL KEY



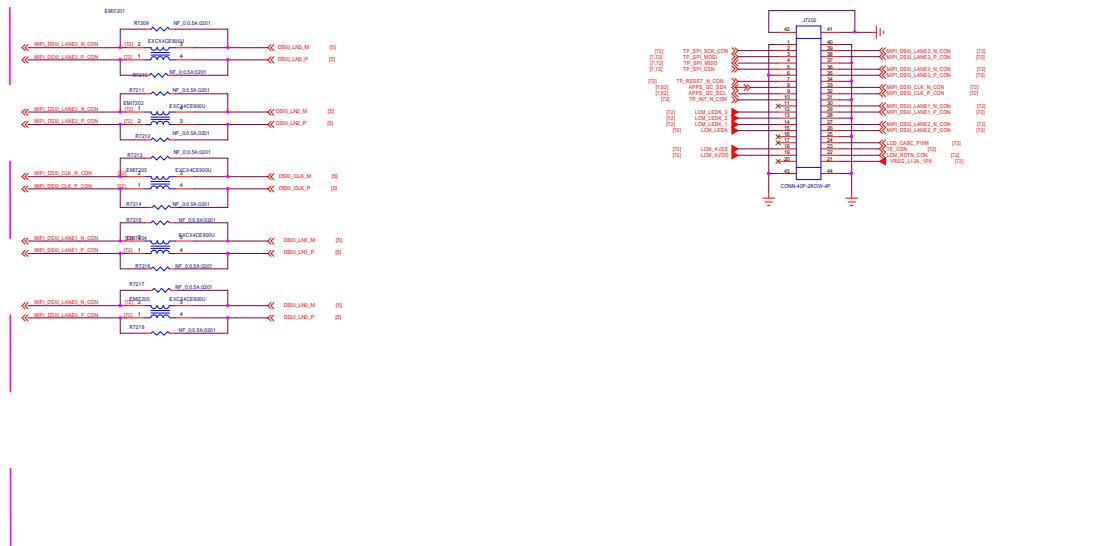
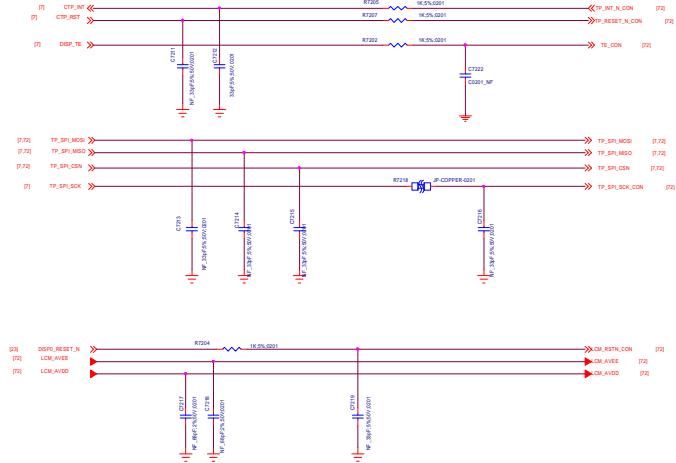
FG



# 072\_LCD/CTP IF

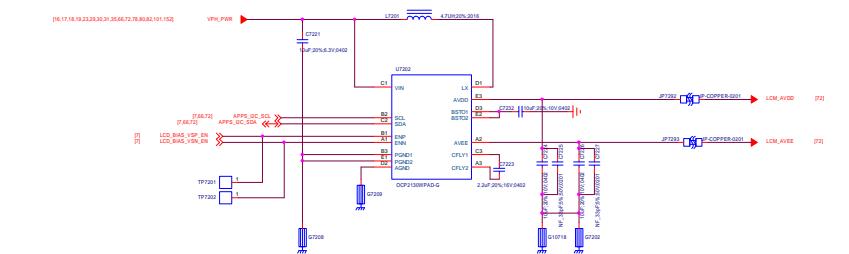
## MIPI CMF

CMP  
1st:811310000121  
2st:811310000126



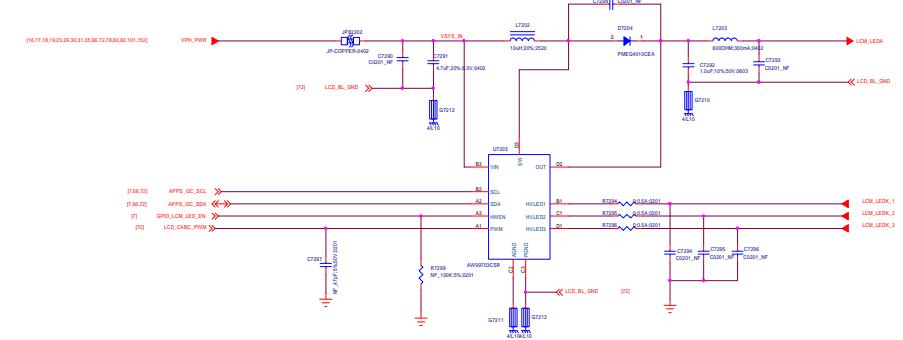
## LCM Gate Drive

SM5109/OCP2130 LCM Gate Driver I2C address: 0X3E (Write:0x7C, Read:0x7D)



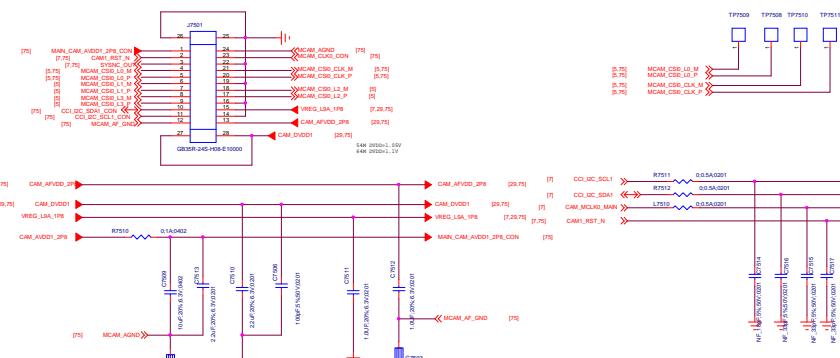
## Reserve for ESD

## LCD-BACKLIGHT

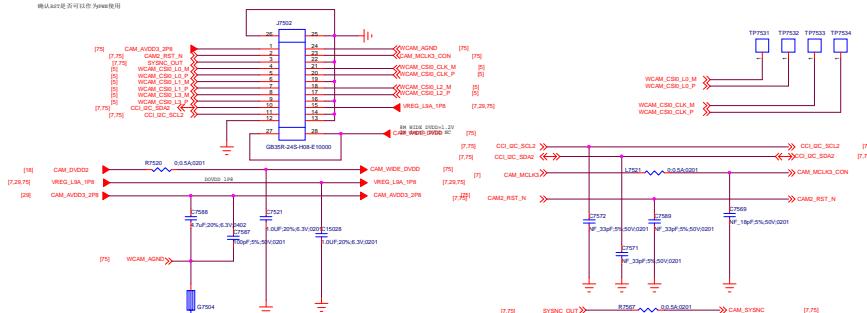


41\_CAMERA IF

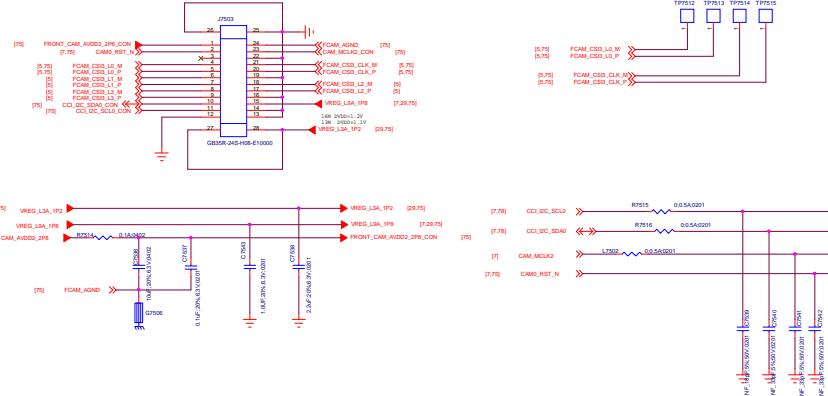
Main Camera 50M



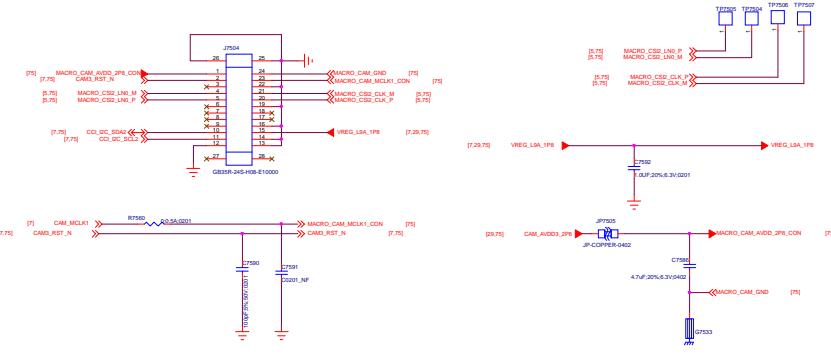
8MP Wide FF



Front Camera 16MP  
8MP/13MP compatible

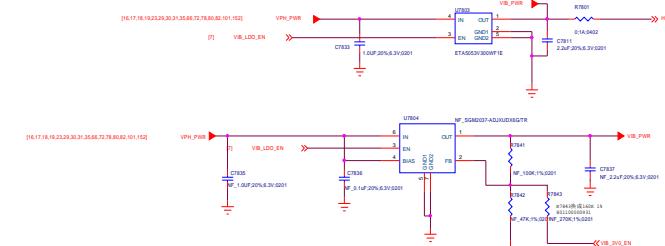
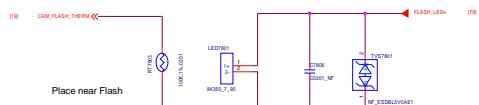


Macro Camera 2M

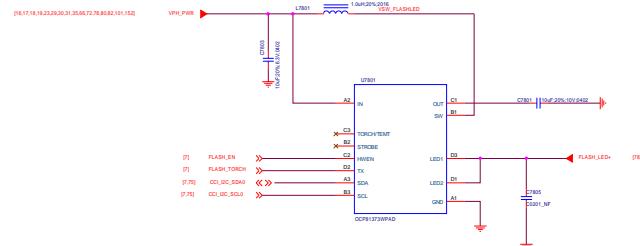


# 078\_Flash/RGB/Vibrator

## Flash LED

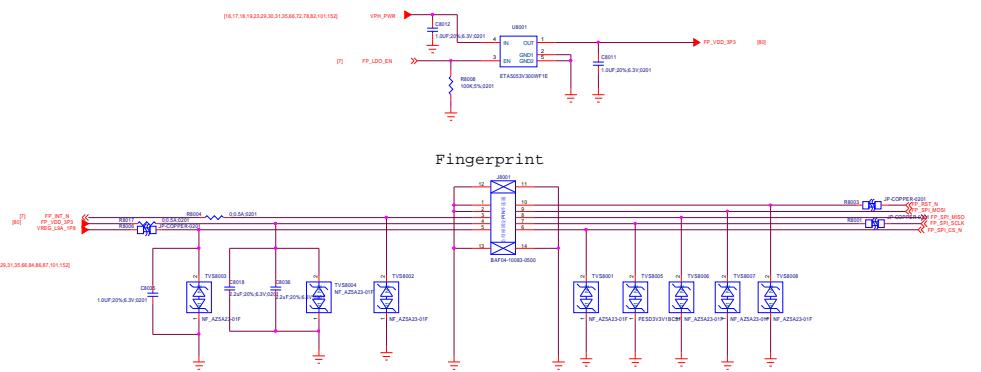


## Flash Driver



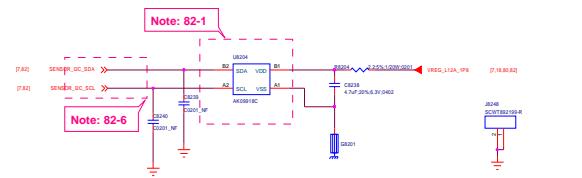
# 080\_FingerPrint

## CONNECTOR

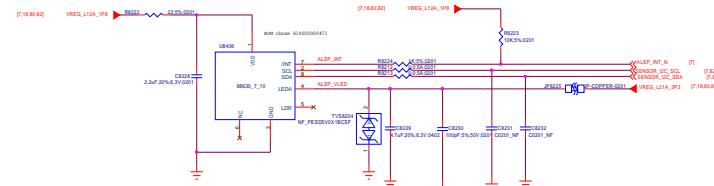


082\_SENSORS

## M-SENSOR

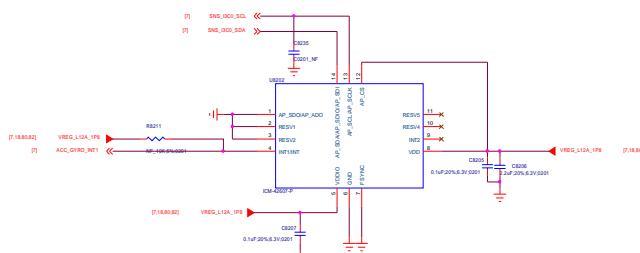


ALS+PS+IR



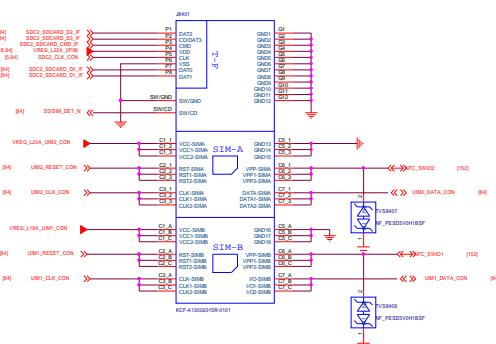
Substation No.	Client Address	Port	Version
SCB8506	0E14	5555	0.0.1

Gyro Sensor

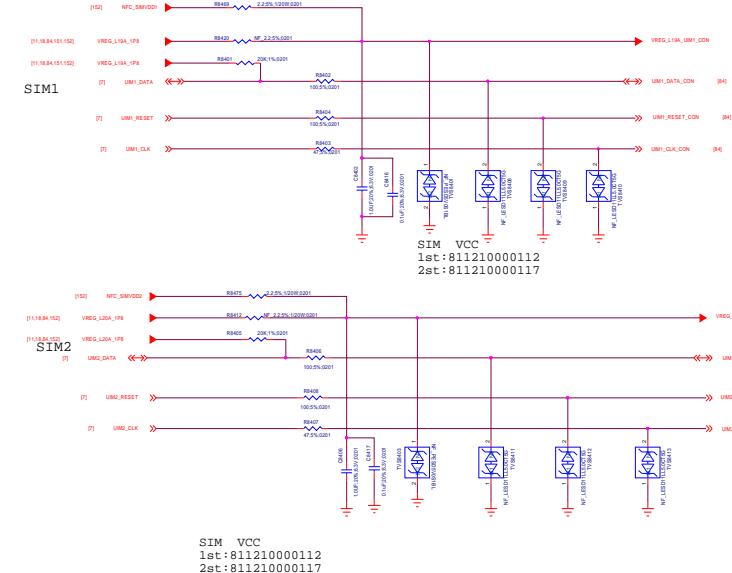


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2ST:813300002271

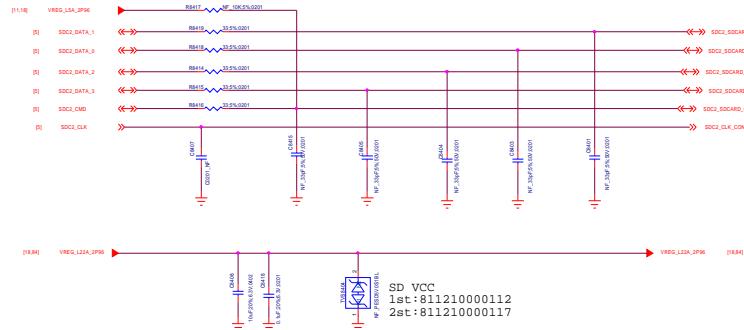
### SIM & T\_Card Slot



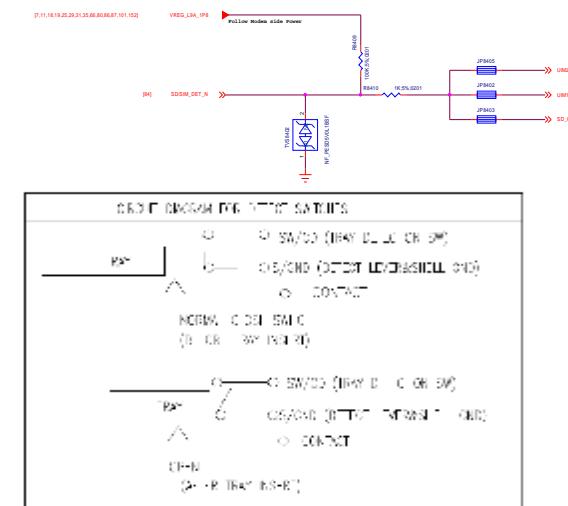
### SIM CARD



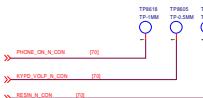
### T\_Card



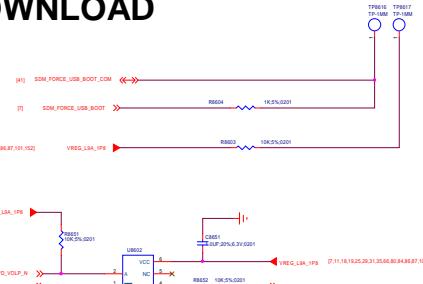
### Detect



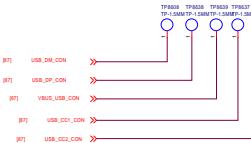
## SIDEKEY



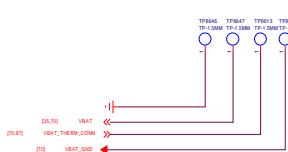
## 9008 DOWNLOAD



## USB



## Battery



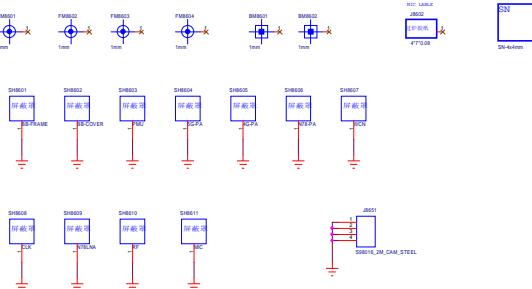
## UART



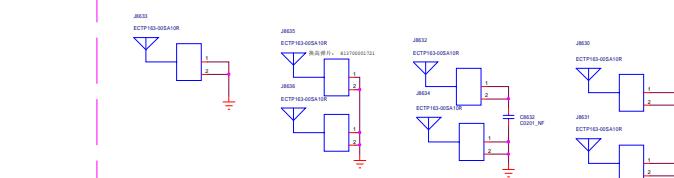
## JTAG



## MARK/Shield/Label/PCB

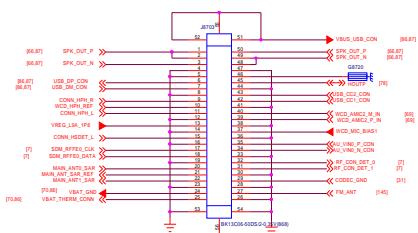


## Hole



087\_Sub PCB IF / USB IF

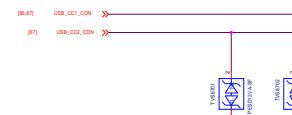
CC IF



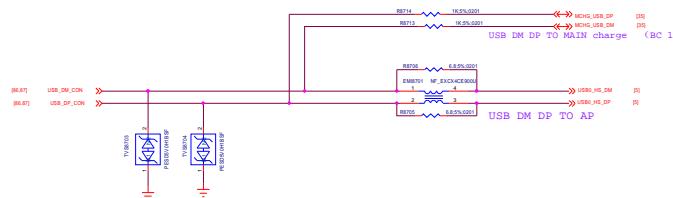
OVP



10.5W



USB IE



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# 100.Customer\_RFI

REVISIONS			
VER	DESCRIPTION	DATE	APPROVED
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1	LAST_EDITOR	2-23-2007_10:06

**101.RF\_Block**

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		

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REV: V10	DOC. NO.: S84386_1_16_30228016_R000	DESIGNER: Kim WM
WINGTECH		
Tuesday, December 01, 2021	Sheet 001 of 102	

# 102.RF\_Transceiver\_SDR735 WMSS

REV	DESCRIPTION	DATE	APPROVED
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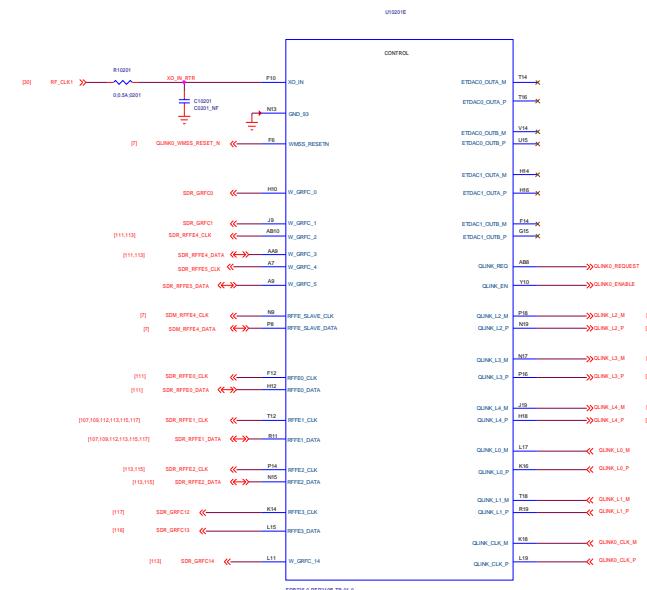
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102.RF_Transceiver_SDR735 WMSS Rev: Y10	
DOCUMENT NO.: 084359_1_16_20230216_0059	Rev: Custom
DEPARTMENT: WINGTECH-XA	DESIGNER: Zou Wei
DATE: Tuesday, December 27, 2022	Page: 102 of 102

# 103.RF\_Transceiver\_SDR735\_TRX

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		

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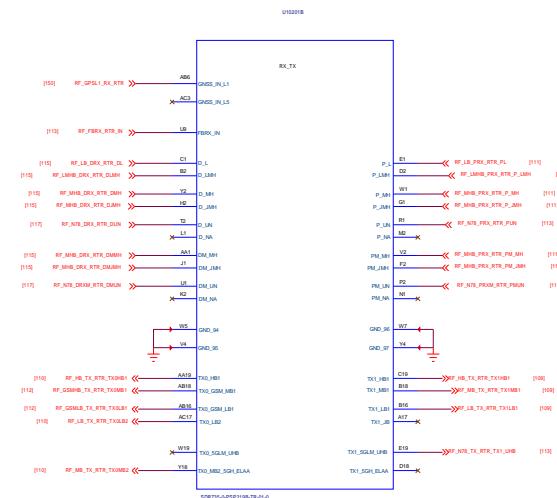
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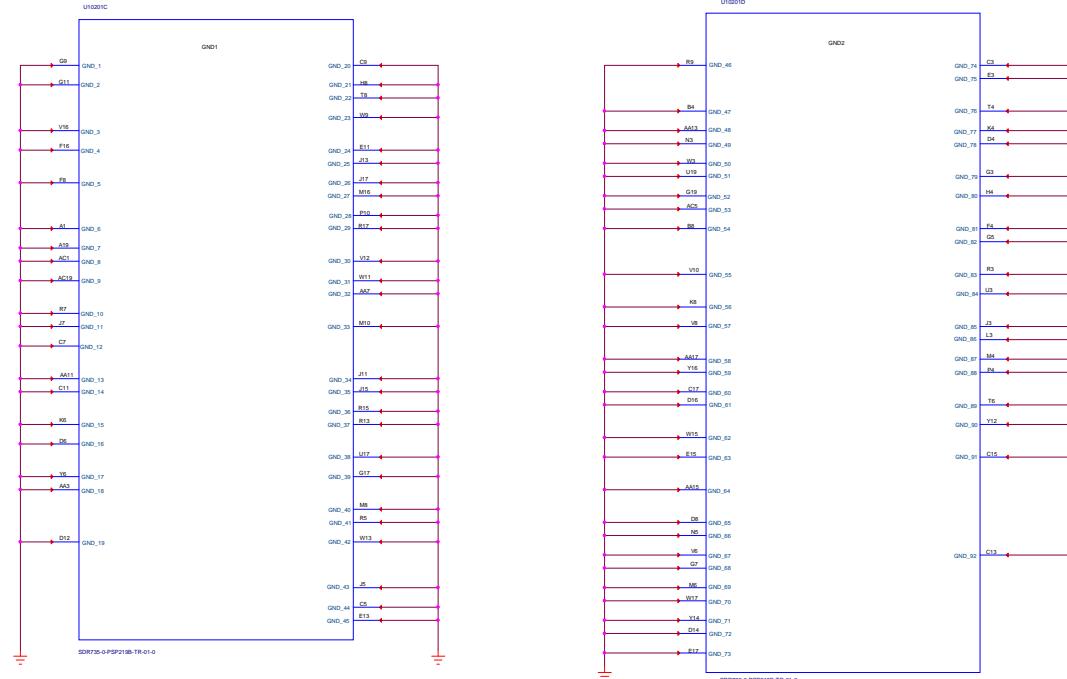
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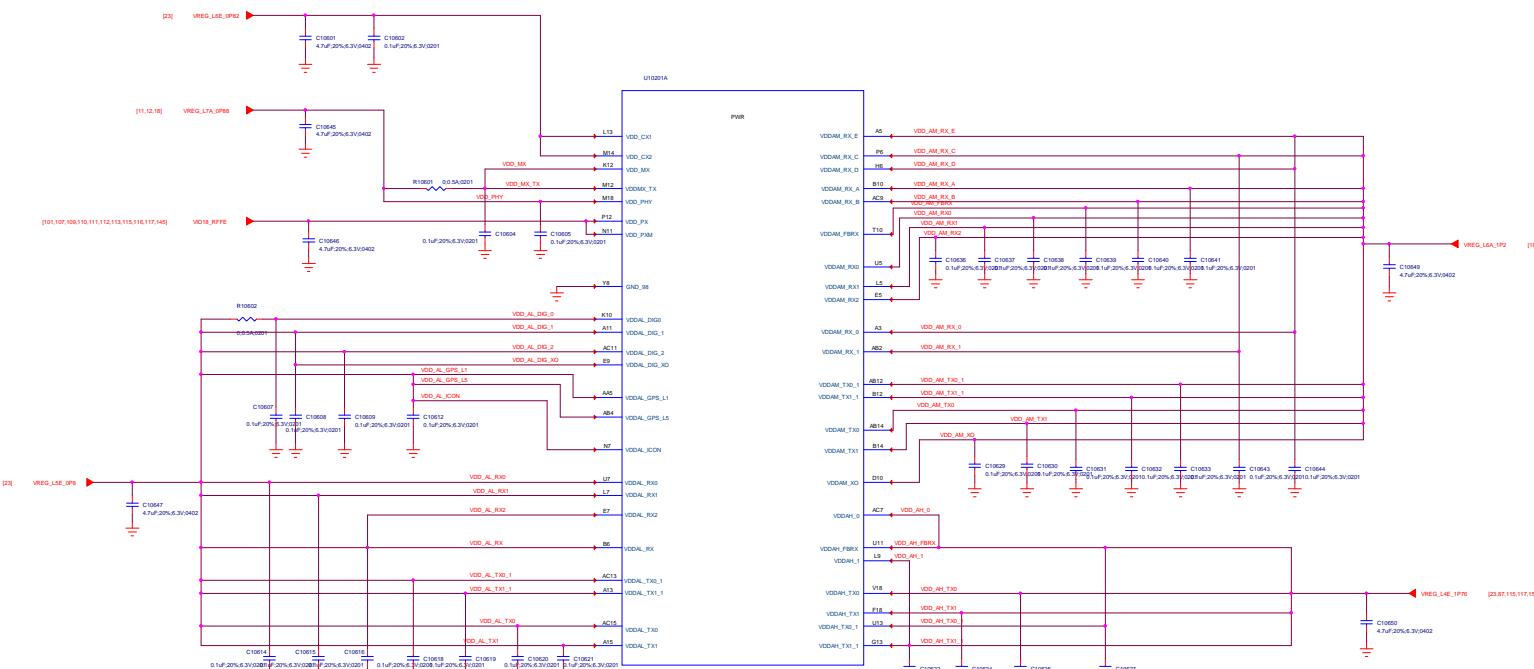
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DOCUMENT NO.: SB4350_1_V6_20230104_0009		Sheet: Custom
DEPARTMENT: WINGSONA		DISSEMINATE: Not Yet
Engineering	Engineering	Engineering
Tuesday, December 07, 2021	Sheet	103 of 103

# 105.RF\_Transceiver\_SDR735\_GND



105.RF_Transceiver_SDR735_GND		REV. V10
DOCUMENT NO.	S04309_1_16_20220216_889	Sheet 0
DEPARTMENT	WINGTECH-XA	DESIGNER
		Xun Wei
		<b>WINGTECH</b>
Date:	Tuesday, December 07, 2021	Sheet 105 of 132

## **106.RF\_Transceiver\_SDR735\_Power**



```

VDDL Max current (mA)
VDDL_DIG0 115.2mA
VDDL_DIG 1 28.8mA
VDDL_DIG 2 19.2mA
VDDL_DIG_XO 14.4mA
VDDL_GPS_L1 26.4mA
VDDL_GPS_L5 26.4mA
VDDL_ICON 6mA
VDDL_RX0 60mA
VDDL_RX1 84mA
VDDL_RX2 60mA
VDDL_RX 6mA
VDDL_TX0_1 78.32mA
VDDL_TX1_1 62.72mA
VDDL_TX0 14.27mA
VDDL_TX1 14.27mA
Total (mA) 333mA

```

VDDAM Max current (mA)  
VDDAM\_RX\_E 27.6mA  
VDDAM\_RX\_C 56.4mA  
VDDAM\_RX\_D 54mA  
VDDAM\_RX\_A 120mA  
VDDAM\_RX\_B 56.76mA  
VDDAM\_FBRX 32.4mA  
VDDAM\_RX0 126mA  
VDDAM\_RX1 126mA  
VDDAM\_RX2 126mA  
VDDAM\_RX\_0 60mA  
VDDAM\_RX\_1 84mA  
VDDAM\_TX0\_1 154.6mA  
VDDAM\_TX1\_1 36mA  
VDDAM\_TX0 21mA  
VDDAM\_TX1 21mA  
VDDAM\_XO 6mA

```

VDD_CX Max current (mA)
VDD_CX 316.45mA
VDD_CX 316.45mA
Total (mA)632.9mA
VDD_PHY/MX Max current (mA)
VDD_MX 32.4mA
VDDMX_TX 24mA
VDD_PHY 90mA
Total (mA)137mA
VDD_PX/PXM Max current (mA)
VDD_PX 3.6mA
VDD_PXM 3.6mA

```

VDDAH Max current (mA)  
 VDDAH\_0 10.8mA  
 VDDAH\_FBRX 12mA  
 VDDAH\_1 20.4mA  
 VDDAH\_TX0 40.2mA  
 VDDAH\_TX1 40.2mA  
 VDDAH\_TX0\_1 24mA  
 VDDAH\_TX1\_1 24mA  
 Total (mA)77mA

Title	REV: V10
DOCUMENT NO.: Design Name = S84350_1_16_20220216	0009 D
DEPARTMENT: DEPARTMENT = RF_Xan	DESIGNER: DESIGNER = XA
<b>ENVINGTECH</b>	
Date: Page	Modify Date = Tuesday, December 06, 2022 (08:00)

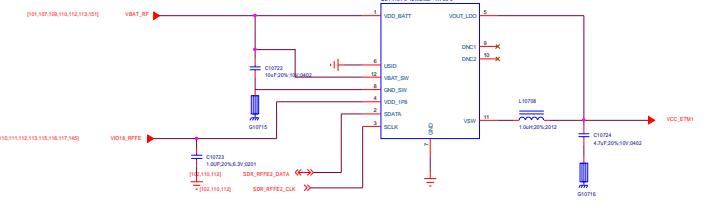
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LTR	DESCRIPTION	DATE	APPROVED
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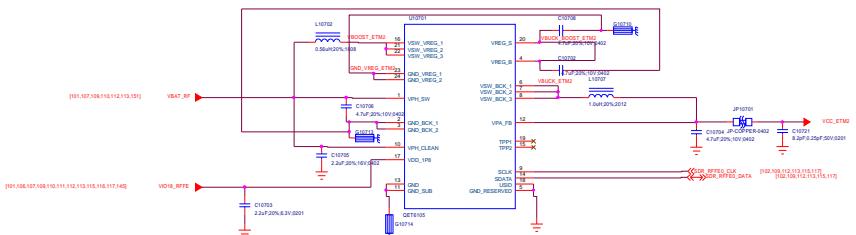
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QET6105\_CH1



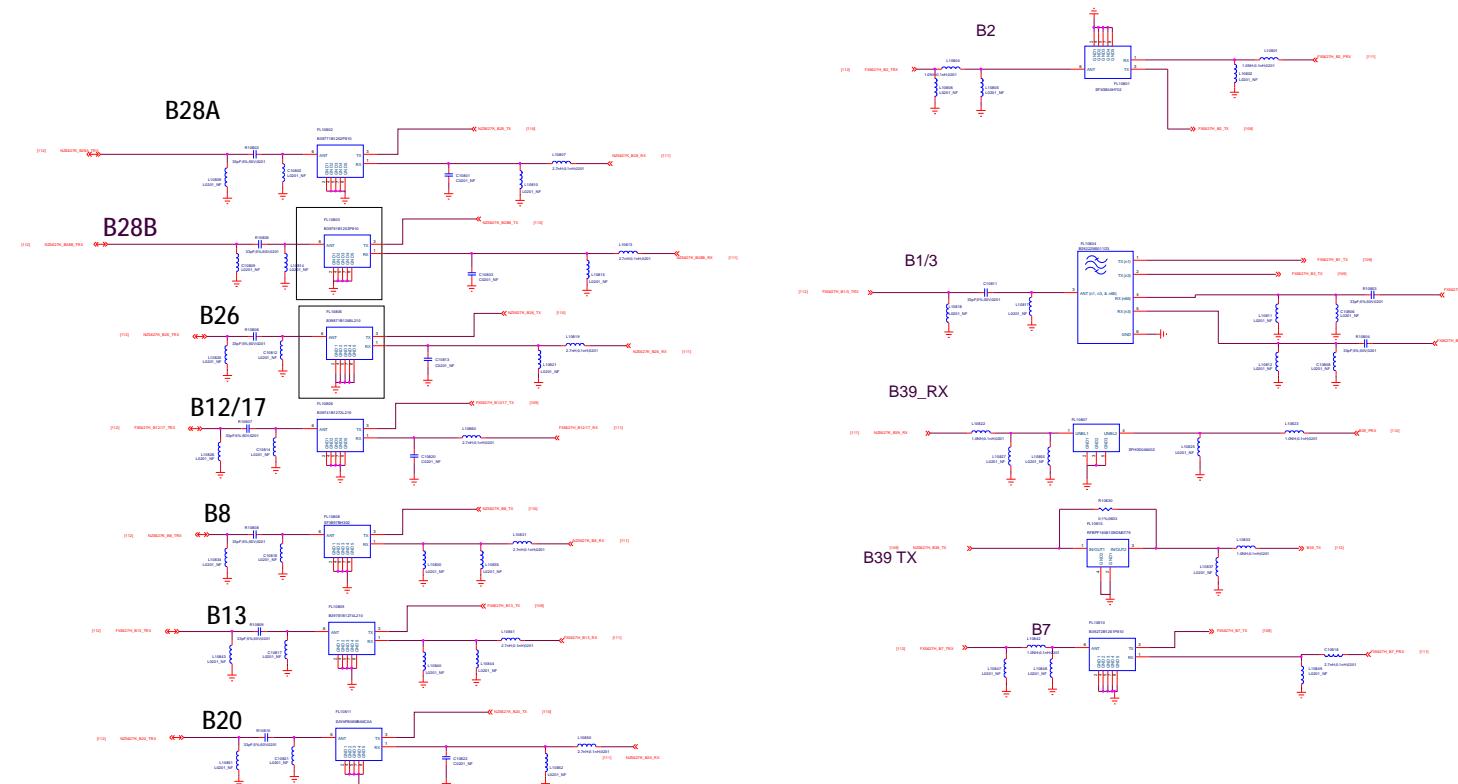
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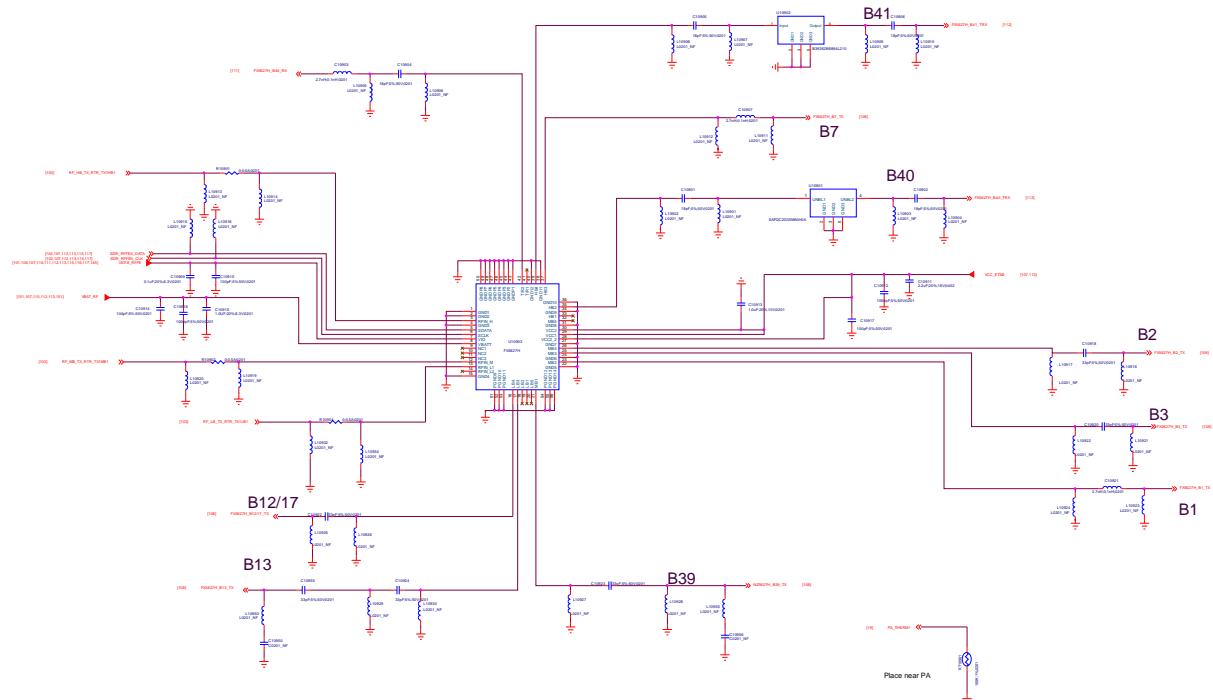
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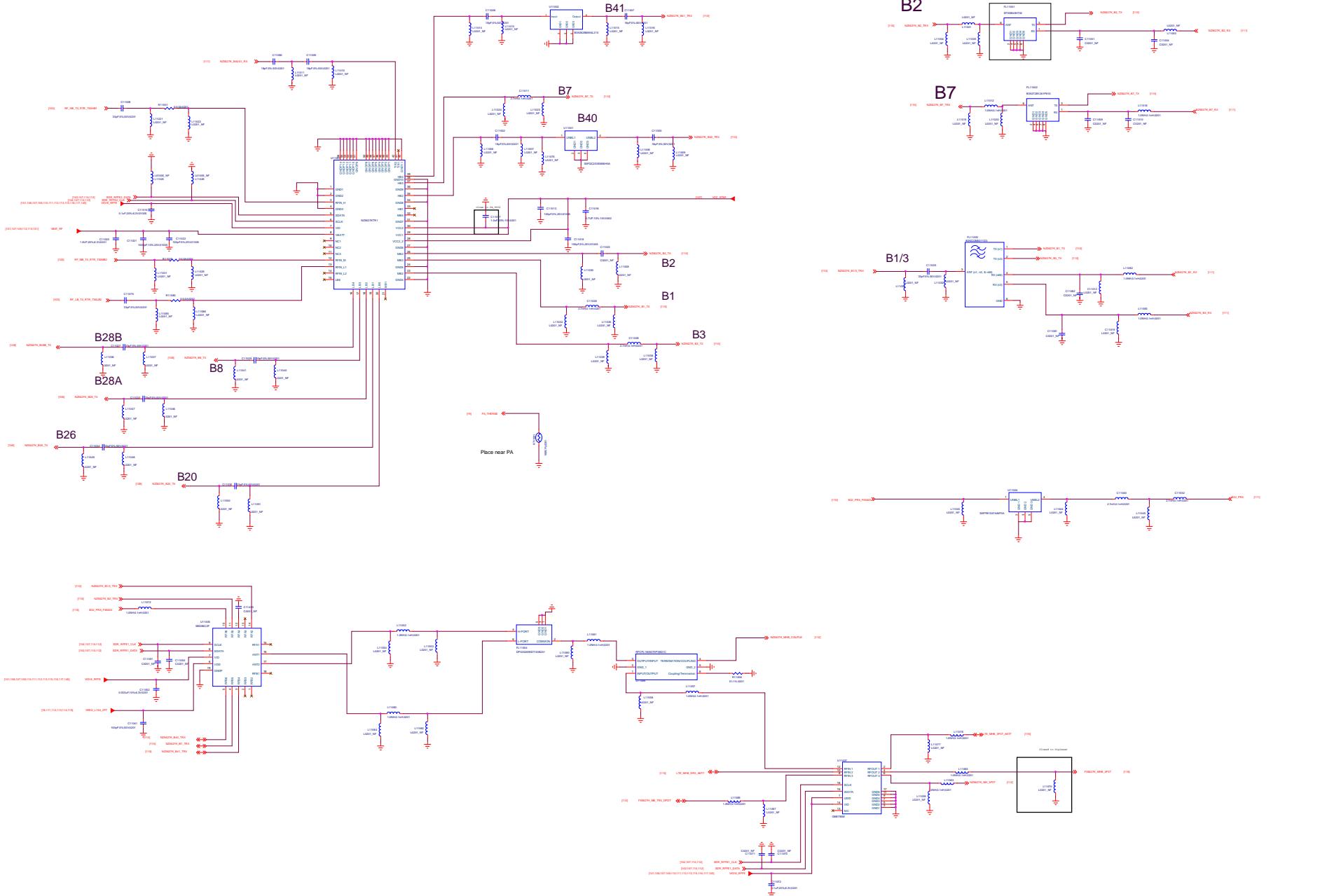
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<b>DOCUMENT NO:</b> S84350_1_16_20220216_0059		<b>Size</b> Custom
<b>DEPARTMENT:</b> WINGTECHXA	<b>DESIGNER:</b> Xu Wei	
<b>WINGTECH</b>		
<b>Date:</b> Tuesday, February 14, 2022	<b>Sheet</b> 1/17	<b>of</b> 1/17



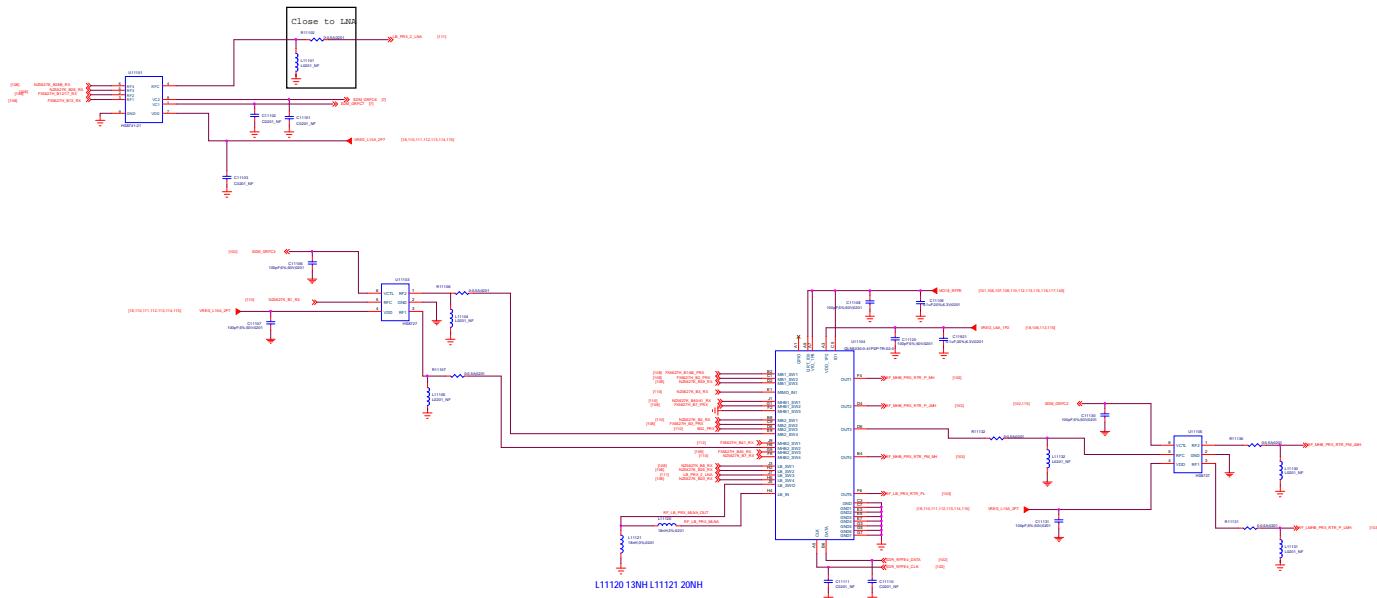


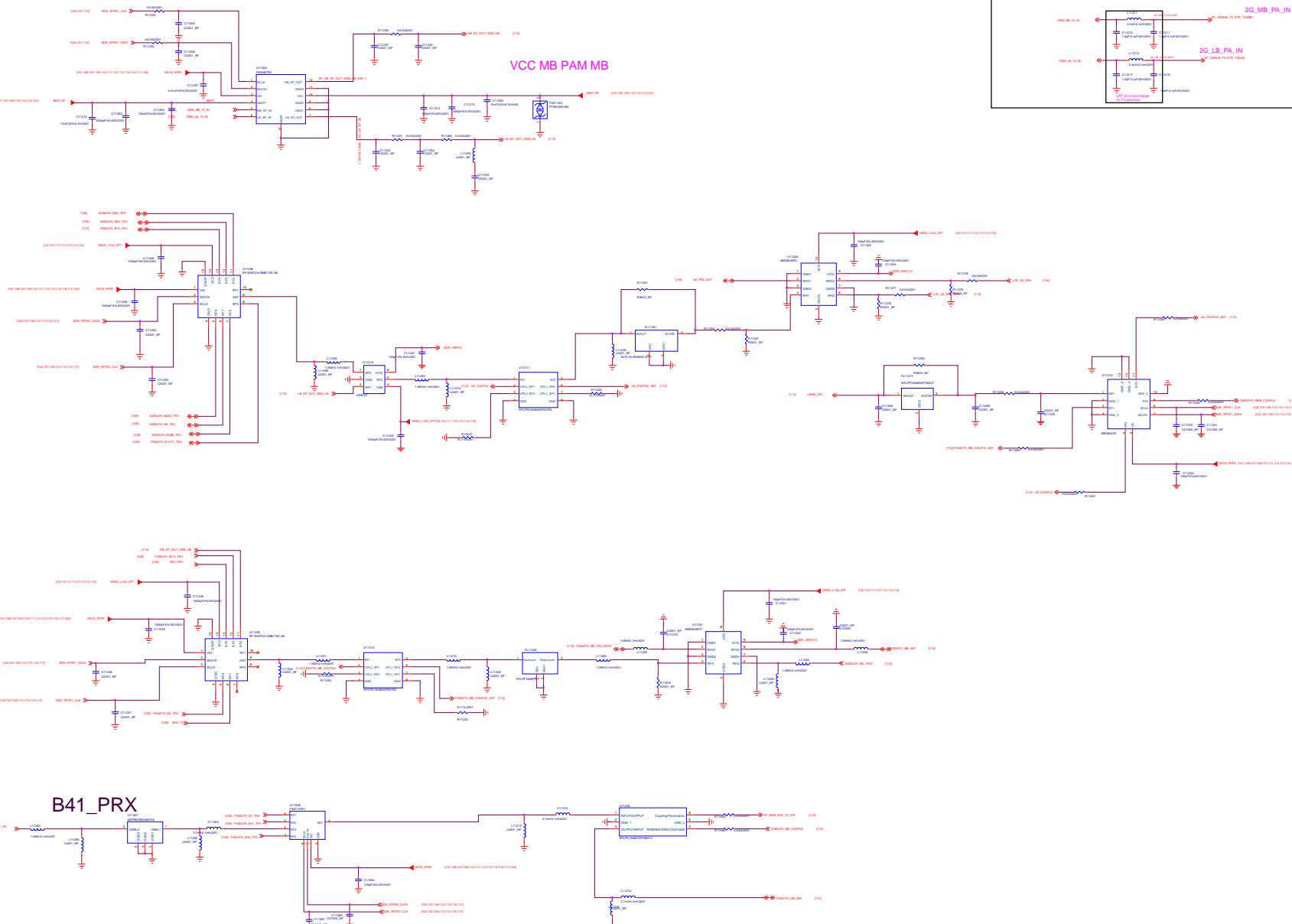
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Document Type:	Operational Amplifier
Document Status:	Production
Page Number:	109

110.NZ5627KTR1



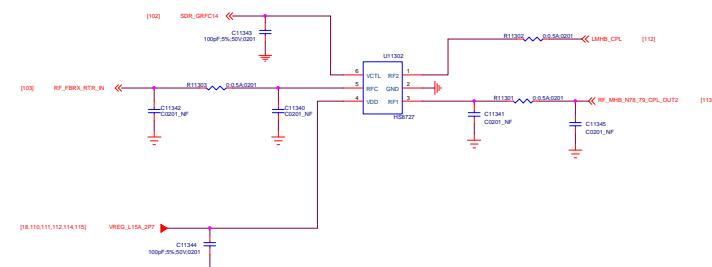
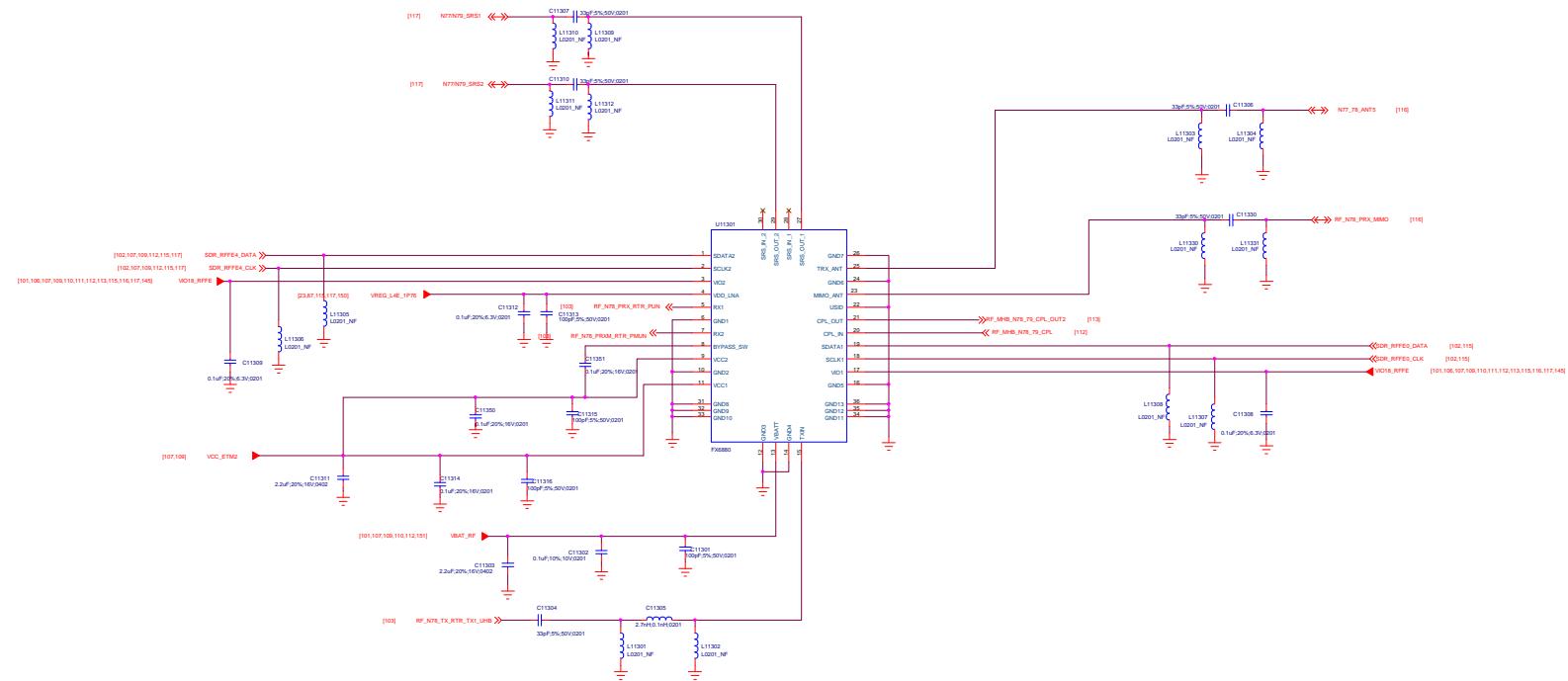
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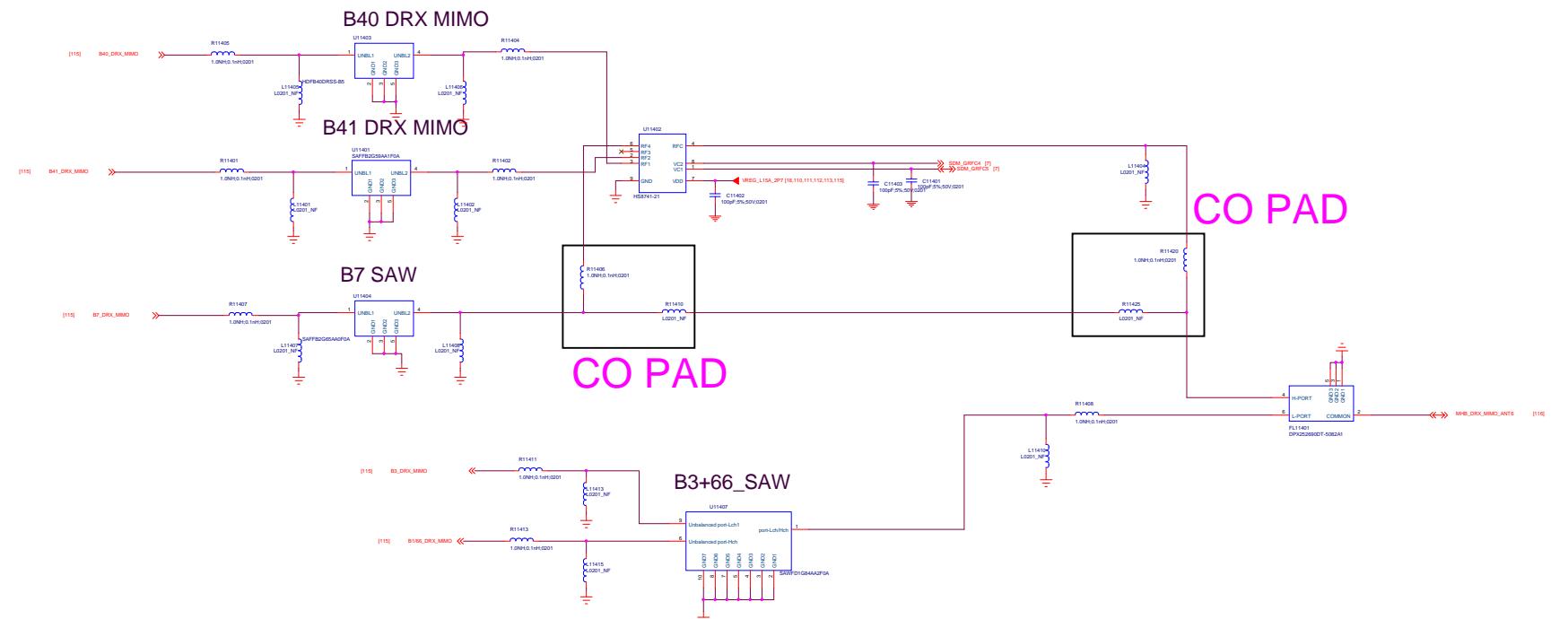


# B48/N77/78\_TRX

## N78 SRS&TRX



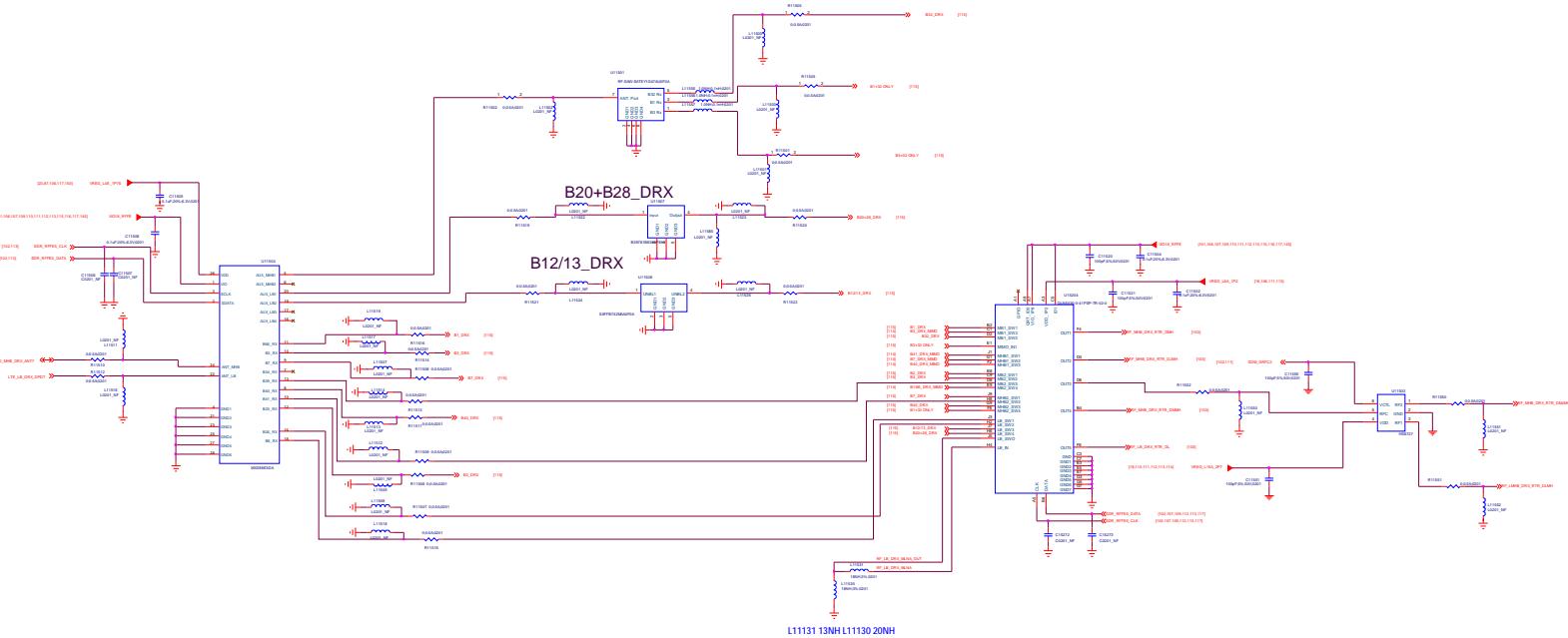
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DOCUMENT NO.:	Design Name = 584380_1_14_26232814, Rev. D
DEPARTMENT:	DEPARTMENT = RF
DESIGNER:	DESIGNER = Ren

Page Modify Date = Tuesday, December 11, 2018 114 of 152

B1+3+32\_SAW



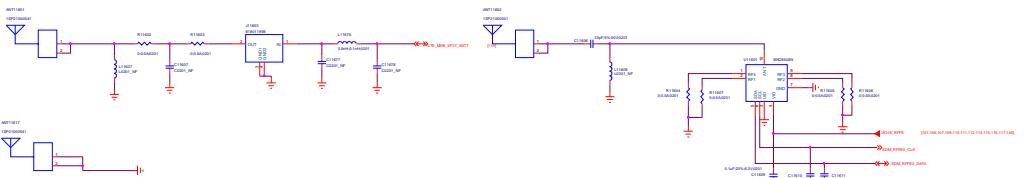
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# ANTO

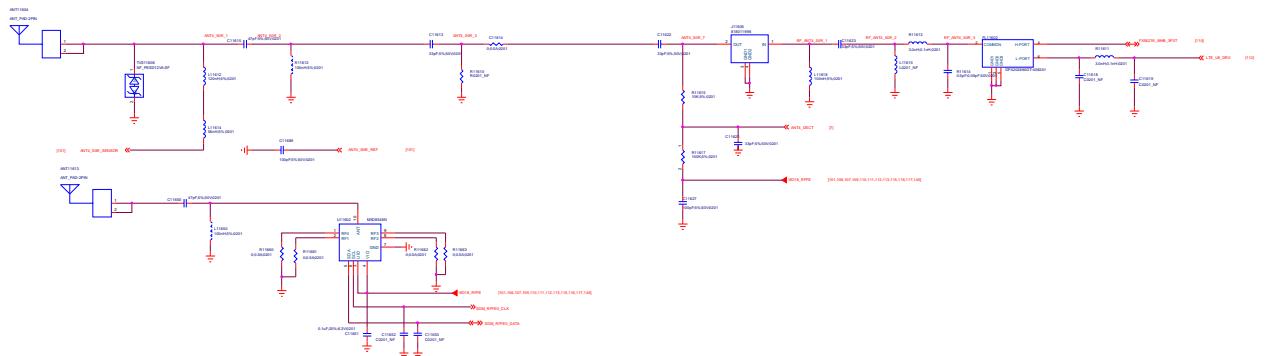
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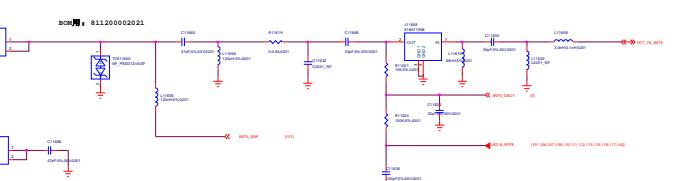
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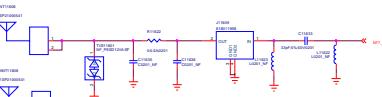
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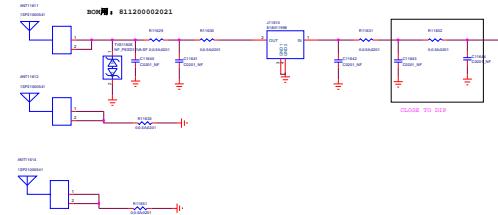
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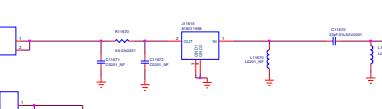
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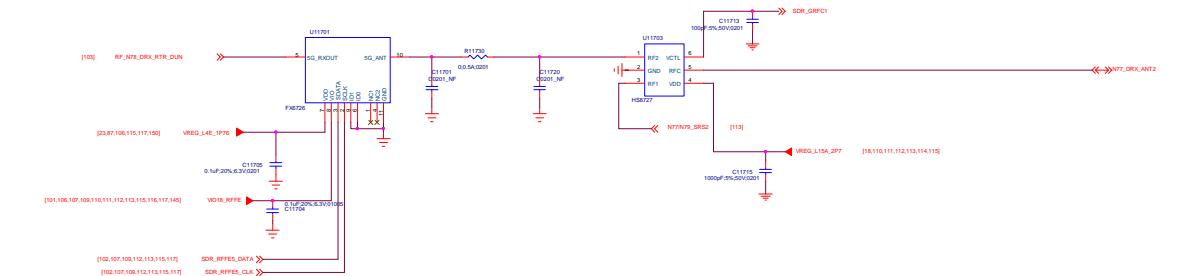
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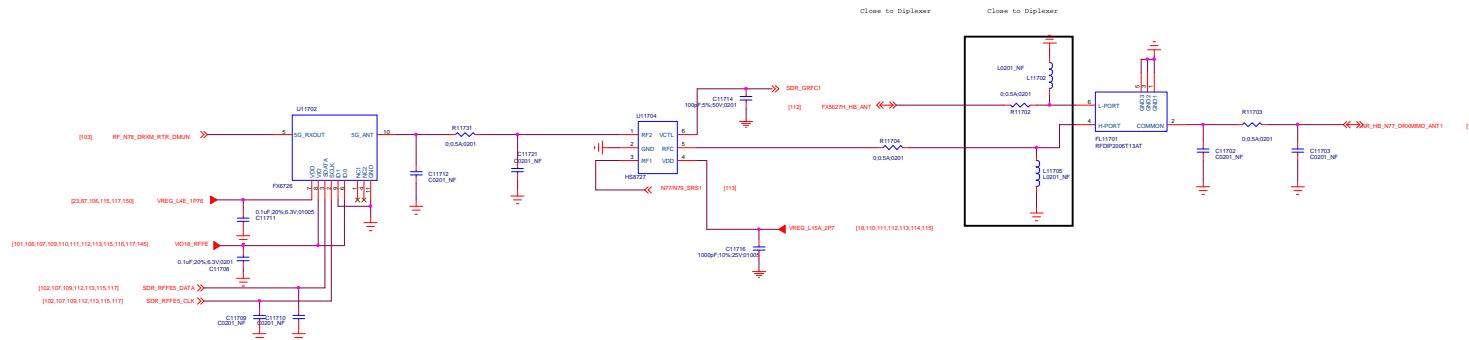
ANT3



### N77\79\_DRX



### N77\79\_DRX\_MIMO



8 7 6 5 4 3 2 1



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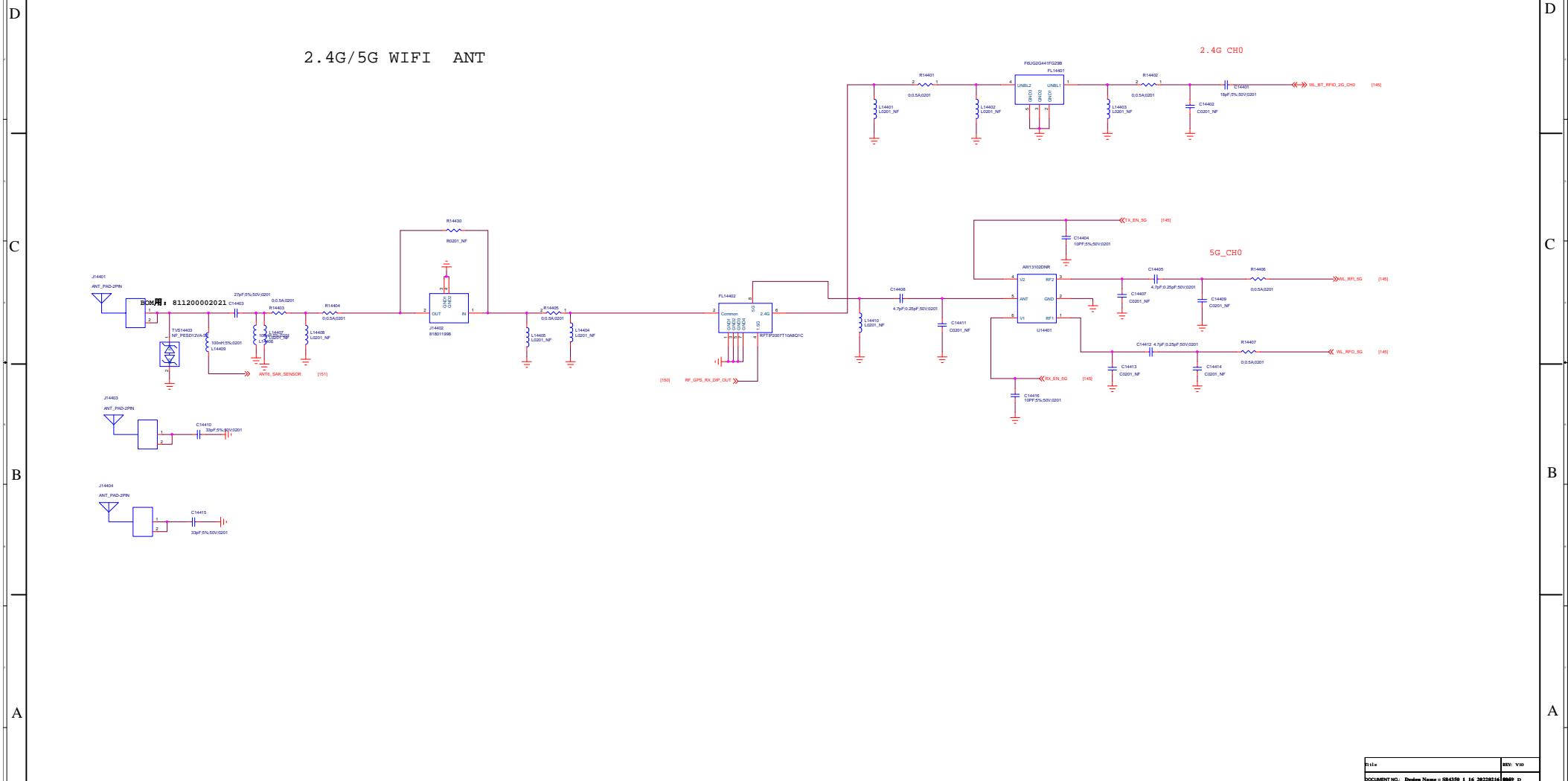
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REVISION:	INITIAL RELEASE		
EFLINGTECH			Sheet 141 of 152
Date: Tuesday December 07, 2021			

8 7 6 5 4 3 2 1

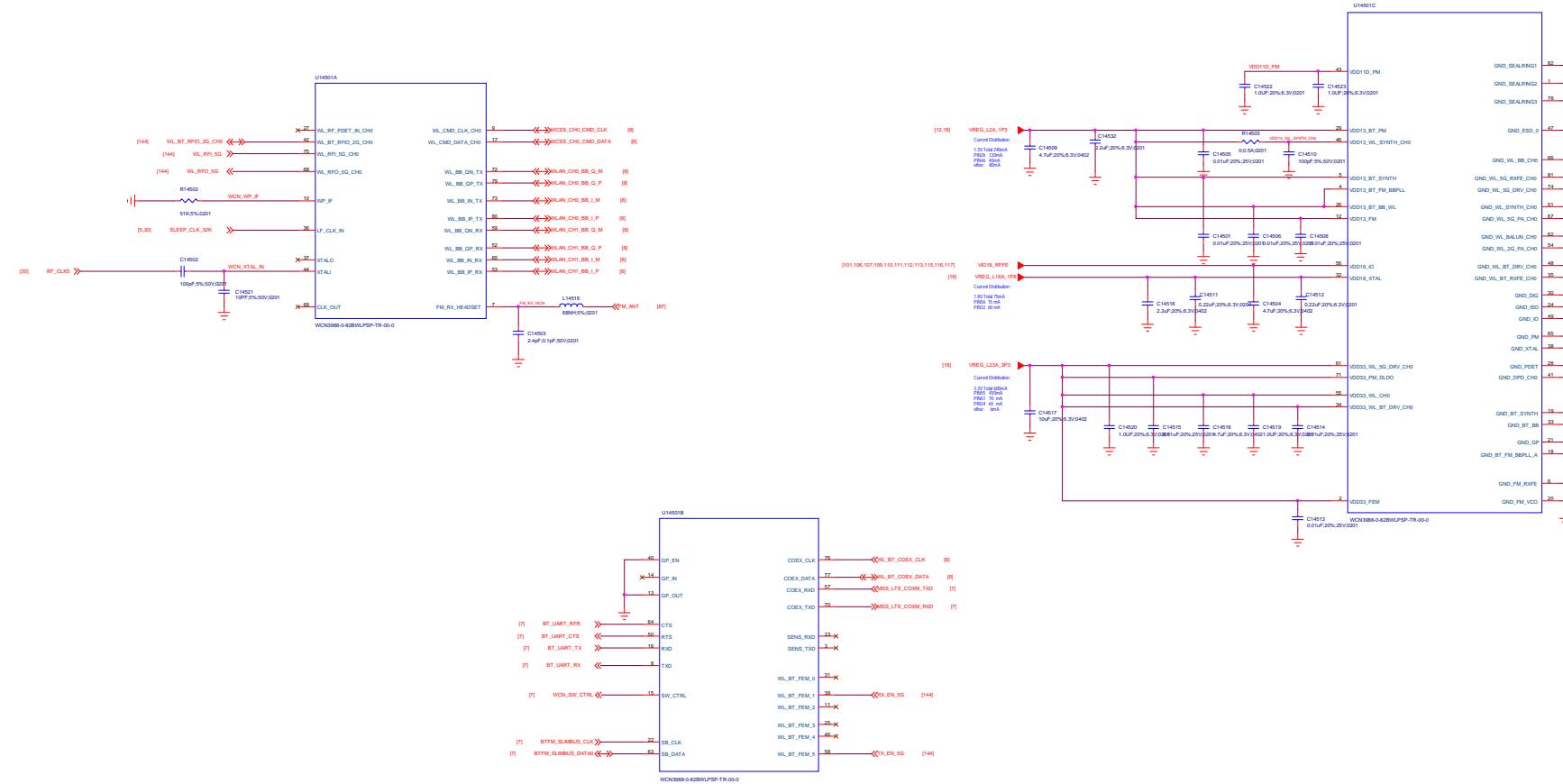
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# 144.Connectivity\_ANT



# **145.Connectivity\_WCN3988**

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# 150.GPS

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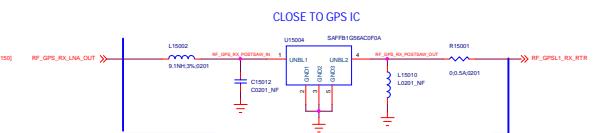
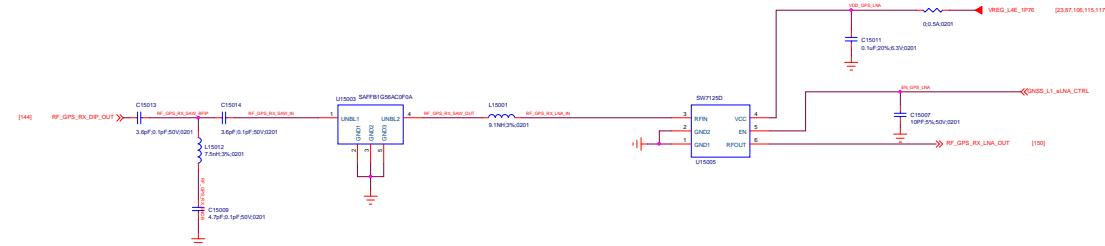
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DEPARTMENT:	DEPARTMENT : RF_XW DESIGNER: DESIGNER : XA0016
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Date: Page Modify Date : Thursday, December 09, 2021 2021 2021 2021	

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## 151.Sar\_sensor

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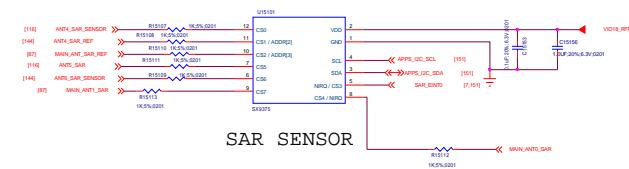
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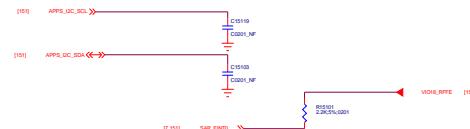
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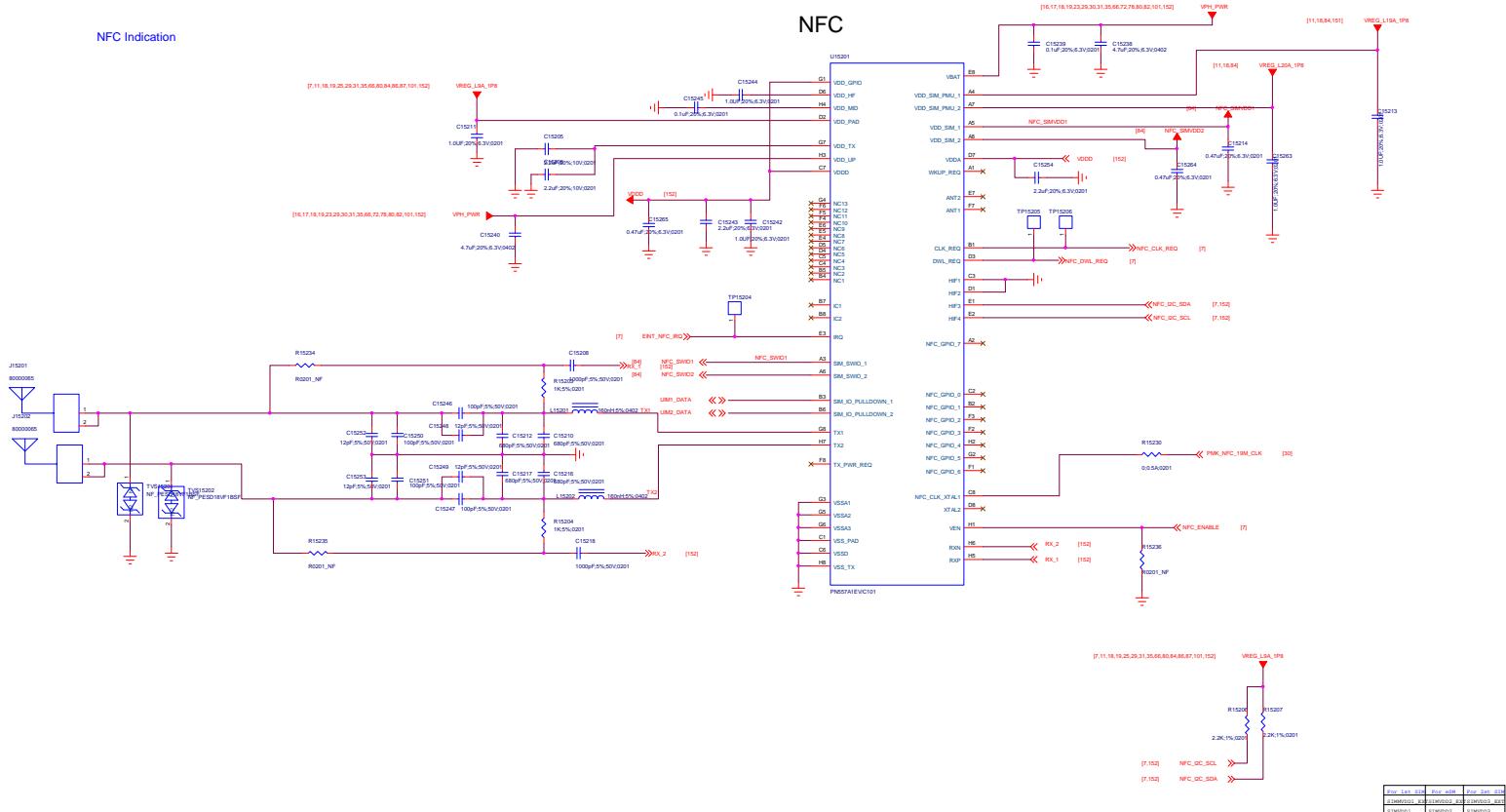
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## SAR\_Control &amp; Pull-up



Page Number	Version	Date
151	V10	
DOCUMENT NO.	Designation: 151.Sar_sensor	Category: Current
DEPARTMENT:	DESIGNER:	REVIEWER:
Rev.:	Page Number:	Page No.:



Title	152_NFC_PN557	REV: V10
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DEPARTMENT:	WINGTECH-SH	DESIGNER: Ishengli
Date:	Tuesday, December 21, 2021	Sheet 152 of 152