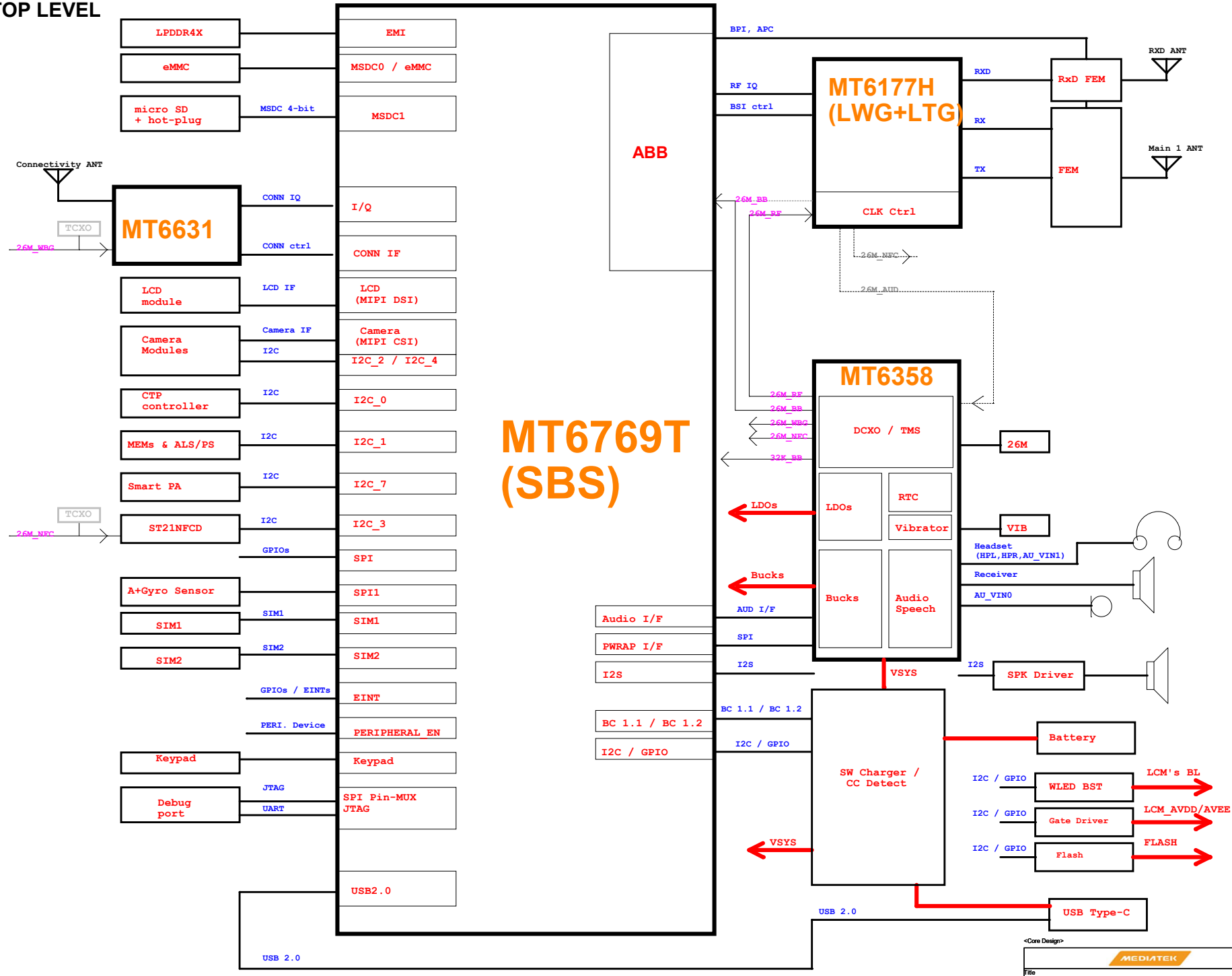
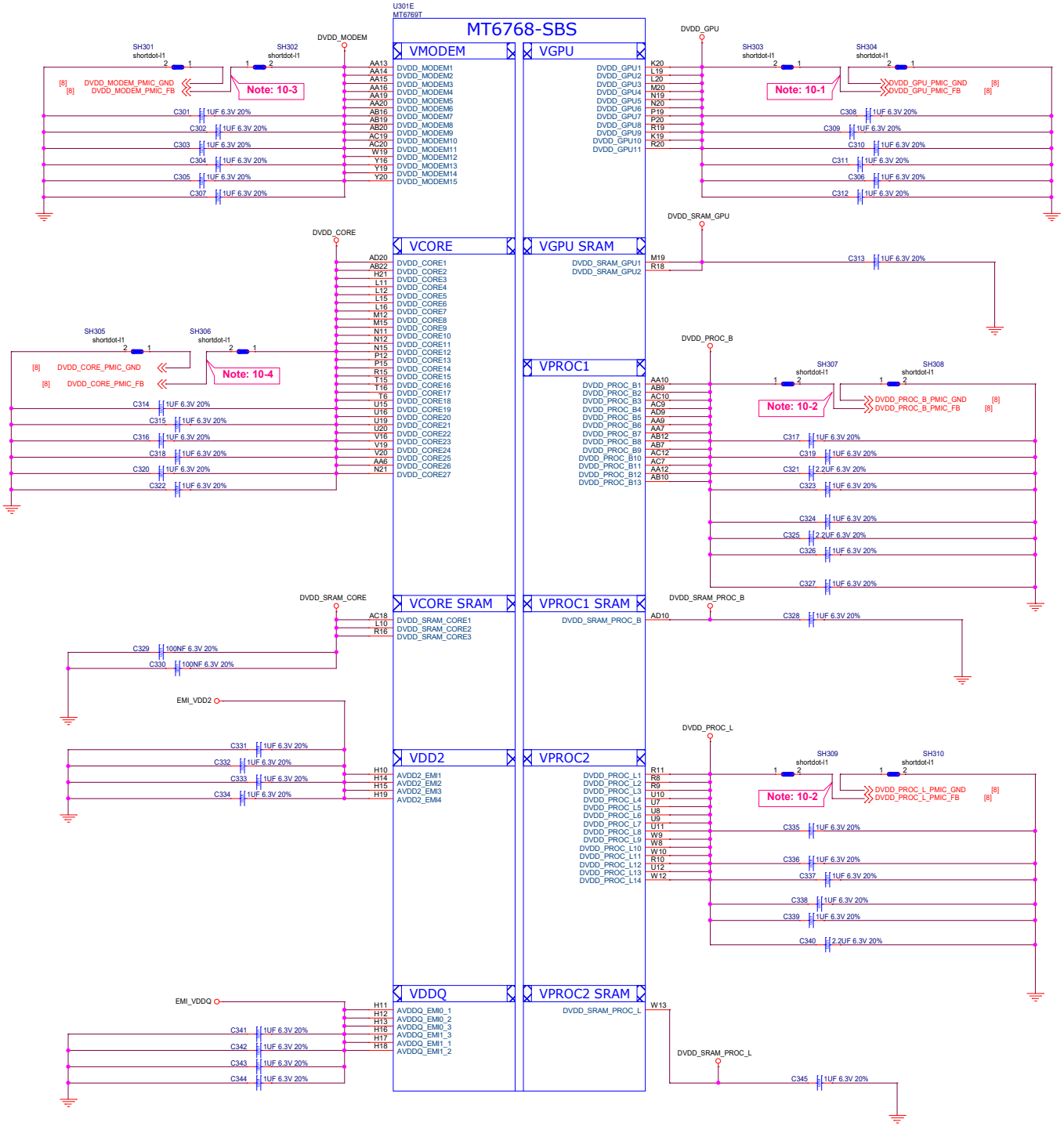
Project : MT6769T LPDDR4x Internal
REF_SCH TOP LEVEL



Date	Category	Item
2020 /6/3		



Schematic design notice of "10_BB_ POWER_PDN" page:

Note 10-1: Differential pair of DVDD_GPU remote sense must be close to BB's ball.
Remote sense trace with GND shielding to PMIC (Differential)

Note 10-2: Differential pair of DVDD_PROC remote sense must be close to BB's ball
Remote sense trace with GND shielding to PMIC (Differential)

Note 10-3: Differential pair of DVDD_MODEM remote sense must be close to BB's ball.
Remote sense trace with GND shielding to PMIC (Differential)

Note 10-4: Differential pair of DVDD_CORE remote sense must be close to BB's ball.
Remote sense trace with GND shielding to PMIC (Differential)

<Core Design>

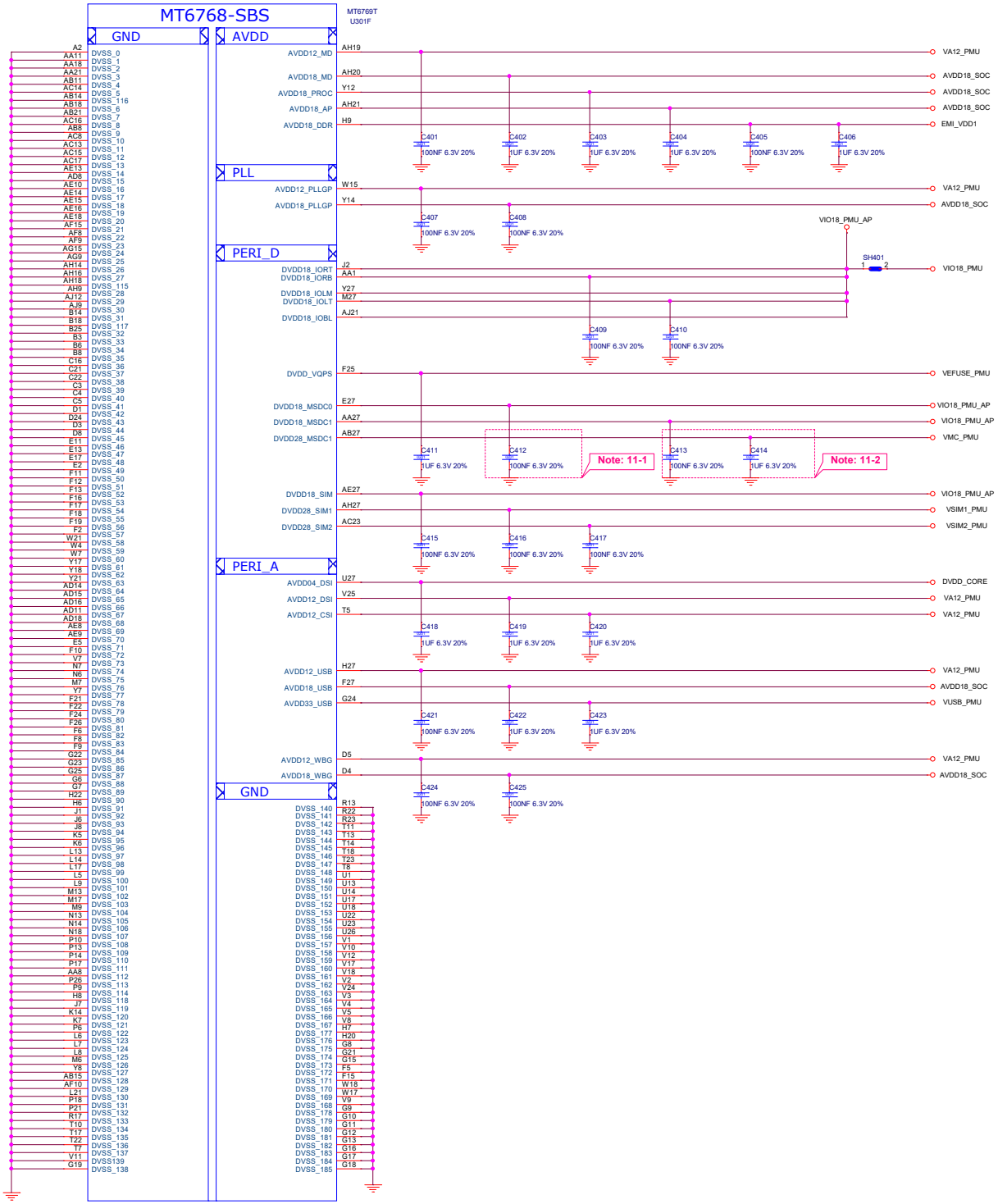
MEDIATEK

Title: 10_BB_ POWER_PDN

Size: C

MTK Confidential

Date: Friday, July 23, 2021 Sheet 3 of 32



Schematic design notice of "11_BB_POWER_IO" page:

Note 11-1: C412 closed DVDD18_MSDC0 150mil

Note 11-2: C413 closed DVDD18_MSDC1 150mil
C414 closed DVDD28_MSDC1 150mil

<Core Design>

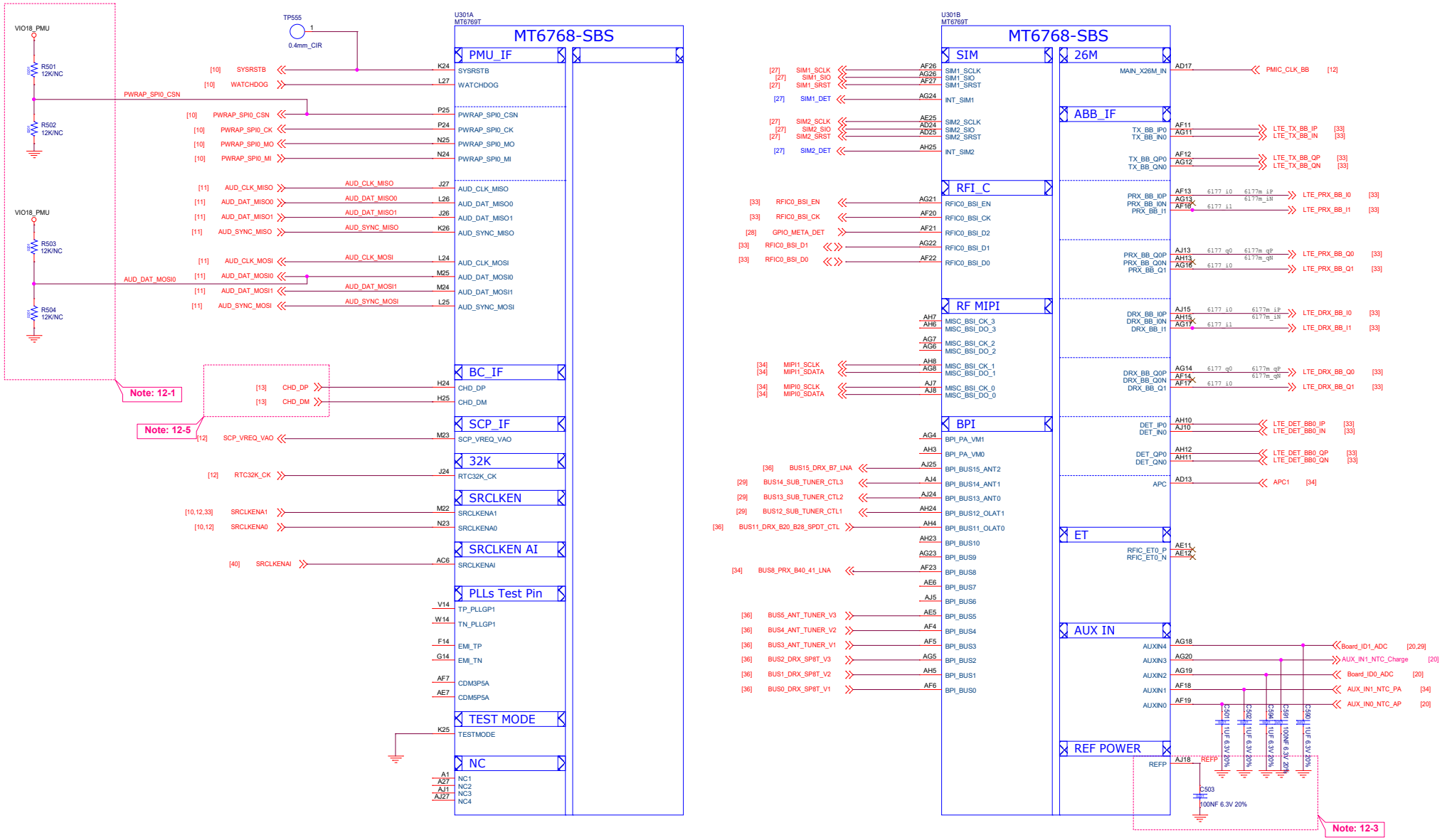
MEDIATEK

Title

Size Custom

MTK Confidential

Date: Friday, July 23, 2021 Sheet 4 of 32



Schematic design notice of "12_BB_1" page:

Note 12-1: PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pins to select which interface will be the JTAG pin out

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	JTAG Function	
default=PU	default=PD	AP_JTAG	MD_JTAG
HI	LO	N/A	N/A
HI	HI (by ext. PU)	SPI0 + EINT8	SPI2 + SPI3
LO (by ext. PD)	LO	SPI0 + EINT8	N/A
LO (by ext. PD)	HI (by ext. PU)	N/A	N/A

Note 12-2: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

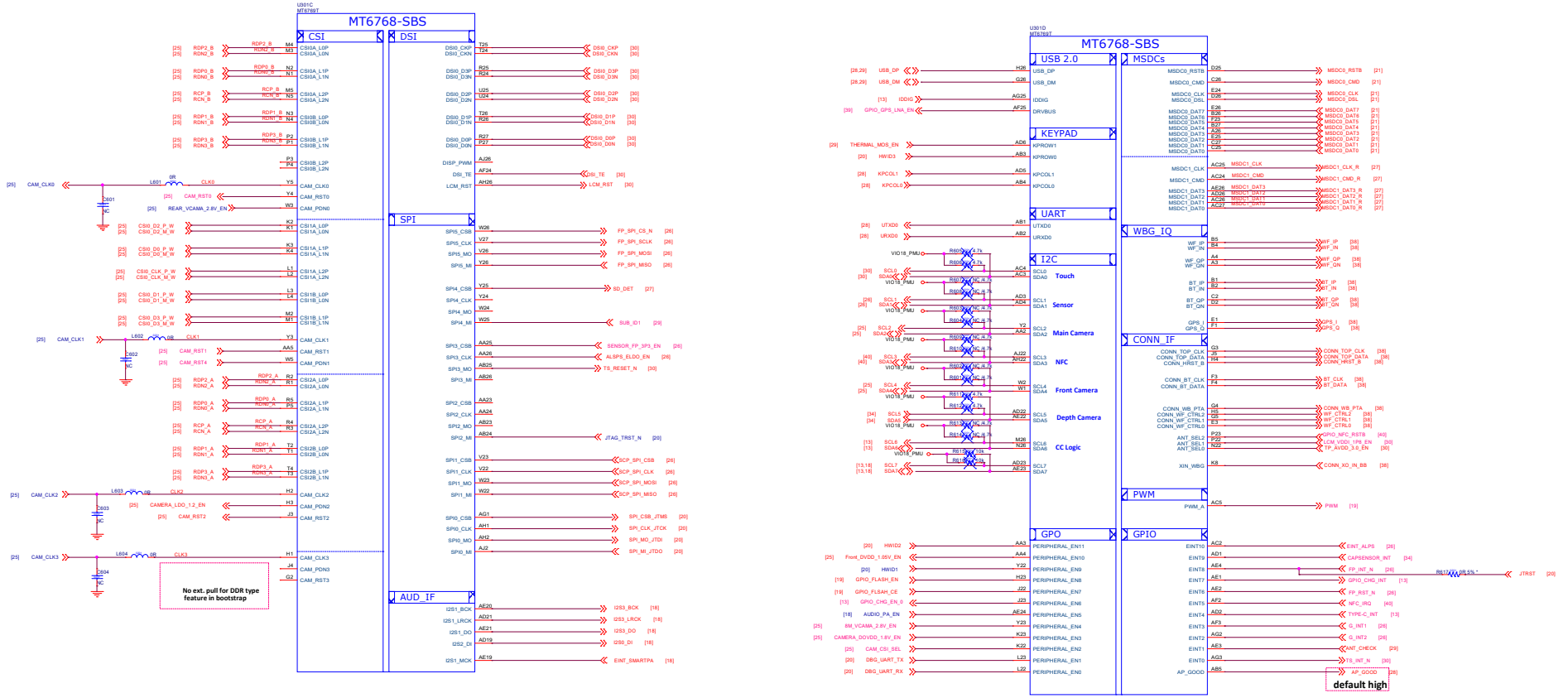
Note 12-3: The de-coupling cap. for REFP (AJ18 ball) have to be placed as close to BB as possible.

Note 12-4: HW pin for DDR type feature in bootstrap (refer to BB HW design Notice)

AUD_SYNC_MISO	AUD_CLK_MISO	CAM_PDN3	PMIC 6358 voltage	DDR Type
default=PD	default=PD	default=PD	VDRAM1 / VDRAM2	DDR
No ext. pull	No ext. pull	No ext. pull	1.125v / 0.6v	LP4X eMCP
No ext. pull	12K pull to VIO18	No ext. pull	OFF / 1.8v	Reserved
12K pull to VIO18	No ext. pull	No ext. pull	1.225v / OFF	LP3 eMCP
12K pull to VIO18	12K pull to VIO18	No ext. pull	1.125v / 1.8v	Reserved

Note 12-5:

Charger must have D+/D- pin for charger type USB detection.
Charger must have at least 500mA USB current for All charger type.



<Core Design>

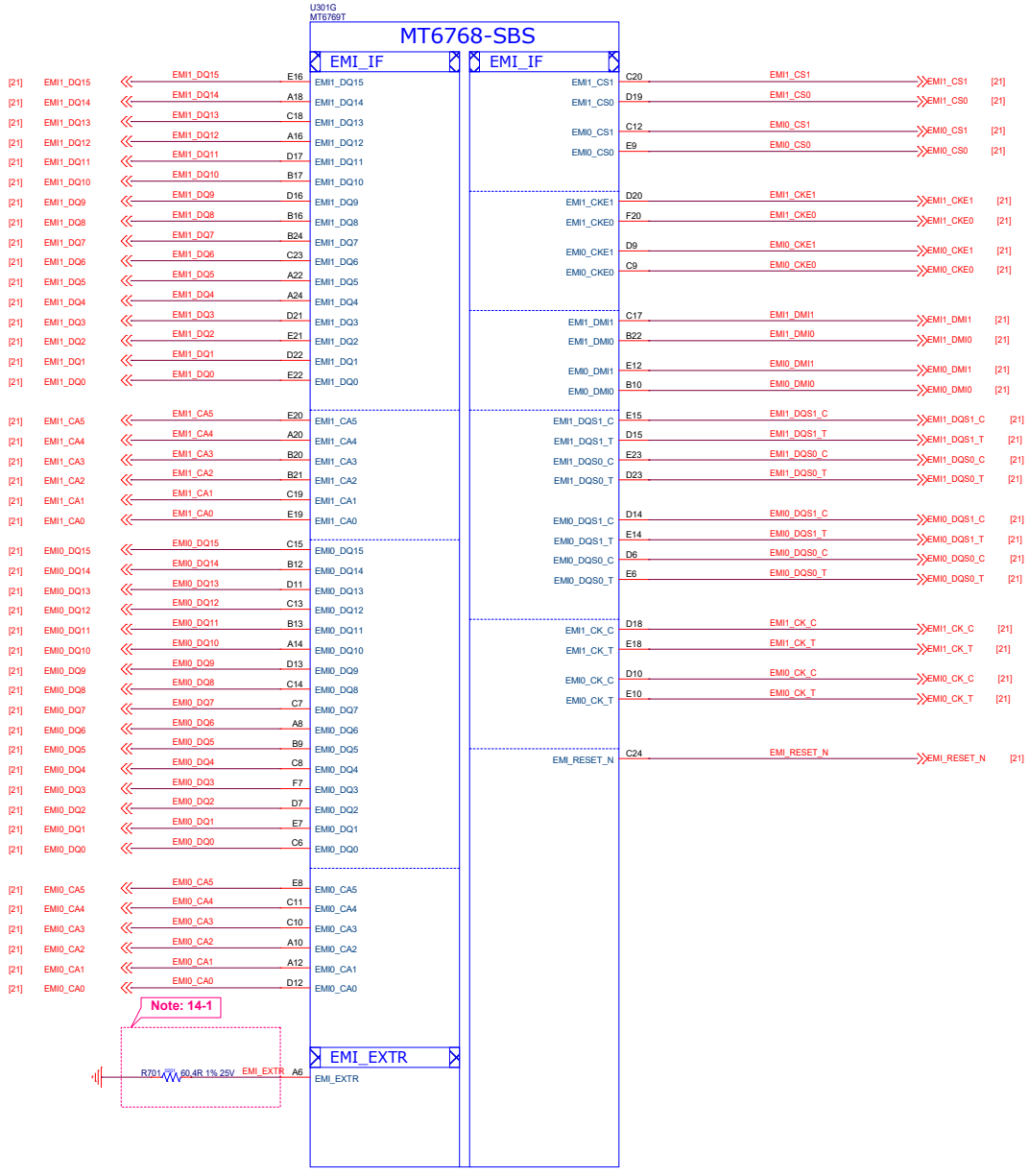
MEDIATEK

Title

Size: D

MTK Confidential

Date: Friday, July 23, 2021 Sheet 8 of 32



Schematic design notice of "14_BB_3" page.

Note 14-1: R701 please select 60.4 ohm (1%) resistor

<Core Design>

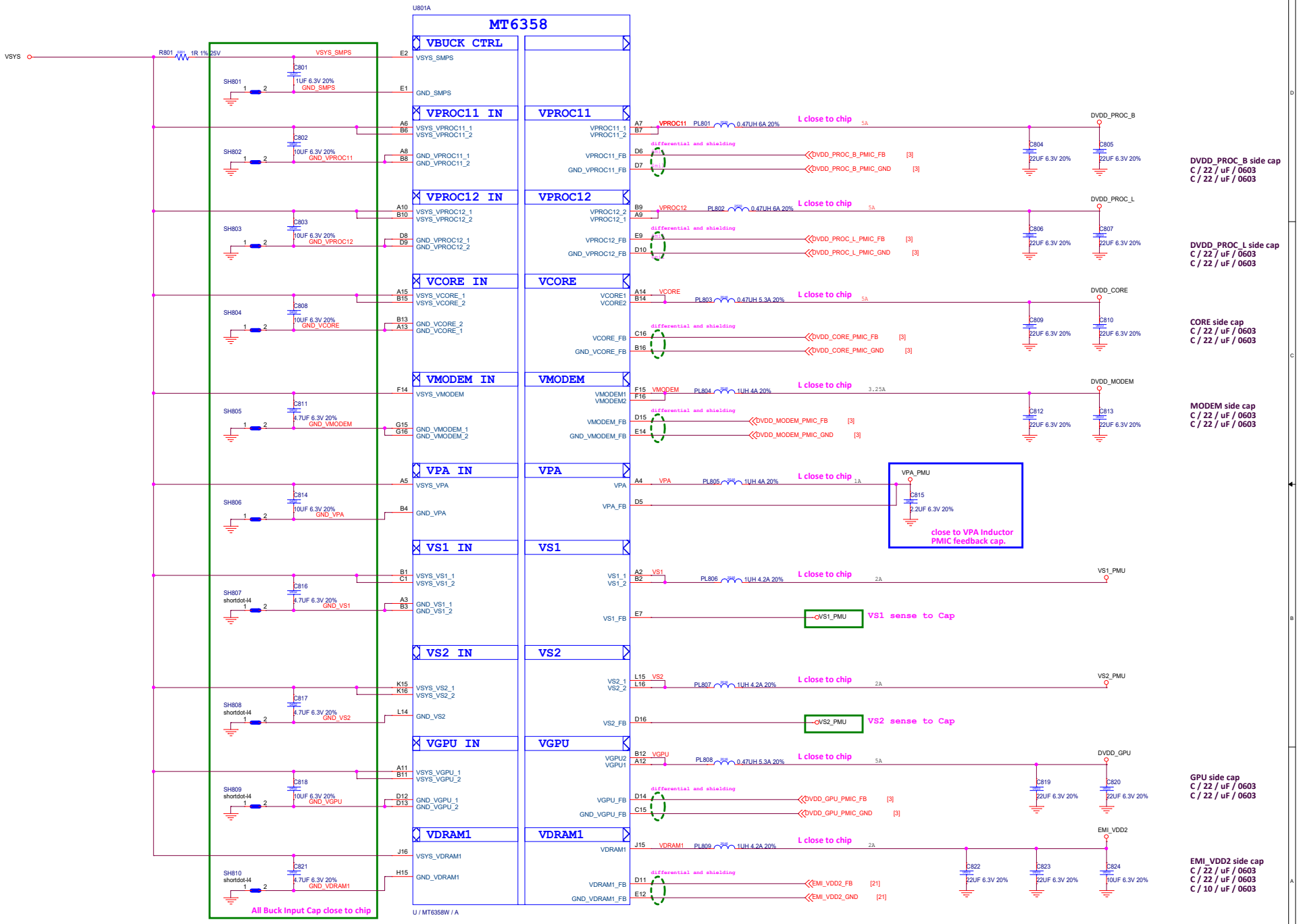
MEDIATEK

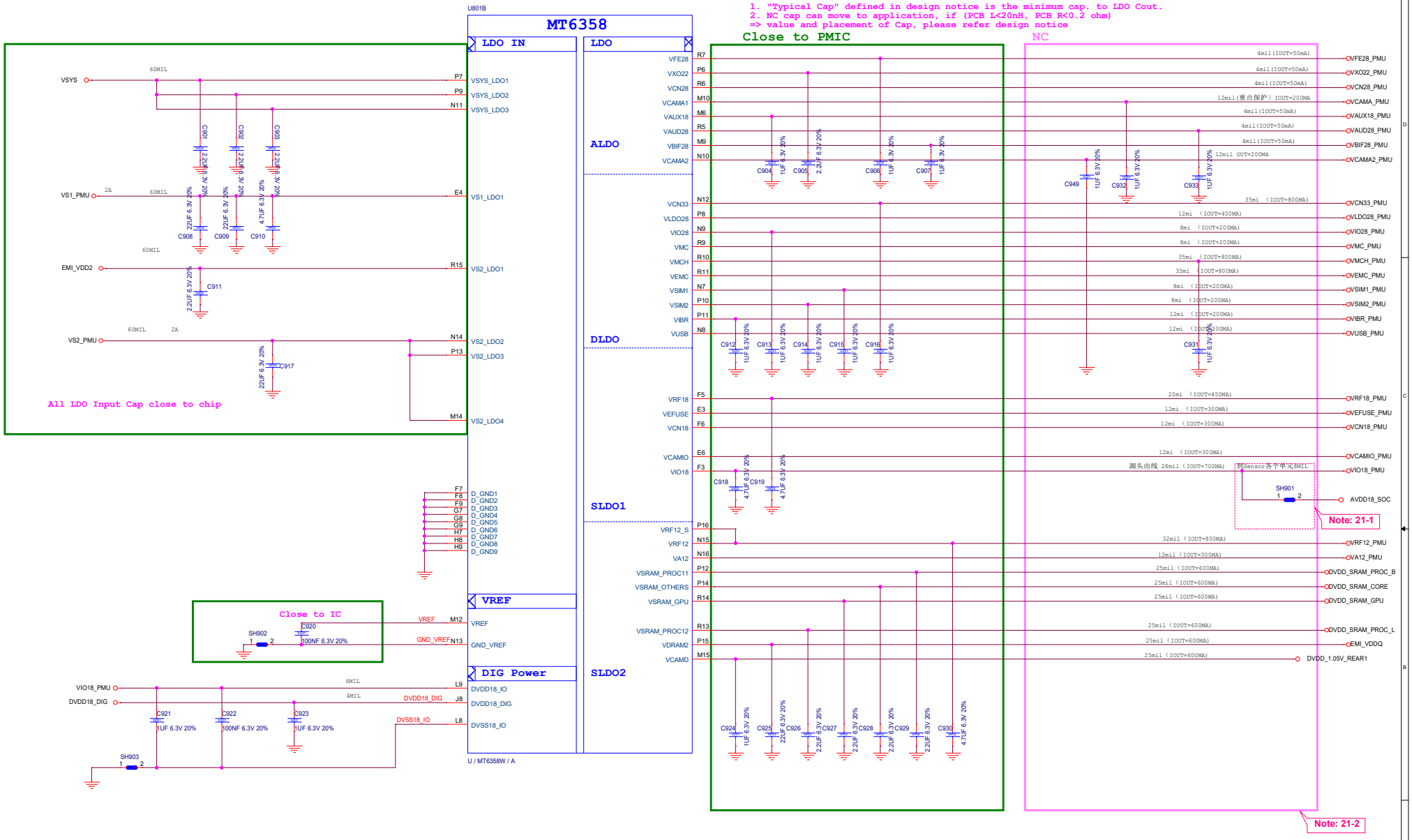
Title

Size C

MTK Confidential

Date: Friday, July 23, 2021 Sheet 7 of 32


U801A
MT6358
VBUCK CTRL
VPROC11 IN
VPROC12 IN
VCORE IN
VMODEM IN
VPA IN
VS1 IN
VS2 IN
VGPU IN
VDRAM1
VPROC11
VPROC12
VCORE
VMODEM
VPA
VS1
VS2
VGPU
VDRAM1
VSYS
R801 1R 1% 25V
VSYS_SMPS
C801 1UF 6.3V 20%
GND_SMPS
SH801
C802 10UF 6.3V 20%
GND_VPROC11
SH802
C803 10UF 6.3V 20%
GND_VPROC12
SH803
C808 10UF 6.3V 20%
GND_VCORE
SH804
C811 4.7UF 6.3V 20%
GND_VMODEM
SH805
C814 10UF 6.3V 20%
GND_VPA
SH806
C816 4.7UF 6.3V 20%
GND_VS1
SH807 shortdot-l4
C817 4.7UF 6.3V 20%
GND_VS2
SH808 shortdot-l4
C818 10UF 6.3V 20%
GND_VGPU
SH809 shortdot-l4
C821 4.7UF 6.3V 20%
GND_VDRAM1
SH810 shortdot-l4
All Buck Input Cap close to chip
VSYS_SMPS
GND_SMPS
VSYS_VPROC11_1
VSYS_VPROC11_2
GND_VPROC11_1
GND_VPROC11_2
VSYS_VPROC12_1
VSYS_VPROC12_2
GND_VPROC12_1
GND_VPROC12_2
VSYS_VCORE_1
VSYS_VCORE_2
GND_VCORE_2
GND_VCORE_1
VSYS_VMODEM
GND_VMODEM_1
GND_VMODEM_2
VSYS_VPA
GND_VPA
VSYS_VS1_1
VSYS_VS1_2
GND_VS1_1
GND_VS1_2
VSYS_VS2_1
VSYS_VS2_2
GND_VS2
VSYS_VGPU_1
VSYS_VGPU_2
GND_VGPU_1
GND_VGPU_2
VSYS_VDRAM1
GND_VDRAM1
U / MT6358W / A
VPROC11_1
VPROC11_2
VPROC11_FB
GND_VPROC11_FB
VPROC12_2
VPROC12_1
VPROC12_FB
GND_VPROC12_FB
VCORE1
VCORE2
VCORE_FB
GND_VCORE_FB
VMODEM1
VMODEM2
VMODEM_FB
GND_VMODEM_FB
VPA
VPA_FB
VS1_1
VS1_2
VS1_FB
VS2_1
VS2_2
VS2_FB
VGPU2
VGPU1
VGPU_FB
GND_VGPU_FB
VDRAM1
VDRAM1_FB
GND_VDRAM1_FB
VPROC11 PL801 0.47UH 6A 20%
VPROC12 PL802 0.47UH 6A 20%
VCORE PL803 0.47UH 5.3A 20%
VMODEM PL804 1UH 4A 20%
VPA PL805 1UH 4A 20%
VS1 PL806 1UH 4.2A 20%
VS2 PL807 1UH 4.2A 20%
VGPU PL808 0.47UH 5.3A 20%
VDRAM1 PL809 1UH 4.2A 20%
L close to chip
differential and shielding
DVDD_PROC_B_PMIC_FB [3]
DVDD_PROC_B_PMIC_GND [3]
DVDD_PROC_L_PMIC_FB [3]
DVDD_PROC_L_PMIC_GND [3]
DVDD_CORE_PMIC_FB [3]
DVDD_CORE_PMIC_GND [3]
DVDD_MODEM_PMIC_FB [3]
DVDD_MODEM_PMIC_GND [3]
VPA_PMU
C815 2.2UF 6.3V 20%
close to VPA Inductor PMIC feedback cap.
VS1_PMU
VS1 sense to Cap
VS2_PMU
VS2 sense to Cap
EMI_VDD2_FB [21]
EMI_VDD2_GND [21]
DVDD_PROC_B
DVDD_PROC_L
DVDD_CORE
DVDD_MODEM
DVDD_GPU
EMI_VDD2
C804 22UF 6.3V 20%
C805 22UF 6.3V 20%
C806 22UF 6.3V 20%
C807 22UF 6.3V 20%
C809 22UF 6.3V 20%
C810 22UF 6.3V 20%
C812 22UF 6.3V 20%
C813 22UF 6.3V 20%
C819 22UF 6.3V 20%
C820 22UF 6.3V 20%
C822 22UF 6.3V 20%
C823 22UF 6.3V 20%
C824 10UF 6.3V 20%
DVDD_PROC_B side cap
C / 22 / uF / 0603
C / 22 / uF / 0603
DVDD_PROC_L side cap
C / 22 / uF / 0603
C / 22 / uF / 0603
CORE side cap
C / 22 / uF / 0603
C / 22 / uF / 0603
MODEM side cap
C / 22 / uF / 0603
C / 22 / uF / 0603
GPU side cap
C / 22 / uF / 0603
C / 22 / uF / 0603
EMI_VDD2 side cap
C / 22 / uF / 0603
C / 22 / uF / 0603
C / 10 / uF / 0603
<Core Design>
MEDIATEK
Title
Size C
MTK Confidential
Date: Friday, July 23, 2021
Sheet 8 of 32



Schematic design notice of "21_POWER_MT6358-LDO" page.

Note 21-1: Please set SH2101 close to C2132, making star connection between VIO18_PMU and AVDD18_SOC near to LDO cap. C2132
Please also refer to MT6358 design notice for further detail design information

Note 21-2: If these power trace can meet LDO layout constraint, these CAP can be NC or removed.
Please refer to MT6358 design notice.

<Core Design>

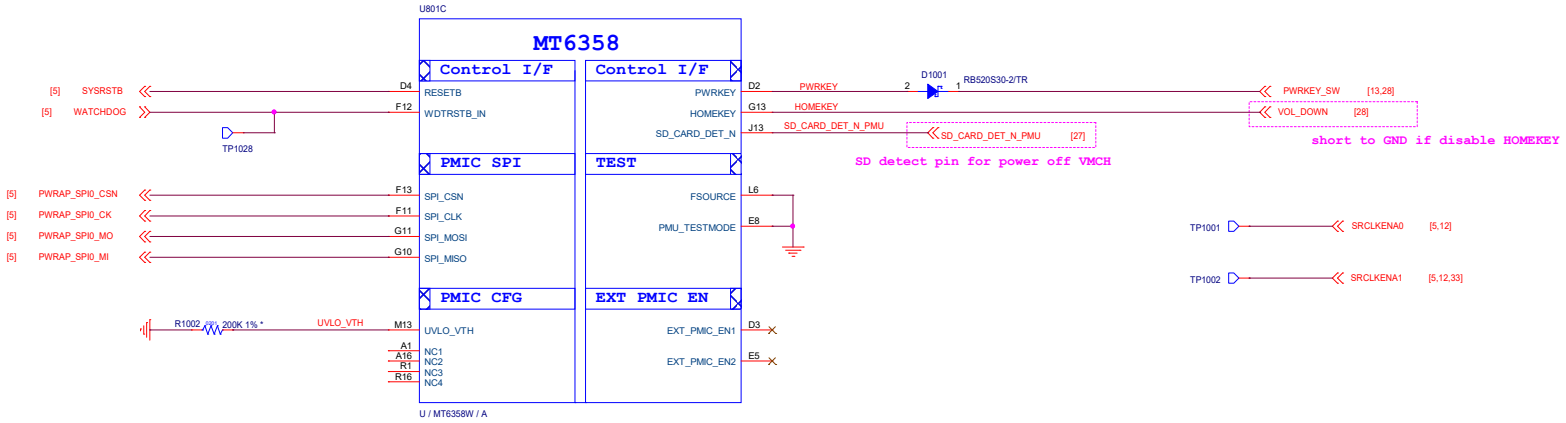
MEDIATEK

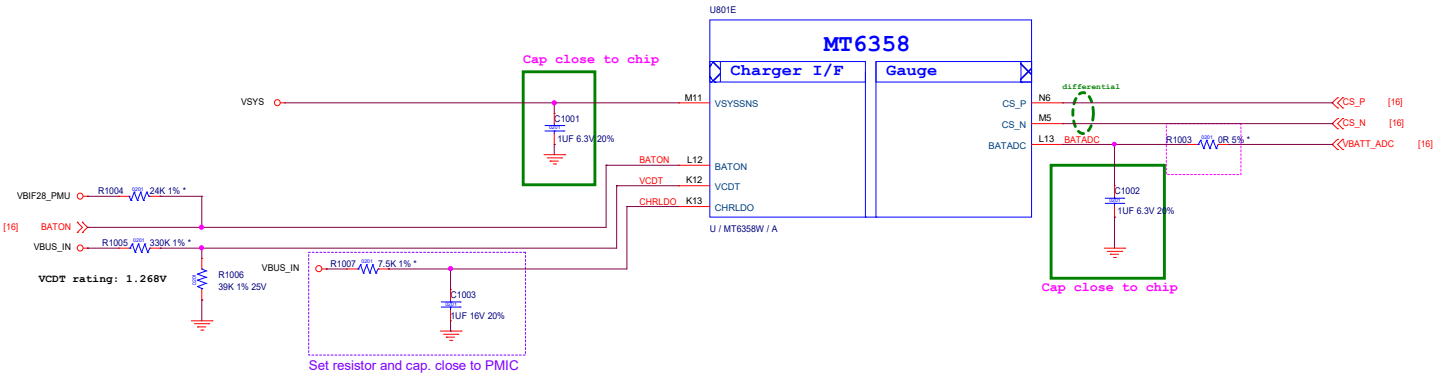
Title: 10_POWER_MT6358-LDO

Size: C

MTK Confidential

Date: Saturday, July 24, 2021 Sheet 9 of 32





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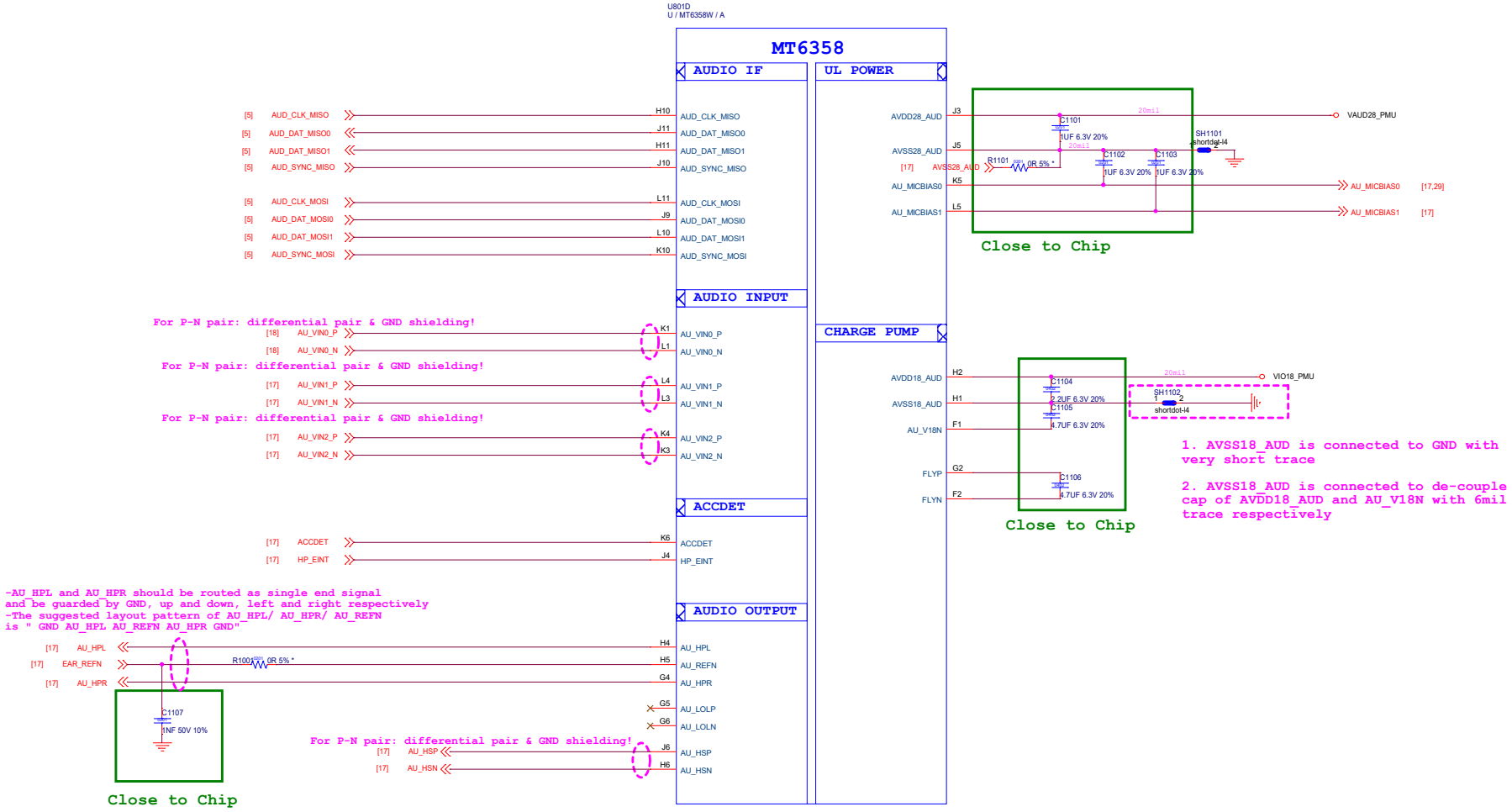
MEDIATEK

Title: 10_POWER_MT6358-IF

Size: C

MTK Confidential

Date: Friday, July 23, 2021 Sheet 10 of 32



<Core Design>

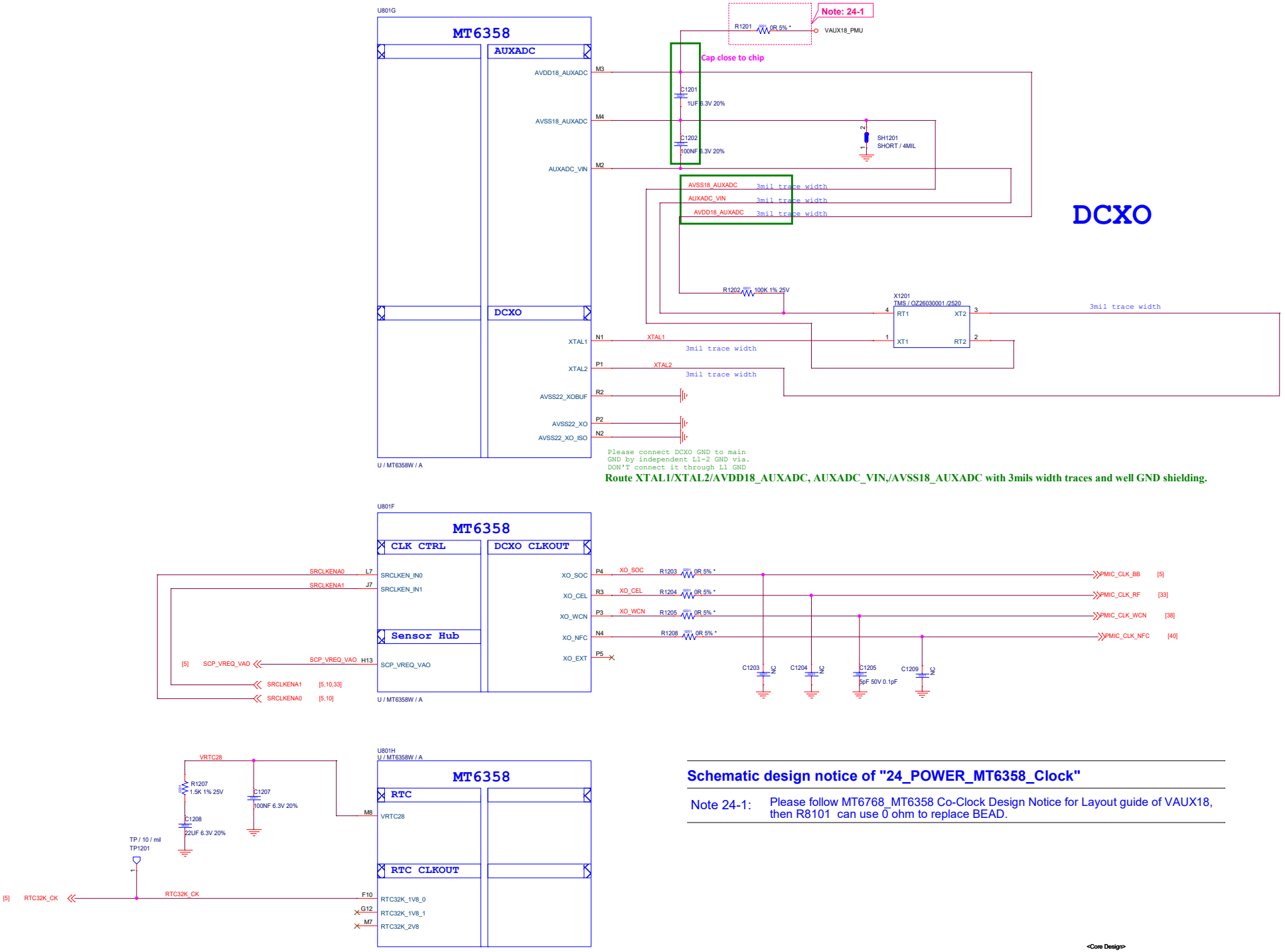
MEDIATEK

Title: 11_POWER_MT6358-Audio

Size: C

MTK Confidential

Date: Friday, July 23, 2021 Sheet 11 of 32



Schematic design notice of "24_POWER_MT6358_Clock"

Note 24-1: Please follow MT6768_MT6358 Co-Clock Design Notice for Layout guide of VAUX18, then R8101 can use 0 ohm to replace BEAD.

<Core Design>

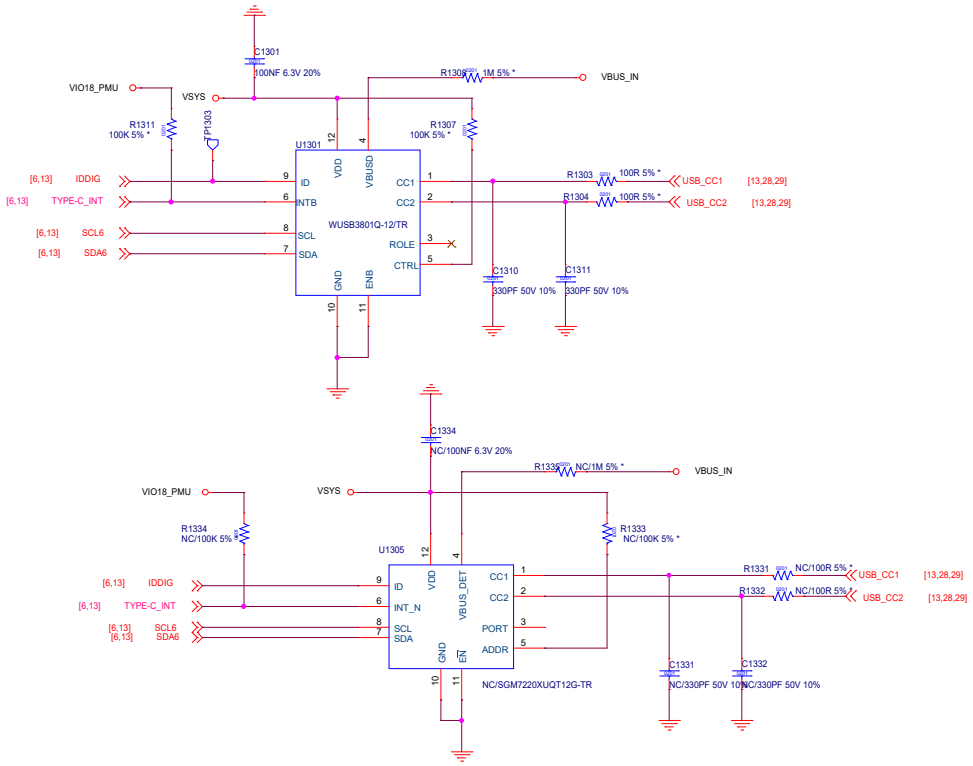
MEDIATEK

Title: 12_POWER_MT6358_Clock

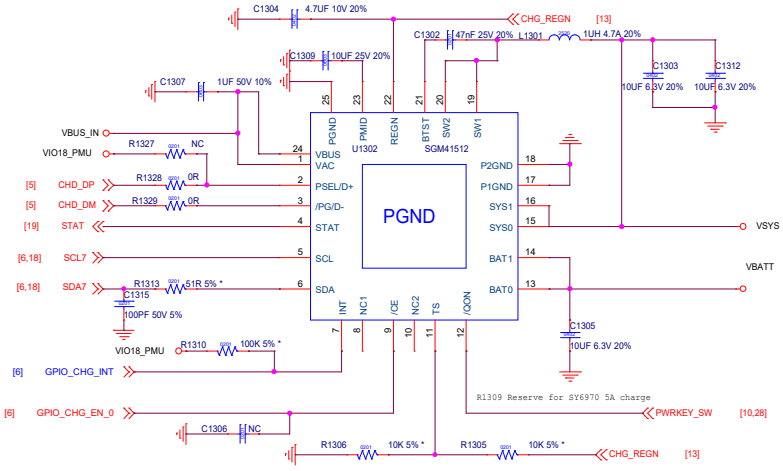
Size: C

MTK Confidential

Date: Friday, July 23, 2021 Sheet 12 of 32



CC logic



SGM41512 I2C slave address :OX6B

Switching Charger Power Path

Title	13_POWER_SubPMIC-General
Size C	MTK Confidential
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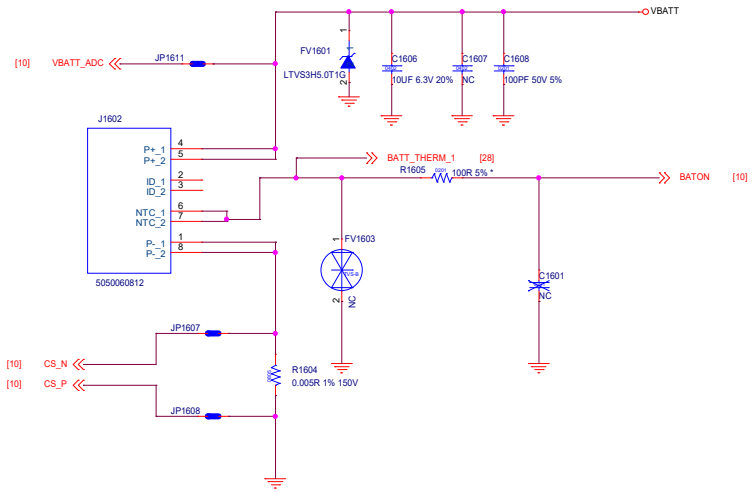
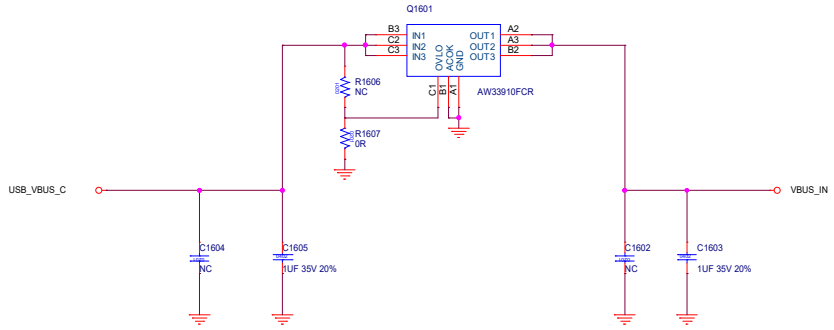


Battery Connector



OVP

<Core Design>

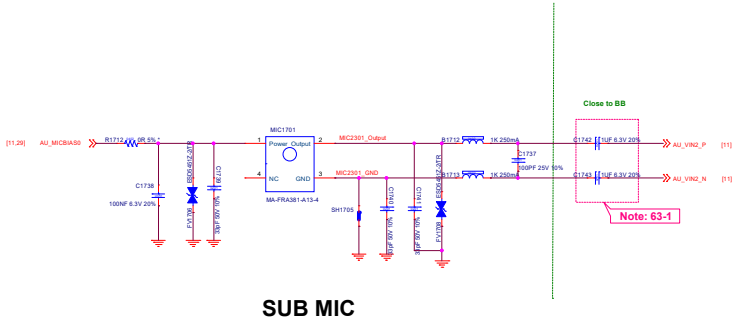
MEDIATEK

Title

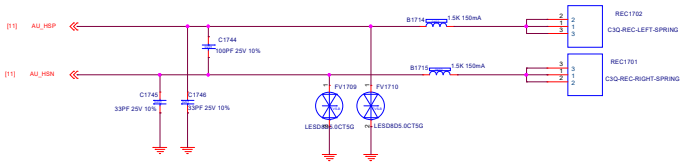
Size C

MTK Confidential

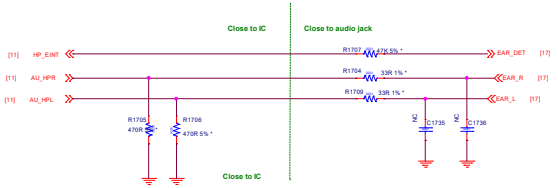
Date: Friday, July 23, 2021 Sheet 16 of 32

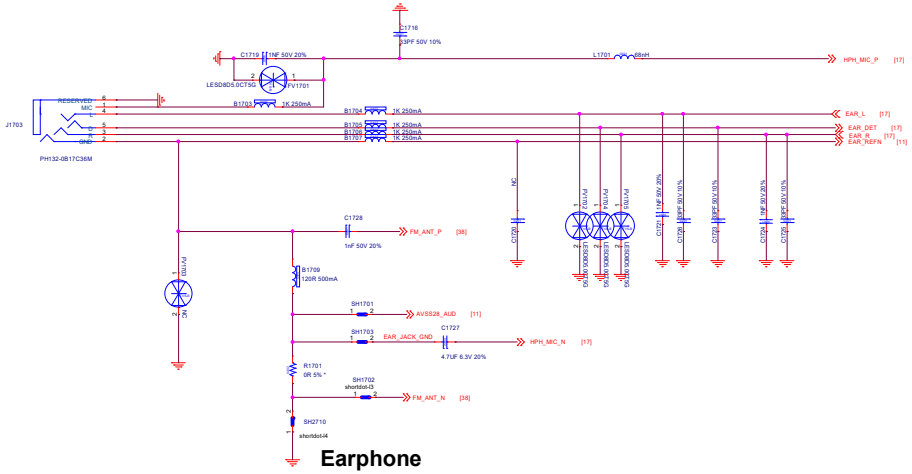


SUB MIC

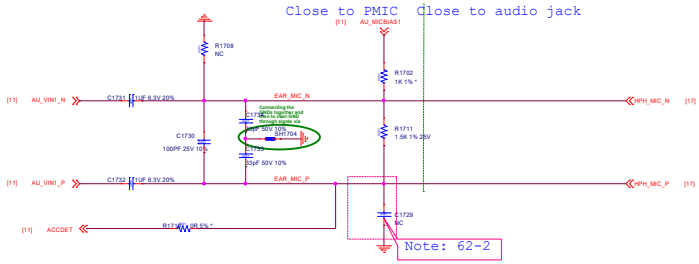


RECEIVER

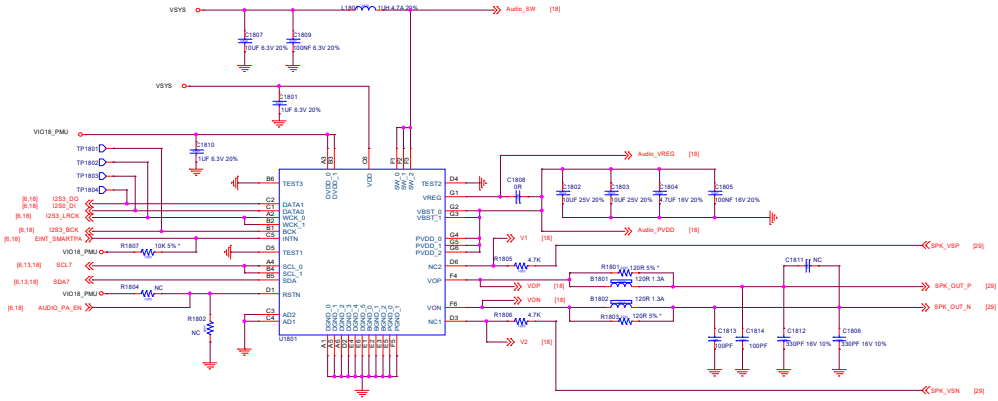




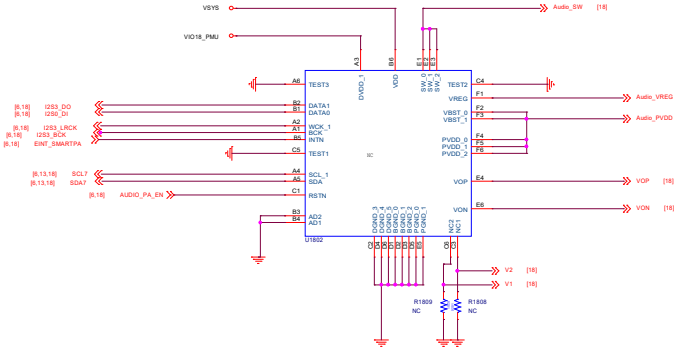
Earphone



Earphone Microphone



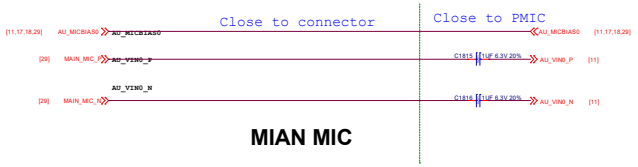
I2C slave address :OX34



I2C slave address :OX34

Smart PA

Audio PA兼容焊盘设计



MIAN MIC

Title	<Title>	
Size: D	Document Number: <Doc>	Rev: <RevCode>
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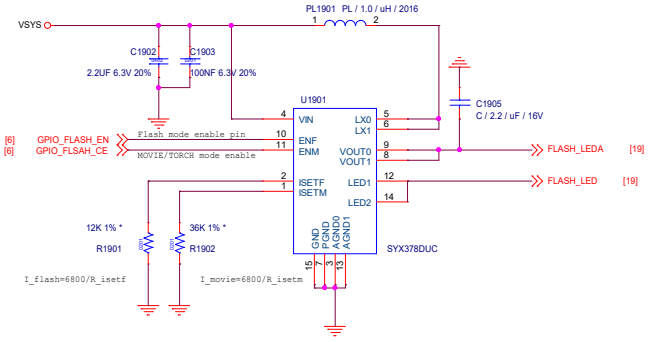
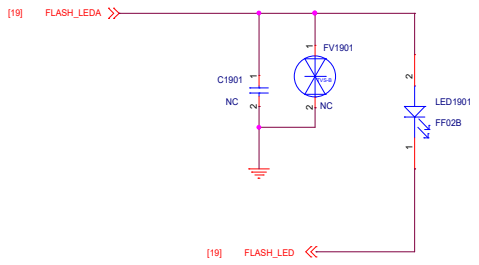
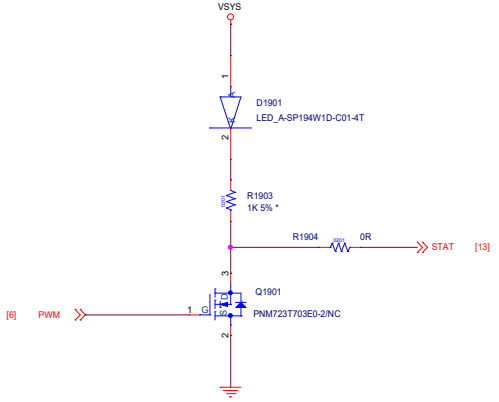


Flash LED Driver



FLASH LED



Charger indicator

SMT ON MAI

MEDIATEK

Title: 19_POWER_SubPMIC-HV powers

Size: C

MTK Confidential

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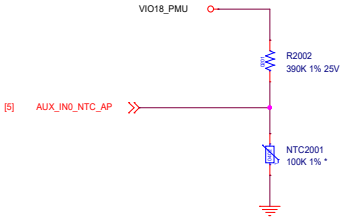
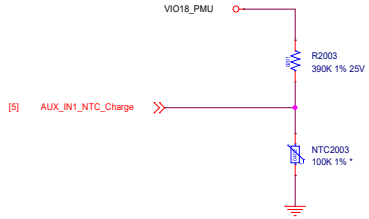
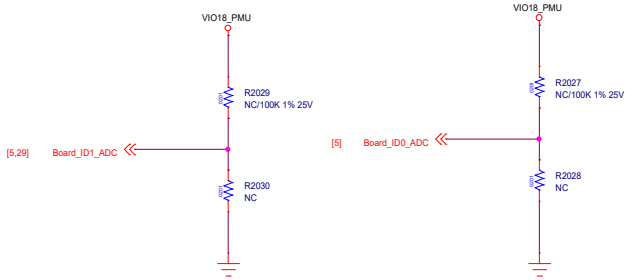


Thermistor to sense AP temperature

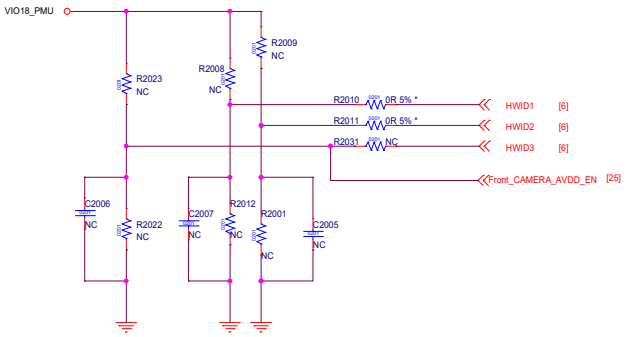


Thermistor to sense charge temperature

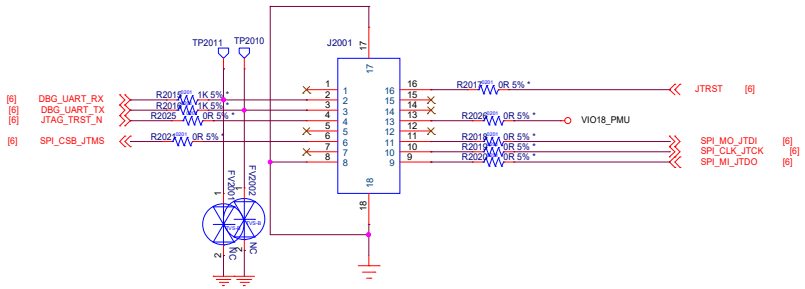
1. NTC2001must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.
2. The distance is the shortest distance from package edge to edge.



RF ADC SKU



HWID



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MEDIATEK

Title: 15_BB_AUXADC_Thermal

Size: C

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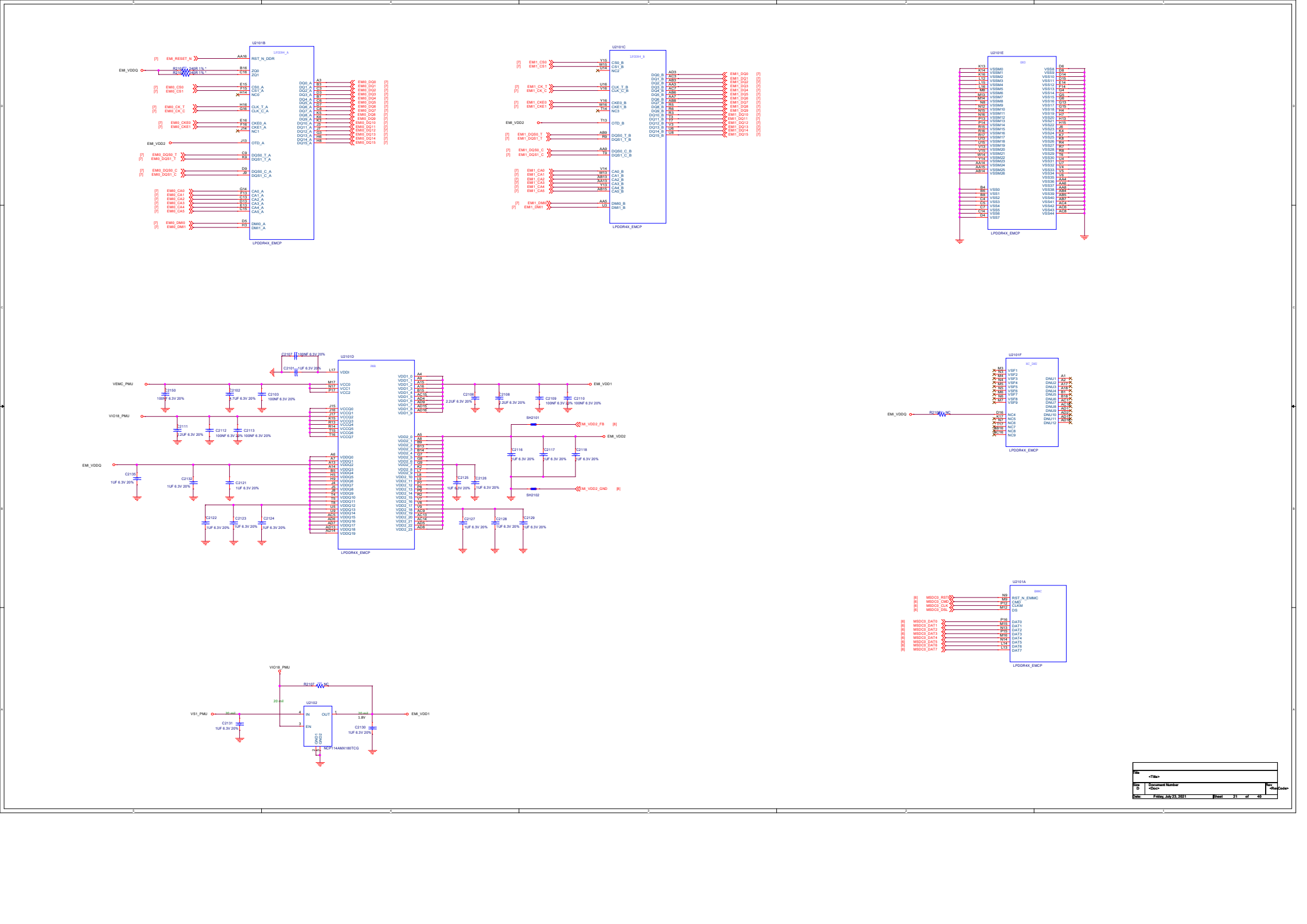
U2101B
LPDDR4X_EMCP
EMI_RESET_N
EMI_VDDQ
EMI_VDD2
U2101C
LPDDR4X_EMCP
U2101E
LPDDR4X_EMCP
U2101D
LPDDR4X_EMCP
VEMC_PMU
VIO18_PMU
EMI_VDD
EMI_VDD1
EMI_VDD2
U2101F
LPDDR4X_EMCP
U2101A
LPDDR4X_EMCP
U2102
TCP7144MX180TCG
VS1_PMU
Title
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Size
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Document Number
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Rev
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Date:
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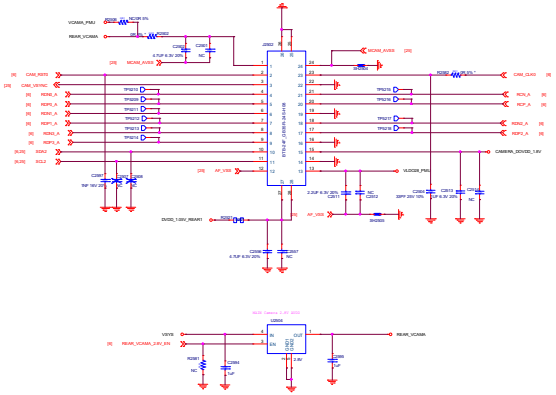
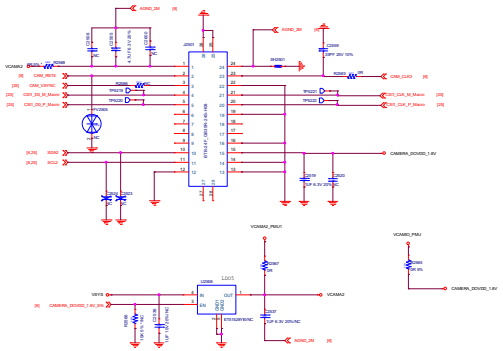
48



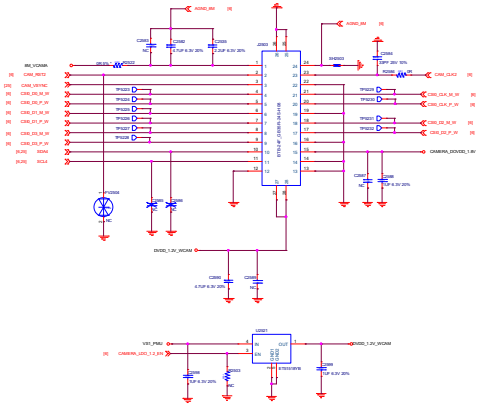
Main Camera 50M

I2C地址 芯片 0xA2#(W)/0XA3#(R)
I2C地址 Driver IC 0x18#(W)/0X19#(R)
I2C地址 EEPROM 0xA0#(W)/0XA1#(R)
---RST Low Active---



Macro Camera 2M

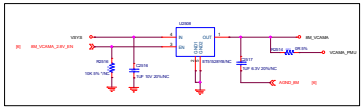
I2C地址 芯片 0x6E#(W)/0X6F#(R)
I2C地址 Driver IC N/A
I2C地址 EEPROM N/A



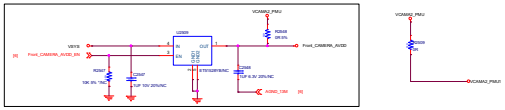
Wide CAMERA 8M

I2C地址 芯片 0x5A#(W)/0X5B#(R)
I2C地址 Driver IC NA
I2C地址 EEPROM NA

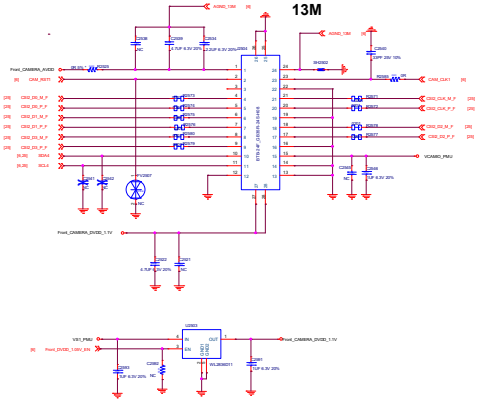
8M AVDD



13M AVDD

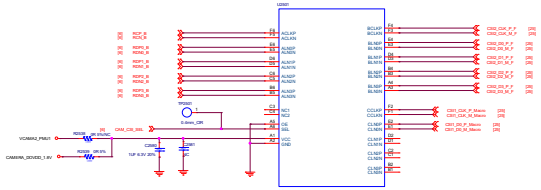


13M



FRONT CAMERA 13MP

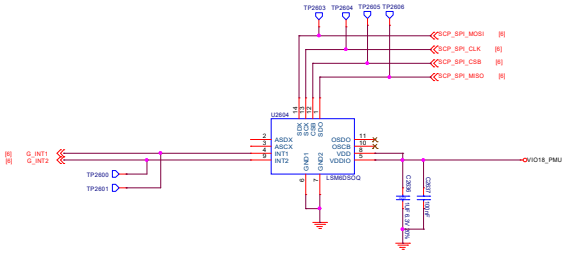
I2C地址 芯片 0x46#(W)/0X47#(R)
I2C地址 Driver IC NA
I2C地址 EEPROM 0xA2#(W)/0XA3#(R)



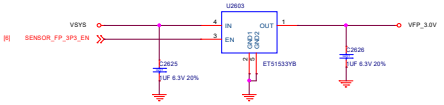
MIPI SW2

FRONT CAMERA

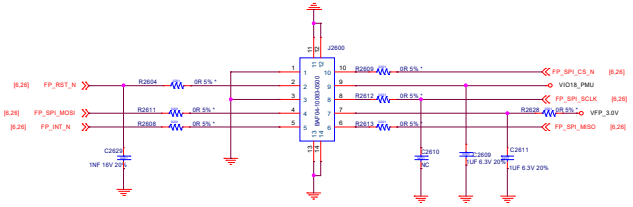
2M Macro



A+GYRO

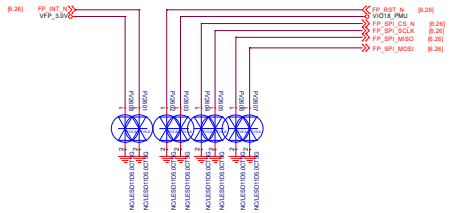


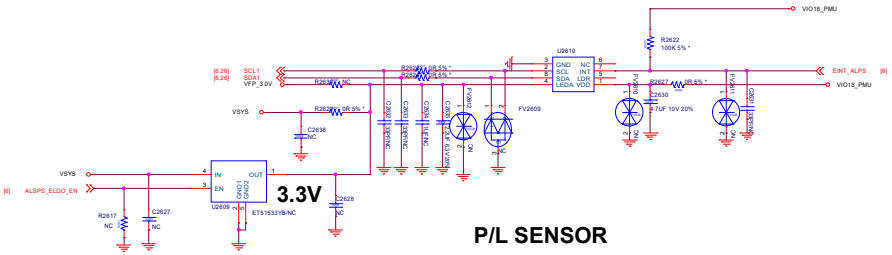
FP



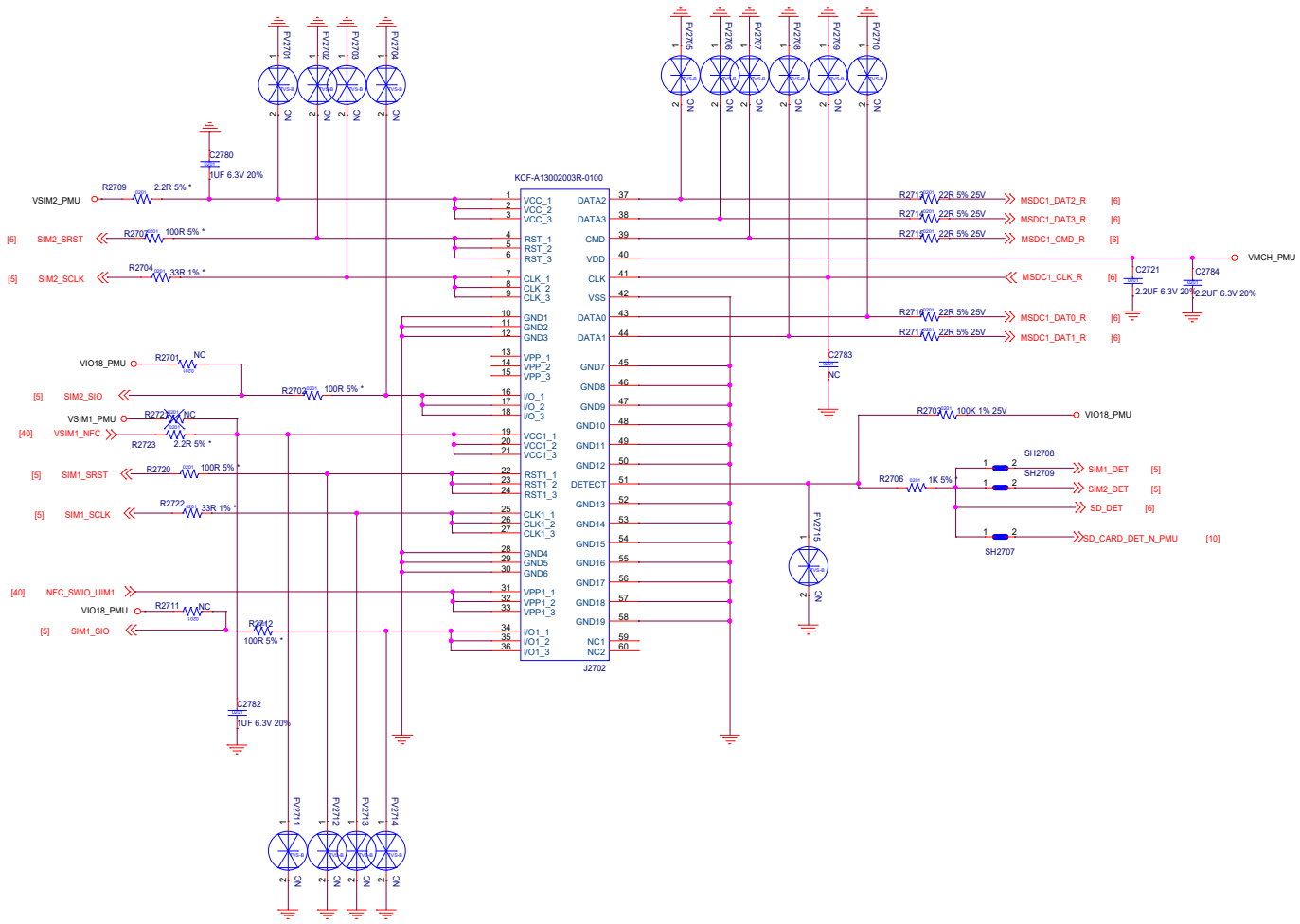
MMC5603NJL I2C slave address :OX30

M SENSOR





P/L SENSOR



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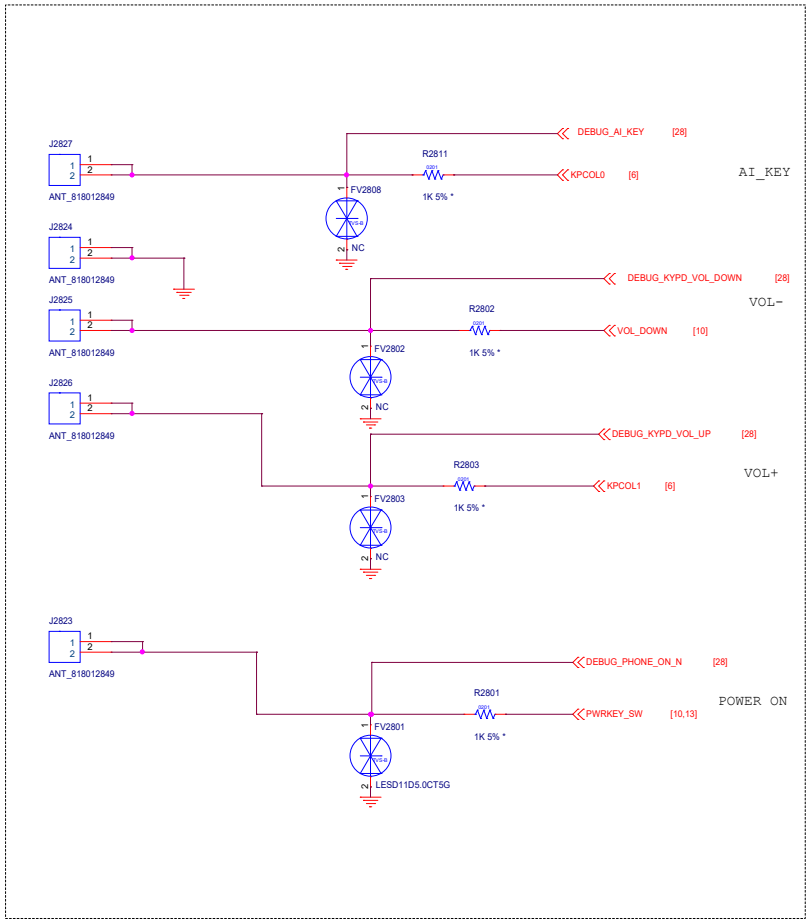
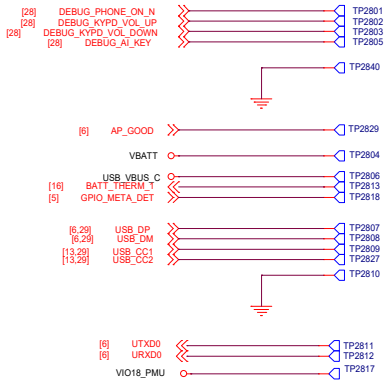
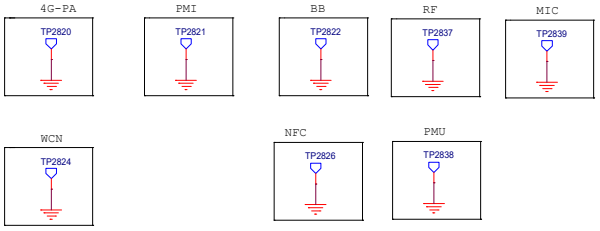
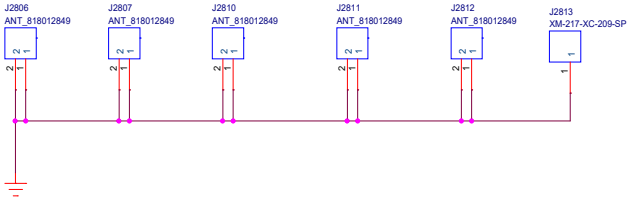
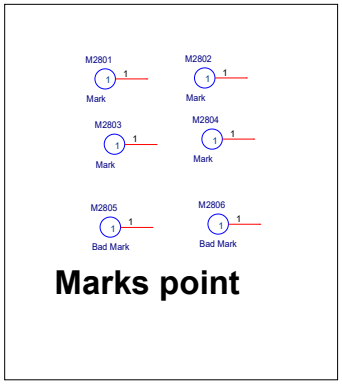




屏蔽盖







USE FOR GND

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MEDIATEK

Title: 28_PERI_KEYPAD

Size: C

MTK Confidential

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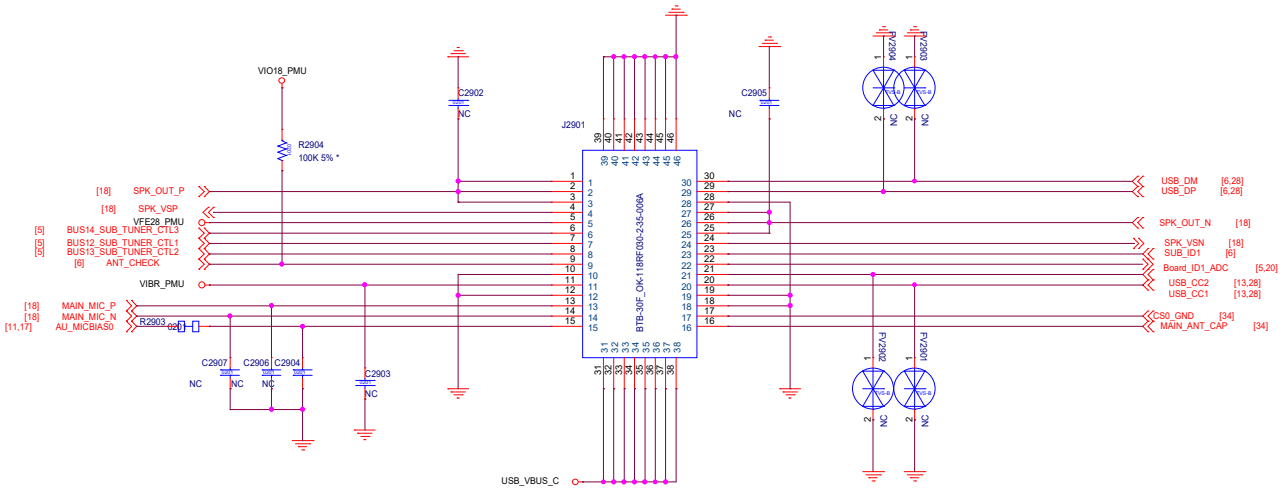
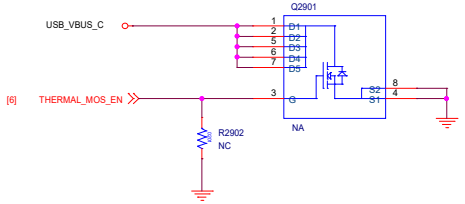


Sub Connector

10V 3A / 5V 2A



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MEDIATEK

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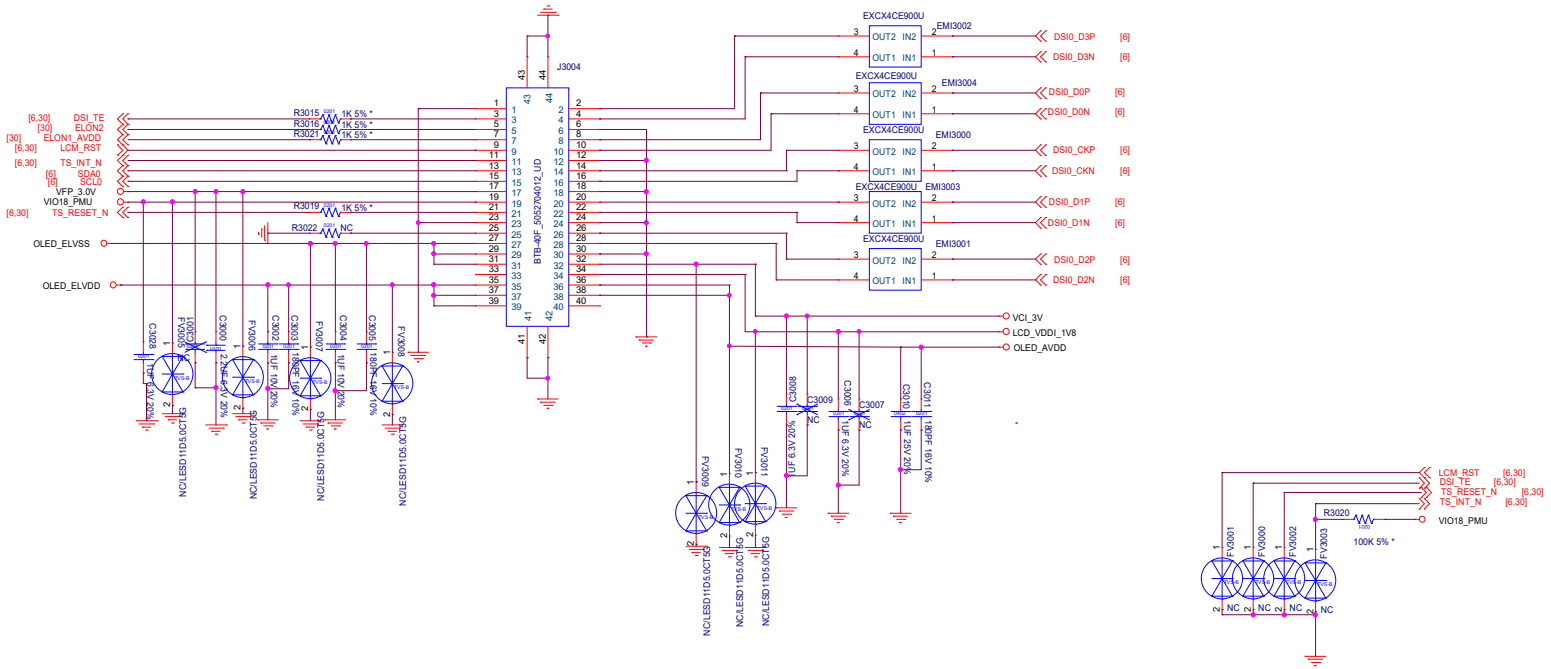
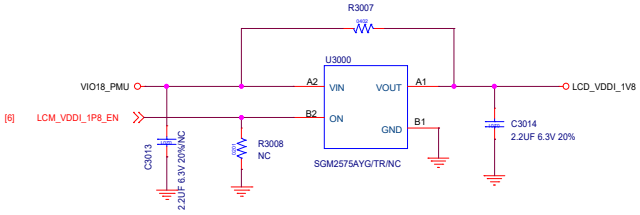
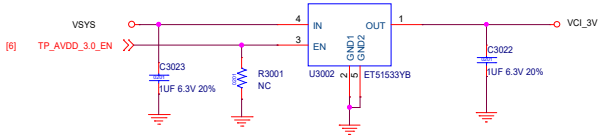
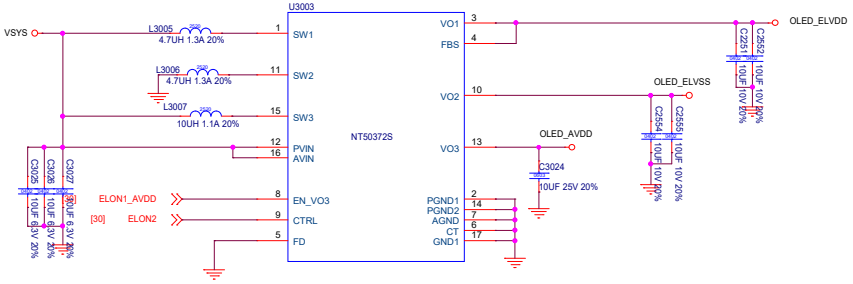
Date: Friday, July 23, 2021 Sheet 29 of 40









OLED POWER

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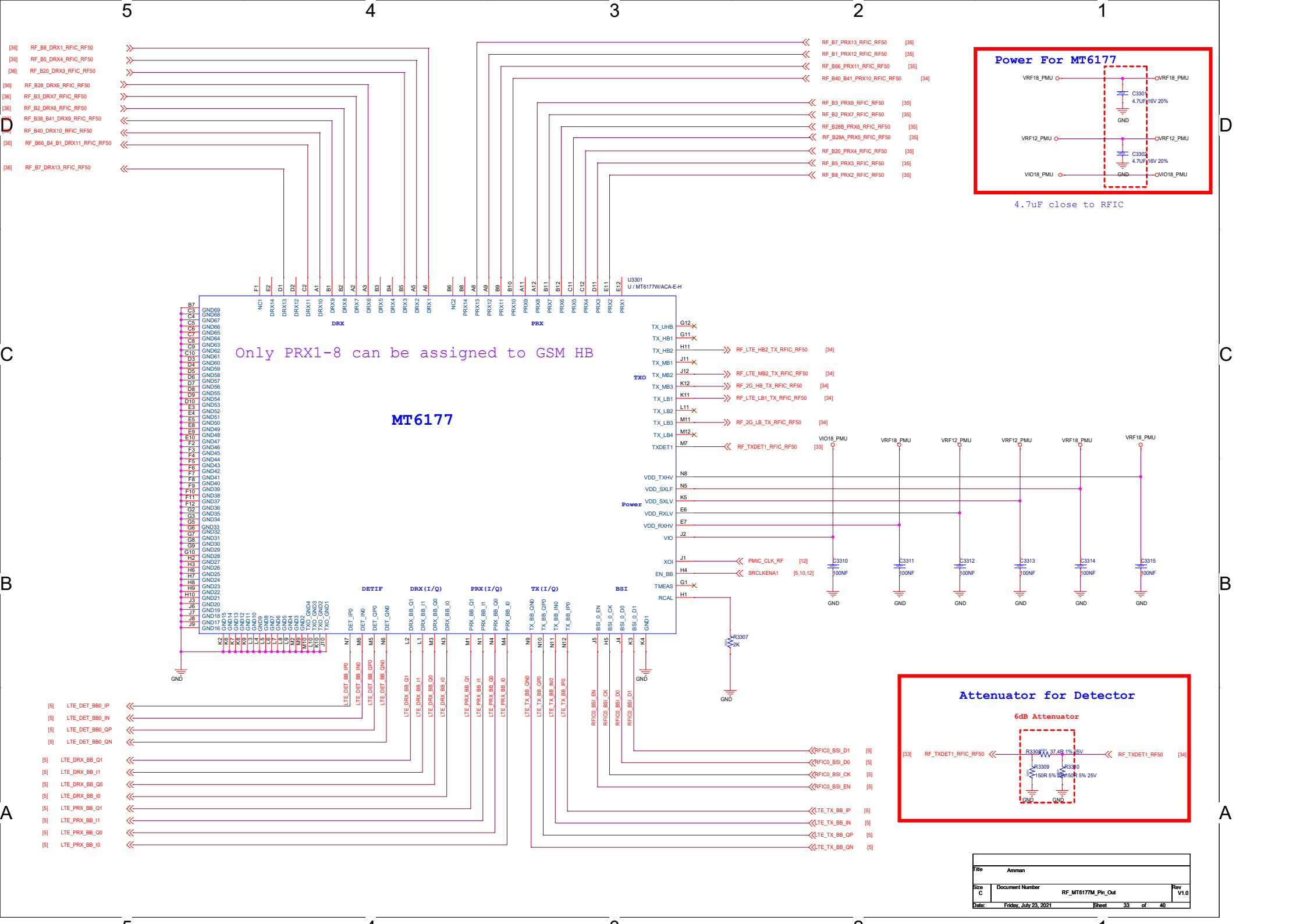
MEDIATEK

Title

Size C

MTK Confidential

Date: Tuesday, July 27, 2021 Sheet 30 of 40


Power For MT6177
VRF18_PMU
VRF12_PMU
VIO18_PMU
C3301
4.7UF 16V 20%
C3304
4.7UF 16V 20%
GND
4.7uF close to RFIC
Only PRX1-8 can be assigned to GSM HB
MT6177
U3301
U / MT6177W/ACA-E-H
DRX
PRX
TXO
Power
DETIF
DRX(I/Q)
PRX(I/Q)
TX(I/Q)
BSI
C3310
C3311
C3312
C3313
C3314
C3315
100NF
R3307
2K
Attenuator for Detector
6dB Attenuator
R3308 37.4R 1% 25V
R3309 150R 5% 25V
R3310 150R 5% 25V
RF_TXDET1_RFIC_RF50
RF_TXDET1_RF50
Title
Amman
Document Number
RF_MT6177M_Pin_Out
Rev
V1.0
Size
C
Date:
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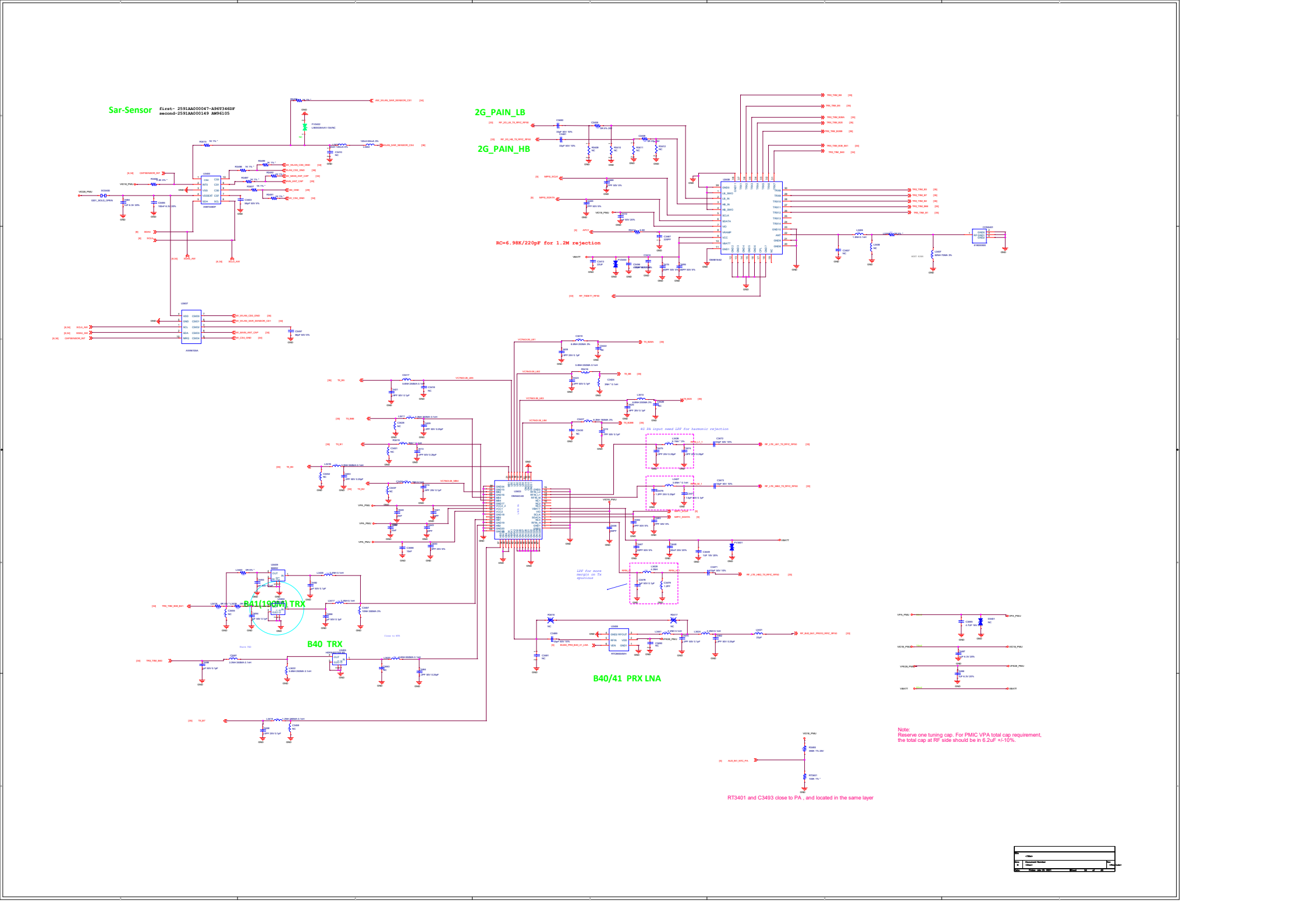
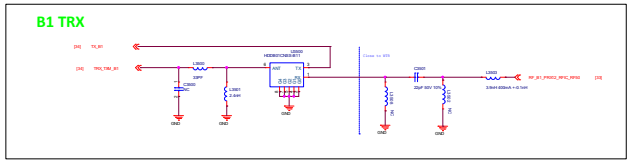
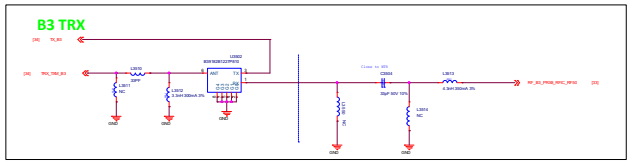

Sar-Sensor
first- 2591AA000047-A96Y346DF
second-2591AA000149 AM96105
2G_PAIN_LB
2G_PAIN_HB
RC=6.98K/220pF for 1.2M rejection
40 PA input need LPF for harmonic rejection
LPF for more margin on Tx spurious
B41(190M) TRX
B40 TRX
B40/41 PRX LNA
Note:
Reserve one tuning cap. For PMIC VPA total cap requirement, the total cap at RF side should be in 6.2uF +/-10%.
RT3401 and C3493 close to PA , and located in the same layer

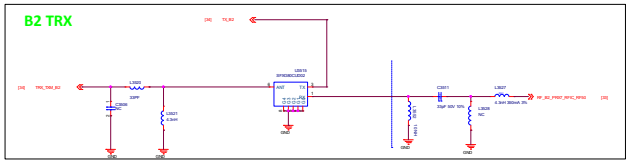
B1 TRX



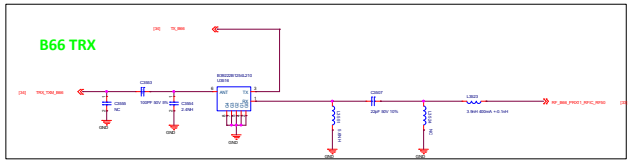
B3 TRX



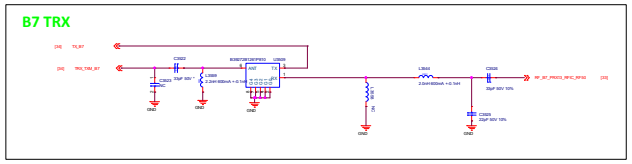
B2 TRX



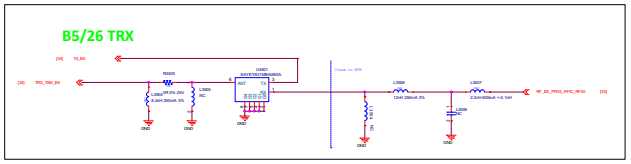
B66 TRX



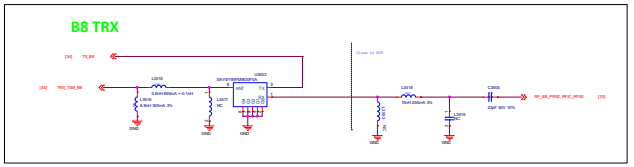
B7 TRX



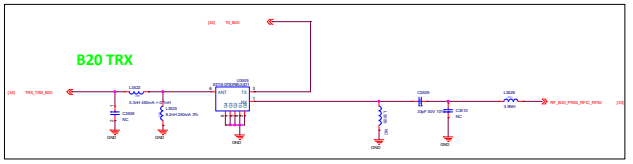
B5/26 TRX



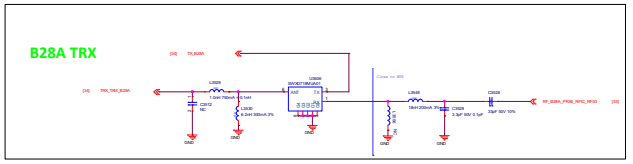
B8 TRX



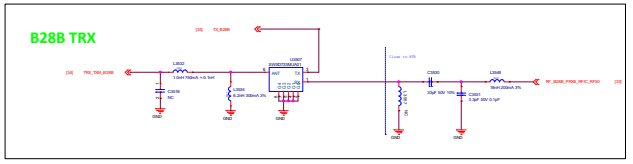
B20 TRX

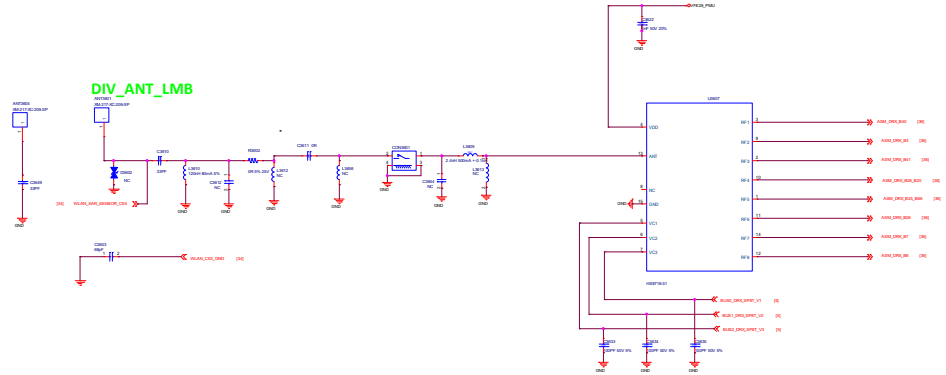


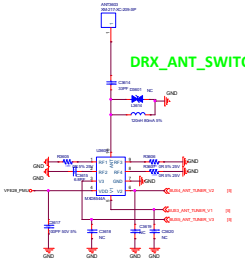
B28A TRX

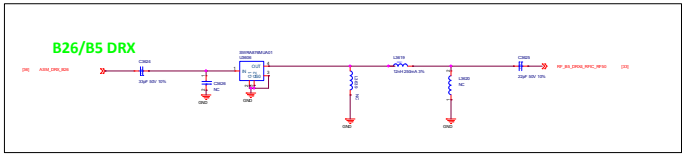


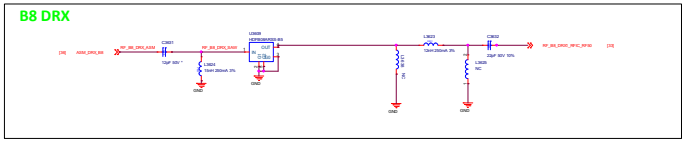
B28B TRX

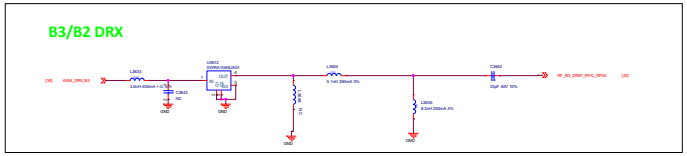


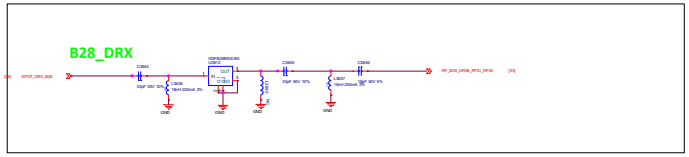

DIV_ANT_LMB


DRX_ANT_SWITCH_LMB


B26/B5 DRX


B8 DRX


B3/B2 DRX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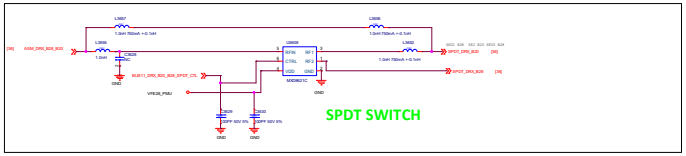
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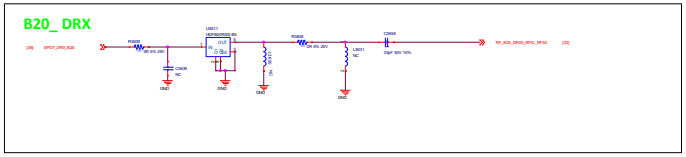
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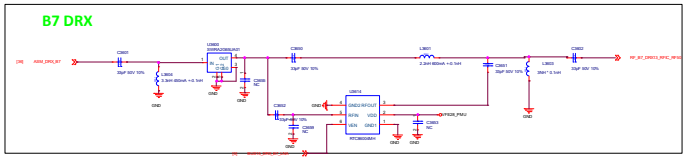
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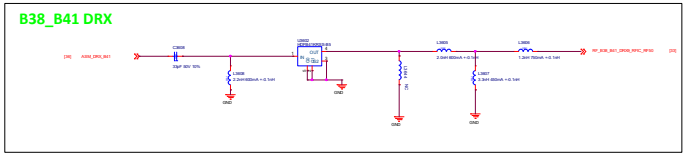
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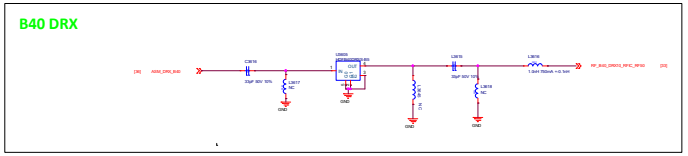
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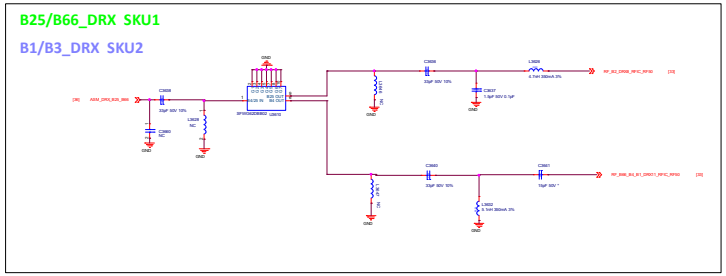
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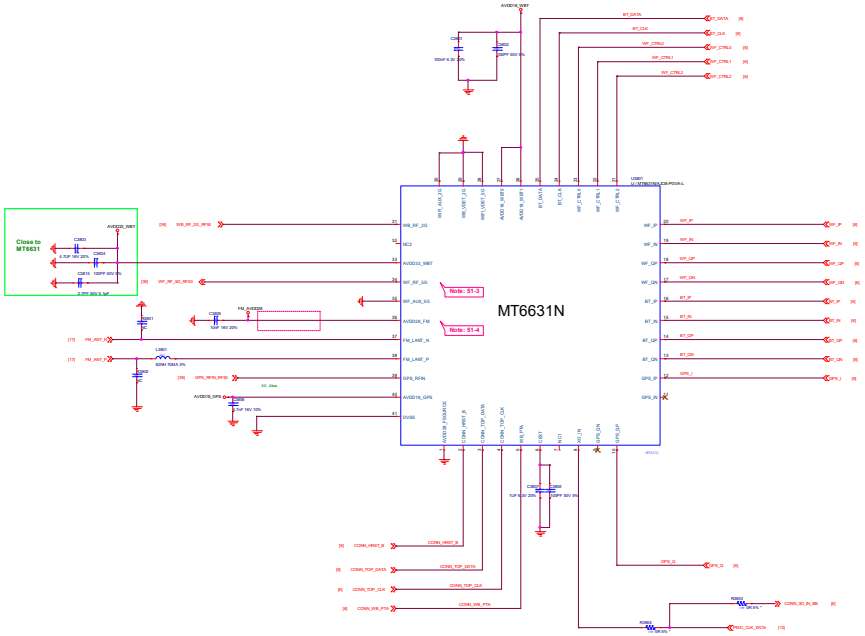

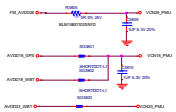

Note 51-1:	For R3808 size, please select 0402 size or larger one
Note 51-2:	Please refer to MT6765 Baseband design notice for VCN33_LDO selection guide
Note 51-3:	If WiFi 5G not support, connect pin 34(WF_RF_5G) to GND
Note 51-4:	Pin 36 (AVDD28_FM) must be connected to VCN28 even if FM not support

PMIC Rail	Pin Name	Pin Number	Peak current at pin (mA)
1.3V_RFA	VDD13_BT_BB_WL	26	120
	VDD13_WL_SYNTH_CH0	46	40
	VDD13_BT_SYNTH	5	15
	VDD11D_PM	43	20
	VDD13_PM	12	15
	VDD13_BT_FM_RBPLL	4	10
	VDD13_BT_PM	29	20
3.3V_CH0	VDD33_WL_CH0	55	450
	VDD33_WL_5GPA_DRV_CH0	61	70
	VDD33_WL_BT_DRV_CH0	34	65
	VDD33_PM_DLDO	71	5
	VDD33_FEM	2	1
1.8V_IO	VDD18_IO	56	15
1.8V_XO	VDD18_XTAL	32	60

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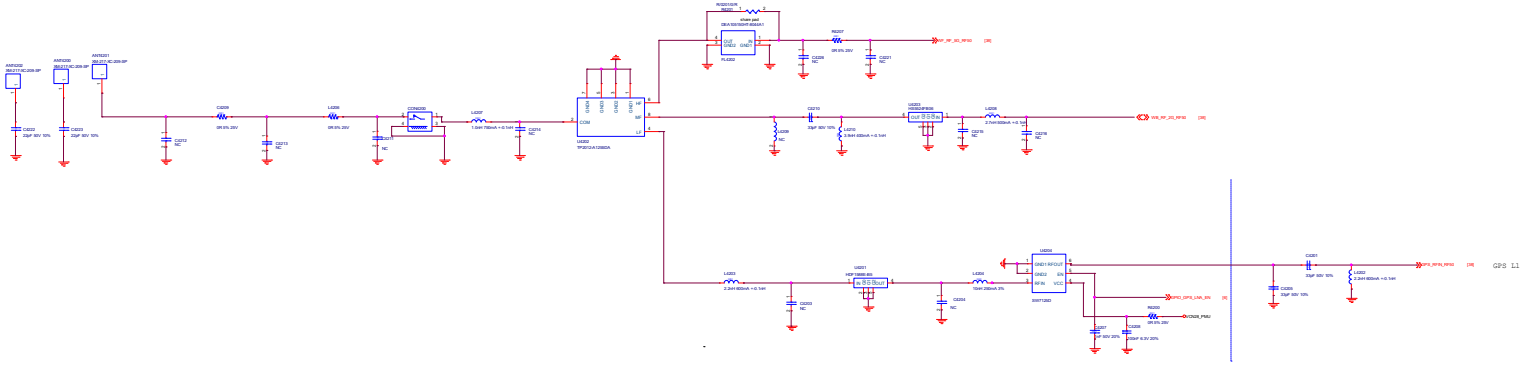

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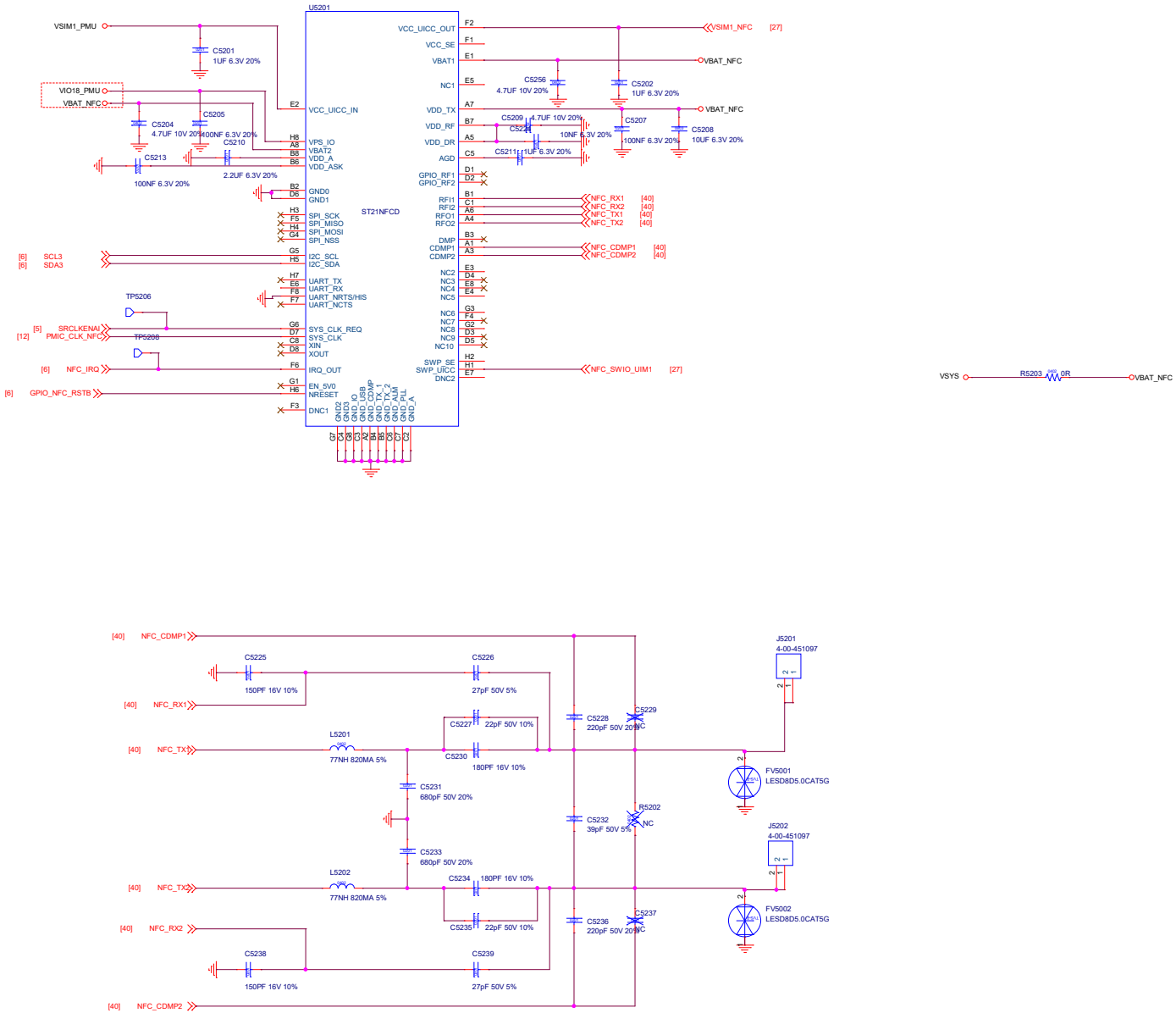

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