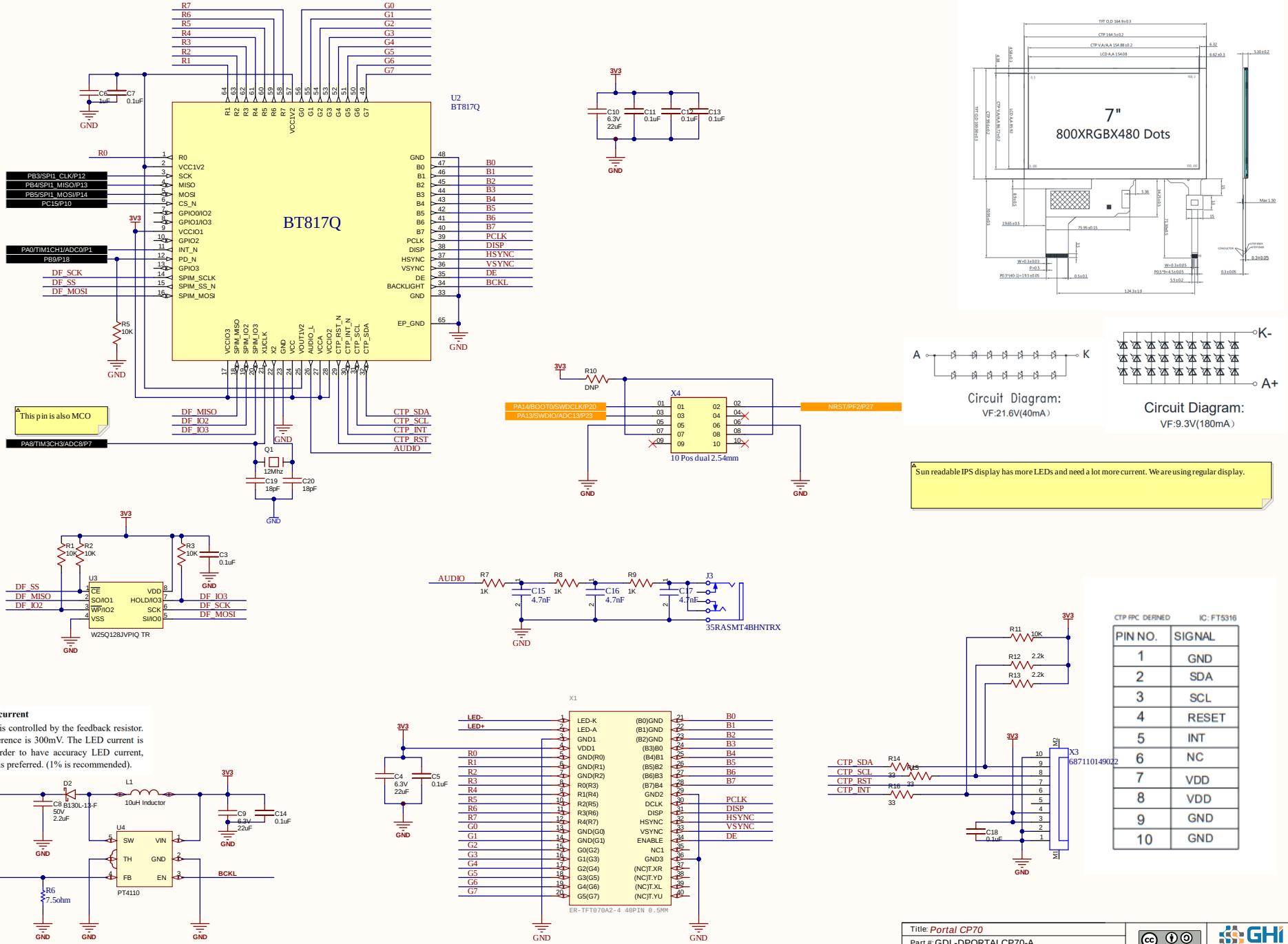
U2
BT817Q
BT817Q
R0
R1
R2
R3
R4
R5
R6
R7
G0
G1
G2
G3
G4
G5
G6
G7
B0
B1
B2
B3
B4
B5
B6
B7
PCLK
DISP
HSYNC
VSYNC
DE
BCKL
PB3/SPI1_CLK/P12
PB4/SPI1_MISO/P13
PB5/SPI1_MOSI/P14
PC15/P10
PA0/TIM1CH1/ADC0/P1
PB9/P18
DF_SCK
DF_SS
DF_MOSI
DF_MISO
DF_IO2
DF_IO3
CTP_SDA
CTP_SCL
CTP_INT
CTP_RST
AUDIO
PA8/TIM3CH3/ADC8/P7
This pin is also MCO
3V3
GND
C6 1uF
C7 0.1uF
C10 6.3V 22uF
C11 0.1uF
C12 0.1uF
C13 0.1uF
R5 10K
Q1
12Mhz
C19 18pF
C20 18pF
R10 DNP
X4
10 Pos dual 2.54mm
PA14/BOOT0/SWDCLK/P20
PA13/SWDIO/ADC13/P23
NRST/PF2/P27
7"
800XRGBX480 Dots
A
K
Circuit Diagram:
VF:21.6V(40mA)
K-
A+
Circuit Diagram:
VF:9.3V(180mA)
Sun readable IPS display has more LEDs and need a lot more current. We are using regular display.
U3
W25Q128JVPIQ TR
R1 10K
R2 10K
R3 10K
C3 0.1uF
AUDIO
R7 1K
R8 1K
R9 1K
C15 4.7nF
C16 4.7nF
C17 4.7nF
J3
35RASMT4BHNTRX
Setting the LED current
The LED current is controlled by the feedback resistor. The feedback reference is 300mV. The LED current is 300mV/R_FB. In order to have accuracy LED current, precision resistor is preferred. (1% is recommended).
LED+
LED-
D2
B130L-13-F
L1
10uH Inductor
C8 50V 2.2uF
C9 6.3V 22uF
C14 0.1uF
U4
PT4110
SW
VIN
TH
GND
FB
EN
R6 7.5ohm
BCKL
X1
ER-TFT070A2-4 40PIN 0.5MM
C4 6.3V 22uF
C5 0.1uF
R11 10K
R12 2.2k
R13 2.2k
R14 33
R15 33
R16 33
C18 0.1uF
X3
687110149022
CTP FPC DEFINED
IC: FT5316
PIN NO. | SIGNAL
1 | GND
2 | SDA
3 | SCL
4 | RESET
5 | INT
6 | NC
7 | VDD
8 | VDD
9 | GND
10 | GND
Title: Portal CP70
Part #: GDL-DPORTALCP70-A
Revision: A
Date: 6/6/2025
Sheet 1 of 5
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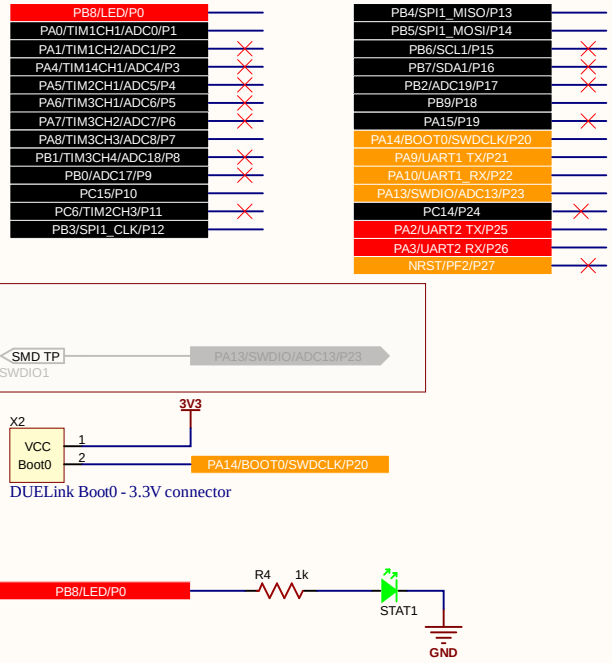


FID1 Fiducial 40 Mil

FID2 Fiducial 40 Mil

FID3 Fiducial 40 Mil

FID4 Fiducial 40 Mil

FID5 Fiducial 40 Mil

FID6 Fiducial 40 Mil

Title: *DUELink Misc*			
Part #: N/A			
Revision: A	Date: 6/6/2025	Sheet 2 of 5	

Software Features:

ADC: P1, P2, P3, P4, P5, P6, P7, P8, P9, P17

Pulse feedback: Can be any pin but hardware need 100pF + 1Mohm

HW PWM: P1, P2, P3, P4, P5, P6, P7, P8, P11
* P1, P2: TIM1
* P3: TIM14
* P4, P11: TIM2
* P5,6,7,8: TIM3

SW PWM: Any pin

SW UART: Pins 1 RX, 2 TX, 3 DBG

Wakeup Pins: P1, P3

Interrupts on: P1, P2, P3, P4, P5, P6, P7, P12, ...

Output compare: P2 (PA1)
Input capture: TBD

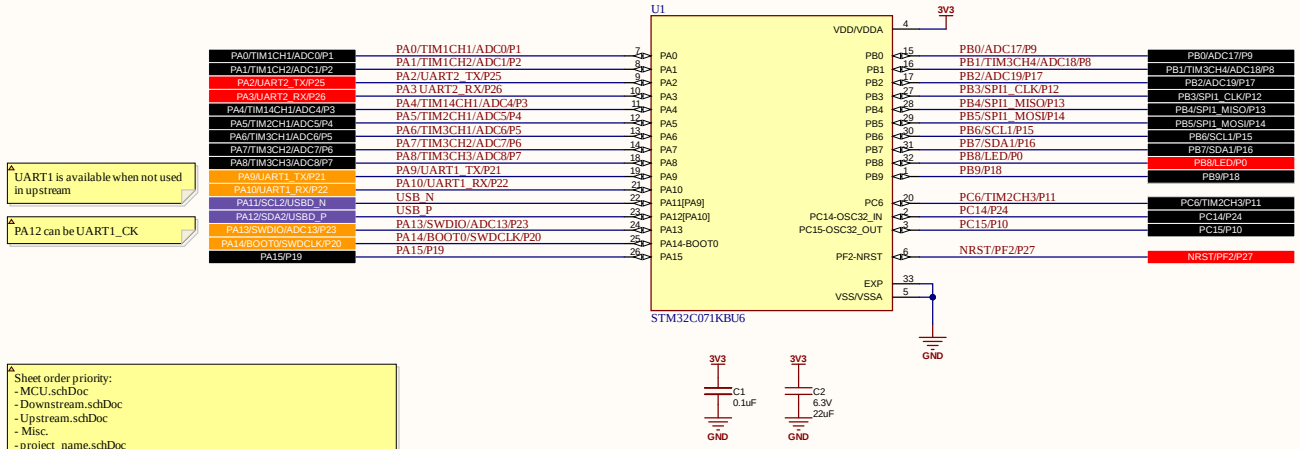
Neopixel: Any pin (blocking mode)

IR reciever: P1

// PB8 - P0 -> LED
// PA0 - P1 -> TIM1_CH1 ADC0
// PA1 - P2 -> TIM1_CH2 ADC1
// PA4 - P3 -> TIM14_CH1 ADC4
// PA5 - P4 -> TIM2_CH1 ADC5
// PA6 - P5 -> TIM3_CH1 ADC6
// PA7 - P6 -> TIM3_CH2 ADC7
// PA8 - P7 -> TIM3_CH3 ADC8
// PB1 - P8 -> TIM3_CH4 ADC18
// PB0 - P9 -> ADC17
//PC15 - P10
// PC6 - P11
// PB3 - P12 -> SPI1_CLK
// PB4 - P13 -> SPI1_MISO
// PB5 - P14 -> SPI1_MOSI
// PB6 - P15 -> I2C1_SCL
// PB7 - P16 -> I2C1_SDA

// PB2 - P17 -> ADC19
// PB9 - P18
//PA15 - P19
//PA14 - P20 -> SWCLK BOOT0

// PA9 - P21 -> UART1 TX - Can be used when no Upstream
//PA10 - P22 -> UART1 - Can be used when no Upstream
//PA13 - P23 -> SWDIO ADC13
// PF2 - P24 -> NRST - Reserved for emergency

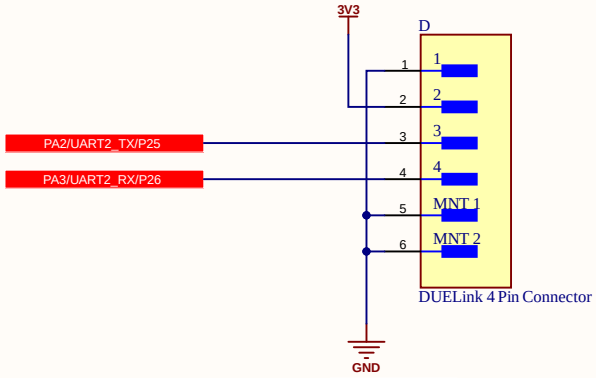


UART1 is available when not used in upstream

PA12 can be UART1_CK

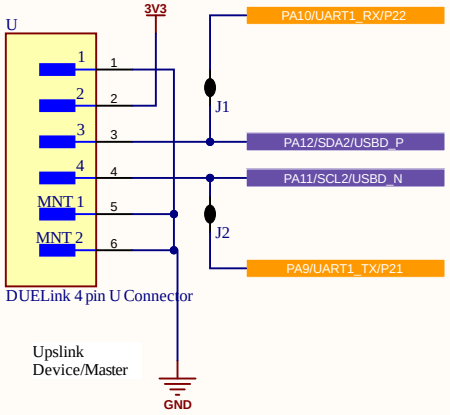
Sheet order priority:
- MCU.schDoc
- Downstream.schDoc
- Upstream.schDoc
- Misc.
- project_name.schDoc

Title: DUELink MCU		
Part #: STM32071KBU6		
Revision: v14	Date: 6/6/2025	Sheet 3 of 5



Downlink Device

Title:			
Part #:			
Revision:	Date: 6/6/2025	Sheet of	



Title: *DUELink Uplink*			
Part #: N/A			
Revision: A	Date: 6/6/2025	Sheet 5 of 5	