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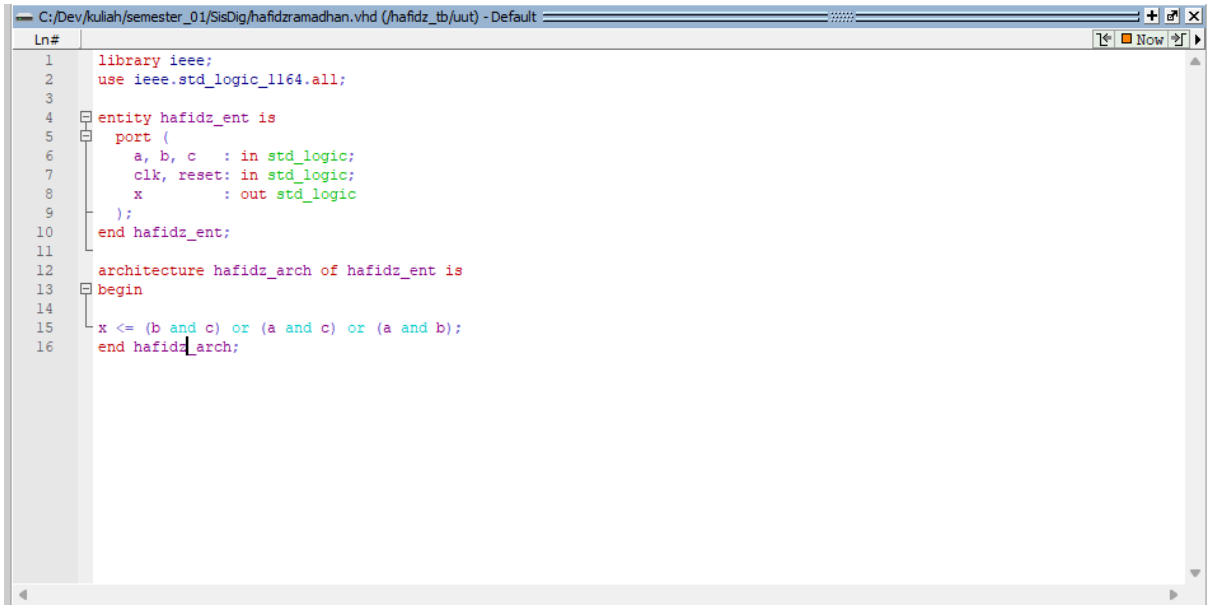
## Screenshot vhdl




```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity hafidz_ent is
5    port (
6      a, b, c    : in std_logic;
7      clk, reset: in std_logic;
8      x          : out std_logic
9    );
10 end hafidz_ent;
11
12 architecture hafidz_arch of hafidz_ent is
13 begin
14
15 x <= (b and c) or (a and c) or (a and b);
16 end hafidz_arch;
```

## Screenshot testbench

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity hafidz_tb is
5  end hafidz_tb;
6
7  architecture testbench of hafidz_tb is
8    signal a, b, c, clk, reset, x: std_logic;
9
10   component hafidz_ent
11     port (
12       a, b, c    : in std_logic;
13       clk, reset: in std_logic;
14       x          : out std_logic
15     );
16   end component;
17
18 begin
19   uut: hafidz_ent port map (a, b, c, clk, reset, x);
20
21   process
22   begin
23     a <= '0';
24     b <= '1';
25     c <= '0';
26     clk <= '0';
27     reset <= '0';
28     wait for 10 ns;
```

```
29
30     a <= '1';
31     b <= '0';
32     c <= '1';
33     clk <= '1';
34     reset <= '0';
35     wait for 10 ns;
36
37     wait;
38   end process;
39 end testbench;
```

Screenshot wave