

A

B

C

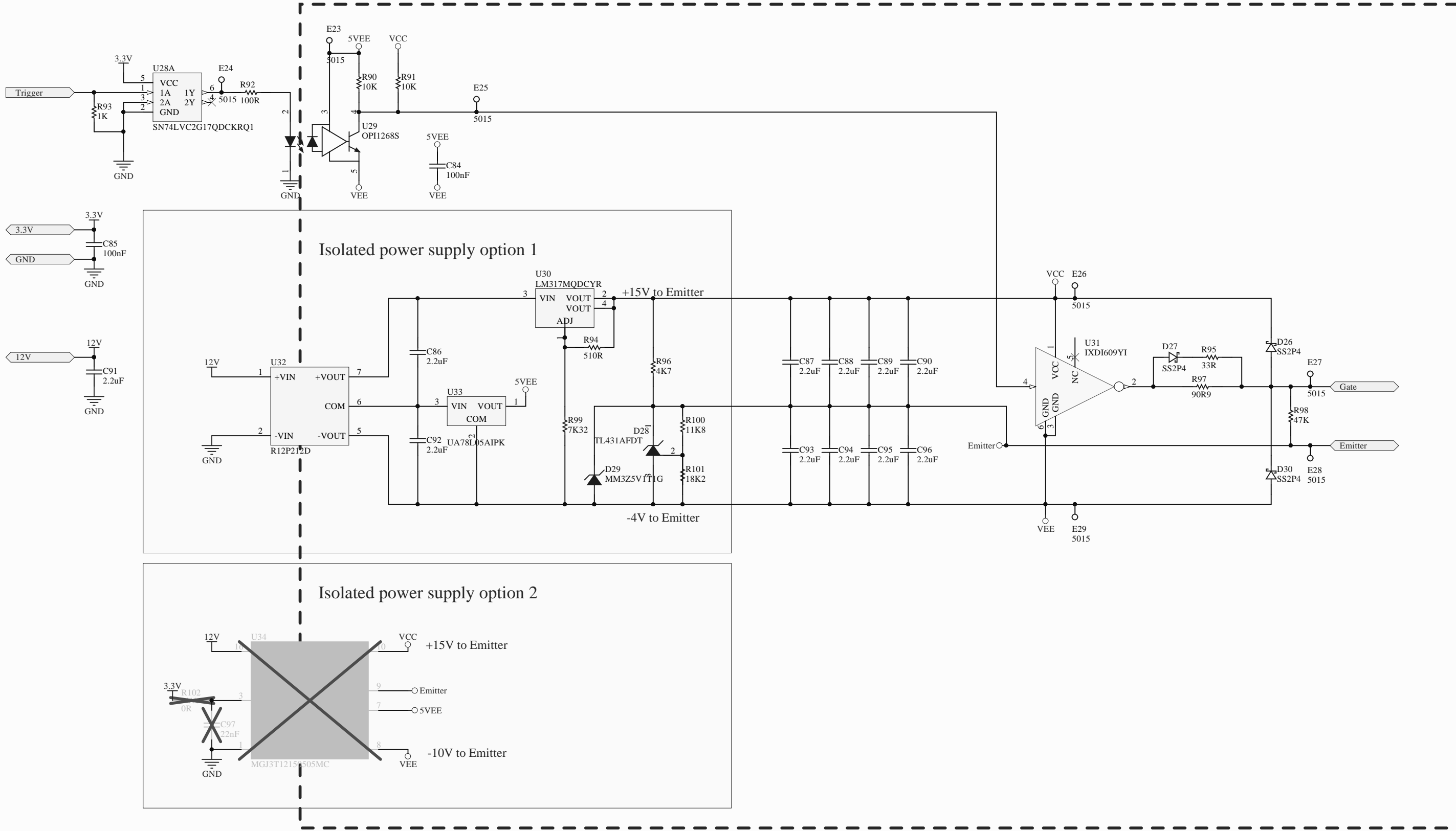
D

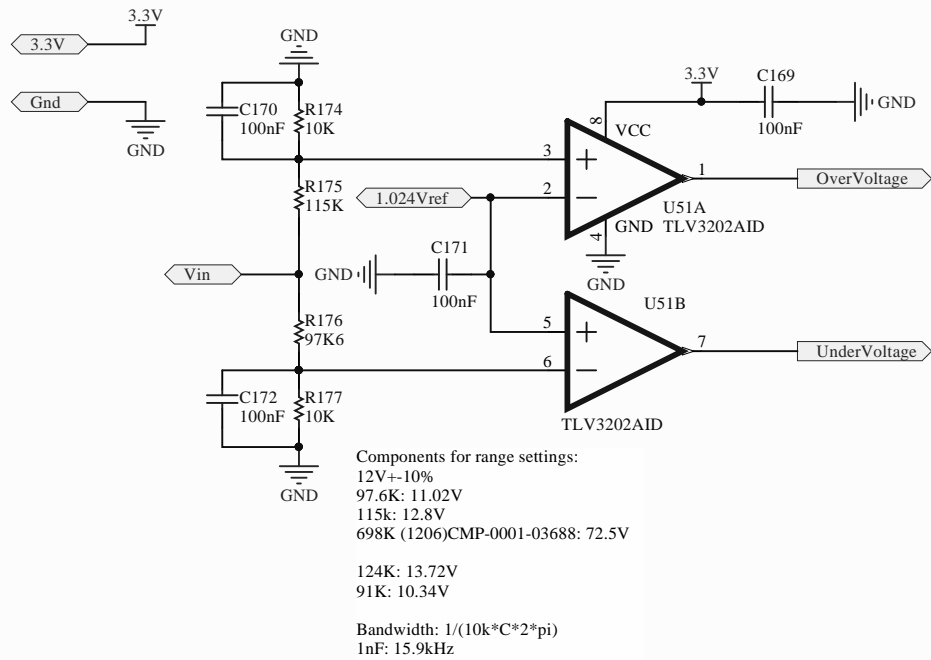
A

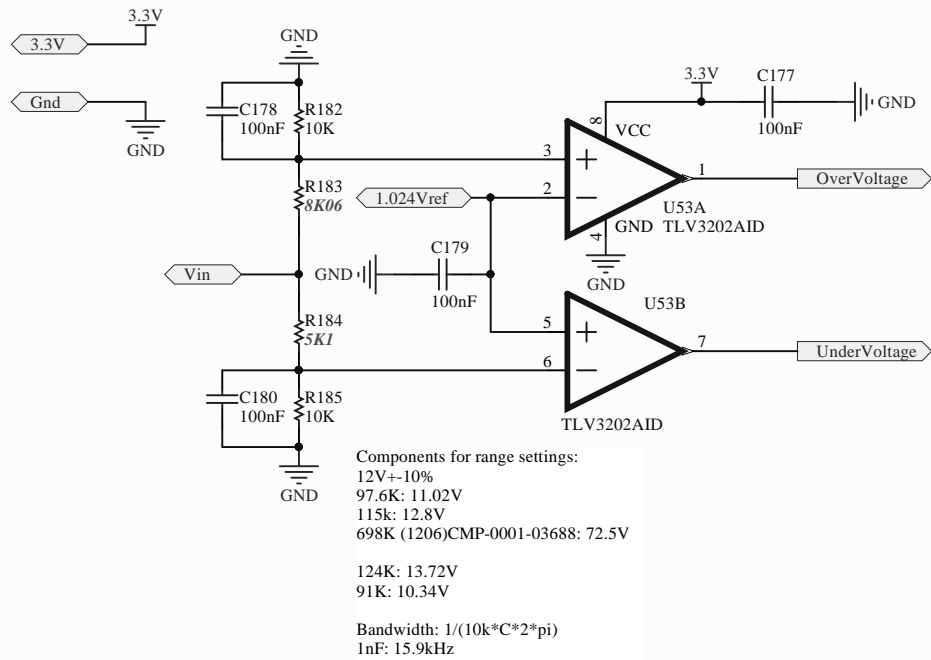
B


C

D

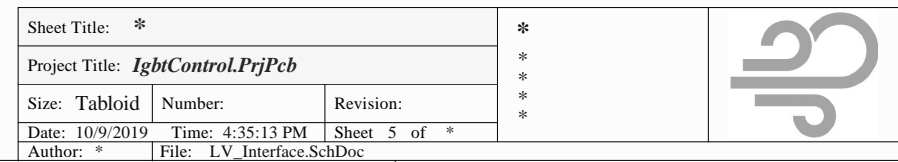






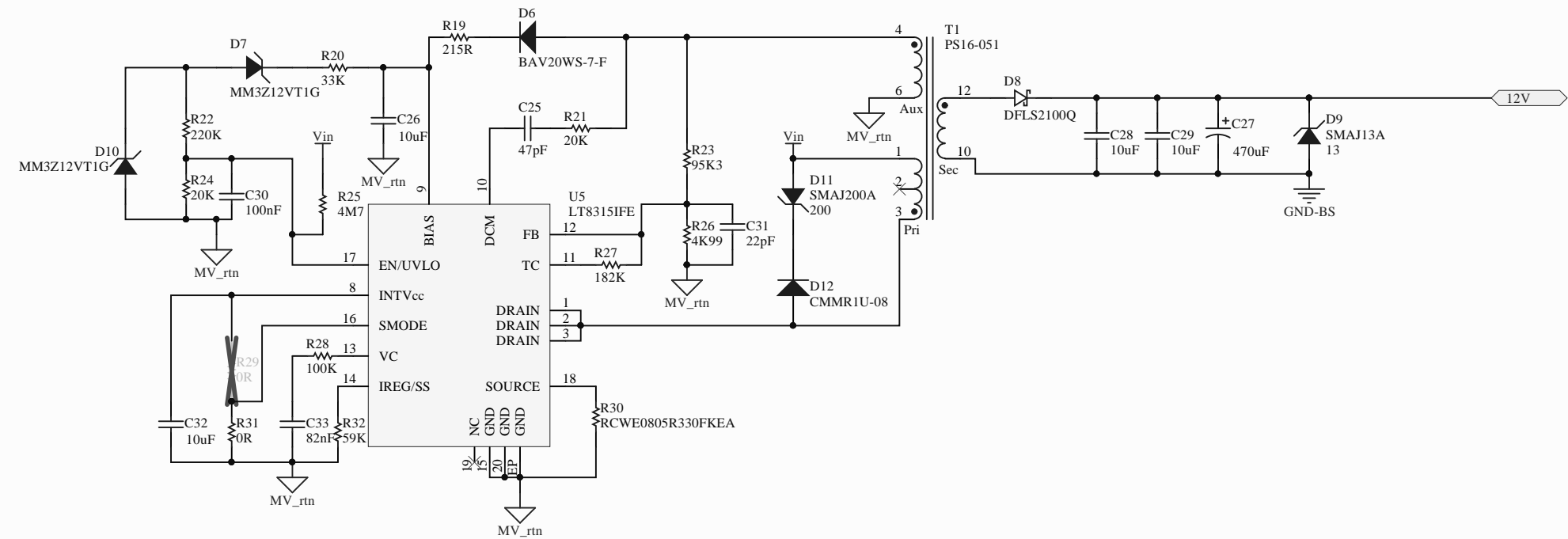
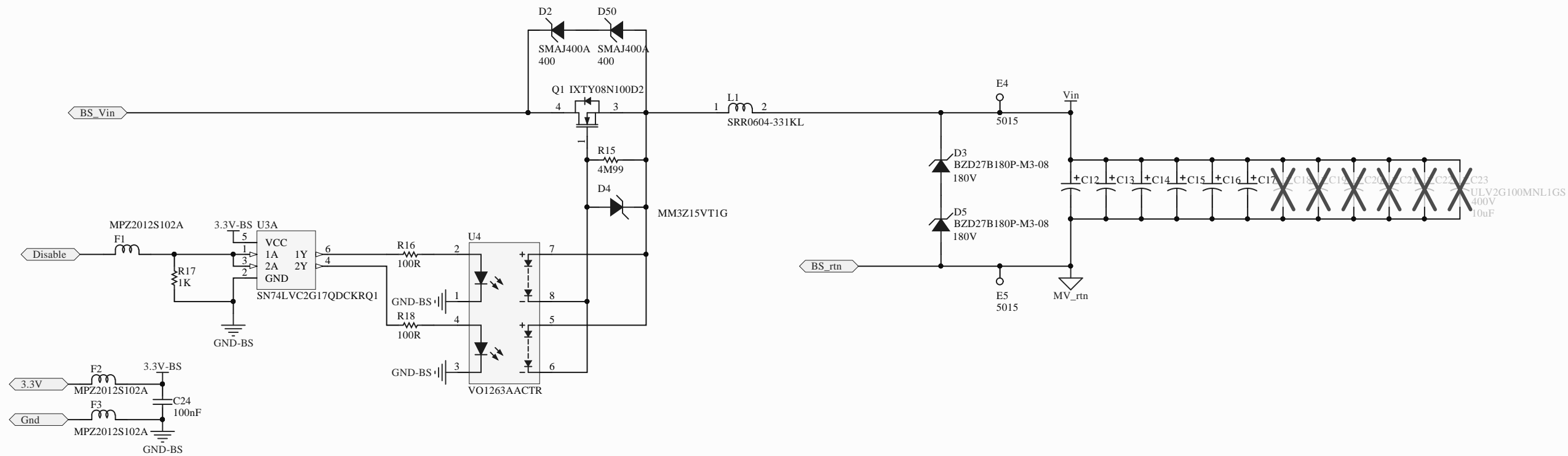
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Project Title: <i>IgbtControl.PrjPcb</i>				
Size: Tabloid	Number:	Revision:		
Date: 10/9/2019	Time: 4:35:13 PM	Sheet * of *		
Author: *	File: Window_Comparator.SchDoc			

Assume Z0=120 ohm in GSSG configuration:  
According to TI AN-847 (<http://www.ti.com/lit/an/snla031/snla031.pdf>), 750/130/750 will be a good value




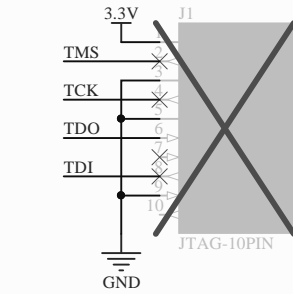
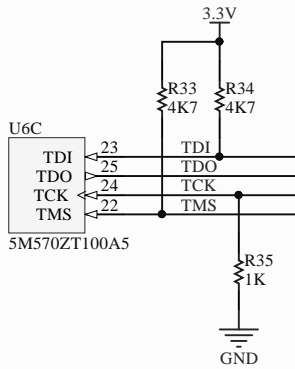
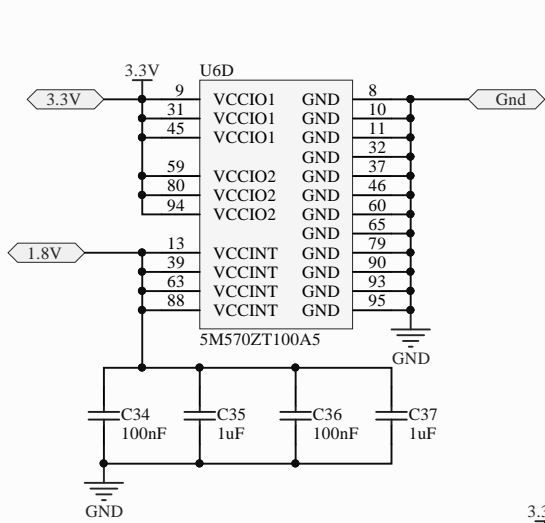




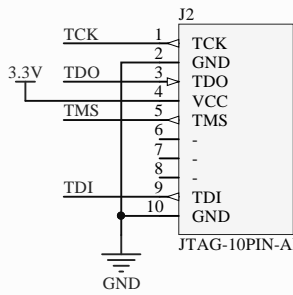


From DC2337A demo board design:  
<http://www.analog.com/media/en/dsp-documentation/evaluation-kit-manuals/DC2337AF.PDF>

Sheet Title: *			<b><i>Makani Project</i></b> Google Inc. 2175 Monarch St. Alameda CA, 94501 USA	
Project Title: <b><i>IgbtControl.PrjPcb</i></b>				
Size: Tabloid	Number:	Revision:		
Date: 10/9/2019	Time: 4:35:14 PM	Sheet * of *		
Author: *	File: Bootstrap.SchDoc			

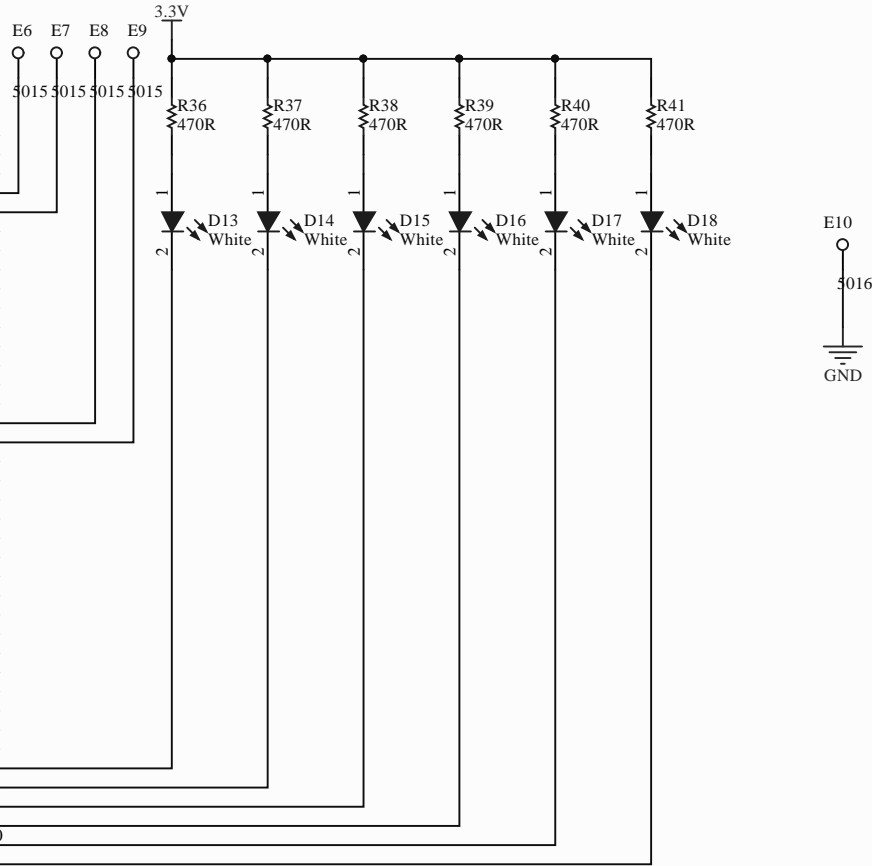
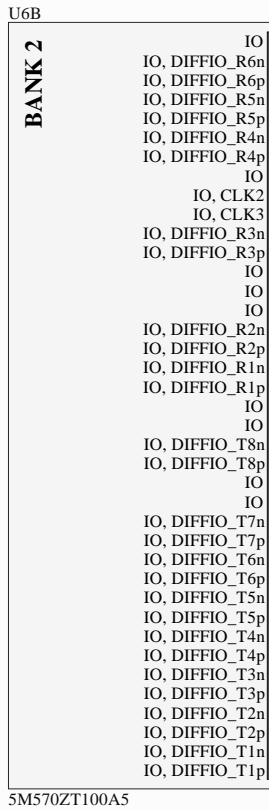
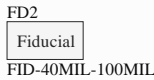
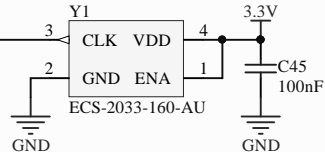
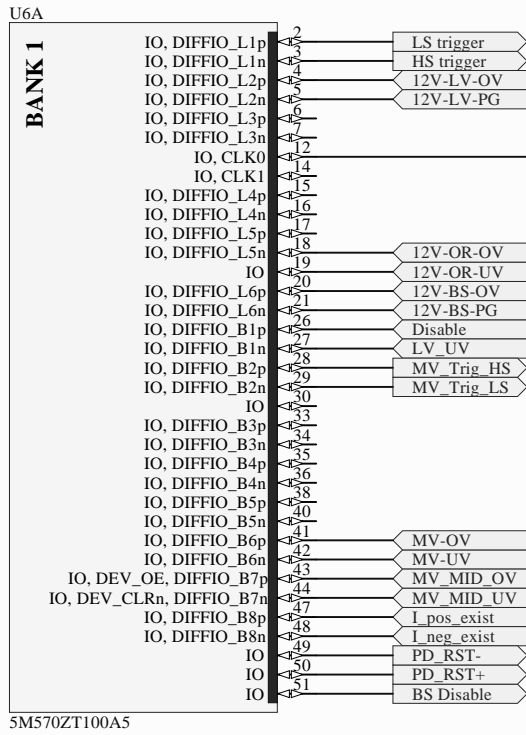
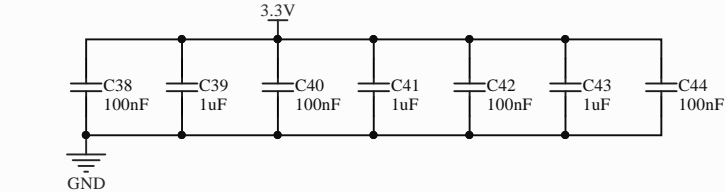


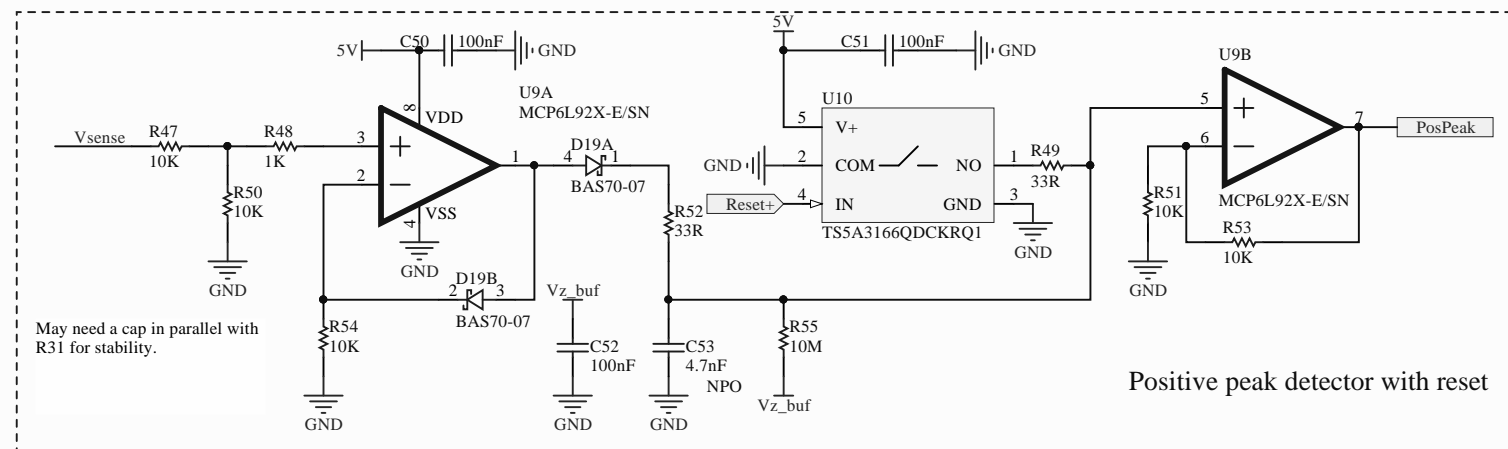
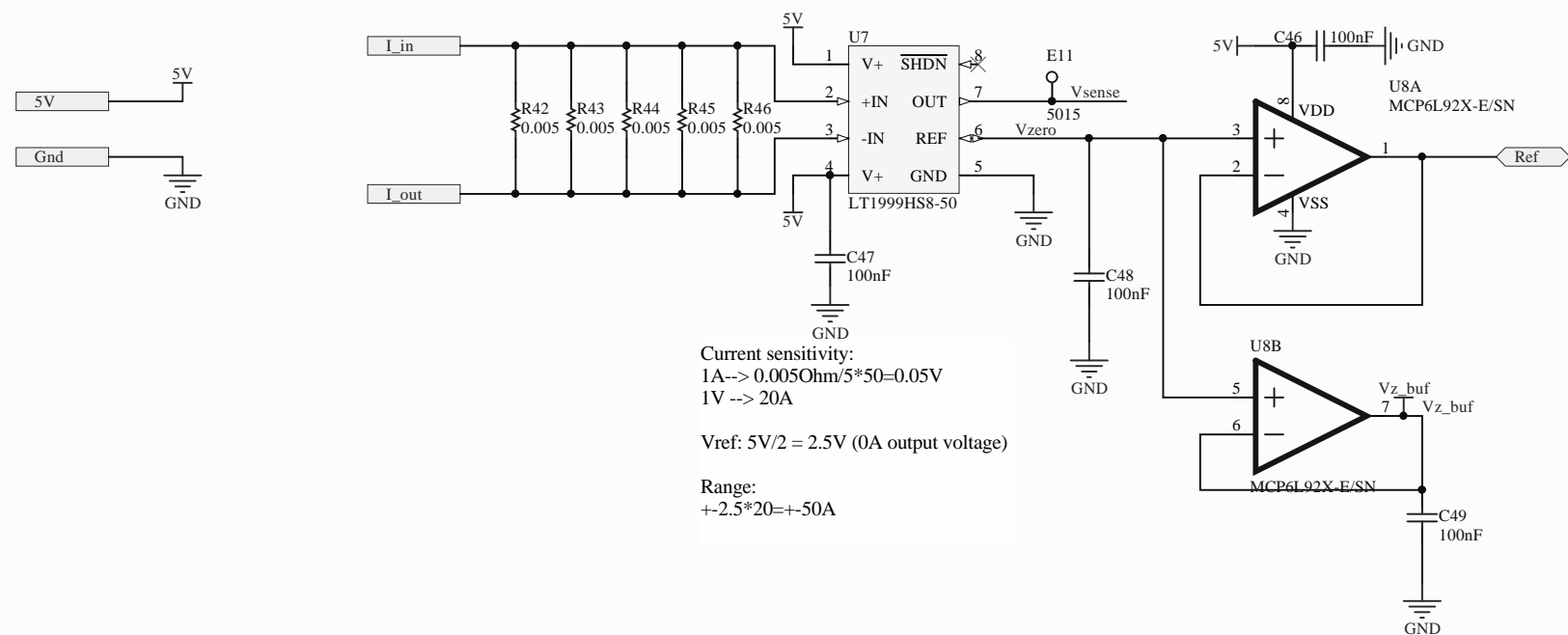
ARM JTAG



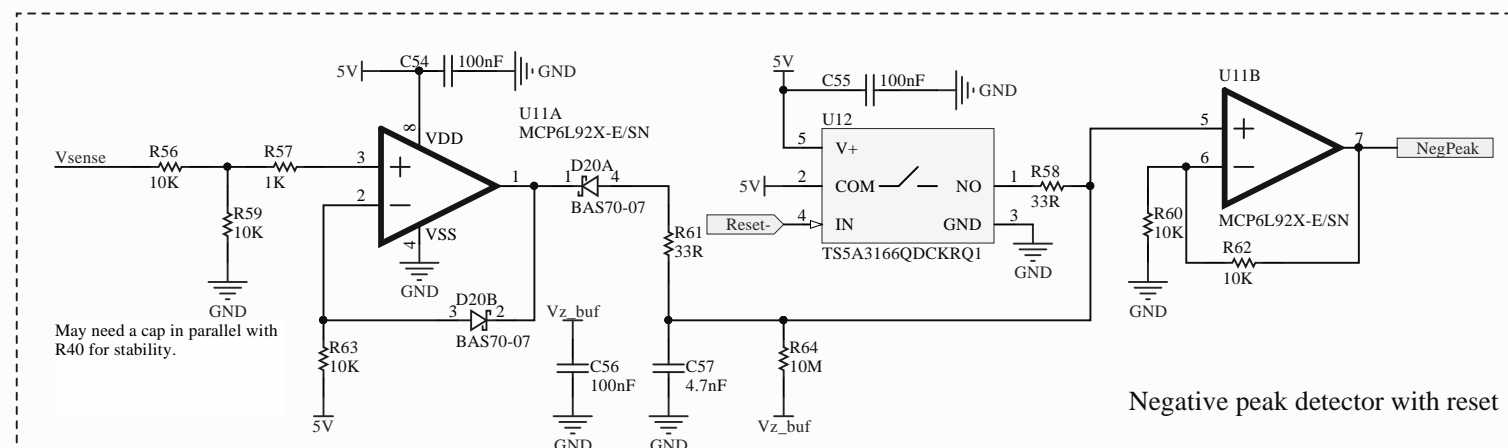
Altera JTAG


[https://www.altera.com/en\\_US/pdfs/literatu re/ug/ug\\_usb\\_blstr.pdf](https://www.altera.com/en_US/pdfs/literatu re/ug/ug_usb_blstr.pdf)





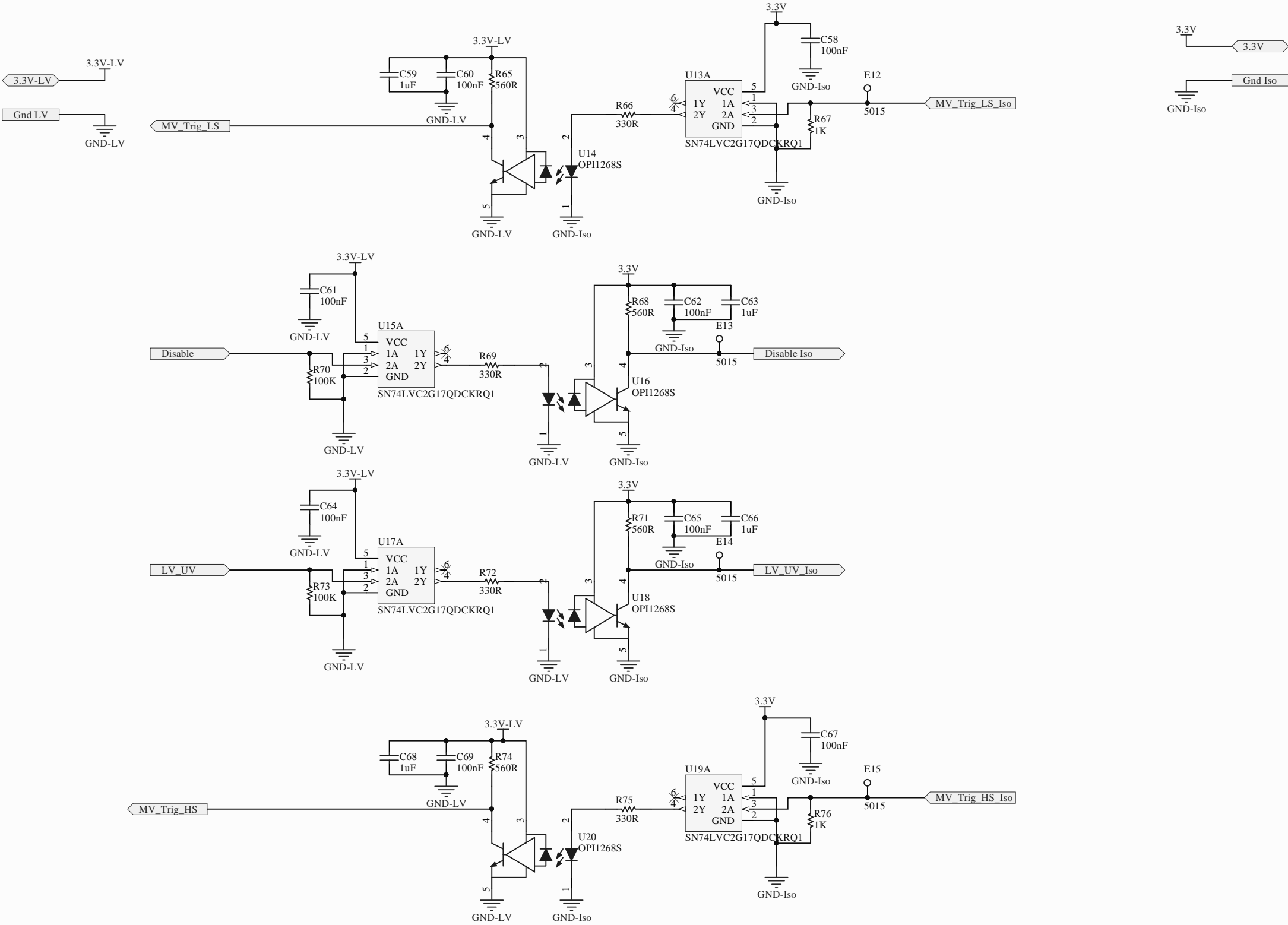
BAS70-07 from Infinion for  
matched pair.  
BAS7007E6327HTSA1  
Digikey PN  
BAS7007E6327HTSA1CT-ND

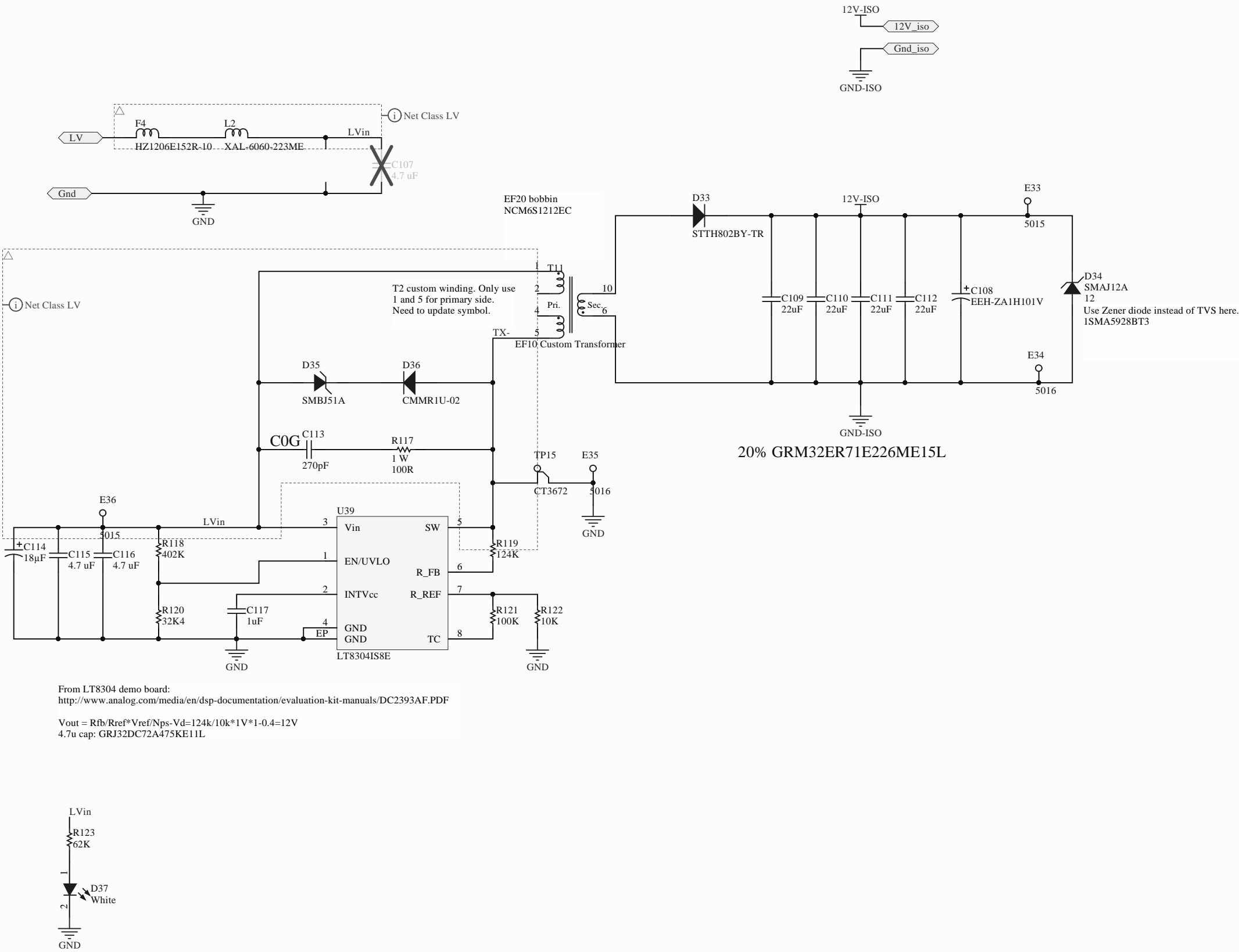


Sheet Title: *			* * * * *	
Project Title: <b><i>IgbtControl.PrjPcb</i></b>				
Size: Tabloid	Number:	Revision:		
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Author: *	File: Current_Sensor.SchDoc			



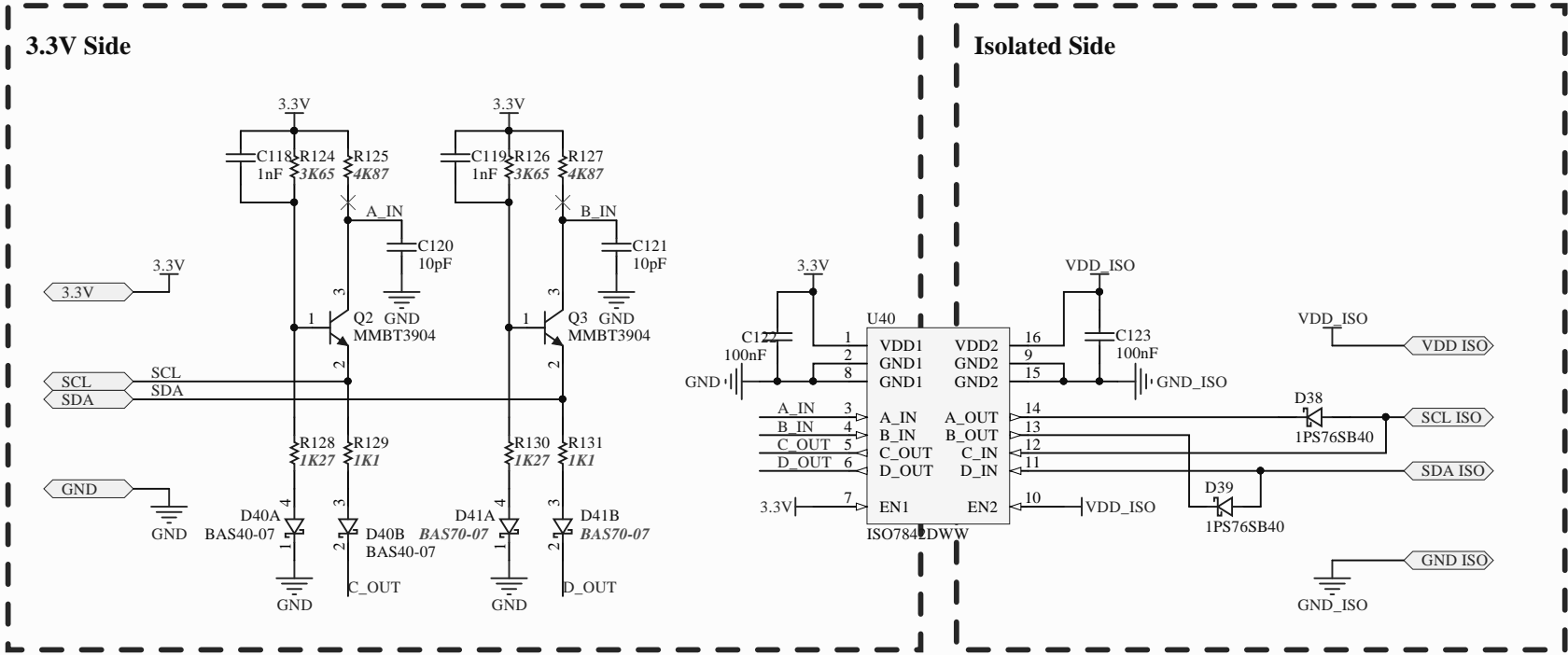
This configuration is a non-inverting buffer. Need to check turn-on/turn-off conditions





From LT8304 demo board:  
<http://www.analog.com/media/en/dsp-documentation/evaluation-kit-manuals/DC2393AF.PDF>

$V_{out} = R_{fb}/R_{ref} \cdot V_{ref}/N_{ps} - V_d = 124k/10k \cdot 1V \cdot 1 - 0.4 = 12V$   
4.7u cap: GRJ32DC72A475KE11L

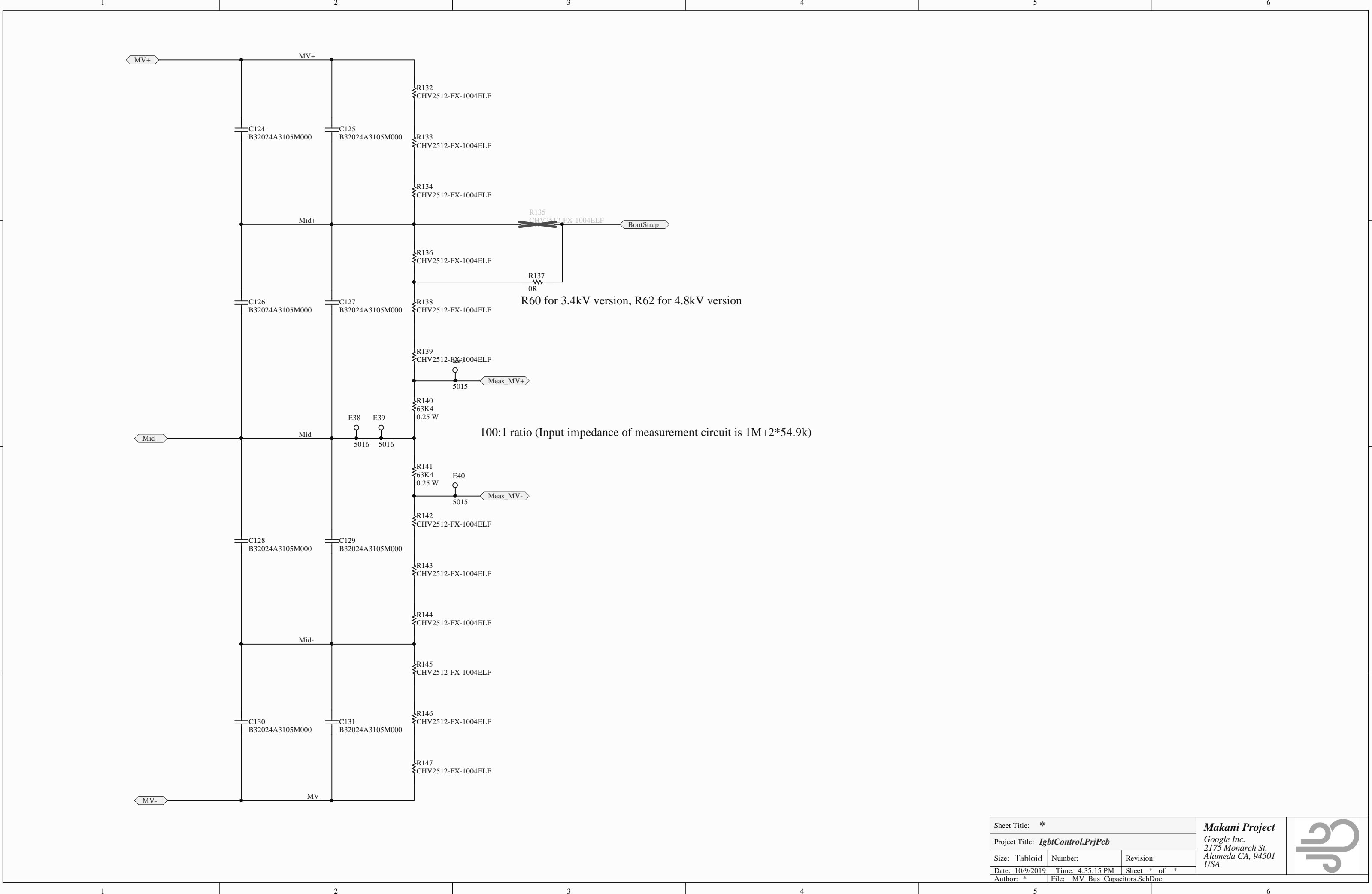


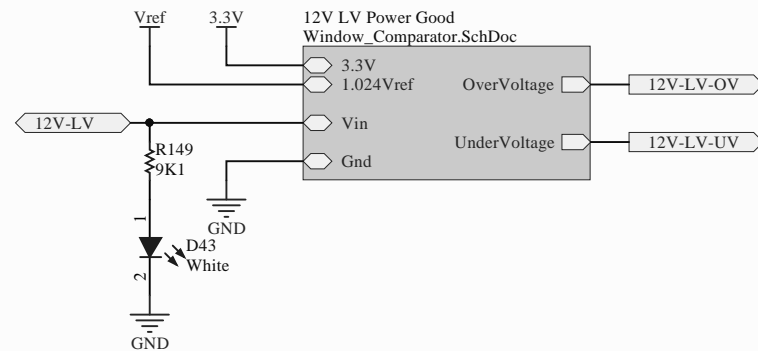
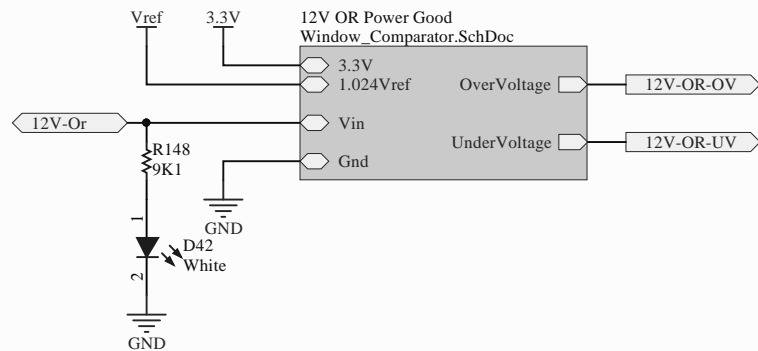
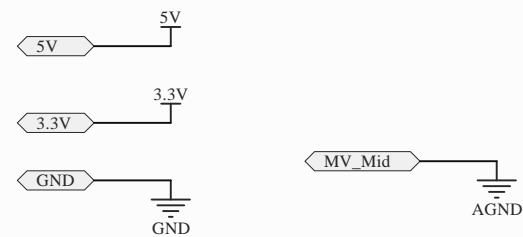
Bidirectional isolated I2C interface (external 4.7kOhm I2C pullup resistor required)

Function:  
2828Vdc isolated I2C interface with bidirectional I2C bus  
Input: (3.3V side, I2C master)  
3.3V 3.3V power  
GND Ground of 3.3V power  
SCL I2C bus clock input on 3.3V logic side, bidirectional  
SDA I2C bus data I/O on 3.3V logic side, bidirectional  
Output: (VDD\_ISO side)  
VCC\_ISO DC power of output side, 2.5V to 5V  
GND\_ISO Ground of output side  
SCL\_ISO I2C bus clock output on VCC2 side, bidirectional  
SDA\_ISO I2C bus data I/O on VCC2 side, bidirectional

Specification:  
Isolation  
Viowm 2828Vdc (working voltage)  
Viotm 8000Vpk  
Viso 5700Vrms (UL 1577 1minutes)  
Input voltage 3.3V  
Ouput voltage 2.5-5V

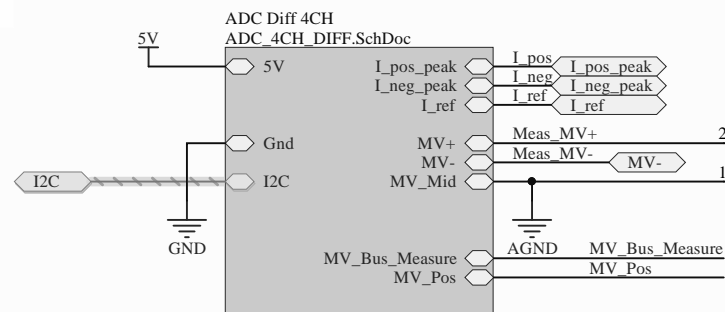
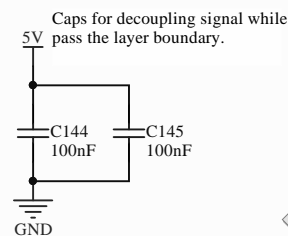
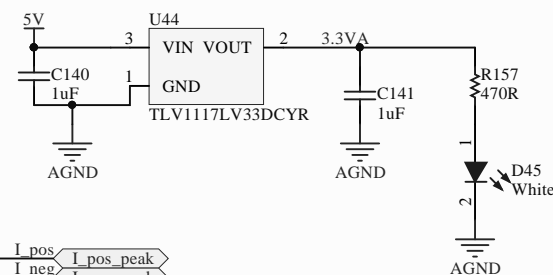
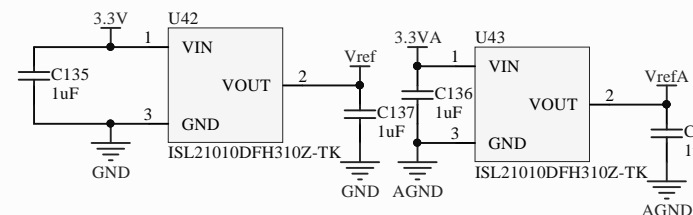
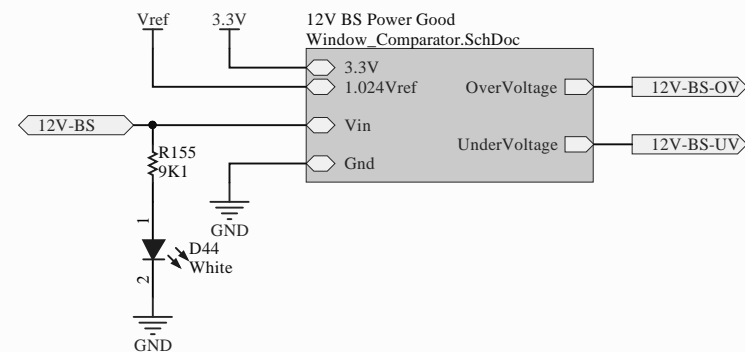
Comments:  
1. C3, C5(1nF) is optional. It can reduce propagation delay by increase the charge injection into Q1's base  
2. C4, C6 (10pF) is optional. It is used to avoid false triggering of the isolator  
3. R2/R7, R3/R6, R4/R5, adn R1/R8 are optimized for 3.3V input and 4.7kOhm bus pull up resistor.  
4. VCC2 side pull up resistor can be other value





Difference amplifier to convert differential signal to single ended.  
Compare with reference

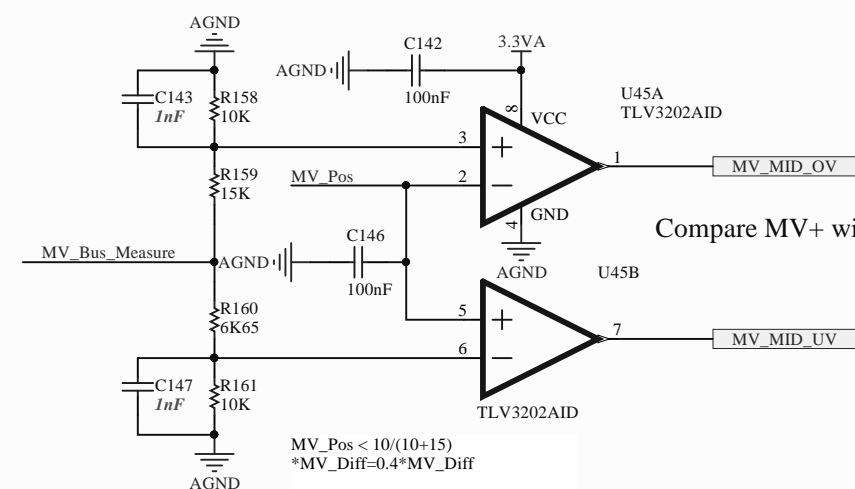
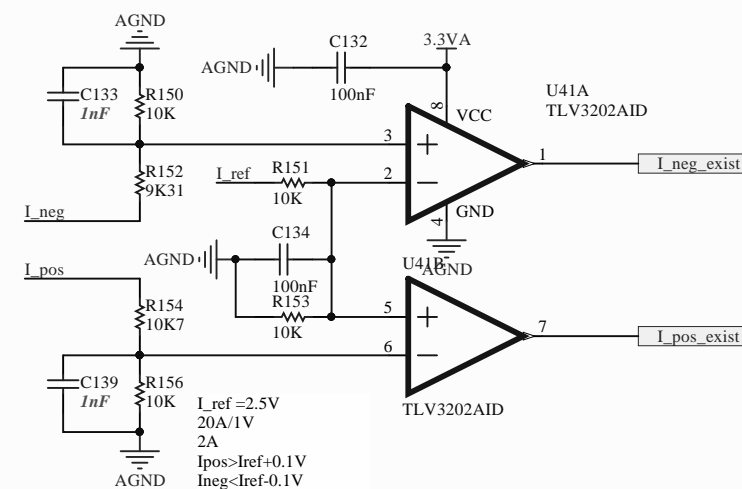
CPLD for fast fault handling  
Slow signal can be processed by AIO on LV side  
12V power should be processed by CPLD to determine operation mode (BS vs Normal)



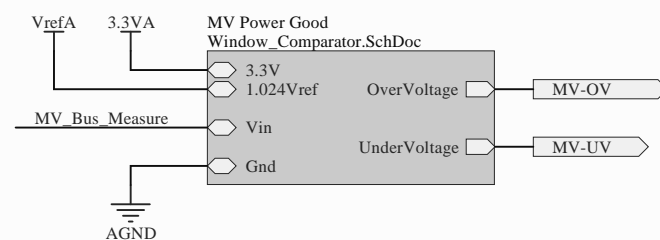
## Seperated ground for noise immunity


MV+ measurement locates at far side of the board. Although it is reference to the same AGND, it is treated as a differential signal here. A long PCB trace of AGND from far side should run with the signal.

Current: 20A/1V; Voltage 0.515V/1000V



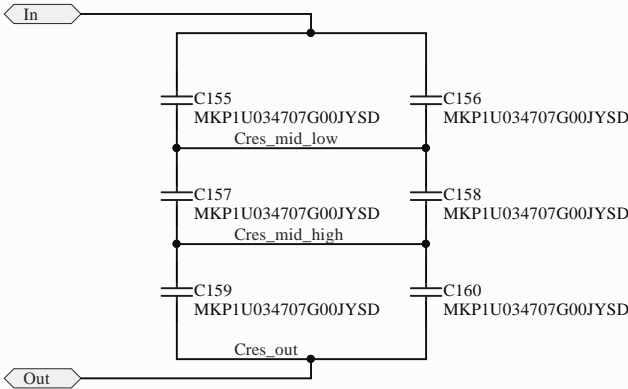
Compare  $MV_+$  with  $MV/2$ , if the difference is too much,  $MV$  is not balanced



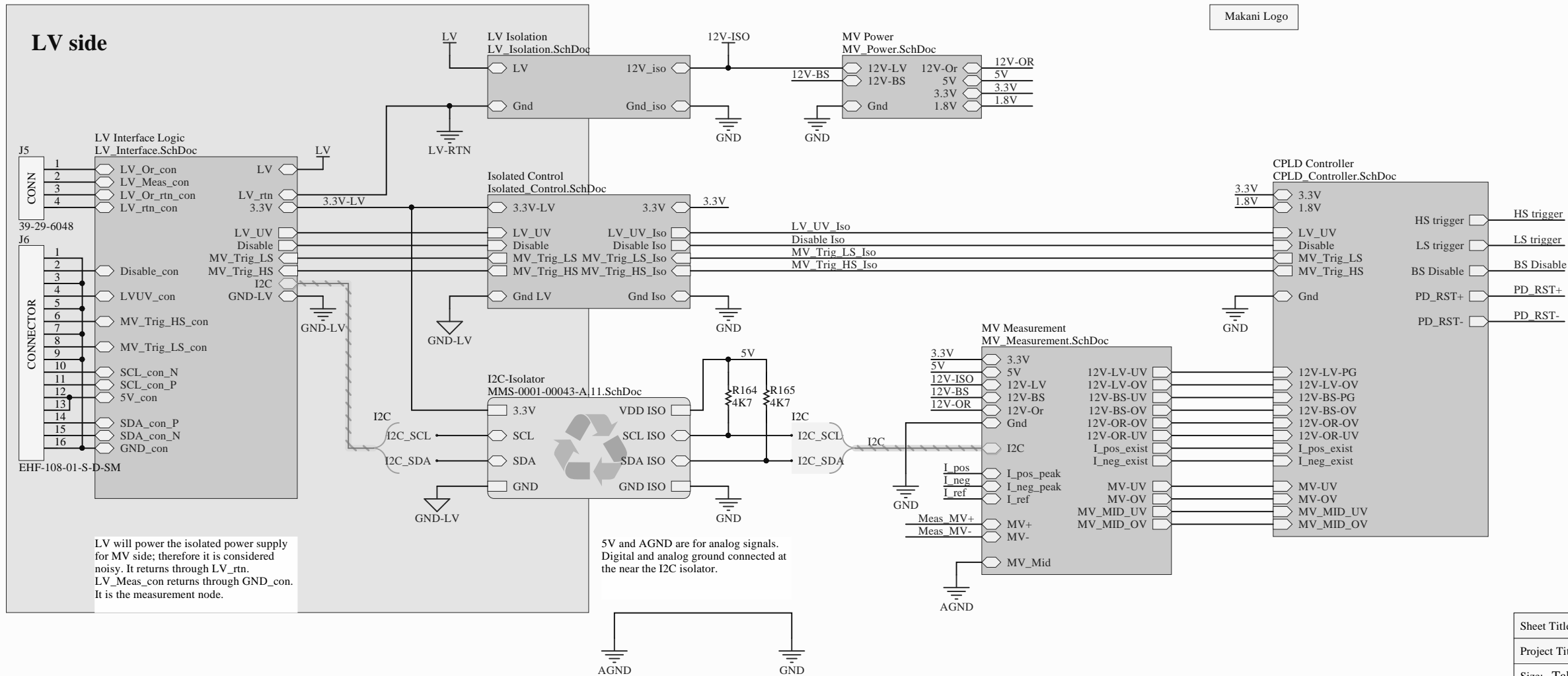
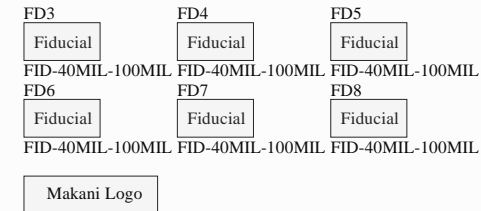
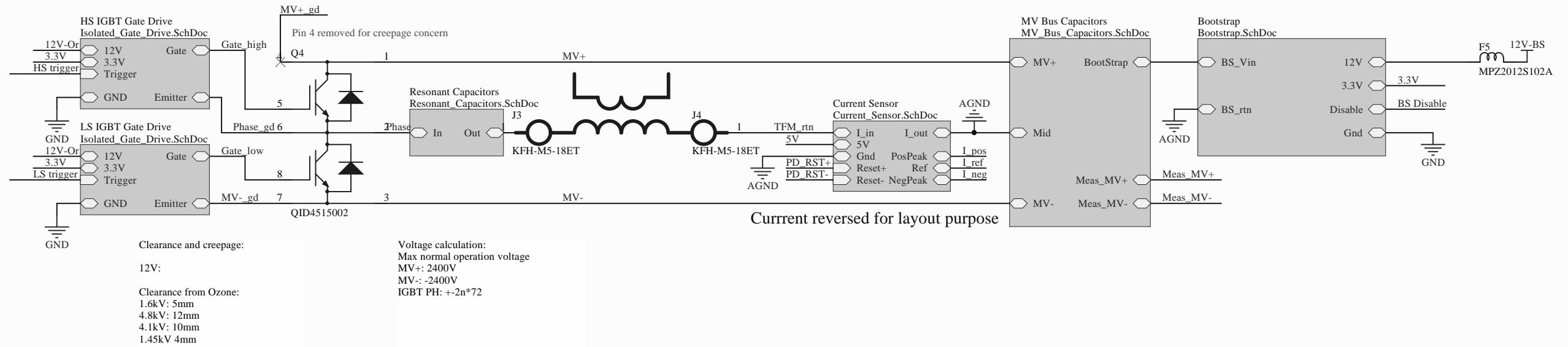
Sheet Title: *			<b>Makani Project</b> Google Inc. 2175 Monarch St. Alameda CA, 94501 USA	
Project Title: <b>IgbtControl.PrjPcb</b>				
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Naming convention:  
1. LV side netname ends with "-LV".



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