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VLSI LAB 4

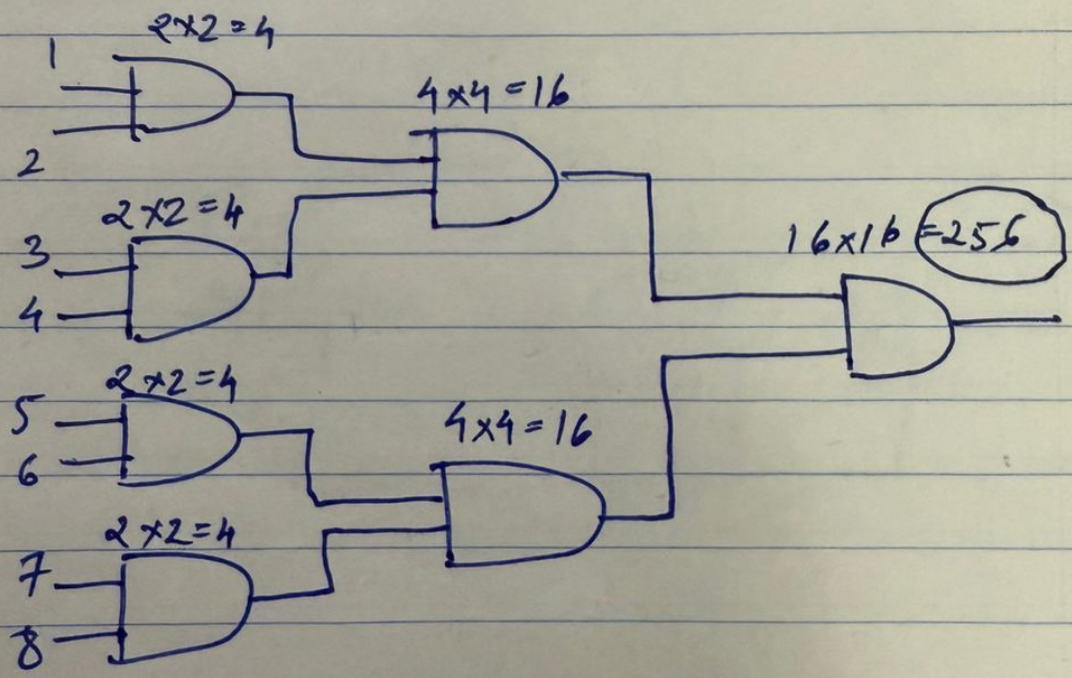
1.

8b-256 WL decoder design for an SRAM array.

Q.1.) (i) 8b-256 WL

8 input lines

256 output lines

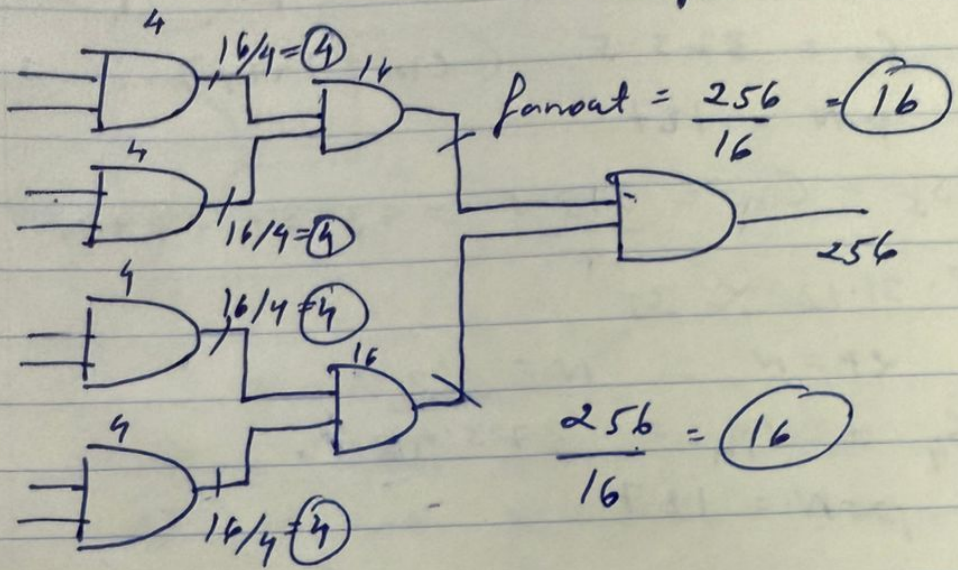


Replica count

RC of address input = 2

(8 inputs)

(ii) Fanout factor = $\frac{\text{RC of given gate}}{\text{RC of driver}}$



fanout at each stage.

(iii) $C_{LOAD} = (C_{passgate} + C_{WL}) \times 256$

$C_{LOAD} = (120 + 55)af \times 256$

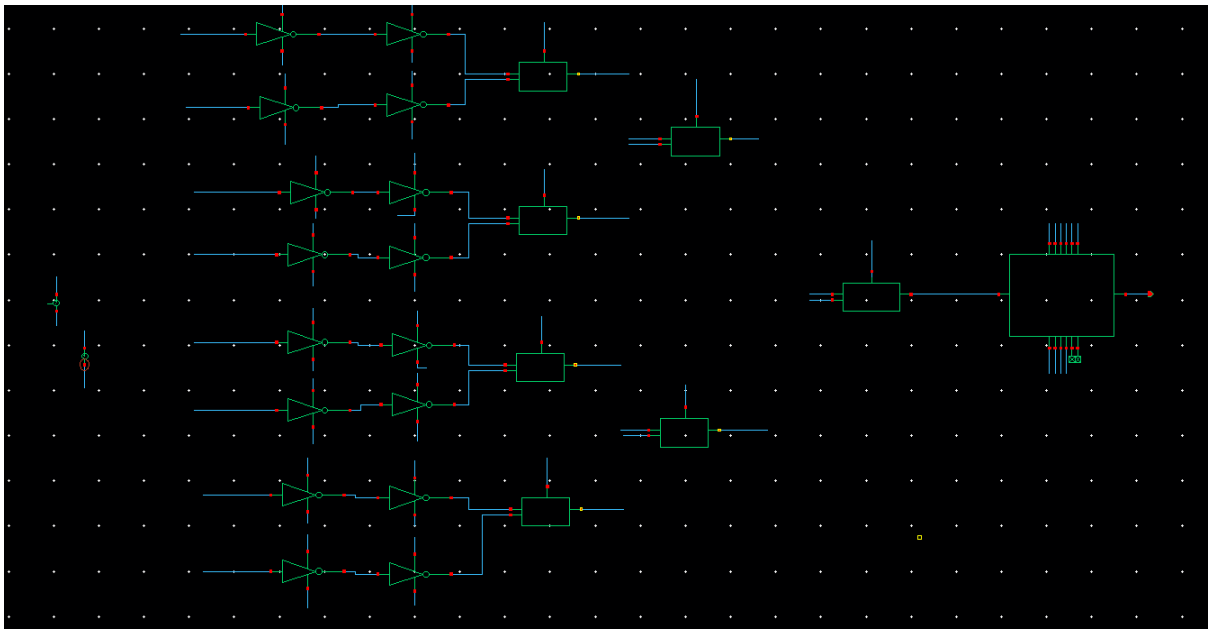
$= 0.175 \times 256 = 44.8$

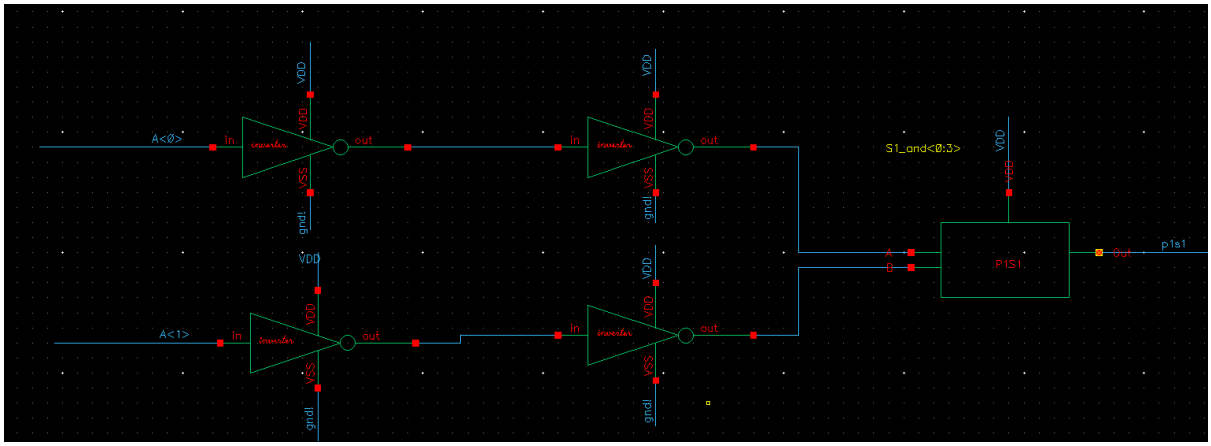
Per gate $c = \frac{120}{fanout} = \frac{120}{4} = 30$ fins.

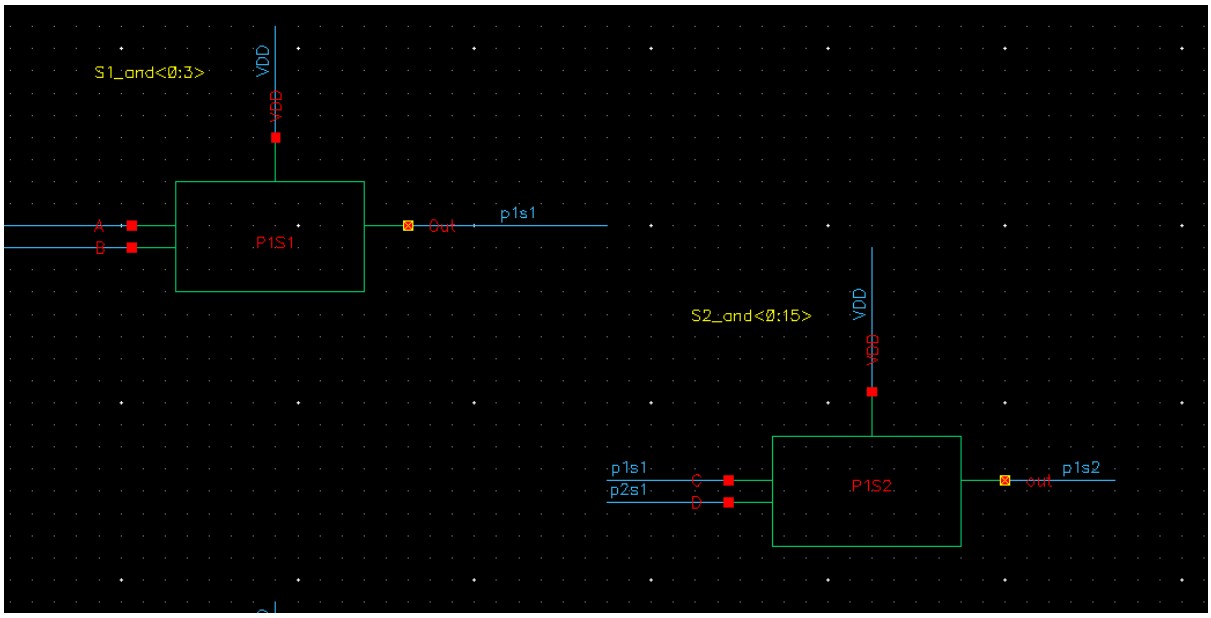
$\frac{44.8}{0.030} = 1493.3 \approx 1494$ fins.

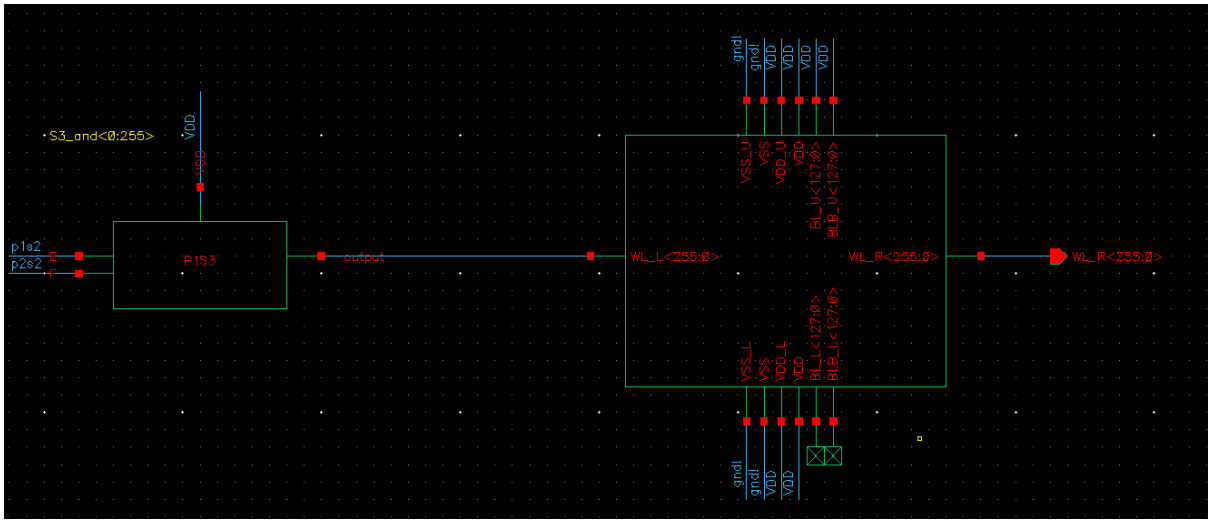
C load = 1494 fins.

SCHEMATIC DESIGN. Broke down the schematic in multiple screenshots for visibility.



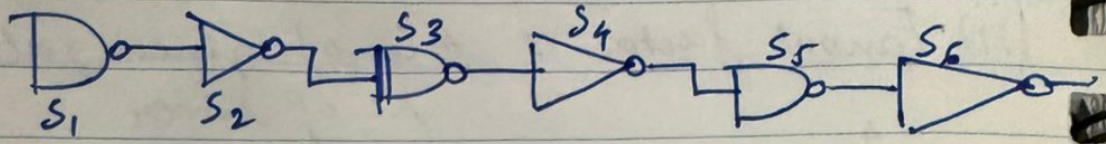





S3_and<0:255>
VDD
vdd
p1s2
p2s2
E
F
P1S3
output
gnd!
VDD
VSS_U
VSS
VDD_U
BL_U<127:0>
BLB_U<127:0>
WL_L<255:0>
WL_R<255:0>
VSS_L
VDD_L
BL_L<127:0>
BLB_L<127:0>
WL_R<255:0>

2. Sizing calculations

Q2.)



$S_6 = 373.5 \quad (C_{in} = 1494)$

$p.N = 187$

$S_5 = C_{in} = \frac{373.5}{4} = 93.37 = p+N$

$p \cdot 31.12 \approx 31$

$2p = N \quad \therefore N = 62.$

$S_4 = C_{in} = 373.48$

$p = N = 187$

$S_3 = \frac{373.48}{4} = 93.37 = p+N$

$2p = N$

$p = 31 \; ; N = 62$

$S_2 : C_{in} = \frac{93.37 \times 4}{4}$

$p = N = 47$

$S_1 : C_{in} = \frac{93.37}{4} = 23.34 = p+N$

$2p = N$

$p = 7.78 \approx 8 \; , N = 16.$

3.

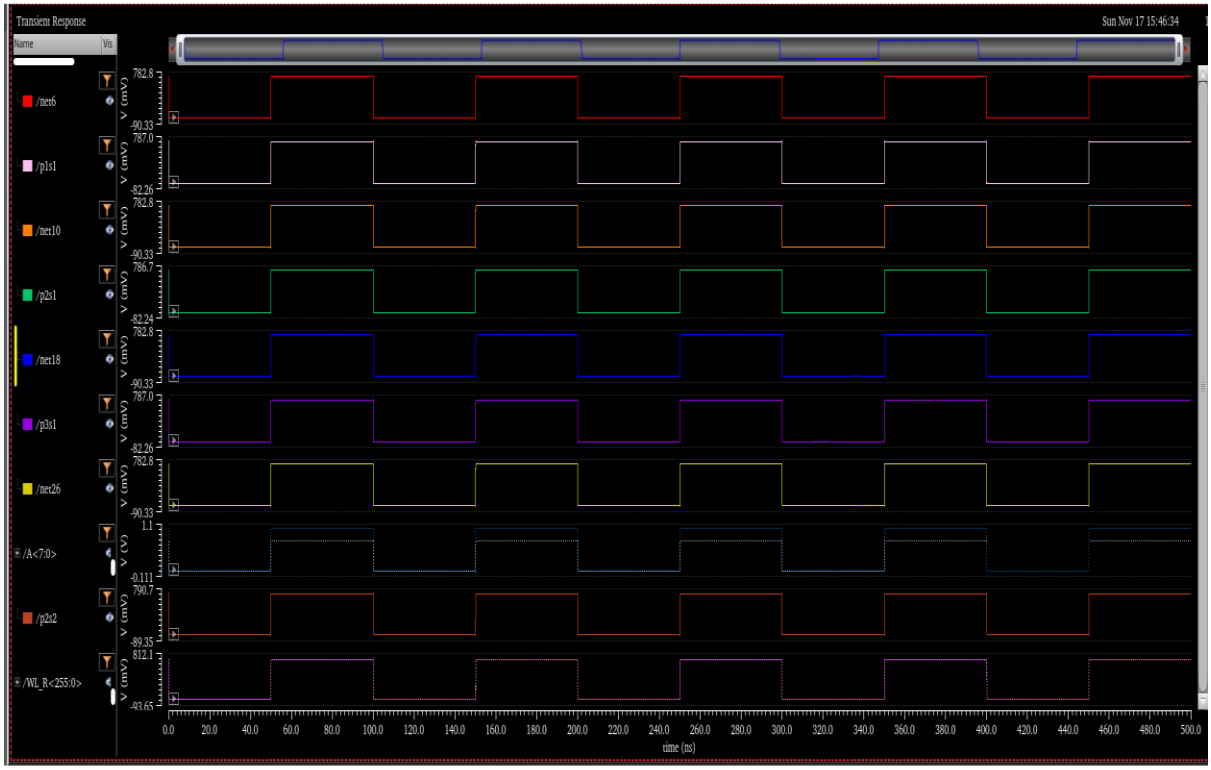


Figure 1 Simulation for Q1 schematic

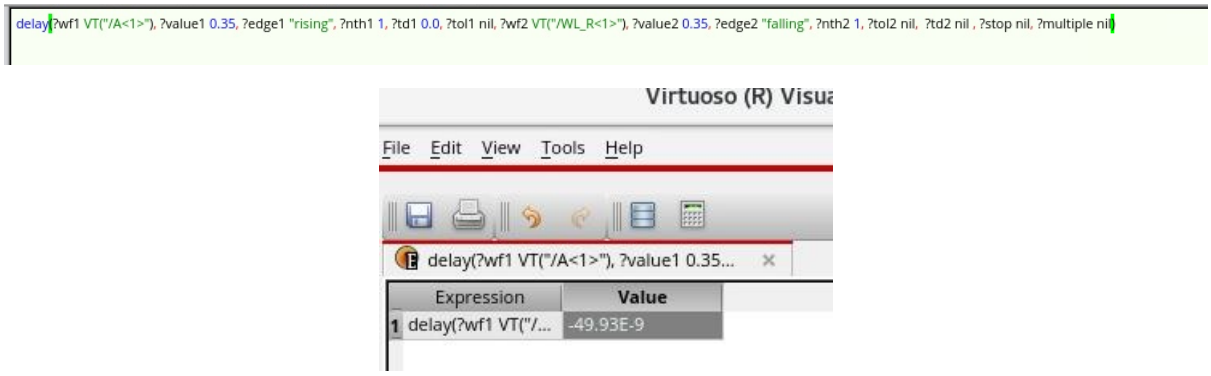
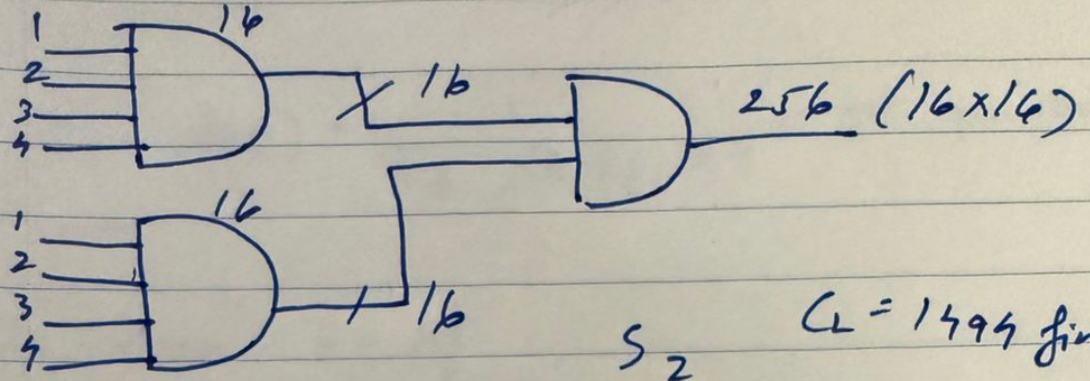


Figure 2 Power for Q1 schematic

4.

Q4) Increasing fan in



$S_2 \therefore C_{in} = \frac{1494}{4} = 373.5$

Inv : $P = N = 187$

AND : $P + N = \frac{373.5}{4} = 93.37$

$2P = N \longrightarrow P = 31, N = 62.$

$S_1 \div C_{in} = \frac{373.5 \times 93.37}{4} = 373.48$

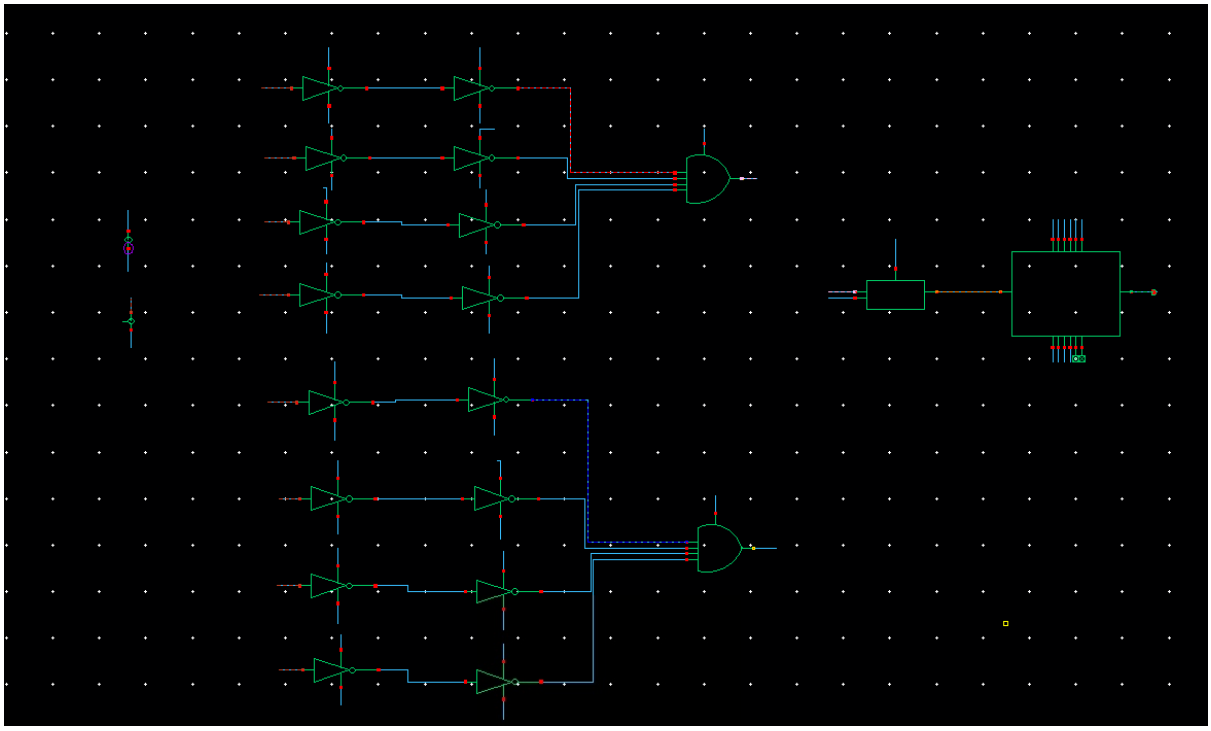
Inv = $P = N = 187$

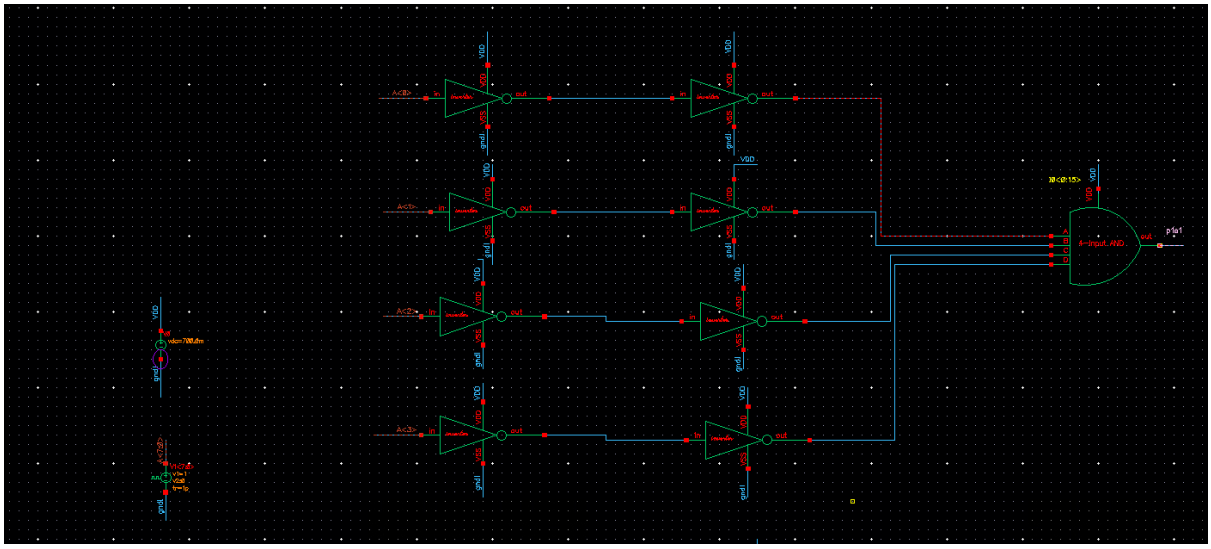
AND = $P + N = \frac{373.48}{4} = 93.37$

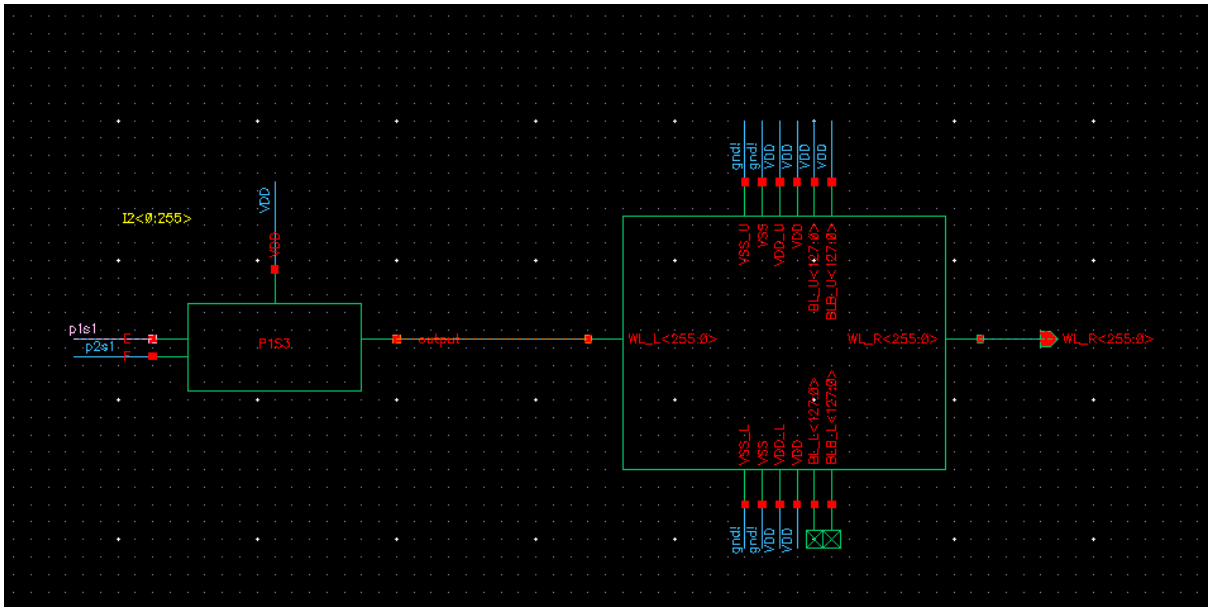
$4P = N$

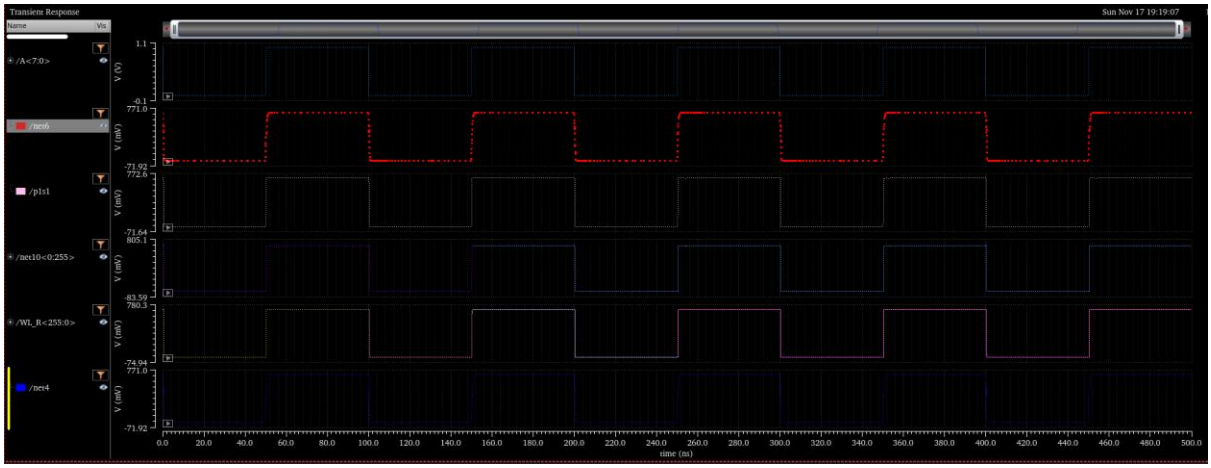
$P = 18.6 \simeq 19$

$N = 76.$




vdd
gnd
A<0>
A<1>
A<2>
A<3>
in
out
inverter
A<0:15>
4-input_AND
P1p1





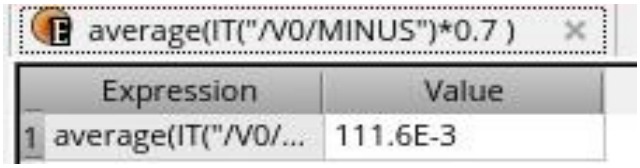


Figure 3 Power consumption

Figure 4 Delay

5.

Expression	Value
average(IT("/V0/...	128.9E-3

From the simulation and graph, the average power is calculated using the AVERAGE function from the calculator. (Q1 schematic)

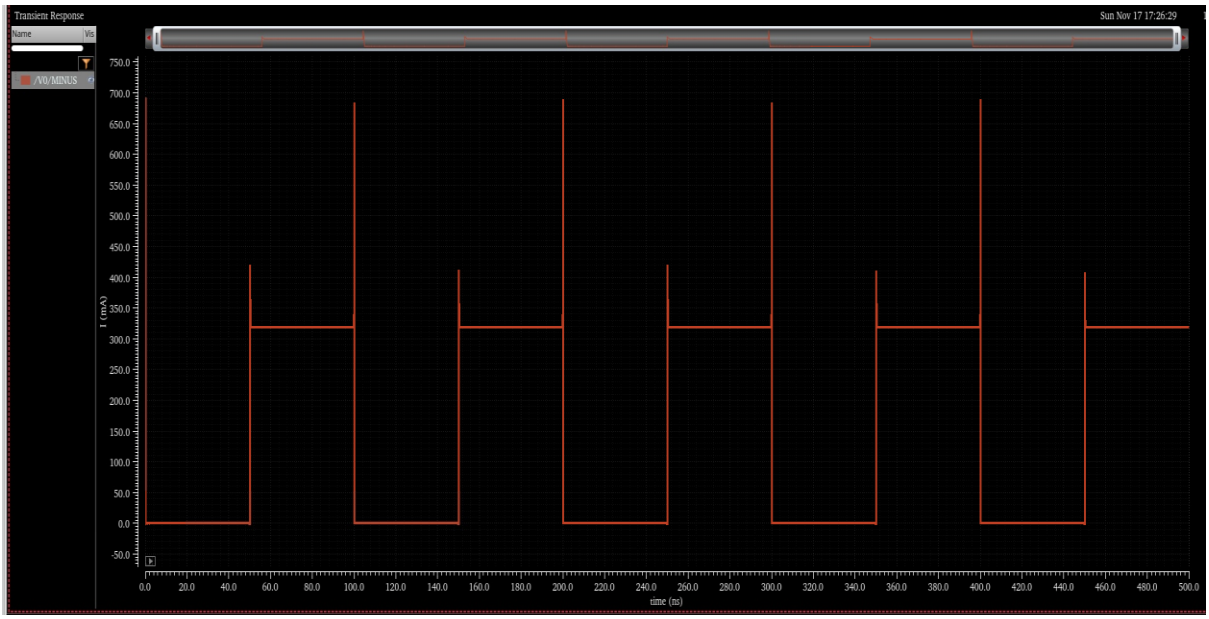


Figure 5 Current waveform of schematic in Q1

6. To resolve or minimize glitches caused by unequal arrival times of input waveforms in downstream decode stages for a low power design,

- The signal paths should have equal length to synchronize signal arrival.
- Symmetric design/ layout can help minimise delay.
- Buffer insertion for signal synchronization.

7.

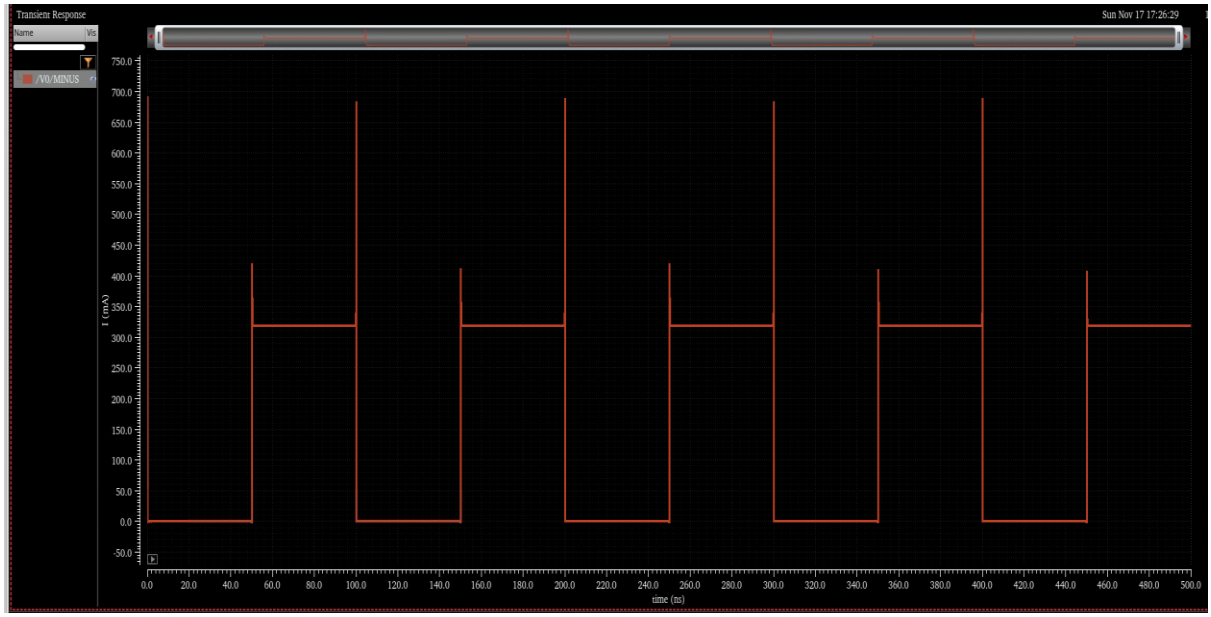


Figure 6 Current waveform of schematic in Q1

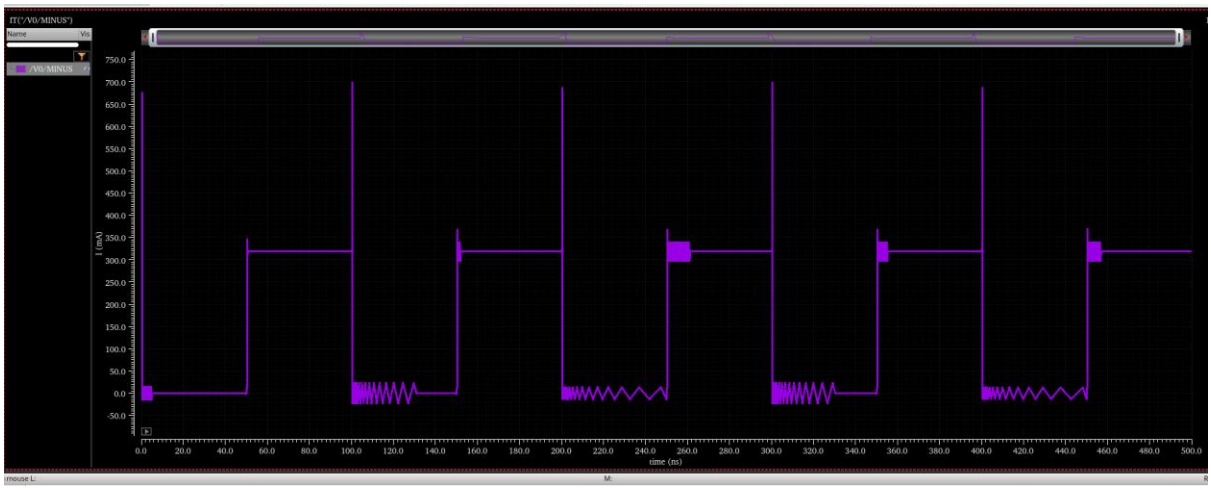


Figure 7 Current waveform of 4-input AND 8b decoder (Q4 schematic)