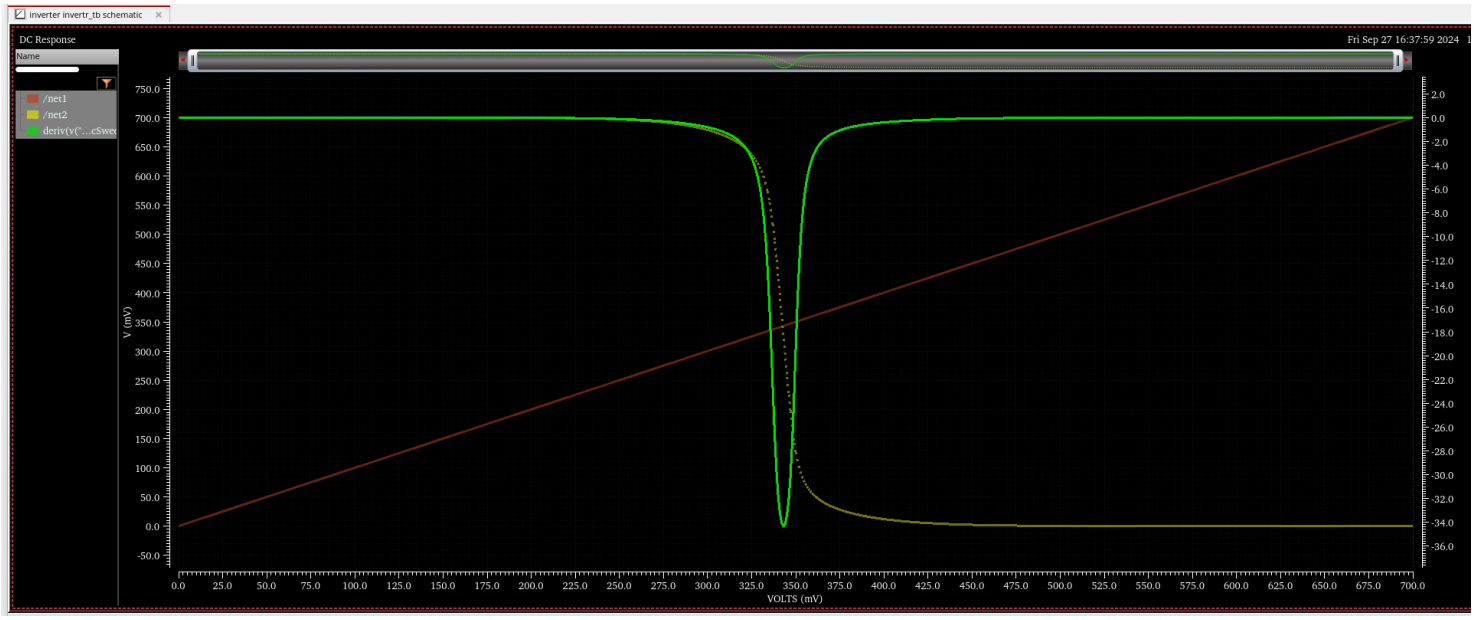
VLSI LAB-2

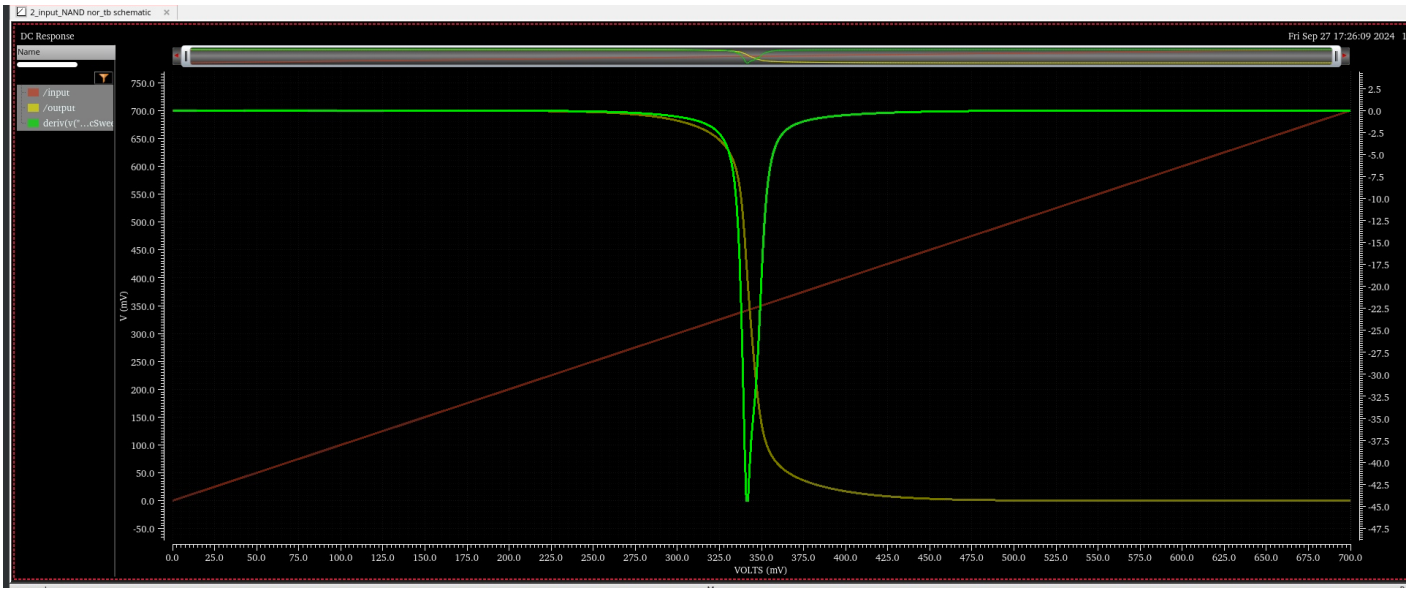
1) INVERTER



Gain at Vin = Vout is -34.324

Threshold voltage 342.6 mV

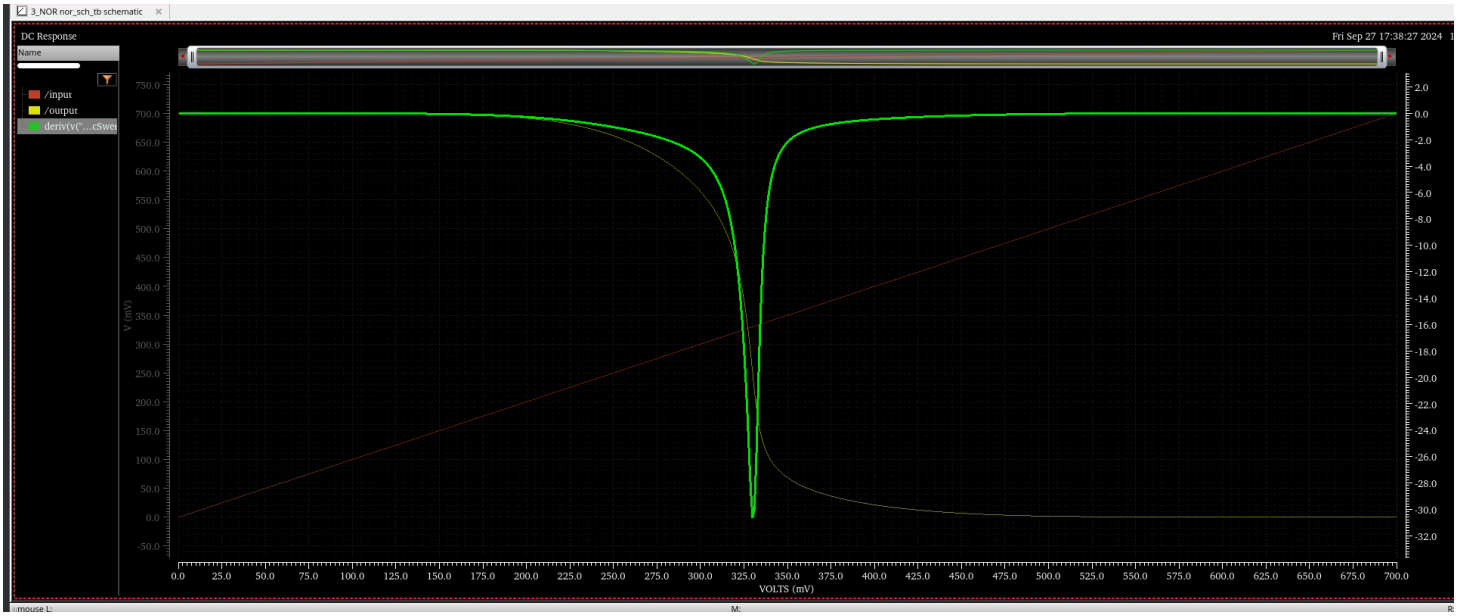
2) NAND



Gain at Vin = Vout is -33.792

Threshold voltage = 348.6 mV

3) 3 input nor

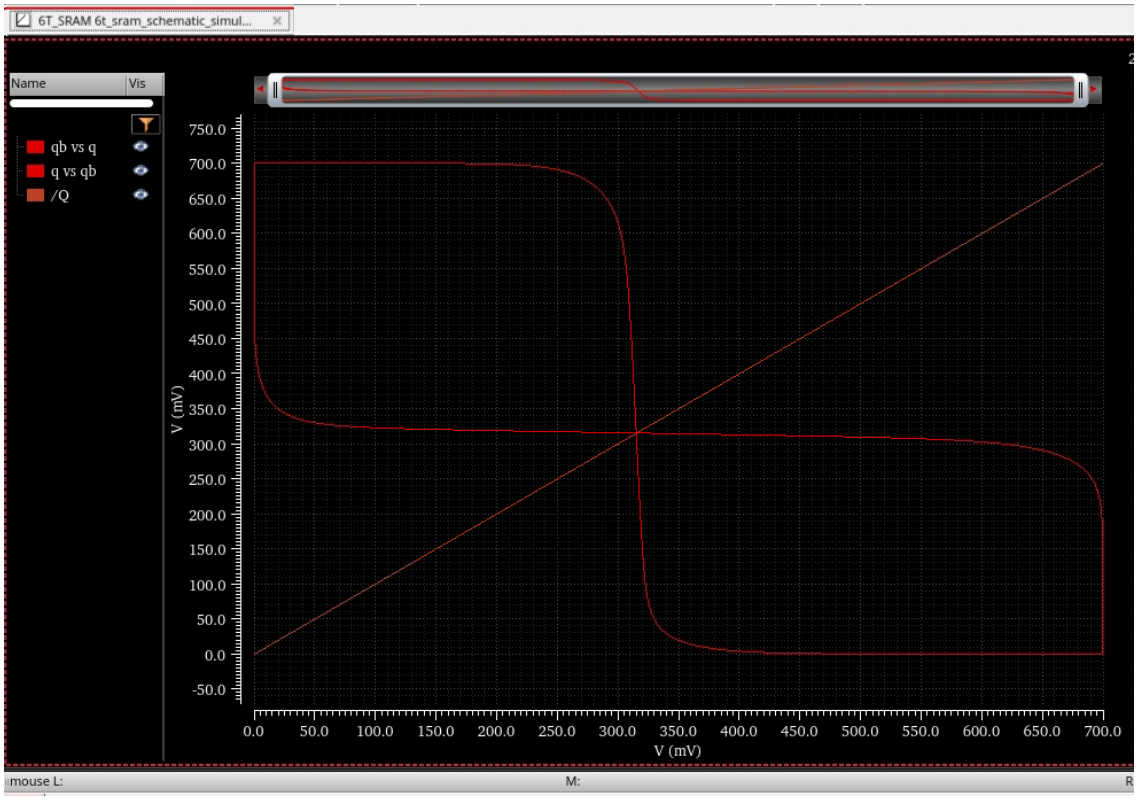


Gain = -55.6

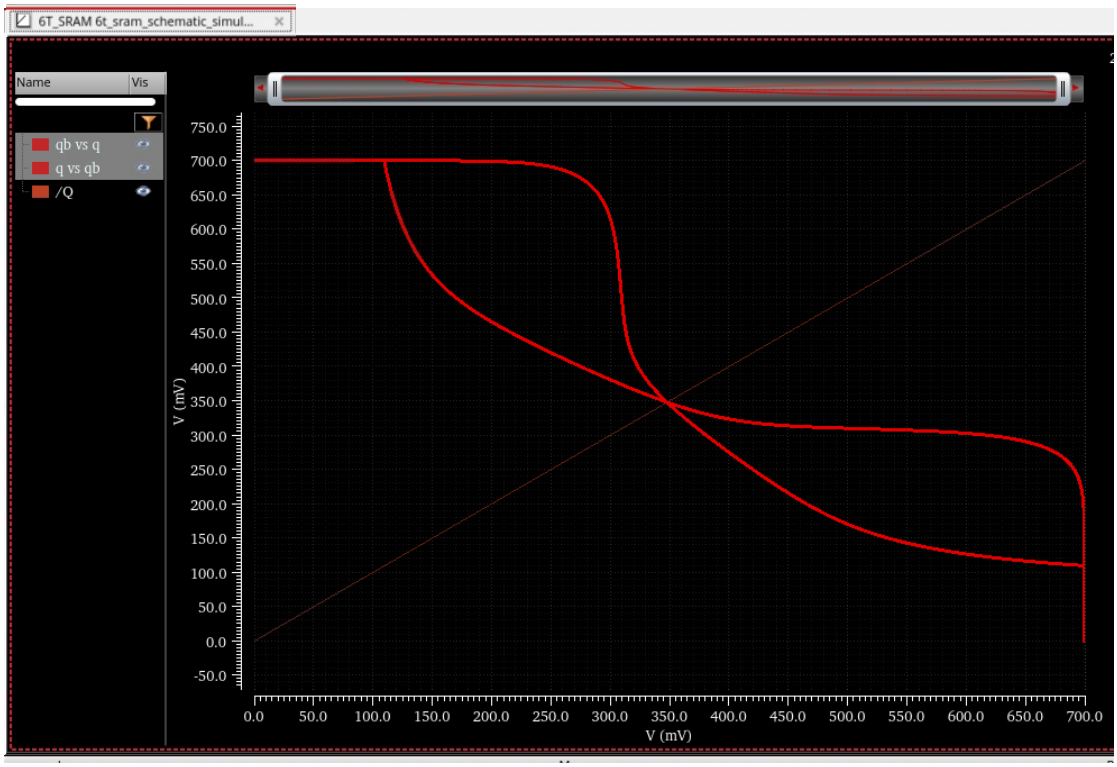
Threshold voltage = 343.2 mV

4) SRAM

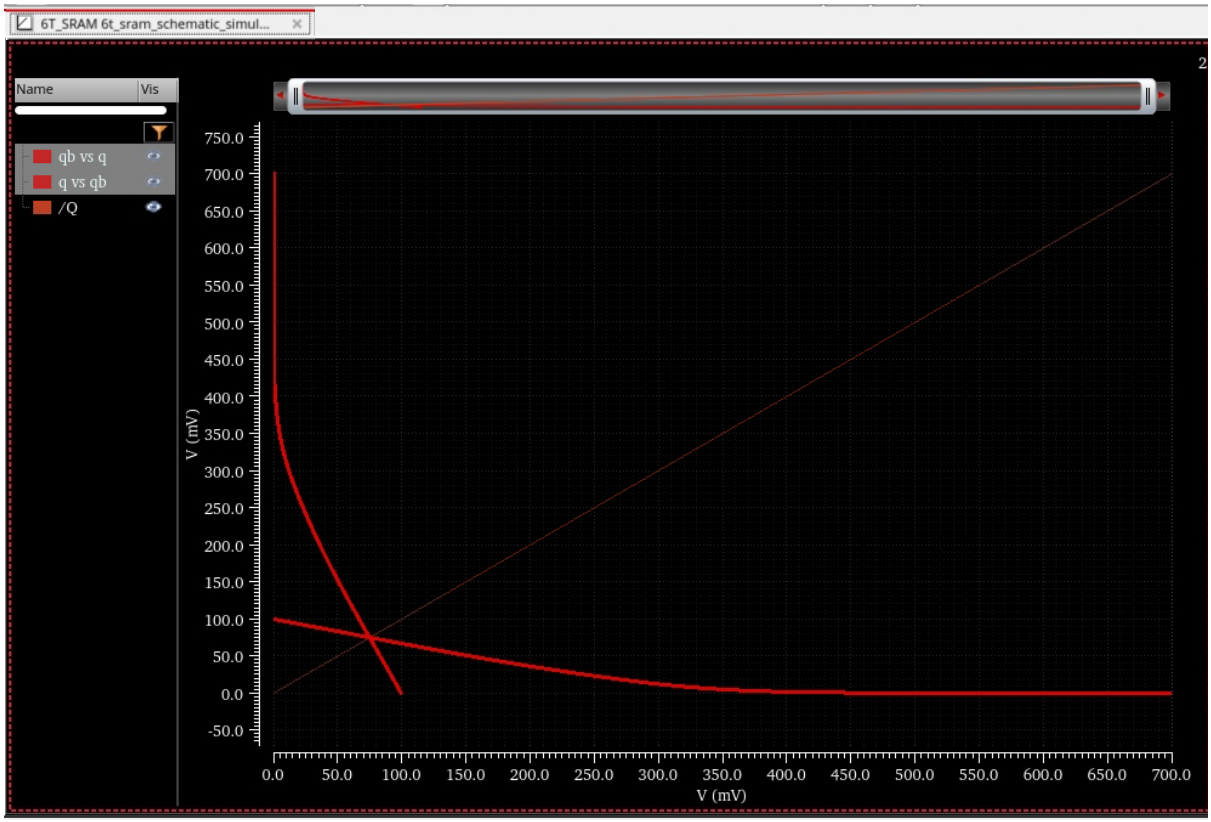
a)


6T_SRAM 6t_sram_schematic_simul...
Name
Vis
qb vs q
q vs qb
/Q
V (mV)
V (mV)
mouse L:
M:

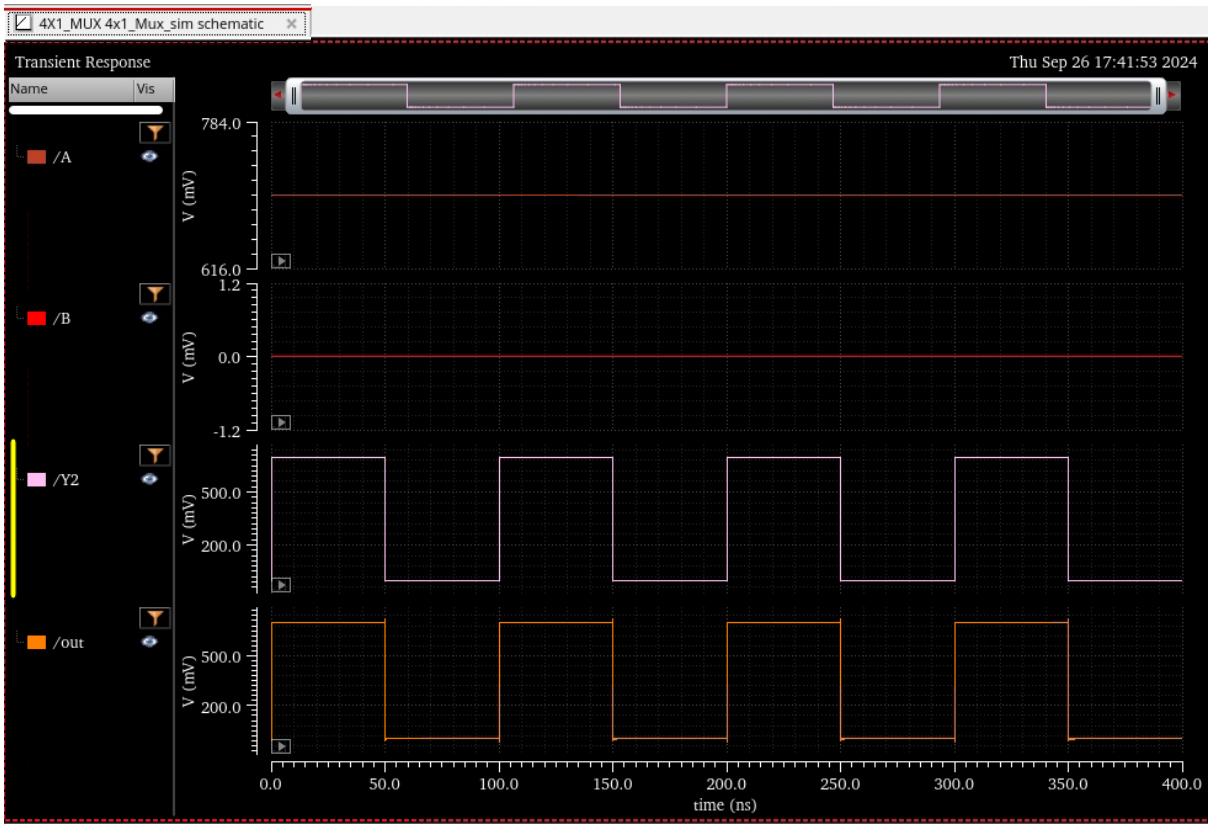
b)


6T_SRAM 6t_sram_schematic_simul...
Name
Vis
qb vs q
q vs qb
/Q
V (mV)
V (mV)

C)


6T_SRAM 6t_sram_schematic_simul...
Name
Vis
qb vs q
q vs qb
/Q
750.0
700.0
650.0
600.0
550.0
500.0
450.0
400.0
350.0
300.0
250.0
200.0
150.0
100.0
50.0
0.0
-50.0
V (mV)
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
550.0
600.0
650.0
700.0
V (mV)

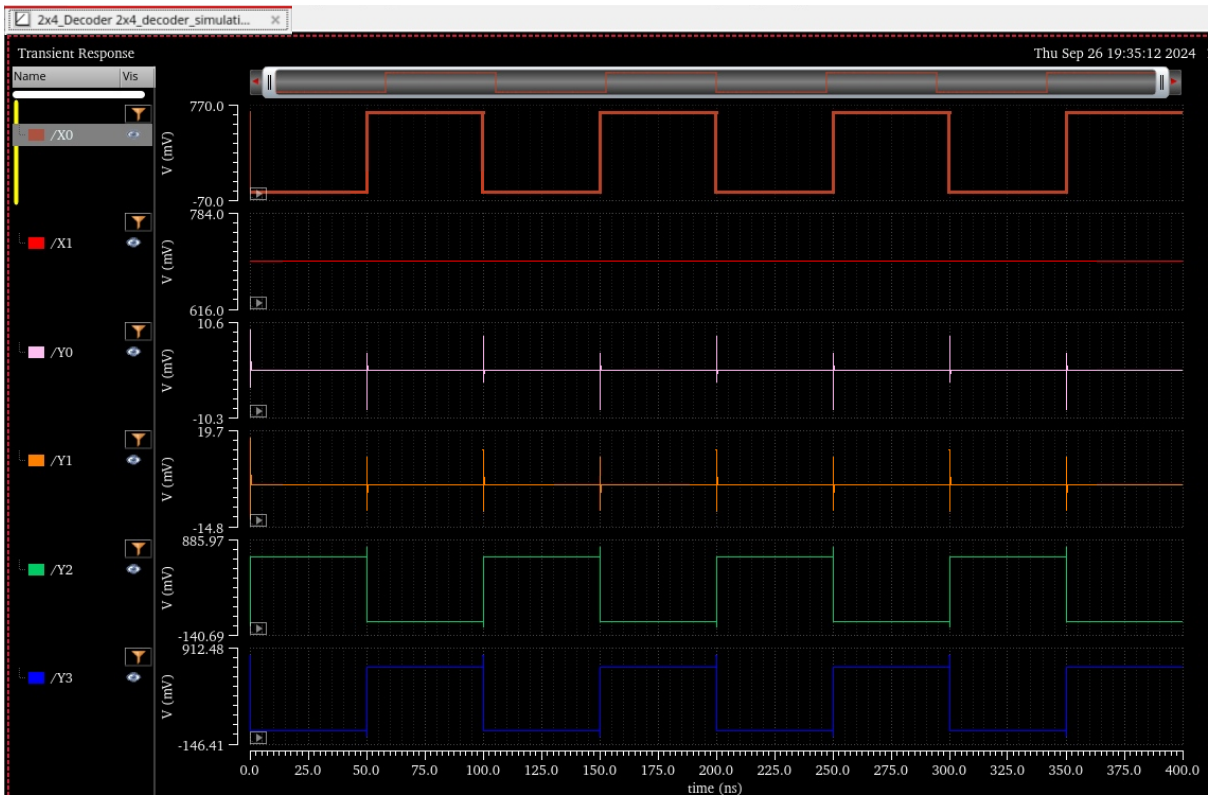
5) 4X1 MUX



Delay (edge1: rising and edge2: falling) : 52.11E-9

Delay (edge1: falling and edge2: rising) : -47.39E-9

6) 2x4 DECODER



Y3 and Y2 are the only outputs that changes with X0

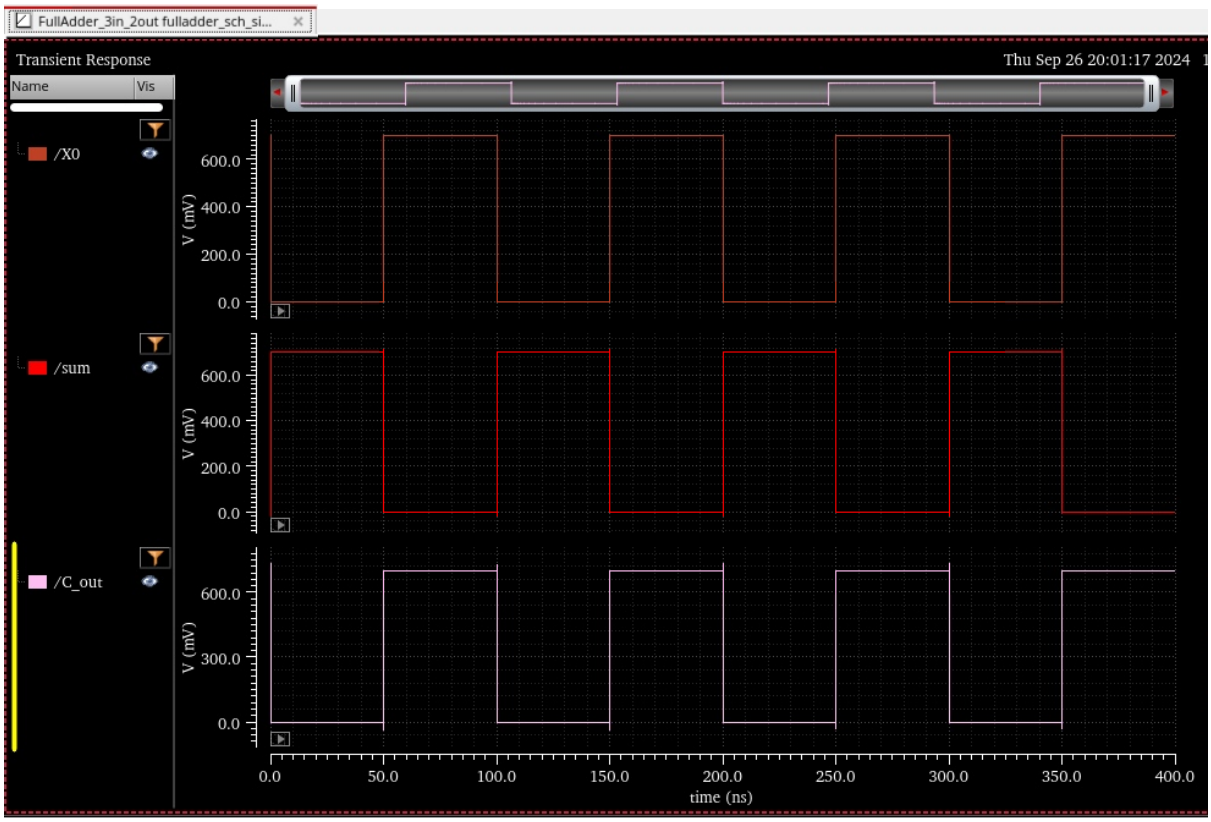
Delay for Y2: Edge type1 rising: 7.221E-12

: Edge type1 falling: 9.354E-12

Delay for Y3: Edge type1 rising: -50.8E-9

: Edge type1 falling: 50.15E-9

7) FULL ADDER



Delay for sum: Edge type1 rising: 27.68E-12

: Edge type1 falling: 21.76E-12

Delay for Co: Edge type1 rising: -49.86E-9

: Edge type1 falling: 51.22E-9