

NYU Tandon School of Engineering

Fall 2024, ECE 6473

Homework Assignment 4Instructor: Azeez Bhavnagarwala, email: ajb20@nyu.eduCourse Staff: Charan Chintha: cc8473@nyu.edu, Poojitha Vadinuri: pv2260@nyu.edu[released **Monday November 11th 2024**] [due* **Monday Nov 25th 2024, before 11:59 PM**]

You are *allowed* to discuss HW assignments only with other colleagues taking the class. You are *not allowed* to share your solutions with other colleagues in the class. Please feel free to reach out to the CA or to the instructor during office hours or by appointment if you need any help with the HW.

1. In this problem, the minimum sized (labeled as 1x in the picture) inverter has $L = 0.1\mu m$, $W_p = 2\mu m$, $W_n = 1\mu m$ and for this technology $R_{n, on} = 10k\Omega/\text{sq}$ (i.e. the resistance of an NMOS with width W and length L is equal to $10k\Omega(L/W)/\text{sq}$) and $R_{p, on} = 20k\Omega/\text{sq}$ (i.e. the resistance of a PMOS with width W and length L is equal to $20k\Omega(L/W)/\text{sq}$). Note that a 6x inverter has 6 times the width of a 1x inverter.

For the wire, $R_{\text{wire}} = 0.1\Omega/\text{sq}$. the parallel plate capacitance is $C_{pp} = 20aF/\mu m^2$ and the fringing capacitance per each side of wire is $C_{fr} = 14aF/\mu m$. The wire widths and lengths are shown in *Figure a*.

Using the π wire representation (Figure c) of the wires in shown in *Figure a*, as an equivalent RC switch model (figure b). What is the propagation delay from a step at V_{in} to V_a and V_b using Elmore models?

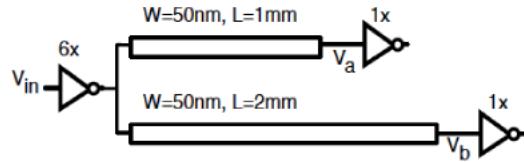


Figure a: Determine response of above wire-tree

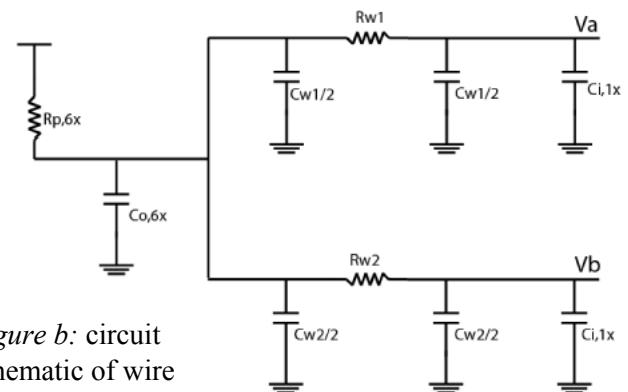


Figure b: circuit schematic of wire tree in Figure a using pi-model of wire

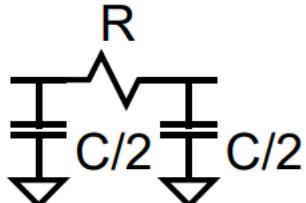
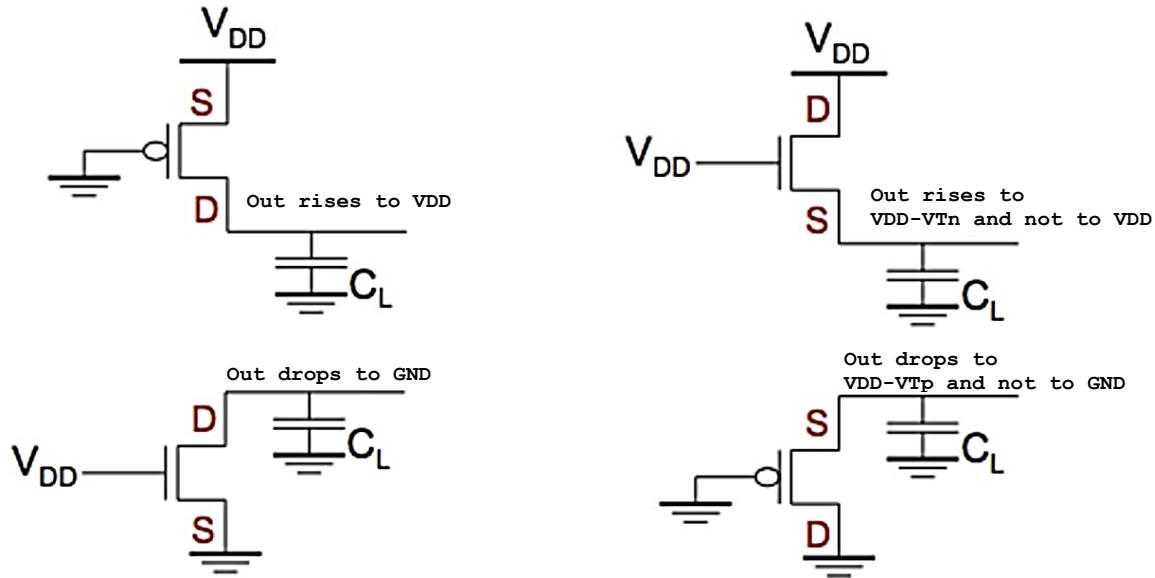
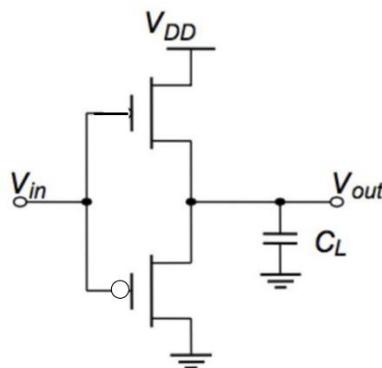


Figure c: Distributed wire approximated with a 'pi' model

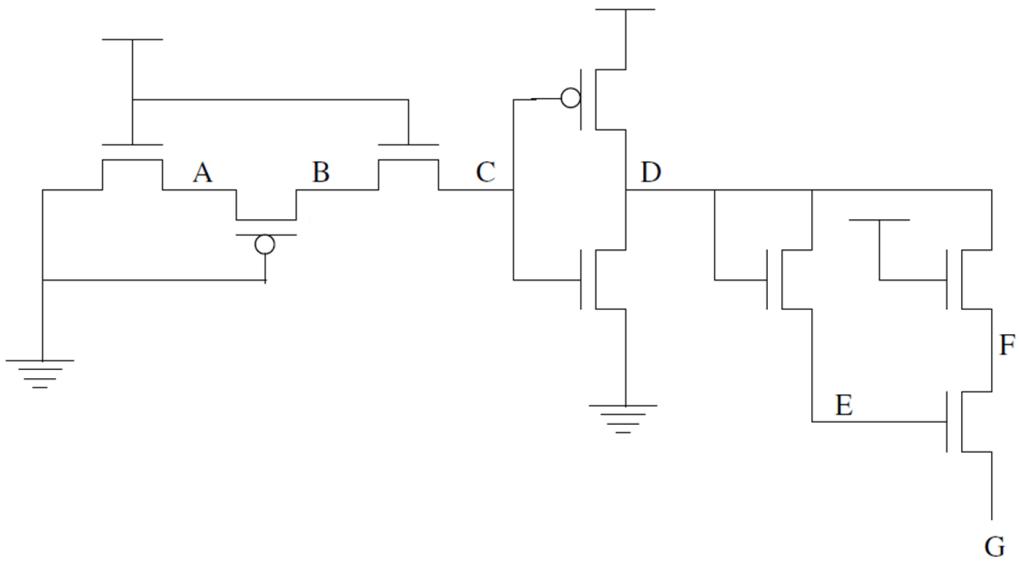
2. We observe that NFETs do not transmit a '1' very well and PFETs do not transmit a '0' very well because with $V_{GS} = V_{DD}$ and $V_{DS} = V_{DD}$ in an NFET, the Source terminal will charge up only until it reaches $V_{DD} - V_{Tn}$ because at higher voltages, the Gate-Source voltage difference is less than the Threshold Voltage V_{Tn} of the NFET causing it to 'turn-off' when the Source Terminal rises to within a V_{Tn} of V_{DD} .



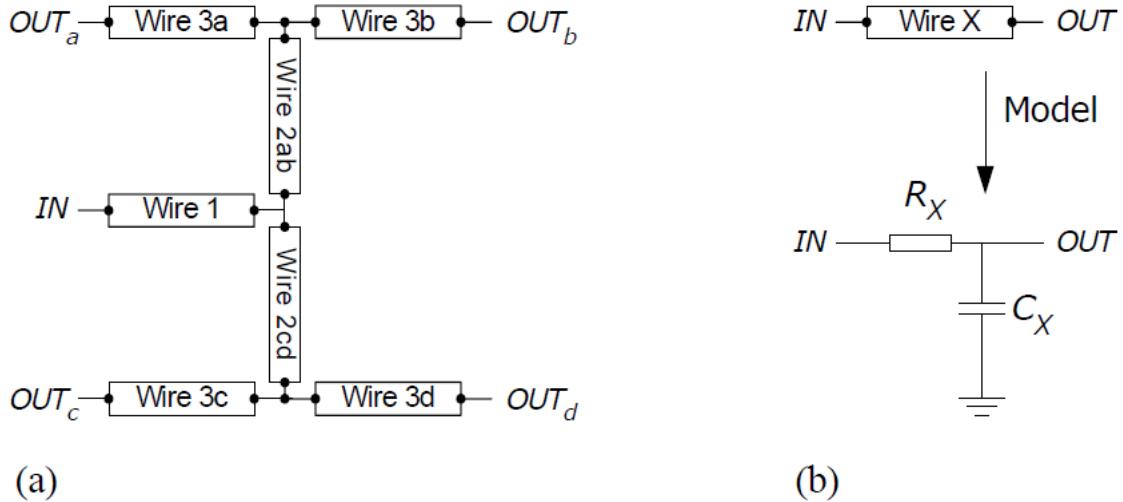
- (i) Sketch the output voltage characteristic if the PFET and the NFET positions were swapped as shown below?



- (ii) Write down the voltages at A, B, C, D, E, F, G in the following circuit, assuming that the initial voltage on each node is 2.5 volts. The relevant transistor parameters are, $V_{DD}=5V$, $V_{Tn} = 1V$ and $|V_{Tp}| = 0.7V$



- 3.** The figure (a) below shows a network consisting of 7 metal wires, where each wire has the length $L = 20 \text{ mm}$. Figure (b) introduces a simple model for each wire. The metal has the sheet resistance $R_{\square} = 0.07 \Omega$, the bottom plate capacitance $C_b = 0.04 \text{ fF}/\mu\text{m}^2$ and the fringe capacitance $C_f = 0.06 \text{ fF}/\mu\text{m}$ towards the substrate.



3a. Assume that each wire has a width of $W = 1.0 \mu\text{m}$. Use the lumped RC model and determine the propagation delay time at the outputs OUT_i . Assume an ideal step at the input IN .

3b. Use the Elmore delay equation to determine the propagation delay time for the whole network at the outputs OUT_i .

3c. The first wire feeds all other wires. The current is thus higher in the beginning wires compared to the wires at the end. A practiced method is to use wider wires in the beginning to reduce the current density. Therefore, it would be interesting to see how that affects the propagation delay.

Assume that Wire 1 has the width $W_1 = 4.0 \mu\text{m}$, Wire 2i has the width $W_2 = 2.0 \mu\text{m}$ and Wire 3i has the width $W_3 = 1.0 \mu\text{m}$. Use the Elmore delay equation to determine the propagation delay time for the whole network at the outputs OUTi.

- 4.1** Consider the static situation in the **Figure P4.1** where line-1 is at 1.5 V and line-2 is floating. What is the induced voltage on line-2 when Line-1 makes a $0 \rightarrow 1$ transition from GND to 1.5V and if Line-2 was initially at 0.5V (and floating)?
- 4.2** What is the induced voltage on line-2 when Line-1 makes a $0 \rightarrow 1$ transition from GND to 1.5V and if Line-2 was initially at 0.0V (and floating)?
- 4.3** What is the induced voltage on line-2 when Line-1 makes a $0 \rightarrow 1$ transition from GND to 1.5V and if Line-2 was initially at 1.5V (and floating)?

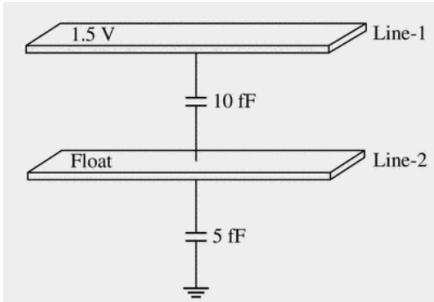


Figure P4.1

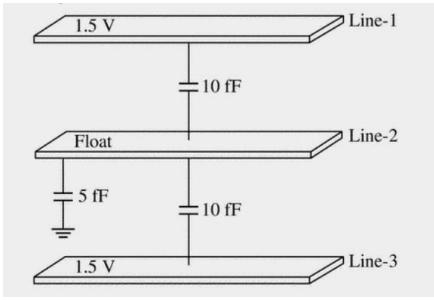


Figure P4.2

- 4.4** Consider the static situation in the **Figure P2.2** where line-1 is at 1.5 V, line-2 is floating and line-3 is at 1.5V. What is the induced voltage on line-2 when Line-1 makes a $0 \rightarrow 1$ transition from GND to 1.5V and if Line-2 was initially at 0.5V (and floating)?

$$1. R_{Wire} = k_{sheet} \cdot \frac{L}{W}$$

$$\underline{V_a, L=1\text{mm}} \\ R_{u,1} = 0.1 \cdot \frac{1000}{0.05} = 2000 \text{ m}$$

$$\underline{V_b, L=2\text{mm}} \\ R_{u,2} = 0.1 \cdot \frac{2000}{0.05} = 4000 \text{ m}$$

$$C_{Wire} = C_{pp} \cdot W \cdot L + C_f \cdot 2L$$

$$\underline{V_A : C_{u,1} = (20 \cdot 0.05 \cdot 1000) + (14 \cdot 2 \cdot 1000) = 1000 + 28000 = 29 \text{ FF}}$$

$$\underline{V_B : C_{u,2} = (20 \cdot 0.05 \cdot 2000) + (14 \cdot 2 \cdot 2000) = 2000 + 56000 = 58 \text{ FF}}$$

$$R_{n,in,1x} = 10 \text{ m} ; R_{p,in,1x} = 20 \text{ m}$$

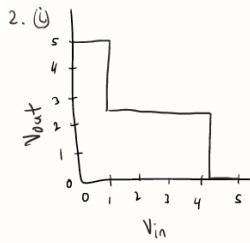
$$R_{n,in,6x} = \frac{10 \text{ m}}{6} = 1667 \text{ m} ; R_{p,in,6x} = \frac{20 \text{ m}}{6} = 3333 \text{ m}$$

$$C_{downstream,a} = C_{u,1} \cdot C_{ix} = 29 + 16 = 45 \text{ FF}$$

$$\begin{aligned} T_a &= (R_{p,6x} \cdot C_{downstream,a}) + (R_{u,1} \cdot C_{ix}) \\ &= (3333 \text{ m} \cdot 45 \text{ FF}) + (2000 \text{ m} \cdot 16 \text{ FF}) = \boxed{181.985 \text{ ps}} \end{aligned}$$

$$C_{downstream,b} = C_{u,2} \cdot C_{ix} = 58 + 16 = 74 \text{ FF}$$

$$\begin{aligned} T_b &= (R_{p,6x} \cdot C_{downstream,b}) + (R_{u,2} \cdot C_{ix}) \\ &= (3333 \text{ m} \cdot 74 \text{ FF}) + (4000 \text{ m} \cdot 16 \text{ FF}) = \boxed{310.642 \text{ ps}} \end{aligned}$$



(ii) Node A:

PMOS is on, pulls A to GND $\rightarrow 0\text{ V}$

Node B:

NMOS D is off, stays at initial voltage $\rightarrow 2.5\text{ V}$

Node C:

NMOS is off, stays at initial voltage $\rightarrow 2.5\text{ V}$

Node D:

PMOS is on, pulls node up to $V_{DD} \rightarrow 5\text{ V}$

Node E:

PMOS is off, stays at initial voltage $\rightarrow 2.5\text{ V}$

Node F:

NMOS is on, pulls node to GND $\rightarrow 0\text{ V}$

Node G:

PMOS is off, remains at initial voltage $\rightarrow 2.5\text{ V}$

$$3.8) R_{\text{wire}} = R \cdot \frac{L}{W}$$

$$= 0.07 \Omega \cdot \frac{20,000 \mu\text{m}}{1.0 \mu\text{m}} = \boxed{1400 \Omega}$$

$$C_{\text{wire}} = C_b \cdot W \cdot L + C_f \cdot L$$

$$= 0.04 \text{ pF}/\mu\text{m}^2 \cdot 1.0 \mu\text{m} \cdot 20,000 \mu\text{m} + 0.06 \text{ pF}/\mu\text{m} \cdot 20,000 \mu\text{m}$$

$$= 800 \text{ pF} + 1200 \text{ pF} = \boxed{2000 \text{ pF}}$$

$$T_{\text{wire}} = R_{\text{wire}} \cdot C_{\text{wire}}$$

$$= 1400 \Omega \cdot 2 \text{ pF} = \boxed{2.8 \text{ ns} = T_{\text{outA}};}$$

(b) $T_{\text{outA}} = (R_1 \cdot C_1) + (R_{2a} \cdot C_{2ab}) + (R_{3a} \cdot C_{3a})$

$$= (1400 \Omega \cdot 4 \text{ pF}) + (1400 \Omega \cdot 4 \text{ pF}) + (1400 \Omega \cdot 2 \text{ pF})$$

$$= \boxed{19.2 \text{ ns} = T_{\text{outB}} = T_{\text{outC}} - T_{\text{outA}}}$$

(c) Wire 1 ($W_1 = 4 \mu\text{m}, L = 20,000 \mu\text{m}$)

$$R = 0.07/4 = 0.0175 \Omega/\mu\text{m}$$

$$R_1 = 0.0175 \cdot 20,000 = 350 \Omega$$

$$C_{\text{per unit length}} = (C_b \cdot W) + C_f = (0.04 \cdot 4.0) + 0.06 = 0.22 \text{ pF}/\mu\text{m}$$

$$C_1 = 0.22 \cdot 20,000 = 4400 \text{ pF} = 4.4 \text{ nF}$$

Wire 2 ($W_2 = 2 \mu\text{m}, L = 20,000 \mu\text{m}$)

$$R = 0.07/2.0 = 0.035 \Omega/\mu\text{m}$$

$$R_2 = 0.035 \cdot 20,000 = 700 \Omega$$

$$C = (0.04 \cdot 2) + 0.06 = 0.14 \text{ pF}/\mu\text{m}$$

$$C_2 = 0.14 \cdot 20,000 = 2800 \text{ pF} = 2.8 \text{ nF}$$

Wire 3 ($W_3 = 1.0 \mu\text{m}$)

$$R = 0.07/1.0 = 0.07 \Omega/\mu\text{m}$$

$$R_3 = 0.07 \cdot 20,000 = 1400 \Omega$$

$$C = (0.04 \cdot 1.0) + 0.06 = 0.1 \text{ pF}/\mu\text{m}$$

$$C_3 = 0.1 \cdot 20,000 = 2000 \text{ pF} = 2.0 \text{ nF}$$

Out:

$$\text{Wire 1: } R_1(C_1 + C_2) = 350 \cdot (4.4 + 2.8 + 2) = 3.2 \text{ ns}$$

$$\text{Wire 2: } R_2(C_2 + C_3) = 700 \cdot (2.8 + 2.0) = 3.36 \text{ ns}$$

$$\text{Wire 3: } R_3 \cdot C_3 = 1400 \cdot 2.0 = 2.8 \text{ ns}$$

$$T_{\text{out}} = 3.2 \text{ ns} + 3.36 \text{ ns} + 2.8 \text{ ns} = \boxed{9.38 \text{ ns}}$$

$$4.1 \quad W1 = 4.0 \mu\text{m}, W2 = 2.0 \mu\text{m}, W3 = 1.0 \mu\text{m}$$

$$4.1 \quad K = \frac{C_{12}}{C_{12} + C_{23}} = \frac{10 \text{ fF}}{10 \text{ fF} + 5 \text{ fF}} = \frac{10}{15} = 0.6667$$

$$V_{induced} = K \cdot V_{transition} = 0.6667 \cdot 1.0 \text{ V} = 1.0 \text{ V}$$

$$V_{final} = V_{initial} + V_{induced} = 0.5 \text{ V} + 1.0 \text{ V} = \boxed{1.5 \text{ V}}$$

$$4.2 \quad V_{induced} = K \cdot V_{transition} = 0.6667 \cdot 1.0 \text{ V} = 1.0 \text{ V}$$

$$V_{final} = V_{initial} + V_{induced} = 0.0 \text{ V} + 1.0 \text{ V} = \boxed{1.0 \text{ V}}$$

$$4.3 \quad V_{induced} = K \cdot V_{transition} = 0.6667 \cdot 1.5 \text{ V} = 1.0 \text{ V}$$

$$V_{final} = V_{initial} + V_{induced} = 1.5 \text{ V} + 1.0 \text{ V} = \boxed{2.5 \text{ V}}$$

$$4.4 \quad C_{total} = C_{12} + C_{23} + C_{26} = 10 \text{ fF} + 10 \text{ fF} + 5 \text{ fF} = 25 \text{ fF}$$

$$V_{induced, L1} = \frac{C_{12}}{C_{total}} \cdot V_{transition} = \frac{10 \text{ fF}}{25 \text{ fF}} \cdot 1.5 \text{ V} = 0.6 \text{ V}$$

$$V_{final} = V_{initial} + V_{induced} = 0.5 \text{ V} + 0.6 \text{ V} = \boxed{1.1 \text{ V}}$$