

Q.1

Q.1)

$$\begin{aligned} \text{a) Final load} &= 500 \times C_{in} \\ \text{Total fan out} &= 500 \times C_{in} / C_{in} \\ &= 500 \end{aligned}$$

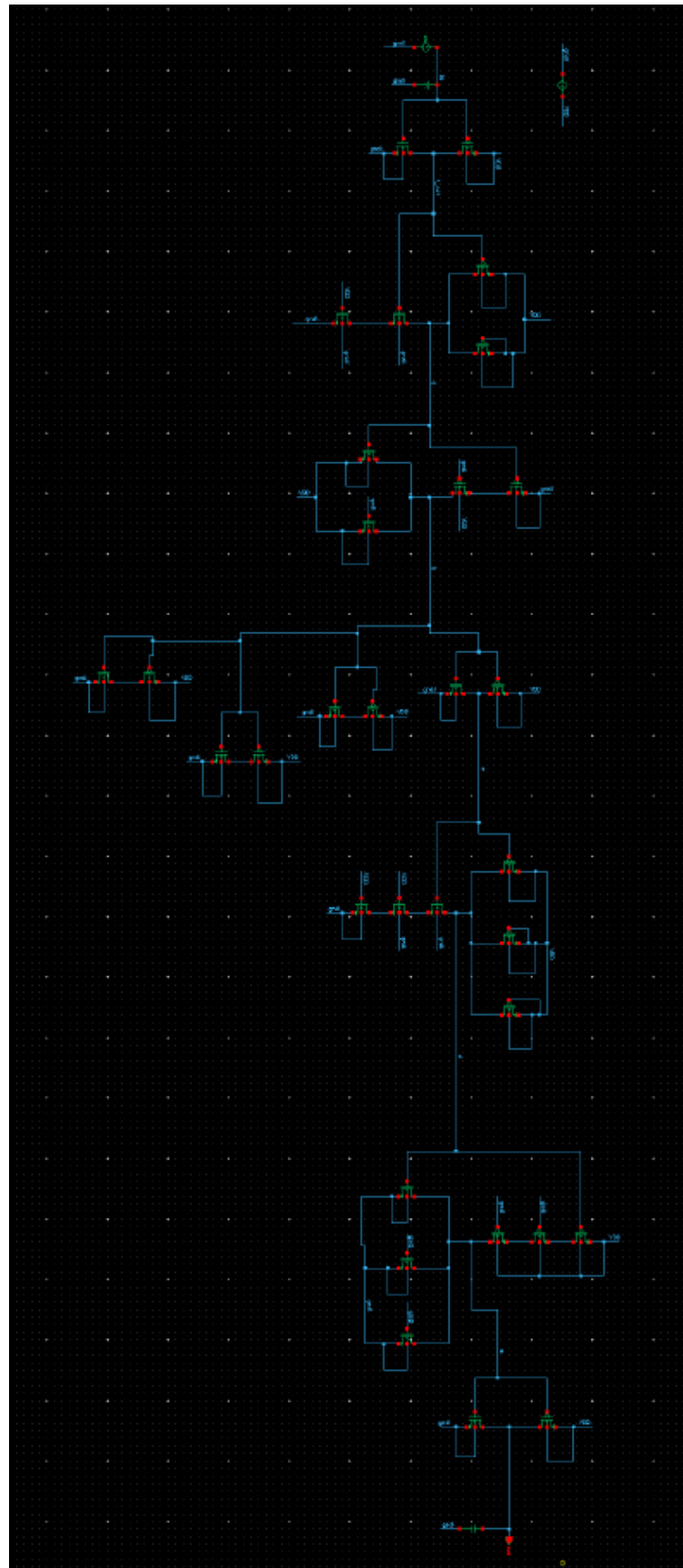
$$\text{Min total delay } f = 500^{(1/5)}$$

$$f = 500^{(1/5)} = 2.43$$

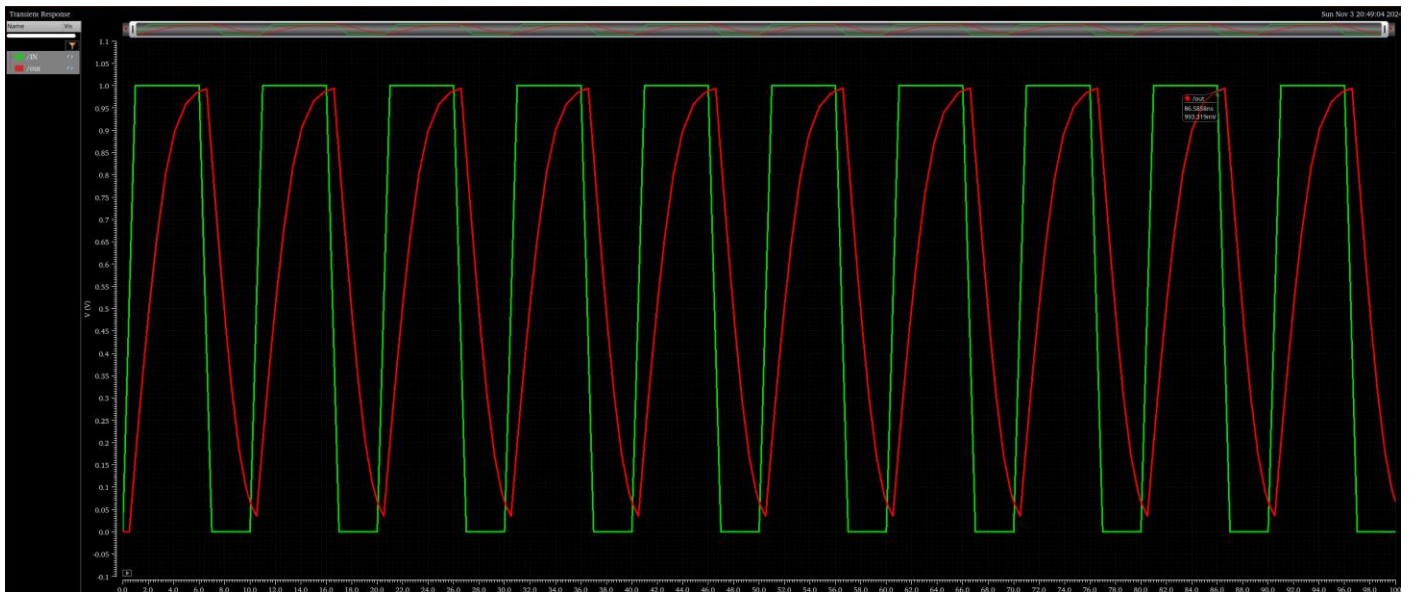
$$\begin{aligned} \text{b) } f \text{ stage has input capacitance} \\ \text{of } 500 \times 2 \text{ fms} / 2.43 &= 411.52 \\ &= 412. \end{aligned}$$

Since it's an inverter
206 fms for NFET & PFET.

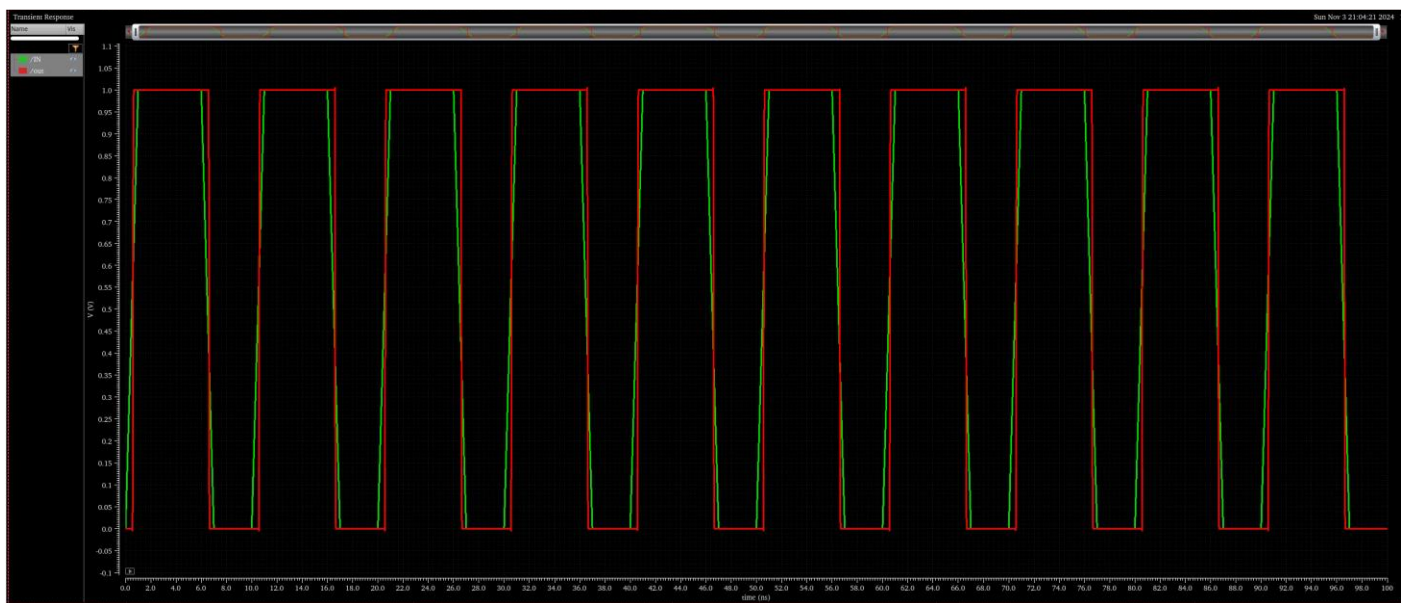
$$\begin{aligned} \text{Stage e} &: P=3N, P+N (P=128; N=43) \\ \text{Stage d} &: P=17.5, N=54 \\ \text{Stage c} &: P=N=15 \\ \text{Stage b} &: P=34, N=16.66=17 \\ \text{Stage a} &: P=7, N=14 \\ \text{Stage 1} &: P=N=5 \end{aligned}$$



c)



Input to output : $1.578\text{E-}9$

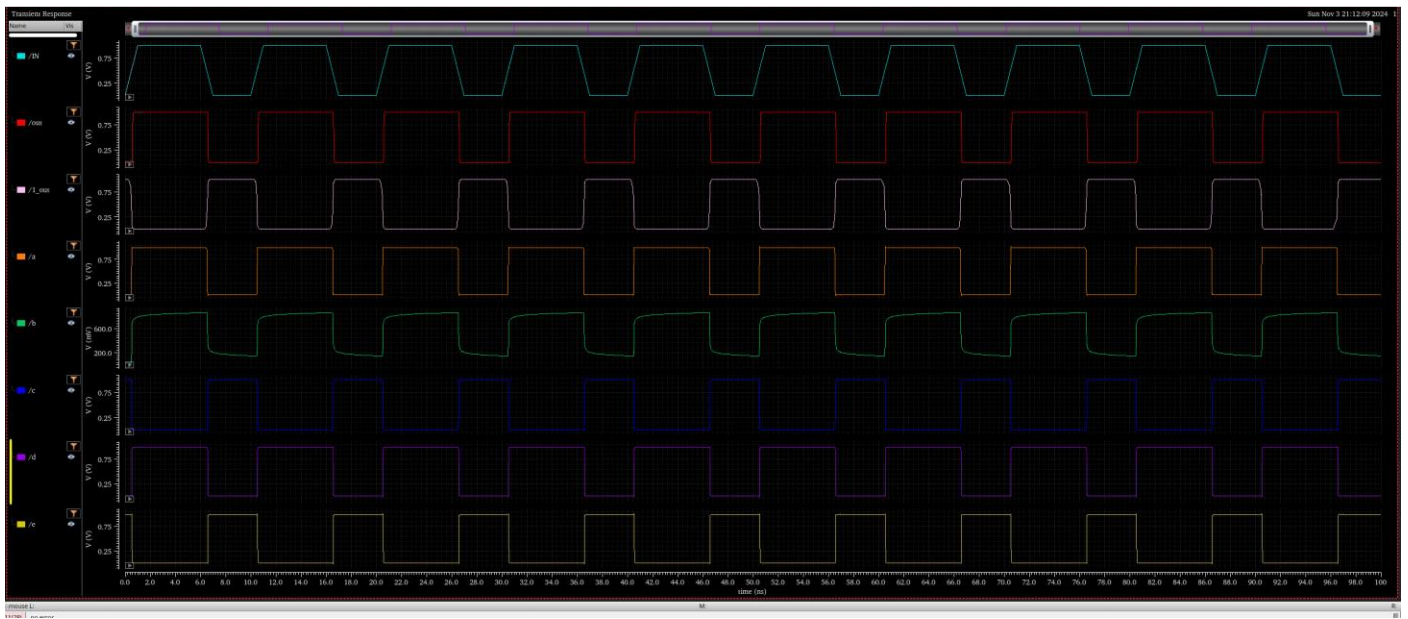


One with sizing: $88.18\text{E-}12$

So it takes lesser time

d)

every stage



Input to output = $88.18\text{E-}12$

1 to output = $80.75\text{E-}12$

A to output = $68.33\text{E-}12$

B to output = $54.68\text{E-}12$

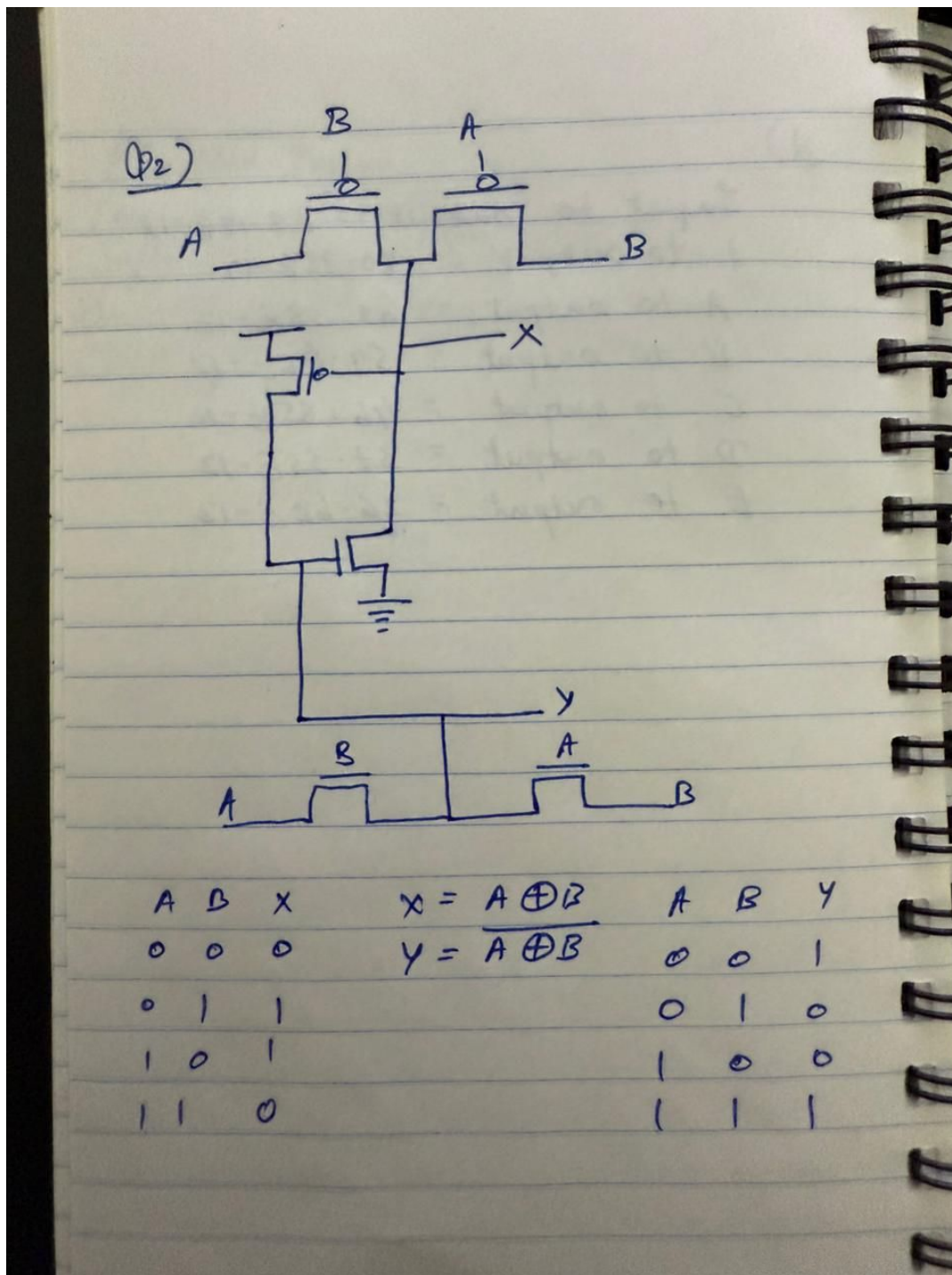
C to output = $46.85\text{E-}12$

D to output = $37.35\text{E-}12$

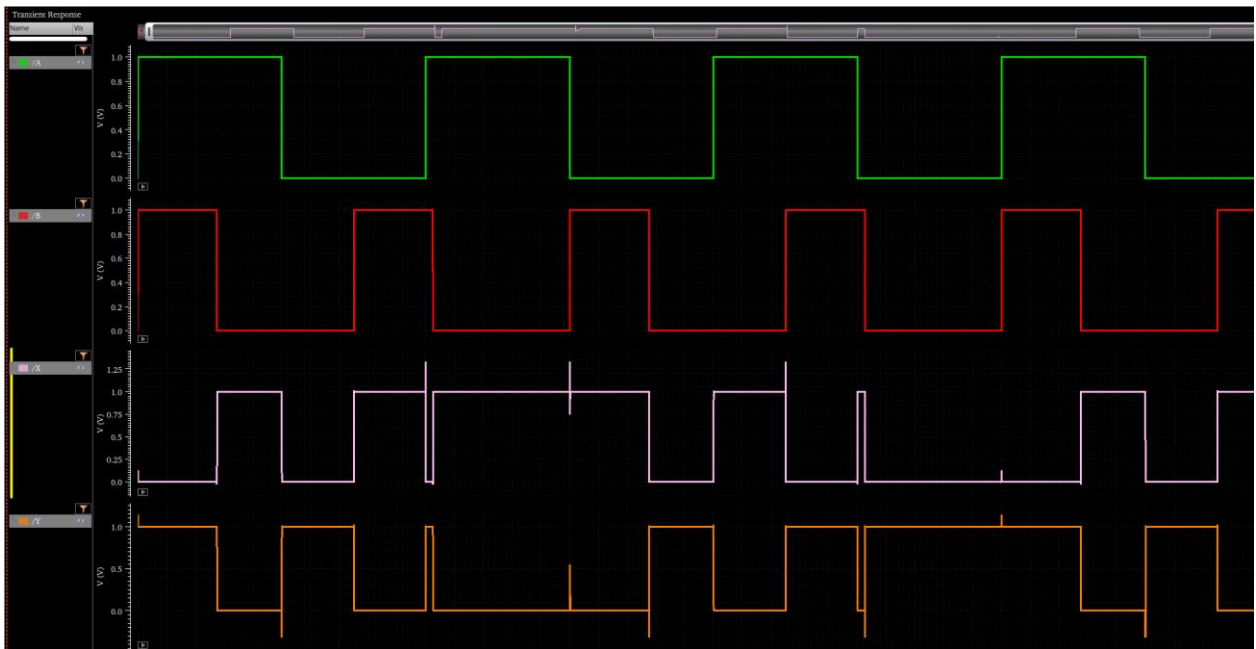
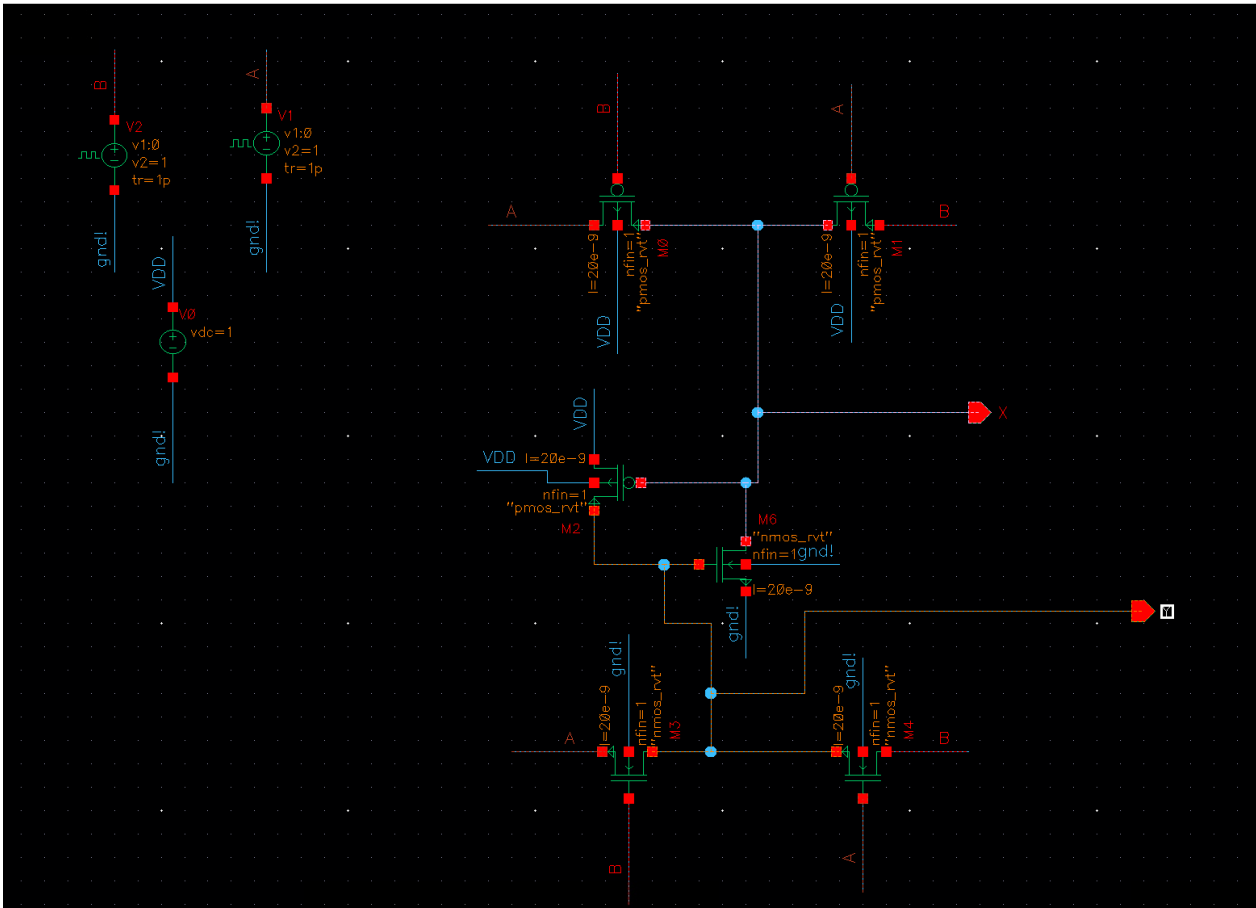
E to output = $26.62\text{E-}12$

Q2

A)



B)



Delay:

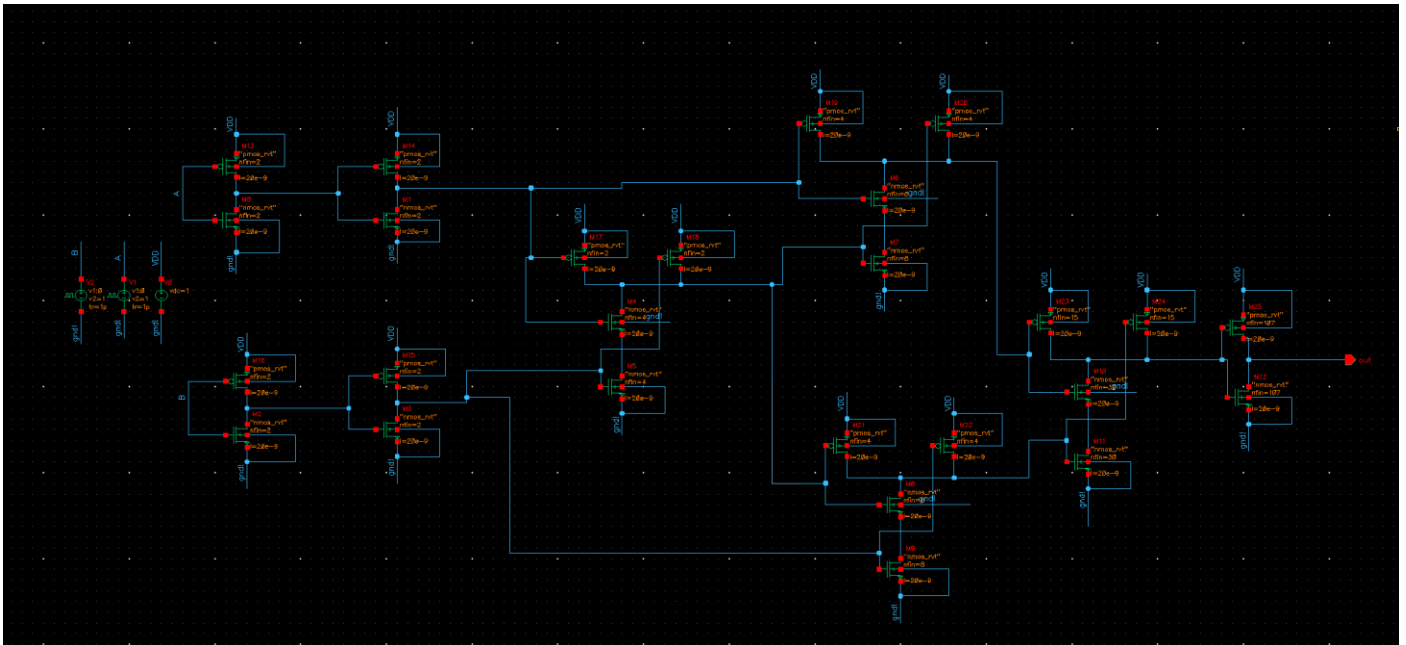
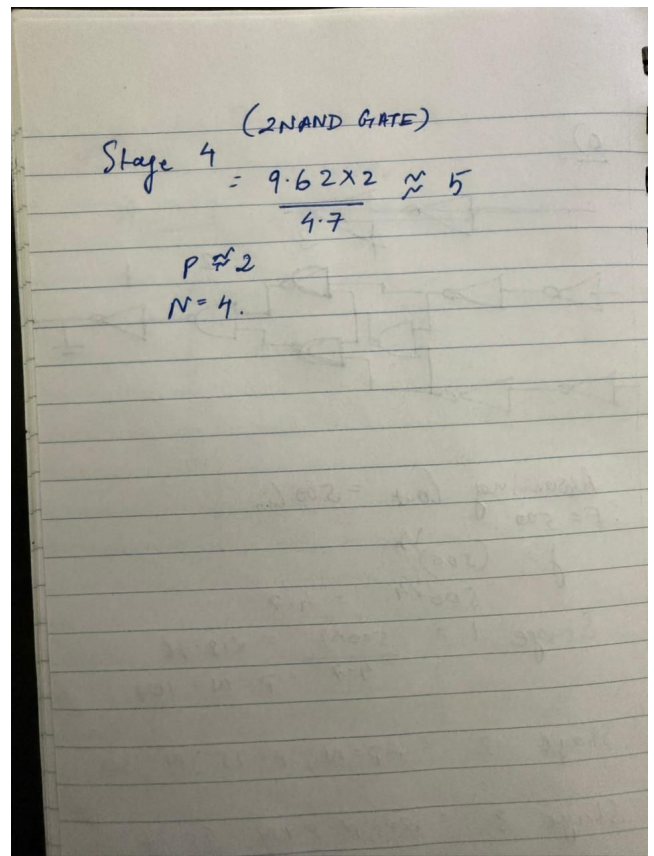
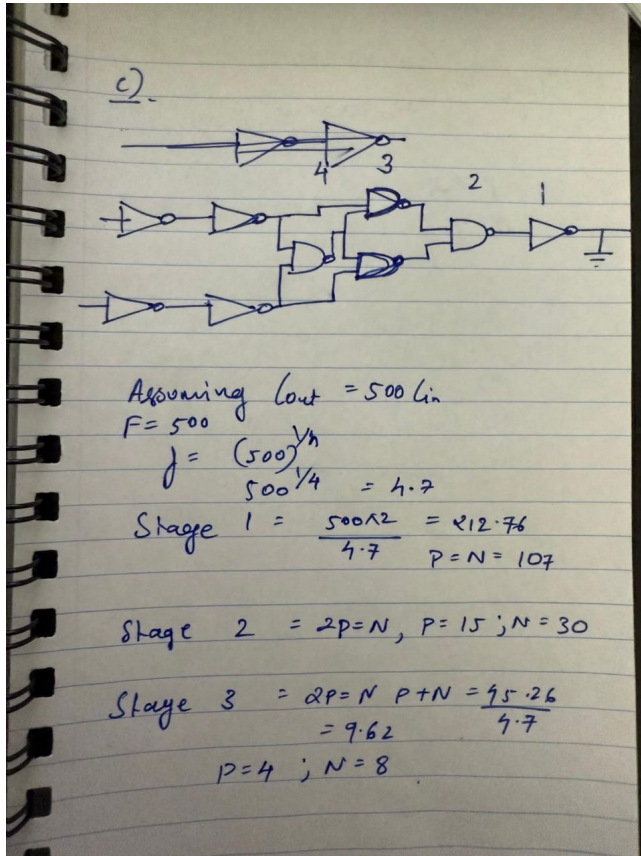
A to X: $12.5\text{E-}9$

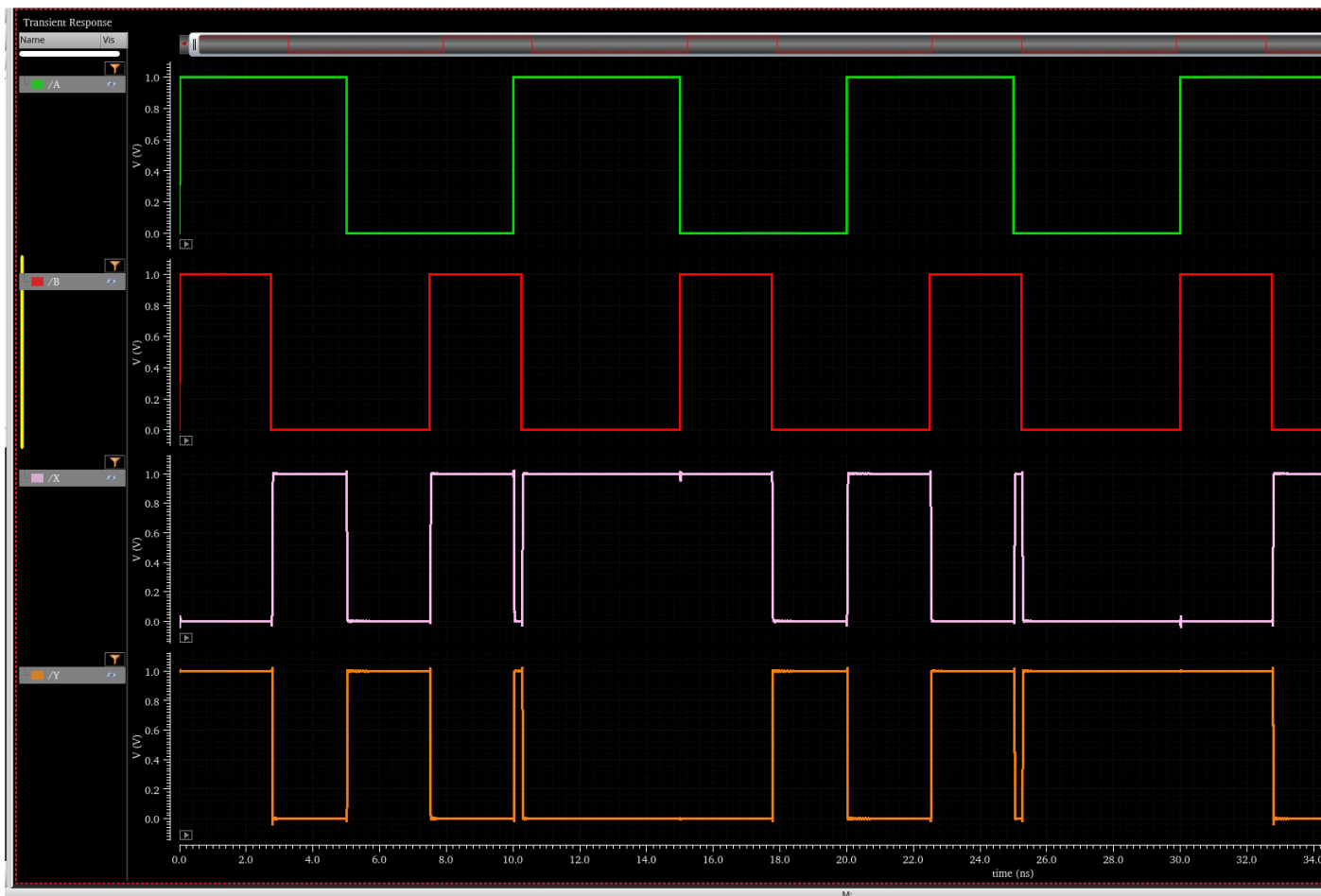
B to X: $2.533\text{E-}12$

A to Y: $5.0\text{E-}9$

B to Y: $2.503\text{E-}9$

C)





A to X: $22.28\text{E-}12$

B to X: $34.67\text{E-}12$

A to Y: $24.24\text{E-}12$

B to Y: $35.52\text{E-}12$