

Take Home Assignment 2

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1) LUT UTILISATION REPORT

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```
| Tool Version : Vivado v.2019.2 (win64) Build 2708876 Wed Nov 6 21:40:23 MST 2019
| Date       : Tue Feb 18 14:21:32 2025
| Host       : DESKTOP-Q29BN3N running 64-bit major release (build 9200)
| Command    : report_utilization -file {D:/IIT GANDHINAGAR/Semester 4/ES204 - Digital
|               Systems/a/utilization_report.txt} -name utilization_1
| Design     : a
| Device     : 7a35tcp236-1
| Design State : Routed
```

Utilization Design Information

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1. Slice Logic

Site Type	Used	Fixed	Available	Util%

Slice LUTs	7	0	20800	0.03
LUT as Logic	7	0	20800	0.03
LUT as Memory	0	0	9600	0.00
Slice Registers	4	0	41600	<0.01
Register as Flip Flop	4	0	41600	<0.01
Register as Latch	0	0	41600	0.00
F7 Muxes	0	0	16300	0.00
F8 Muxes	0	0	8150	0.00

1.1 Summary of Registers by Type

Total	Clock	Enable	Synchronous	Asynchronous
0	-	-	-	-
0	-	-	Set	
0	-	-	Reset	
0	-	Set	-	
0	-	Reset	-	
0	Yes	-	-	
0	Yes	-	Set	
0	Yes	-	Reset	
0	Yes	Set	-	
4	Yes	Reset	-	

2. Slice Logic Distribution

Site Type	Used	Fixed	Available	Util%
Slice	2	0	8150	0.02
SLICEL	2	0		
SLICEM	0	0		
LUT as Logic	7	0	20800	0.03
using O5 output only	0			
using O6 output only	6			
using O5 and O6	1			
LUT as Memory	0	0	9600	0.00

LUT as Distributed RAM	0	0		
LUT as Shift Register	0	0		
Slice Registers	4	0	41600	<0.01
Register driven from within the Slice	4			
Register driven from outside the Slice	0			
Unique Control Sets	1		8150	0.01

* Note: Available Control Sets calculated as Slice Registers / 8, Review the Control Sets Report for more information regarding control sets.

3. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

4. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	90	0.00

5. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	23	23	106	21.70
IOB Master Pads	10			

IOB Slave Pads	12				
Bonded IPADs	0	0	10	0.00	
Bonded OPADs	0	0	4	0.00	
PHY_CONTROL	0	0	5	0.00	
PHASER_REF	0	0	5	0.00	
OUT_FIFO	0	0	20	0.00	
IN_FIFO	0	0	20	0.00	
IDELAYCTRL	0	0	5	0.00	
IBUFDS	0	0	104	0.00	
GTPE2_CHANNEL	0	0	2	0.00	
PHASER_OUT/PHASER_OUT_PHY	0	0	20	0.00	
PHASER_IN/PHASER_IN_PHY	0	0	20	0.00	
IDELAYE2/IDELAYE2_FINEDELAY	0	0	250	0.00	
IBUFDS_GTE2	0	0	2	0.00	
ILOGIC	0	0	106	0.00	
OLOGIC	0	0	106	0.00	

6. Clocking

Site Type	Used	Fixed	Available	Util%	
BUFGCTRL	1	0	32	3.13	
BUFIO	0	0	20	0.00	
MMCME2_ADV	0	0	5	0.00	
PLLE2_ADV	0	0	5	0.00	
BUFMRCE	0	0	10	0.00	
BUFHCE	0	0	72	0.00	
BUFR	0	0	20	0.00	

7. Specific Feature

Site Type	Used	Fixed	Available	Util%	
BSCANE2	0	0	4	0.00	
CAPTUREE2	0	0	1	0.00	
DNA_PORT	0	0	1	0.00	

EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
PCIE_2_1	0	0	1	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

8. Primitives

Ref Name	Used	Functional Category
OBUF	12	IO
IBUF	11	IO
LUT5	5	LUT
FDRE	4	Flop & Latch
LUT6	2	LUT
LUT4	1	LUT
BUFG	1	Clock

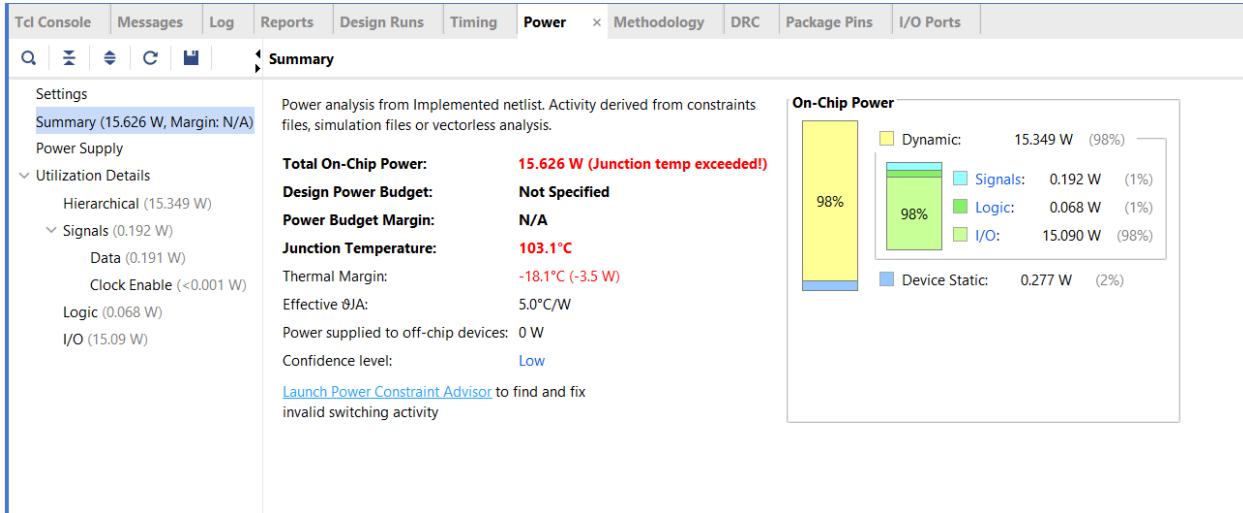
9. Black Boxes

Ref Name	Used

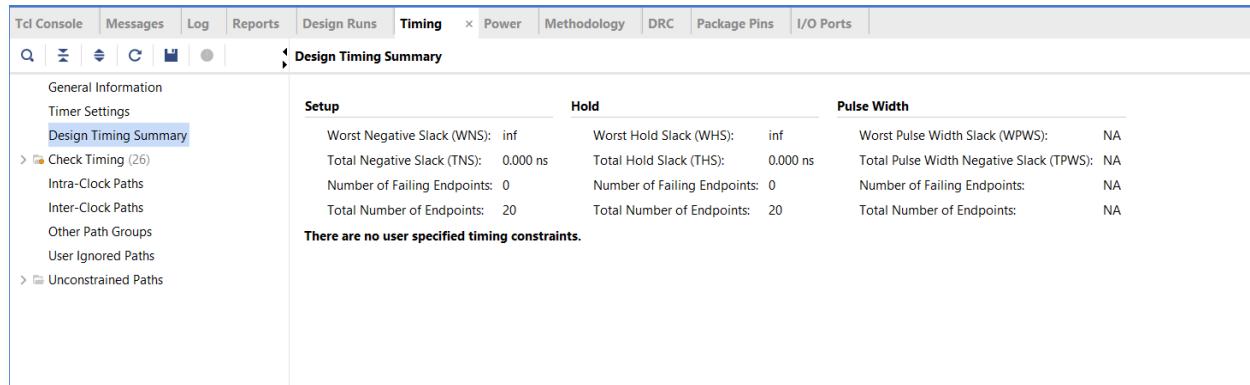
10. Instantiated Netlists

Ref Name	Used

2) Power Report



3) Timing Analysis



Design Source

```
module a(clk,mode,Load,X,Y,out,out_x,out_y);
input clk;
input mode,Load;
input [3:0]X,Y;
output reg [3:0]out,out_x,out_y;
always@(*)
begin
    out_x <= X;
    out_y <= Y;
end
always@(posedge clk)
begin
    if(!mode && Load)
    begin
        out <= X;
    end

    else if(!mode && !Load && (out == Y))
    begin
        out <= out ;
    end
    else if(!mode && !Load)
    begin
        out <= out + 1;
    end
    else if(mode && Load)
    begin
        out <= Y;
    end
    else if(mode && !Load)
    begin
        out <= out - 1;
    end
end
endmodule
```

```

        else if(mode && Load)
        begin
            out <= Y;
        end
        else if(mode && !Load)
        begin
            out <= out - 1;
        end
        else if (mode && !Load && (out == X) )
        begin
            out <= out;
        end
        else
        begin
            out <= 4'bX;
        end
    end
endmodule

```

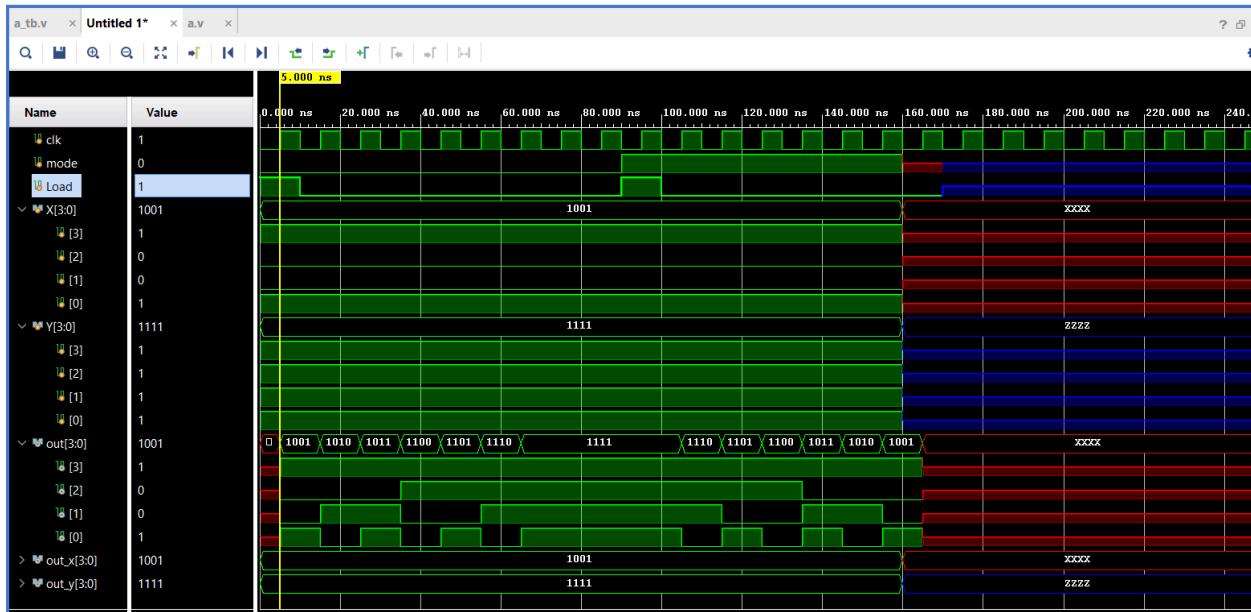
4) Testbench

```

module a_tb();
reg clk;
reg mode,Load;
reg [3:0]X,Y;
wire [3:0]out,out_x,out_y;
a uut(.clk(clk),.mode(mode),.Load(Load),.X(X),.Y(Y),.out(out),.out_x(out_x),.out_y(out_y));
initial begin
    clk = 0;
    forever #5 clk = ~clk;
end
initial begin
    X = 4'b1001; Y = 4'b1111;
    mode = 0; Load = 1; #10;
    mode = 0; Load = 0; #80;
    mode = 1; Load = 1; #10;
    mode = 1; Load = 0; #60;
    X = 4'bX; Y = 4'bZ;
    mode = 1'bX; Load = 0;#10;
    mode = 1'bZ; Load = 1'bZ;#10;
end
endmodule

```

5) Simulation waveform

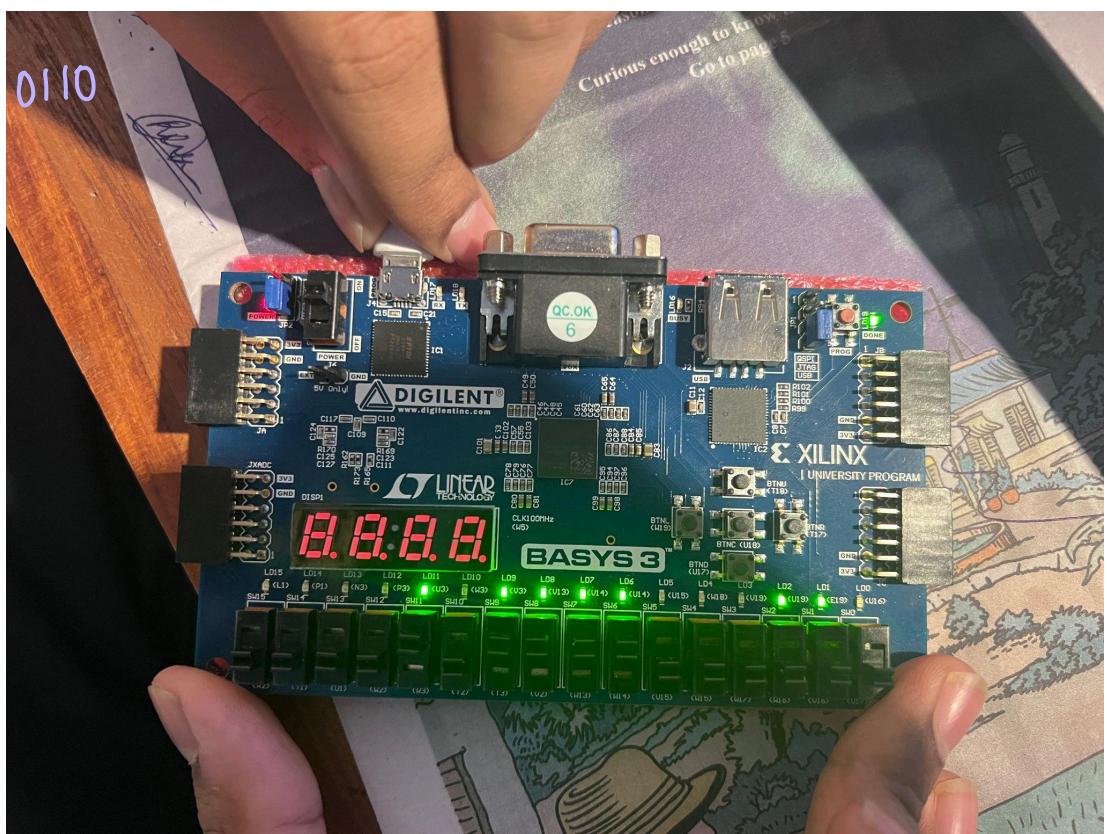
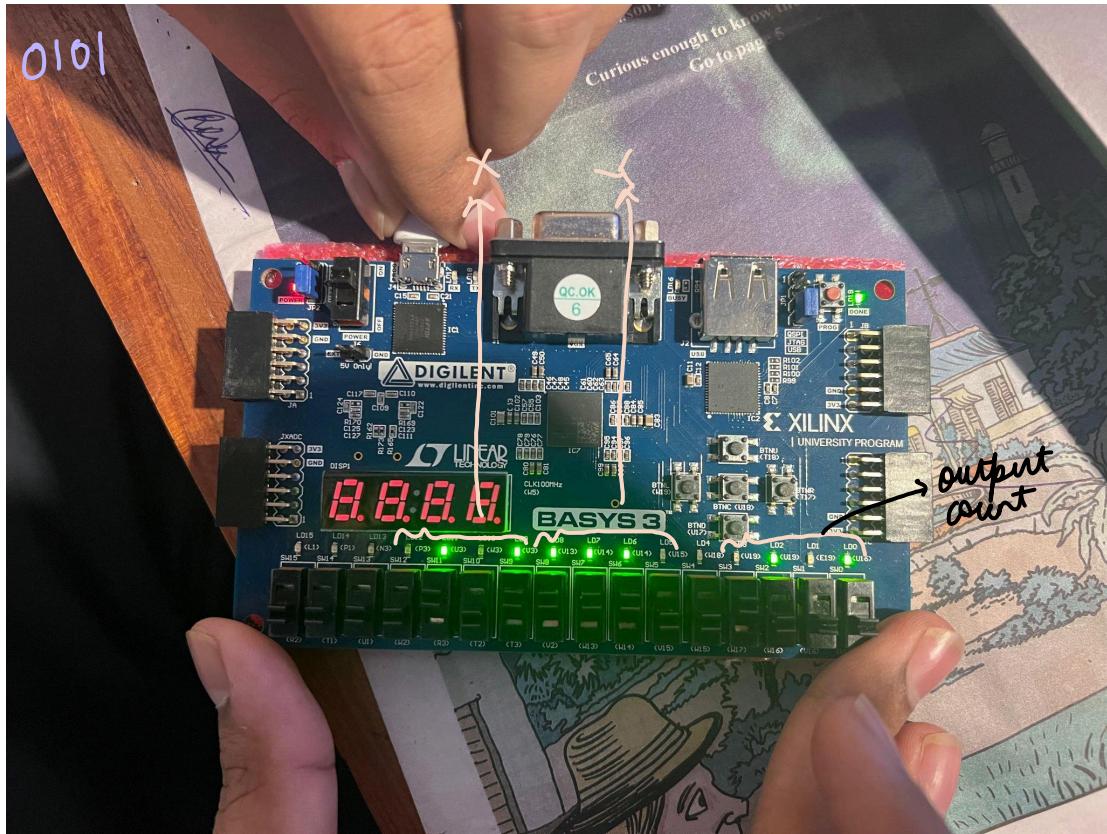


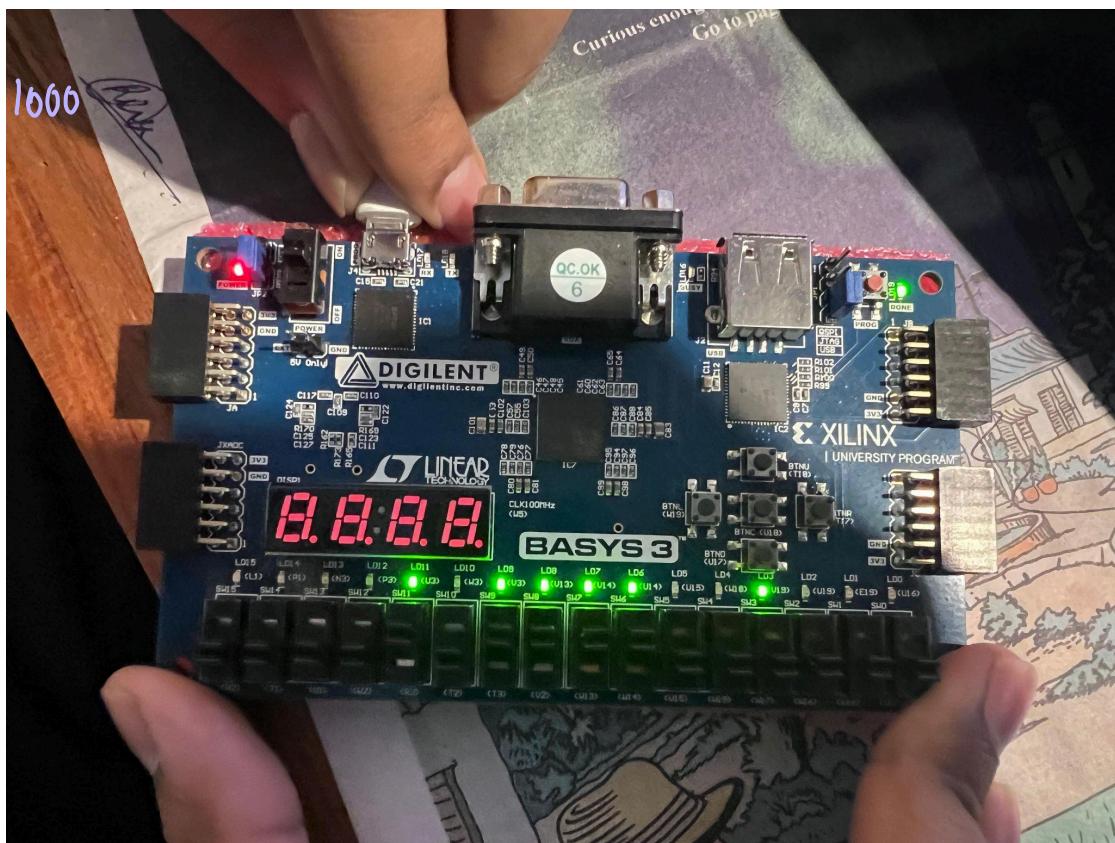
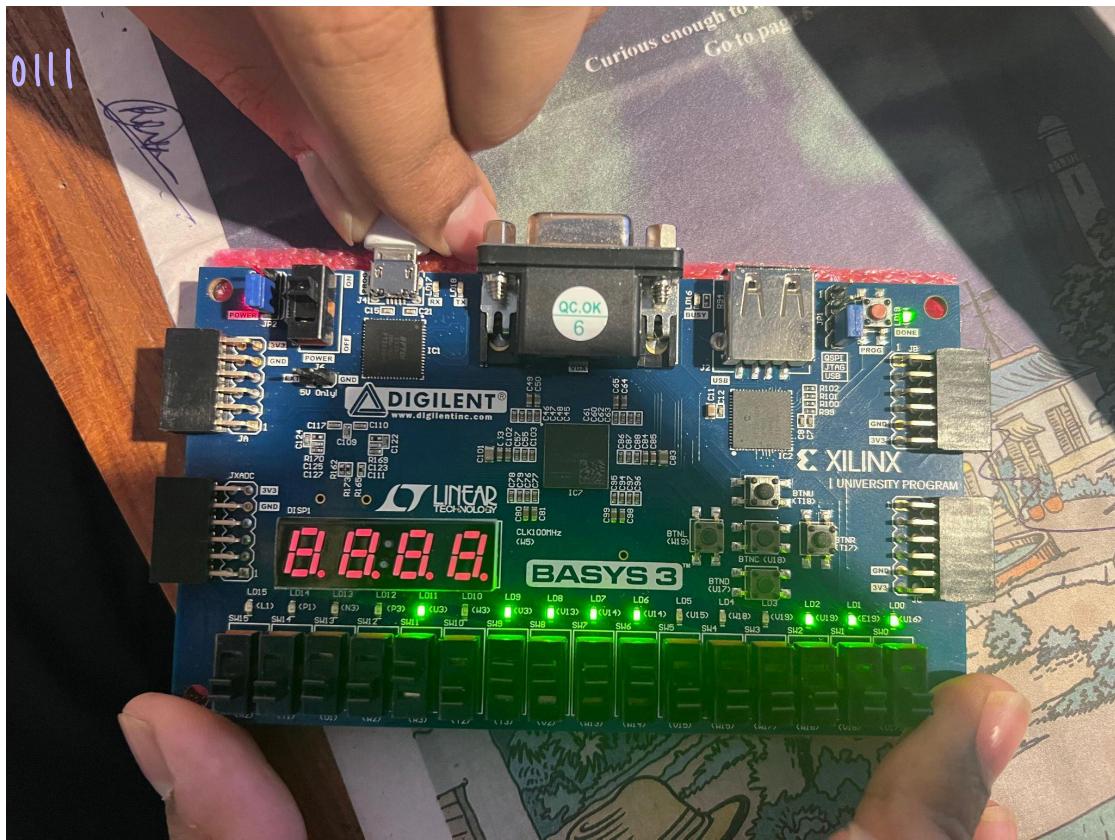
6) Ports

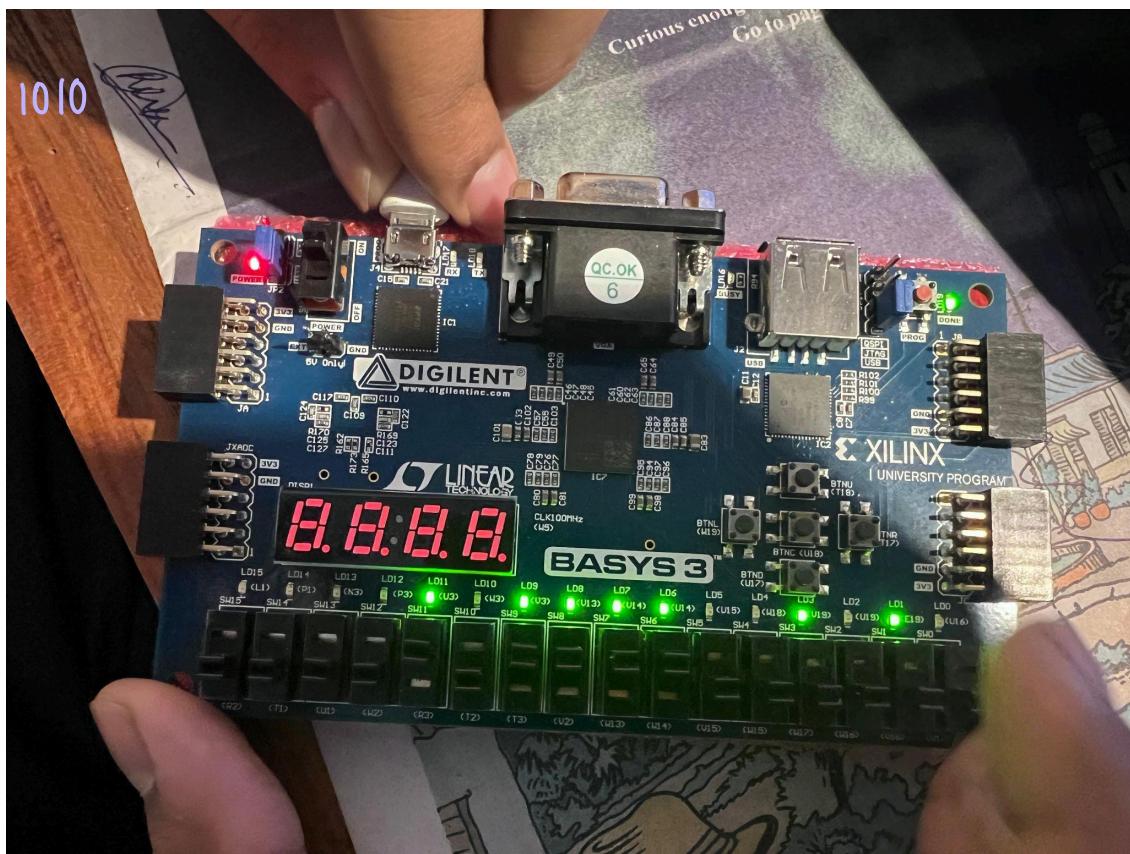
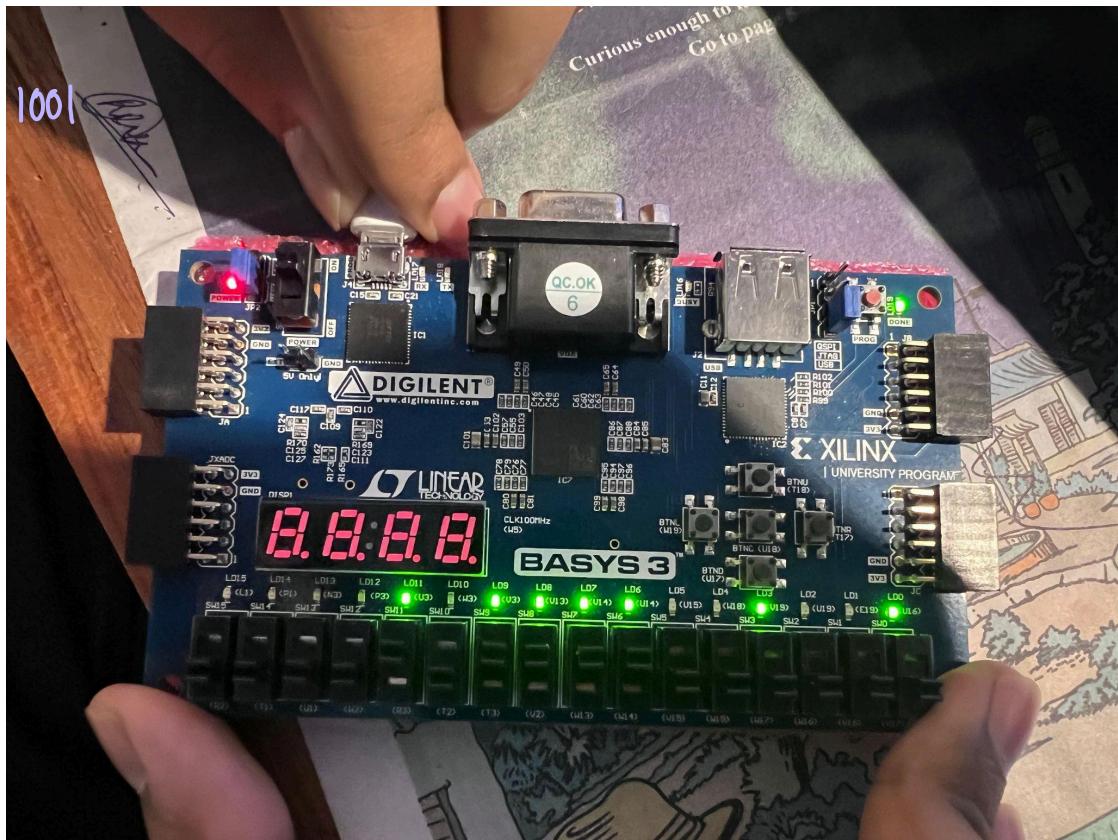
Name	Direction	Board Part Pin	Board Part Interface	Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type
Load	IN					W17	✓	✓	14	LVC MOS33*	-	3.300	
clk	IN					T17	✓	✓	14	LVC MOS33*	-	3.300	
mode	IN					W16	✓	✓	14	LVC MOS33*	-	3.300	
X[3]	IN					W2	✓	✓	34	LVC MOS33*	-	3.300	
X[2]	IN					R3	✓	✓	34	LVC MOS33*	-	3.300	
X[1]	IN					T2	✓	✓	34	LVC MOS33*	-	3.300	
X[0]	IN					T3	✓	✓	34	LVC MOS33*	-	3.300	
Y[3]	IN					V2	✓	✓	34	LVC MOS33*	-	3.300	
Y[2]	IN					W13	✓	✓	14	LVC MOS33*	-	3.300	
Y[1]	IN					W14	✓	✓	14	LVC MOS33*	-	3.300	
Y[0]	IN					W15	✓	✓	14	LVC MOS33*	-	3.300	
out[3]	OUT					V19	✓	✓	14	LVC MOS33*	-	3.300	12
out[2]	OUT					U19	✓	✓	14	LVC MOS33*	-	3.300	12
out[1]	OUT					E19	✓	✓	14	LVC MOS33*	-	3.300	12
out[0]	OUT					U16	✓	✓	14	LVC MOS33*	-	3.300	12
out_x[3]	OUT					P3	✓	✓	35	LVC MOS33*	-	3.300	12
out_x[2]	OUT					U3	✓	✓	34	LVC MOS33*	-	3.300	12
out_x[1]	OUT					W3	✓	✓	34	LVC MOS33*	-	3.300	12
out_x[0]	OUT					V3	✓	✓	34	LVC MOS33*	-	3.300	12
out_y[3]	OUT					V13	✓	✓	14	LVC MOS33*	-	3.300	12
out_y[2]	OUT					V14	✓	✓	14	LVC MOS33*	-	3.300	12
out_y[1]	OUT					U14	✓	✓	14	LVC MOS33*	-	3.300	12

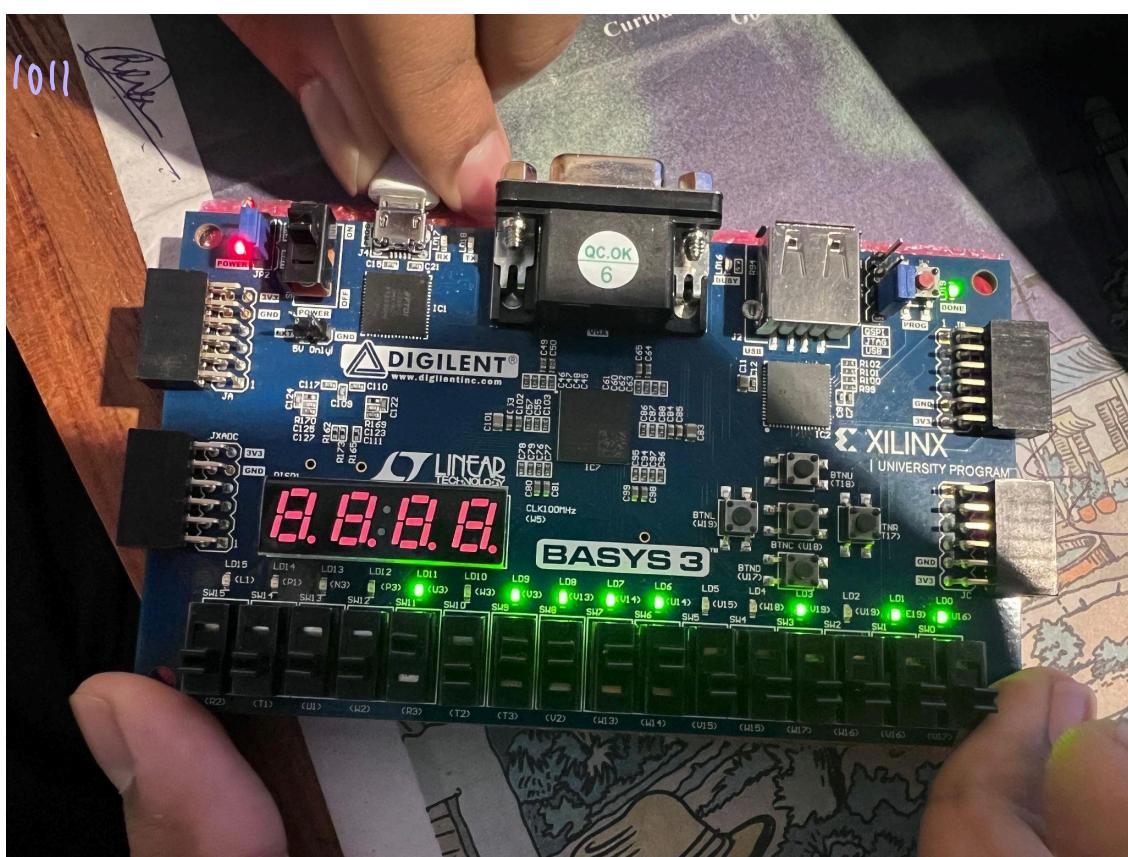
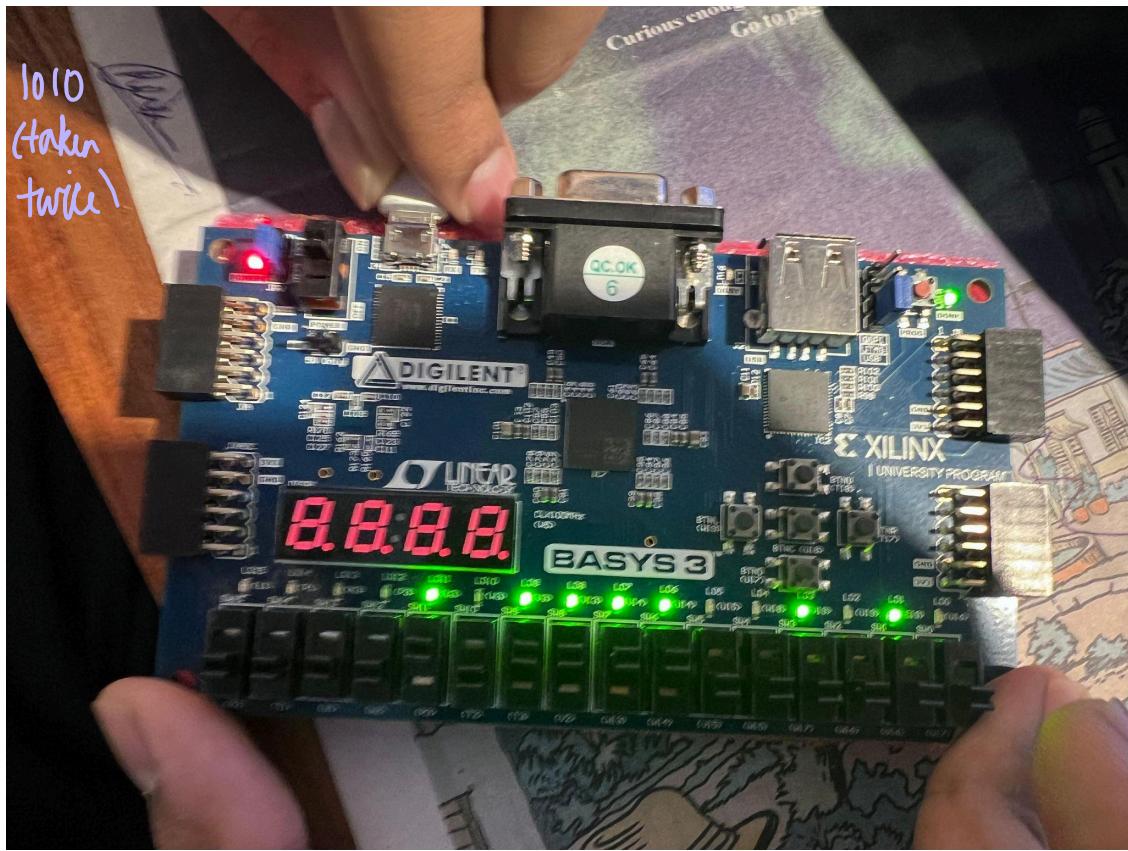
7) Implementation and Working

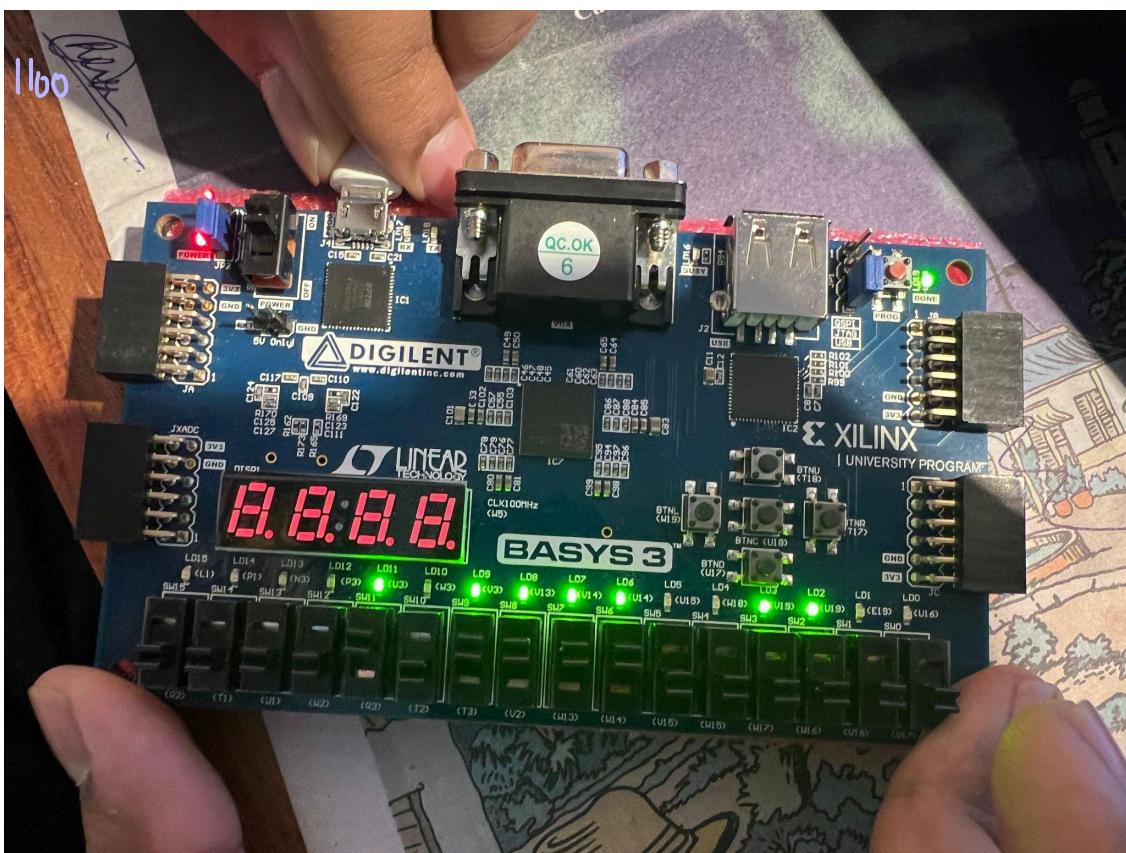
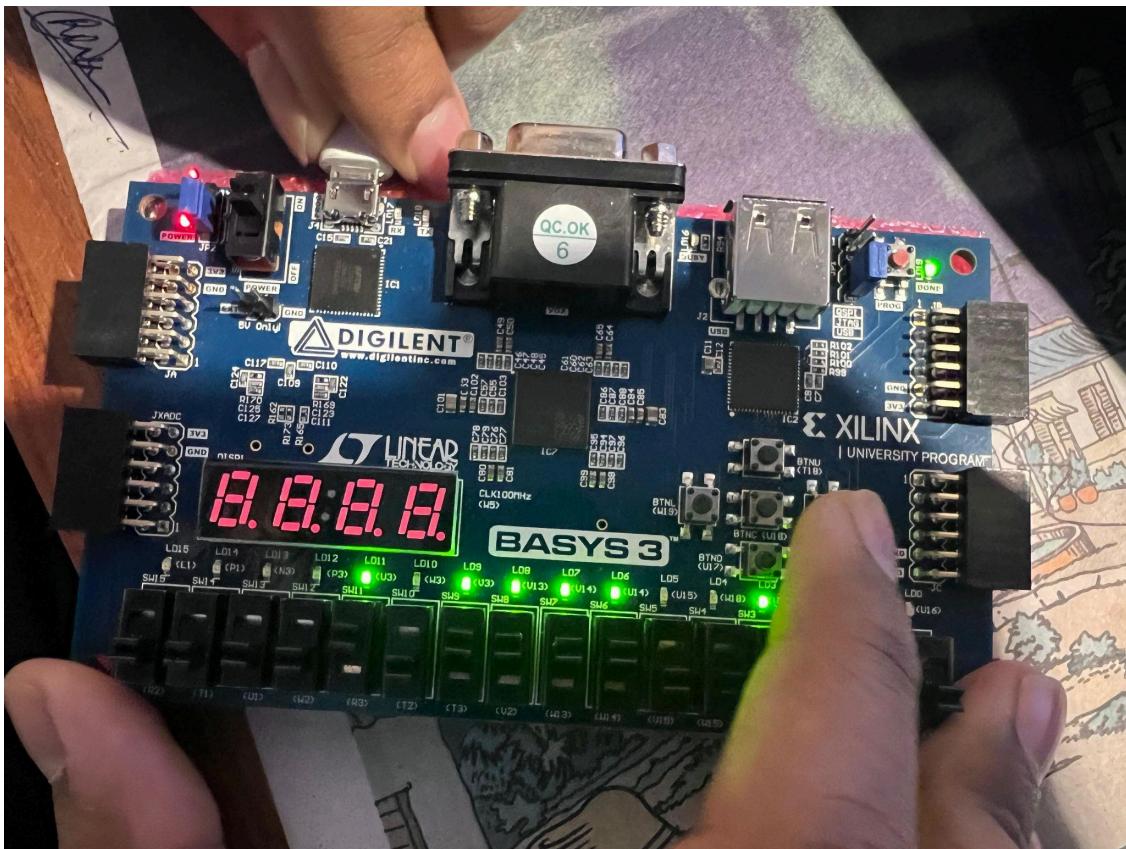
As shown in the ports, the input X is 0101 and input Y is 1110. The initial loaded signal is X as 0101 in the rightmost side. As can be seen in the first picture Load(W17) is on and mode(W16) is off.

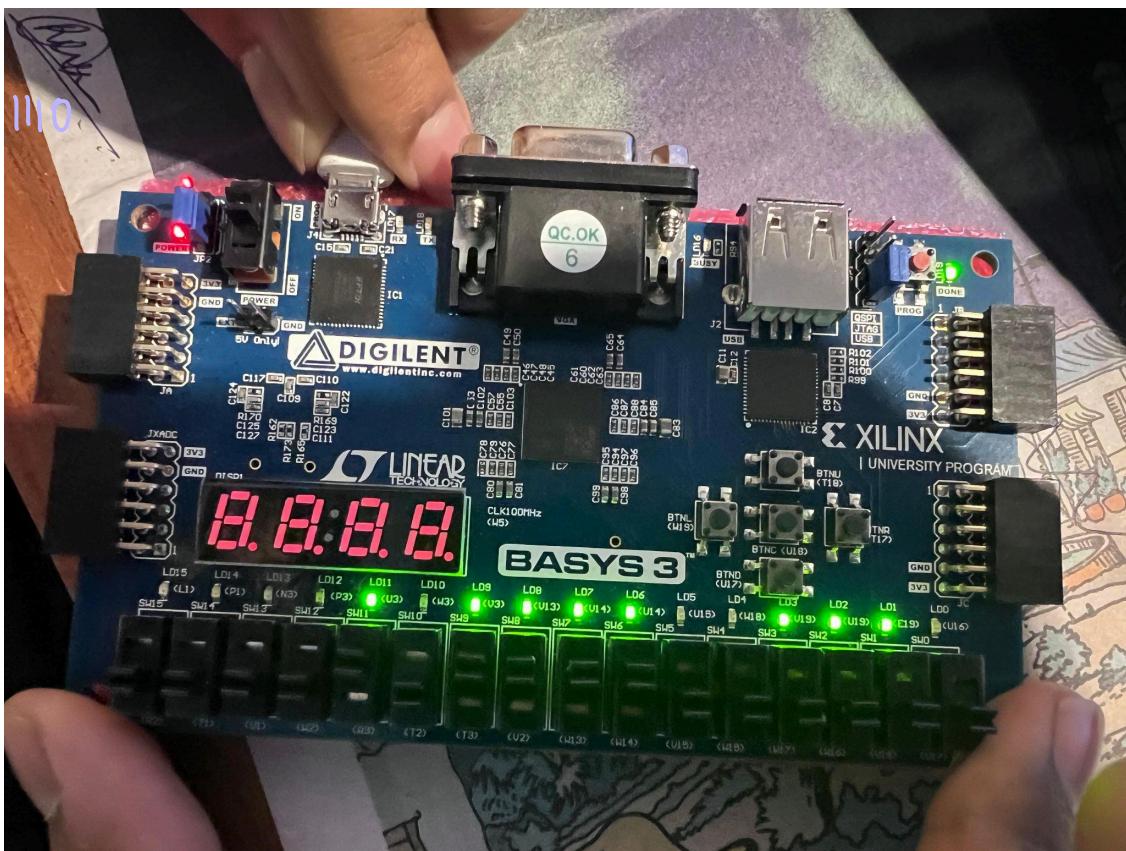
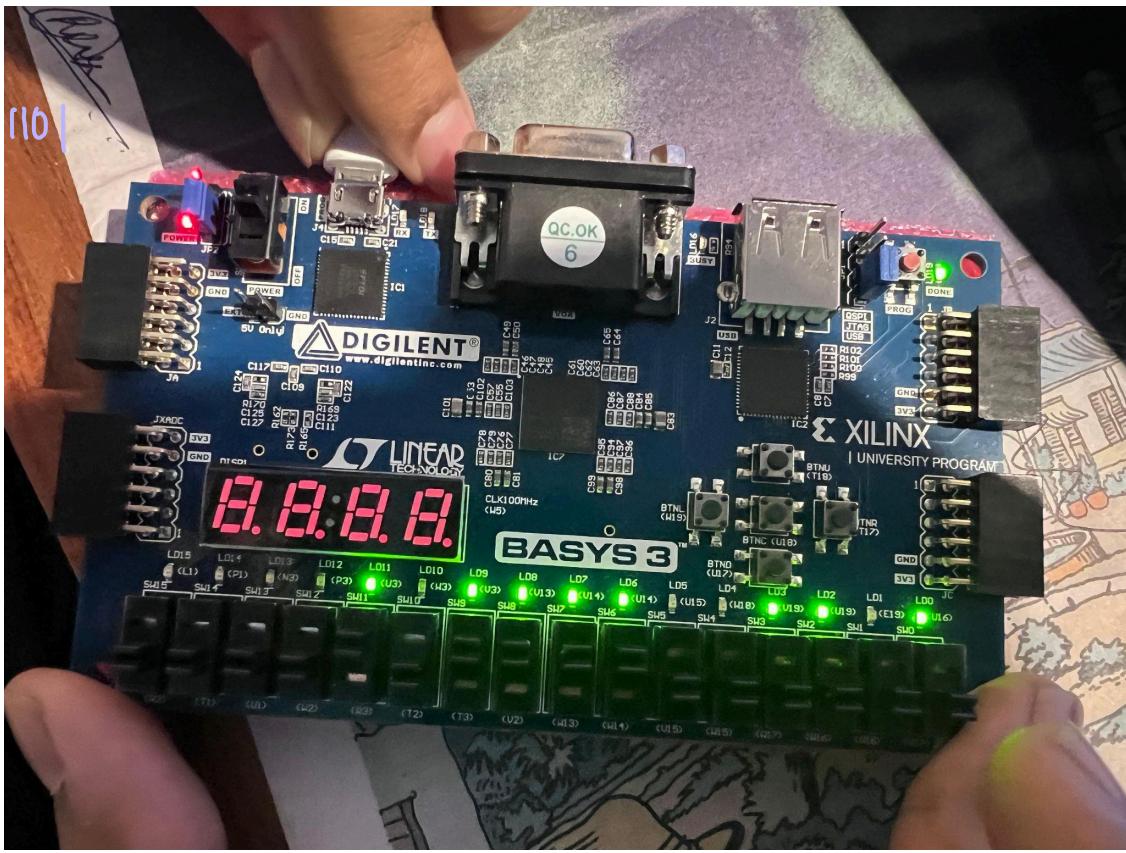


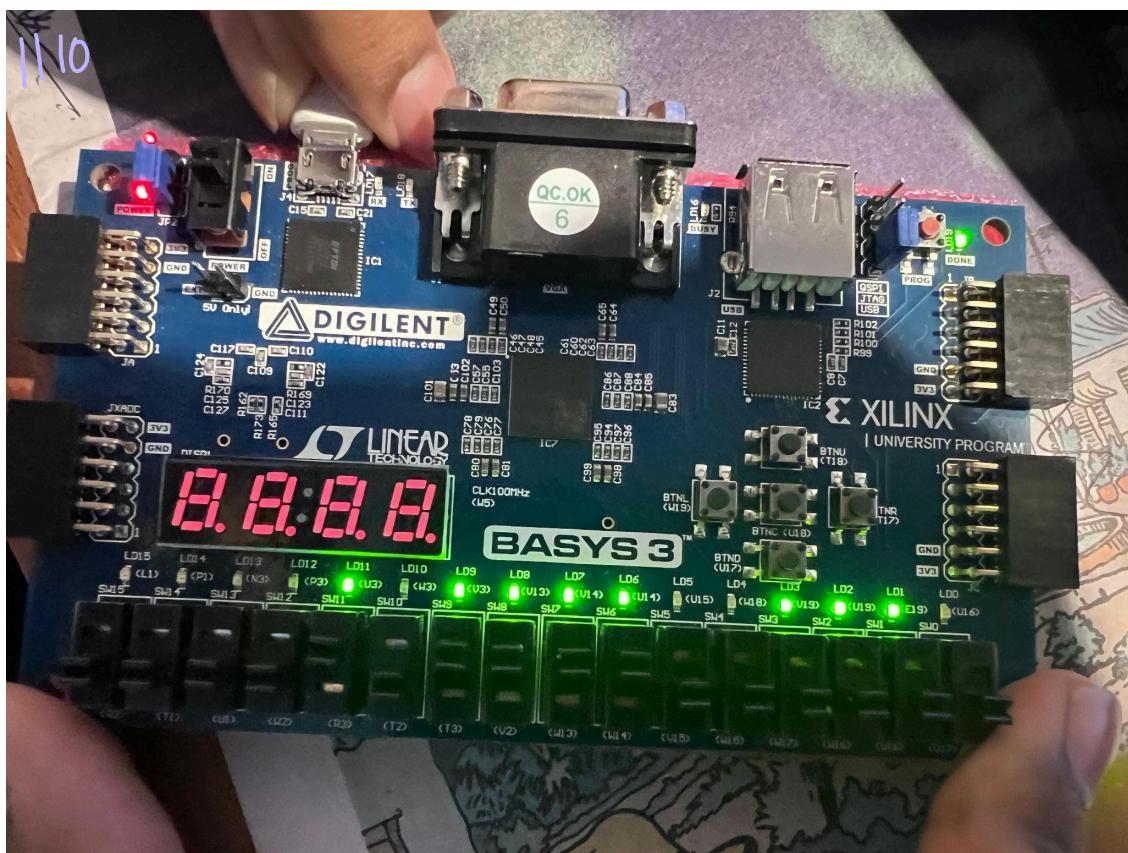
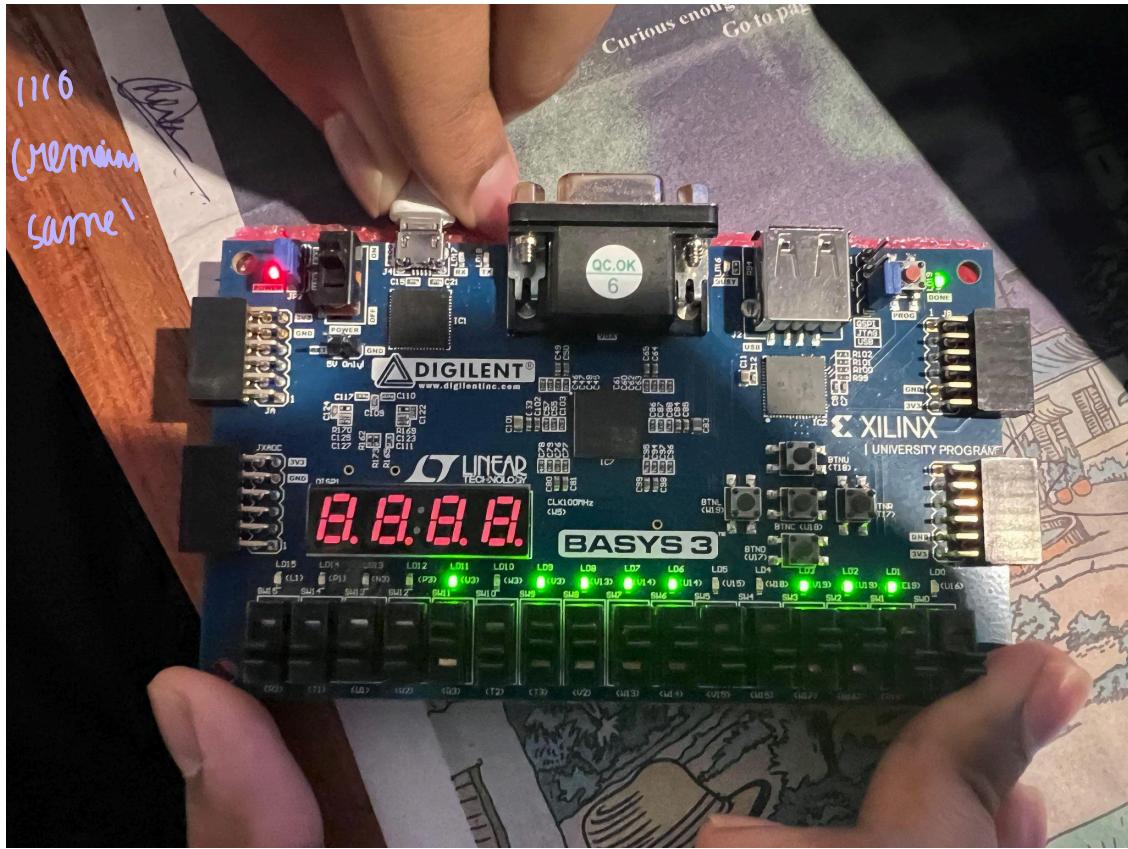


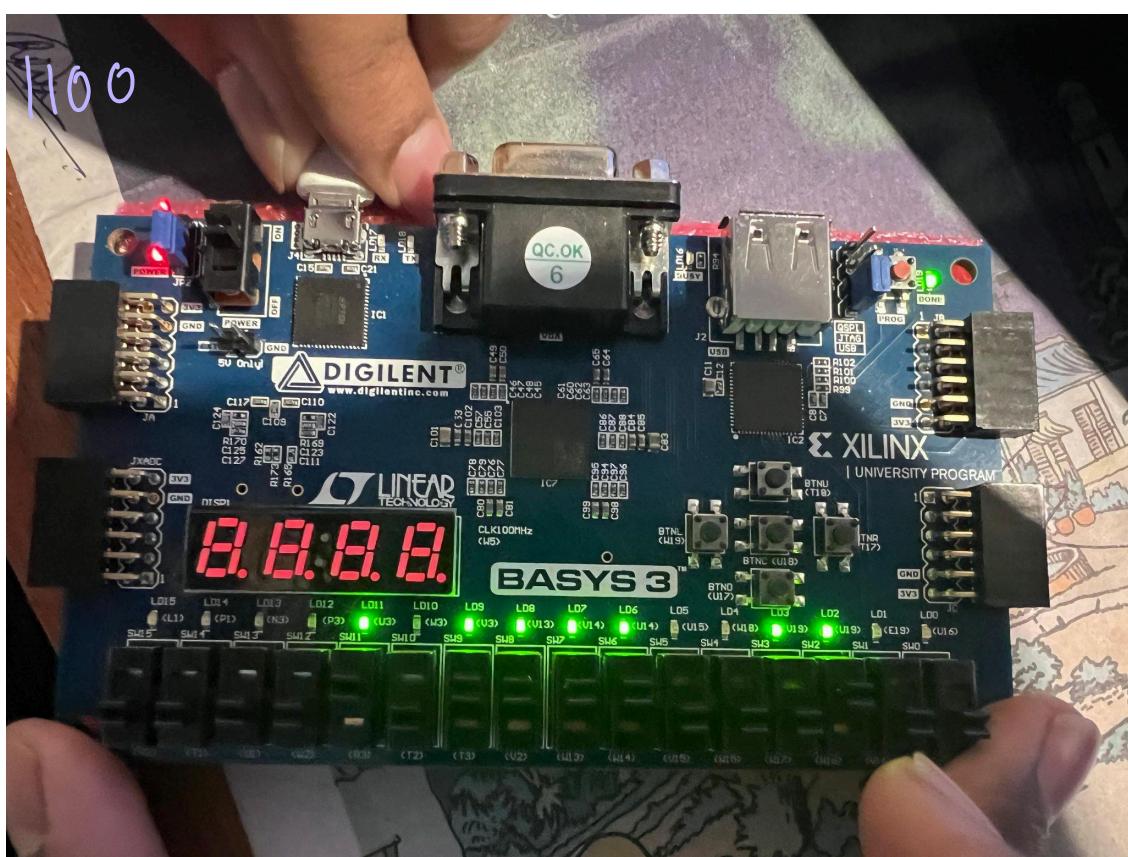
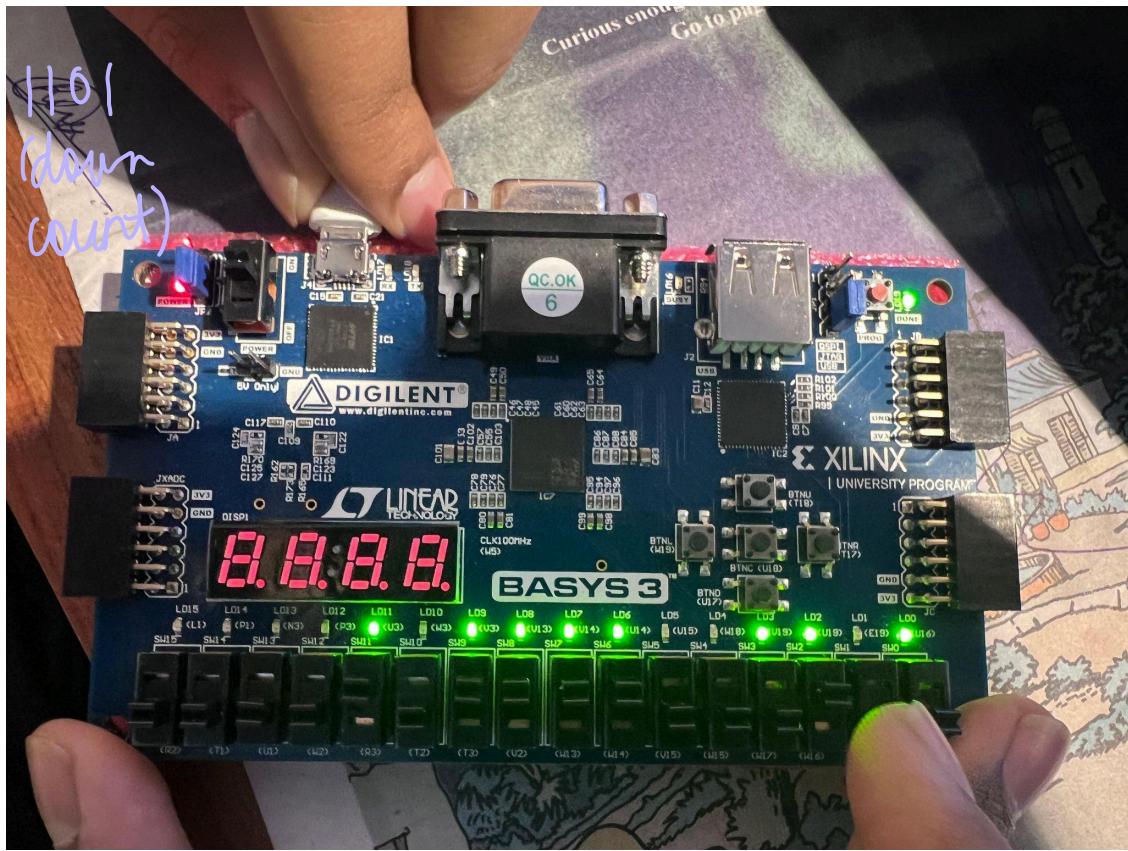




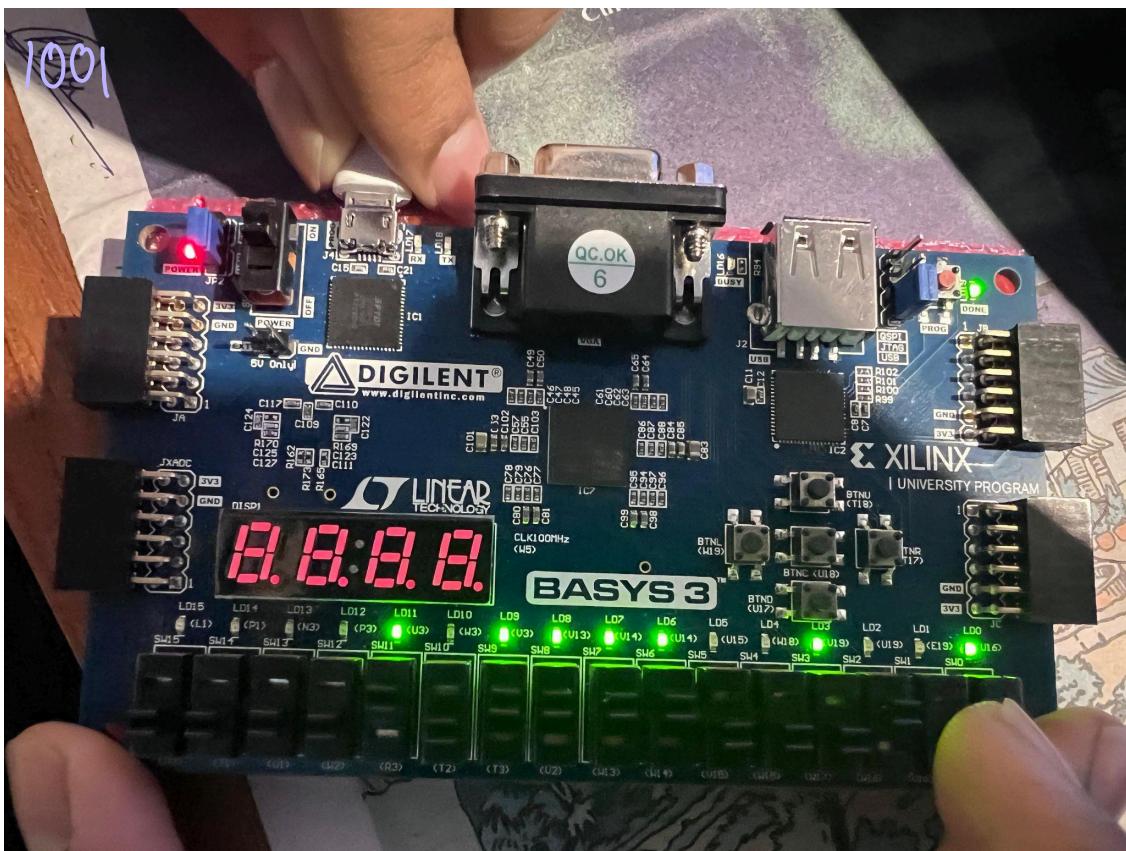
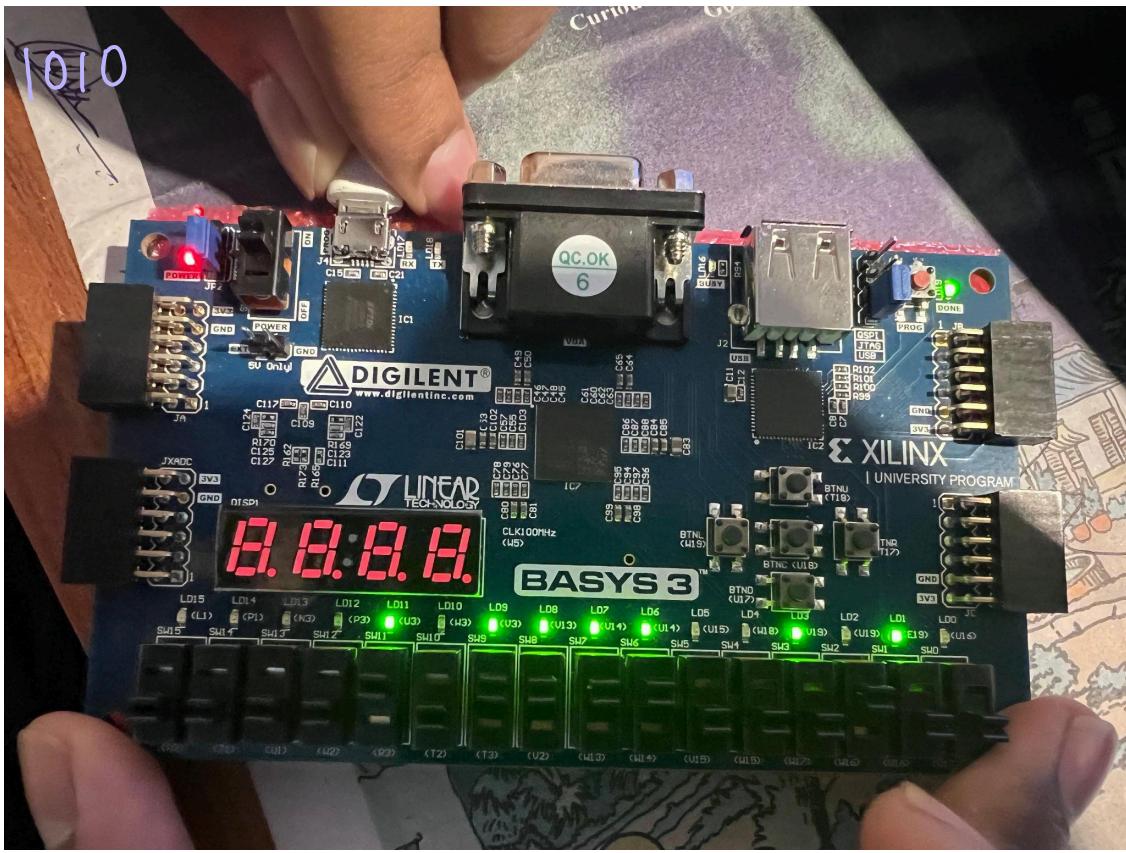


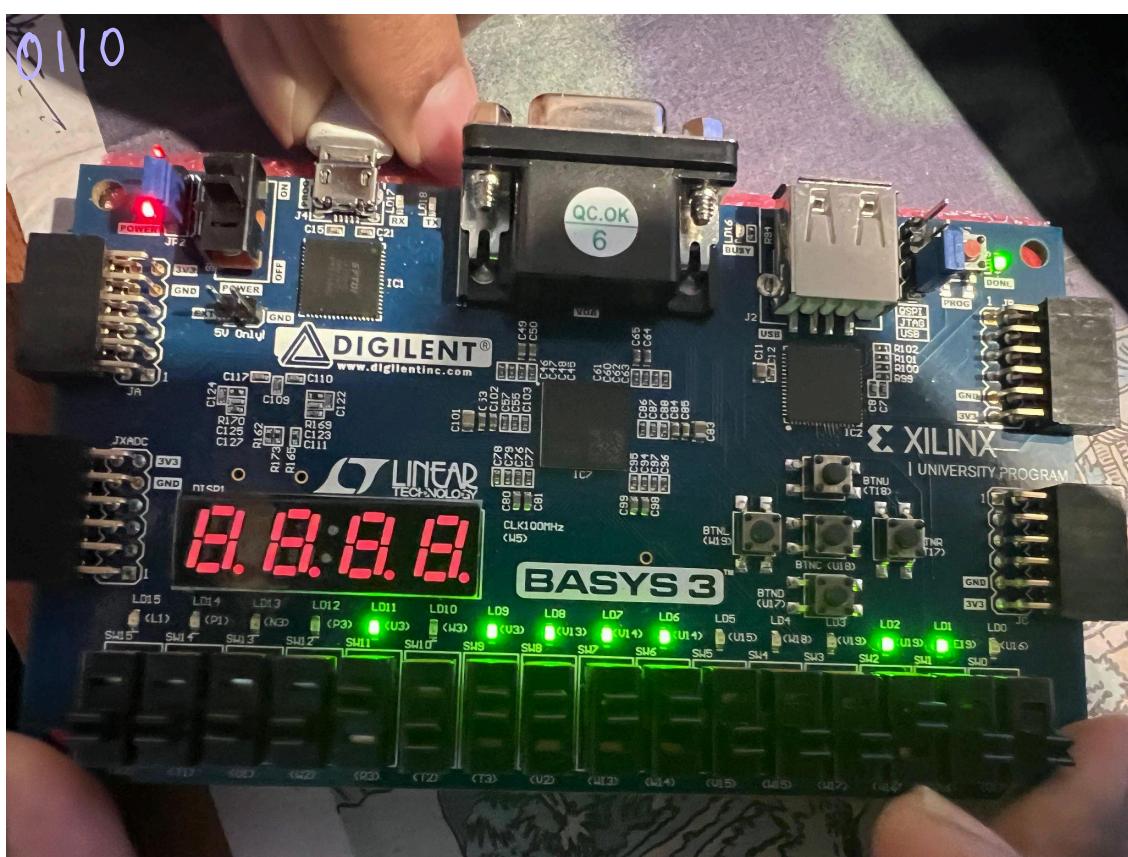
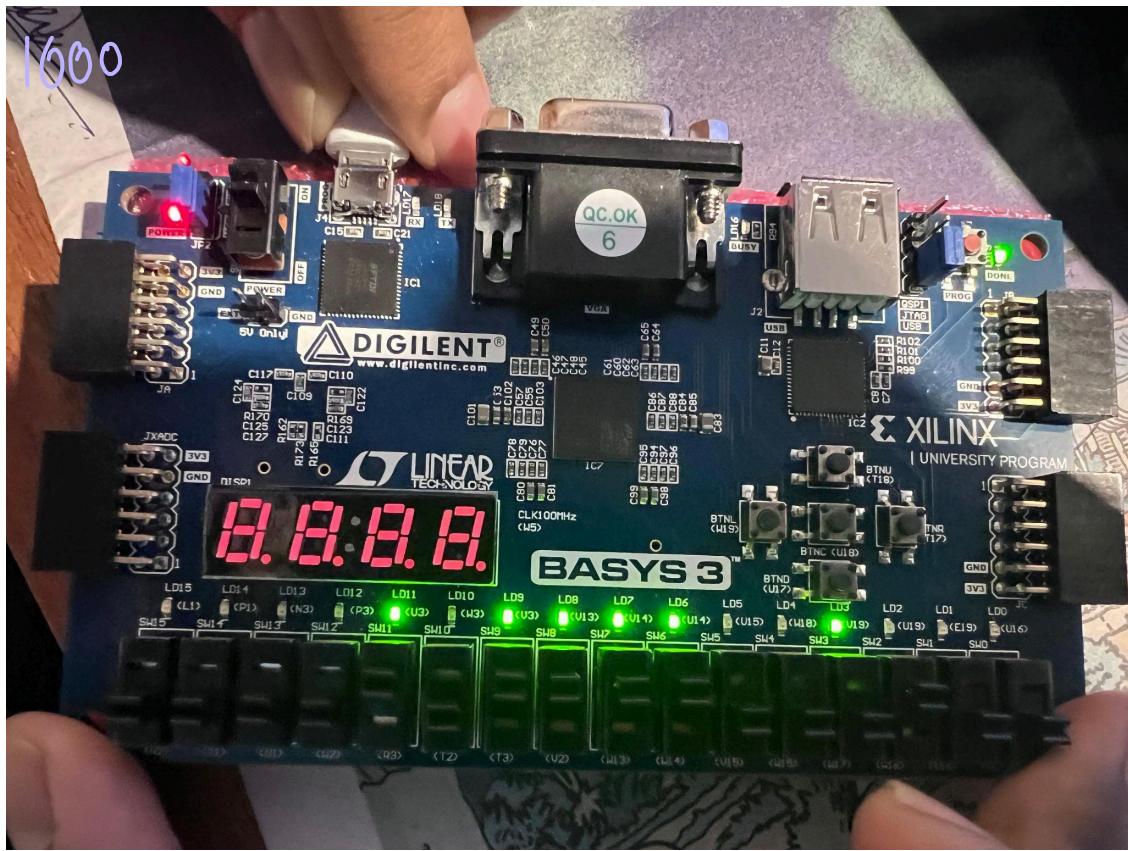




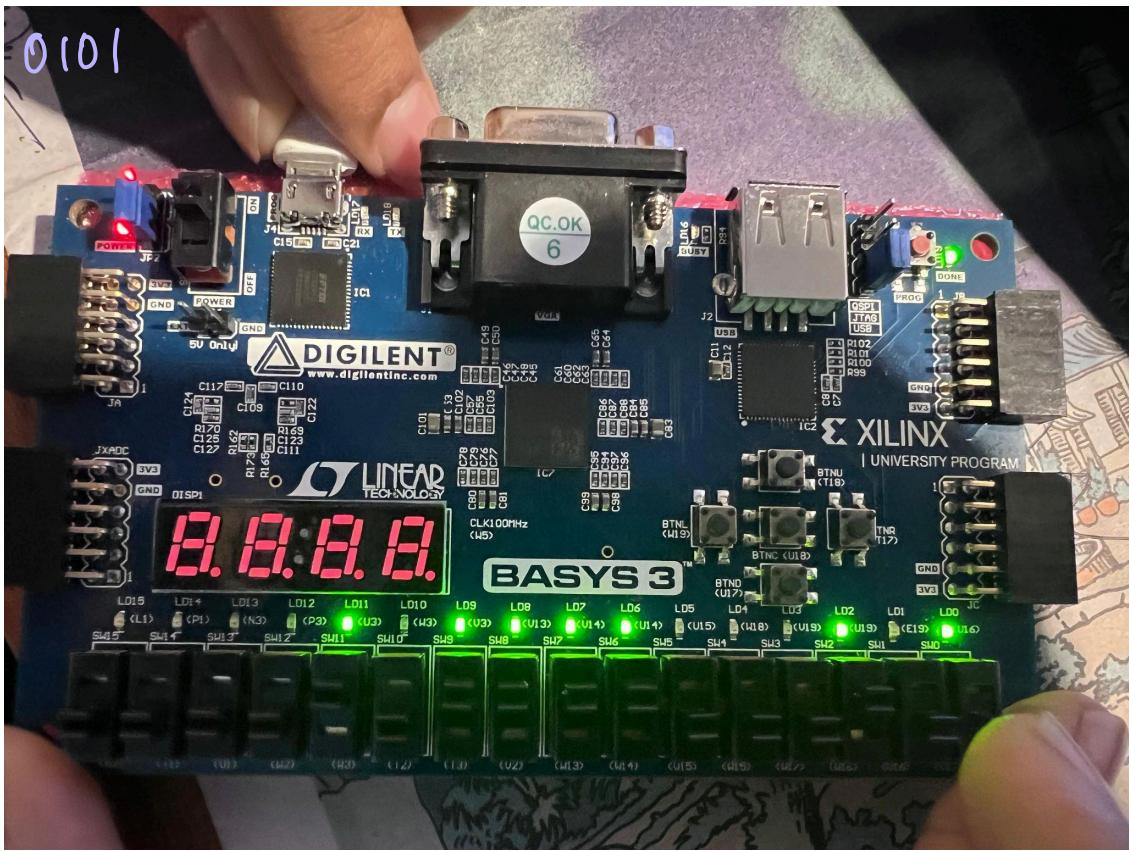


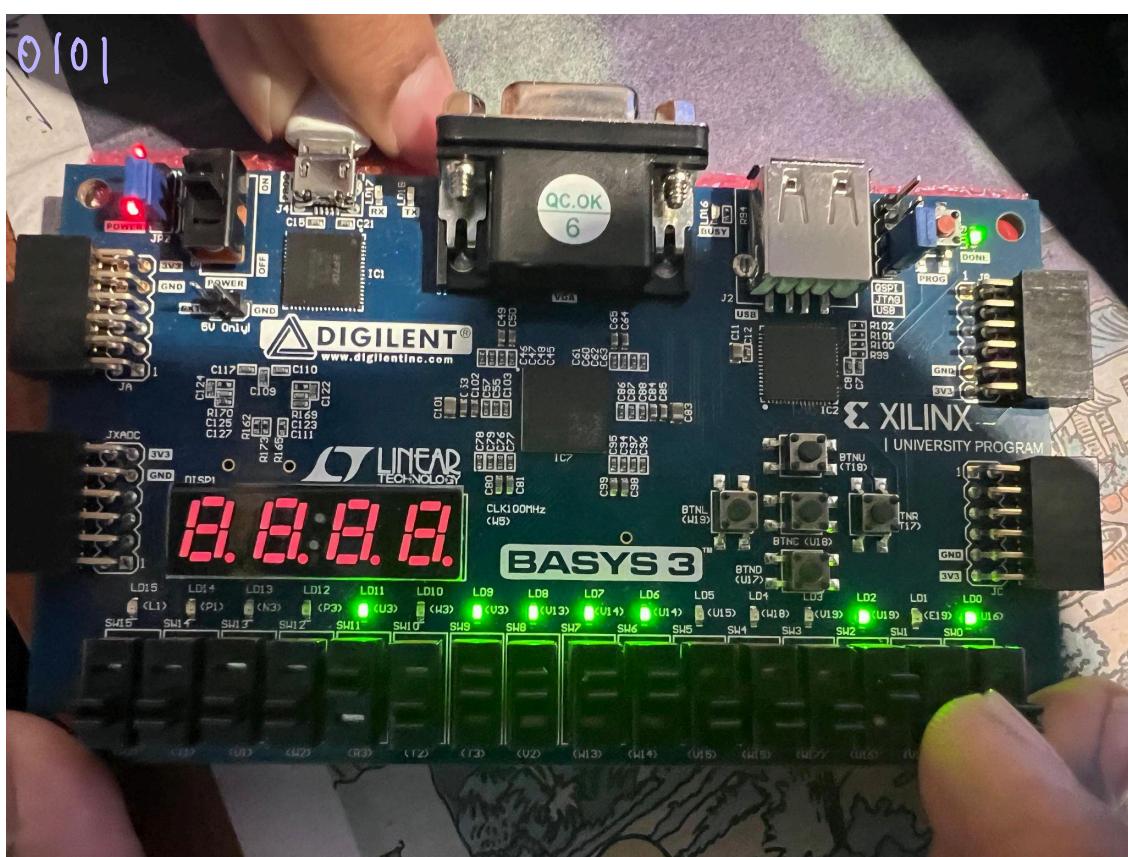
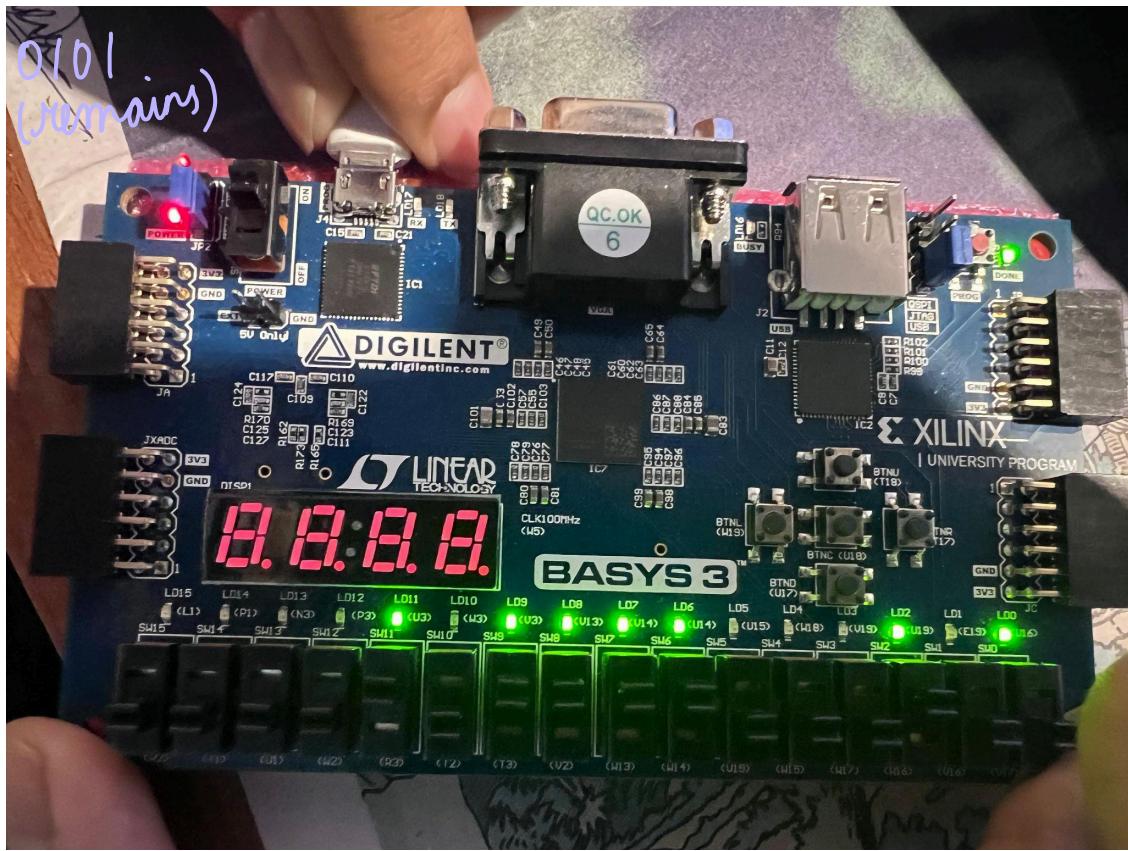
(1011 has been missed)





(0111 config has been mixed)





8) Timing report

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```
| Tool Version : Vivado v.2019.2 (win64) Build 2708876 Wed Nov 6 21:40:23 MST 2019
| Date       : Tue Feb 18 16:50:35 2025
| Host       : DESKTOP-Q29BN3N running 64-bit major release (build 9200)
| Command    : report_timing_summary -delay_type min_max -report_unconstrained
-check_timing_verbose -max_paths 10 -input_pins -routable_nets -name timing_2 -file {D:/IIT
GANDHINAGAR/Semester 4/ES204 - Digital Systems/a/timing_report.txt} -append -rpx {D:/IIT
GANDHINAGAR/Semester 4/ES204 - Digital Systems/a/a.runs/impl_1/timing_report.rpx}
| Design     : a
| Device     : 7a35t-cpg236
| Speed File : -1 PRODUCTION 1.23 2018-06-13
```

Timing Summary Report

Timer Settings

```
Enable Multi Corner Analysis      : Yes
Enable Pessimism Removal        : Yes
Pessimism Removal Resolution    : Nearest Common Node
Enable Input Delay Default Clock : No
Enable Preset / Clear Arcs       : No
Disable Flight Delays           : No
Ignore I/O Paths                : No
Timing Early Launch at Borrowing Latches : No
Borrow Time for Max Delay Exceptions : Yes
Merge Timing Exceptions          : Yes
```

Corner Analyze Analyze
Name Max Paths Min Paths

Slow	Yes	Yes
Fast	Yes	Yes

check_timing report

Table of Contents

1. checking no_clock
2. checking constant_clock
3. checking pulse_width_clock
4. checking unconstrained_internal_endpoints
5. checking no_input_delay
6. checking no_output_delay
7. checking multiple_clock
8. checking generated_clocks
9. checking loops
10. checking partial_input_delay
11. checking partial_output_delay
12. checking latch_loops

1. checking no_clock

There are 4 register/latch pins with no clock driven by root clock pin: clk (HIGH)

out_reg[0]/C
 out_reg[1]/C
 out_reg[2]/C
 out_reg[3]/C

2. checking constant_clock

There are 0 register/latch pins with constant_clock.

3. checking pulse_width_clock

There are 0 register/latch pins which need pulse_width check

4. checking unconstrained_internal_endpoints

There are 8 pins that are not constrained for maximum delay. (HIGH)

```
out_reg[0]/CE
out_reg[0]/D
out_reg[1]/CE
out_reg[1]/D
out_reg[2]/CE
out_reg[2]/D
out_reg[3]/CE
out_reg[3]/D
```

There are 0 pins that are not constrained for maximum delay due to constant clock.

5. checking no_input_delay

There are 10 input ports with no input delay specified. (HIGH)

```
Load
X[0]
X[1]
X[2]
X[3]
Y[0]
Y[1]
Y[2]
Y[3]
mode
```

There are 0 input ports with no input delay but user has a false path constraint.

6. checking no_output_delay

There are 4 ports with no output delay specified. (HIGH)

```
out[0]
out[1]
out[2]
out[3]
```

There are 0 ports with no output delay but user has a false path constraint

There are 0 ports with no output delay but with a timing clock defined on it or propagating through it

7. checking multiple_clock

There are 0 register/latch pins with multiple clocks.

8. checking generated_clocks

There are 0 generated clocks that are not connected to a clock source.

9. checking loops

There are 0 combinational loops in the design.

10. checking partial_input_delay

There are 0 input ports with partial input delay specified.

11. checking partial_output_delay

There are 0 ports with partial output delay specified.

12. checking latch_loops

There are 0 combinational latch loops in the design through latch input

| Design Timing Summary

WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns)
THS Failing Endpoints THS Total Endpoints WPWS(ns) TPWS(ns) TPWS Failing
Endpoints TPWS Total Endpoints

inf	0.000	0	20	inf	0.000	0
20	NA	NA	NA	NA	NA	

There are no user specified timing constraints.

| Clock Summary

| Intra Clock Table

Clock	WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)
THS(ns)	THS Failing Endpoints	THS Total Endpoints	WPWS(ns)	TPWS(ns)	TPWS
Failing Endpoints	TPWS Total Endpoints				

| Inter Clock Table

From Clock	To Clock	WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)
	THS(ns)	THS Failing Endpoints	THS Total Endpoints			

| Other Path Groups Table

Path Group	From Clock	To Clock	WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints
Total Endpoints	WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints		

| User Ignored Path Table

Path Group From Clock To Clock

| Unconstrained Path Table

Path Group From Clock To Clock

(none)

| Timing Details

Path Group: (none)

From Clock:

To Clock:

Max Delay	20 Endpoints
Min Delay	20 Endpoints

Max Delay Paths

Slack: inf

Source: Y[3]
 (input port)
 Destination: out_y[3]
 (output port)
 Path Group: (none)
 Path Type: Max at Slow Process Corner
 Data Path Delay: 10.273ns (logic 4.959ns (48.268%) route 5.314ns (51.732%))
 Logic Levels: 2 (IBUF=1 OBUF=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
V2		0.000	0.000	r Y[3] (IN)
	net (fo=0)	0.000	0.000	Y[3]
V2			r	Y_IBUF[3]_inst/I
V2	IBUF (Prop_ibuf_I_O)	1.454	1.454	r Y_IBUF[3]_inst/O
	net (fo=3, routed)	5.314	6.769	out_y_OBUF[3]
V13			r	out_y_OBUF[3]_inst/I
V13	OBUF (Propobuf_I_O)	3.504	10.273	r out_y_OBUF[3]_inst/O
	net (fo=0)	0.000	10.273	out_y[3]
V13			r	out_y[3] (OUT)

Slack: inf
 Source: X[3]
 (input port)
 Destination: out_x[3]
 (output port)
 Path Group: (none)
 Path Type: Max at Slow Process Corner
 Data Path Delay: 8.172ns (logic 4.987ns (61.021%) route 3.185ns (38.979%))
 Logic Levels: 2 (IBUF=1 OBUF=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
W2		0.000	0.000	r X[3] (IN)
	net (fo=0)	0.000	0.000	X[3]
W2			r	X_IBUF[3]_inst/I
W2	IBUF (Prop_ibuf_I_O)	1.469	1.469	r X_IBUF[3]_inst/O
	net (fo=2, routed)	3.185	4.654	out_x_OBUF[3]
P3			r	out_x_OBUF[3]_inst/I
P3	OBUF (Propobuf_I_O)	3.518	8.172	r out_x_OBUF[3]_inst/O
	net (fo=0)	0.000	8.172	out_x[3]
P3			r	out_x[3] (OUT)

Slack: inf
 Source: X[2]
 (input port)
 Destination: out_x[2]
 (output port)
 Path Group: (none)
 Path Type: Max at Slow Process Corner
 Data Path Delay: 7.327ns (logic 4.968ns (67.798%) route 2.359ns (32.202%))
 Logic Levels: 2 (IBUF=1 OBUF=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
R3		0.000	0.000 r	X[2] (IN)
	net (fo=0)	0.000	0.000	X[2]
R3			r	X_IBUF[2]_inst/I
R3	IBUF (Prop_ibuf_I_O)	1.464	1.464 r	X_IBUF[2]_inst/O
	net (fo=2, routed)	2.359	3.823	out_x_OBUF[2]
U3			r	out_x_OBUF[2]_inst/I
U3	OBUF (Propobuf_I_O)	3.504	7.327 r	out_x_OBUF[2]_inst/O
	net (fo=0)	0.000	7.327	out_x[2]
U3			r	out_x[2] (OUT)

Slack: inf
 Source: X[1]
 (input port)
 Destination: out_x[1]
 (output port)
 Path Group: (none)
 Path Type: Max at Slow Process Corner
 Data Path Delay: 7.195ns (logic 4.983ns (69.262%) route 2.212ns (30.738%))
 Logic Levels: 2 (IBUF=1 OBUF=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
T2		0.000	0.000 r	X[1] (IN)
	net (fo=0)	0.000	0.000	X[1]
T2			r	X_IBUF[1]_inst/I
T2	IBUF (Prop_ibuf_I_O)	1.458	1.458 r	X_IBUF[1]_inst/O
	net (fo=2, routed)	2.212	3.669	out_x_OBUF[1]
W3			r	out_x_OBUF[1]_inst/I
W3	OBUF (Propobuf_I_O)	3.525	7.195 r	out_x_OBUF[1]_inst/O
	net (fo=0)	0.000	7.195	out_x[1]

W3

r out_x[1] (OUT)

Slack: inf
 Source: Y[1]
 (input port)
 Destination: out_y[1]
 (output port)
 Path Group: (none)
 Path Type: Max at Slow Process Corner
 Data Path Delay: 7.114ns (logic 4.956ns (69.669%) route 2.158ns (30.331%))
 Logic Levels: 2 (IBUF=1 OBUF=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
W14		0.000	0.000 r	Y[1] (IN)
	net (fo=0)	0.000	0.000	Y[1]
W14			r	Y_IBUF[1]_inst/I
W14	IBUF (Prop_ibuf_I_O)	1.450	1.450 r	Y_IBUF[1]_inst/O
	net (fo=3, routed)	2.158	3.607	out_y_OBUF[1]
U14			r	out_y_OBUF[1]_inst/I
U14	OBUF (Prop_obuf_I_O)	3.506	7.114 r	out_y_OBUF[1]_inst/O
	net (fo=0)	0.000	7.114	out_y[1]
U14			r	out_y[1] (OUT)

Slack: inf
 Source: X[0]
 (input port)
 Destination: out_x[0]
 (output port)
 Path Group: (none)
 Path Type: Max at Slow Process Corner
 Data Path Delay: 7.112ns (logic 4.960ns (69.751%) route 2.151ns (30.249%))
 Logic Levels: 2 (IBUF=1 OBUF=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
T3		0.000	0.000 r	X[0] (IN)
	net (fo=0)	0.000	0.000	X[0]
T3			r	X_IBUF[0]_inst/I
T3	IBUF (Prop_ibuf_I_O)	1.452	1.452 r	X_IBUF[0]_inst/O
	net (fo=2, routed)	2.151	3.603	out_x_OBUF[0]
V3			r	out_x_OBUF[0]_inst/I

V3	OBUF (Prop_obuf_I_O) net (fo=0)	3.508 0.000	7.112 r out_x_OBUF[0]_inst/O 7.112 out_x[0]
V3			r out_x[0] (OUT)

Slack: inf
 Source: Y[2]
 (input port)
 Destination: out_y[2]
 (output port)
 Path Group: (none)
 Path Type: Max at Slow Process Corner
 Data Path Delay: 7.107ns (logic 4.960ns (69.783%) route 2.148ns (30.217%))
 Logic Levels: 2 (IBUF=1 OBUF=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
W13		0.000	0.000 r Y[2] (IN)	
	net (fo=0)	0.000	0.000 Y[2]	
W13			r Y_IBUF[2]_inst/I	
W13	IBUF (Prop_ibuf_I_O)	1.459	1.459 r Y_IBUF[2]_inst/O	
	net (fo=3, routed)	2.148	3.606 out_y_OBUF[2]	
V14			r out_y_OBUF[2]_inst/I	
V14	OBUF (Prop_obuf_I_O)	3.501	7.107 r out_y_OBUF[2]_inst/O	
	net (fo=0)	0.000	7.107 out_y[2]	
V14			r out_y[2] (OUT)	

Slack: inf
 Source: Y[0]
 (input port)
 Destination: out_y[0]
 (output port)
 Path Group: (none)
 Path Type: Max at Slow Process Corner
 Data Path Delay: 6.914ns (logic 4.965ns (71.819%) route 1.948ns (28.181%))
 Logic Levels: 2 (IBUF=1 OBUF=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
W15		0.000	0.000 r Y[0] (IN)	
	net (fo=0)	0.000	0.000 Y[0]	
W15			r Y_IBUF[0]_inst/I	
W15	IBUF (Prop_ibuf_I_O)	1.451	1.451 r Y_IBUF[0]_inst/O	

	net (fo=3, routed)	1.948	3.399	out_y_OBUF[0]
U15			r	out_y_OBUF[0]_inst/l
U15	OBUF (Prop_obuf_I_O)	3.514	6.914	r out_y_OBUF[0]_inst/O
	net (fo=0)	0.000	6.914	out_y[0]
U15			r	out_y[0] (OUT)

Slack: inf
 Source: out_reg[1]/C
 (rising edge-triggered cell FDRE)
 Destination: out[1]
 (output port)
 Path Group: (none)
 Path Type: Max at Slow Process Corner
 Data Path Delay: 6.568ns (logic 3.986ns (60.688%) route 2.582ns (39.312%))
 Logic Levels: 2 (FDRE=1 OBUF=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
SLICE_X0Y15	FDRE	0.000	0.000	r out_reg[1]/C
SLICE_X0Y15	FDRE (Prop_fdre_C_Q)	0.456	0.456	r out_reg[1]/Q
	net (fo=5, routed)	2.582	3.038	out_OBUF[1]
E19			r	out_OBUF[1]_inst/l
E19	OBUF (Prop_obuf_I_O)	3.530	6.568	r out_OBUF[1]_inst/O
	net (fo=0)	0.000	6.568	out[1]
E19			r	out[1] (OUT)

Slack: inf
 Source: out_reg[0]/C
 (rising edge-triggered cell FDRE)
 Destination: out[0]
 (output port)
 Path Group: (none)
 Path Type: Max at Slow Process Corner
 Data Path Delay: 6.107ns (logic 3.961ns (64.860%) route 2.146ns (35.140%))
 Logic Levels: 2 (FDRE=1 OBUF=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
SLICE_X0Y14	FDRE	0.000	0.000	r out_reg[0]/C
SLICE_X0Y14	FDRE (Prop_fdre_C_Q)	0.456	0.456	r out_reg[0]/Q
	net (fo=6, routed)	2.146	2.602	out_OBUF[0]
U16			r	out_OBUF[0]_inst/l

U16	OBUF (Prop_buf_I_O)	3.505	6.107	r	out_OBUF[0].inst/O
	net (fo=0)	0.000	6.107		out[0]
U16			r	out[0]	(OUT)

Min Delay Paths

Slack: inf
 Source: out_reg[1]/C
 (rising edge-triggered cell FDRE)
 Destination: out_reg[1]/D
 Path Group: (none)
 Path Type: Min at Fast Process Corner
 Data Path Delay: 0.385ns (logic 0.186ns (48.370%) route 0.199ns (51.630%))
 Logic Levels: 2 (FDRE=1 LUT6=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
SLICE_X0Y15	FDRE	0.000	0.000	r out_reg[1]/C
SLICE_X0Y15	FDRE (Prop_fred_C_Q)	0.141	0.141	r out_reg[1]/Q
	net (fo=5, routed)	0.199	0.340	out_OBUF[1]
SLICE_X0Y15			r out[1].i_1/I4	
SLICE_X0Y15	LUT6 (Prop_lut6_I4_O)	0.045	0.385	r out[1].i_1/O
	net (fo=1, routed)	0.000	0.385	p_1_in[1]
SLICE_X0Y15	FDRE		r out_reg[1]/D	

Slack: inf
 Source: out_reg[0]/C
 (rising edge-triggered cell FDRE)
 Destination: out_reg[0]/D
 Path Group: (none)
 Path Type: Min at Fast Process Corner
 Data Path Delay: 0.396ns (logic 0.186ns (46.938%) route 0.210ns (53.062%))
 Logic Levels: 2 (FDRE=1 LUT5=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
SLICE_X0Y14	FDRE	0.000	0.000	r out_reg[0]/C
SLICE_X0Y14	FDRE (Prop_fred_C_Q)	0.141	0.141	f out_reg[0]/Q

net (fo=6, routed)	0.210	0.351	out_OBUF[0]
SLICE_X0Y14		f	out[0]_i_1/I4
SLICE_X0Y14	LUT5 (Prop_lut5_I4_O)	0.045	0.396 r out[0]_i_1/O
	net (fo=1, routed)	0.000	0.396 p_1_in[0]
SLICE_X0Y14	FDRE		r out_reg[0]/D

Slack: inf
 Source: out_reg[1]/C
 (rising edge-triggered cell FDRE)
 Destination: out_reg[3]/D
 Path Group: (none)
 Path Type: Min at Fast Process Corner
 Data Path Delay: 0.490ns (logic 0.231ns (47.137%) route 0.259ns (52.863%))
 Logic Levels: 3 (FDRE=1 LUT5=2)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
SLICE_X0Y15	FDRE	0.000	0.000 r out_reg[1]/C	
SLICE_X0Y15	FDRE (Prop_fdre_C_Q)	0.141	0.141 r out_reg[1]/Q	
	net (fo=5, routed)	0.201	0.342 out_OBUF[1]	
SLICE_X0Y15			r out[3]_i_4/I2	
SLICE_X0Y15	LUT5 (Prop_lut5_I2_O)	0.045	0.387 r out[3]_i_4/O	
	net (fo=1, routed)	0.058	0.445 out[3]_i_4_n_0	
SLICE_X0Y15			r out[3]_i_2/I4	
SLICE_X0Y15	LUT5 (Prop_lut5_I4_O)	0.045	0.490 r out[3]_i_2/O	
	net (fo=1, routed)	0.000	0.490 p_1_in[3]	
SLICE_X0Y15	FDRE		r out_reg[3]/D	

Slack: inf
 Source: out_reg[2]/C
 (rising edge-triggered cell FDRE)
 Destination: out_reg[0]/CE
 Path Group: (none)
 Path Type: Min at Fast Process Corner
 Data Path Delay: 0.500ns (logic 0.231ns (46.201%) route 0.269ns (53.799%))
 Logic Levels: 3 (FDRE=1 LUT5=1 LUT6=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
SLICE_X0Y15	FDRE	0.000	0.000 r out_reg[2]/C	
SLICE_X0Y15	FDRE (Prop_fdre_C_Q)	0.141	0.141 r out_reg[2]/Q	
	net (fo=4, routed)	0.142	0.283 out_OBUF[2]	

SLICE_X0Y14			r out[3]_i_3/I5
SLICE_X0Y14	LUT6 (Prop_lut6_I5_O)	0.045	0.328 r out[3]_i_3/O
	net (fo=1, routed)	0.058	0.387 out[3]_i_3_n_0
SLICE_X0Y14			r out[3]_i_1/I2
SLICE_X0Y14	LUT5 (Prop_lut5_I2_O)	0.045	0.432 r out[3]_i_1/O
	net (fo=4, routed)	0.068	0.500 out[3]_i_1_n_0
SLICE_X0Y14	FDRE		r out_reg[0]/CE

Slack: inf
 Source: out_reg[2]/C
 (rising edge-triggered cell FDRE)
 Destination: out_reg[1]/CE
 Path Group: (none)
 Path Type: Min at Fast Process Corner
 Data Path Delay: 0.555ns (logic 0.231ns (41.632%) route 0.324ns (58.368%))
 Logic Levels: 3 (FDRE=1 LUT5=1 LUT6=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
SLICE_X0Y15	FDRE	0.000	0.000	r out_reg[2]/C
SLICE_X0Y15	FDRE (Prop_fdre_C_Q)	0.141	0.141	r out_reg[2]/Q
	net (fo=4, routed)	0.142	0.283	out_OBUF[2]
SLICE_X0Y14			r out[3]_i_3/I5	
SLICE_X0Y14	LUT6 (Prop_lut6_I5_O)	0.045	0.328	r out[3]_i_3/O
	net (fo=1, routed)	0.058	0.387	out[3]_i_3_n_0
SLICE_X0Y14			r out[3]_i_1/I2	
SLICE_X0Y14	LUT5 (Prop_lut5_I2_O)	0.045	0.432	r out[3]_i_1/O
	net (fo=4, routed)	0.123	0.555	out[3]_i_1_n_0
SLICE_X0Y15	FDRE		r out_reg[1]/CE	

Slack: inf
 Source: out_reg[2]/C
 (rising edge-triggered cell FDRE)
 Destination: out_reg[2]/CE
 Path Group: (none)
 Path Type: Min at Fast Process Corner
 Data Path Delay: 0.555ns (logic 0.231ns (41.632%) route 0.324ns (58.368%))
 Logic Levels: 3 (FDRE=1 LUT5=1 LUT6=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
SLICE_X0Y15	FDRE	0.000	0.000	r out_reg[2]/C

SLICE_X0Y15	FDRE (Prop_fdre_C_Q)	0.141	0.141	r out_reg[2]/Q
	net (fo=4, routed)	0.142	0.283	out_OBUF[2]
SLICE_X0Y14				r out[3]_i_3/I5
SLICE_X0Y14	LUT6 (Prop_lut6_I5_O)	0.045	0.328	r out[3]_i_3/O
	net (fo=1, routed)	0.058	0.387	out[3]_i_3_n_0
SLICE_X0Y14				r out[3]_i_1/I2
SLICE_X0Y14	LUT5 (Prop_lut5_I2_O)	0.045	0.432	r out[3]_i_1/O
	net (fo=4, routed)	0.123	0.555	out[3]_i_1_n_0
SLICE_X0Y15	FDRE			r out_reg[2]/CE

Slack: inf
 Source: out_reg[2]/C
 (rising edge-triggered cell FDRE)
 Destination: out_reg[3]/CE
 Path Group: (none)
 Path Type: Min at Fast Process Corner
 Data Path Delay: 0.555ns (logic 0.231ns (41.632%) route 0.324ns (58.368%))
 Logic Levels: 3 (FDRE=1 LUT5=1 LUT6=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
SLICE_X0Y15	FDRE	0.000	0.000	r out_reg[2]/C
SLICE_X0Y15	FDRE (Prop_fdre_C_Q)	0.141	0.141	r out_reg[2]/Q
	net (fo=4, routed)	0.142	0.283	out_OBUF[2]
SLICE_X0Y14				r out[3]_i_3/I5
SLICE_X0Y14	LUT6 (Prop_lut6_I5_O)	0.045	0.328	r out[3]_i_3/O
	net (fo=1, routed)	0.058	0.387	out[3]_i_3_n_0
SLICE_X0Y14				r out[3]_i_1/I2
SLICE_X0Y14	LUT5 (Prop_lut5_I2_O)	0.045	0.432	r out[3]_i_1/O
	net (fo=4, routed)	0.123	0.555	out[3]_i_1_n_0
SLICE_X0Y15	FDRE			r out_reg[3]/CE

Slack: inf
 Source: out_reg[1]/C
 (rising edge-triggered cell FDRE)
 Destination: out_reg[2]/D
 Path Group: (none)
 Path Type: Min at Fast Process Corner
 Data Path Delay: 0.594ns (logic 0.293ns (49.298%) route 0.301ns (50.702%))
 Logic Levels: 3 (FDRE=1 LUT4=1 LUT5=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
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SLICE_X0Y15	FDRE	0.000	0.000	r	out_reg[1]/C
SLICE_X0Y15	FDRE (Prop_fdre_C_Q)	0.141	0.141	r	out_reg[1]/Q
	net (fo=5, routed)	0.201	0.342		out_OBUF[1]
SLICE_X0Y15				r	out[2]_i_2/I2
SLICE_X0Y15	LUT4 (Prop_lut4_I2_O)	0.042	0.384	r	out[2]_i_2/O
	net (fo=1, routed)	0.100	0.484		out[2]_i_2_n_0
SLICE_X0Y15				r	out[2]_i_1/I4
SLICE_X0Y15	LUT5 (Prop_lut5_I4_O)	0.110	0.594	r	out[2]_i_1/O
	net (fo=1, routed)	0.000	0.594	p_1_in[2]	
SLICE_X0Y15	FDRE			r	out_reg[2]/D

Slack: inf
 Source: out_reg[2]/C
 (rising edge-triggered cell FDRE)
 Destination: out[2]
 (output port)
 Path Group: (none)
 Path Type: Min at Fast Process Corner
 Data Path Delay: 1.771ns (logic 1.343ns (75.851%) route 0.428ns (24.149%))
 Logic Levels: 2 (FDRE=1 OBUF=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
SLICE_X0Y15	FDRE	0.000	0.000	r out_reg[2]/C
SLICE_X0Y15	FDRE (Prop_fdre_C_Q)	0.141	0.141	r out_reg[2]/Q
	net (fo=4, routed)	0.428	0.569	out_OBUF[2]
U19			r out_OBUF[2]_inst/I	
U19	OBUF (Propobuf_I_O)	1.202	1.771	r out_OBUF[2]_inst/O
	net (fo=0)	0.000	1.771	out[2]
U19			r out[2] (OUT)	

Slack: inf
 Source: out_reg[3]/C
 (rising edge-triggered cell FDRE)
 Destination: out[3]
 (output port)
 Path Group: (none)
 Path Type: Min at Fast Process Corner
 Data Path Delay: 1.778ns (logic 1.351ns (75.978%) route 0.427ns (24.022%))
 Logic Levels: 2 (FDRE=1 OBUF=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
SLICE_X0Y15	FDRE	0.000	0.000 r out_reg[3]/C	
SLICE_X0Y15	FDRE (Prop_fdre_C_Q) net (fo=3, routed)	0.141 0.427	0.141 r out_reg[3]/Q 0.568 out_OBUF[3]	
V19			r out_OBUF[3]_inst/I	
V19	OBUF (Propobuf_I_O) net (fo=0)	1.210 0.000	1.778 r out_OBUF[3]_inst/O 1.778 out[3]	
V19			r out[3] (OUT)	

Design source code

```
else if(mode && Load)
begin
    out <= Y;
end
else if (mode && !Load && (out == X))
begin
    out <= out;
end
else if(mode && !Load)
begin
    out <= out - 1;
end
else
begin
    out <= 4'bX;
end
end

endmodule
```