University of Central Florida

Department of Computer Science

CDA 5106: Fall 2022

Machine Problem 1: Cache Design, Memory Hierarchy Design

by

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Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

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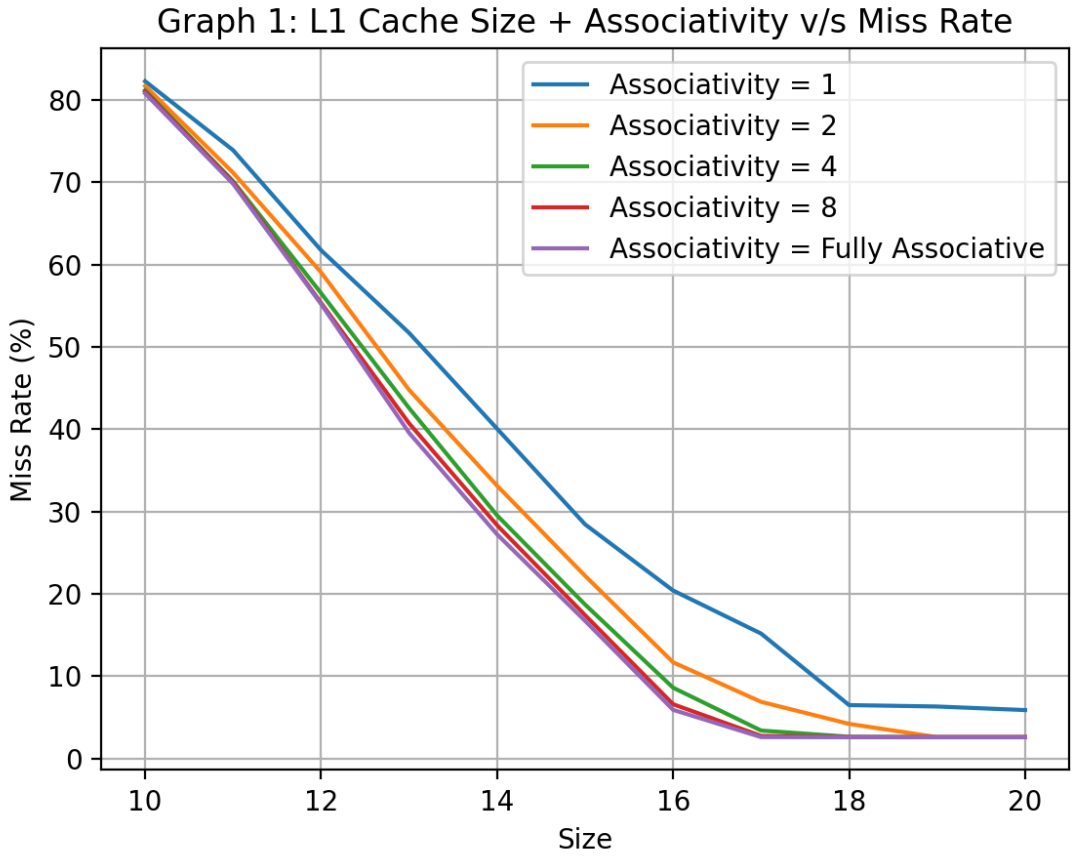
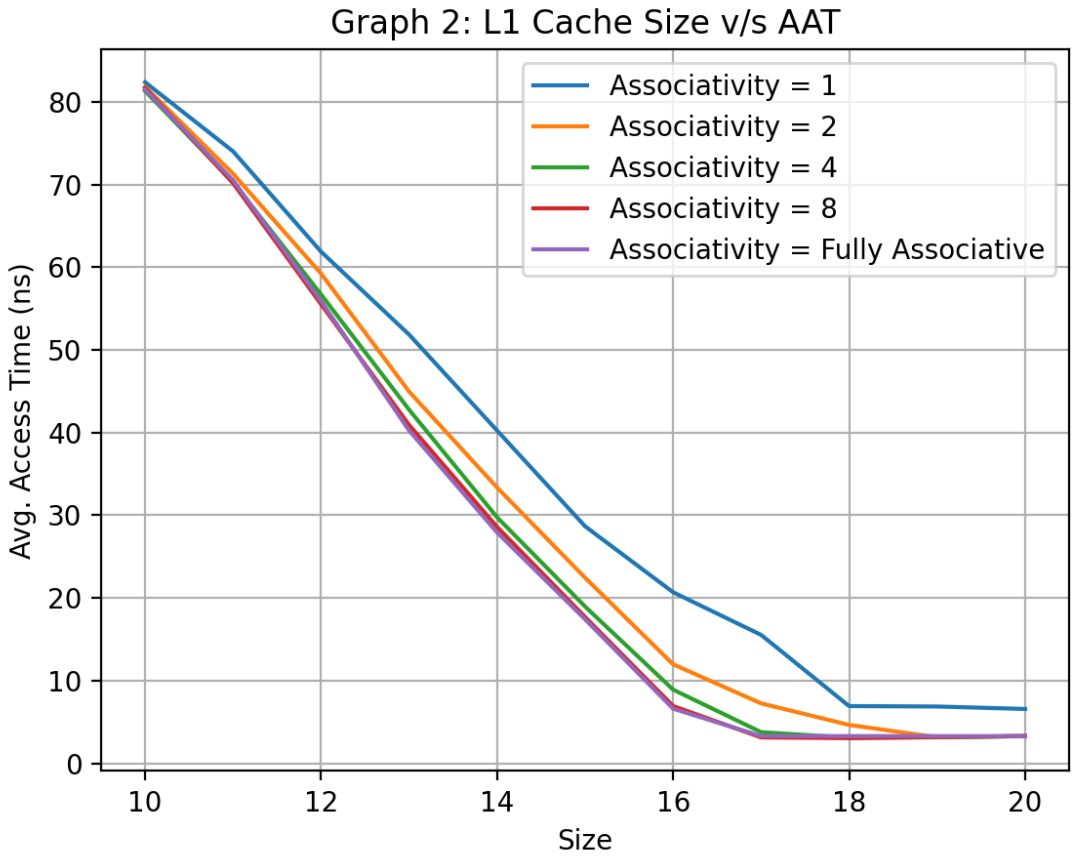
1. *L1 cache exploration: SIZE and ASSOC*

- The L1 miss rate falls as cache capacity grows (regardless of associativity). Furthermore, increasing cache associativity reduces the L1 miss rate, though not as dramatically as increasing the cache size. The gap in associativity between assoc-8 and assoc-FA will grow as cache size grows.



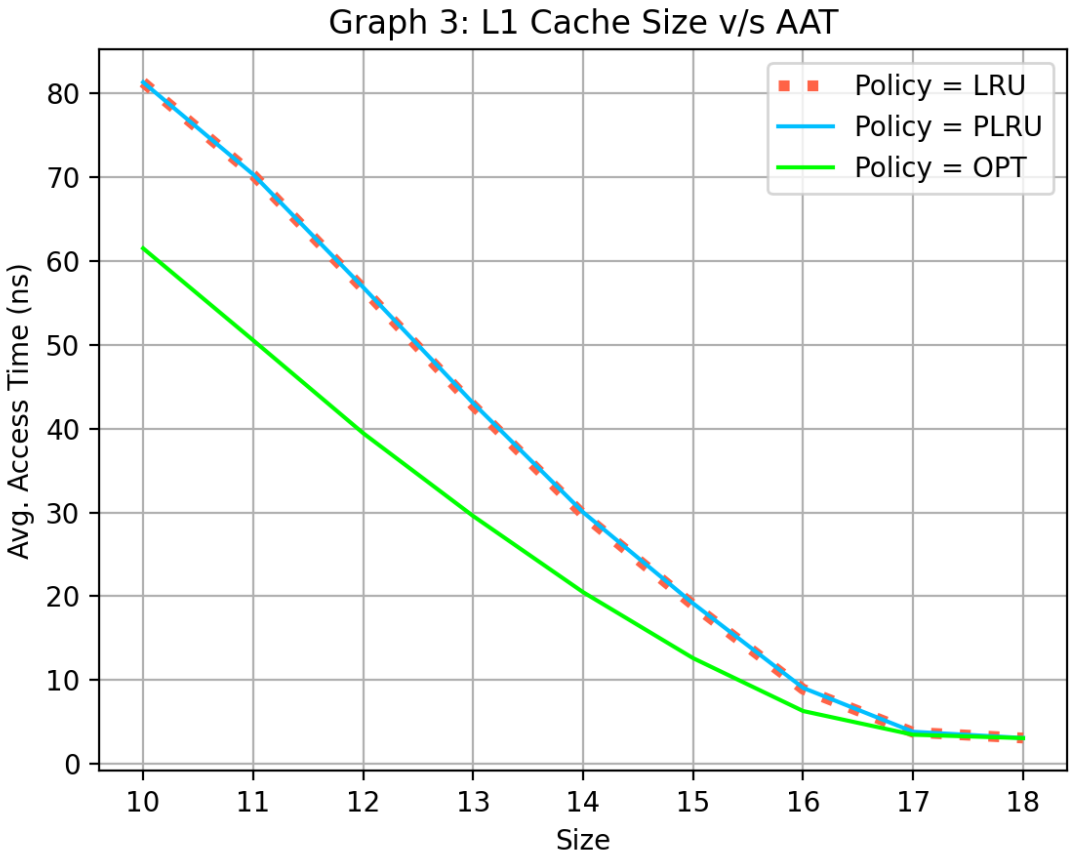
2. *L1 cache exploration: SIZE and ASSOC*

- The fully-associative cache would be the best feasible cache configuration to choose given the parameters depicted (provided others, such as block size, remain constant) based on the graph's trends though an 8-way set associative cache is nearly as good.



3. *Replacement Policy*

- No doubt Optimal policy has the best performance with AAT being far lower than that of Pseudo LRU and LRU. Of course, the cache with the highest size is the best performer. This makes sense because this policy ensures that the block that will not be needed for the longest (or ever) is replaced.



4. *Inclusion Property*

- Initially, the non-inclusive has a lower AAT than inclusive but as the cache size increases the gap between them becomes negligible. This could be due to that inclusive property works better in systems having multiple caches The below graph depicts this for 2 level caches, i.e., L1 and L2.