SRI MANAKULA VINAYAGAR ENGINEERING COLLEGE
(An Autonomous Institution)
(Approved by AICTE, New Delhi & Affiliated to Pondicherry University)
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Accredited by NAAC with “A” Grade)
Madagadipet, Puducherry - 605 107

BASIC ELECTRICAL AND ELECTRONICS ENGINEERING

PART-B
ELECTRONICS

TRANSISTORS

UNIT 5 Transistors

Bipolar Junction Transistor:

- NPN and PNP transistors-construction and operation
- CB, CE and CC configurations
- Transistor characteristic
- Biasing

Field Effect Transistor:

- **JFET** : Drain and transfer characteristics
- Comparison between JFET and BJT
- **MOSFET**
  - Types and characteristics

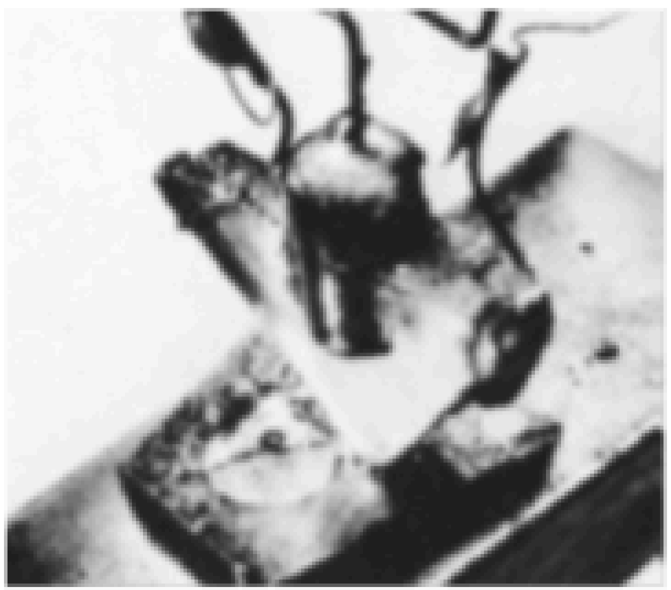
Course Outcome

- *After completion of the course, the students will be able to*

Apply CB, CE and CC Configurations of BJT in applications like isolator, amplifier and voltage follower circuit respectively

The Invention

The First Transistor : On **Dec 23, 1947**, three scientists led by Dr. William Shockley at the Bell Telephone Laboratories demonstrated the amplifying action of the first transistor. (Courtesy Bell Telephone Laboratories.)



Co-inventors:

Dr. William Shockley (seated);

Dr. John Bardeen (left);

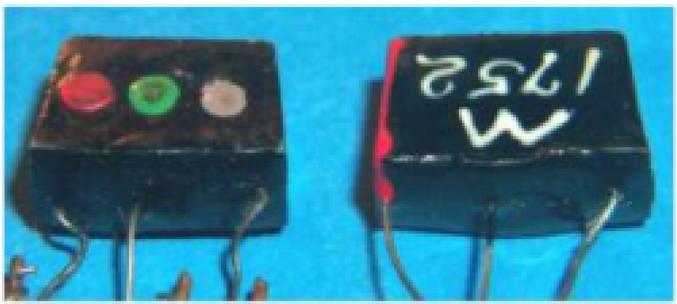
Dr. Walter H. Brattain.

Honored with Nobel Prize in Physics in 1956

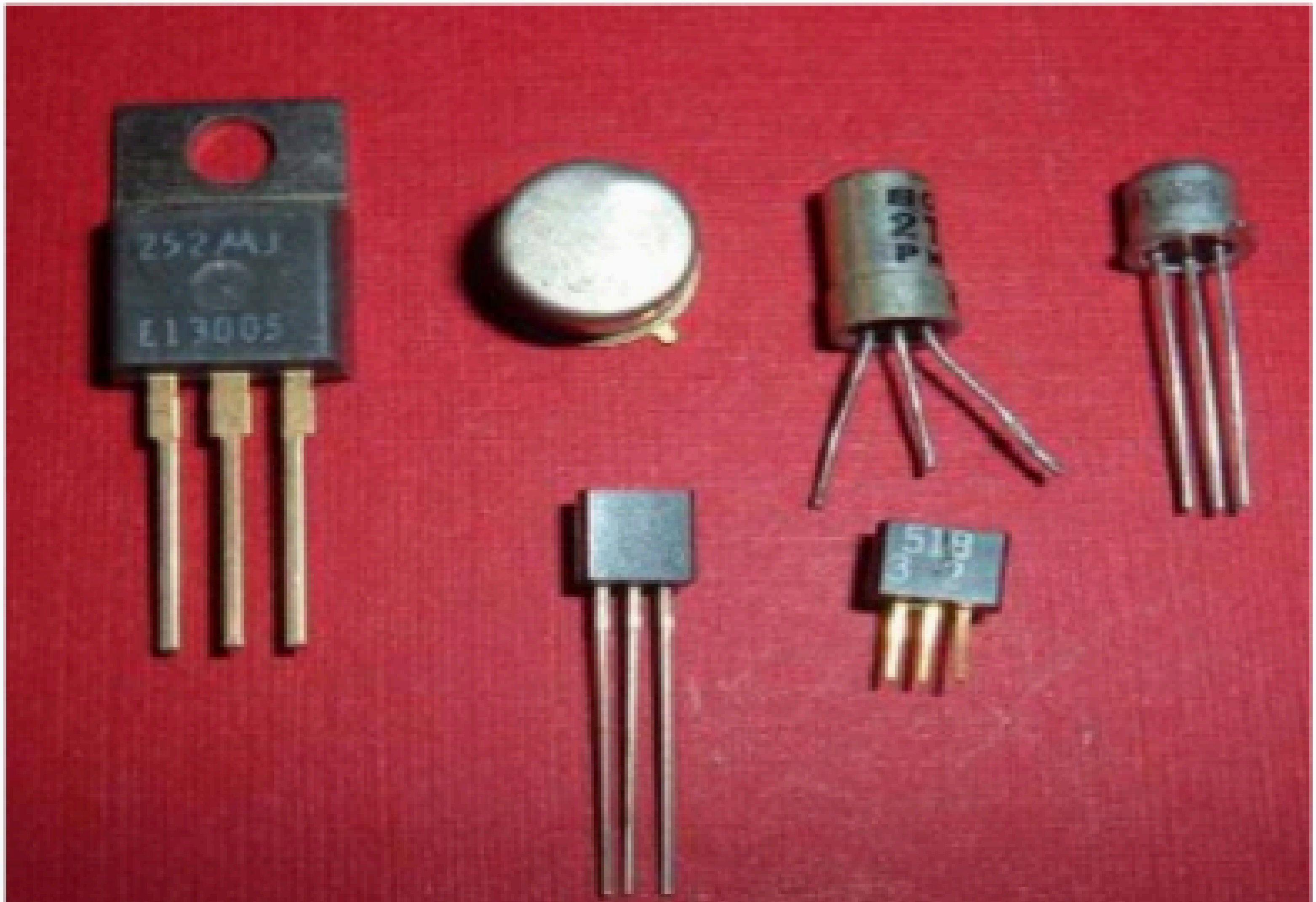
Important Features (compared to Vacuum tubes):

TRANSISTOR RADIO

The First BJT



Transistor Size (3/8”L X 5/32”W X 7/32”H)
No Date Codes. No Packaging.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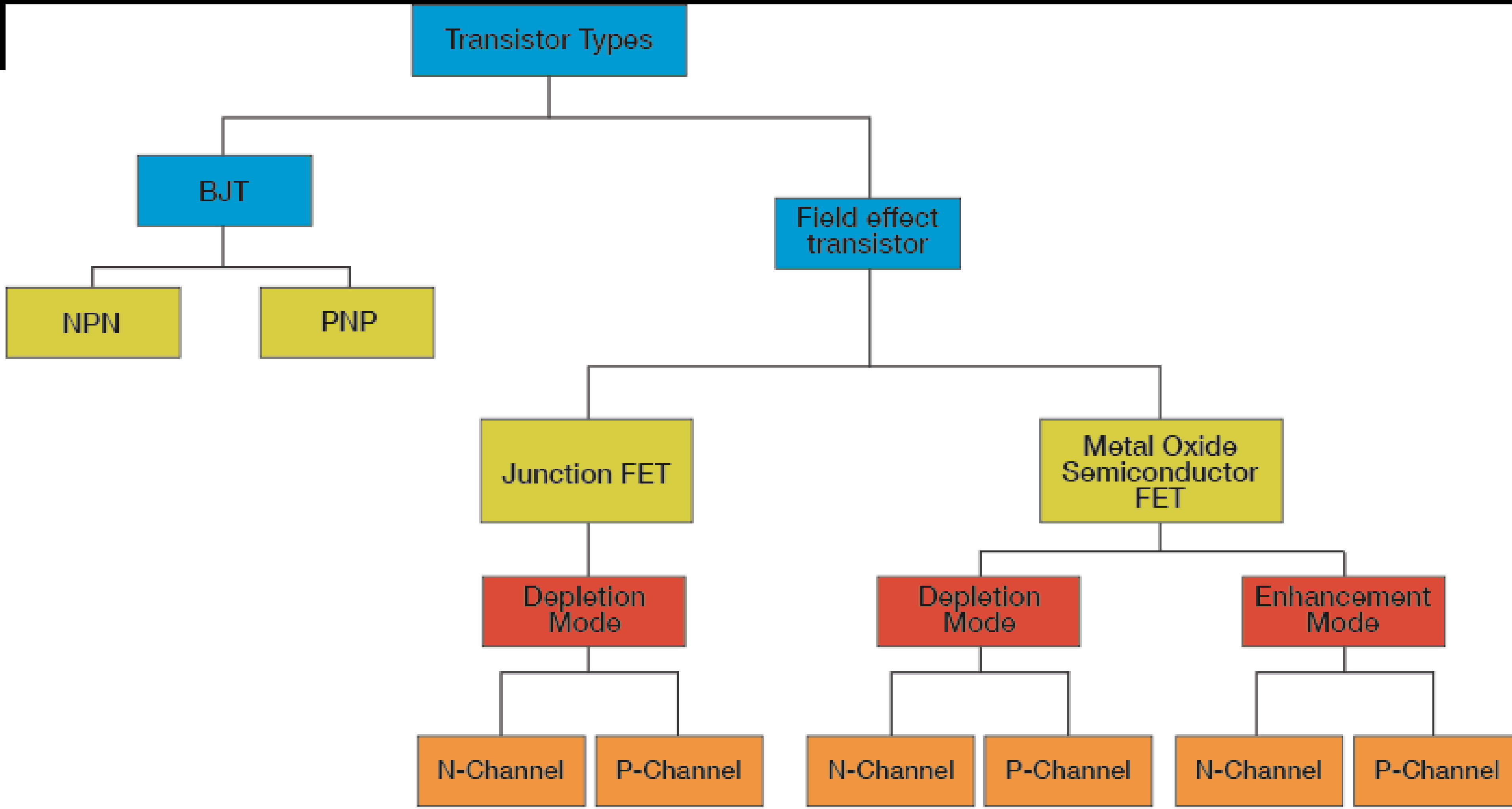
Transistor

- A transistor is a device that can be used as either an amplifier or a switch. Transistor is current controlling device.



Transistor Types
BJT
Field effect transistor
NPN
PNP
Junction FET
Metal Oxide Semiconductor FET
Depletion Mode
Depletion Mode
Enhancement Mode
N-Channel
P-Channel
N-Channel
P-Channel
N-Channel
P-Channel

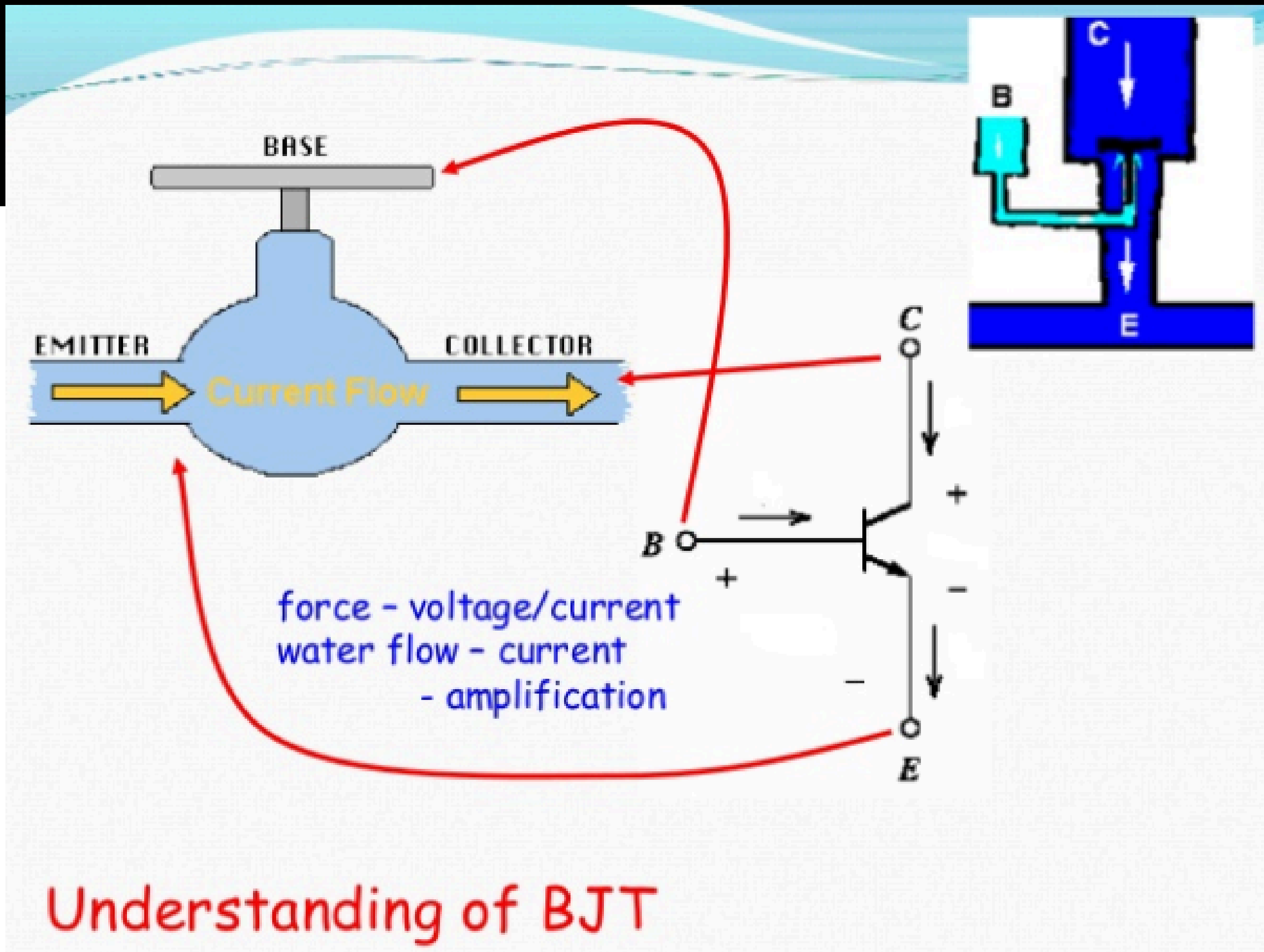
Bipolar Junction transistor

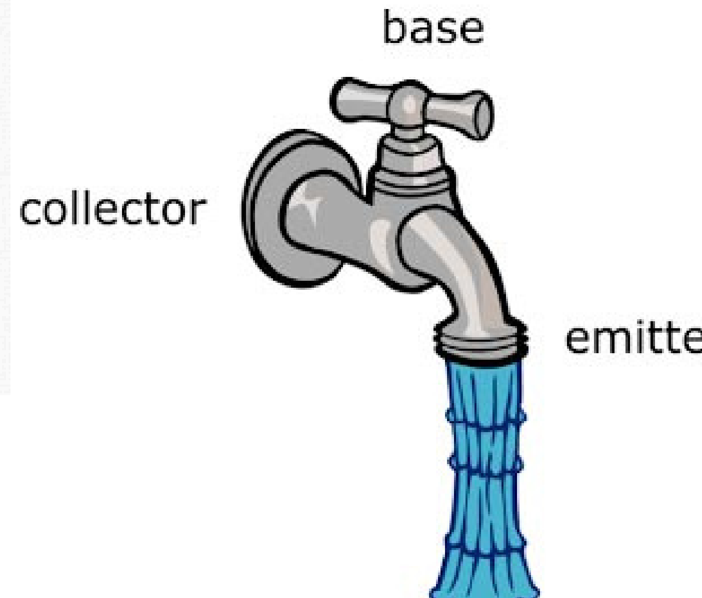
Holes and electrons determine device characteristics

Three terminal device

Control of two terminal currents

Amplification and switching through 3rd contact


BASE
EMITTER
COLLECTOR
Current Flow
C
B
E
force - voltage/current
water flow - current
- amplification
Understanding of BJT


base
collector
emitte

Transistor paramaters :

- **transistor current** – current flowing across the collector **(I_E , I_C , I_B)**

- **alpha** - the ratio of the dc collector current to the dc emitter current;
  almost equal to but slightly less than 1 **(I_E / I_C)**

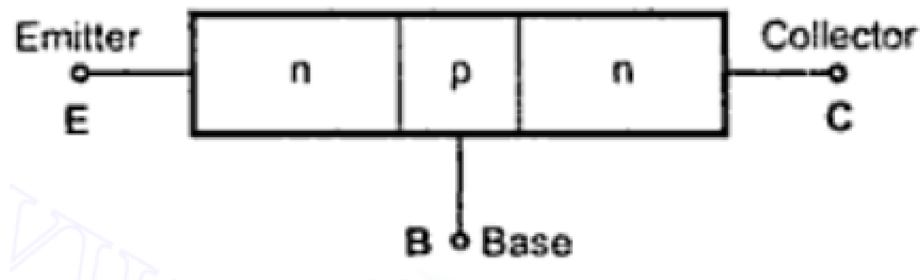
- **beta** – ratio of the dc collector current to the dc base current;
  also known as current gain of transistor **(I_C / I_B)**

- **current rating** – maximum current a transistor can pass through its collector and emitter **(I_{cmax})**

- **voltage rating** – maximum voltage that can be applied across the
  collector to emitter terminals of a transistor **(V_{cmax})**

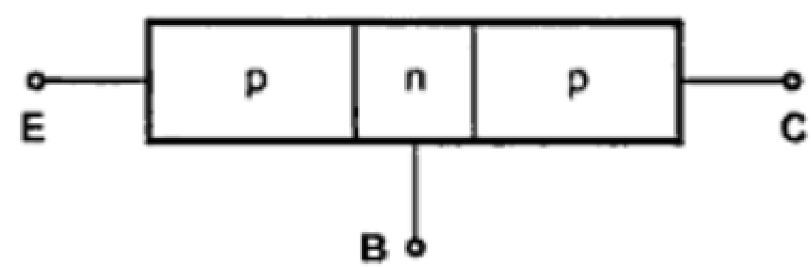
Types of Bipolar Junction Transistor

- Two types:
  - n-p-n type
  - P-n-p type



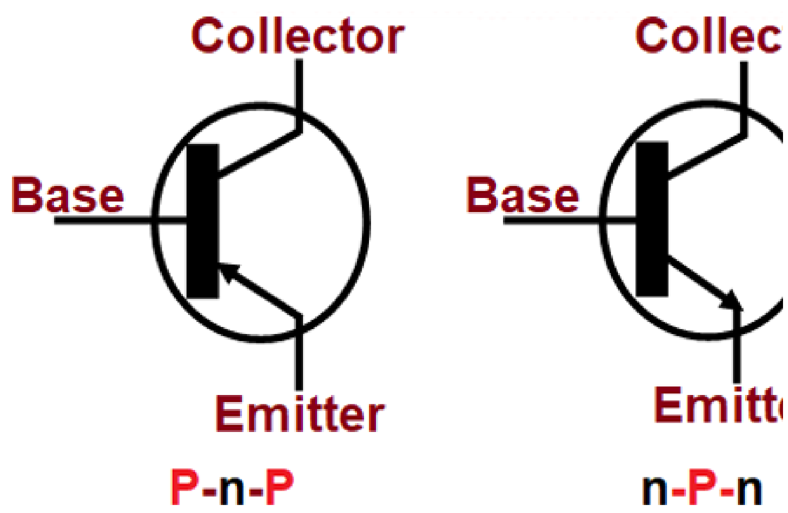
(a) n-p-n

- Construction:
  - Base region is very thin and lightly doped
  - Emitter region is heavily doped
  - Collector region is moderately doped

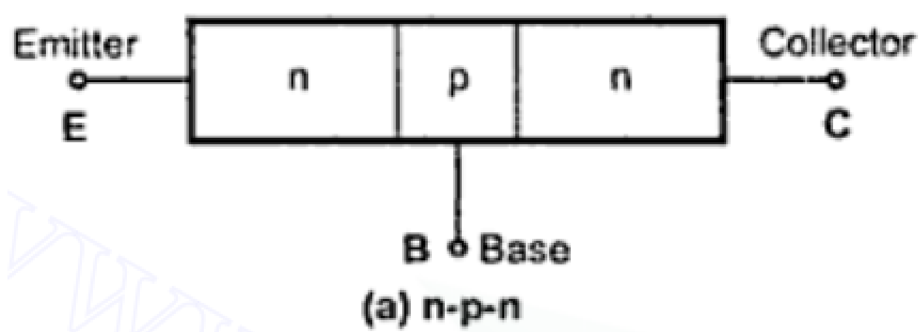


(b) p-n-p

Symbol of BJT

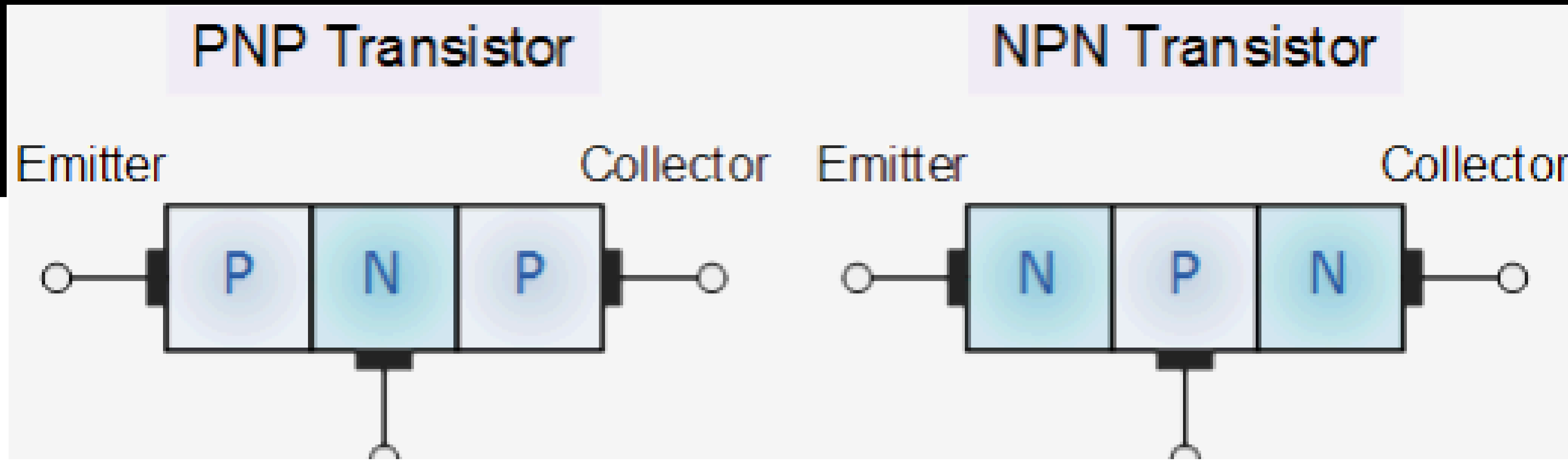


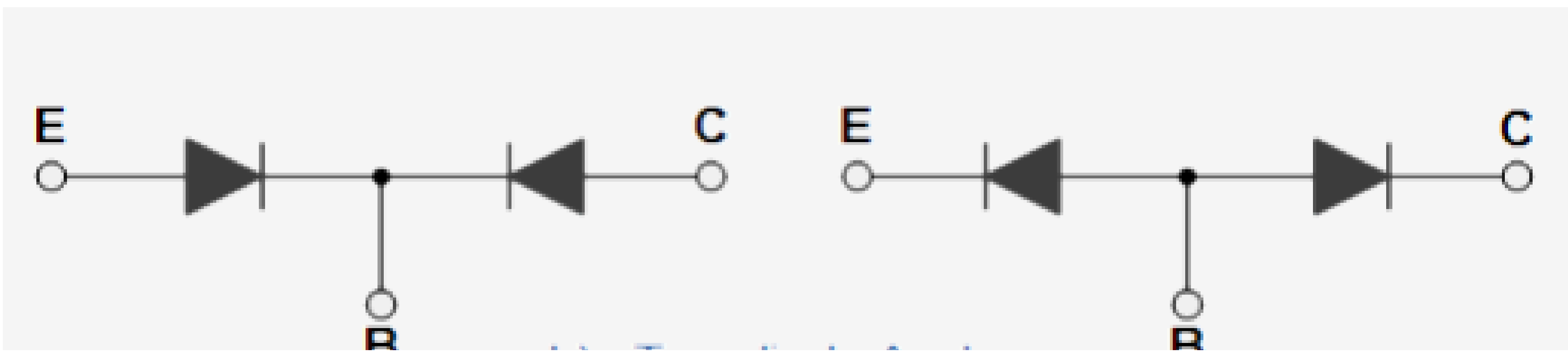
TRANSISTOR-
3 terminal device
2 junction
3 layer

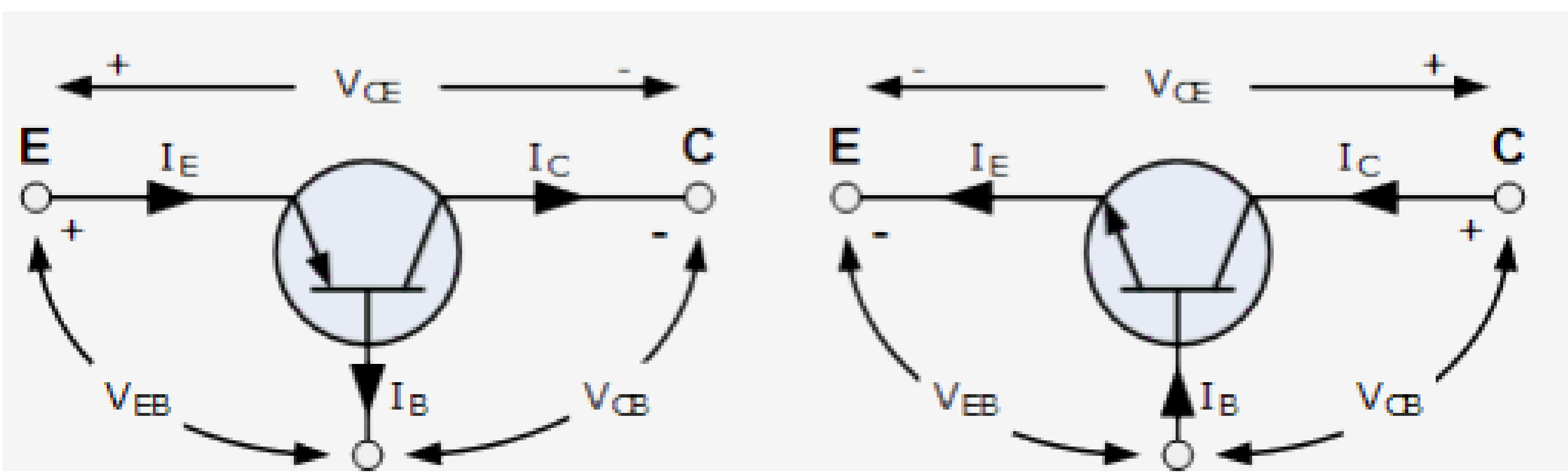


Difference between NPN and PNP

- In NPN transistor the **majority carriers are Electrons** and **minority carriers are holes**.
- In PNP transistor the **majority carriers are Holes** and **minority carriers are electrons**.
- The **main difference between NPN and PNP transistor** is the use of proper biasing (Making transistor power ON).


PNP Transistor
NPN Transistor
Emitter
Collector
P
N
P
Emitter
Collector
N
P
N


E
C
E
C


+
VCE
-
E
IE
IC
C
+
-
VEB
IB
VCB
-
VCE
+
E
IE
IC
C
-
+
VEB
IB
VCB

Naming of Transistor Terminals

1) <u>Emitter:</u>

- The section of one side that supplies carriers is called emitter.
- Emitter is always forward biased with respect to base so it can supply carrier.
- For “npn transistor” emitter supply holes to its junction.
- For “pnp transistor” emitter supply electrons to its junction.

Naming of Transistor Terminals

2) Collector:

- The section on the other side that collects carrier is called collector.
- The collector is always reversed biased with respect to base.
- For “npn transistor” collector receives holes to its junction.
- For “pnp transistor” collector receives electrons to its junction.

Naming of Transistor Terminals

3) Base:

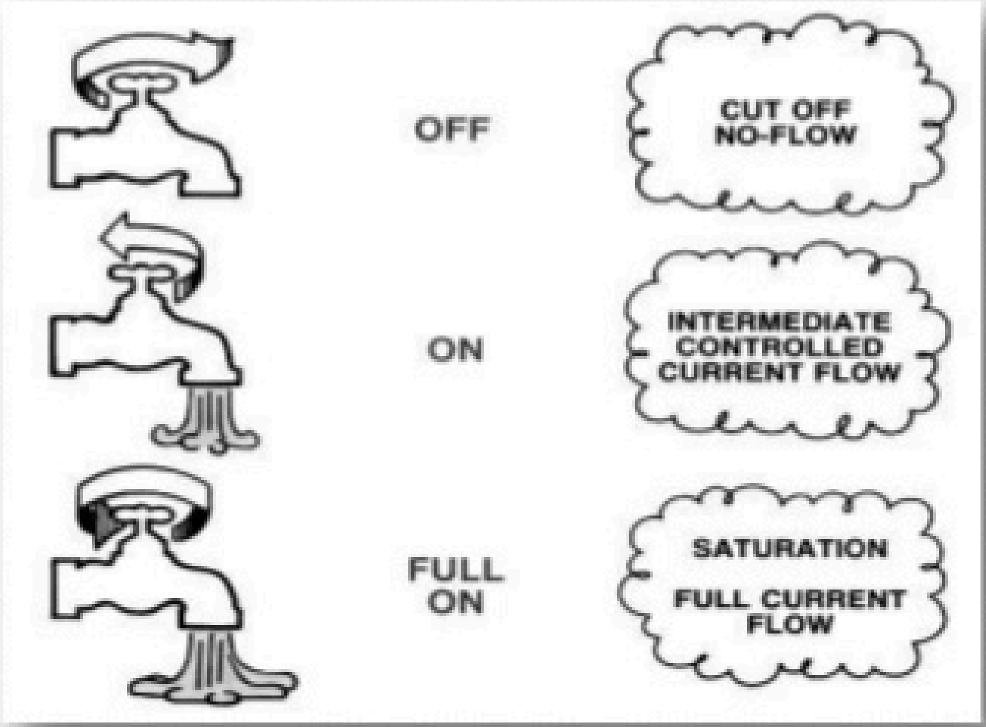
The middle section which forms two pn junction between emitter and collector is called Base.

Operating regions of BJT

Cut off region

Linear region

Saturation region



Transistor Working:(Biasing)

- In order to operate properly as amplifier, it is necessary tc correctly bias the two pn junctions with external voltages
- Depending upon the external bias voltage polarities used, the transistor works in one of the three regions
  - Active Region
  - Cut-Off Region
  - Saturation Region

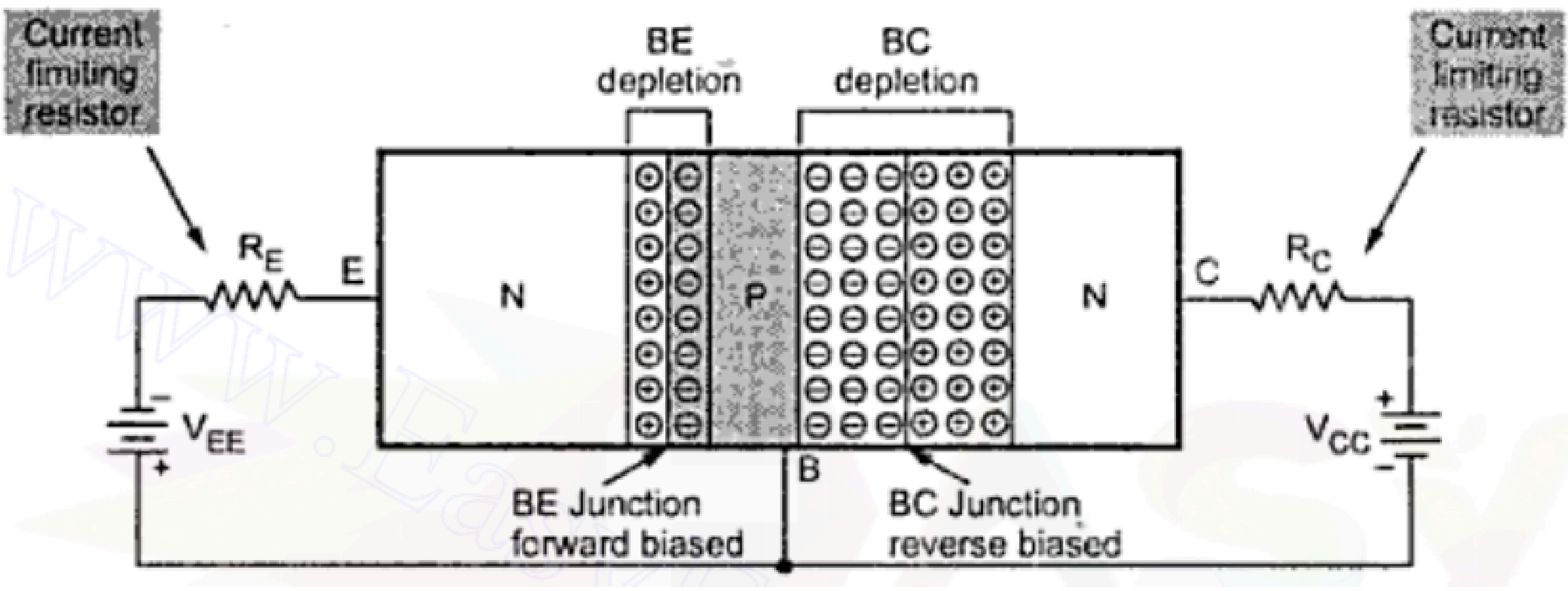
Region	Emitter base junction	Collector base junction
Active	Forward biased	Reverse biased
Cut-off	Reverse biased	Reverse biased
Saturation	Forward biased	Forward biased

BJT operation

- Operation of **NPN** transistor is discussed here

- For normal operation (amplifier application)
- – EB junction should be forward biased
- – CB junction should be reverse biased

- Depletion width at EB junction is narrow (forward bia
- Depletion width at CB junction is wide (reverse biase

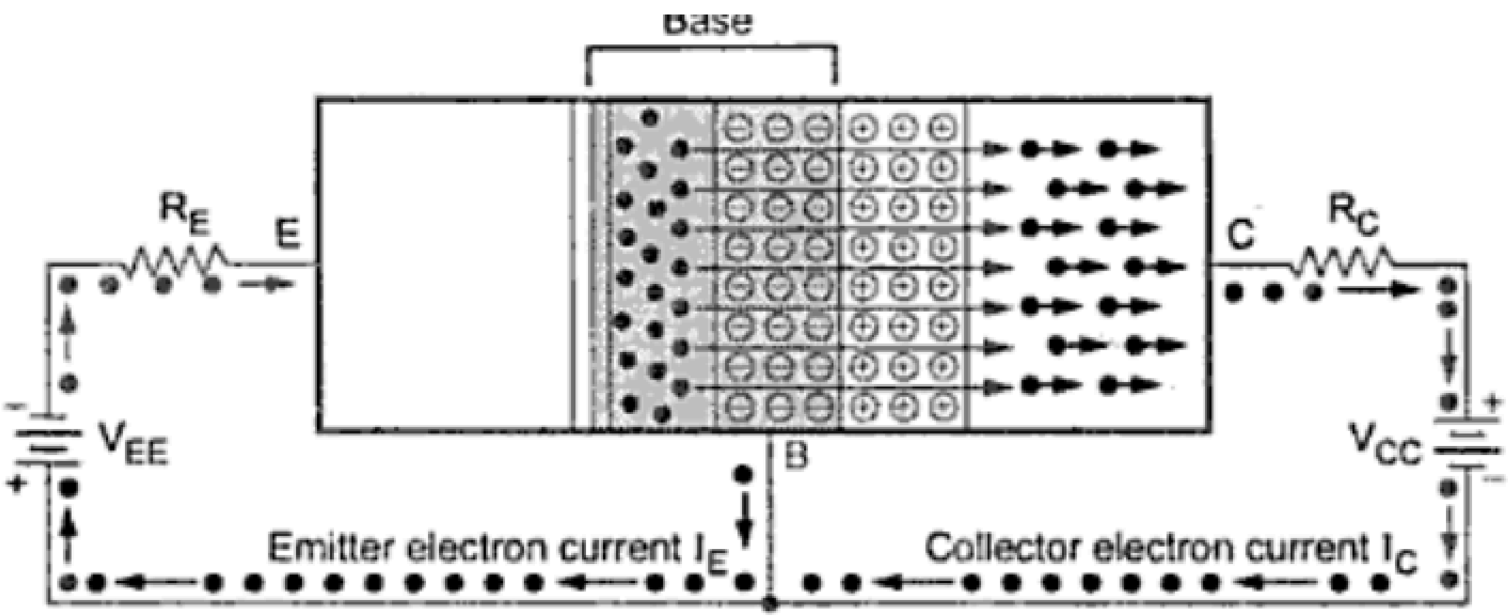


Working of NPN transistor

- When EB junction is forward biased, free electrons fro
emitter region drift towards base region
- Some free electrons combine with holes in the base to form small base current
- Inside the base region (p-type), free electrons are minority carriers. So most of the free electrons are swe
away into the collector region due to reverse biased CE
junction

Working of NPN transistor

- The FB – EB junction causes the e- in the N-type emitter to flow towards the base
- This constitutes the emitter current Ie
- As these electrons flow through the p-type they tend to combine with the holes in p-region (Base)



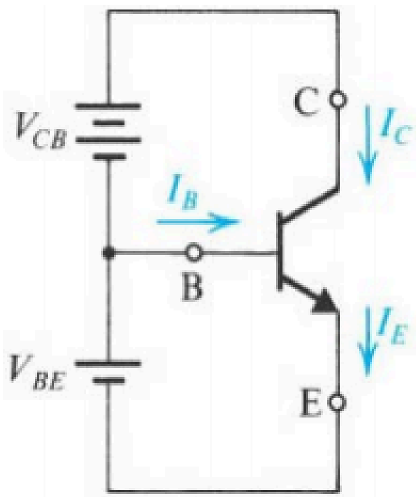
NPN Transistor Operation

1) Working of npn transistor:

- As this electrons flow toward p-type base, they try to recombine with holes. As base is lightly doped only few electrons recombine with holes within the base.
- These recombined electrons constitute small base current.
- The remainder electrons crosses base and constitute collector current.

$$I_E = I_B + I_C$$

NPN transistor operating mode



$$i_E = i_C + i_B$$

$$v_{CE} = v_{CB} + v_{BE}$$

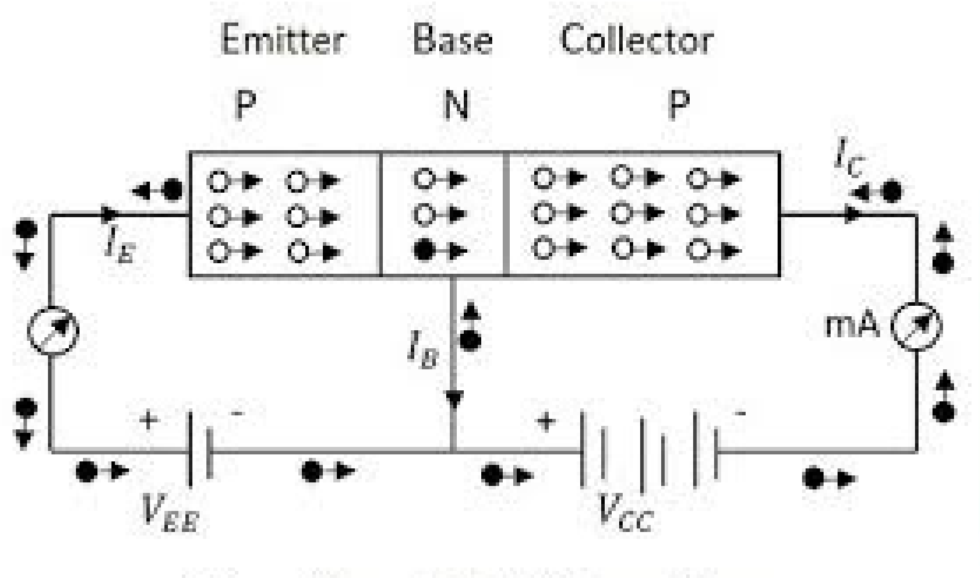
Forward-Active Mode
EBJ forward bias ($V_{BE} > 0$)
CBJ reverse bias ($V_{BC} < 0$)

Mode	V_{BE}	V_{BC}
Forward-Active	> 0	< 0
Reverse-Active	< 0	> 0
Cutoff	< 0	< 0
Saturation	> 0	> 0

← Not Useful!

Transistor Operation

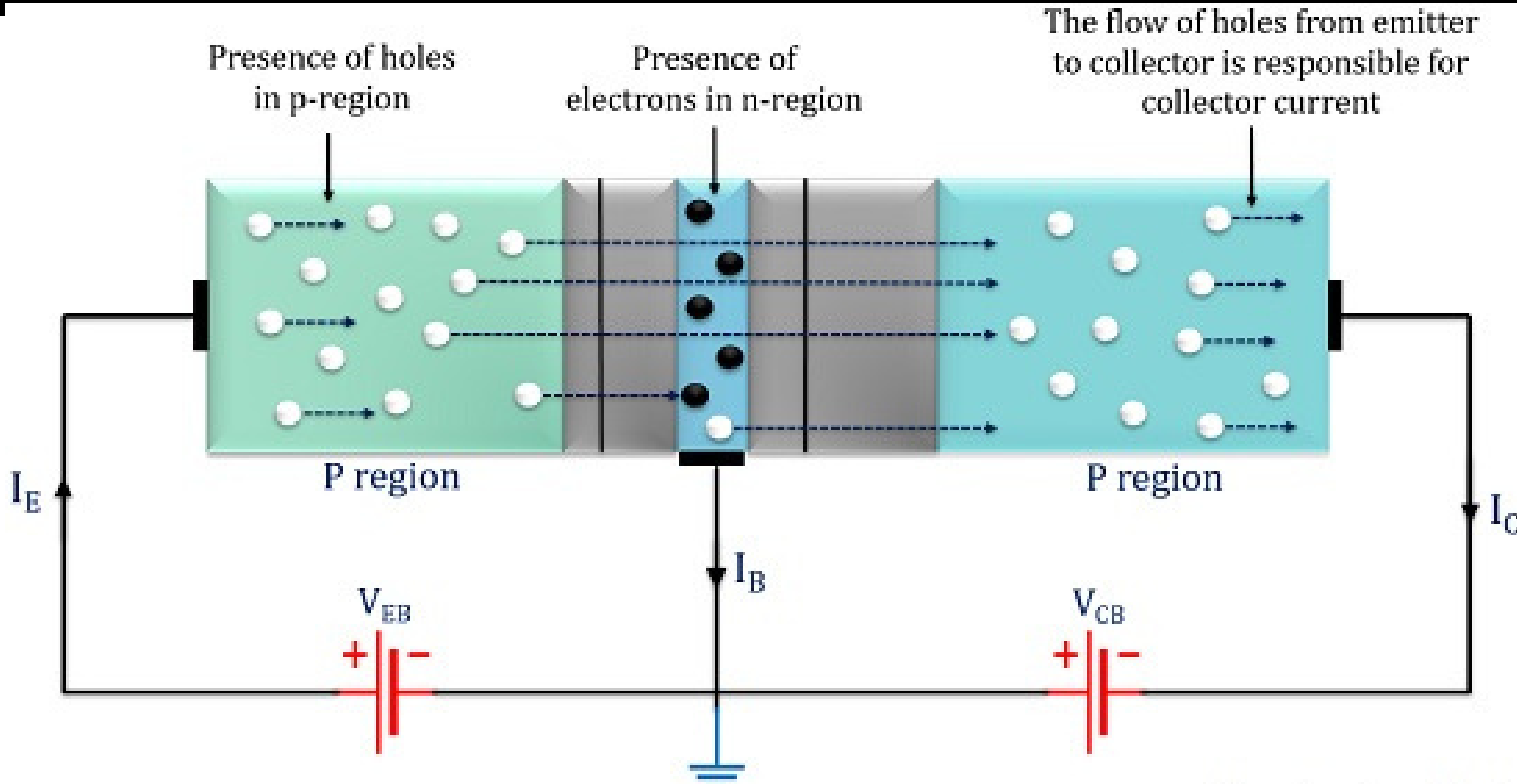
1. Working of pnp transistor:



Operation of a PNP transistor

- Forward bias is applied to emitter-base junction and reverse bias is applied to collector- base junction.

- The forward bias in the emitter-base junction causes holes to move toward base. This


Presence of holes in p-region
Presence of electrons in n-region
The flow of holes from emitter to collector is responsible for collector current
P region
P region
I_E
I_B
I_C
V_{EB}
V_{CB}
+
−
+
−

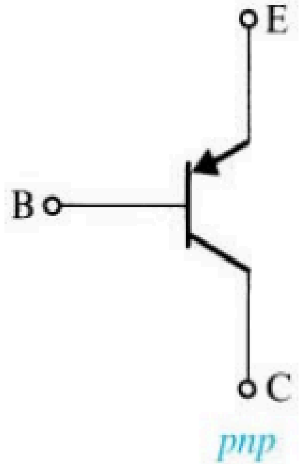
Transistor Operation

2) Working of pnp transistor:

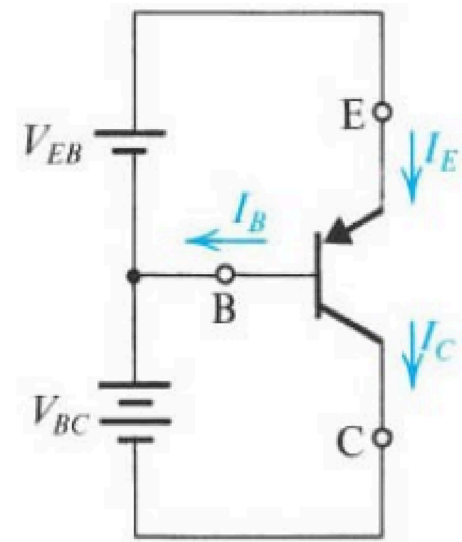
- As this holes flow toward n-type base, they try to recombine with electrons. As base is lightly doped only few holes recombine with electrons within the base.
- These recombined holes constitute small base current.
- The remainder holes crosses base and constitute collector current.

The PNP Transistor

pnp



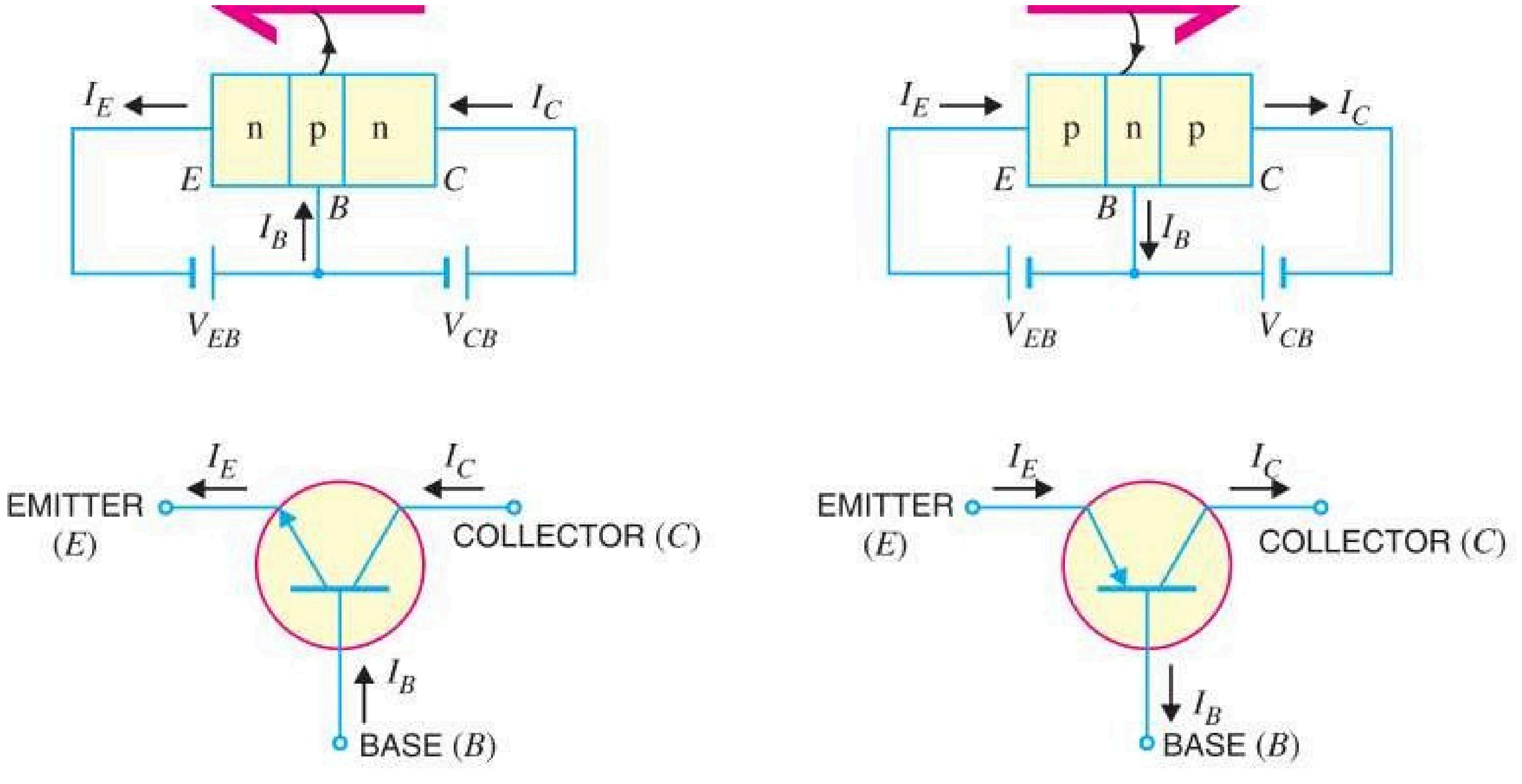
(b)



Mode	V_{EB}	V_{CB}
Forward-Active	> 0	< 0
Reverse-Active	< 0	> 0
Cutoff	< 0	< 0
Saturation	> 0	> 0

Not Useful!

Transistor Symbol in active mode



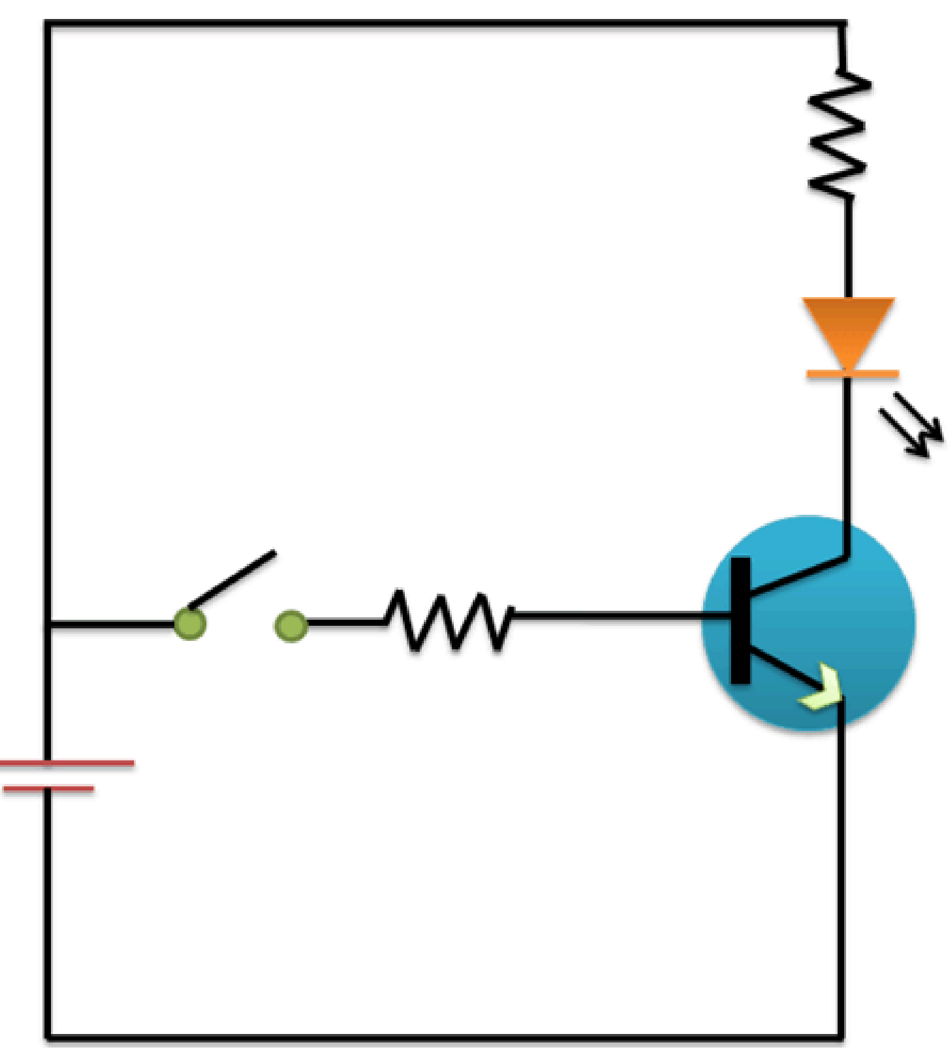
Some important factors to be remembered-

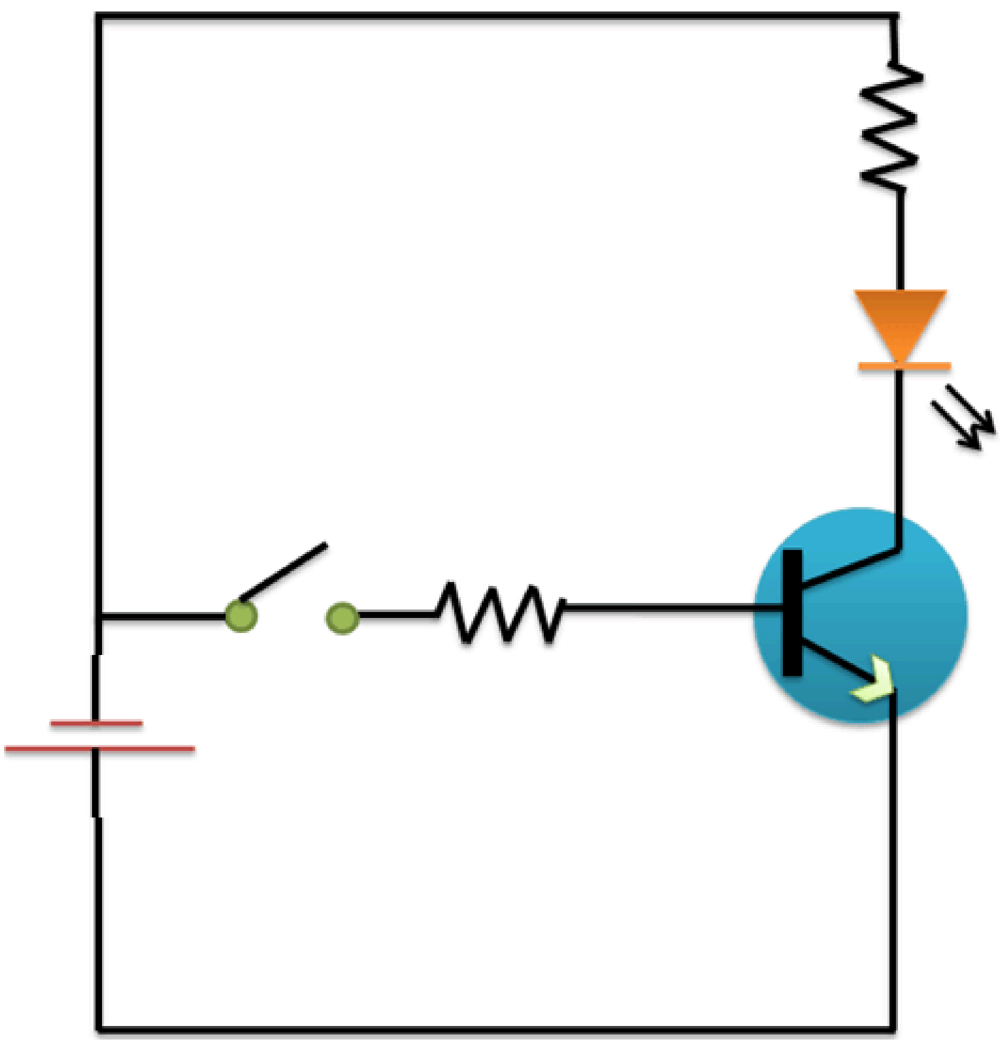
- The transistor has three region named emitter, base and collector.
- The Base is much thinner than other region.
- Emitter is heavily doped so it can inject large amount of carriers into the base.
- Base is lightly doped so it can pass most of the carrier to the collector.
- Collector is moderately doped.

Some important factors to be remembered-

- The junction between emitter and base is called emitter-base junction(emitter diode) and junction between base and collector is called collector-base junction(collector diode).
- The emitter diode is always forward biased and collector diode is reverse biased.
- The resistance of emitter diode is very small(forward) and resistance of collector diode is high(reverse).

When will LED blow





WHY BIASING?

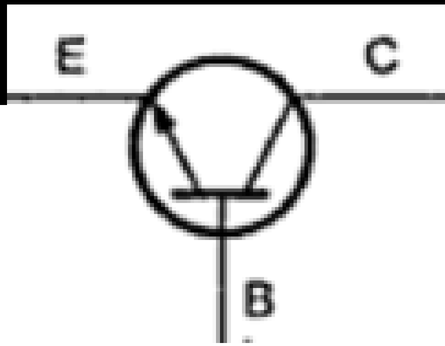
If the transistor is not biased properly, it would work inefficier produce distortion in output signal.

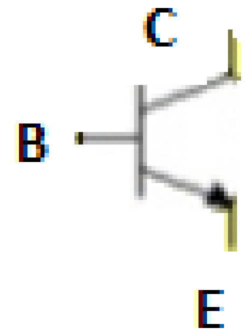
HOW A TRANSISTOR CAN BE BIASED?

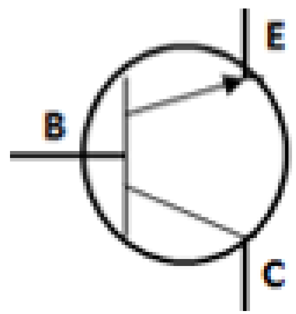
A transistor is biased either with the help of battery or assoc circuit with the transistor. The later method is more efficient frequently used. The circuit used for transistor biasing is cal biasing circuit.

BJT Configurations:

- Depending upon the input given and the output taken- the transistor can be connected in three configurations
- So, One terminal must be common
  - Common Base (CB)
  - Common Emitter (CE)
  - Common collector (CC)


E
C
B


C
B
E


E
B
C

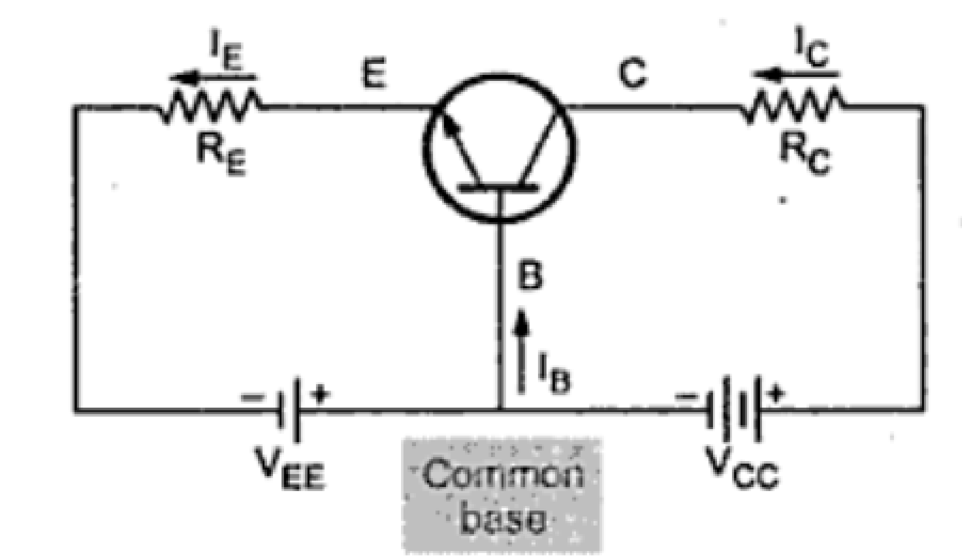
Common-Base Configuration

- Common-base terminology is derived from the fact that the :

  - base is common to both input and output of the configuration.

  - base is usually the terminal closest to or at ground potential.

- All current directions will refer to conventional (hole) flow and the arrows in all electronic symbols have a direction defined by this convention.
- Note that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch.



- In this configuration – Input is applied between emitter and base
- Output is taken from the collector and base
- Hence base terminal is common

Common Base Configuration

Current gain in CB configuration

- **Common base DC current gain:**

$$\text{DC Current Gain} = \frac{\text{Output Current}}{\text{Input Current}} :$$

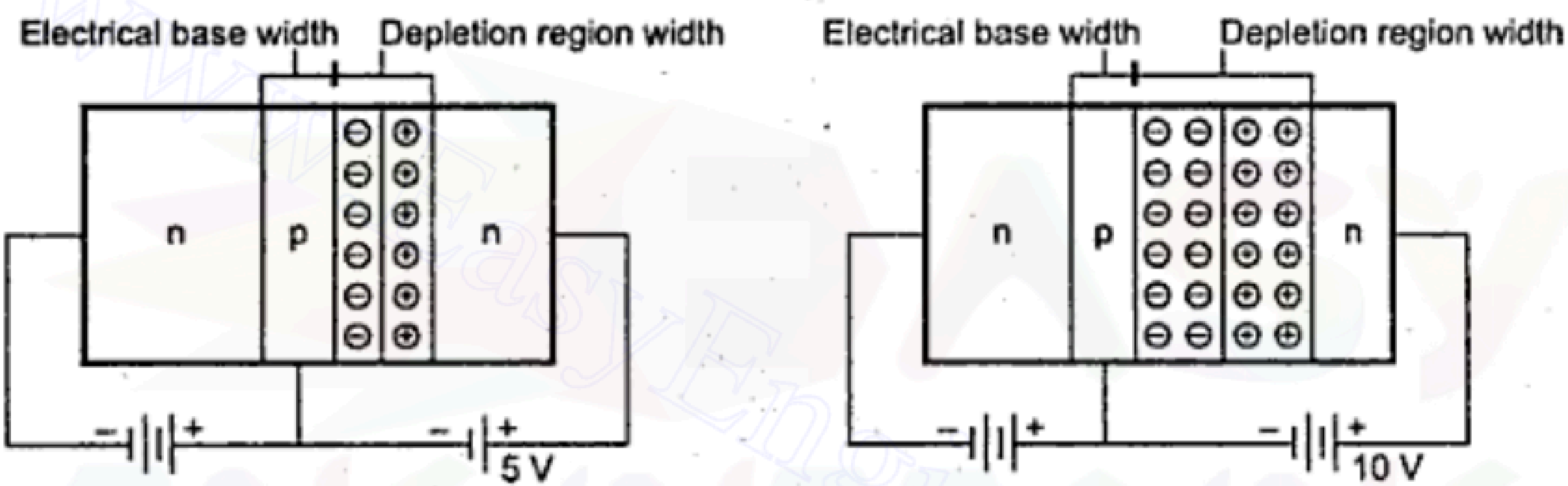
$$\frac{I_C}{I_E} = \alpha$$

Con rrent gain:

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

CB_Input Conf._Observation

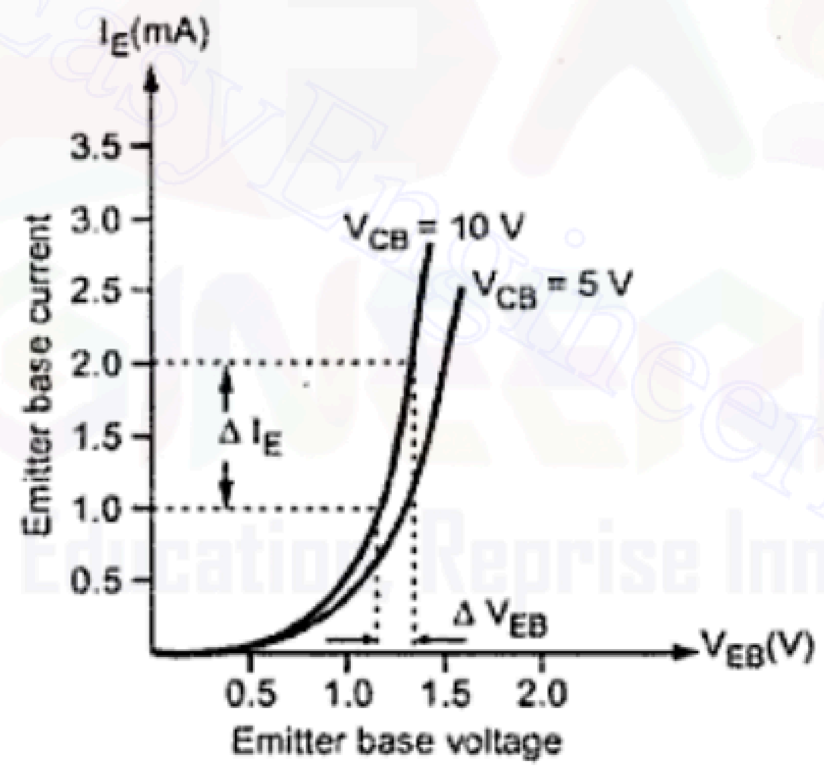
- After cut-in voltage (barrier potential), Ie increases rapidly with small change in Veb – It means the input resistance is very small
- There is slight increase in emitter current (Ie) with increase in Vcb – This is due to change in width of the depletion region in the base region under reverse biased condition – (Early effect / Base width modulation)



CB_Characteristics

- The relation between Voltages and Currents are represented graphically to known about the electrical behaviour of the transistor (is called Characteristics)
- Input and Output characteristics

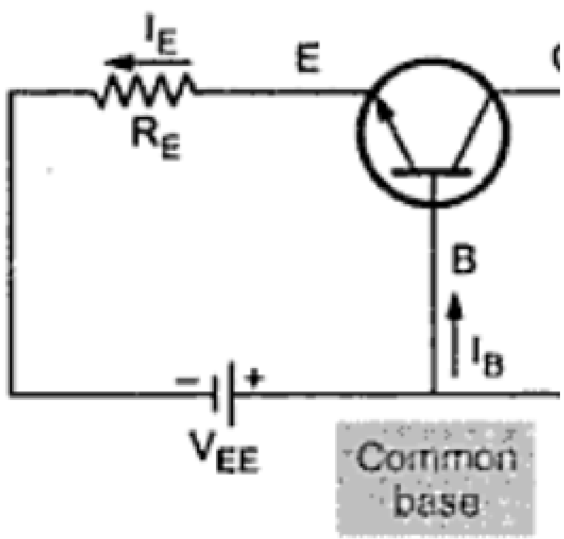
- CB_Input Characteristics:
  - curve between Ie and Veb at constant Vcb
  - Ie is taken in Y-axis
  - Veb is taken in X-axis

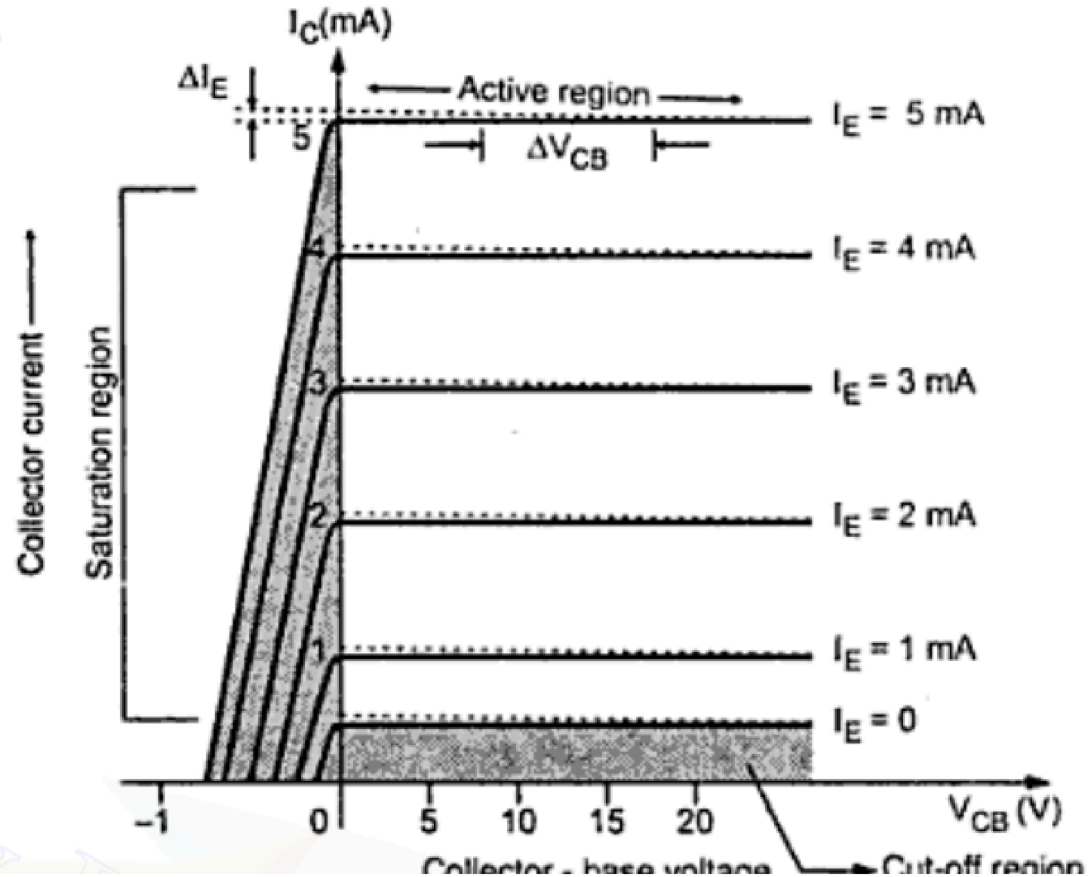


Input characteristics of transistor in CB configu

CB_Output Characteristics:

- Curve between Ic ad Vcb at constant Ie
- Take Ic is the Y-axis
- Vcb in X-axis





CB_Ouput Conf._Observation

- The output characteristics has three regions:

State	Emitter base junction	Collector base junction
Active	Forward biased	Reverse biased
Cut-off	Reverse biased	Reverse biased

- In active region – Ic is approximatey equal to the Ie and the transistor works as an amplifier
- If the emitter current is zero, the collector current is Icb0 (i.e.Leakage current)
- So, the region below the curve Ie=0 is known as the cut-off region
- Characteristics left of Vcb=0 is the saturation region – As Vcb increases – Ic increases exponentially towards zero
- Ic depends upon Ie (not Vc) – therefore input current drives the output current – So, transistor in CB is current operating device

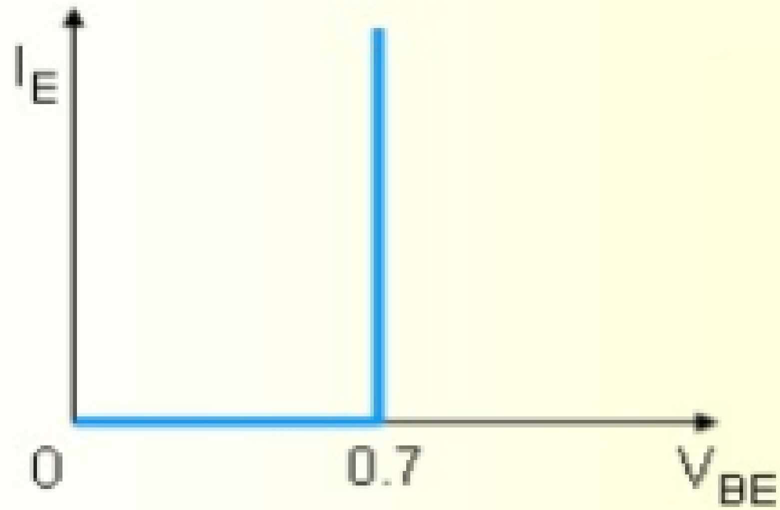
Active region	Saturation region	
• I_E increased, I_C increased • BE junction forward bias and CB junction reverse bias • Refer to the graf, $I_C \approx I_E$ • I_C not depends on V_{CB} • Suitable region for the transistor working as amplifier	• BE and CB junction is forward bias • Small changes in V_{CB} will cause big different to I_C • The allocation for this region is to the left of V_{CB} = 0 V.	• Re line • BE reve • no at c leak

- The curves (output characteristics) clearly indicate that a first approximation to the relationship between IE and IC in the active region is given by

$$I_C \approx IE$$

- Once a transistor is in the 'on' state, the base-emitter voltage will be assumed to be

$$V_{BE} = 0.7V$$

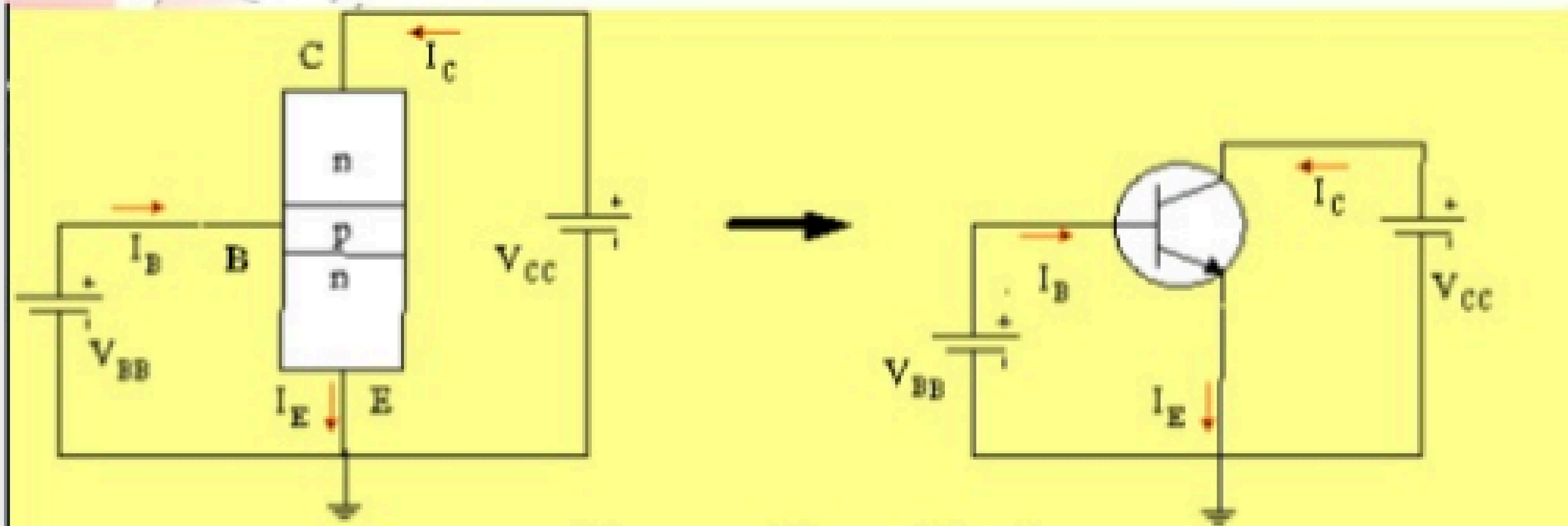


Common-Emitter Configuration

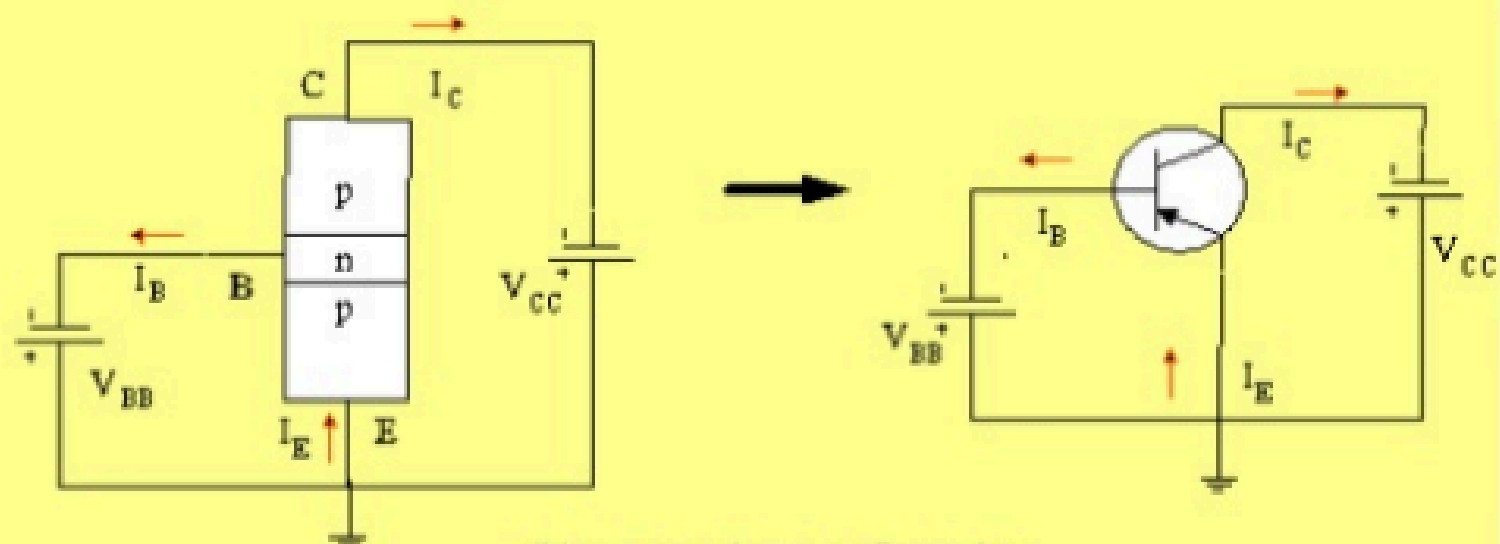
- It is called common-emitter configuration since :
  - emitter is common or reference to both input a
    output terminals.
  - emitter is usually the terminal closest to or at
    ground

    potential.
- Almost amplifier design is using connection of CE
  to the high gain for current and voltage.
- Two set of characteristics are necessary to descri
  the behavior for CE ;input (base terminal) and ou
  (collector terminal) parameters.

Proper Biasing common-emitter configuration in active region



(a) npn transistor configuration



(b) pnp transistor configuration

Fig 4.7 : Common-emitter configuration

$$\boxed{I_E = I_C + I_B}$$

Common emitter current gain

$$\beta = \frac{I_C}{I_B}$$

Relationship between and

$$\text{DC Current Gain} = \frac{\text{Output Current}}{\text{Input Current}} = \frac{I_C}{I_B}$$

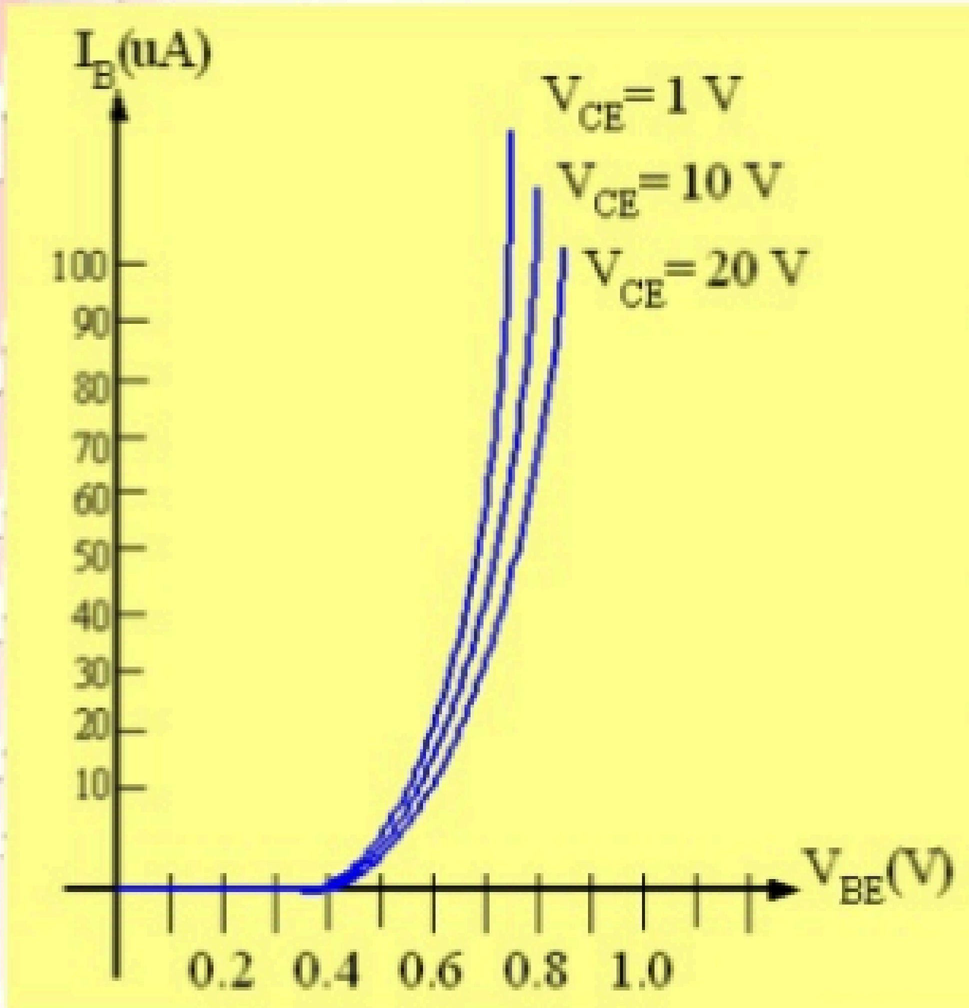
$$I_E = I_B + I_C \;\ldots\ldots\; (\text{KCL}) \quad \text{and} \quad \frac{I_C}{I_E} = \alpha$$

$$\text{Thus:} \quad I_B = I_E - I_C$$

$$I_B = I_E - \alpha I_E$$

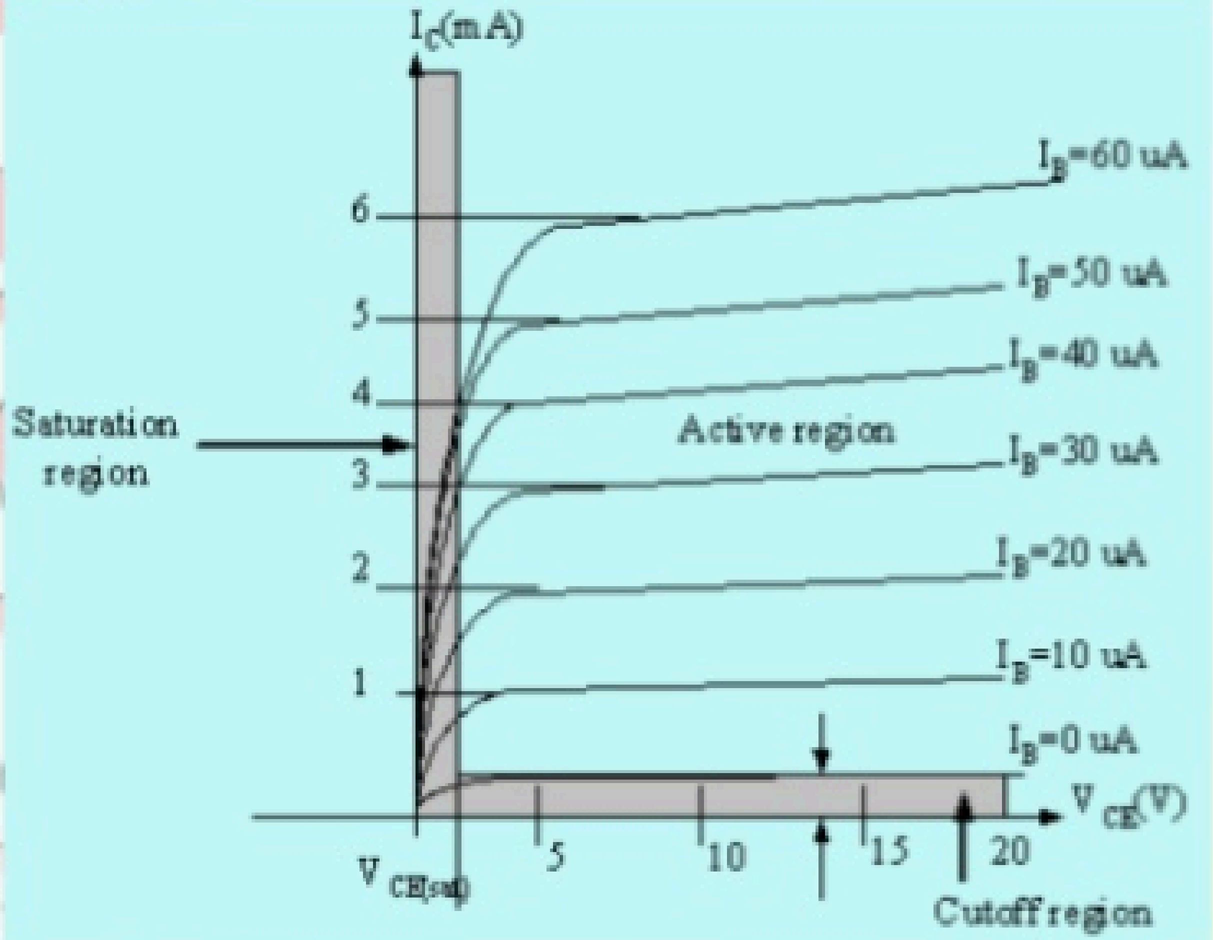
$$I_B = I_E\left(1 - \alpha\right)$$

$$\therefore \quad \beta = \frac{I_C}{I_B} = \frac{I_C}{I_E\left(1-\alpha\right)} = \frac{\alpha}{1-\alpha}$$



Input characteristics for a common-emitter NPN transistor

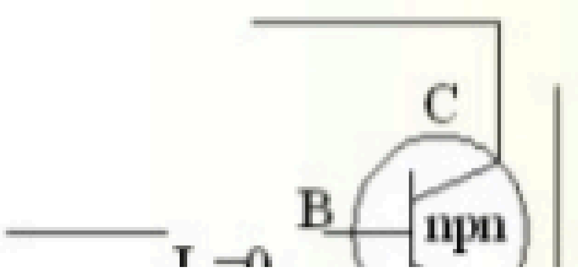
- I_B is microamperes compare to miliamperes of I_C.
- I_B will flow when V_{BE} > 0.7V for silicon and 0.3V for germanium
- Before this value I_B is very small and no I_B.
- Base-emitter junction is forward bias
- Increasing V_{CE} will reduce I_B for different values.

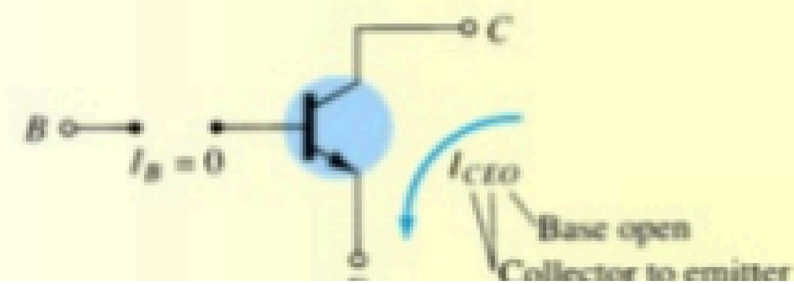


Output characteristics for a common-emitter npn transistor

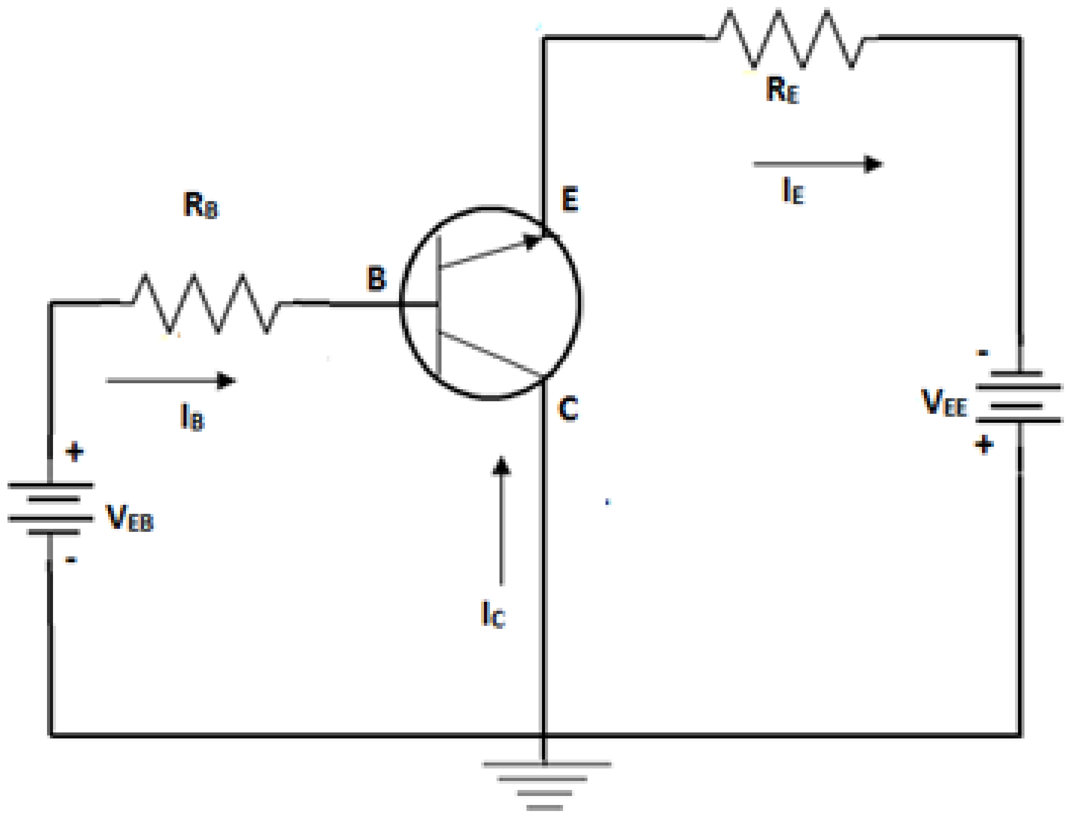
- For small V_{CE} ($V_{CE} < V_{CESAT}$, I_C increase linearly with increasing of V_{CE}
- $V_{CE} > V_{CESAT}$ I_C not totally depends on V_{CE} → constant I_C
- I_B(uA) is very small compare to I_C (mA). Small increase in I_B cause big increase in I_C
- I_B=0 A → I_{CEO} occur.

Active region	Saturation region	Cut-off region
• B-E junction is forward bias • C-B junction is reverse bias • can be employed for voltage, current and power amplification	• B-E and C-B junction is forward bias, thus the values of I_B and I_C is too big. • The value of V_{CE} is so small. • Suitable region when the transistor as a logic switch. • NOT and avoid this region when the transistor as an amplifier.	• region below I_B=0μA is to be avoided if an undistorted o/p signal is required • B-E junction and C-B junction is reverse bias • I_B=0, I_C not zero, during this condition I_C=I_{CEO} where is this current flow when B-E is reverse bias.

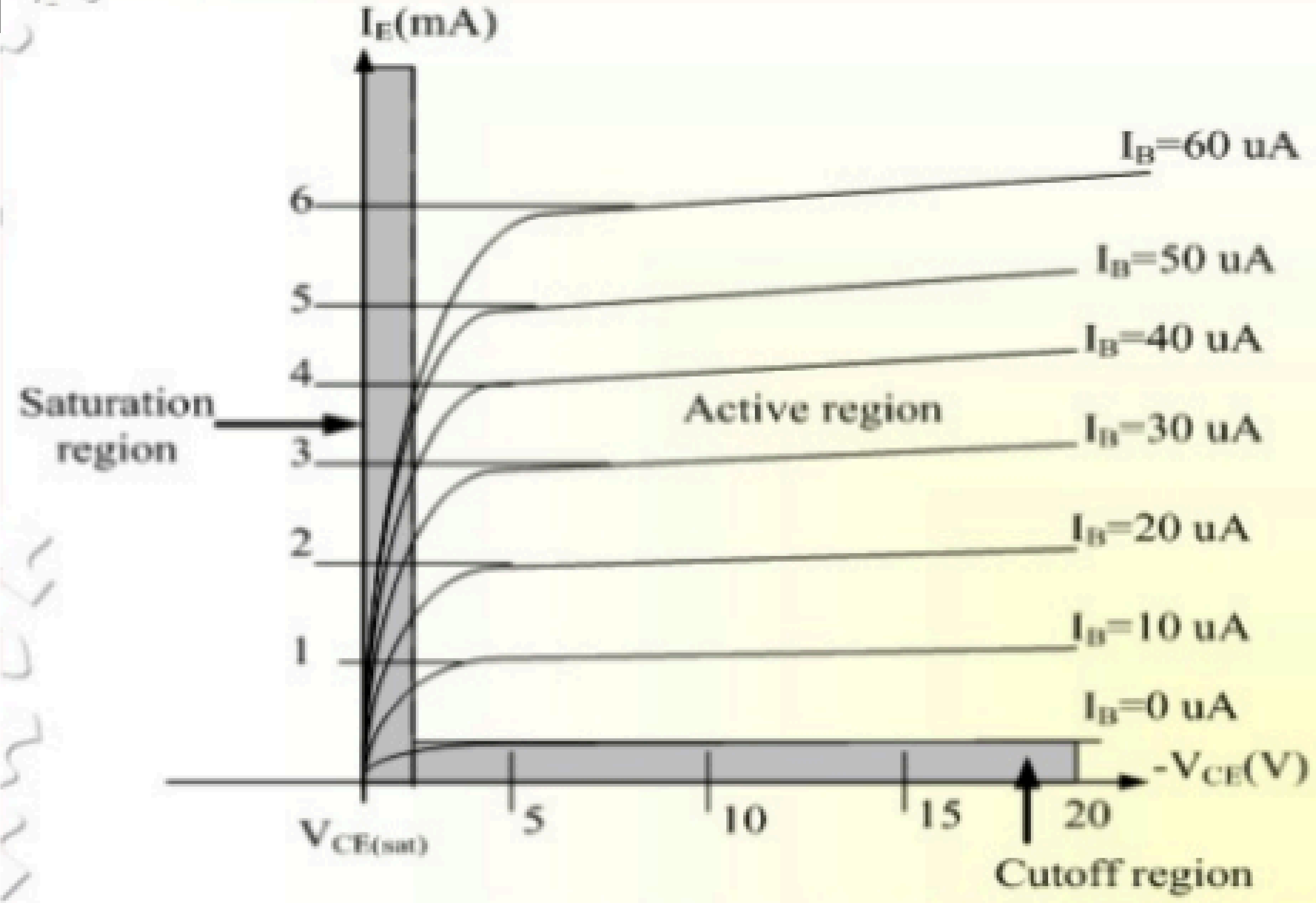




Common Collector Configuration



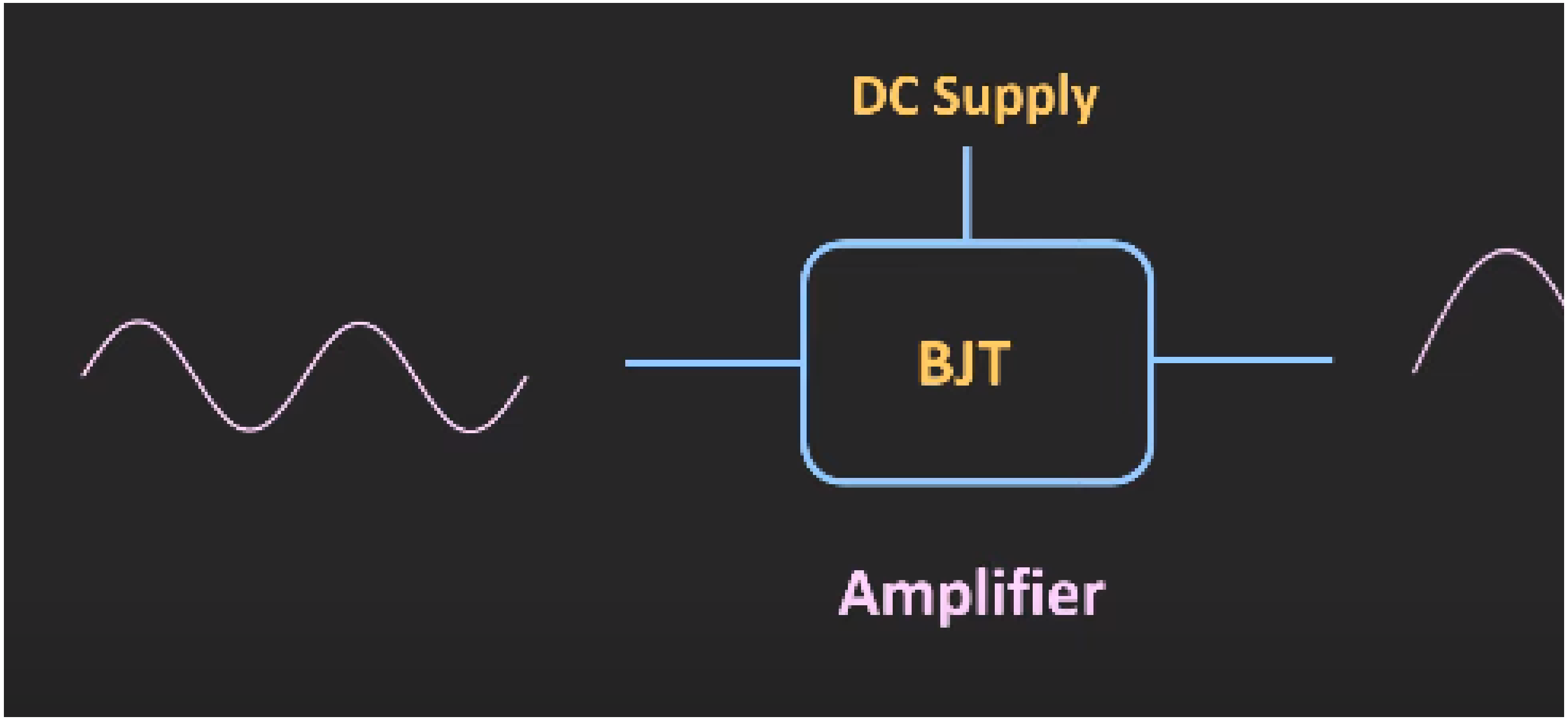
- For the common-collector configuration, the output characteristics are a plot of I_E vs V_{CE} for a range of values of I_B.



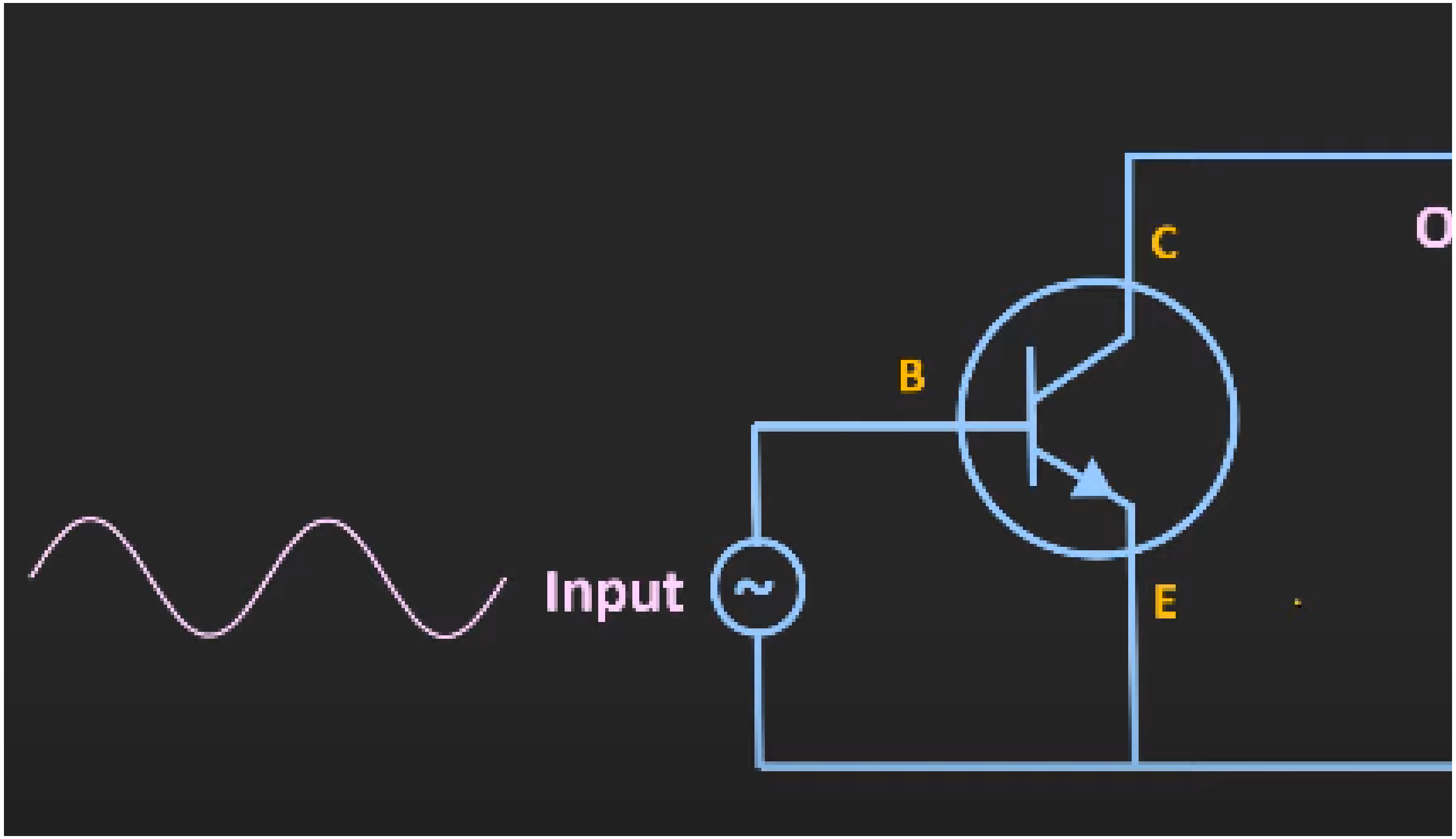
Comparison of Transistor

aracteristic	Common base	Common emitter	Comm
ut resistance	Low (about 100 Ω)	Low (about 750 Ω)	Very h 750 k
tput resistance	Very high (about 450 kΩ)	High (about 45 kΩ)	Low (
ltage gain	about 150	about 500	less th
plications	For high frequency applications	For audio frequency applications	For im matchi
rrent gain	No (less than 1)	High (β)	Appre

Purpose of Biasing in amplification



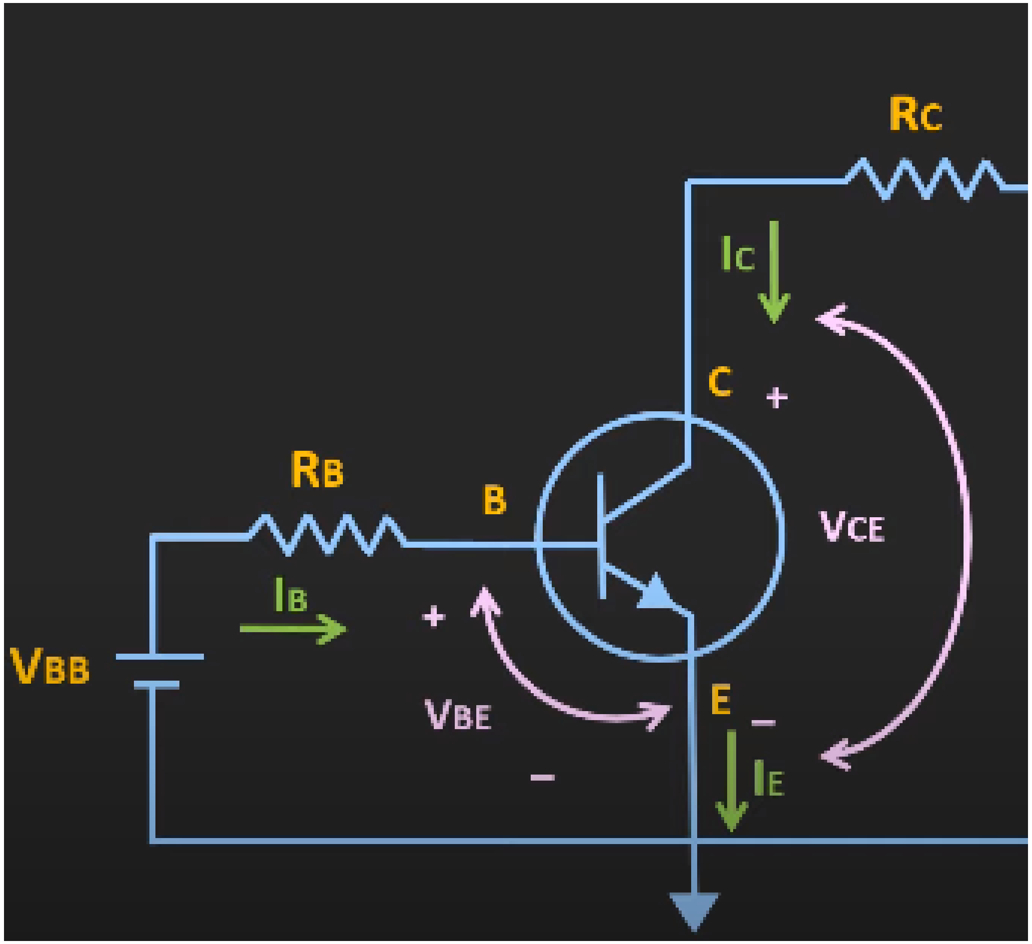
Proper biasing

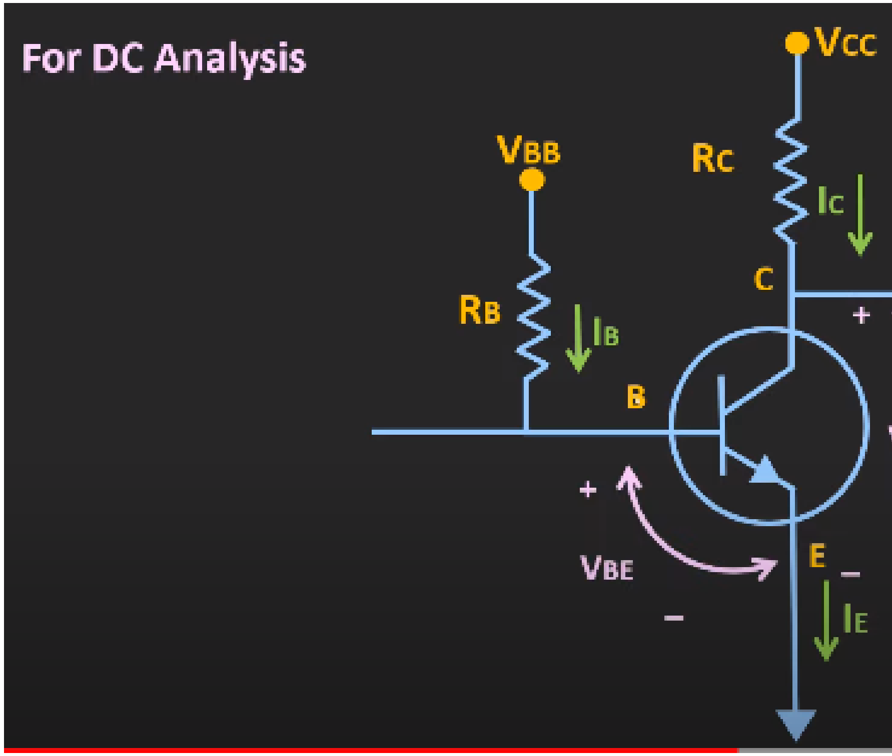


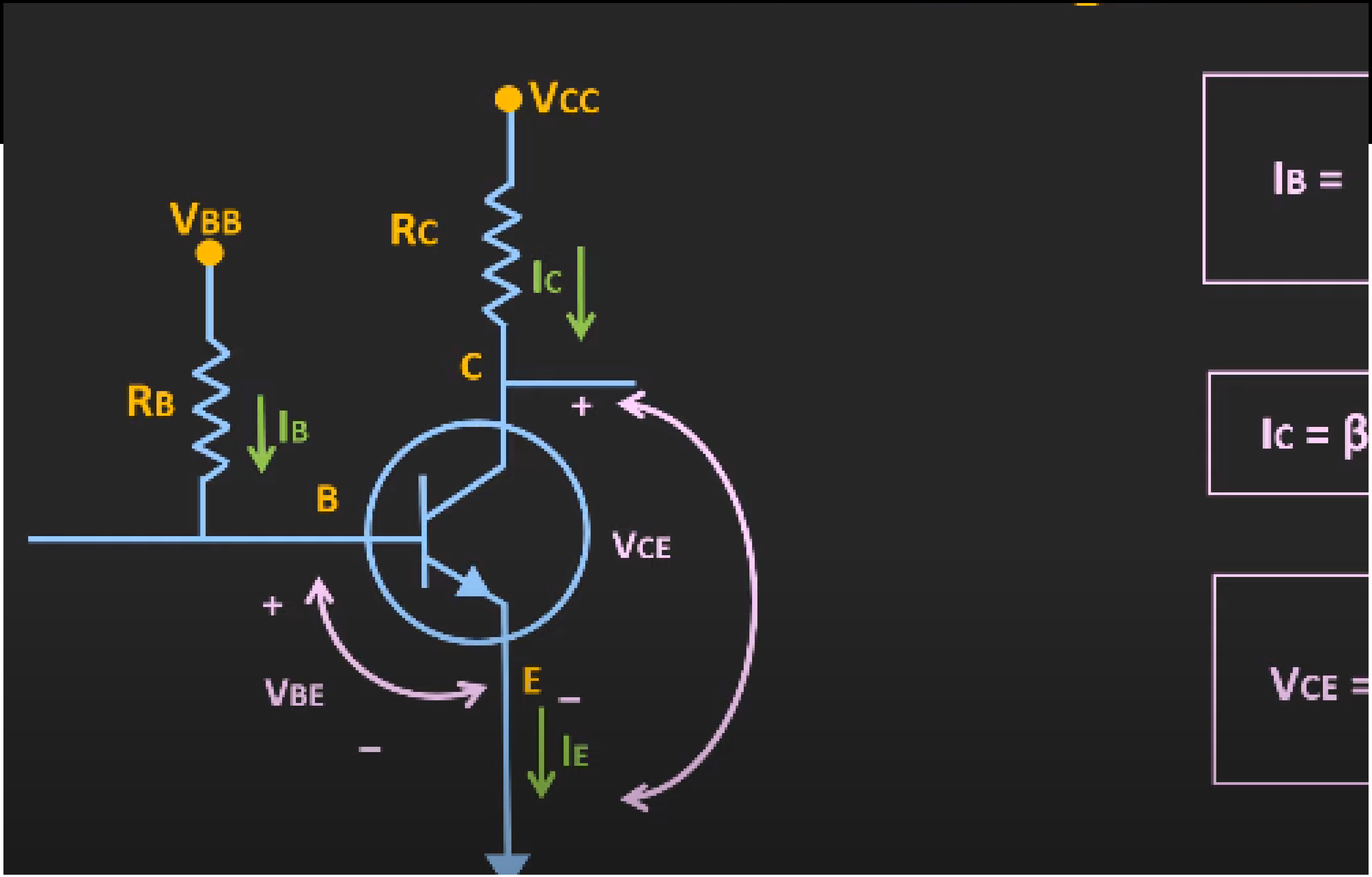
Types of biasing

- (1) Base bias (also called fixed bias).
- (2) Base bias with collector feedback (also called *collector feedback bias).*
- (3) Voltage divider bias (also called *self bias).*

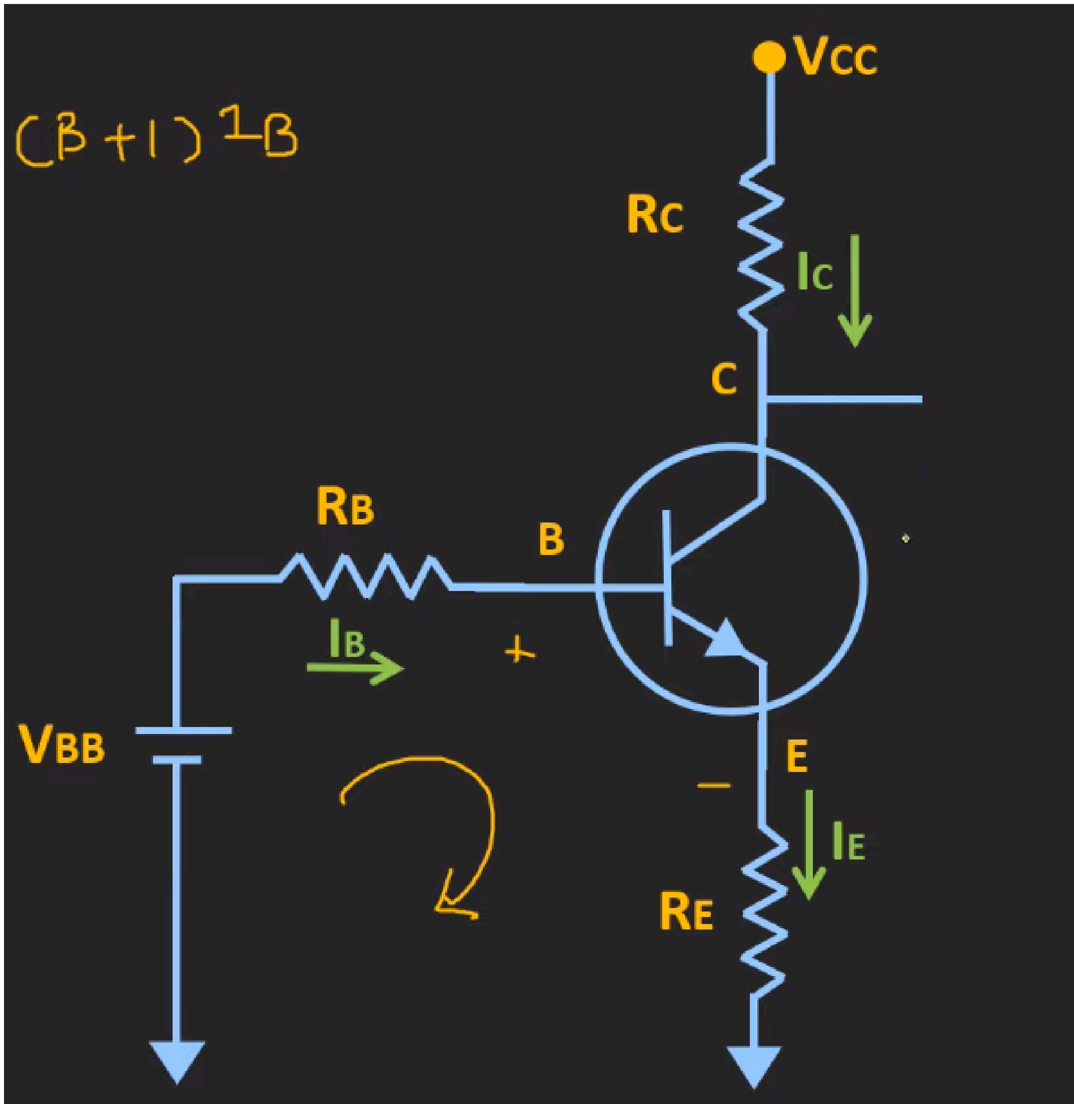
Fixed biasing (base bias)






VCC
VBB
RC
IC
C
RB
IB
B
VCE
+
VBE
E
–
IE
IB =
IC = β
VCE =

Base bias with emitter feedback



$V_{BB} - I_B R_B - V_{BE} -$

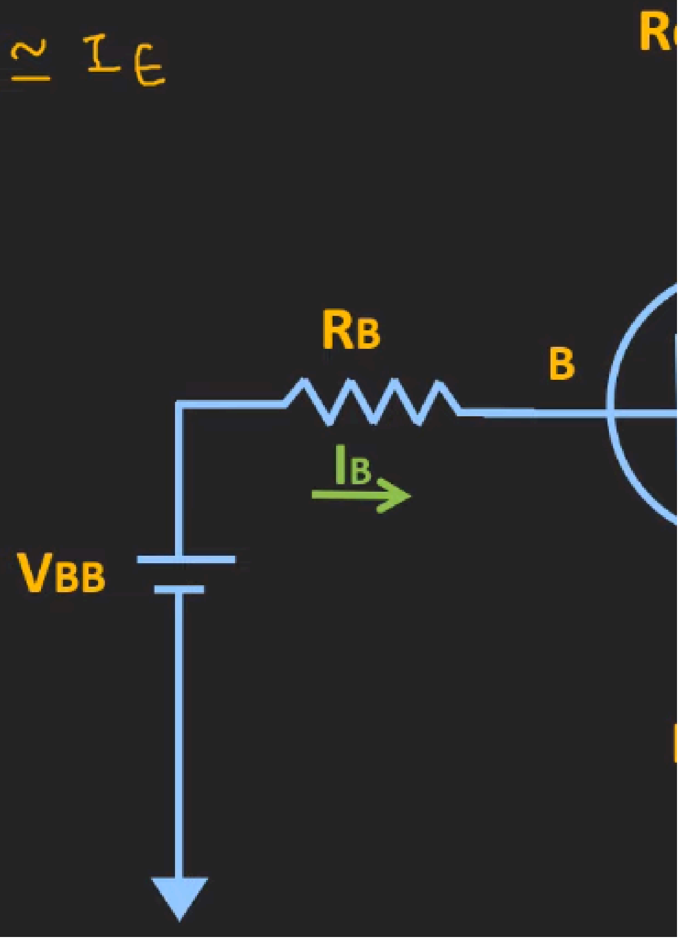
$\Rightarrow I_B = \dfrac{V_{BB} - V_{BE}}{R_B + (\beta+1)R}$

$I_C = \beta I_B$

At output side

$I_C = \alpha I_E$

$I_C \simeq I_E$



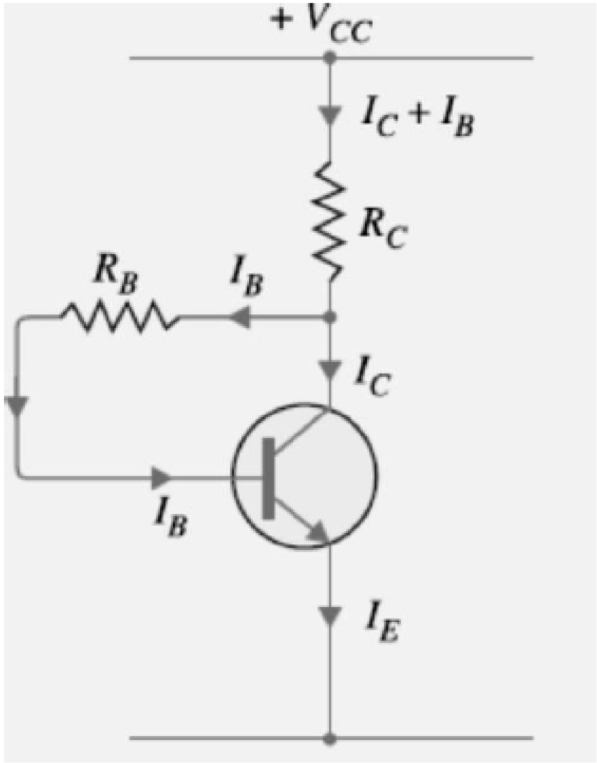
$V_{CC} - I_C R_C - V_{CE} -$

$\Rightarrow V_{CE} = V_{CC} - I_C R_C$

$\Rightarrow V_{CE} = V_{CC} - I_C ($

Biasing with collector feedback resistor.

 Here, the required zero signal base current is determined not by VCC but by the collector base voltage VCB. It is clear that VCB forward biases the base-emitter junction and hence base current IB flows through RB . This causes the zero signal collector current to flow in the circuit.



$$V_{CC} = I_C R_C + I_B R_B + V_{BE}$$

$$R_B = \frac{V_{CC} - V_{BE} - I_C R_C}{I_B}$$

$$= \frac{V_{CC} - V_{BE} - \beta\, I_B R_C}{I_B} \qquad (\because I_C = \beta\, I_B)$$

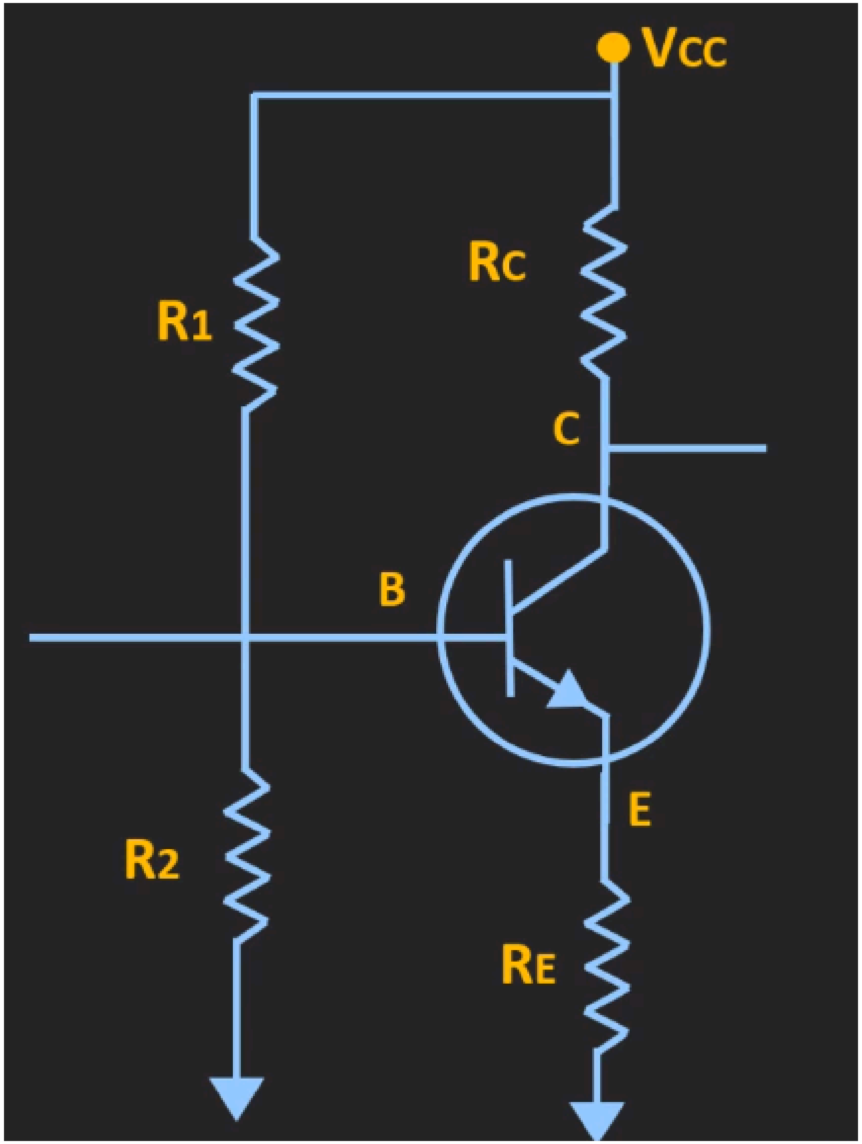
It can be shown mathematically that stability factor *S* for this method of biasing is less than
(β+ 1) *i.e.*
 Stability factor, $S < (\beta + 1)$
 Therefore, this method provides better thermal stability than the fixed bias.

Note. It can be easily proved that Q-point values (IC and VCE) for the circuit are given by

$$I_C = \frac{V_{CC} - V_{BE}}{R_B / \beta + R_C}$$

$$V_{CE} = V_{CC} - I_C R_C$$

Voltage divider biasing

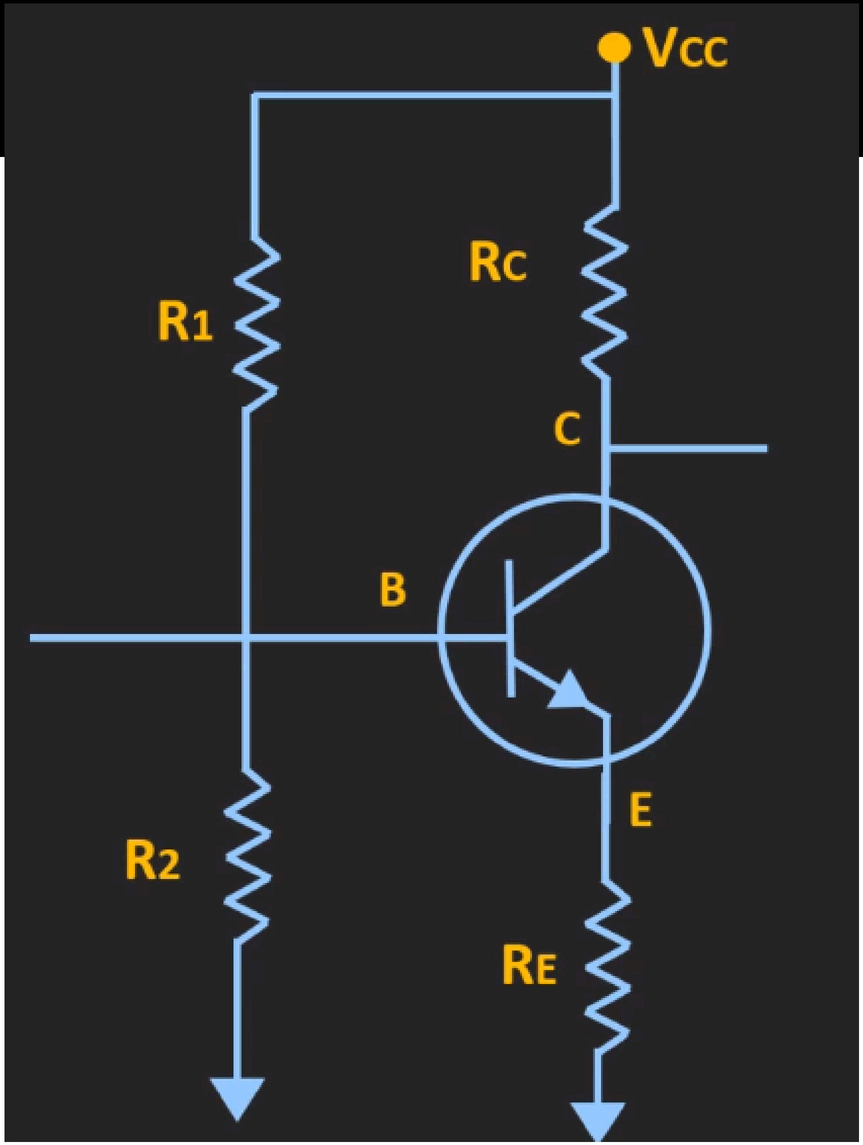


$$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

$$V_{CC} - I_C R_C - V_{CE} - V_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$



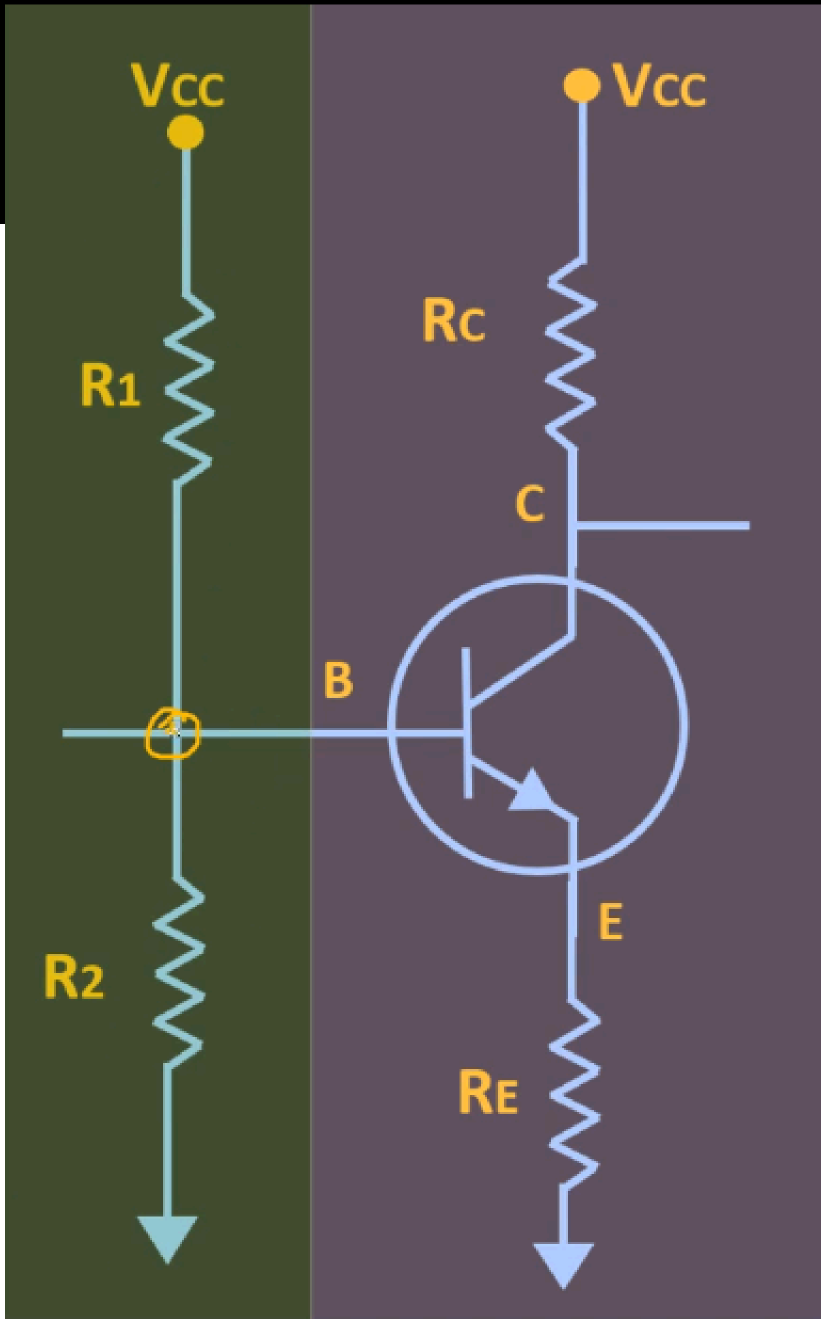
$$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

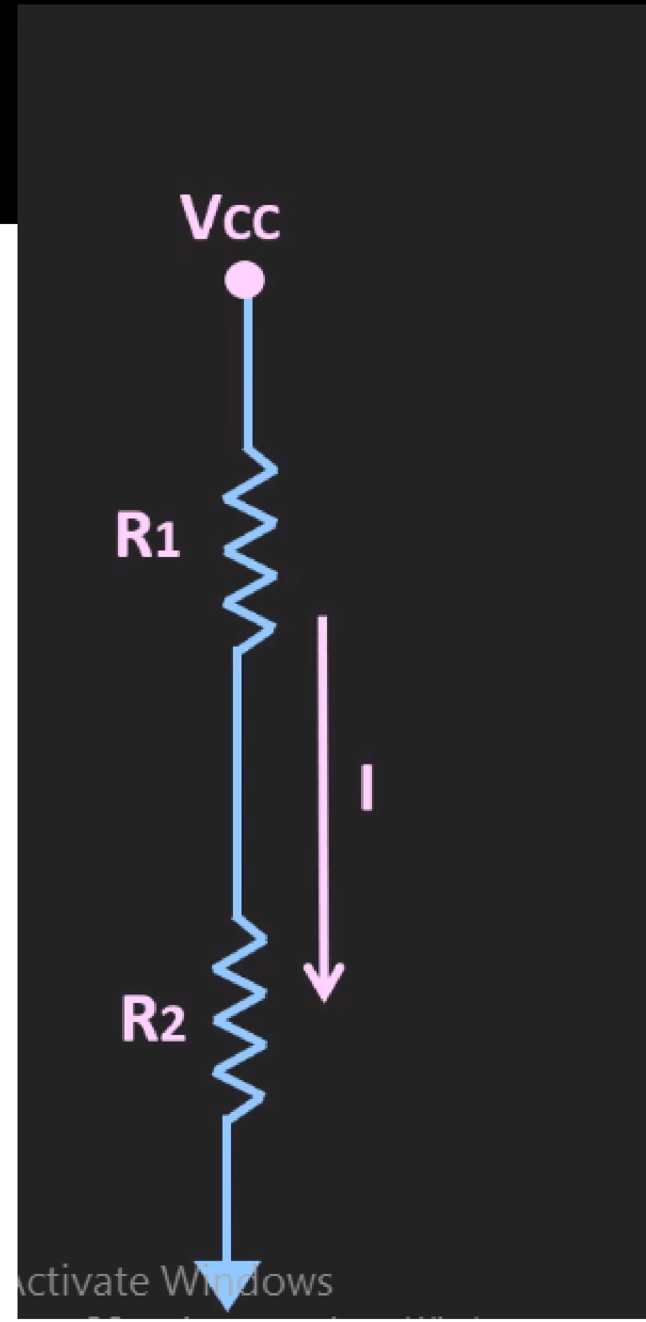
$$V_E = V_B - V_{BE}$$

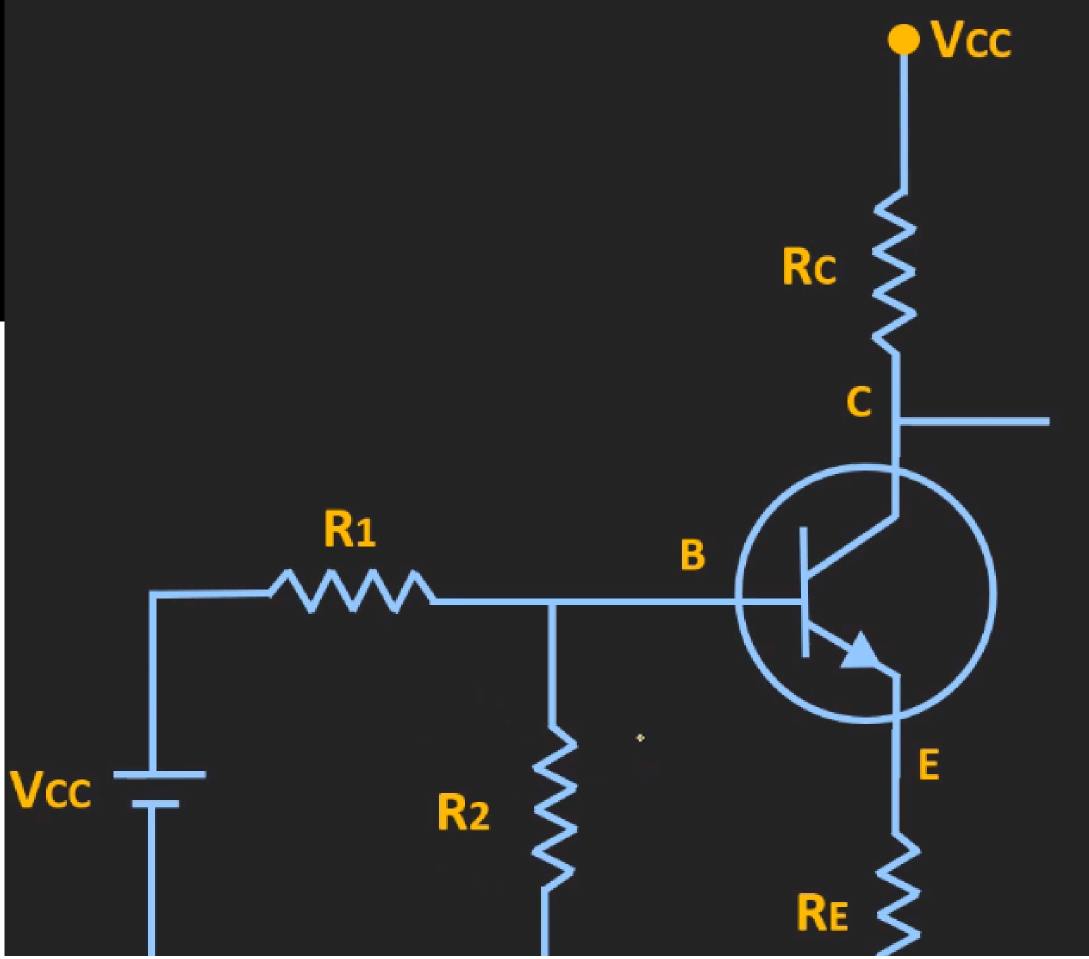
$$I_E = \frac{V_E}{R_E}$$

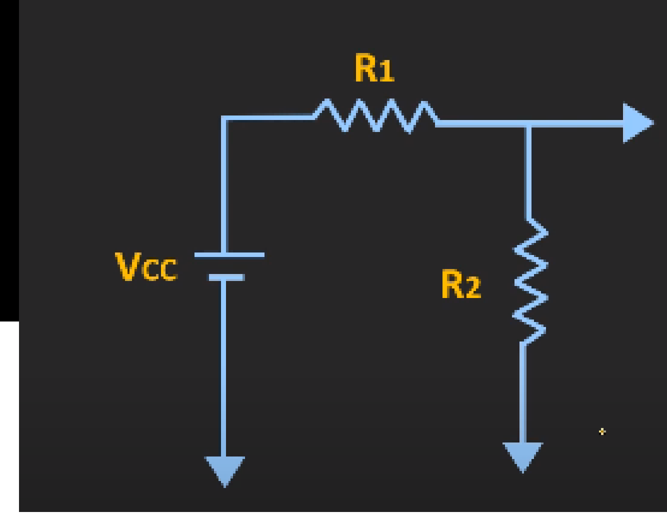
$$I_C \approx I_E$$

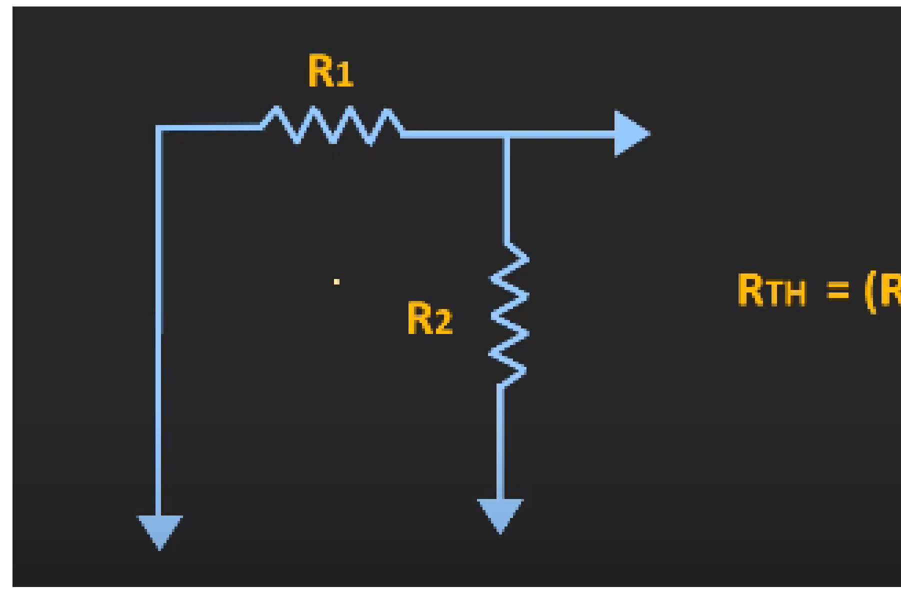
$$V_{CE} = V_{CC} - I_C\,(R_C + R_E)$$

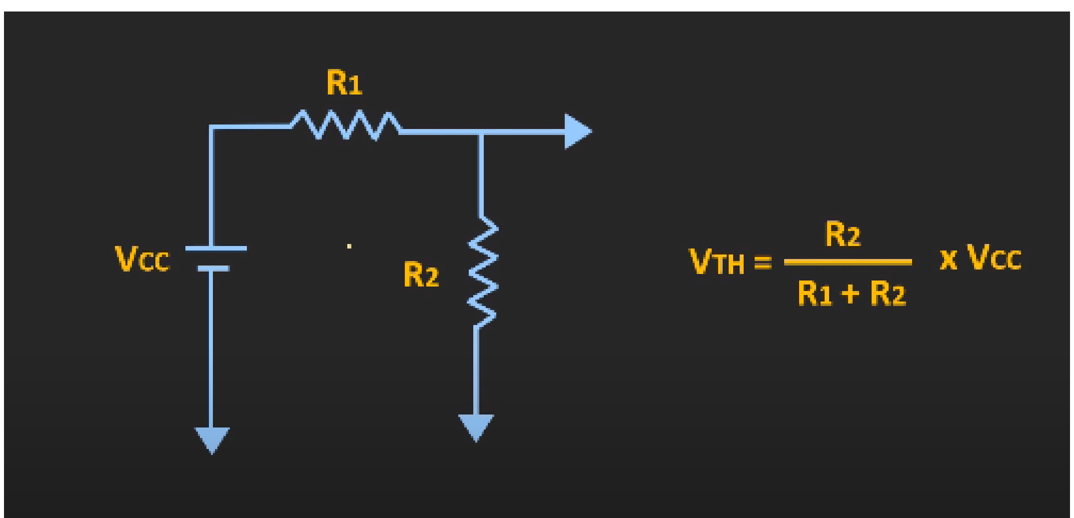

VCC
R1
R2
VCC
RC
C
B
E
RE

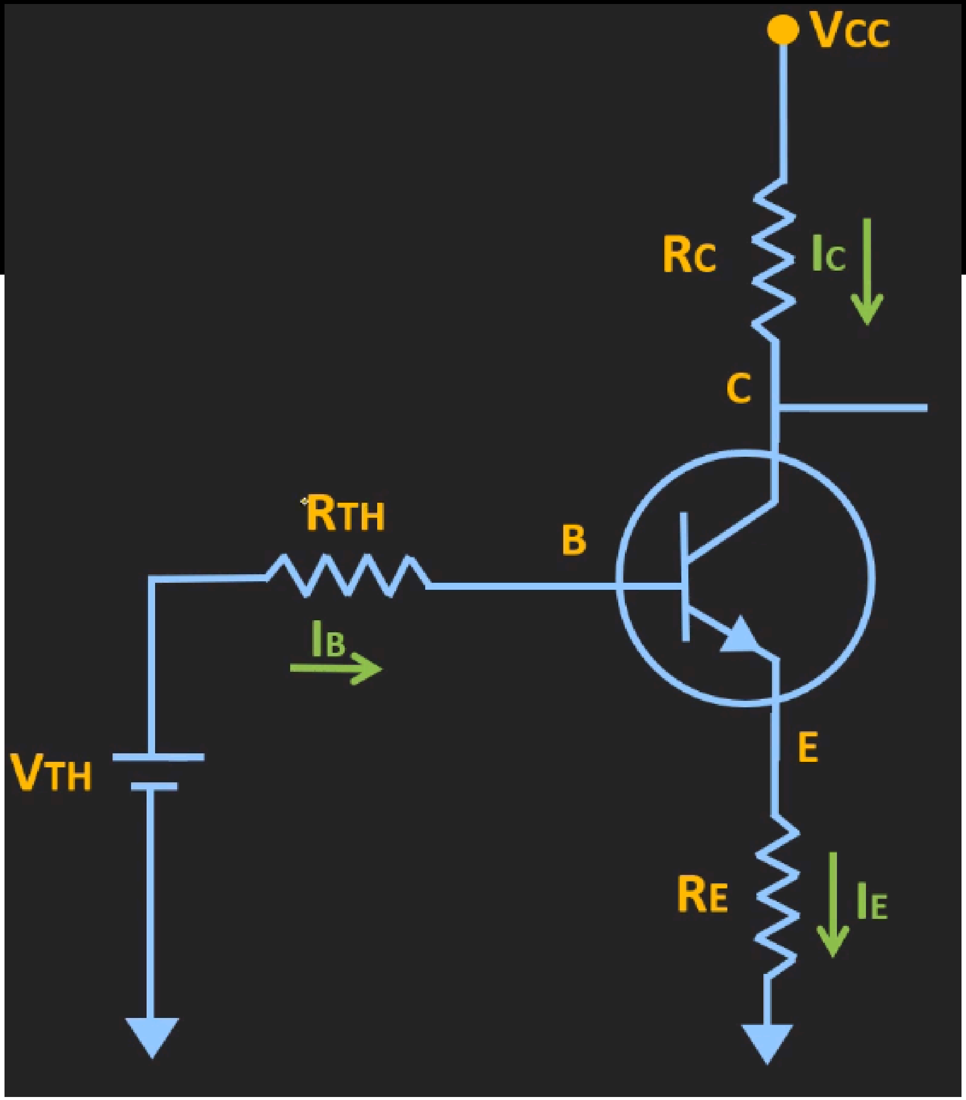

VCC
R1
I
R2


Vcc
Rc
C
R1
B
E
Vcc
R2
RE


R1
Vcc
R2


R1
R2
RTH = (R1


R1
Vcc
R2
VTH = R2 / R1 + R2 x Vcc

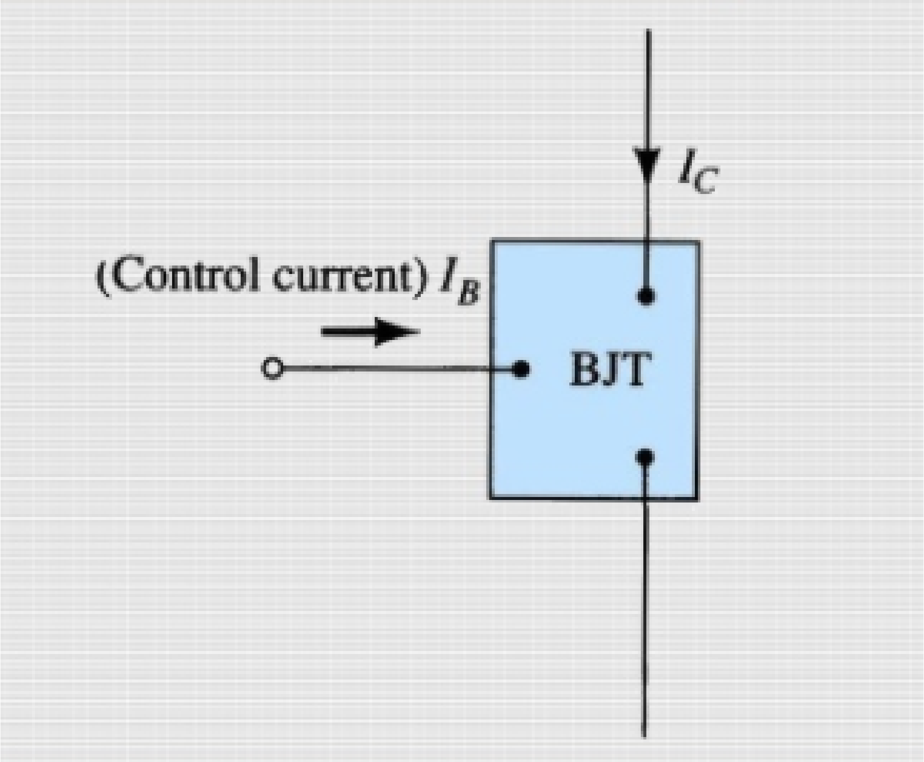


$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E}$$

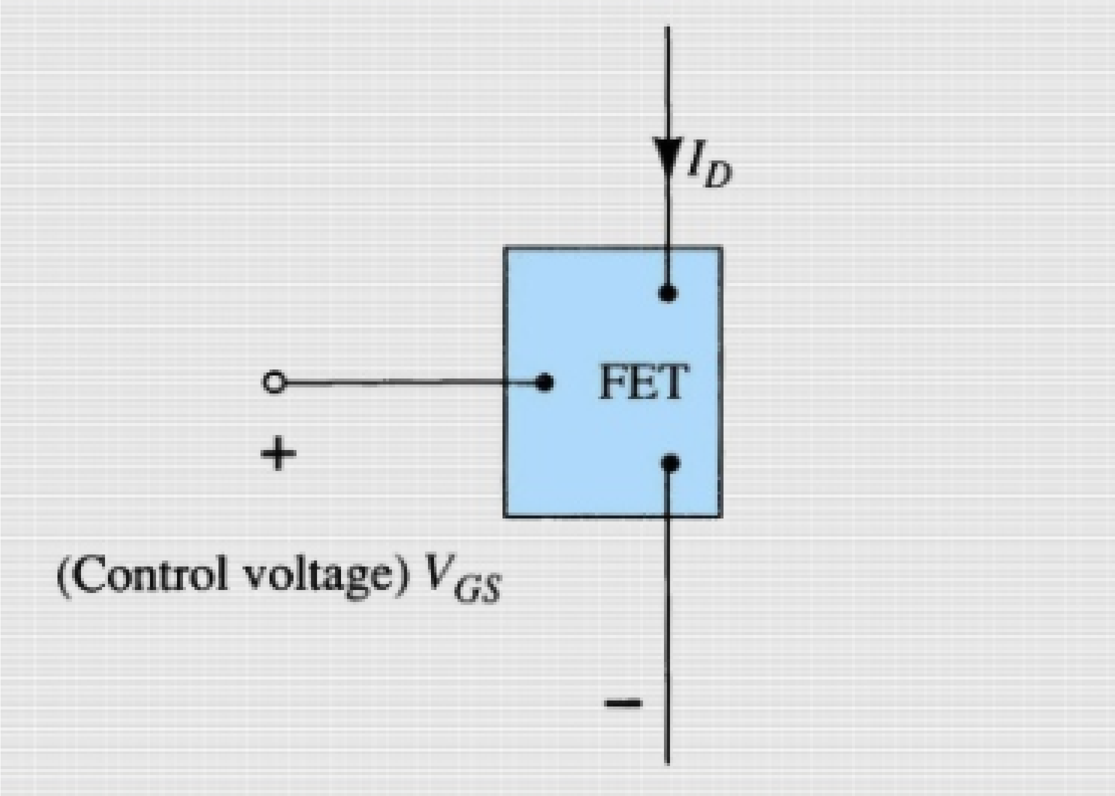
$$I_C = \beta I_B$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Bipolar Junction Transistor



Field Effect Transistor



Introduction of FET

The ordinary or bipolar transistor has two main disadvantage.

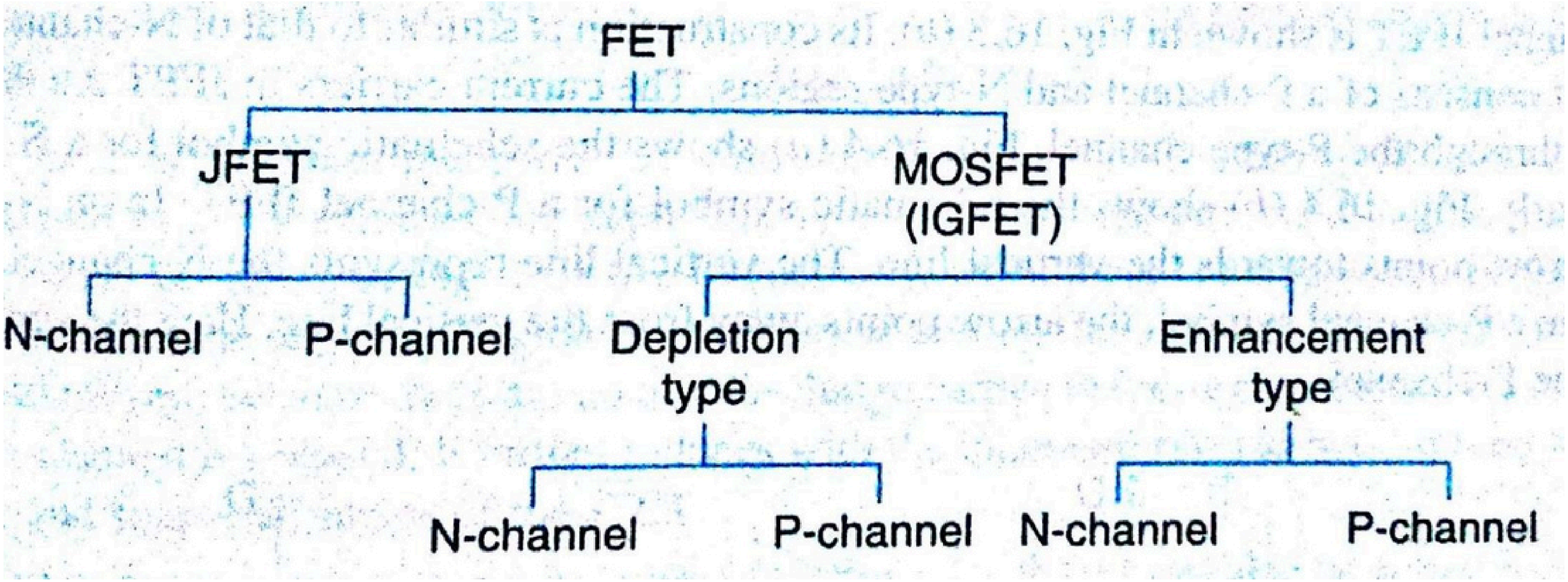
- It has a low input impedance
- It has considerable noise level

To overcome this problem Field effect transistor (FET) is introduced because of its:

- High input impedance
- Low noise level than ordinary transistor

And Junction Field Effect Transistor (JFET) is a type of FET.

Types of FET:


FET
JFET
MOSFET
(IGFET)
N-channel
P-channel
Depletion type
Enhancement type
N-channel
P-channel
N-channel
P-channel

Field Effect Transistor

FET has several advantages over BJT

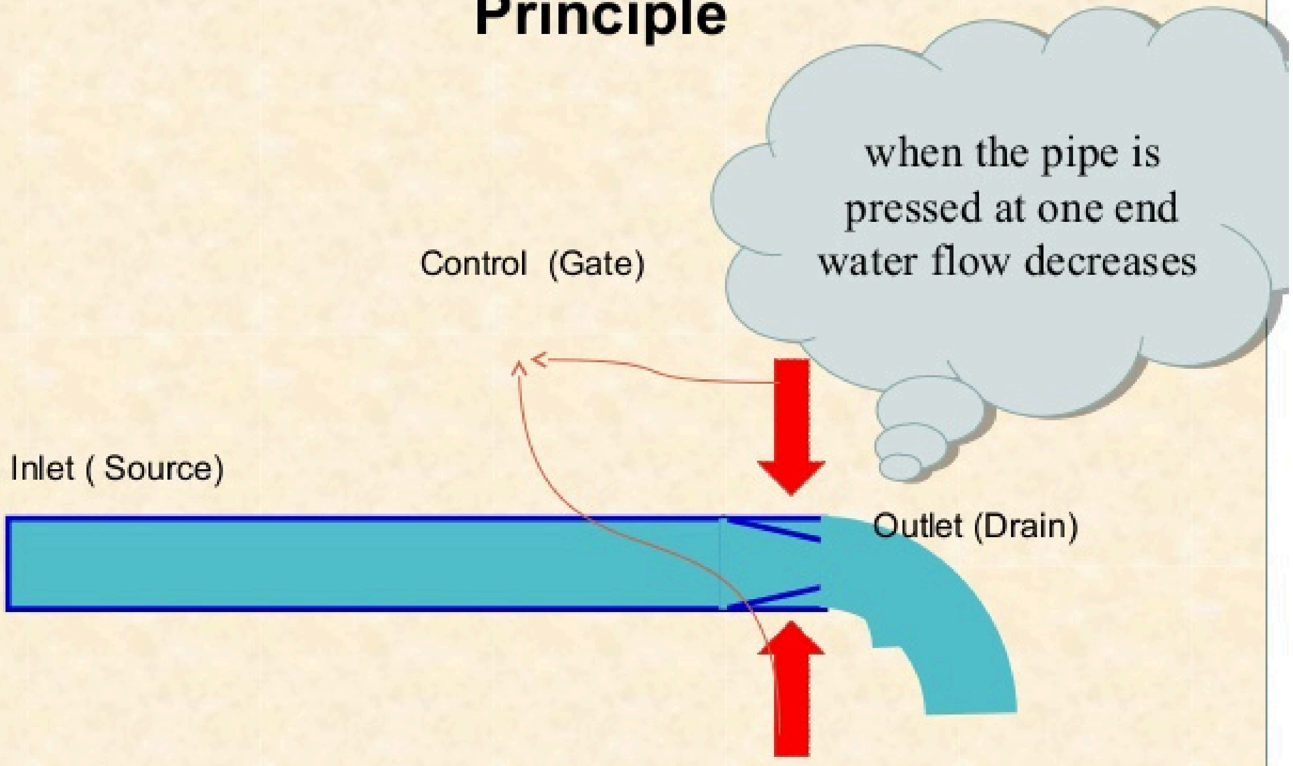
1. Current flow is due to majority carriers only
2. Immune to radiation
3. High input resistance
4. Less noisy than BJT
5. No offset voltages at zero drain current
6. High thermal stability

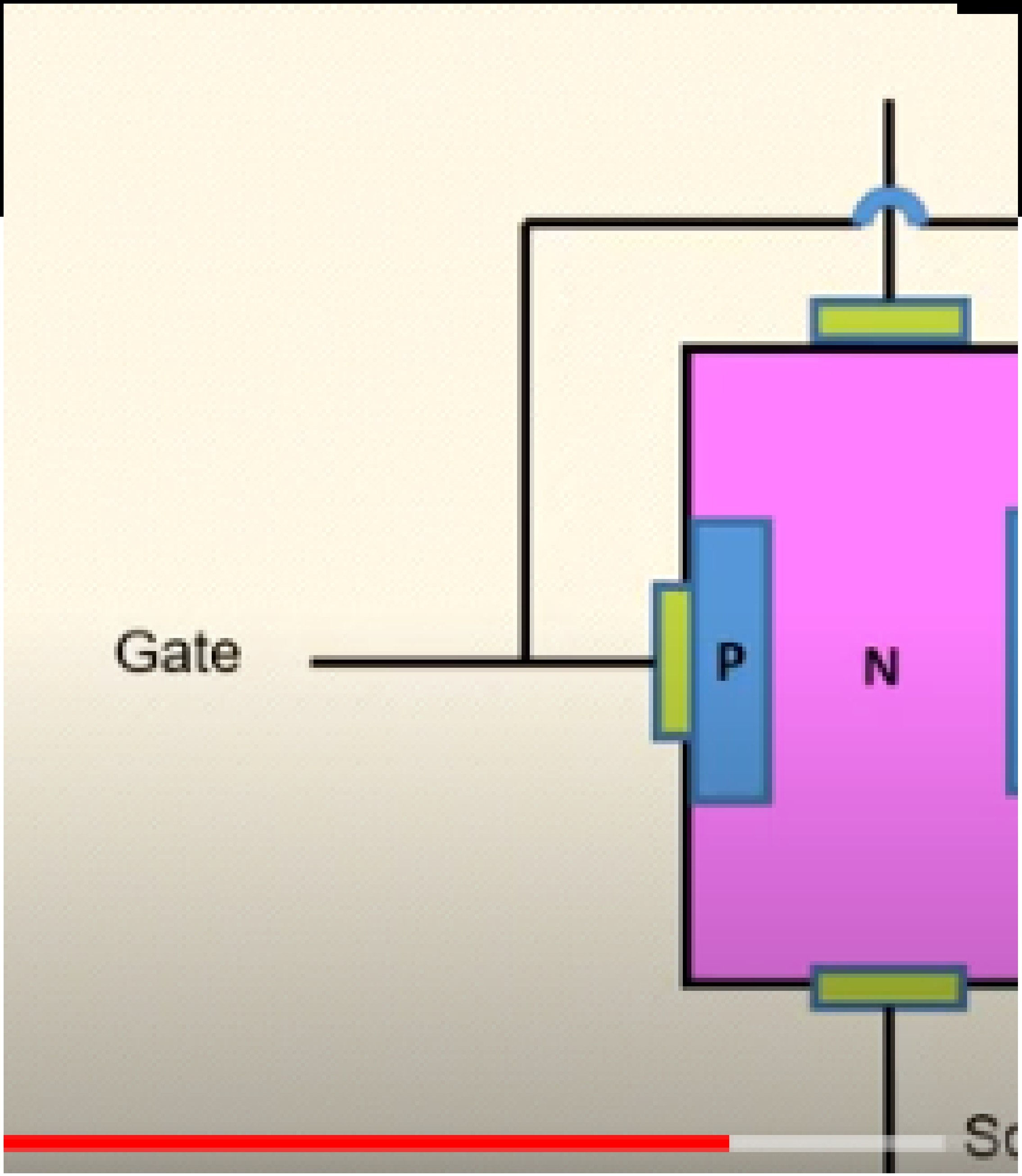
Construction of FET

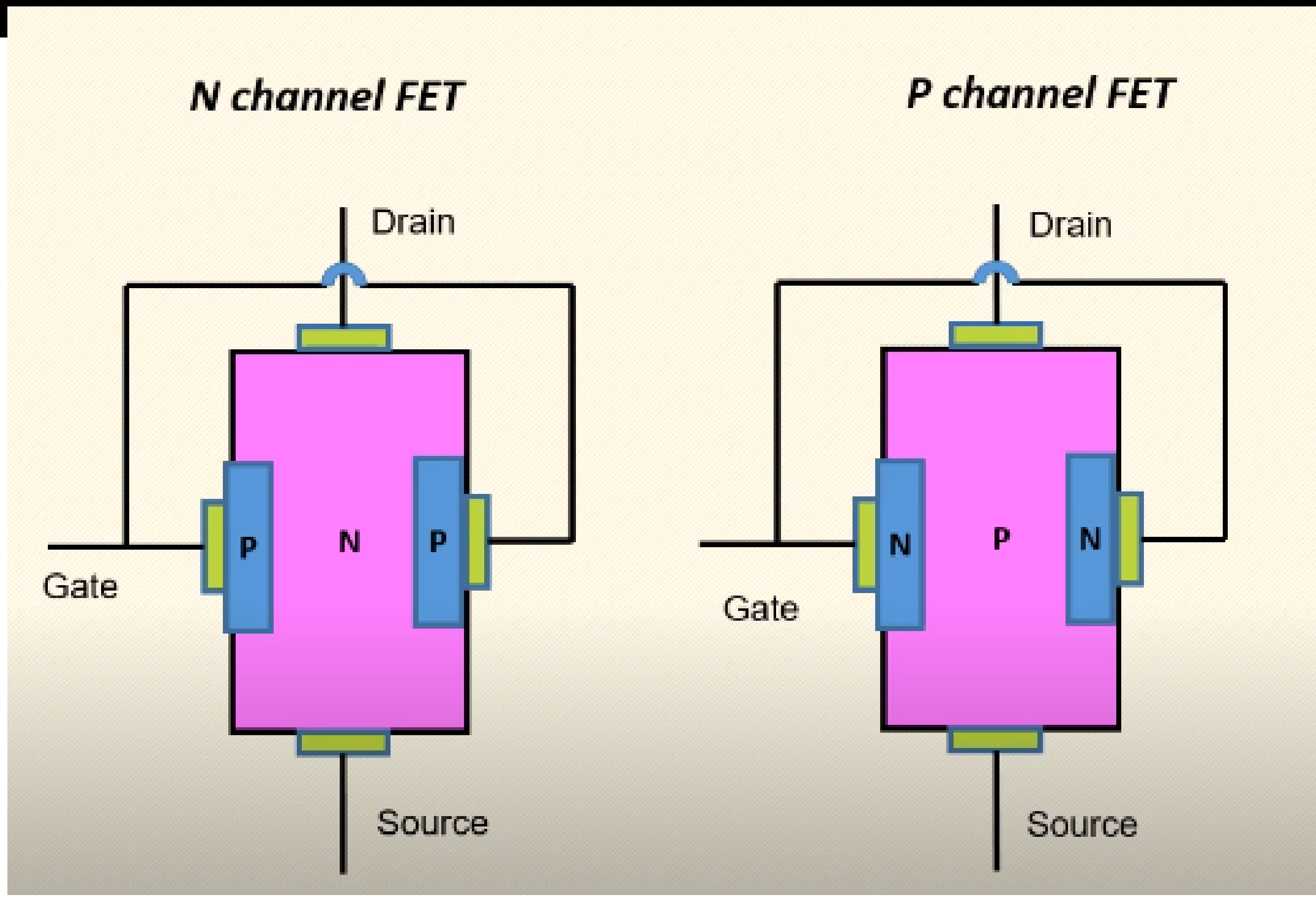
Analogy :

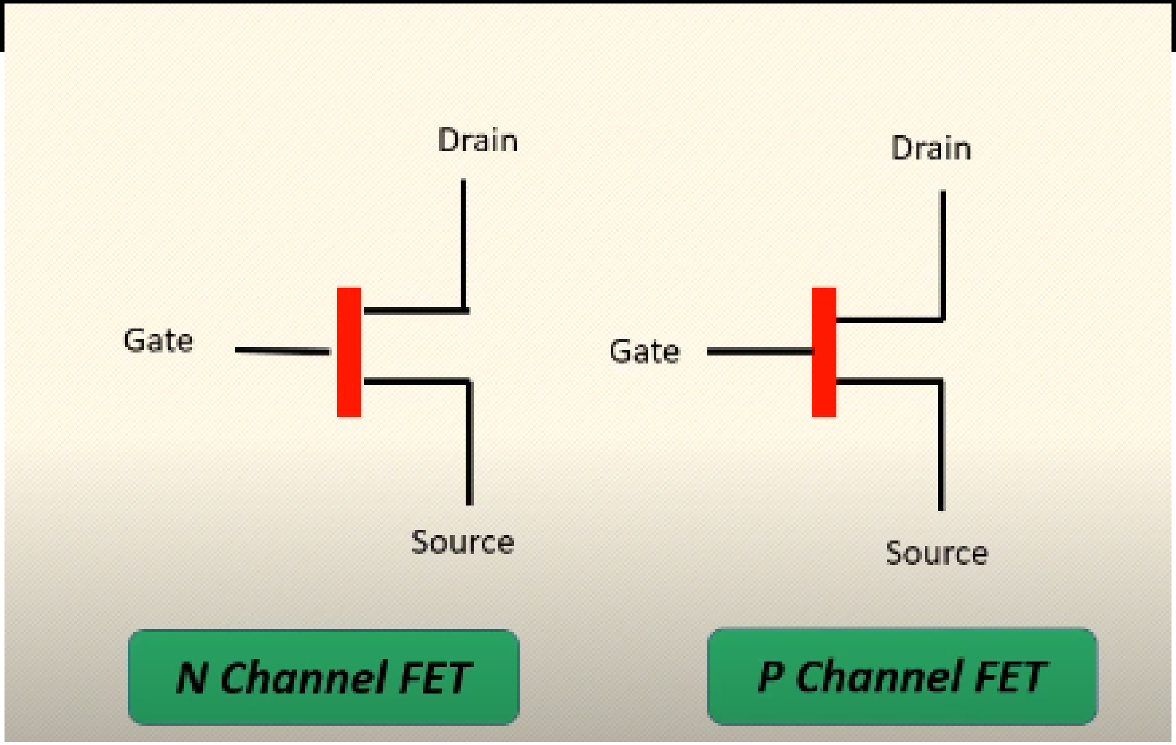
- The operation of FET can be compared to the water flow through a flexible pipe
- When One end is pressed the cross sectional area decreases hence water flow decreases
- In a FET drain is similar to outlet
- Gate is similar to control in the figure 2

Principle


when the pipe is
pressed at one end
water flow decreases
Control (Gate)
Inlet (Source)
Outlet (Drain)


Gate
P
N


N channel FET
P channel FET
Drain
Drain
Gate
P
N
P
Gate
N
P
N
Source
Source


Drain
Gate
Source
N Channel FET
Drain
Gate
Source
P Channel FET

Operation

Principle : To control the drain current FET makes use of channel formed in by Space charge region between Gate and the bar

By increasing the reverse bias the width of space charge region decreases

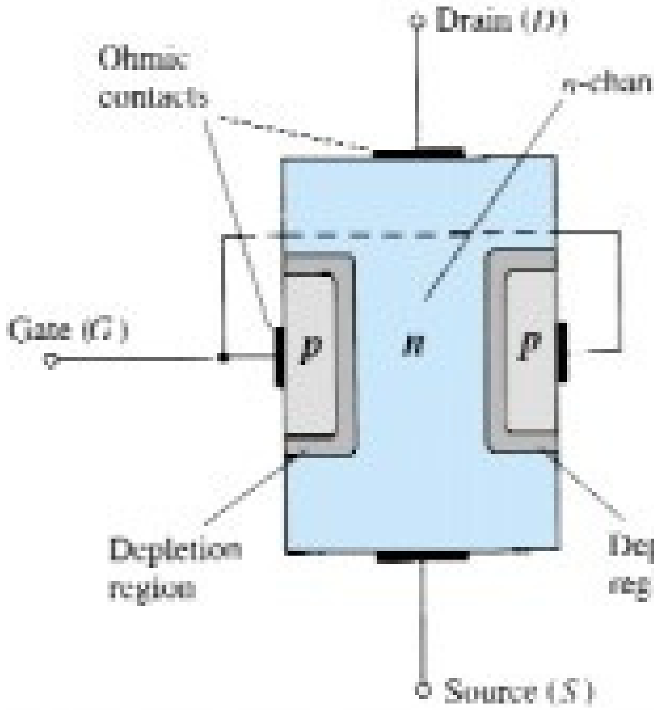
As a result the channel Resistance increases

The Drain current decreases

Working

N Channel FET	P Channel FET
Source connected to -VE	Source connected to +VE
Drain Connected to +ve	Drain Connected to -ve
Gate connected to –ve (Reverse Biased)	Gate connected to +ve (Reverse Biased)

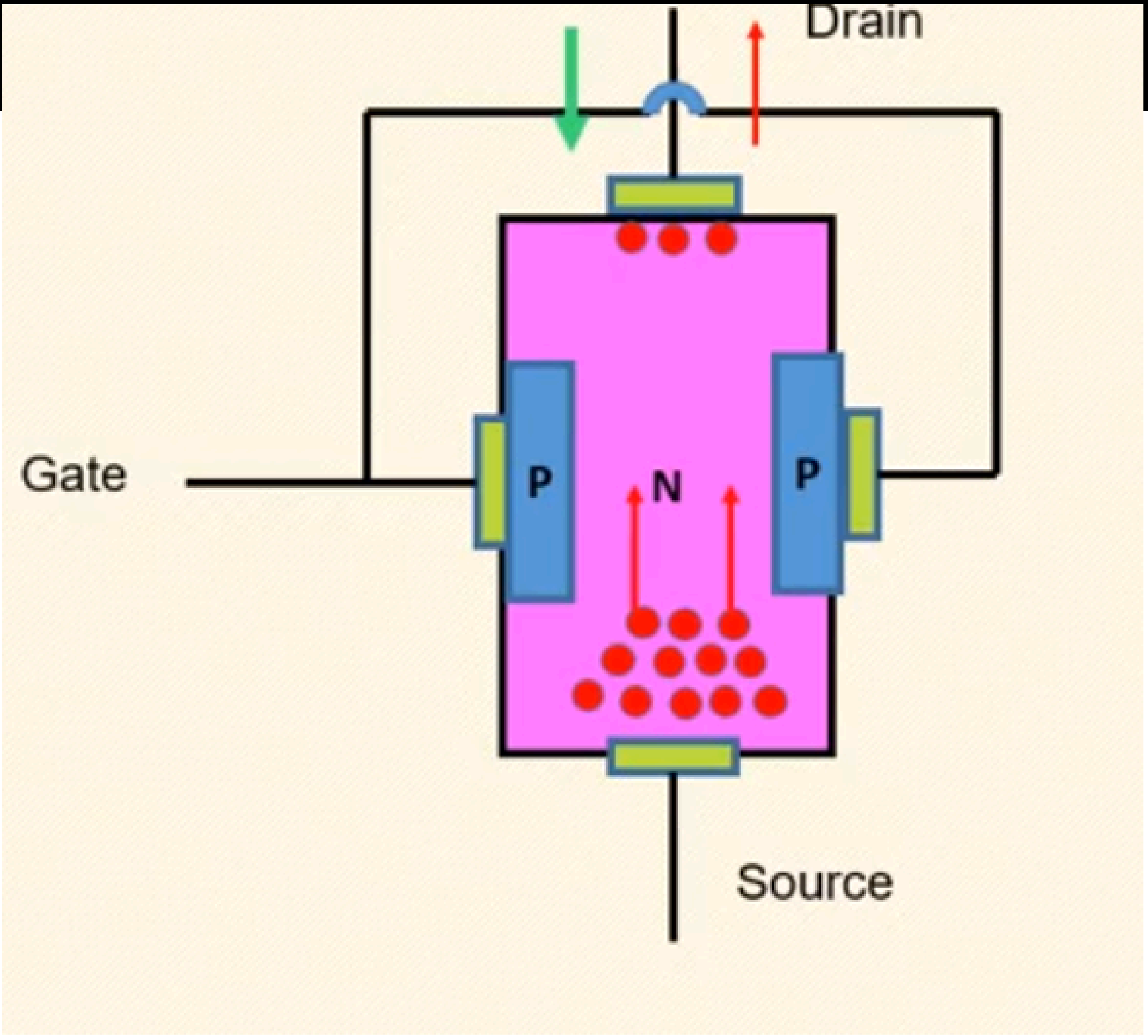
N channel JFET



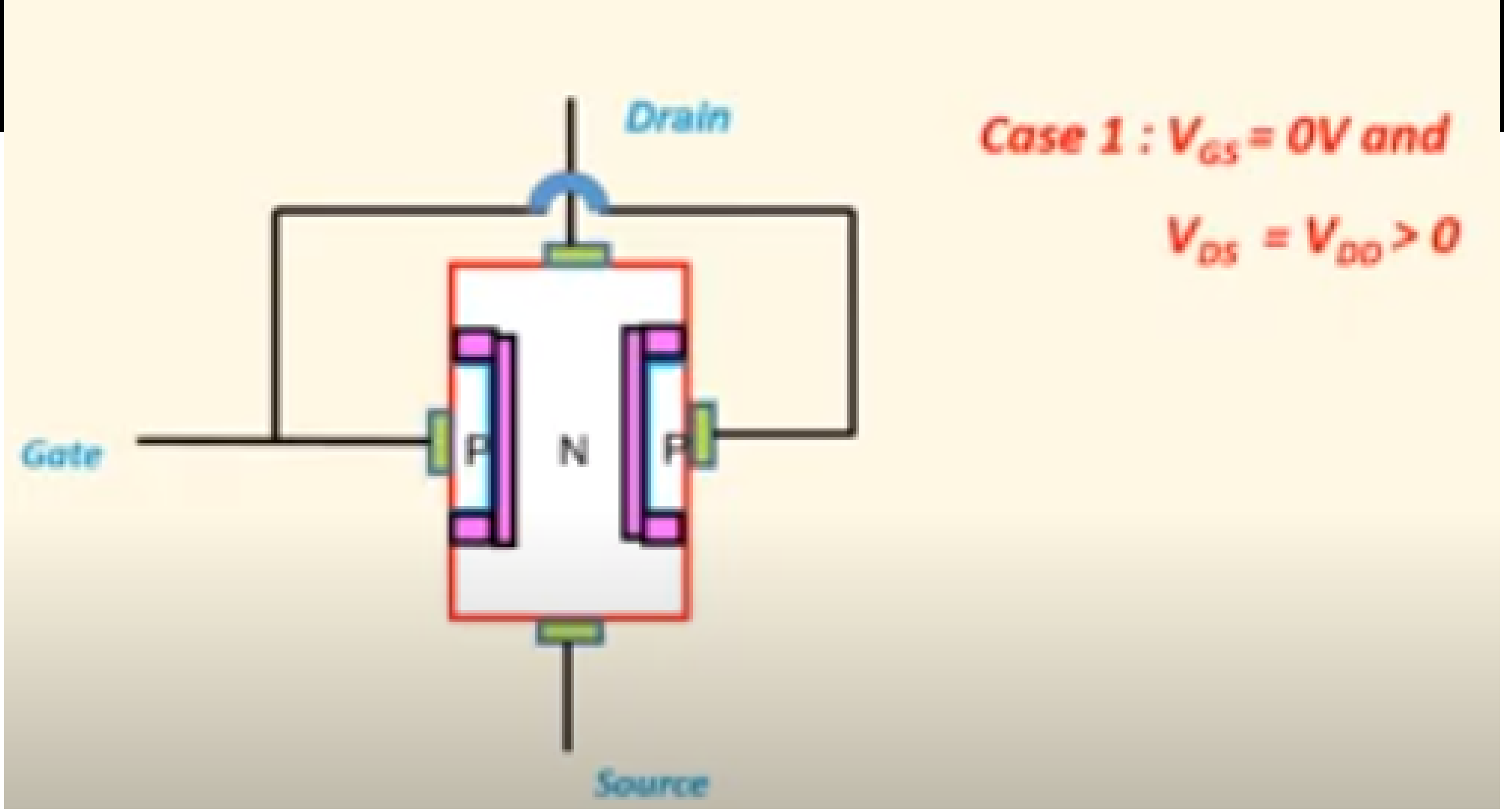
- The basic construction of the n-channel JFET is shown in Fig. Note that the major part of the structure is the n-type material that forms the channel between the embedded layers of p-type material.

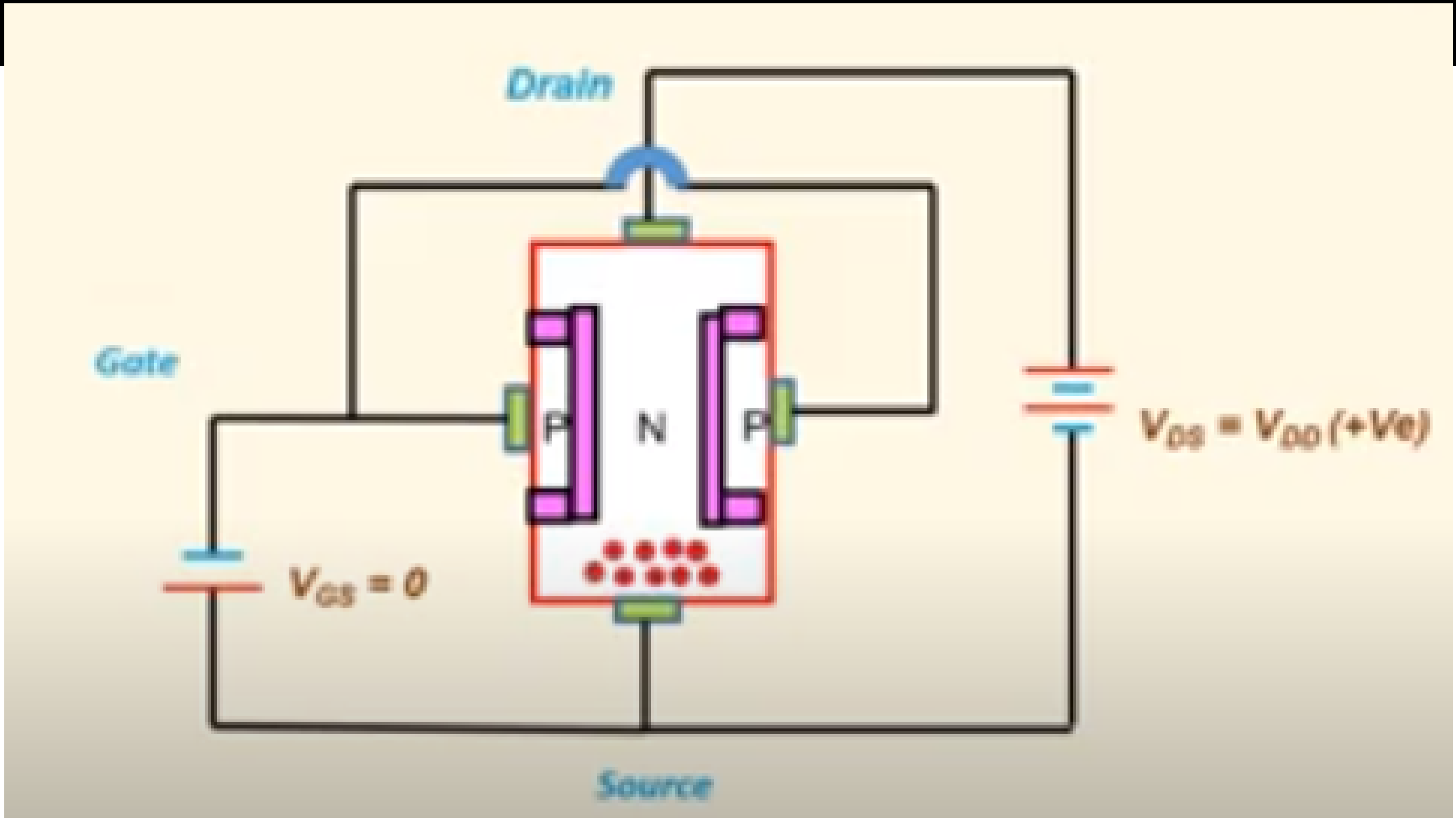
Construction of N channel JFET

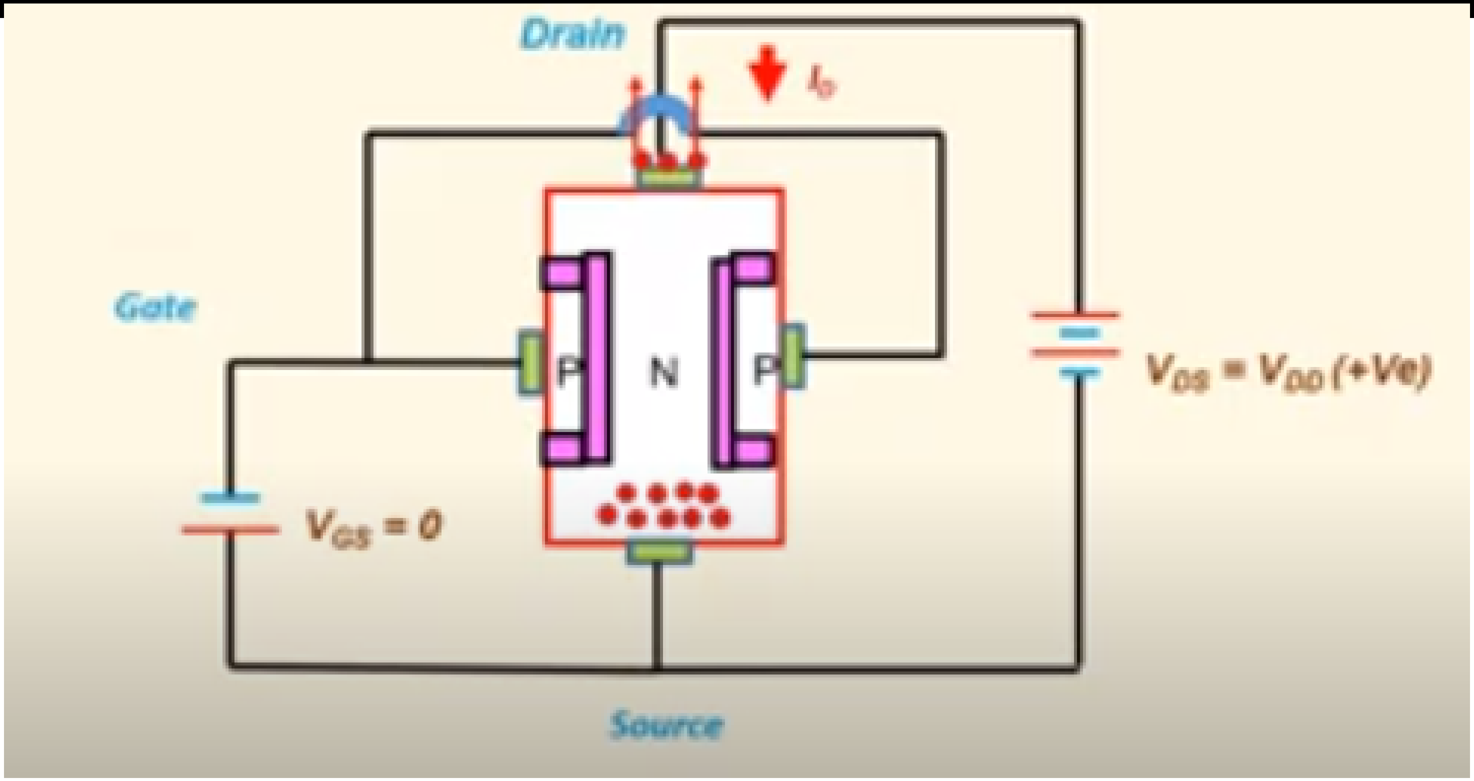
- The top of the n-type channel is connected through an ohmic contact to a terminal referred to as the drain (D), while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the source (S).
- The two p-type materials are connected together and to the gate (G) terminal.
- In essence, therefore, the drain and source are connected to the ends of the n-type channel and the gate to the two layers of p-type material.



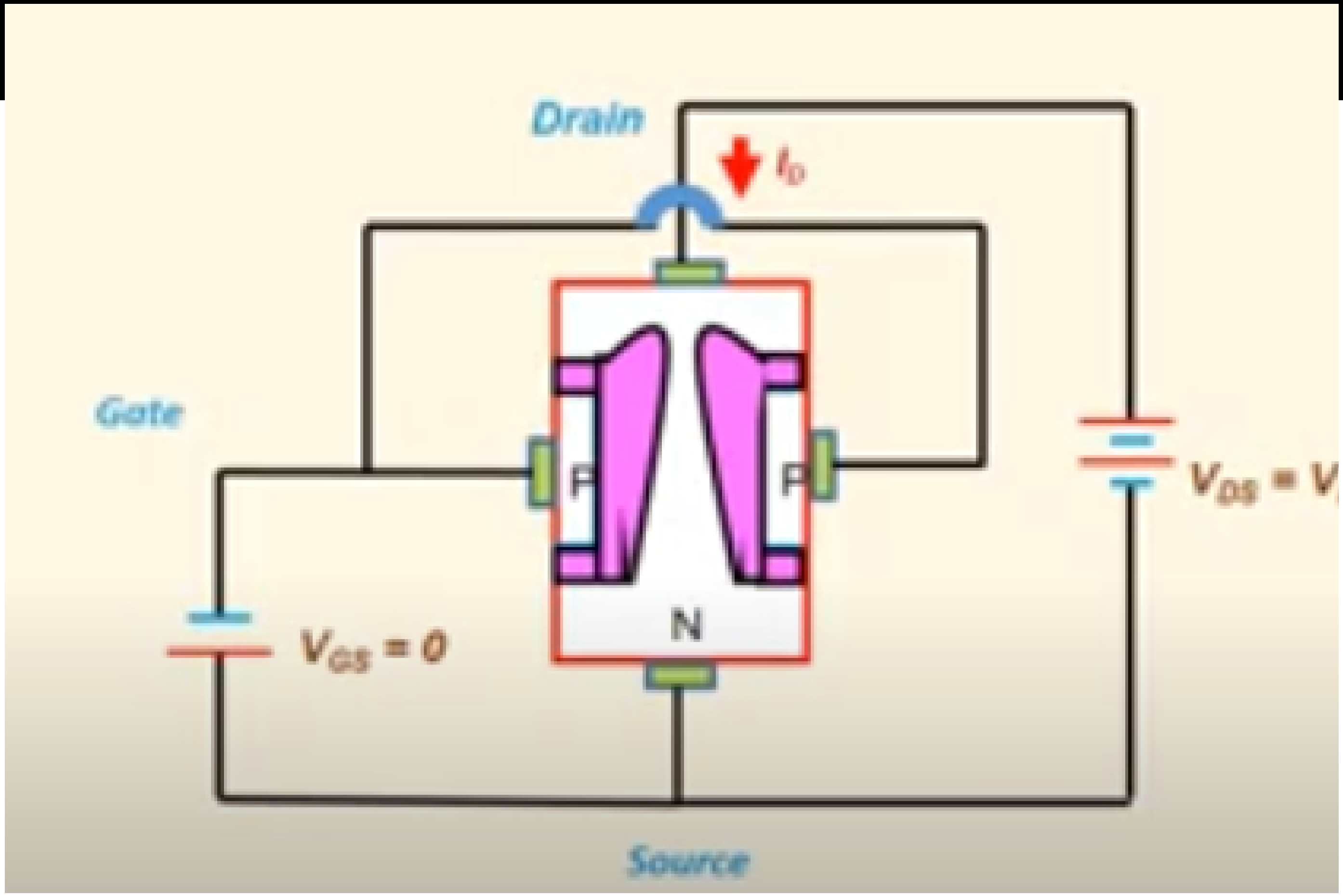
Drain
Gate
P
N
P
Source

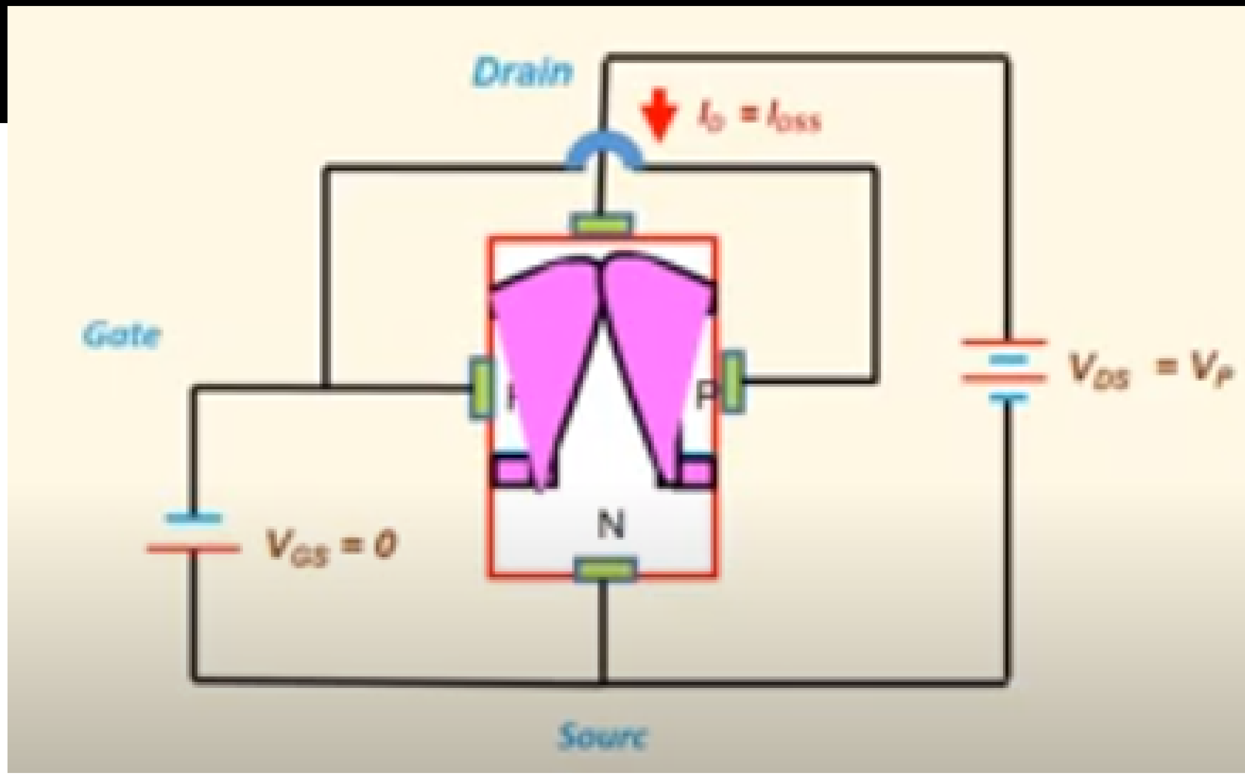

Drain
Case 1 : $V_{GS} = 0V$ and
$V_{DS} = V_{DD} > 0$
Gate
P
N
P
Source


Drain
Gate
P
N
P
VDS = VDD (+Ve)
VGS = 0
Source

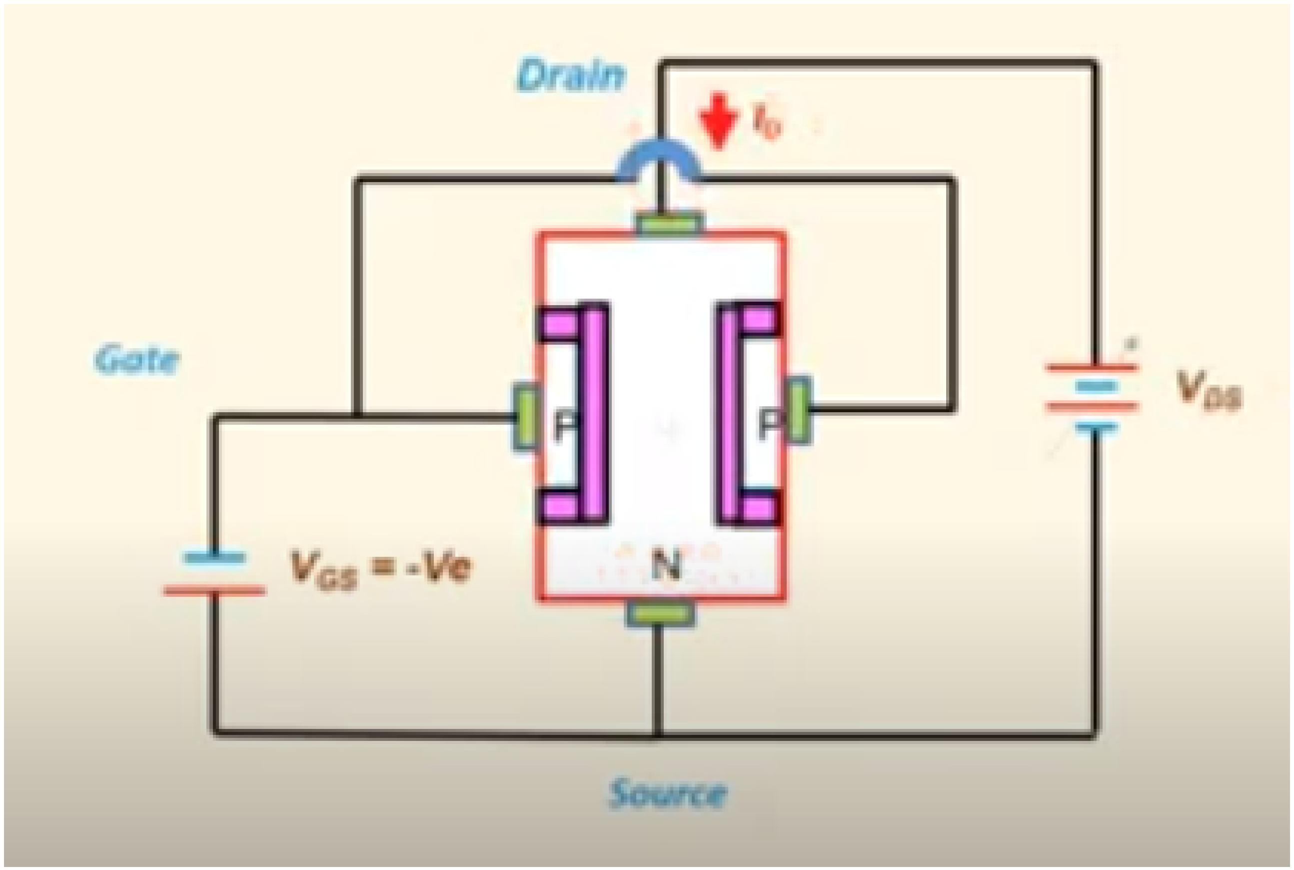


Drain
I_D
Gate
P
N
P
$V_{DS} = V_{DD}$ (+Ve)
$V_{GS} = 0$
Source

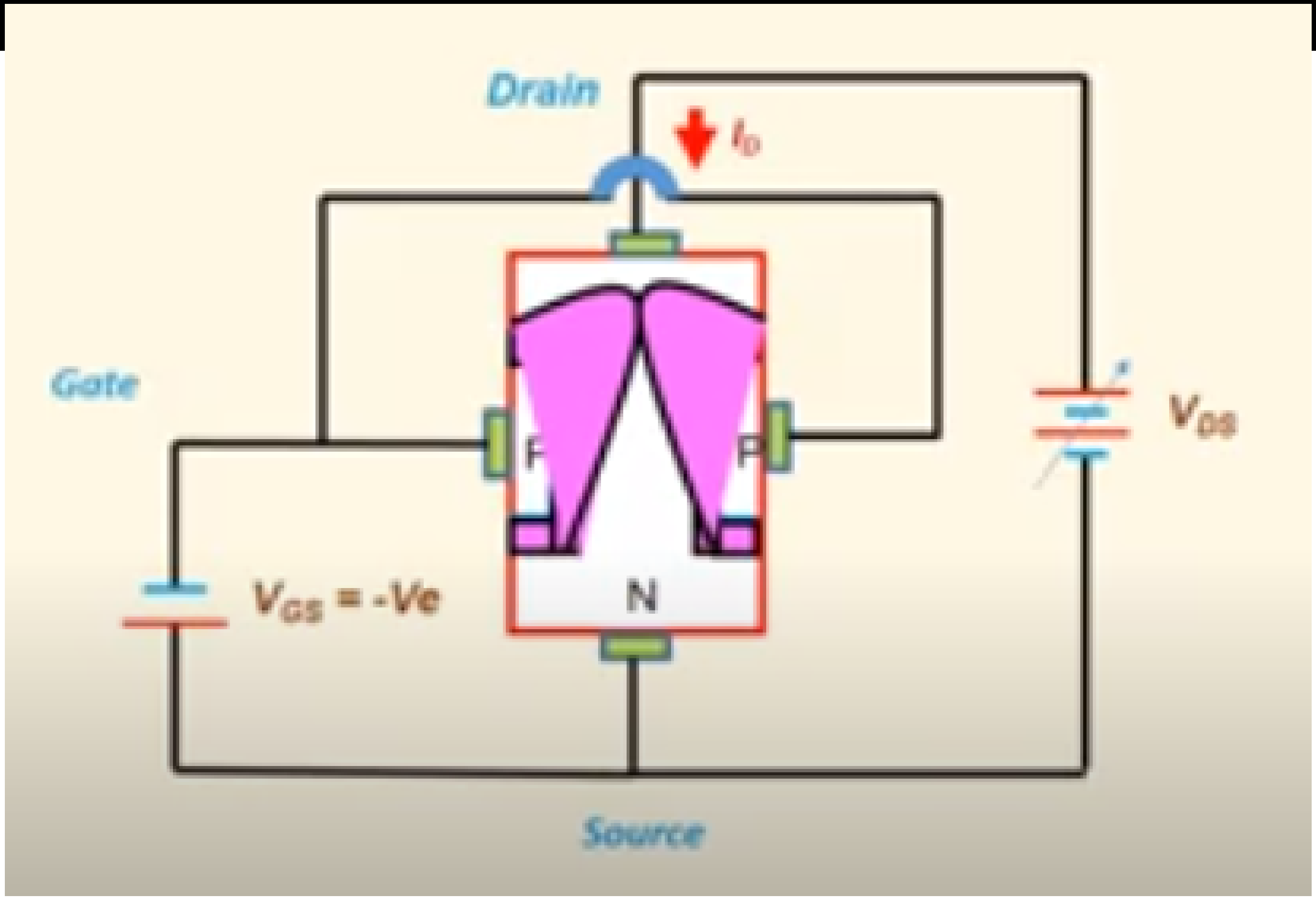

Drain
I_D
Gate
P
P
N
$V_{GS} = 0$
$V_{DS} = V$
Source



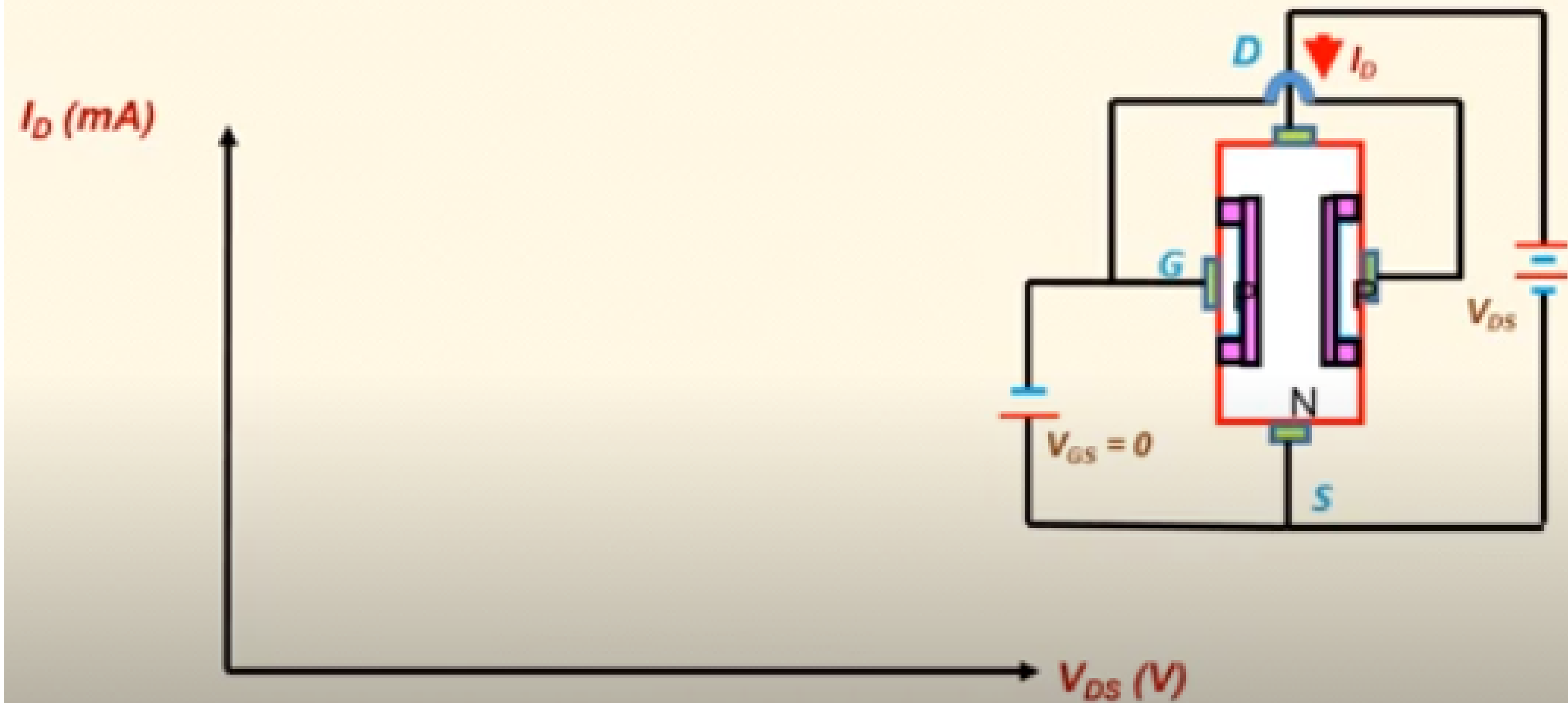
Drain
$I_D = I_{DSS}$
Gate
P
$V_{DS} = V_P$
N
$V_{GS} = 0$
Sourc



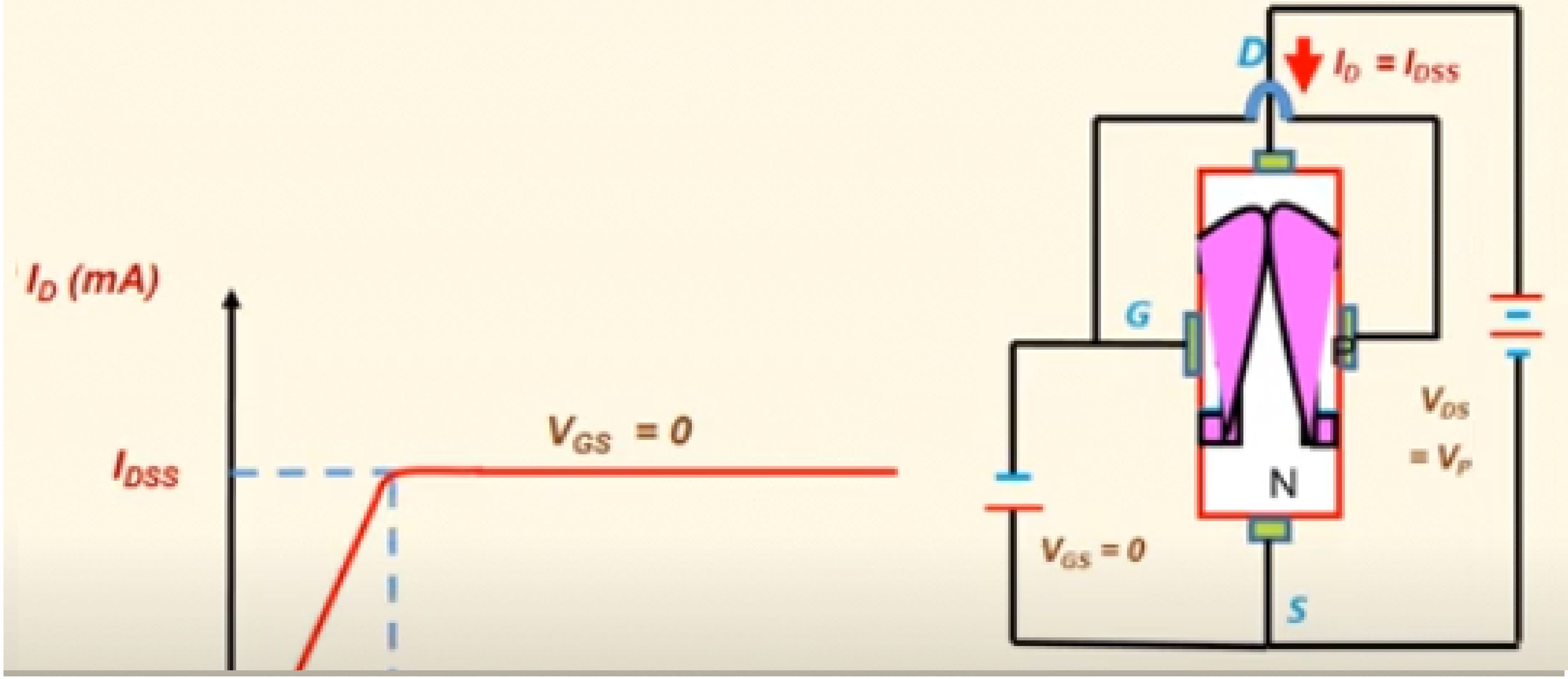
Drain
I_D
Gate
P
P
N
V_{GS} = -Ve
V_{DS}
Source

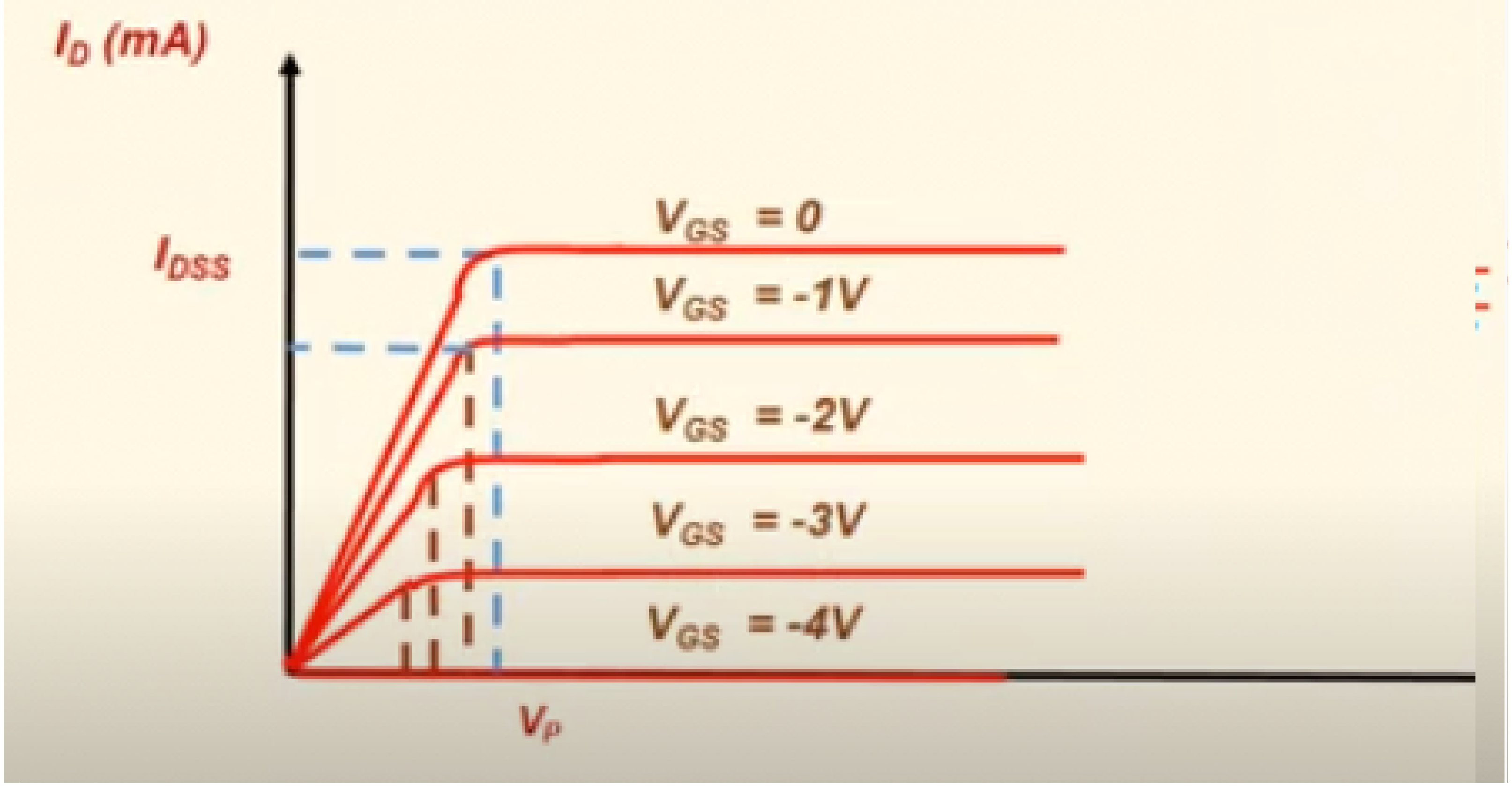

Drain
I_D
Gate
P
P
N
V_{GS} = -Ve
V_{DS}
Source

➤ *Relation between output current I_D and output voltage V_{DS}*

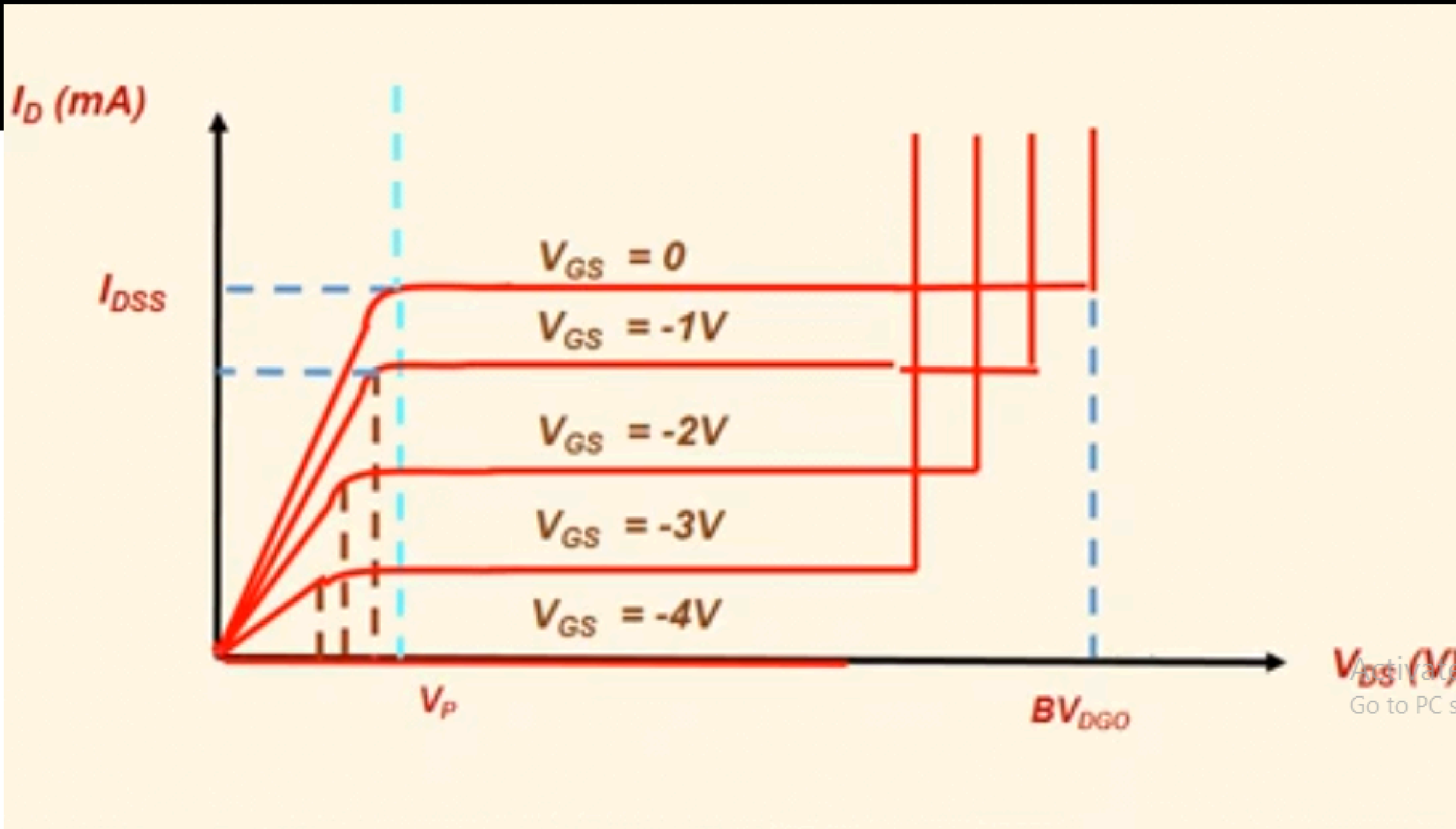


➢ Relation between output current I_D and output voltage V_{DS}

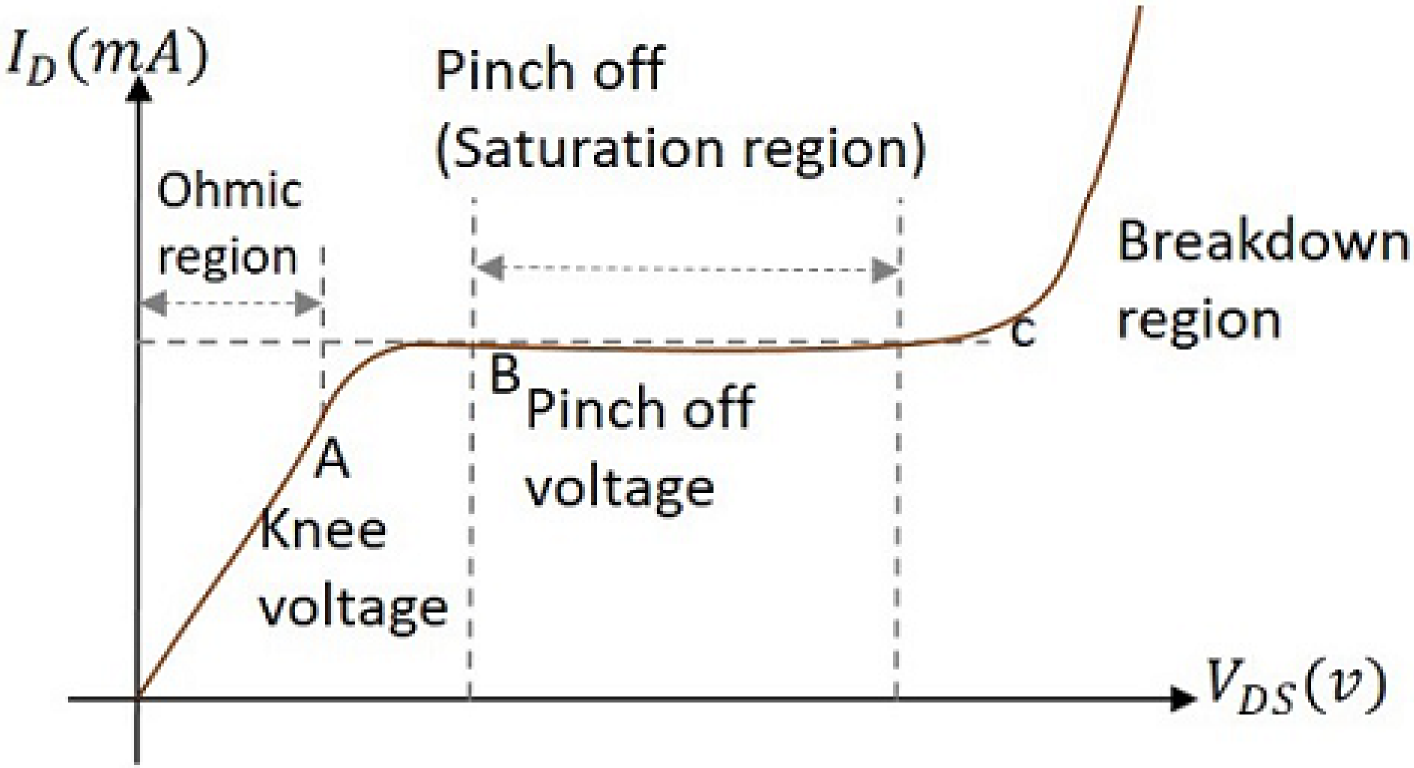


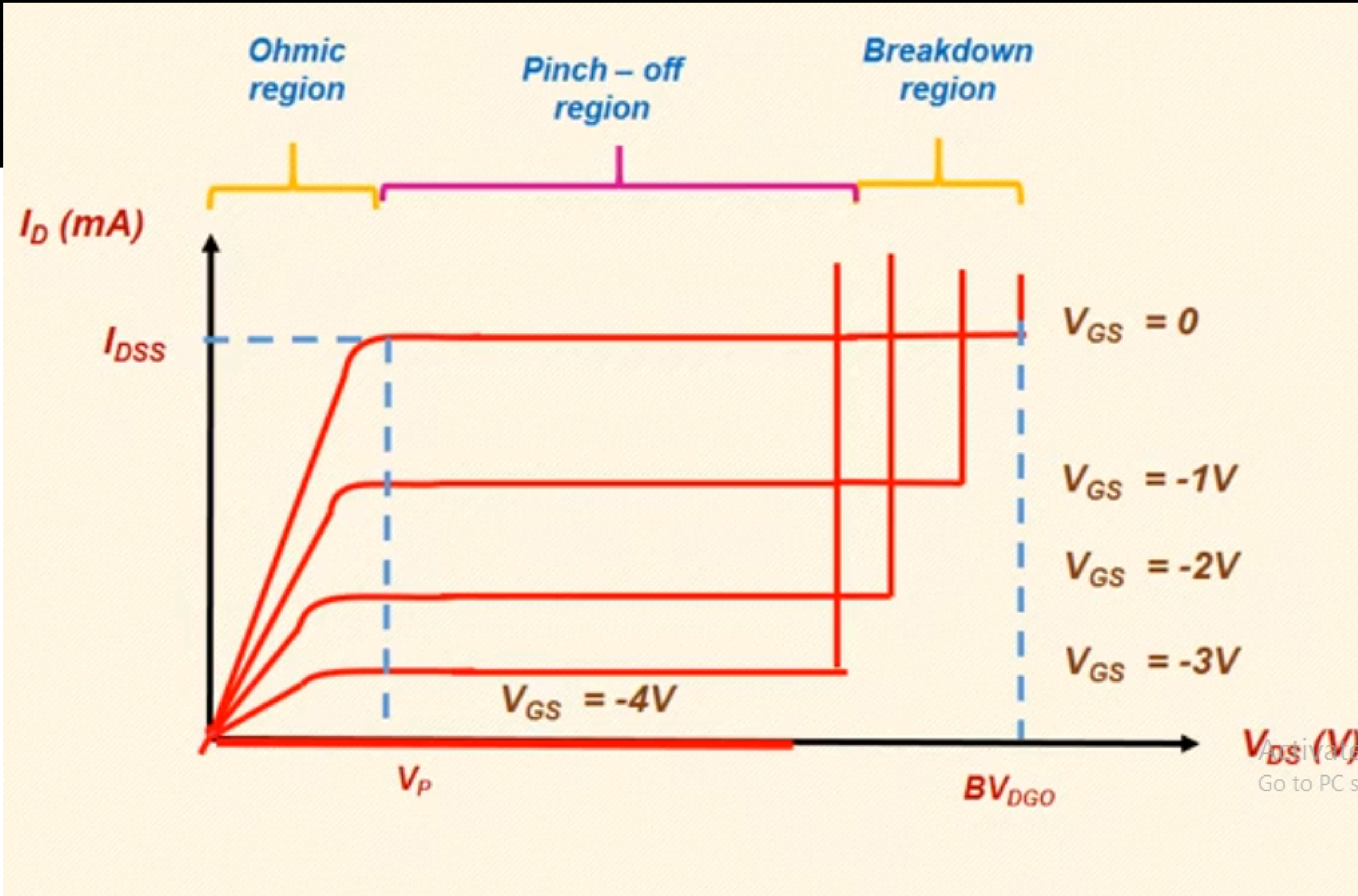


I_D (mA)
I_{DSS}
V_{GS} = 0
V_{GS} = -1V
V_{GS} = -2V
V_{GS} = -3V
V_{GS} = -4V
V_P



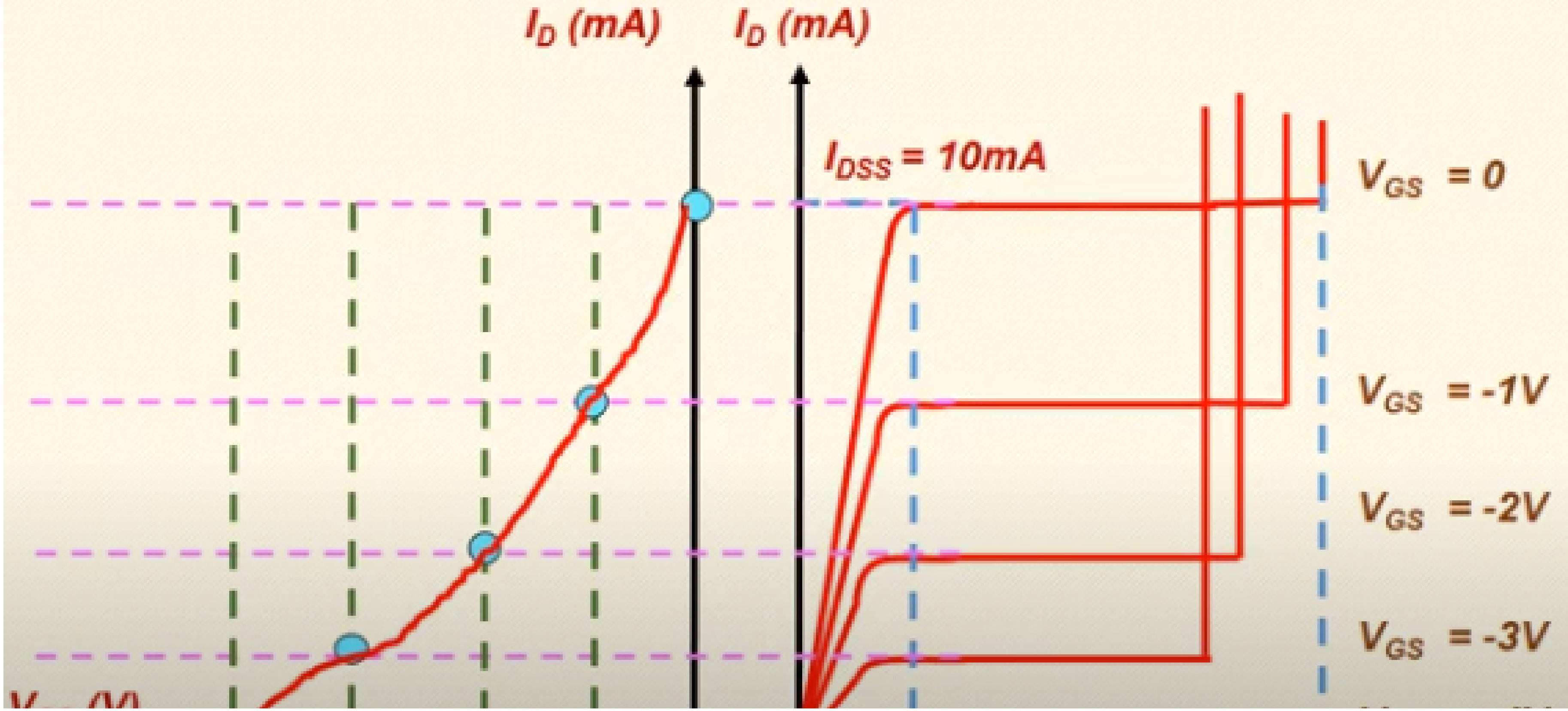
I_D (mA)
I_{DSS}
V_{GS} = 0
V_{GS} = -1V
V_{GS} = -2V
V_{GS} = -3V
V_{GS} = -4V
V_P
BV_{DGO}
V_{DS} (V)


$I_D(mA)$
Pinch off
(Saturation region)
Ohmic
region
Breakdown
region
c
B
Pinch off
voltage
A
Knee
voltage
$V_{DS}(v)$



Ohmic region
Pinch – off region
Breakdown region
I_D (mA)
I_{DSS}
V_{GS} = 0
V_{GS} = -1V
V_{GS} = -2V
V_{GS} = -3V
V_{GS} = -4V
V_{DS} (V)
V_P
BV_{DGO}

Transfer Characteristics of FET from Drain characteristics



JFET Parameters

Electrical behavior is described in terms of the parameters of the Device. They are obtained from the characteristics. Important Parameters for FET are

1. DC Drain resistance
2. AC drain Resistance
3. Transconductance

JFET Parameters

1. DC Drain resistance : Defined as Ratio of Drain to source Voltage V_{DS} to Drain current $I_{D.}$ Also called static or Ohmic Resistance
2. Mathematically

$$R_{DS} = V_{DS}/I_{D}$$

JFET Parameters

1. AC Drain resistance : Defined as the resistance between Drain to source when JFET is operating in Pinch off Region or saturation Region
2. Mathematically

$$r_D = \frac{\Delta V_{DS}}{\Delta I_D}$$ When V_{GS} is constant

JFET Parameters

1. Transconductance (g_m): It is given by the ratio of small change in drain current to the corresponding change in the Gate to source Voltage VGS. Also known as Forward Transmittance
2. Mathematically

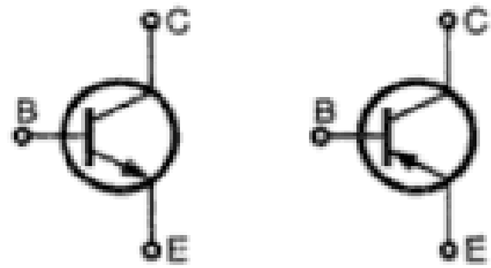
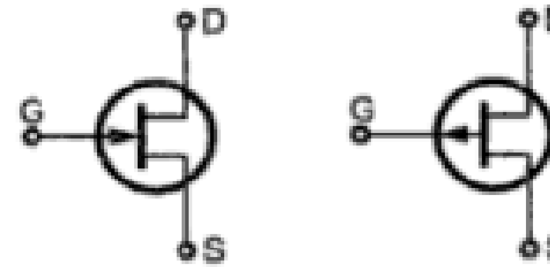
$$g_m = \frac{\Delta I_D}{\Delta V_{DS}}$$

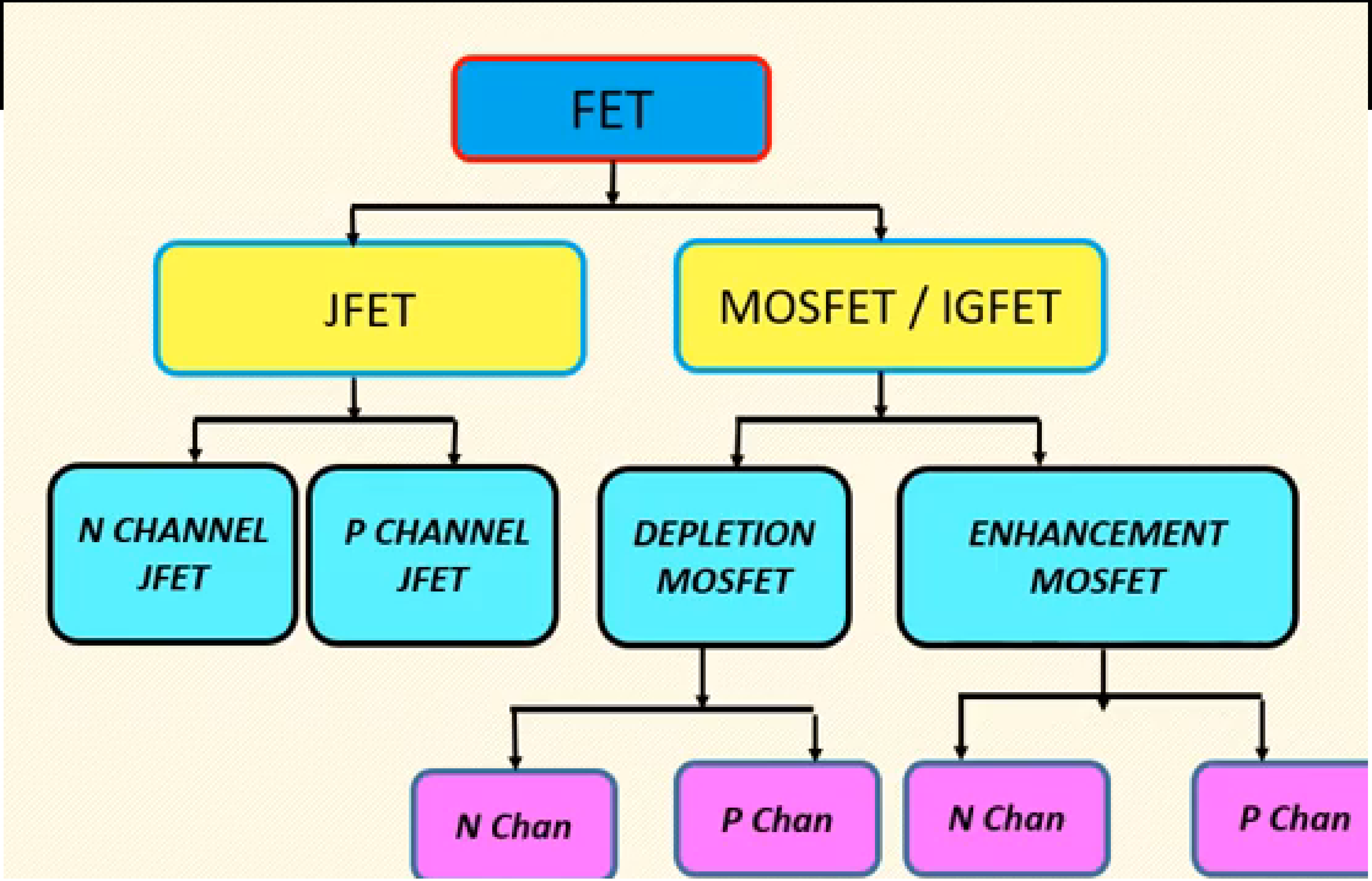
FET APPLICATIONS

Phase shift oscillators: The high input impedance of FET is especially valuable in phase shift oscillator to minimize the loading effect.

In voltmeters: The high input impedance of FET is useful in voltmeters to act as an input stage.

	JFET	BJT
1.	Unipolar device (current conduction is only due to one type of majority carrier either electron or hole).	Bipolar device (current condition, by both types of carriers, i.e., majority and minority-electrons and holes)
2.	The operation depends on the control of a junction depletion width under reverse bias.	The operation depends on the injection of minority carriers across a forward biased junction.
3.	Voltage driven device. The current through the two terminals is controlled by a voltage at the third terminal (gate).	Current driven device. The current through the two terminals is controlled by a current at the third terminal (base).
4.	Low noise level.	High noise level.
5.	High input impedance (due to reverse bias).	Low input impedance (due to forward bias).
6.	Gain is characterised by	Gain is characterized by voltage gain.

Sr. No.	Parameter	BJT	FET
1	Control element	Current controlled device. Input current I_B controls output current I_C.	Voltage controlled device. Input voltage V_{GS} controls drain current I_D.
2	Device type	Current flows due to both, majority and minority carriers and hence **bipolar device.**	Current flows only due to majority carriers and hence **unipolar device.**
3	Types	npn and pnp	n-channel and p-channel.
4	Symbols	 npn pnp	 n-channel p-channel
5	Configurations	CE, CB, CC	CS, CG, CD
6	Input resistance	Less compare to JFET.	High compare to BJT.
7	Size	Bigger than JFET.	Smaller in construction than BJT, thus making them useful in integrated - circuits (IC).
8	Sensitivity	Higher sensitivity to changes in the applied signals.	Less sensitivity to changes in the applied voltage.
9	Thermal stability	Less	More
10	Thermal runaway	Exists in BJT, because of cummulative effect of increase in I_C with temperature, resulting increase in temeperature in the device.	Does not exist in JFET, because drain resistance r_d increases with temperature, which reduces I_D, reducing the I_D and hence the temperature of the device.


FET
JFET
MOSFET / IGFET
N CHANNEL JFET
P CHANNEL JFET
DEPLETION MOSFET
ENHANCEMENT MOSFET
N Chan
P Chan
N Chan
P Chan

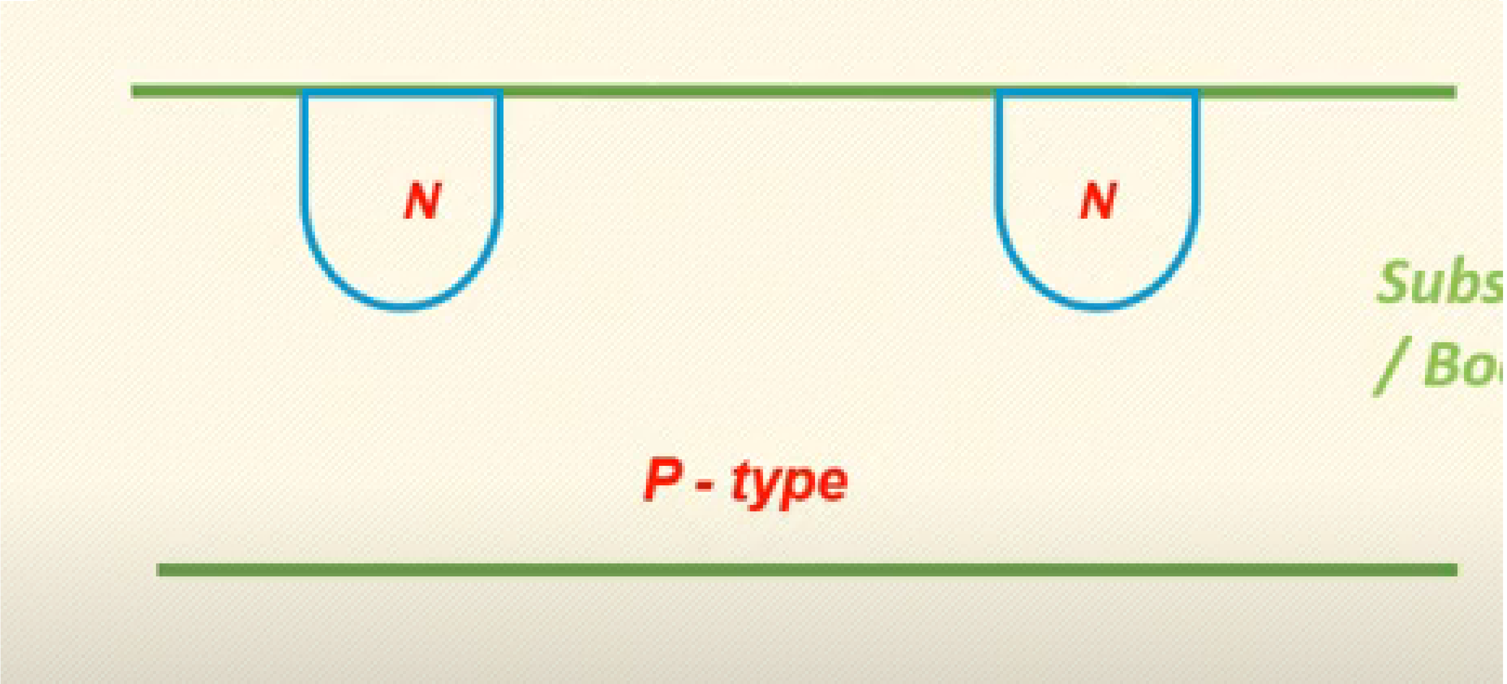
MOSFET (Metal oxide semiconductor field effect transistor)

- MOSFET is an important semiconductor device and is widely used in many circuit application.

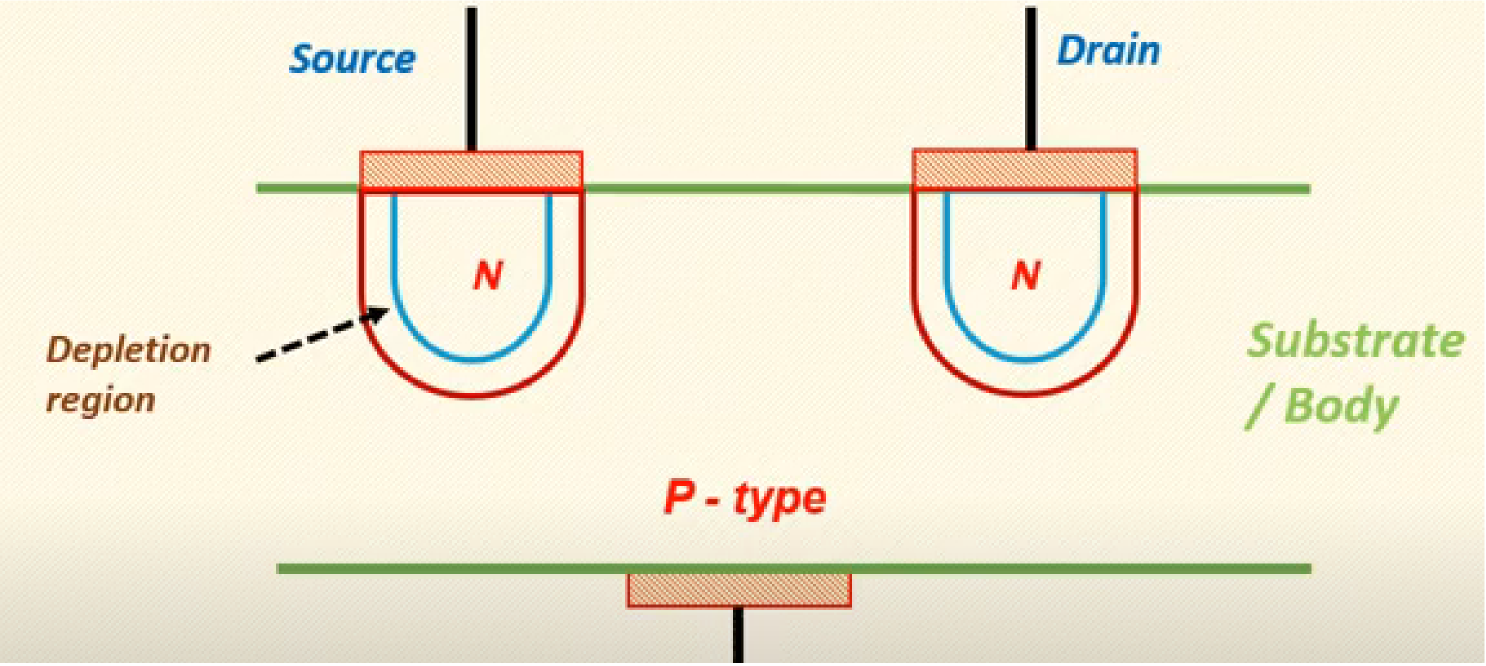
- The input impedance of a MOSFET is much more than that if a FET because of very small leakage current.
- MOSFETs has much greater commercial Importance than JFET

Construction of N channel MOSFET

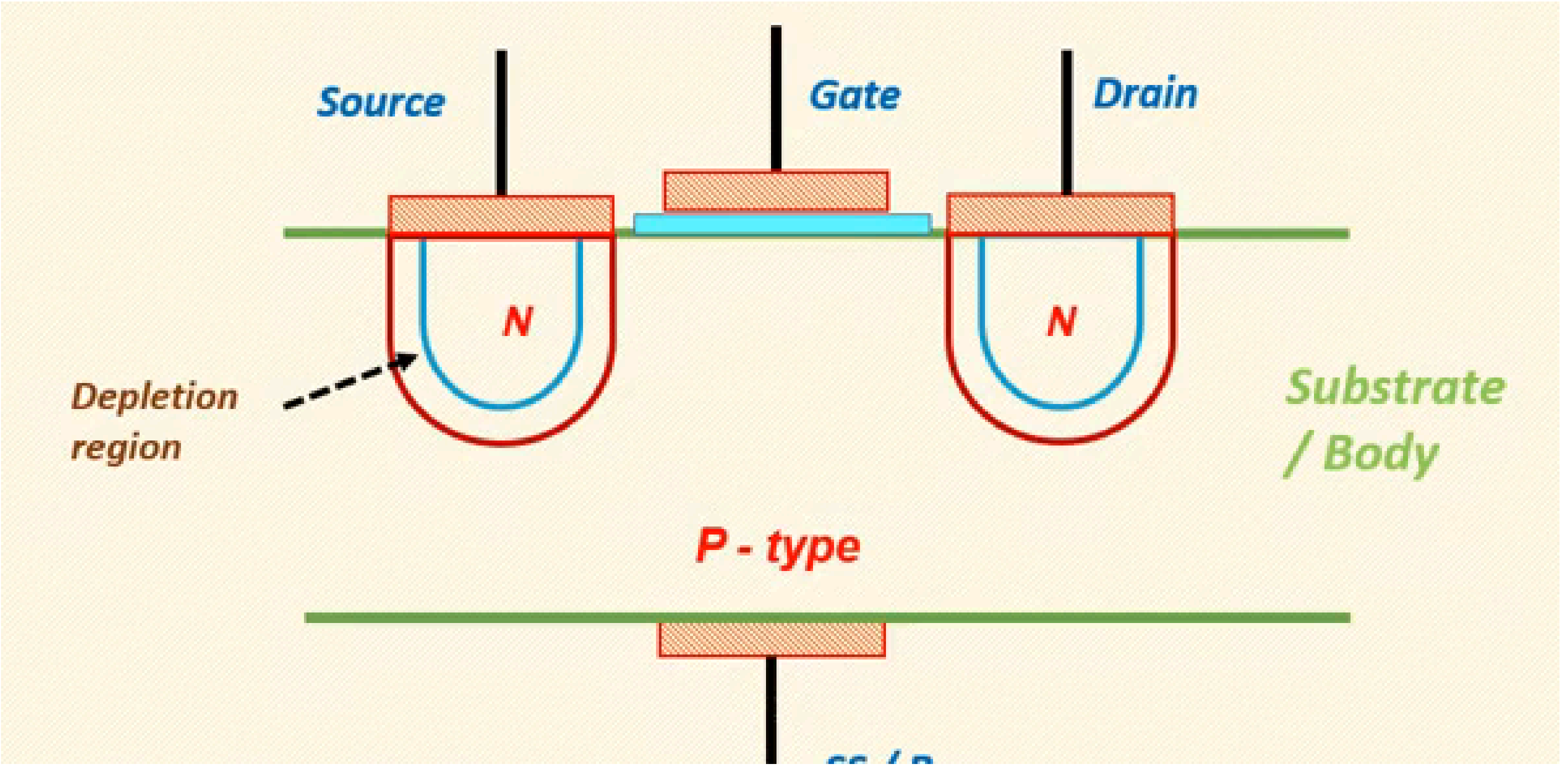
N channel MOSFET

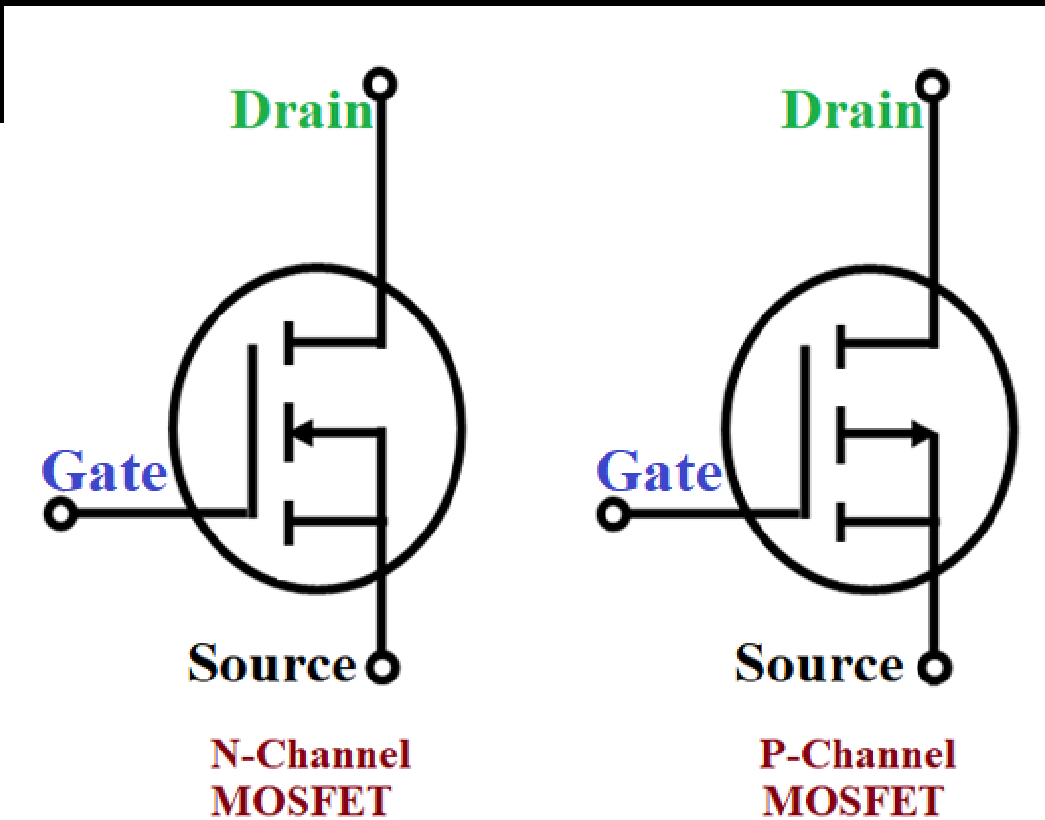


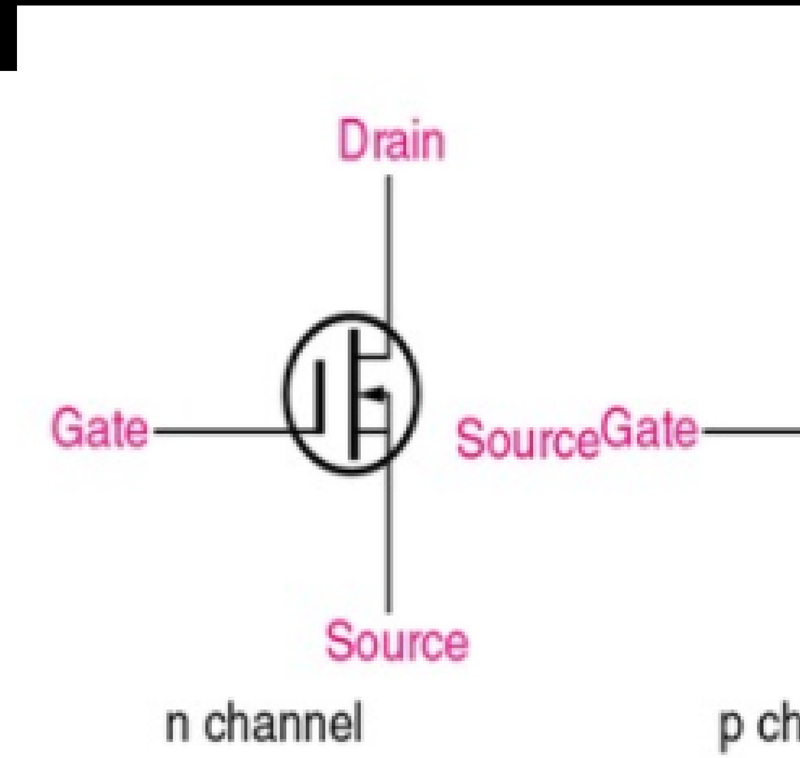
N channel MOSFET-depletion region formation

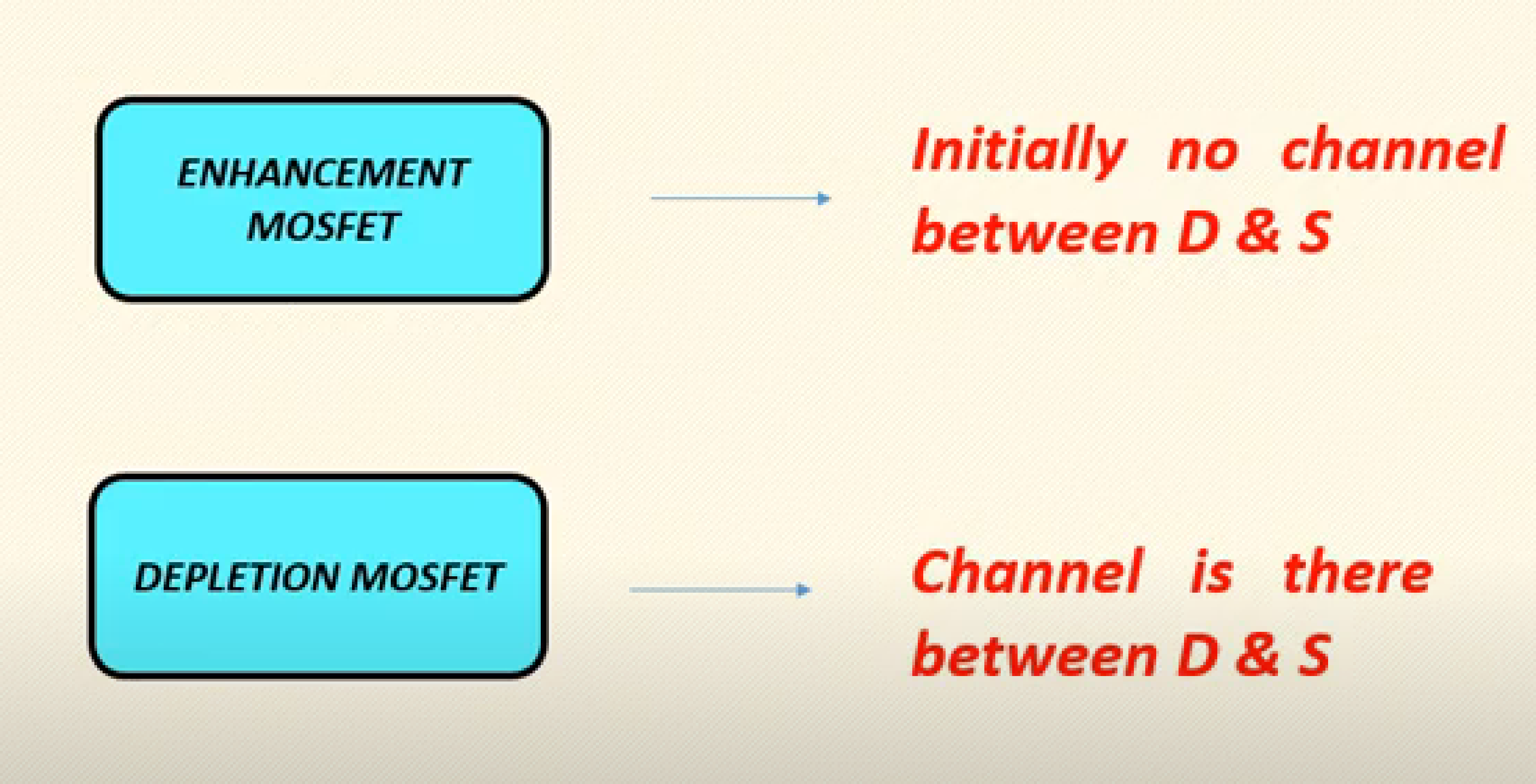


N channel MOSFET-region for name :



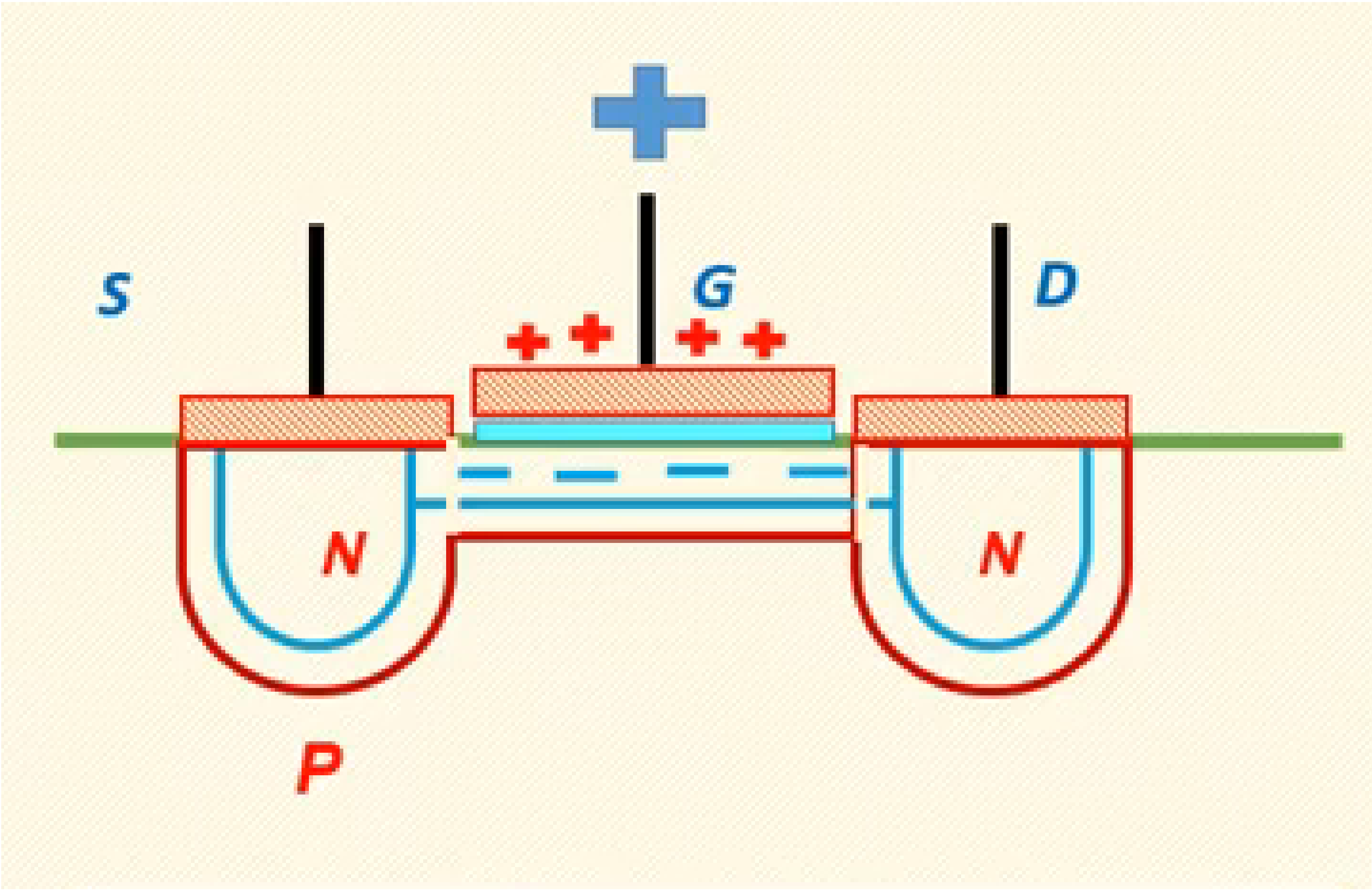

Drain
Gate
Source
N-Channel
MOSFET
Drain
Gate
Source
P-Channel
MOSFET


Drain
Gate
Source
Gate
Source
n channel

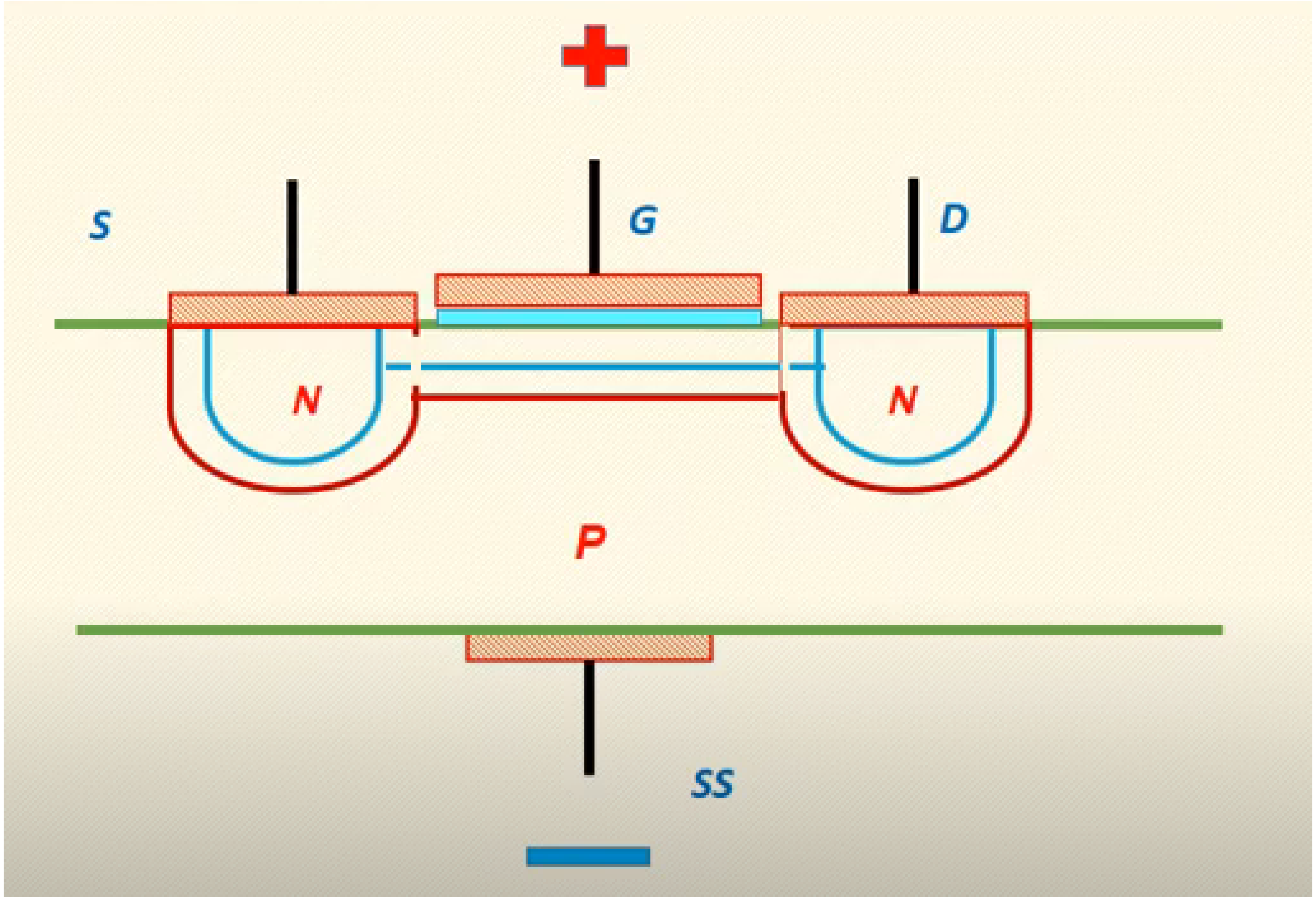


MOSFET Types

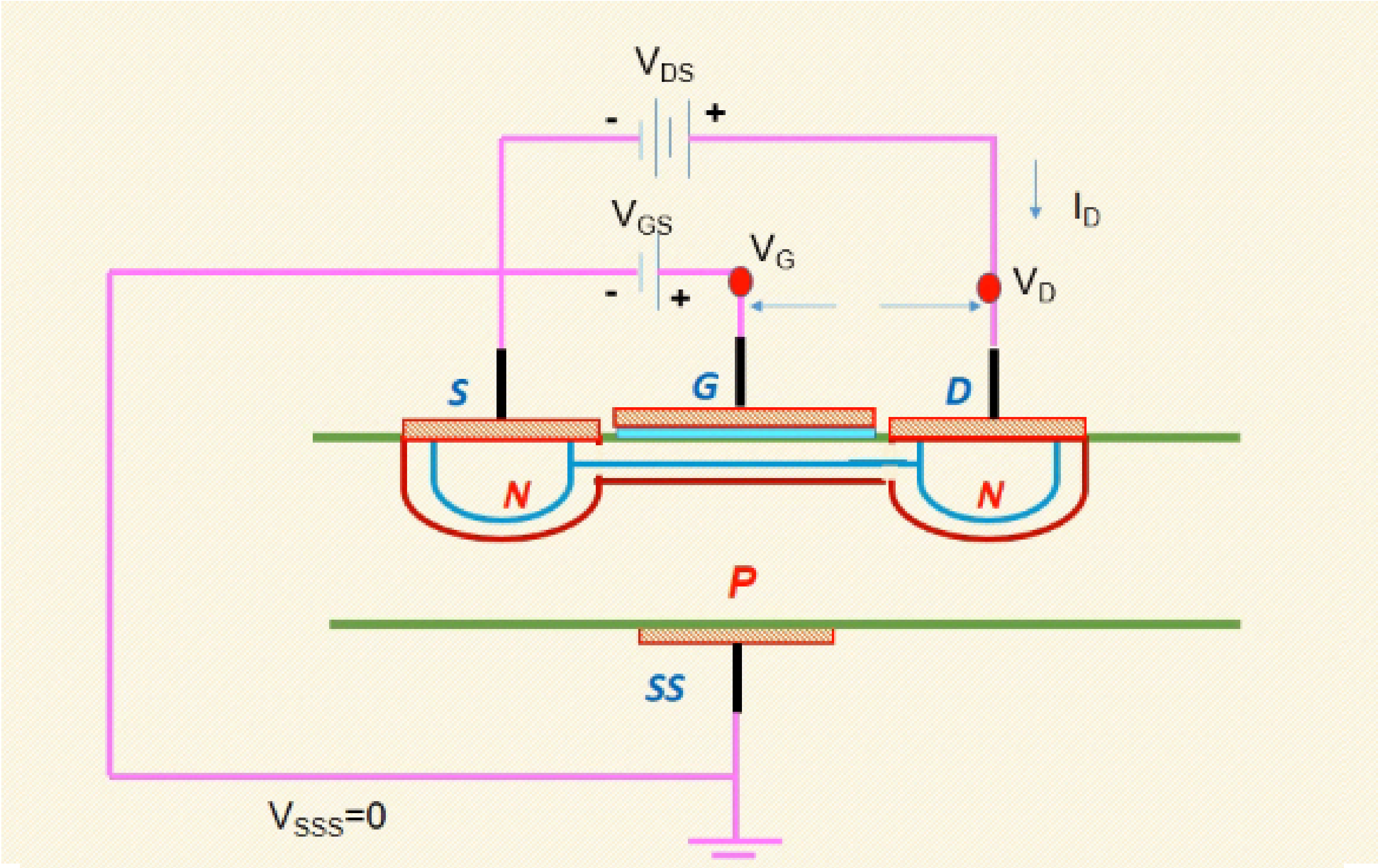
To create channel between drain and souce



Final N channel enhancement type MOSFET



Working of enhancement of MOSFET

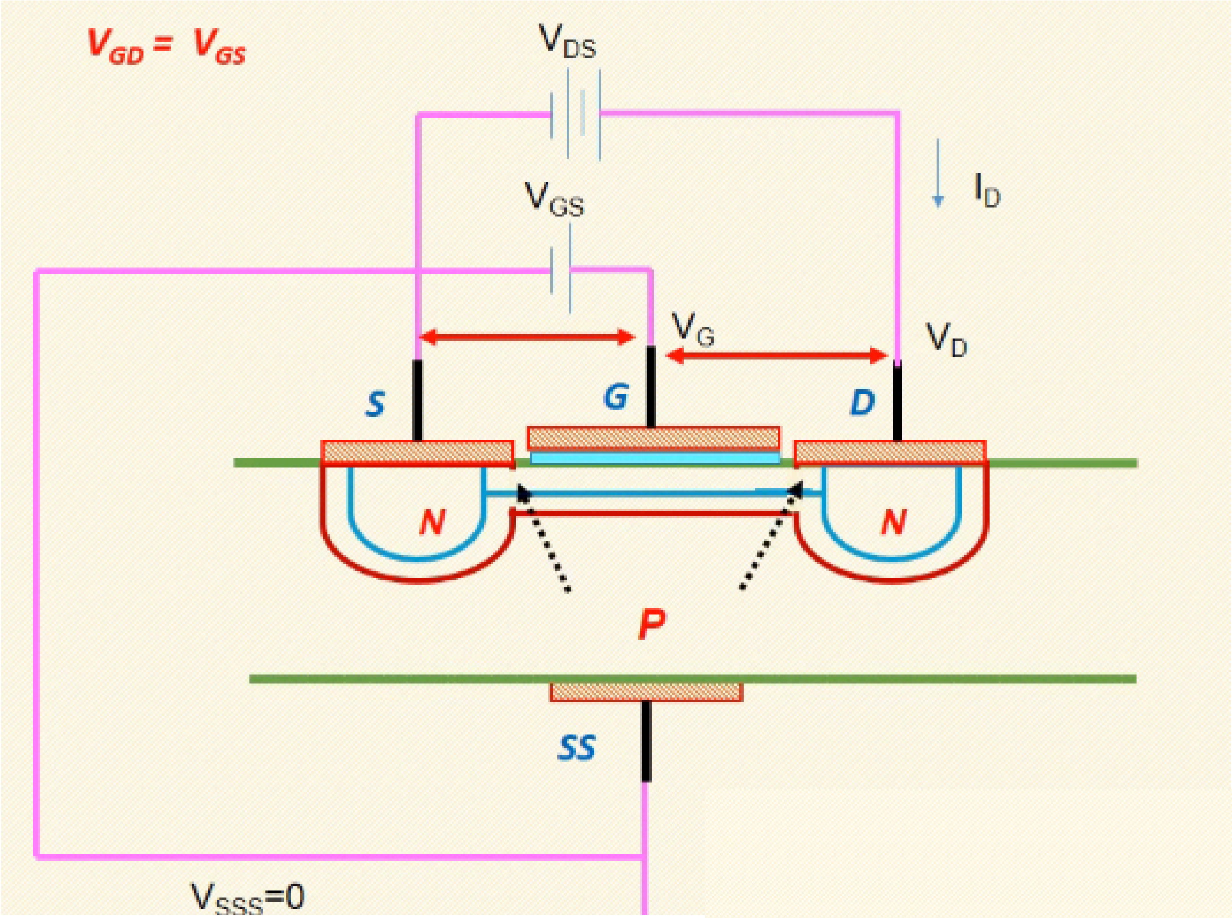


CASE I:

$V_{GD} = V_{GS} - V_{DS}$

Case 1 : $V_{DS} = 0V$

$V_{GD} = V_{GS}$



Uniform dep.reg

CASE II :

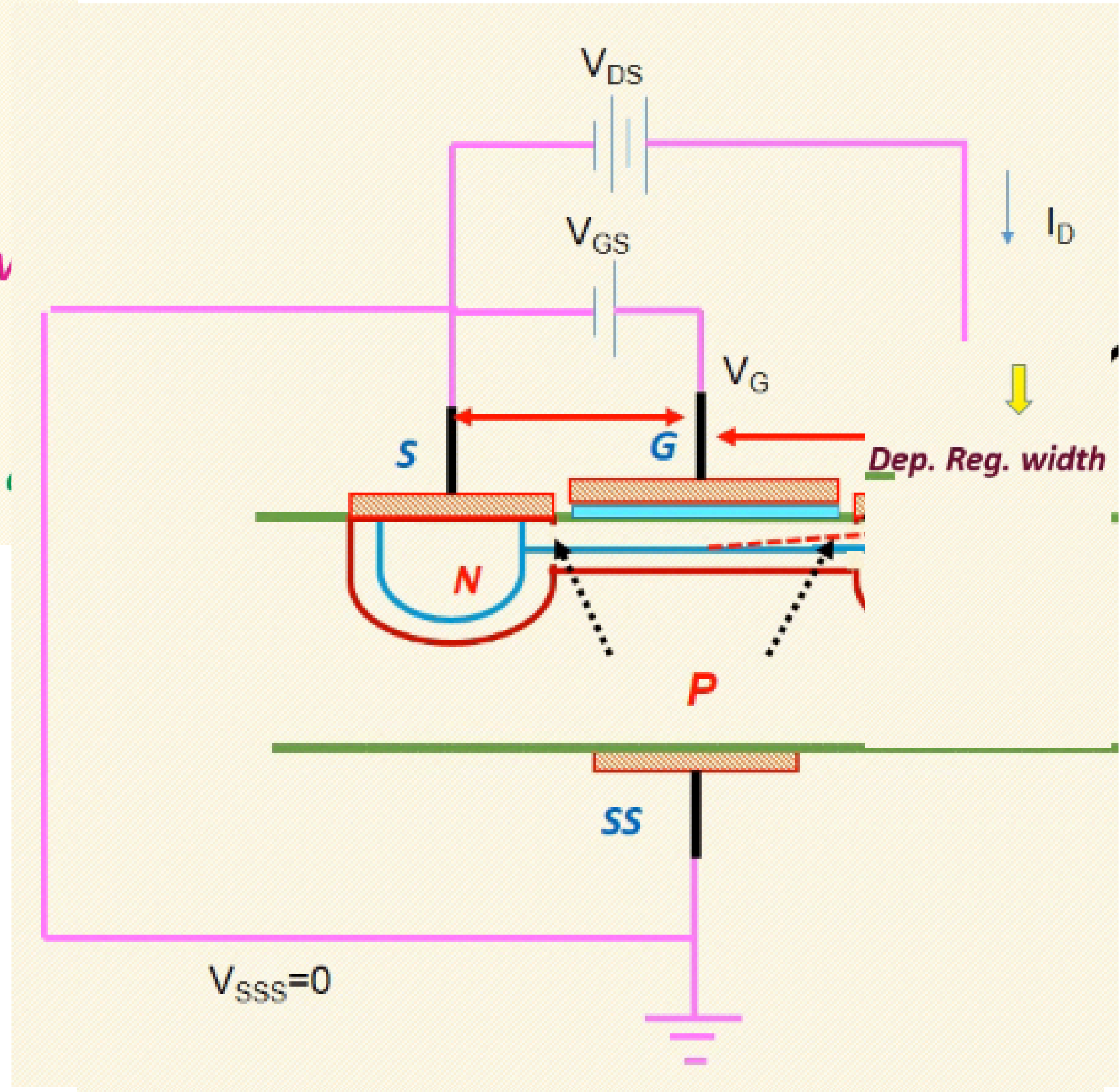
$V_{GD} = V_{GS} - V_{DS}$

Case 2 : V_{DS} > 0V

$V_{DS} \uparrow$ ⟹ $V_{GD} \downarrow$ V_{GD} = V

Drain becomes more +ve than Gate

$V_{GD} \neq V_{GS}$ ⟹ *No Uniform*



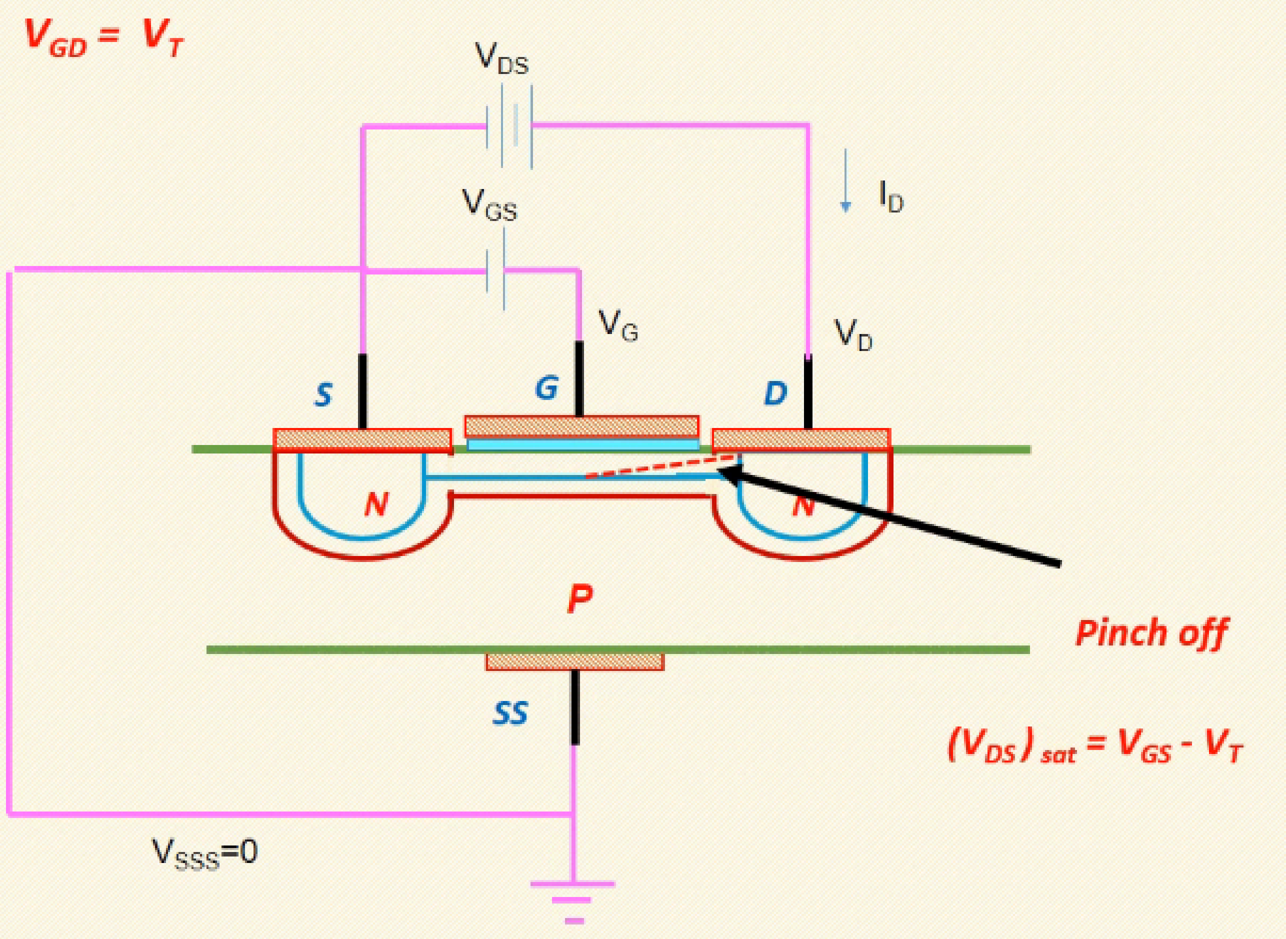
CASE III:

$V_{GD} = V_{GS} - V_{DS}$

Case 3 : $V_{DS} = V_{GS} - V_T$

$V_{GD} = V_{GS} - V_{GS} + V_T$

$V_{GD} = V_T$



Case 1 : $V_{DS} = 0V$

$V_{GD} = V_{GS}$ — Uniform dep.reg

$V_{GS} > V_T$ — Chan. width is sufficient for Current flow

Case 2 : $V_{DS} > 0V$

$V_{DS} \uparrow \Rightarrow V_{GD} \downarrow$

$V_{GD} < V_{GS}$ — Non - Uniform dep.reg

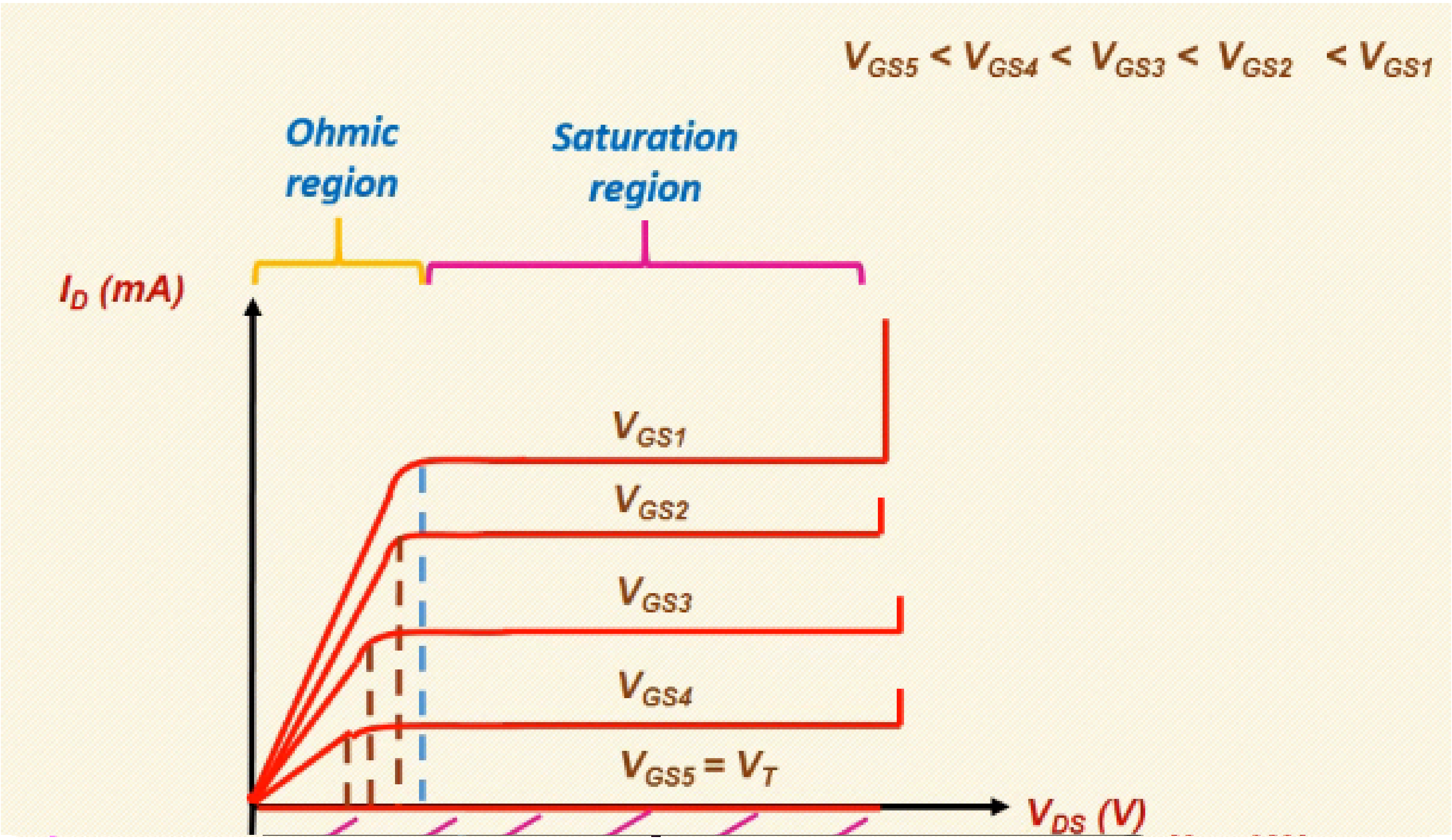
Chan. Width $\downarrow$

Case 3 : $V_{DS} = V_{GS} - V_T$

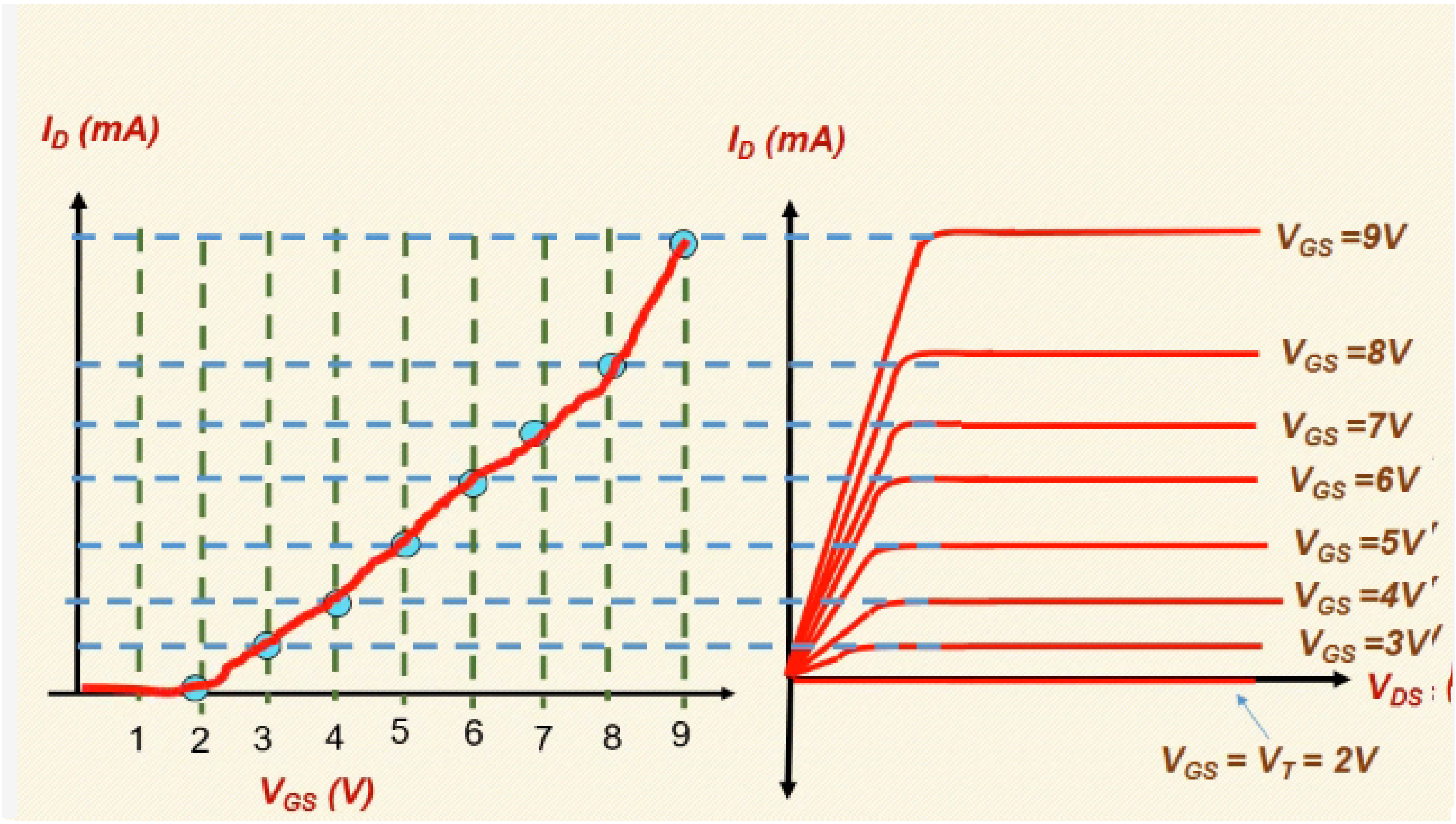
$V_{GD} = V_T$ — Pinch off

Current Constant

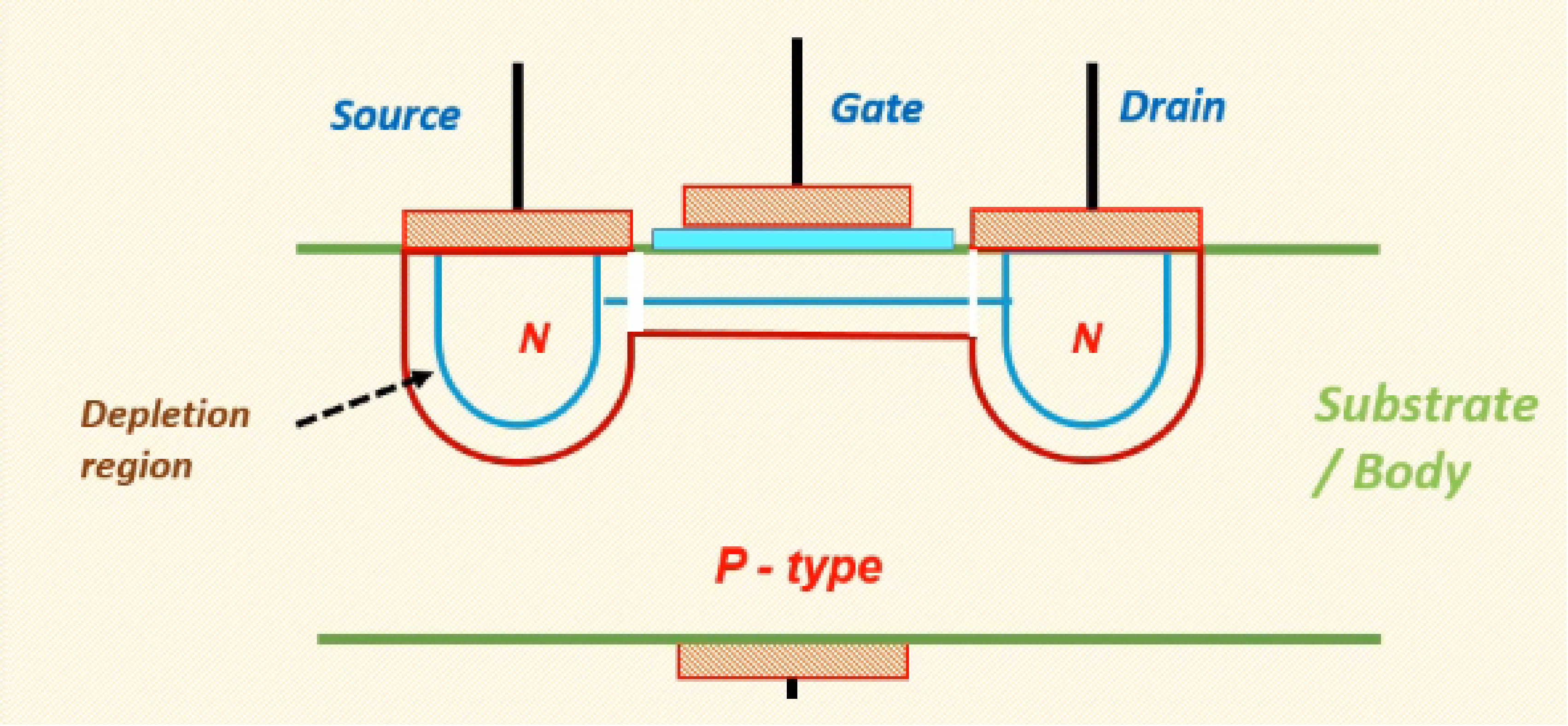
Drain characteristic of Enhancement type MOSFET



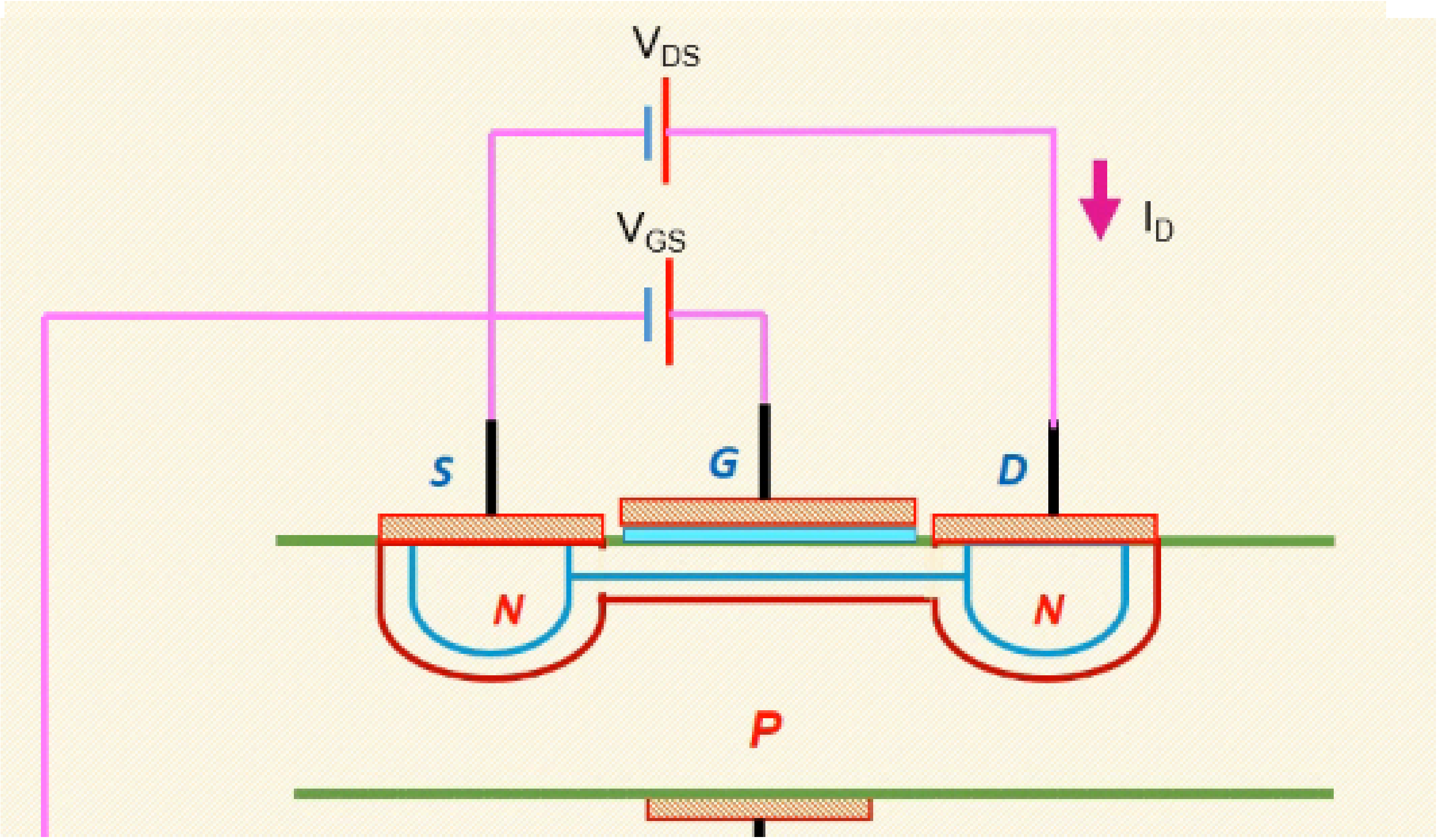
Transfer characteristic of Enhancement type MOSFET



Depletion type N channel MOSFET

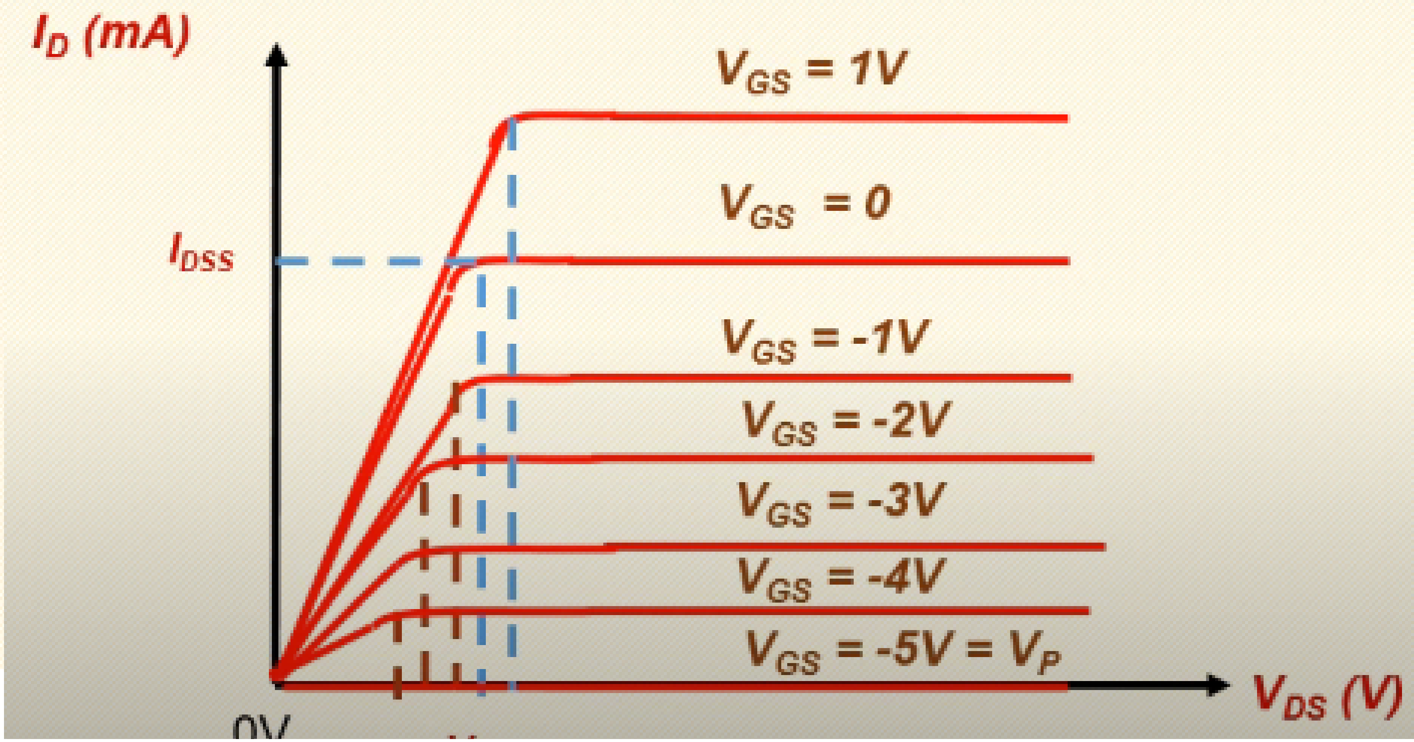


Working of Depletion type N channel MOSFET



Drain characteristic of depletion type MOSFET

- *Relation between output current I_D and output voltage V_{DS}*



Transfer characteristic of depletion type MOSFET