AN016
CC1000 / CC1050 used with on-off keying

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Keywords

- *CC1000, CC1050*
- *OOK - On-Off Keying*
- *ASK – Amplitude Shift Keying*
- *RSSI – Received Signal Strength Indicator*
- *Data slicer*

Introduction

The CC1000 and CC1050 products from Chipcon are highly integrated multichannel FSK (Frequency Shift Keying) transceivers and transmitters respectively. However, in some applications OOK (On-Off Keying) or ASK (Amplitude Shift Keying) are required.

FSK is a kind of FM (Frequency Modulation) used in digital transmission systems. Changing the frequency of the signal transfers the information. On the other hand, AM (Amplitude Modulation) carries information by changing the amplitude of the signal.

OOK is a type of amplitude modulation used in digital systems where the RF carrier is turned on and off in order to modulate the data. Manchester coding and 1/3 – 2/3 coding are popular coding schemes using this modulation technique.

ASK is also amplitude modulation, but in this case the carrier is not turned complete off. The most common ASK scheme is to shift the amplitude between two levels (2-level ASK).

This application note gives a typical application circuit for OOK/ASK. The implementation of an analogue data decision slicer is discussed in some detail. For 868 MHz operation a typical sensitivity of –107 dBm @2.4 kbit/s data rate is possible using the proposed circuitry.

Chipcon is a supplier of RFICs for all kinds of short range communication devices. Chipcon has a world-wide distribution network.

OOK modulation through the programming interface

The CC1000/1050 power amplifier (PA) is enabled through the configuration interface. By switching the PA on and off, OOK modulation can be generated

In order to turn off the PA the *TX_PD* bit in the *MAIN* register could be reconfigured. The PA is disabled when *TX_PD* = 1. Refer to the data sheet for details. Table 1 gives typical CC1000 parameters.

Parameter	434 MHz	869 MHz
Modulation depth	50 dB	70 dB

Table 1. CC1000 OOK parameters when programming *MAIN* register.

The modulation speed is only restricted by the microcontroller. The microcontroller must be able to reconfigure the CC1000/1050 in less than one bit-period. 16 bits must be transferred from the MCU in order to change the *MAIN* register. Using a datarate of 1.2 kbit/s the bit duration is 833 us. Transferring 16 bits in 833 us takes a clock frequency (PCLOCK) of 19.2 kHz. If 10 instruction cycles are used for each clock, then it is possible to use a microcontroller running at 192 kHz to achieve 1.2 kbit/s. To achieve higher modulation data rates, the minimum microcontroller speed must be increased accordingly.

ASK modulation through the programming interface

The CC1000/1050 PA output power is set through the configuration interface. By switching the PA output power, ASK modulation can be generated. Compared to OOK, the ASK is using a modulation depth less than maximum. Switching between two different power settings sets the modulation depth.

In order to change the output power of the PA the *PA_POW* register must be reconfigured. Refer to the data sheet for details.

Again the modulation speed is only restricted by the microcontroller. The microcontroller must be able to reconfigure the CC1000/1050 in less than one bit-period. 16 bits must be transferred from the MCU in order to change the *PA_POW* register. The speed requirement for the microcontroller is as for the OOK case above.

Modulation by switching PA supply voltage

Another way to do OOK / ASK modulation is to switch the power (AVDD) of the PA stage. If we insert a switching transistor between the supply voltage and the CC1000/1050 PA power pin (pin5 for CC1000, pin 1 for CC1050), then the output power can be modulated. A simplified schematic is shown in Figure 1.

The transistor should be a PNP or pMOS with low voltage drop that can be switched by a logic signal from the microcontroller. This solution puts less demand on the microcontroller speed, but involves a small extra cost in the additional transistor.

The modulation depth at 868 MHz is measured as typically 47 dB. In these measurements the CC1000 Evaluation Board was used but with separate power for the PA supply voltage.

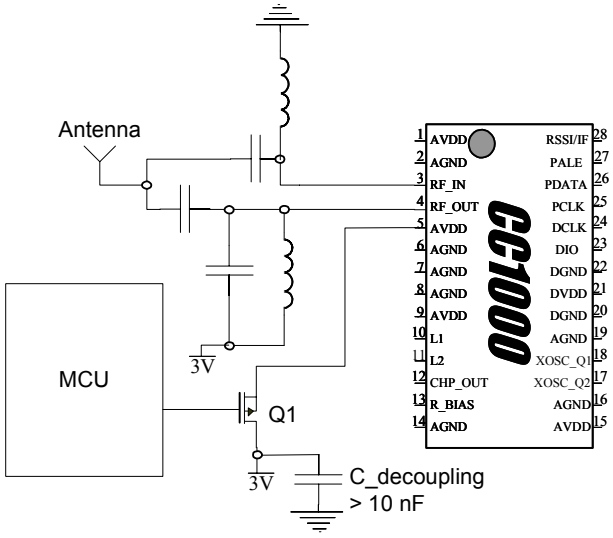

Figure 1. OOK / ASK modulation by switching PA supply voltage.

The PA supply voltage de-coupling capacitors must be connected on the 'battery-side' of the switch (see Figure 1). In order to achieve a clean spectrum the capacitor value must be chosen larger than 10 nF.

Table 2 gives the CC1000 modulation bandwidth for different data rates at 868 MHz. The modulation bandwidth is defined as the –36 dBm bandwidth for maximum output power (5 dBm).

Data rate (kbit/s)	Modulation bandwidth (kHz)
1.2	160
2.4	160
4.8	240
9.6	380

Table 2. CC1000 868 MHz modulation bandwidth.

Receiving OOK and ASK signals

Although the CC1000 is intended for FSK demodulation it can also be used for OOK and ASK demodulation due to its internally integrated RSSI (Received Signal Strength Indicator). The RSSI output (IF/RSSI pin) is enabled trough the *FRONT_END* register. The IF/RSSI output is a current output and must be terminated in a resistor to give a voltage that is inversely proportional to the incoming signal strength. The RSSI signal should be connected to a comparator, or it can be sampled by an ADC and used for further signal processing. See the data sheet for further details on the RSSI output.

OOK / ASK demodulation

The voltage at the RSSI-pin will change according to the input signal level. Figure 2 shows a typical plot of the CC1000 RSSI voltage as a function of input power.

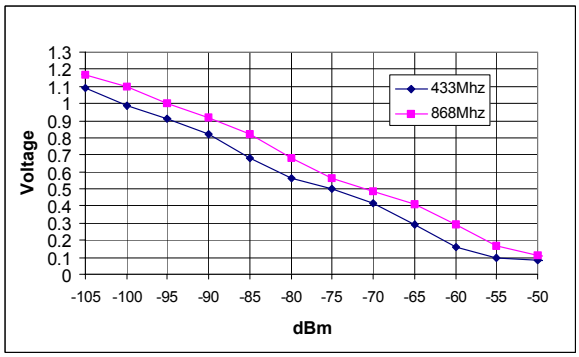

Figure 2. CC1000 RSSI voltage vs. input power.

We can determine if the input signal corresponds to a logic 1 or 0 by comparing the RSSI-voltage with a reference level. At 868 MHz the reference level should be between approximately 1.1 V and 0.1 V. This results in the following requirements:

1) The minimum logic 1 is –107 dBm (logic 0 is then –152 dBm assuming 45 dB modulation depth).
2) The maximum logic 0 is –55 dBm (logic 1 is then –10 dBm assuming 45 dB modulation depth).

The RSSI signal can be connected to a comparator, or it can be sampled by an ADC and used for further signal processing. The ADC should preferably be integrated in the MCU. Both these methods require that a reference level be established. In order to set the correct reference level a balanced preamble is required. The bit pattern should be '010101010….'.

If an ADC is used the average between the two digital numbers during the preamble will be the reference level.

If a comparator is employed a network similar to Figure 3 could be used. The reference level is then found using an analouge 2^{nd} order Sallen-Key low-pass filter connected between the comparator and the RSSI output. This filter is preceded by a simple RC-filter.

For NRZ coded data, the reference level must be sampled during the preamble and held after the preamble. The LOCK_AVG_FILTER (CHP_OUT pin) output can be used as a control signal for the sample-and-hold circuit. Since Manchester coded data is dc balanced there is no need for a sample-and-hold circuit in this case.

The comparator could have hysteresis to minimize multiple transitions as the input swings through the threshold region. The comparator in Figure 3 is implemented using a similar op amp to the one used in the low-pass filter. This keeps the component count down. The op amp must have minimum 0.1 – 1.3 V input common-mode range.

Close to the sensitivity limits the difference (in V) at the RSSI output between logic 0 and 1 is very small (only a few mV). The inclusion of hysteresis in the comparator is not recommended in this case. A better approach is to perform oversampling of the comparator output and filter the noise by using a majority vote decision.

Simple RC-filter

The simple RC-filter (R1 and C1) should have a cut-off frequency f_c less than the IF-frequency but higher than the data rate. R1 should be fixed at 27 kΩ in order to set the desired RSSI

sensitivity. A good choice is to set the cut off frequency equal to 1.5 times the data rate in *bit/s* (= half the Baud rate for Manchester coded data).

As an example, for a 19.2 kbit/s data rate choose the cut off frequency as 28.8 kHz. Since R1 is 27 kΩ select C1 as 180 pF.

For improved sensitivity an additional low-pass (R6 and C6) filter can be connected between the R1C1-filter and the comparator input to attenuate the 150 kHz IF-frequency further. A good choice is to set the cut off frequency equal to 3 times the data rate in *bit/s*.

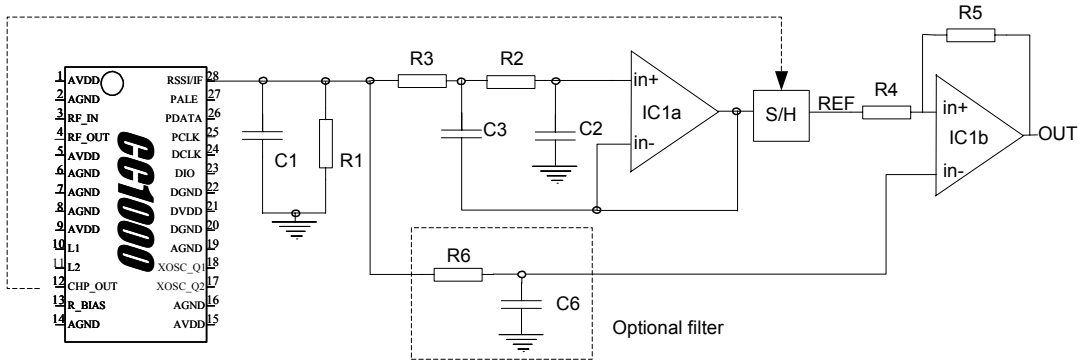

Figure 3. Analouge data slicer. S/H can be omitted for Manchester coded data.

Sallen-Key low pass filter
An active filter can be used to improve data filtering. For a Butterworth response in a Sallen-Key configuration, use equal resistances and 2:1 capacitors. Choose a value for the capacitor C2 and set the desired 3 dB cut off frequency (f_c). The latter should be significantly lower than the preamble data rate. There exists a trade-off between the accuracy of the reference level (i.e. filter amplitude response) and the filter response time (i.e. the required number of preambles). 6.9 time constants $(\tau = 1/2\pi \cdot f_c)$ are required for the reference frequency to settle to within 0.1% of final value. A good compromise is to set the cut off frequency to 1/20th of the data rate in *bit/s* (= half the Baud rate for Manchester coded data).

Design equations for the Sallen-Key filter are as follows:

$$R2 = R3 = \frac{1}{2\pi\sqrt{2} \cdot f_c C2} \quad ; \quad C3 = 2 \cdot C2$$

As an example, for a 19.2 kbit/s data rate the preamble will be a square wave of 9.6 kbit/s. Choose the cut off frequency as 960 Hz and C2 as 220 pF. R2 = R3 is then 560 kΩ and C3 = 470 pF. 0.1% settling accuracy requires 23 preambles in this case.

Comparator
Design equations for the comparator with hysteresis are as follows:

$$High\_Threshold = \frac{(OUT - REF) \cdot R4}{R4 + R5} + REF \qquad Low\_Threshold = REF \cdot \frac{R5}{R4 + R5}$$

- OUT is the maximum comparator output voltage
- REF is the reference level
- Hysteresis is given by the difference in the two threshold levels

As an example: For 3 V supply voltage and 20 mV hysteresis, R4 = 6.8 kΩ and R5 = 1 MΩ.

Bill of materials

	Data rate (kbit/s)					
Reference	**1.2**	**2.4**	**4.8**	**9.6**	**19.2**	**38.4**
C1	3.3 nF	1.5 nF	820 pF	390 pF	180 pF	100 pF
C2	220 pF	220 pF	220 pF	220 pF	220 pF	220 pF
C3	470 pF	470 pF	470 pF	470 pF	470 pF	470 pF
C6	150 pF	82 pF	39 pF	22 pF	10 pF	4.7 pF
R1	27 kΩ	27 kΩ	27 kΩ	27 kΩ	27 kΩ	27 kΩ
R2, R3	8.2 MΩ	3.9 MΩ	2.2 MΩ	1.0 MΩ	560 kΩ	270 kΩ
R6	270 kΩ	270 kΩ	270 kΩ	270 kΩ	270 kΩ	270 kΩ
IC1a, IC1b	TS912	TS912	TS912	TS912	TS912	TS912
Q1	SI9424DY	SI9424DY	SI9424DY	SI9424DY	SI9424DY	SI9424DY

Table 3. Bill of materials for analogue data slicer and switch.

Measurements

Sensitivity
Measurements were performed at 869 MHz with the analogue data slicer. The key parameters are summarized below. Note that the data rate is specified in bit/s.

Data rate (kbit/s)	C1	C6	Sensitivity without R6C6-filter (dBm)	Sensitivity with R6C6-filter (dBm)
1.2	3.3 nF	150 pF	-108	-109
2.4	1.5 nF	82 pF	-107	-107
19.2	180 pF	10 pF	-97	-97
38.4	100 pF	4.7 pF	-93	-93

Table 4. CC1000 868 MHz sensitivity measurement with 150 kHz IF-frequency (BER = 10^{-3}). Low current setting.

We note from Table 4 that the sensitivity drops for increasing data rates. The reason being that the IF-frequency is not sufficiently attenuated at high data rates. Hence for high data rates it might be advantageous that an ADC samples the RSSI output, and digital signal processing is used for data demodulation.

Crystal frequency accuracy
The worst case frequency error between the transmitter and receiver is given by

$$f_{error} = \pm 2 \cdot XTAL\_ppm \cdot f_{RF}$$

where XTAL_ppm is the total accuracy of the crystal including initial tolerance, temperature drift, loading and ageing, f_{RF} is the RF operating frequency. Ideally the IF-frequency should be 150 kHz, but due to the crystal accuracy the IF-frequency will be

$$f_{IF} = 150\ kHz \pm 2 \cdot XTAL\_ppm \cdot f_{RF}$$

Figure 4 shows the sensitivity versus IF-frequency offset for 2.4 kbit/s data rate.

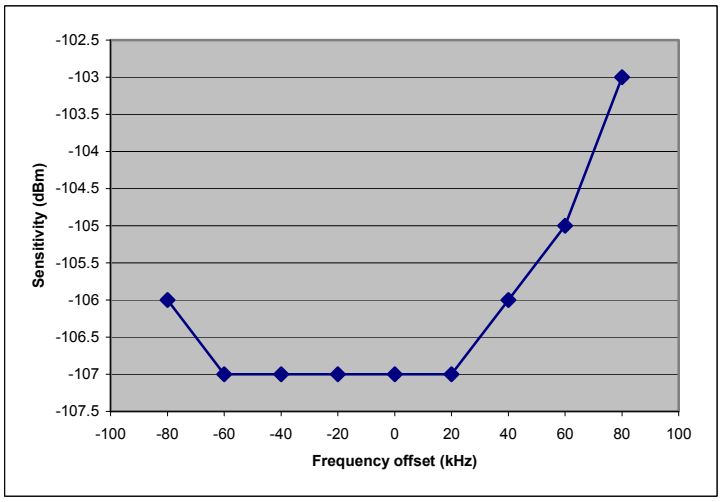

Figure 4. Sensitivity versus IF-frequency for 2.4 kbit/s data rate. R6C6 filter used.

Blocking performance

Figure 5 shows the ratio in dB of the highest level of an unwanted signal to the level of the wanted signal, which is set to 3 dB above sensitivity limit, without degrading the sensitivity. Up to ±900 kHz offset the unwanted signal is AM modulated. From ±1 MHz to ±10 MHz offset the unwanted signal is unmodulated (CW). The carrier frequency of the wanted signal is kept constant. The frequency separation in Figure 5 is the difference between the two channels. The minima in Figure 5 is due to 1) an unwanted modulated signal at the same frequency as the wanted modulated signal (co-channel rejection) and 2) the image frequency spaced 300 kHz above the wanted modulated signal. The blocking performance meets EN 300 220-1, Class 2 receiver requirements.

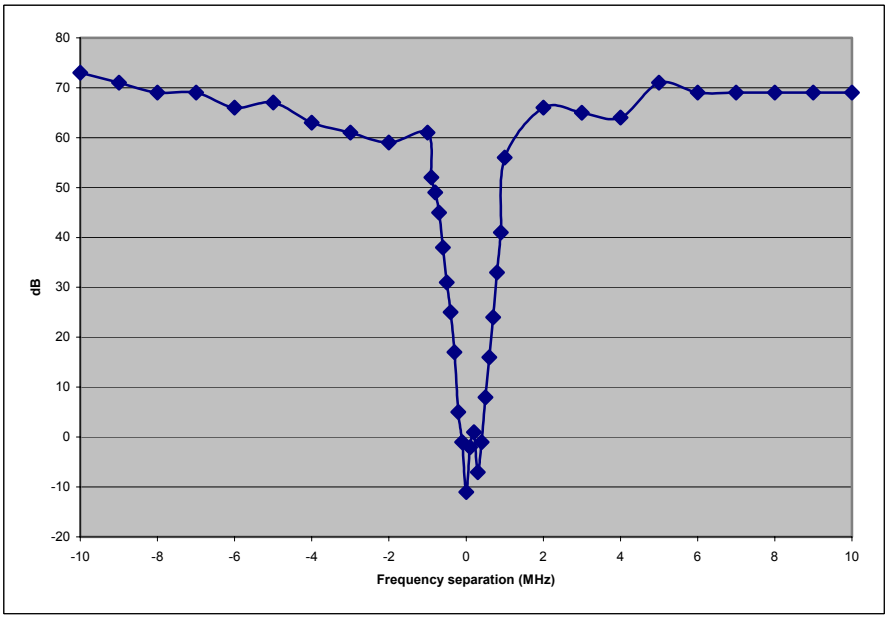

Figure 5. Selectivity/blocking for 2.4 kbit/s data rate. R6C6 filter used.

Configuration data

The SmartRF Studio software is used for generating configuration data. This software is developed for FSK operation, but can also be used for OOK/ASK by setting the frequency separation to 0. The data format and data rate options are not relevant for OOK/ASK operation. The RSSI output must be enabled.

It is possible to switch off the modem used in FSK operation by setting the *MODEM_RESET_N* bit in register *MODEM1* to logic 0. This reduces the current consumption in Tx by 100 uA. In Rx the reduction in current consumption is dependent on the data rate; for 2.4 kBaud and 76.8 kBaud there is a 100 uA and 350 uA reduction respectively.

Conclusion

Measurements using the proposed application circuit show that CC1000/CC1050 performs well for OOK/ASK operation. At 2.4 kbit/s data rate the sensitivity is typically –107 dBm @868 MHz, BER = 10^{-3}. The blocking performance is very good and complies with receiver class 2 requirements as defined in ETSI EN 300 220-1, section 9.3.

For high data rates (> 38.4 kbit/s) we suggest that a digital filter (ADC) is used. For low data rates an analogue filter could be used.

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