Hi3716M V430 Satellite HD Chip Brief Data Sheet

Key Specifications

CPU

- High-performance ARM Cortex-A7 processor
- Built-in I-cache, D-cache, and L2 cache
- Hardware Java acceleration
- Floating-point coprocessor

Memory Control Interfaces

- DDR3/DDR3L interface
  - Maximum capacity of 512 MB for an external DDR SDRAM or of 128 MB/256 MB for a built-in DDR SDRAM
  - 16-bit data width
- A SPI NOR flash/SPI NAND flash, a parallel SLC NAND flash, or a SPI NOR flash+a parallel SLC NAND flash

Video Decoding (HiVXE 2.0 Processing Engine)

- H.265 Main/Main 10@Level 4.1 high-tier
- H.264 BP/MP/HP@Level 4.2; MVC
- MPEG-1
- MPEG-2 SP@ML and MP@HL
- MPEG-4 SP@Levels 0–3, ASP@Levels 0–5, GMC, and MPEG-4 short header format (H.263 baseline)
- AVS baseline@Level 6.0 and AVS+
- VC-1 SP@ML, MP@HL, and AP@Levels 0–3
- VP6/VP8
- 1-channel 1080p@60 fps decoding

Image Decoding

JPEG decoding, supporting at most 64 MP

Audio Decoding

- MPEG L1/L2
- Dolby Digital/Dolby Digital Plus decoder-converter
- AAC-LC and HE-AAC V1/V2 decoding
- Downmixing, resampling, and automatic volume control

TS Demultiplexing/PVR

- Built-in DVB–S/S2/S2X demodulator
- Up to 4-channel TS input, or 3-channel TS+1-channel tuner input
- Up to 1-channel TS output
- Up to 96 hardware PID channels
- Recording of scrambled and non-scrambled streams

Security Processing

- Advanced CA feature
- OTP
- AES, DES, and 3DES data encryption and decryption

Graphics and Display Processing (Imprex 2.0 Processing Engine)

- Hardware TDE
- 3-layer OSD
- Two video layers
- 16-bit and 32-bit color depth
- Full-hardware anti-aliasing and anti-flicker
- IE, NR, and CCS
- DEI

Audio and Video Interfaces

- PAL, NTSC, and SECAM standard outputs, and forcible standard conversion
- Aspect ratio of 4:3 or 16:9, forcible aspect ratio conversion, and free scaling
- 1080p50(60)/1080i/720p/576p/576i/480p/480i output
- HD and SD output for the same source
- Color gamut compliant with the xvYCC (IEC 61966-2-4) standard
- HDMI 1.4b with HDCP1.4
- Analog video interfaces
  - One CVBS interface
  - One built-in VDAC
  - VBI
- Audio interface
  - Audio-left and audio-right channels
  - S/PDIF interface
  - One built-in ADAC
  - Output voltage swing up to 2 Vrms

Peripheral Interfaces

- Two USB 2.0 host interfaces (integrated with the PHY)
- One 10/100 Mbit/s adaptive Ethernet interface with an integrated FE PHY
- One UART interface
- Two SCIs that support T0/T1/T14 protocols, with one SCI supporting 5 V and 3 V cards
- One IR receiver
- One LED and keypad control interface
- Three I^2C interfaces
- Multiple groups of GPIO interfaces
- One CI/CI+ (optional)

Others

- Faster bootup time
- Integrated dedicated standby processor, with the chip standby power consumption less than 30 mW
- TFBGA package
- 2-layer or 4-layer PCB routing

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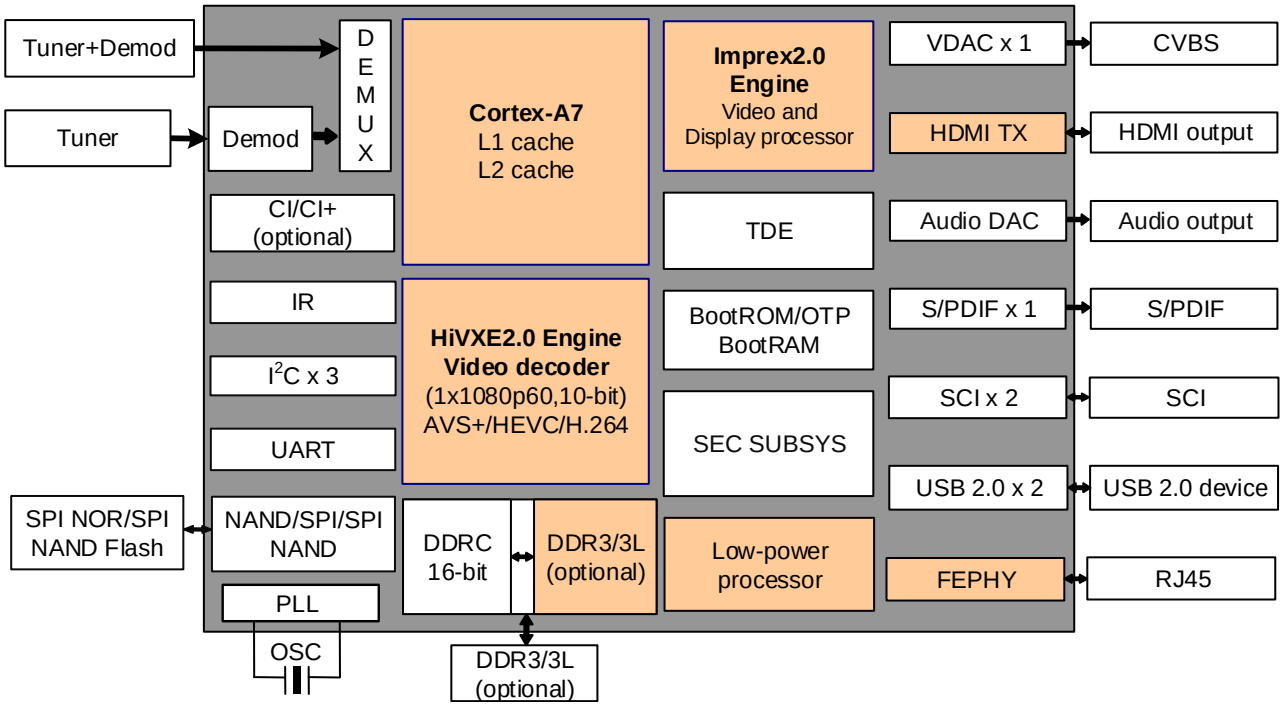
Functional Block Diagram



Hi3716M V430 is an FHD HEVC cost-effective STB chip solution launched by HiSilicon. It integrates the high-performance Cortex-A7 processor and TDE, and supports HD video decoding in various formats such as H.265, H.264, AVS+, MPEG-2, MPEG-4, VC-1, VP6, and VP8, and Dolby audio processing. Hi3716M V430 also provides flexible connection schemes with various peripheral interfaces such as one Ethernet interface and two USB 2.0 interfaces. It delivers the industry's best user experience in stream compatibility, smoothness and picture quality of live video playback, and STB performance.

NOTE

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Acronyms and Abbreviations

3DES	Triple Data Encryption Algorithm
AAC-LC	advanced audio coding low complexity
ADAC	audio digital-to-analog converter
AES	Advanced Encryption Standard
AMR-NB	adaptive multi-rate narrowband
AMR-WB	adaptive multi-rate wideband
APE	Monkey's Audio
AVS	Audio Video Standard/adaptive voltage scaling
CA	conditional access
CCS	cross-color suppression
CI	common interface
CVBS	composite video broadcast signal
DD	Dolby Digital
DDR	double data rate
DEI	de-interlacing
DES	Data Encryption Standard
DVB	Digital Video Broadcasting

DVB-T	Digital Video Broadcasting-Terrestrial
eMMC	embedded multimedia card
FE	fast Ethernet
FHD	full high definition
FLAC	free lossless audio codec
GMC	global motion compensation
GPIO	general-purpose input/output
HD	high definition
HDCP	High-bandwidth Digital Content Protection
HDMI	high definition multimedia interface
HE-AAC	high-efficiency advanced audio coding
HEVC	high efficiency video coding
IE	image enhancement
IF	intermediate frequency
I2C	inter-integrated circuit
I2S	inter-IC sound
IR	infrared
JPEG	Joint Photographic Experts Group
LED	light emitting diode
MP	megapixel
MPEG	Moving Picture Experts Group
MVC	multiview video coding
NR	noise reduction
NTSC	National Television System Committee
OSD	on-screen display
OTP	one-time programmable
PAL	phase alternating line
PCB	printed circuit board
PHY	Port Physical Layer
PID	packet identifier
SCI	smart card interface
SD	standard definition
SDIO	secure digital input/output
SDRAM	synchronous dynamic random access memory
SECAM	sequential color with memory
SLC	single-level cell
S/PDIF	Sony/Philips Digital Interface Format
SPI	serial peripheral interface
STB	set-top box
TDE	two-dimensional engine
TFBGA	thin & fine ball grid array
TS	transport stream
UART	universal asynchronous receiver transmitter
VBI	vertical blanking interval
VDAC	video digital-to-analog converter