# School of Electronics and Telecommunications
# Electronics Devices – ET2015E

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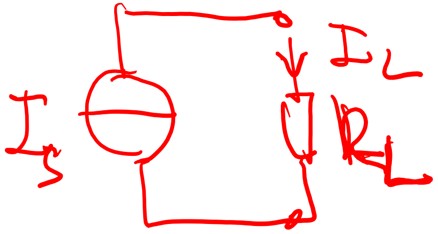
Sources: + Independent: < U, I — Ideal / Real Sources

+ Dependent < U, I

$U_L = k U_1$

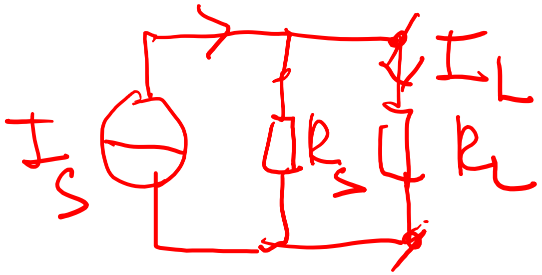
$I_L = n I_1$

Ideal Current Source:




$I_L = I_S$

Real current Source:

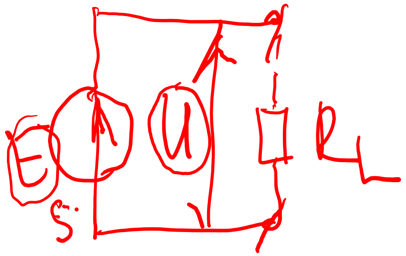



$$I_L = I_S \cdot \frac{R_S}{R_S+R_L} = I_S \cdot \frac{1}{1+\frac{R_L}{R_S}}$$

$\frac{R_L}{R_S} \to 0$

$R_S \approx$ Large $\to \infty$

Ideal voltage Source:




$U = E_S$

Real voltage Source


$$U = E_S \cdot \frac{R_L}{R_S+R_L}$$

$R_S \to 0$

$R_S \approx$ small

# Chapter 2. Semiconductor Devices

## Outline

2.1. PN Junction - Diode and application

2.2. Bipolar Junction Transistor (BJT) and applications

2.3. Operational amplifier (OPAM) and applications

# Chapter 2. Semiconductor Devices

**2.1. PN Junction - Diode and application**

**2.2. Bipolar Junction Transistor (BJT) and applications**

**2.3. Operational amplifier (OPAM) and applications**

**2.4. Voltage regulation**

Si or Ge

14 32

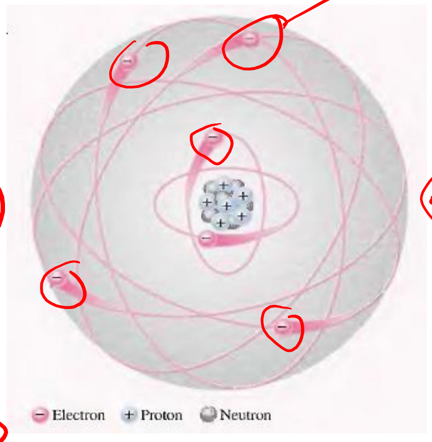
## 2.1.1. N and P semiconductor

### ATOMIC STRUCTURE

Nucleus: Protons (positive charge) + Neutron (uncharged)

Electrons: Negative charged particles

**Atomic number:** = # of protons = # of electrons




electrons

**Atomic shells and orbits**

Electrons orbit its nucleus at certain distances ➔ orbit

Electrons near nucleus have less energy

Energy levels: each orbit corresponds to energy levels

Orbits are grouped into energy bands known as shells

Valence shell: outermost shell

Valence electrons: located in the valence shell

**Number of electrons in each shell:** $N = 2n^2$

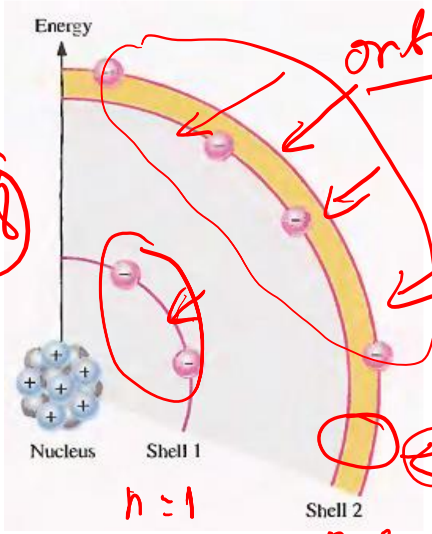
n=3

18

28

n=4

$N = 2 \cdot 3^2 = 18$




orbits

n=1

N=2

n=2

$2 \cdot 2^2 = 8$

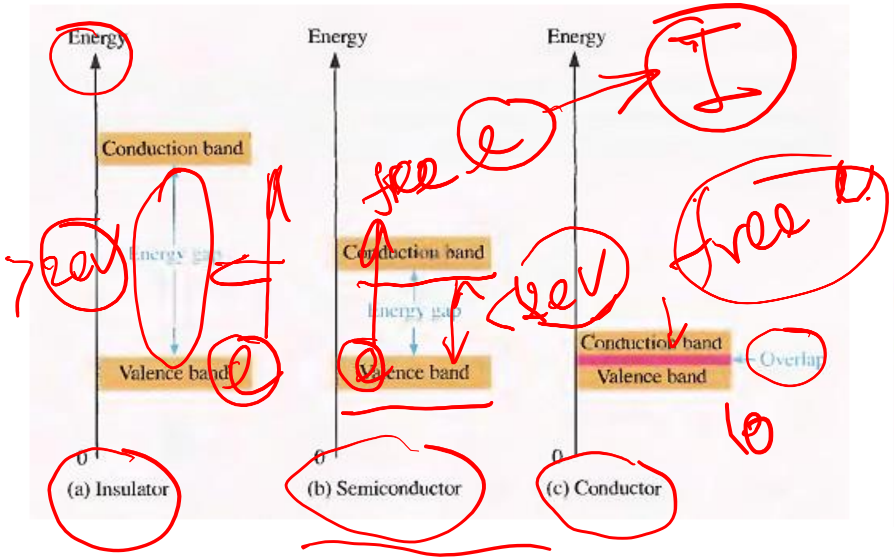
## CONDUCTORS , INSULATORS, SEMICONDUCTORS

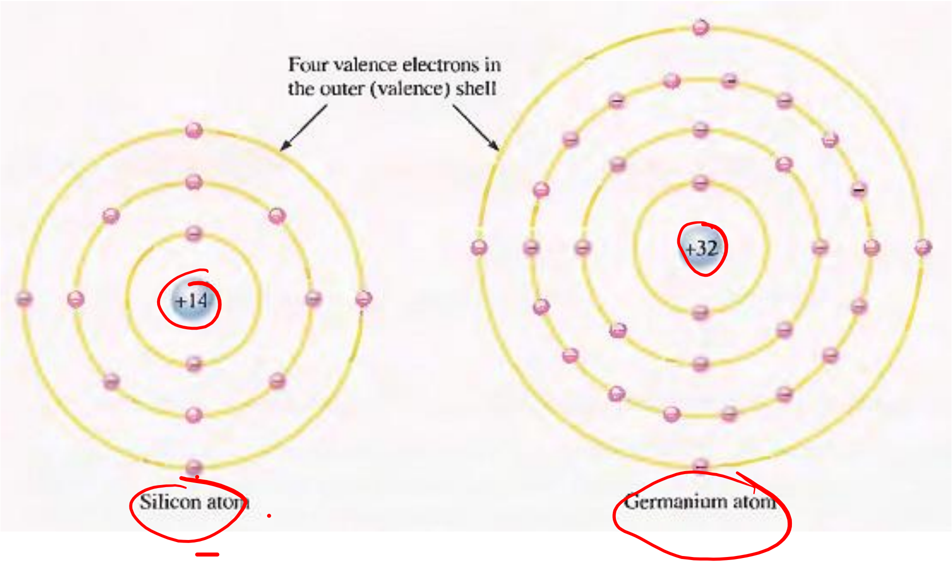
**Conductor:** easily conducts elec. current

**Insulator:** no elec. current  conducted in normal condition

**Semiconductors:** ability to conduct elec. current

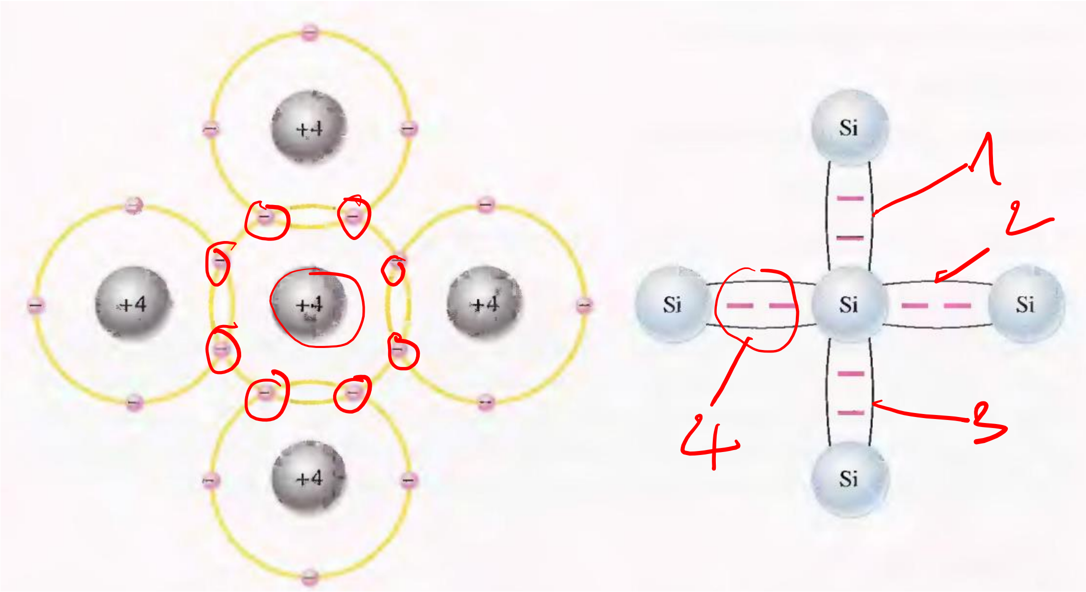
### Energy bands



## COVALENT BONDS

### Shared electrons

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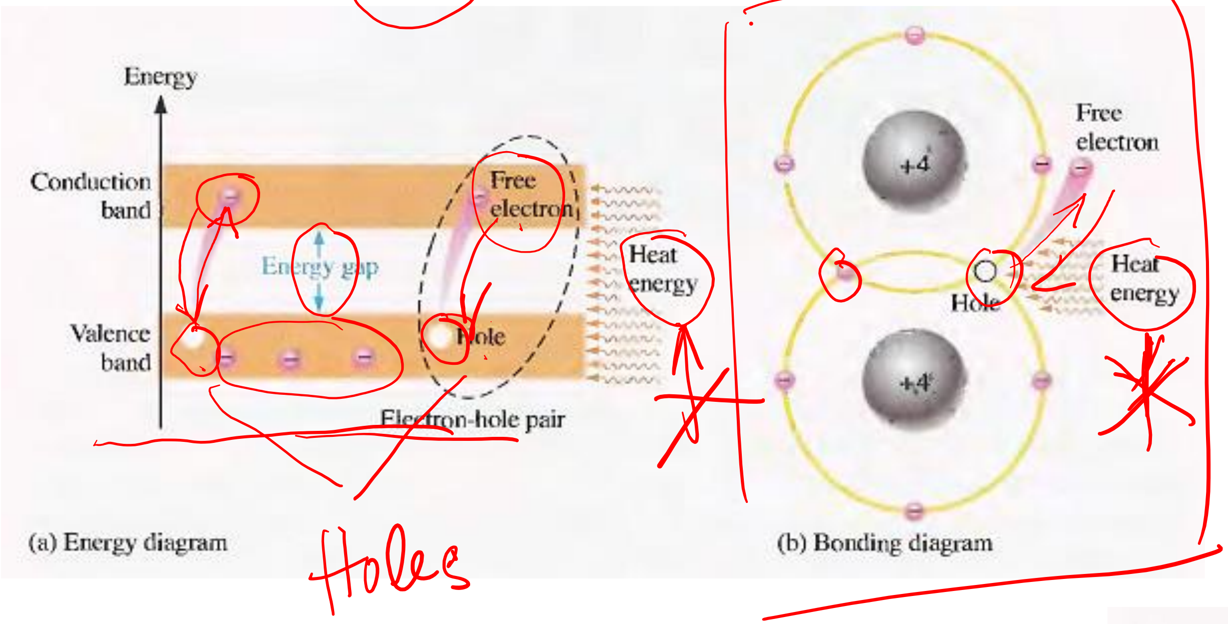
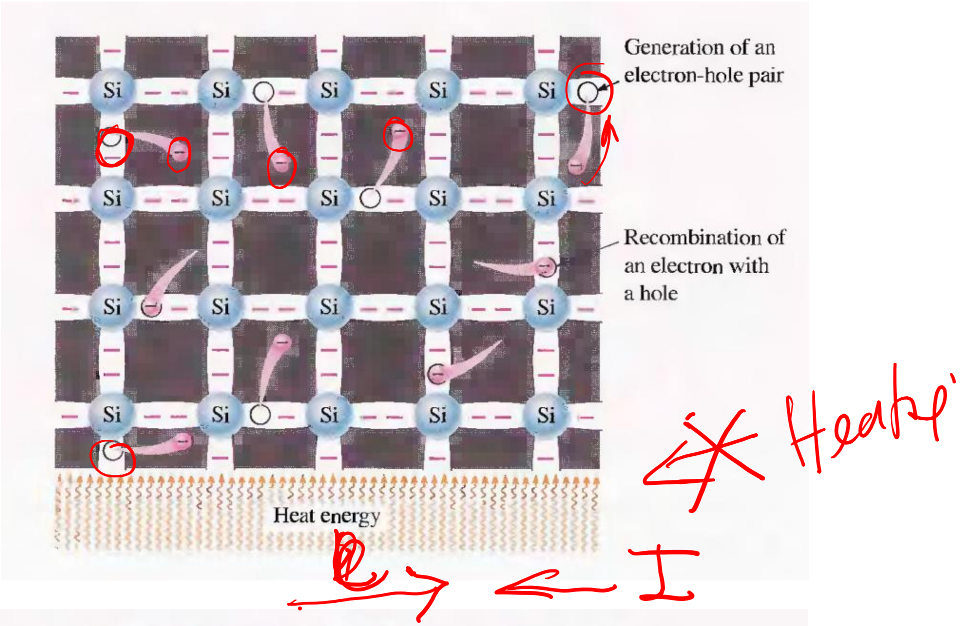
## CONDUCTION IN SEMICONDUCTORS

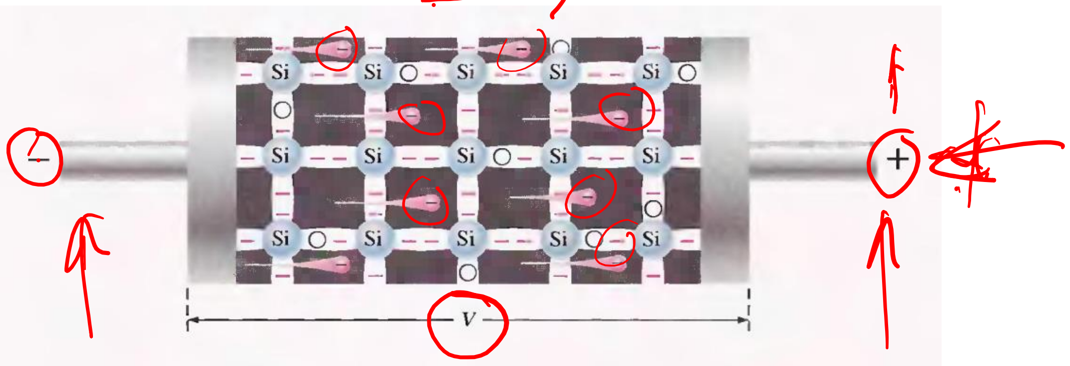
### Electron-hole pairs



(a) Energy diagram (b) Bonding diagram




### Electron and hole currents



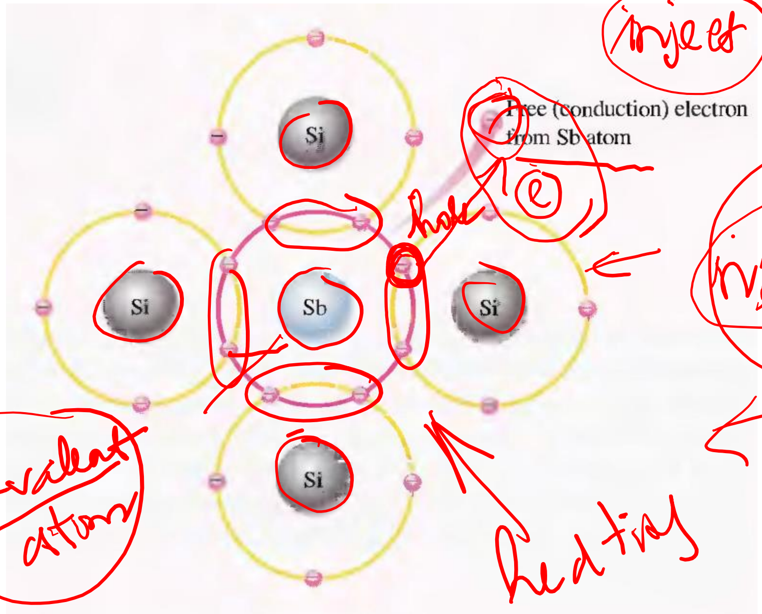
## N-type & P-type SEMICONDUCTORS

- N: negative .
P : positive

**Doping process: addition of impurities to pure semiconductor materials**

inject $10^{12}$

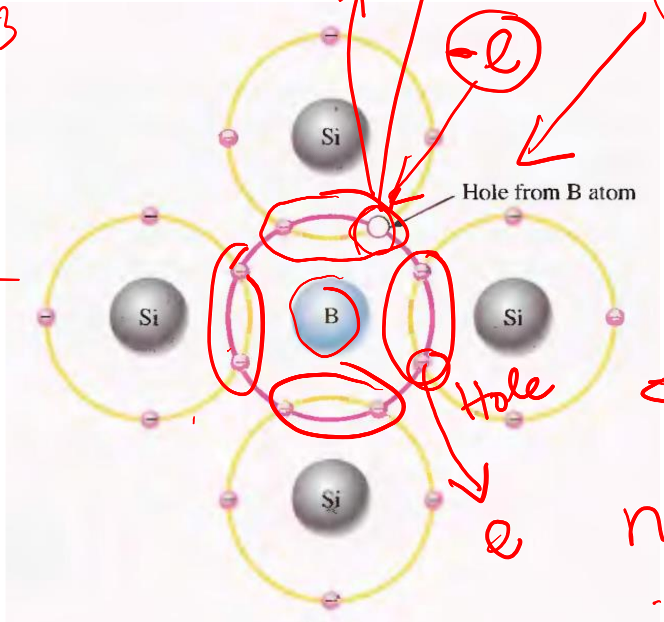
$10^{12}-10^{15}$ atom/cm³




5-valent atom

heating

$n_e >> n_h$ (hole)
(elect)
(-) (+)
N




hole
trivalent atom

$n_e << n_p$
(-) < (+)

**N-type (pentavalent Arsenic/phosphorus atoms)** **P-type (trivalent Boron/Gallium atoms)**

p-type

**Majority and minority carriers**

N-Typ vs P-type

e - major
p - minor

p - major - đa số
e - minor - thiểu số

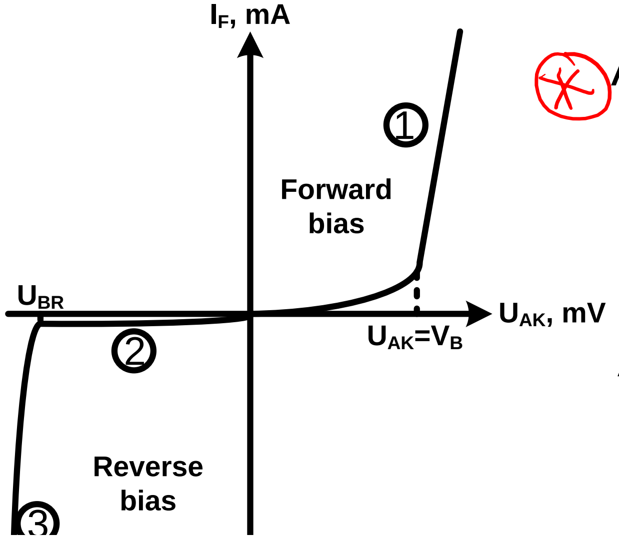
# Chapter 2. Semiconductor Devices

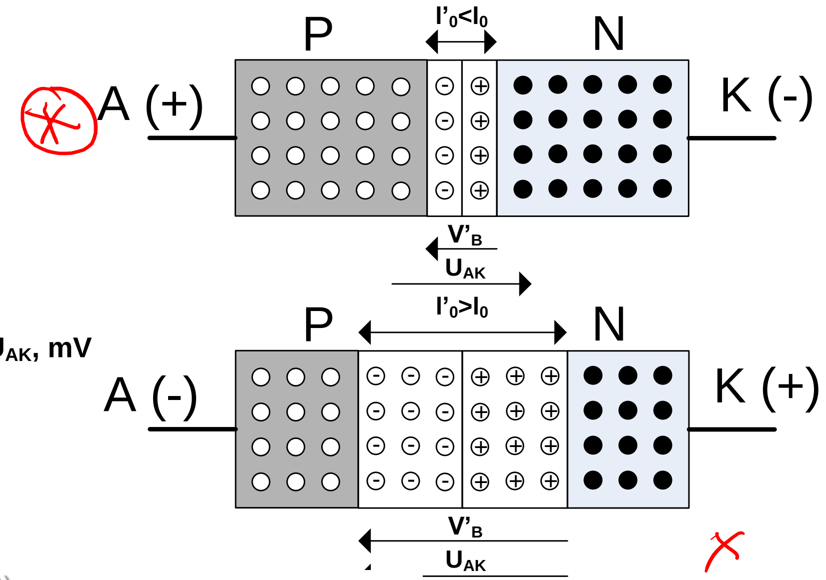
## 2.1. PN Junction - Diode and application

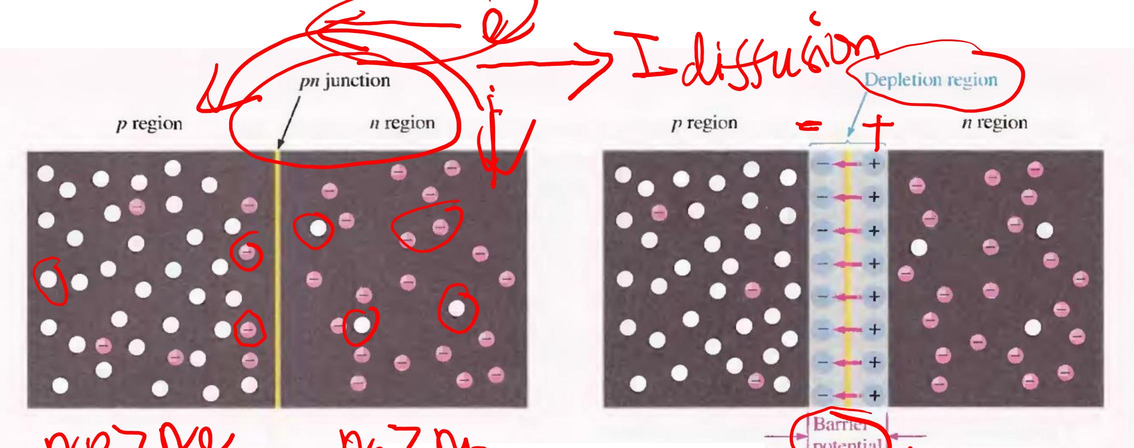
### 2.1.1. N and P semiconductor

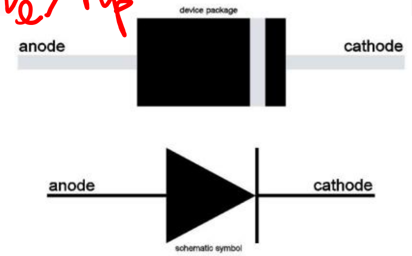
### 2.1.2. PN junction - Diode

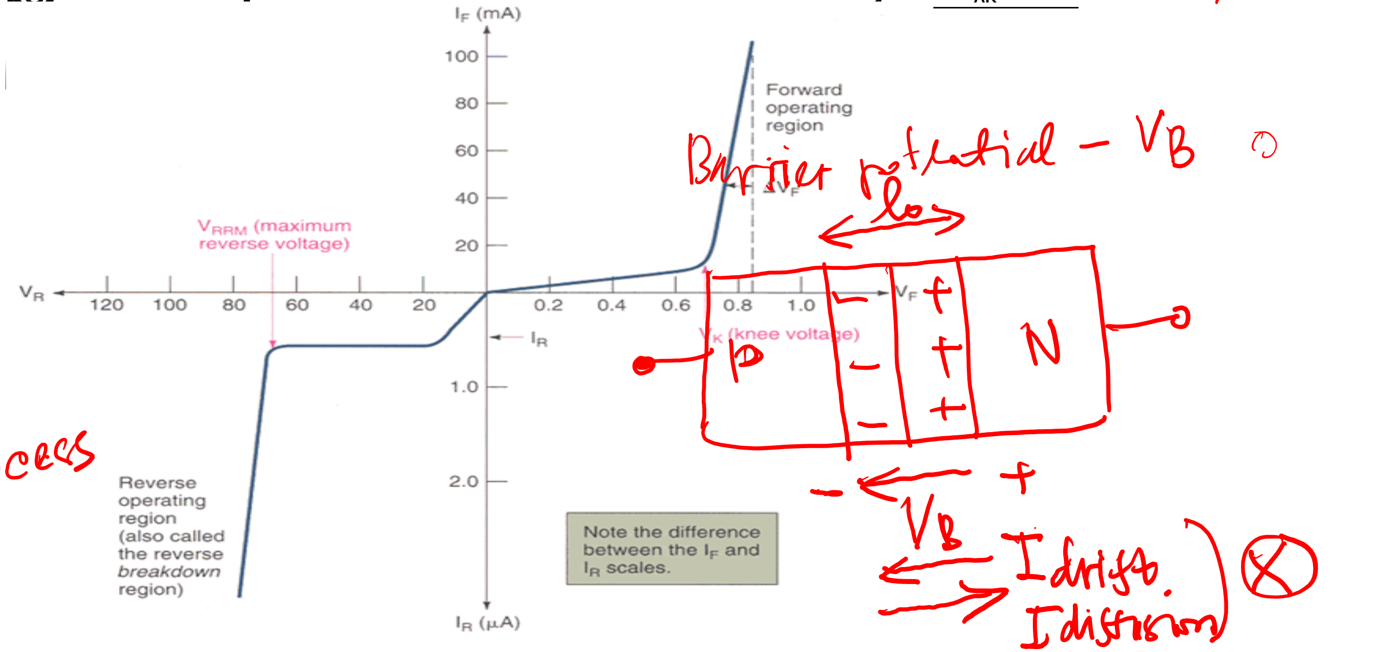
- Forward bias vs reverse bias
- V-A characteristic
- Breakdown: tunneling vs Zener diode

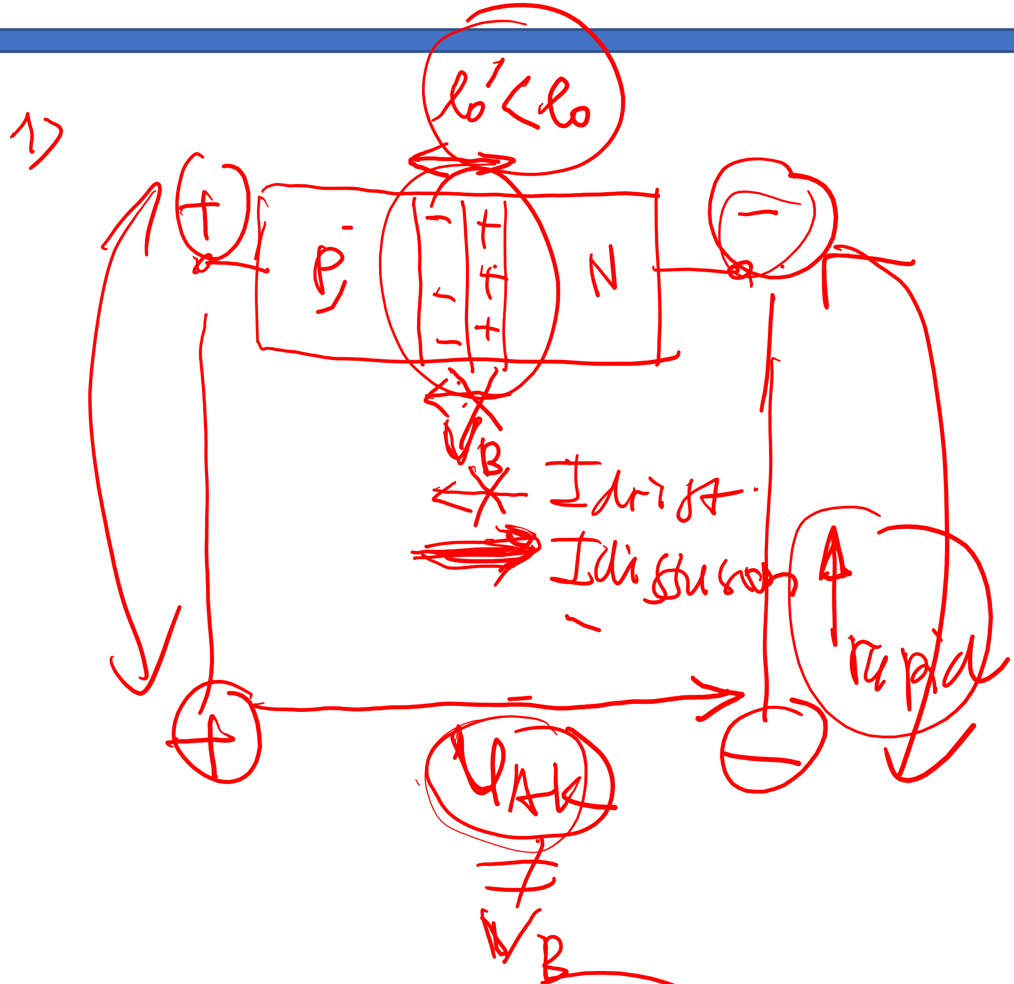


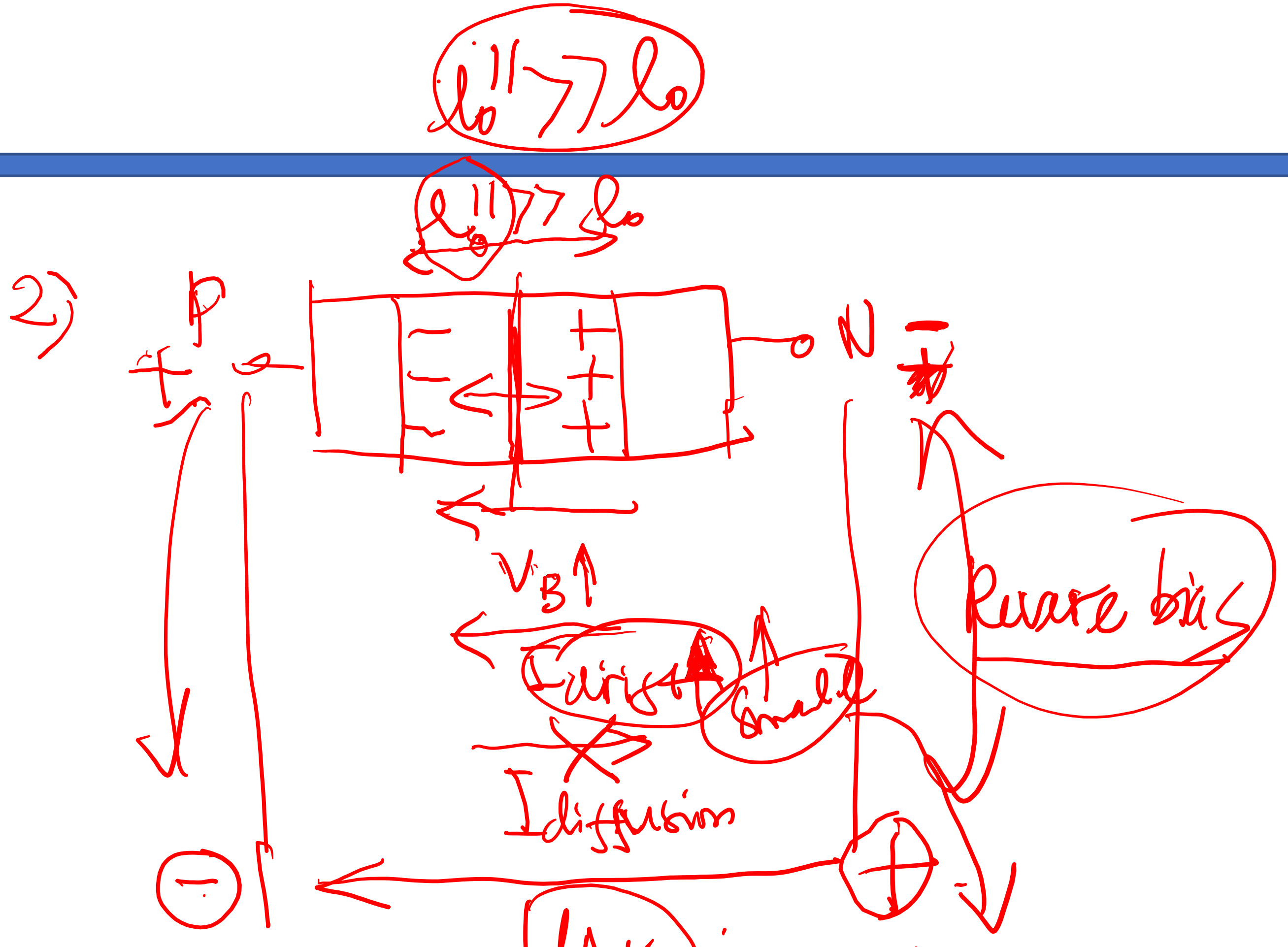





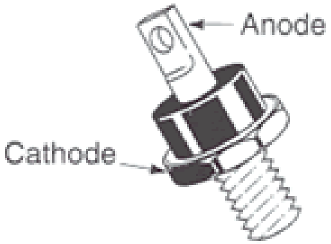

$I_{drift} \equiv$ Reverse current

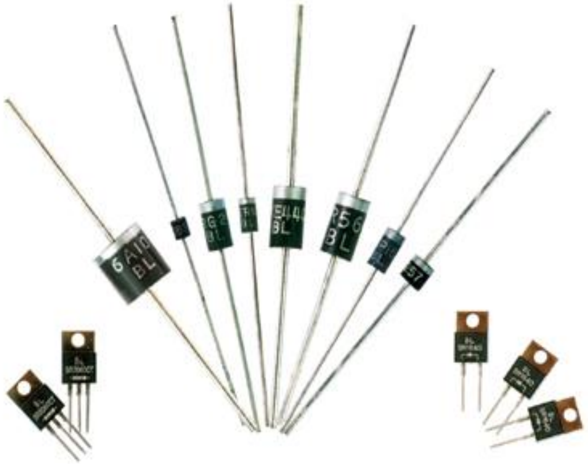
→ Forward Bias · P/c thuận. PN Junction is Forward Biased

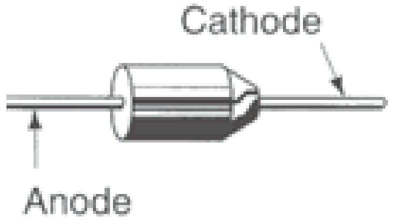
→ $I_{diffusion} \equiv$ Forward current $I_A$ ↑ ≠ $I_S$ small

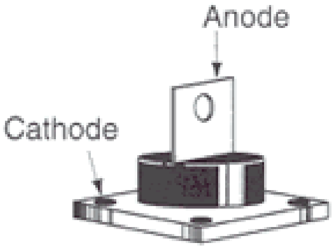
# Chapter 2. Semiconductor Devices (Cont.)

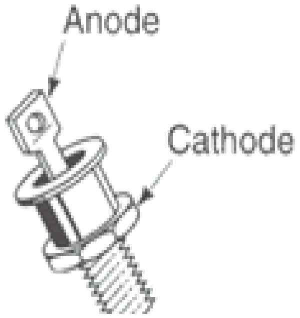
- **Some types of diode**

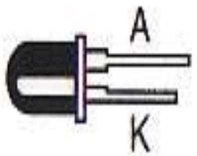


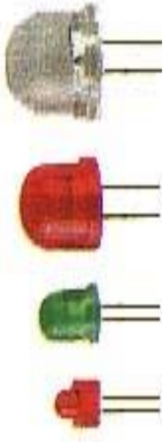



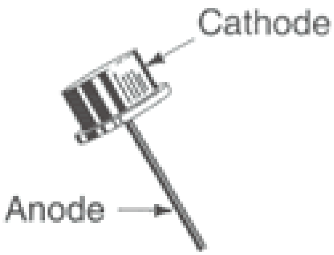


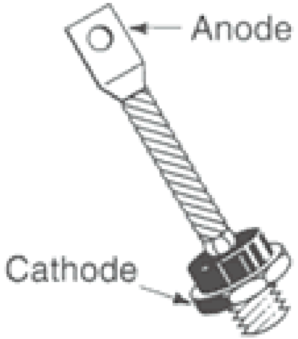



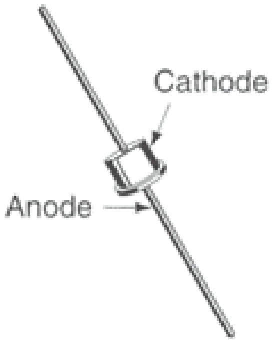



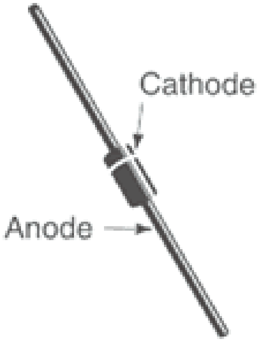



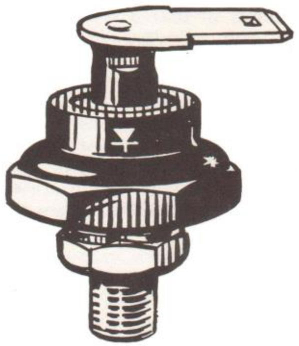





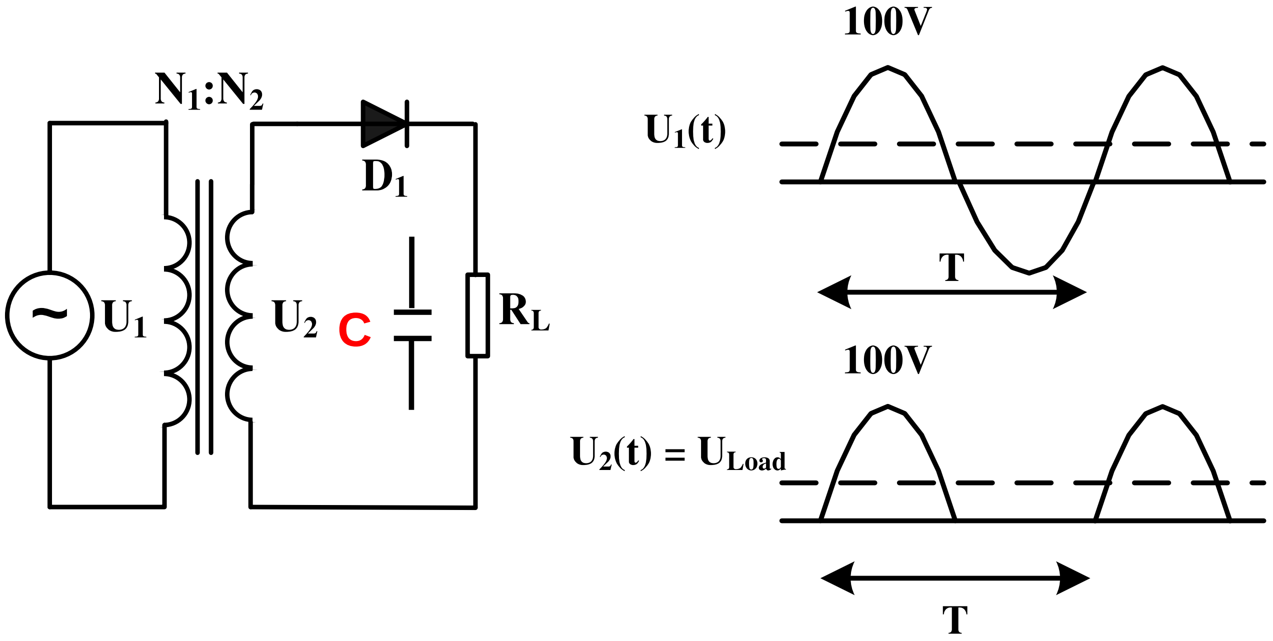



QUESTIONS!

## 2.1.2. System applications

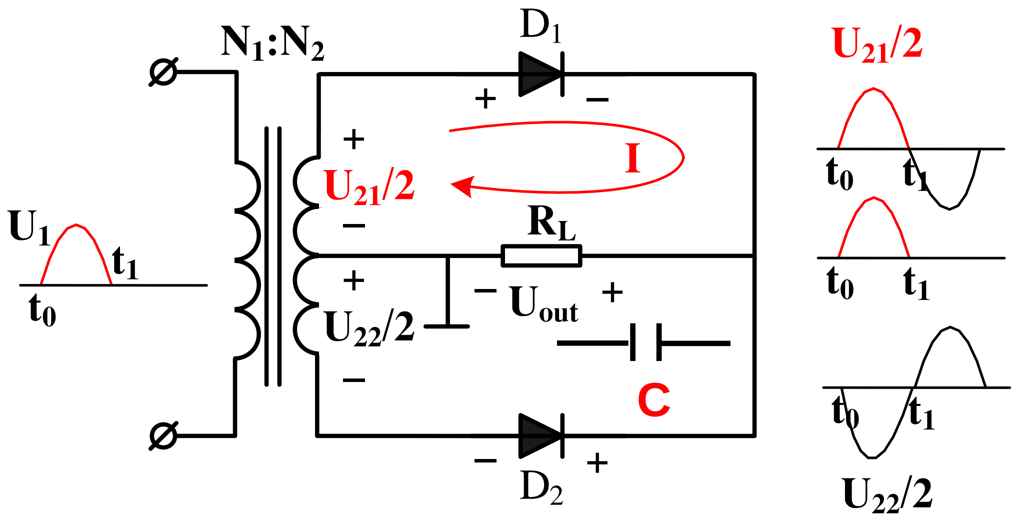
### a. Half-wave rectifier

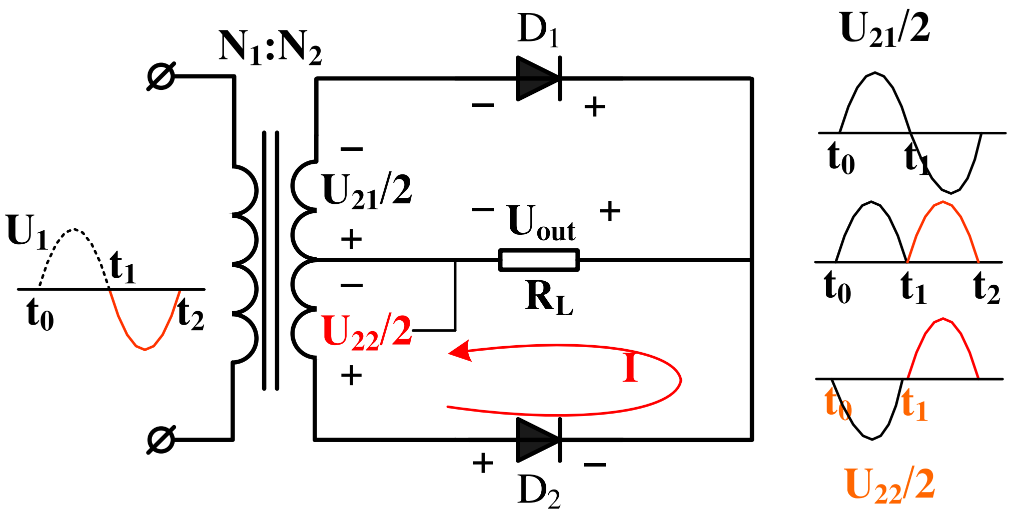
- Positive half-wave: $D_1$ FB, $U_{out} = U_L = U_2$
- Negative half-wave: $D_1$ RB, $U_{out} = 0$




### b. Full-wave (center-tapped) rectifier

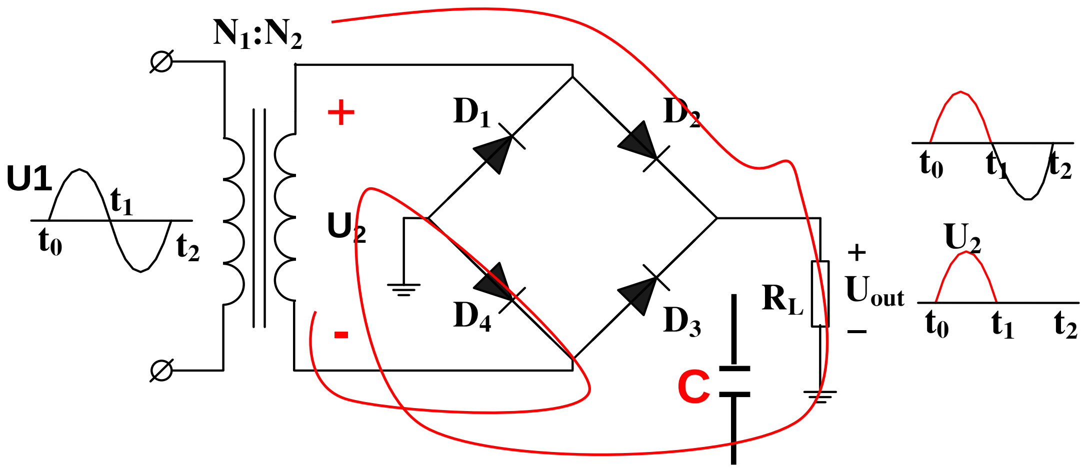
- $U_{21}+$, $U_{22}-$: $D_1$ FB, $D_2$ RB, $U_{out} = U_L = U_{21}$
- $U_{21}-$, $U_{22}+$: $D_1$ RB, $D_2$ FB, $U_{out} = U_L = U_{22}$

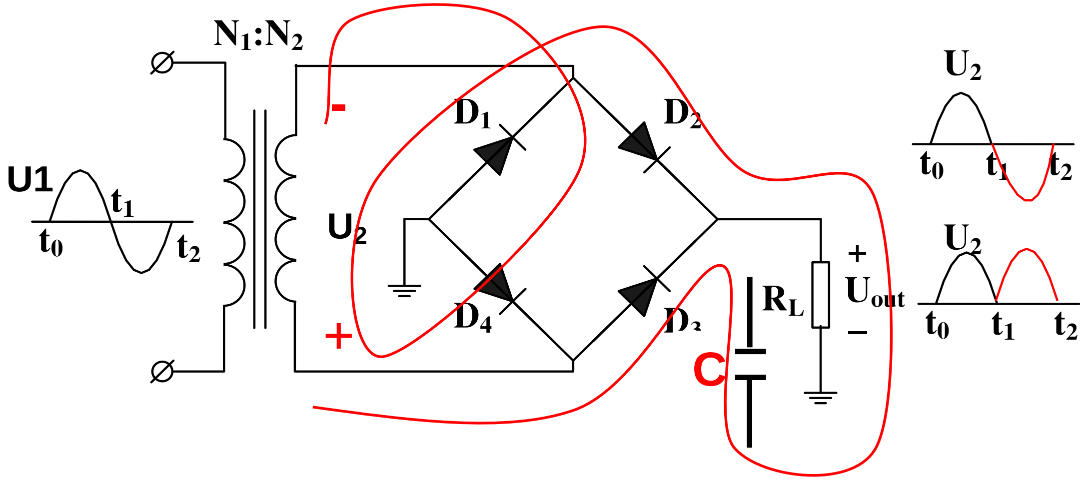


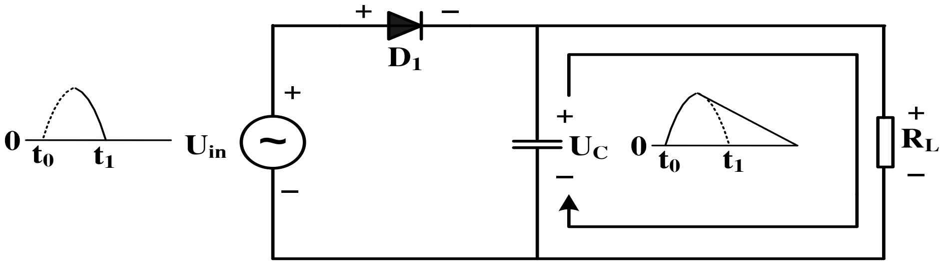
# Chapter 2. Semiconductor Devices (Cont.)

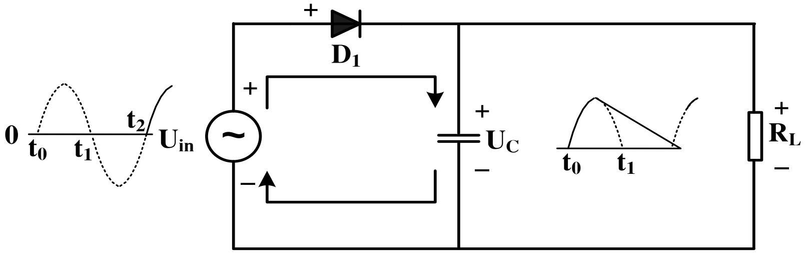
## c. Bridge rectifier

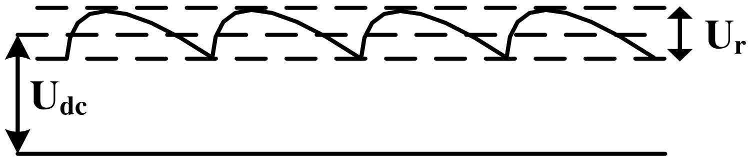



- **Positive half-wave**: $D_2$-$D_4$ FB, $D_1$-$D_3$ RB, $U_{out} = U_L = U_2$
- **Negative half-wave**: $D_2$-$D_4$ RB, $D_1$-D3 FB, $U_{out} = U_L = U_2$



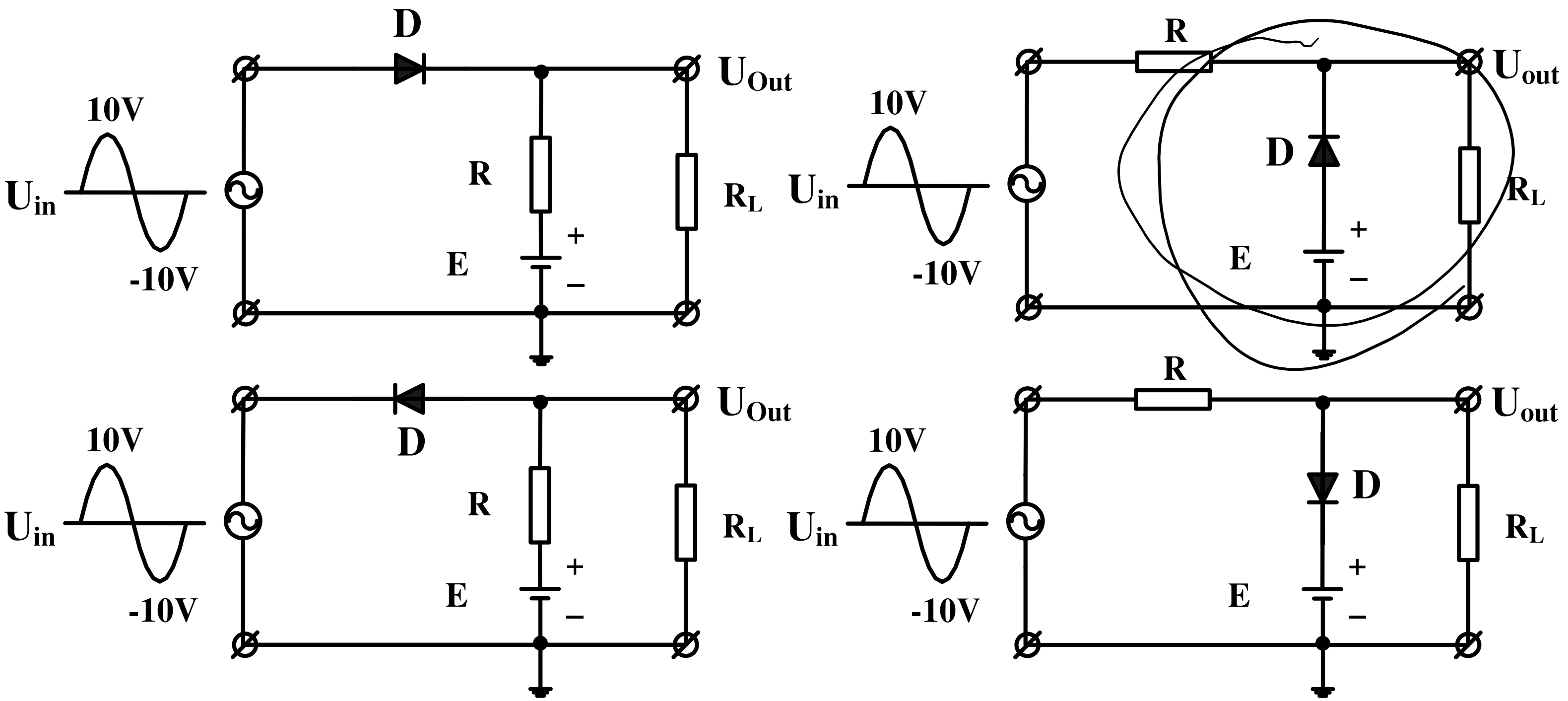

- **Positive half-wave**
- **Positive half-wave**
- **Ripples factor = $Ur/U_{DC}$**

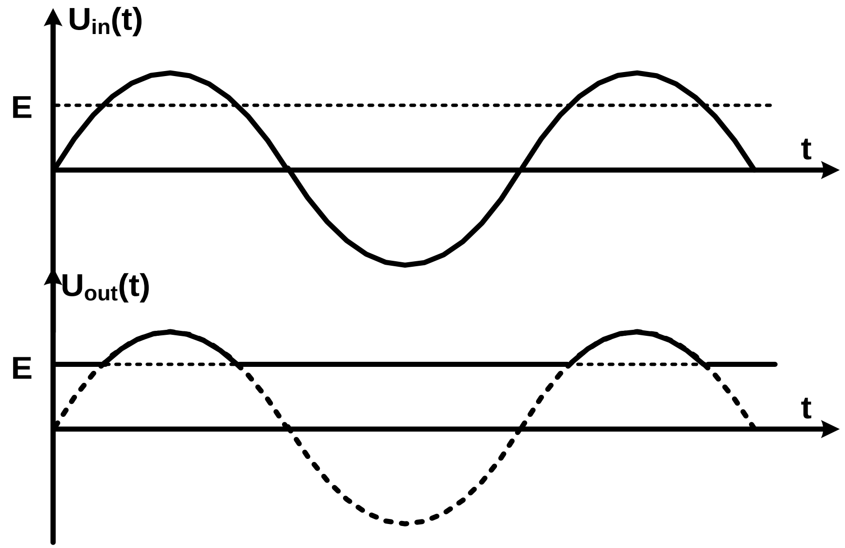
## d. Voltage limiter

- **Lower limiter: Limit a voltage signal under a given threshold**
- **Upper limiter: Limit a voltage signal above a given threshold**
- **Serial limiter: Diode connected in serial to the load**
- **Parallel limiter: Diode connected in parallel to the load**

**QUESTIONS!**

1. The other 2 lower circuits?
2. If E <10V or E >10V?
3. If E removed?



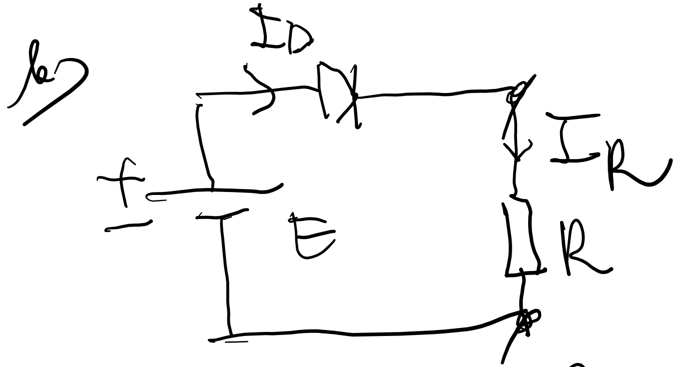
# Chapter 2. Semiconductor Devices (Cont.)

2.1. PN Junction - Diode and application

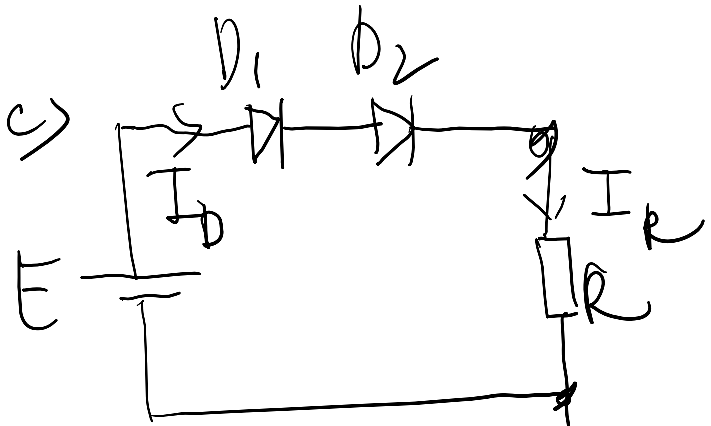
**2.2. Bipolar Junction Transistor (BJT) and applications**

2.3. Operational amplifier (OPAM) and applications

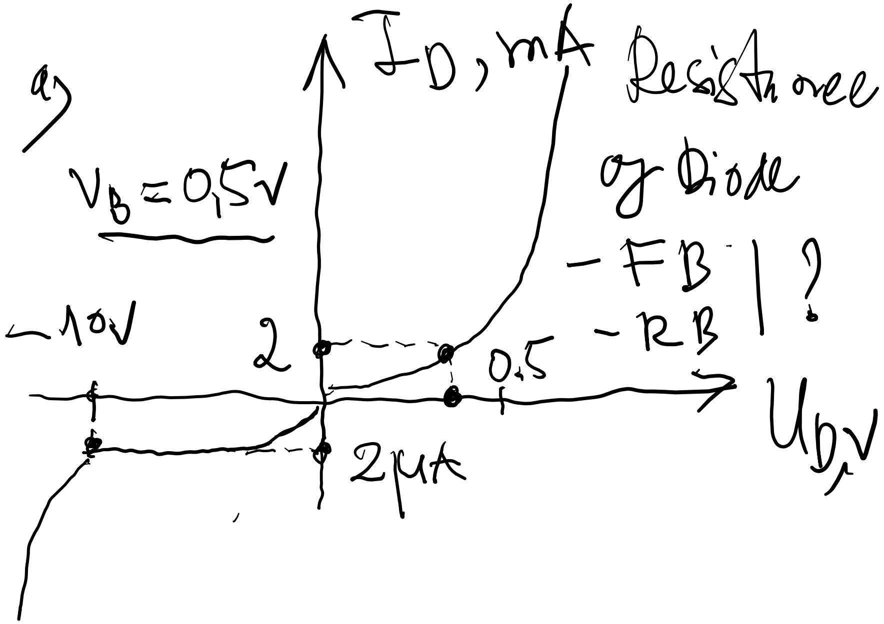
2.4. Voltage regulation




$V_B = U_D = 0.7V$ | $\cdot\ U_R = ?$
$E = +8V$ | $\cdot\ I_R = ?$
$R = 2k\Omega$

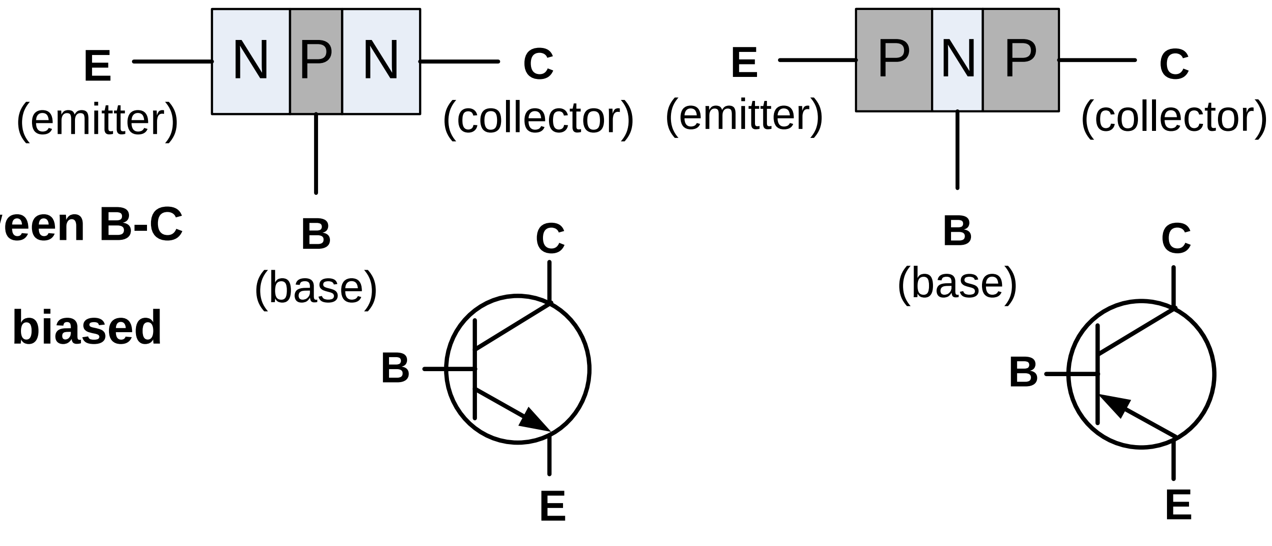



$U_{D1}(Si) = 0.7V$ | $\cdot\ U_R = ?$
$U_{D2}(Ge) = 0.3V$ | $\cdot\ I_R = ?$
$E = +12V,\ R = 6k\Omega$



## 2.2. Bipolar Junction Transistor (BJT) and applications

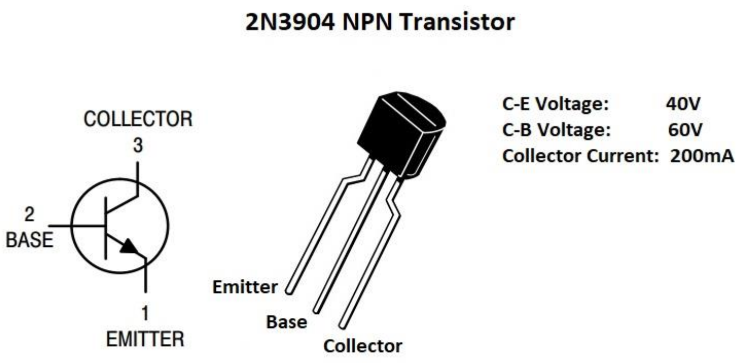
### 2.2.1. Basic construction




NPN PNP

- $J_E$ = PN junction between E-B; $J_C$ = PN junction between B-C
- For amplification: $J_E$ – Forward biased, $J_C$ = Reverse biased
    - NPN: $U_E < U_B < U_C$
    - PNP: $U_E > U_B > U_C$
- Basic equations:
    - Currents $I_E = I_C + I_B$ (1)
    - DC current amplifier gain: $\beta = \frac{I_C}{I_B}$ (2)
    - DC current transfer gain: $\alpha = \frac{I_C}{I_E}$ (3)

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1}$$



## 2.2.2. Transistor as a 4-Terminal system

- **System of impedance equations**

$$U_1 = r_{11} I_1 + r_{12} I_2$$
$$U_2 = r_{21} I_1 + r_{22} I_2$$

***r*$_{ij}$: impedance parameters**

- **System of sucseptance equations**

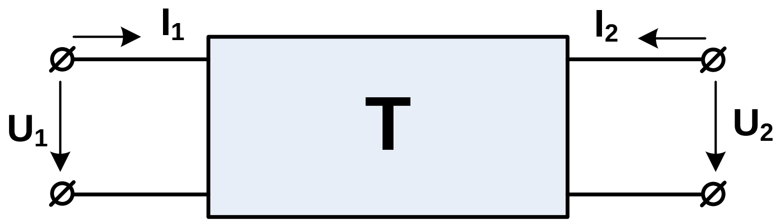
$$I_1 = g_{11} U_1 + g_{12} U_2$$
$$U_2 = g_{21} U_1 + g_{22} U_2$$

***g*$_{ij}$: sucseptive parameters**

- **System of hybrid equations**

$$U_1 = h_{11} I_1 + h_{12}\, U_2$$
$$I_2 = h_{21} I_1 + h_{22}\, U_2$$

***h*$_{ij}$: hybrid parameters**




**Input suceptance/resistance:** $h_{11} = \dfrac{\partial I_1}{\partial U_1} = \dfrac{1}{r_{11}}$ keeping $U_2 = const$

**Voltage amplifier gain:** $h_{12} = \dfrac{\partial U_1}{\partial U_2} = \dfrac{1}{K_u}$ keeping $I_1 = const$

**Current amplifier gain:** $h_{21} = \dfrac{\partial I_1}{\partial I_2} = \dfrac{1}{K_i}$ keeping $U_2 = const$

**Output suceptance/resitance:** $h_{22} = \dfrac{\partial I_2}{\partial U_2} = \dfrac{1}{r_2}$ keeping $I_1 = const$

**Input characteristic:** $I_1 = f(U_1)$ keeping $U_2 = const$

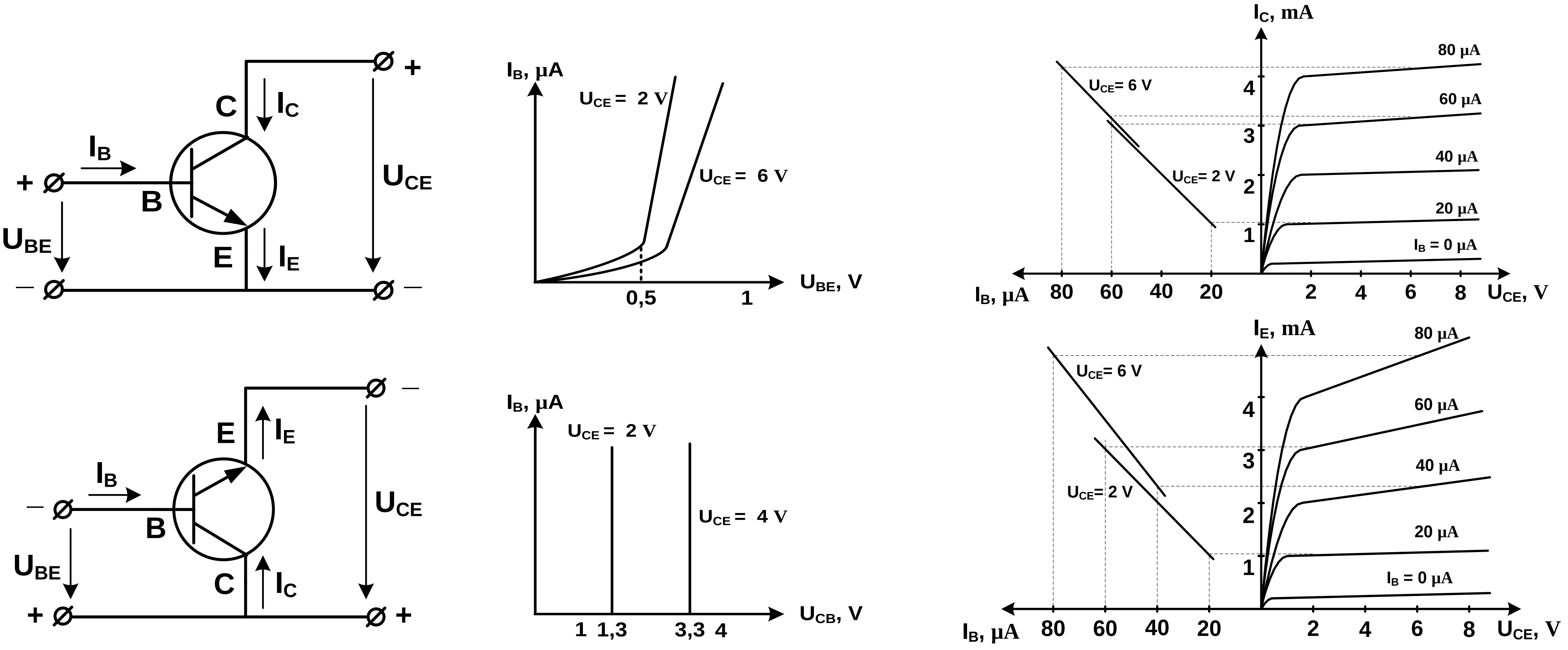
**Out characteristic:** $I_2 = f(U_2)$ keeping $I_1 = const$

**Transfer characteristic:** $I_1 = f(I_2)$ keeping $U_2 = const$

# Chapter 2. Semiconductor Devices (Cont.)

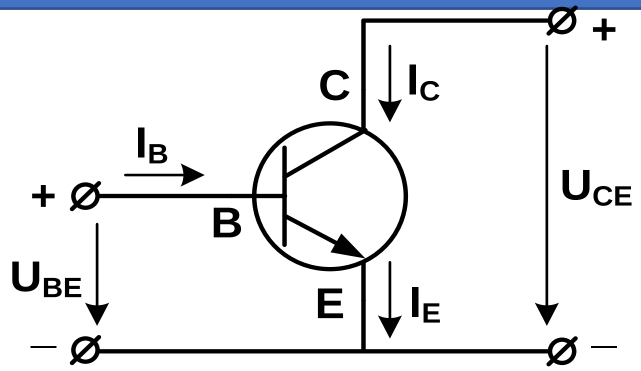
## 2.2.3. Amplifier schemes

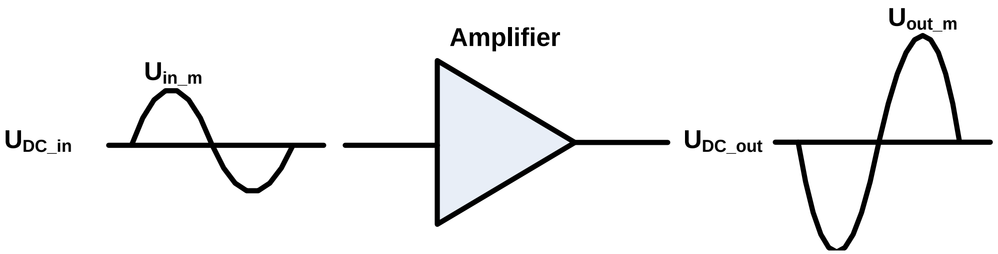
- **EC: Emiter in common; CC: Collector in common; BC: Base in common**



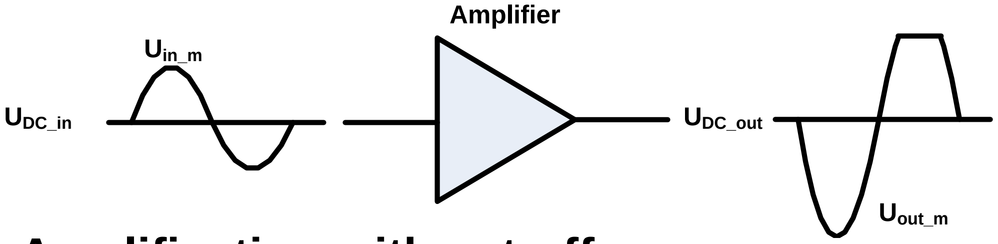
## 2.2.4. BJT amplifier: DC mode

- **Why DC mode? What DC bias?**

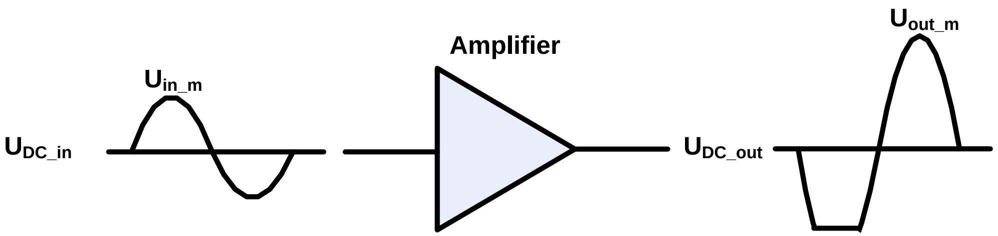


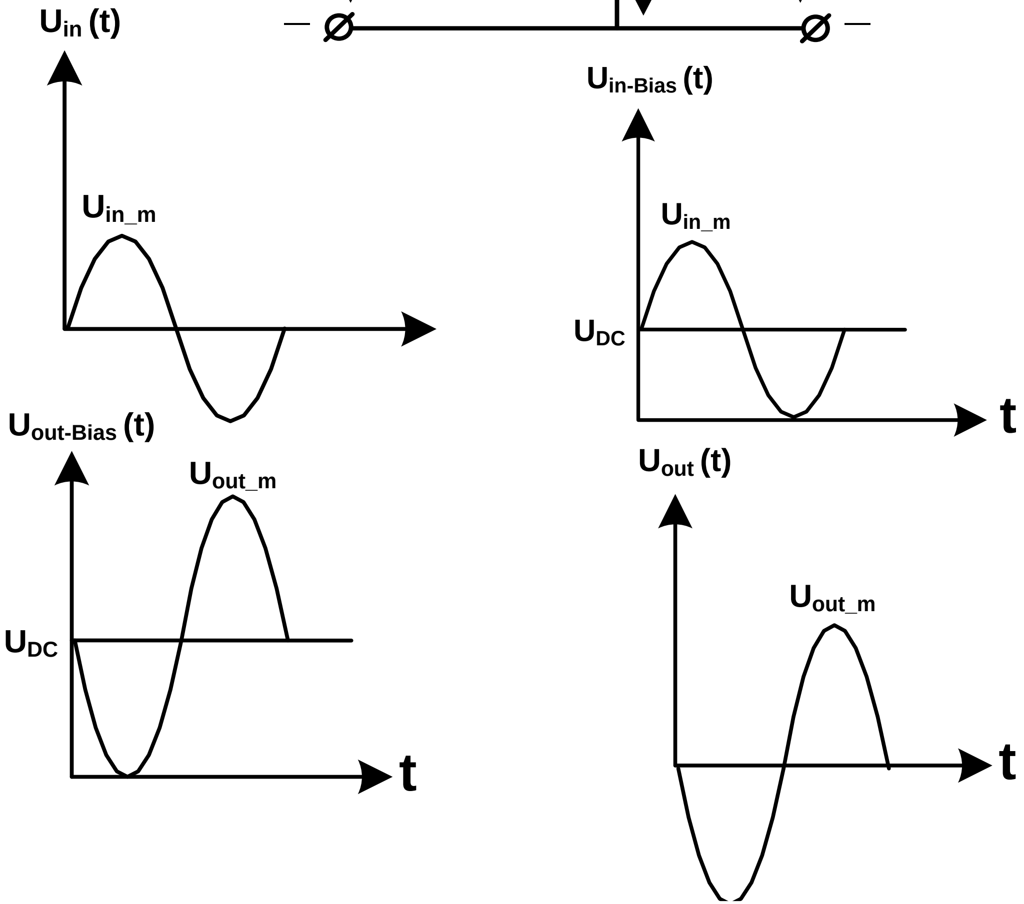

**Linear amplification**




**Amplification with cut-off**

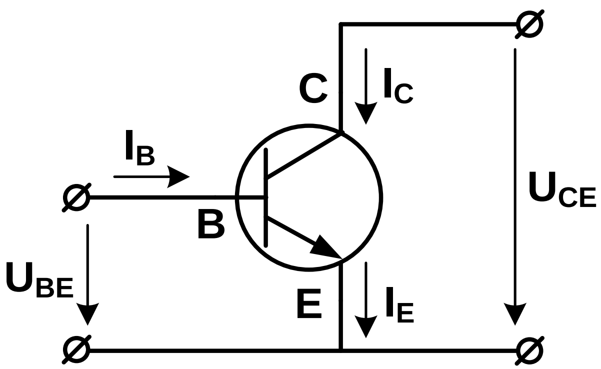


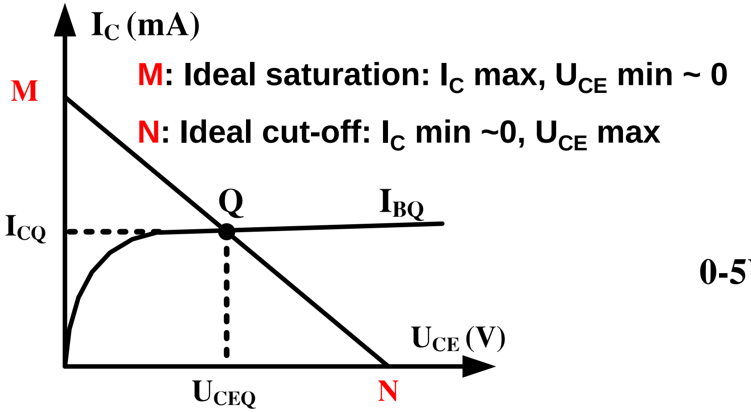

**Amplification saturation**

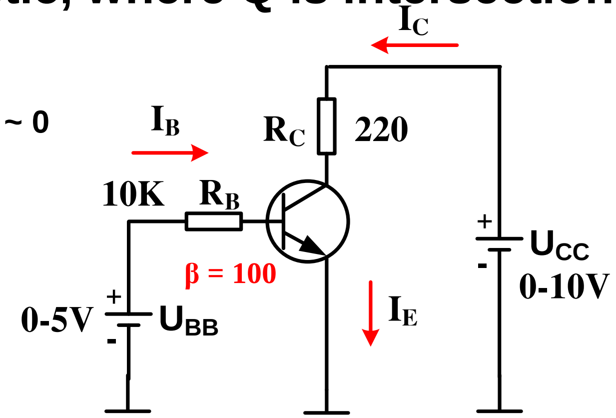


- DC mode: Q (quiescent) point; DC load line, DC load)
  - Q-point (Input current, Output current, Output voltage)

    Question: Q point of EC, CC, BC? Answer: EC: Q($I_B$, $I_C$, $U_{CE}$); CC: Q($I_B$, $I_E$, $U_{CE}$); BC: Q($I_E$, $I_C$, $U_{BC}$)
  - DC load line: Determine on output characteristic, where Q is intersection with DC load line
  - DC load



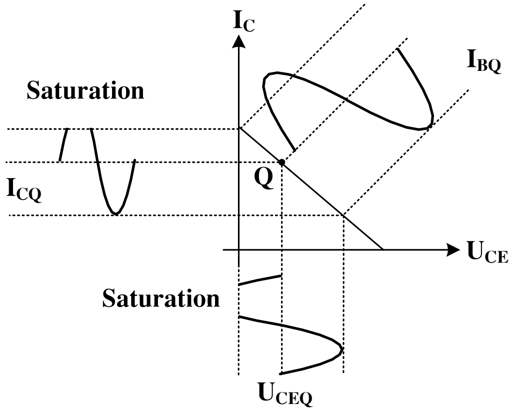

$I_B$ = 100uA ➔ $I_C$ = 100.100uA = 10mA

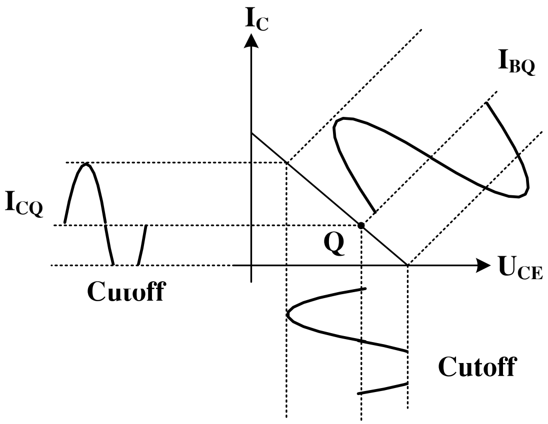
$I_B$ = 200uA ➔ $I_C$ = 100.200uA = 20mA

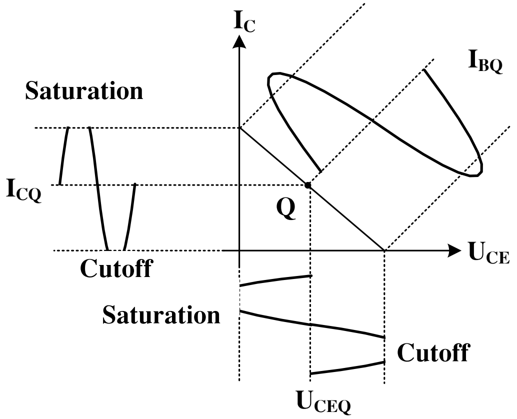
$I_B$ = 300uA ➔ $I_C$ = 100.300uA = 30mA

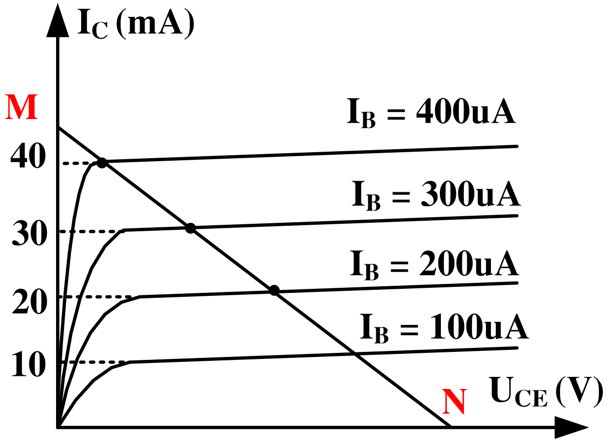
$I_B$ = 400uA ➔ $I_C$ = 100.400uA = 40mA

$U_{CE} = U_{CC} – U_{RC} = U_{CC} - I_CR_C$

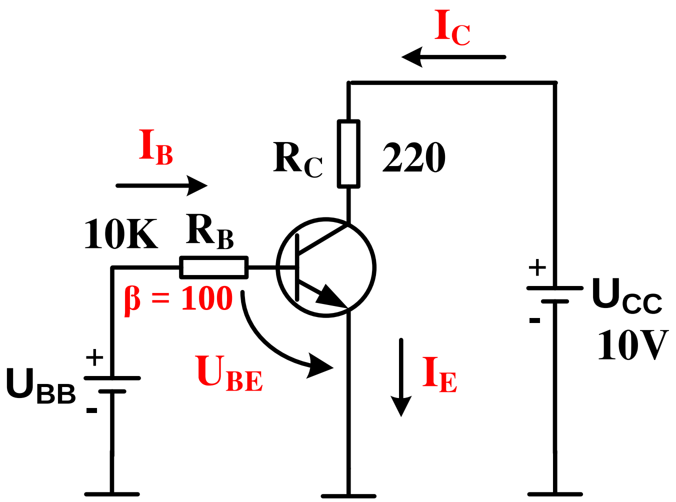


- **Example 1**: $U_{BE}$ = 0.7V. Determine Q point with 1) $U_{BB}$ = 2.7V; 2) $U_{BB}$ = 3.7V; 3) $U_{BB}$ = 4.7V




1. **From input**: $U_{BB}$ = 2.7V ➔ $I_{BQ} = (U_{BB} – U_{BE})/R_B$ = (2.7-0.7)10K = 200 uA ➔ $I_{CQ} = \beta I_B$ = 20 mA

**From output**: $U_{CEQ} = U_{CC} – I_CR_C$ = 10V – 20mA220 = 5.6V

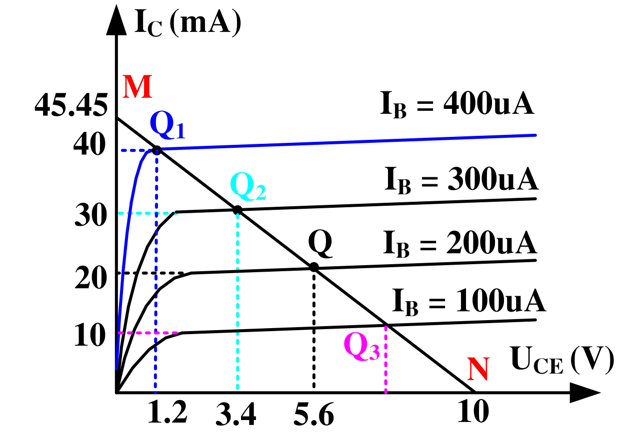
2. $U_{BB}$ = 3.7V ➔ $I_{BQ} = (U_{BB} – U_{BE})/R_B$ = (3.7-0.7)10K = 300 uA ➔ $I_{CQ} = \beta I_B$ = 30 mA

**From output**: $U_{CEQ} = U_{CC} – I_CR_C$ = 10V – 30mA220 = 3.4V

3. $U_{BB}$ = 4.7V ➔ $I_{BQ} = (U_{BB} – U_{BE})/R_B$ = (4.7-0.7)10K = 400 uA ➔ $I_{CQ} = \beta I_B$ = 40 mA

**From output**: $U_{CEQ} = U_{CC} – I_CR_C$ = 10V – 40mA220 = 1.2V

- **Example 2**: Draw DC load line




- **Example 3**: Max variation of $I_B$ = ? for linear operation in case 1, 2, 3

1. $I_{Cmax} = I_{C(sat)} = U_{CC}/R_C$ = 10/220 = 45.45mA, $I_{CQ}$ = 20mA ➔ Max var = 45.45 – 20 = +25.45 mA/-20mA
2. Analogy, $I_{CQ}$ = 30mA ➔ Max var = 45.45 – 30 = +15.45 mA/-30mA
3. Analogy, $I_{CQ}$ = 40mA ➔ Max var = 45.45 – 40 = +5.45 mA/-40mA

Therefore for linear operation:

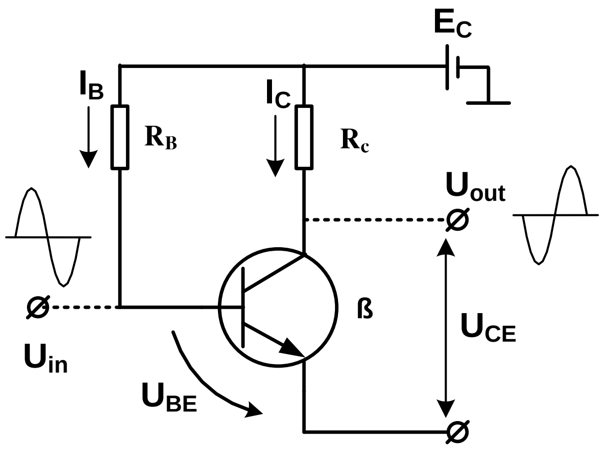
➔ Max variation of $I_B$ 1) $I_B = I_C/\beta$ = 20/100 = 200uA; 2) $I_B$ = 15.45/100 = 155uA; 3) $I_B$ = 5.45/100 = 54.5uA

- DC bias methods: a) Fixed base current; b) Feedback current; c) Emitter current (self-bias); d) Emitter bias

**Goal:** + Setup Q-point for best linear amplification

+ Steps for determination of DC mode

## a) Fixed base current




✓ **Q-point:**

- From input: $E_C = U_{RB} + U_{BE} = I_BR_B + U_{BE}$

➔ $I_{BQ} = (E_C – U_{BE}) / R_B \sim$ constant

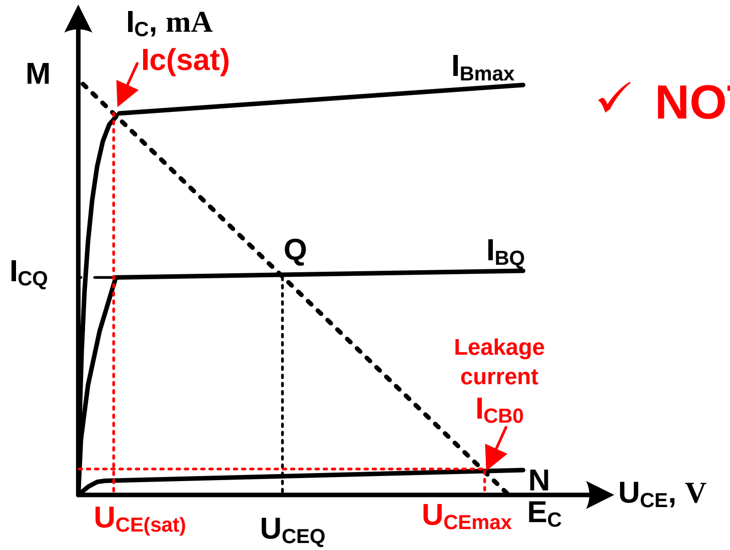
➔ $I_{CQ} = \beta I_{BQ} = \beta(E_C – U_{BE}) / R_B$

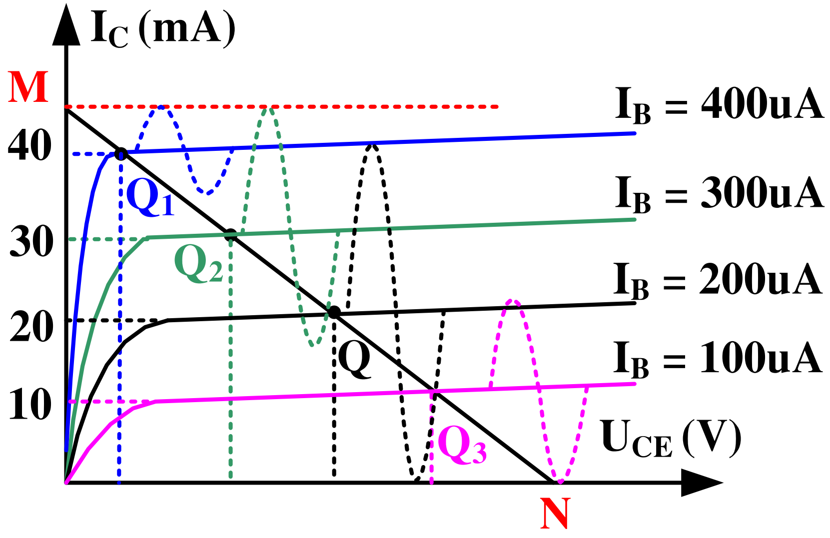
- From output:

$E_C = U_{RC} + U_{CE}$

$= I_CR_C + U_{CE}$

➔ $U_{CEQ} = E_C - I_{CQ}R_C$




✓ **NOTE:**

➢ For best amplification, Q is designed to be at the center of DC load line

➢ Stability of Q-point

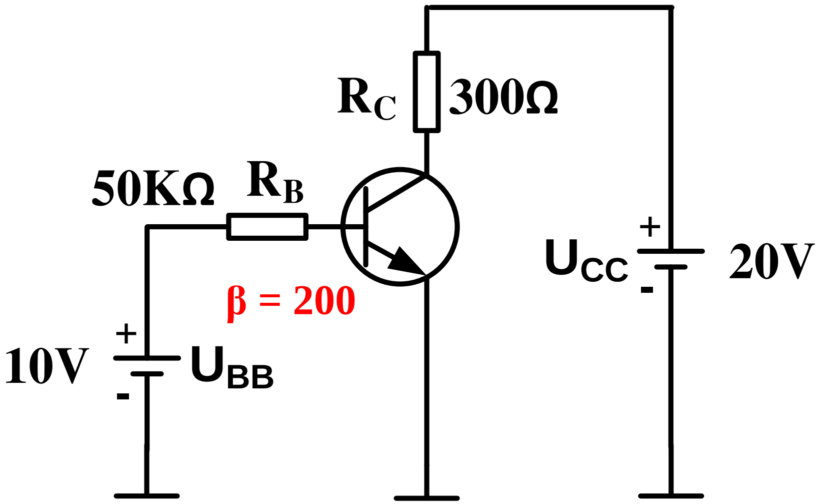
✓ **DC load line:** Linear eqution $U_{CE} = E_C - I_CR_C$

✓ **DC load:** $R_{DC} = R_C$

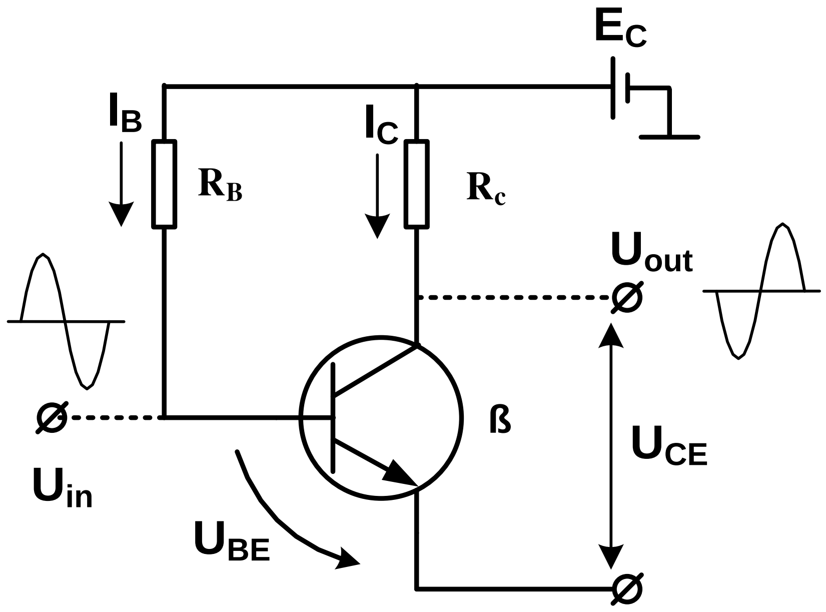
**Quick test 1:** Given a circuit in the figure below.

a) Determine $I_B$, $I_C$, $I_E$, $U_{CE}$, assuming that β = 200, Verify whether the transistor operating in amplification mode.

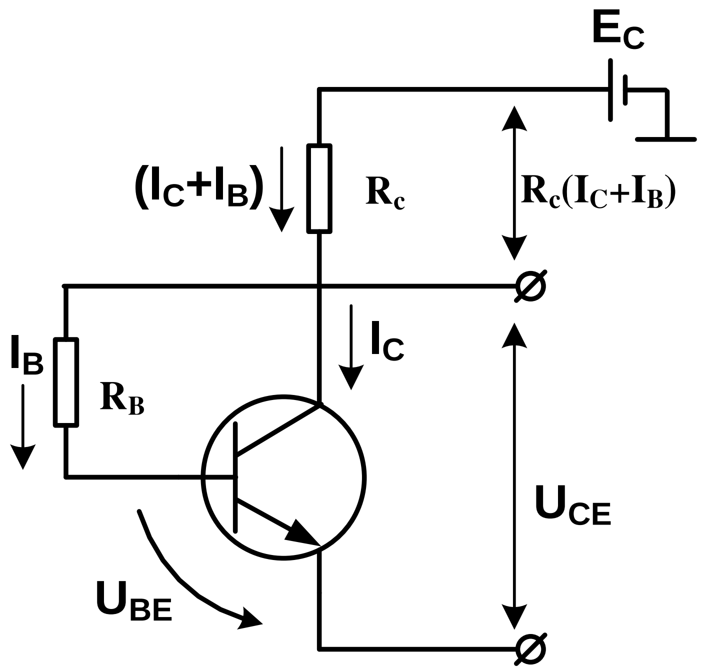
b) Determine Q-point, the maximum peak value (variation) of $I_B$ for linear operation, and the DC load line of the transistor.




**Quick test 2:** $E_C$ = 12V, $R_B$ = 100KΩ, $R_C$ = 560Ω. Investigate the change of Q-point when 1) β change from 85 to 100 and 2) $U_{BE}$ change from 0.7V to 0.6V. Demonstrate on the output characteristic and DC load line for each case.



## b) Feedback (collector) current




✓ **Q-point:**

- From input: $E_C = U_{RC} + U_{RB} + U_{BE} = I_B R_B + I_E R_C + U_{BE} = I_B[R_B + (1+\beta)R_C] + U_{BE}$

➔ $I_{BQ} = (E_C - U_{BE}) / [R_B + (1+\beta)R_C] \sim (E_C - U_{BE}) / (R_B + \beta R_C)$

➔ $I_{CQ} = \beta I_{BQ} = \beta(E_C - U_{BE}) / (R_B + \beta R_C) = (E_C - U_{BE}) / (R_B / \beta + R_C)$

- From output:

$E_C = U_{RC} + U_{CE} = (I_B + I_C)R_C + U_{CE} = I_E R_C + U_{CE} \sim I_C R_C + U_{CE}$

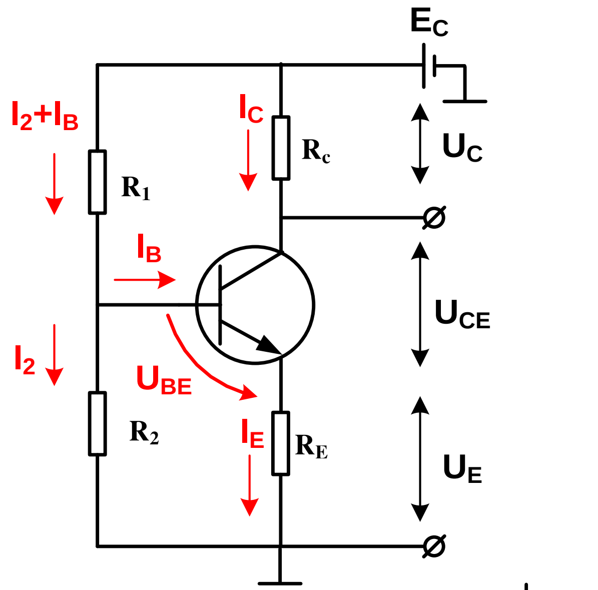
➔ $U_{CEQ} = E_C - I_{CQ} R_C$

✓ **DC load line:** Linear eqution $U_{CE} = E_C - I_C R_C$

✓ **Stability of Q-point**

✓ **DC load:** $R_{LDC} = R_C$

**c) Emitter current (self-bias): Voltage-divider bias – VDB (Single bias source)**




- Use of VDB of $R_1$-$R_2$ instead of $V_{BB}$ for input biasing
- If $I_B << I_2$: ➔ $I_{R1} = I_{R2} = I_2$; o.w: Equivalent input resistance $R_{IN(base)}$ is investigated

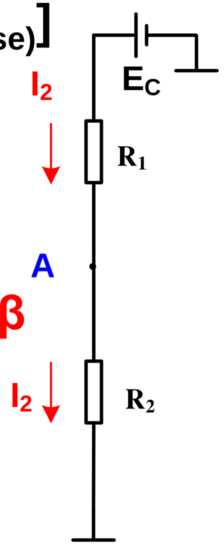
**- DC mode analysis:**

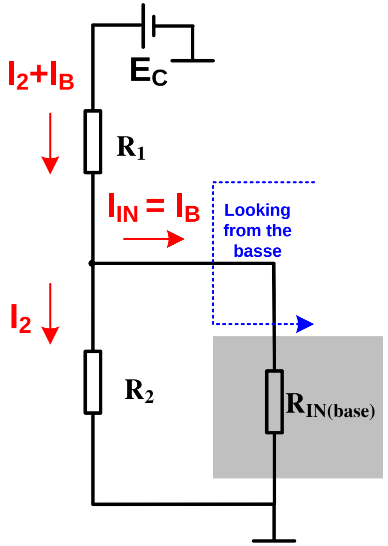
- From input: $R_{IN(base)} = U_{IN}/I_{IN} = (I_ER_E + U_{BE})/I_B \sim (1+\beta)I_BR_E/I_B \sim \beta R_E$; and $U_{IN} = \beta I_BR_E$
- Total input resistance: $R_{IN(total)} = R_2//R_{IN(base)} = R_2//\beta R_E$
- Total input resistance: $U_{IN} = U_B = E_C[R_2//R_{IN(base)}]/[R_1 + R_2//R_{IN(base)}]$

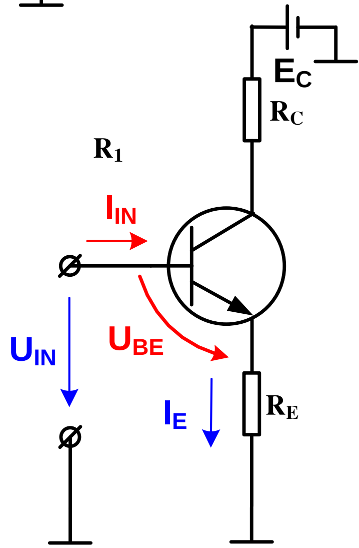
If $R_2 << R_{IN(base)}$ ➔ $U_{IN} = E_CR_2/(R_1+R_2)$

**- Q-point:**

- $U_E = U_B – U_{BE}$ ➔ $I_E \sim I_{CQ} = (U_E - U_{BE})/R_E$ ➔ $I_{CQ} \sim U_E/R_E$ ➔ $I_{BQ} = I_{CQ}/\beta$
- $U_{CE} = E_C – I_C(R_C+R_E)$ ➔ $U_{CEQ} = E_C – I_{CQ}(R_C+R_E)$
- DC load line equation: $U_{CE} = E_C – I_C(R_C+R_E)$
- $R_{LDC} = R_C+R_E$



- Equivalent Thevenine theorem: $U_{TH} = U_B = E_C R_2/(R_1+R_2)$ and $R_{TH} = R_B = R_1//R_2 = R_1R_2/(R_1+R_2)$

  ➔ utilization of equivalent DC circuit

**- Q-point:**

➢ From input loop: $U_B = I_B R_B + U_{BE} + I_E R_E$ ➔ $U_B = I_E/(1+\beta)R_B + I_E R_E + U_{BE}$ ➔ $I_E \sim (U_B - U_{BE})/(R_E + R_B/\beta)$

If $R_E >> R_B/\beta$ ➔ $I_E \sim (U_B - U_{BE})/R_E$ or $U_E = U_B - U_{BE}$ (proven)➔ $I_{CQ} \sim I_E$ ➔ $I_{BQ} = I_{CQ}/\beta$: $I_E$ independent from β

➢ $U_{CE} = E_C - I_C(R_C+R_E)$ ➔ $U_{CEQ} = E_C - I_{CQ}(R_C+R_E)$

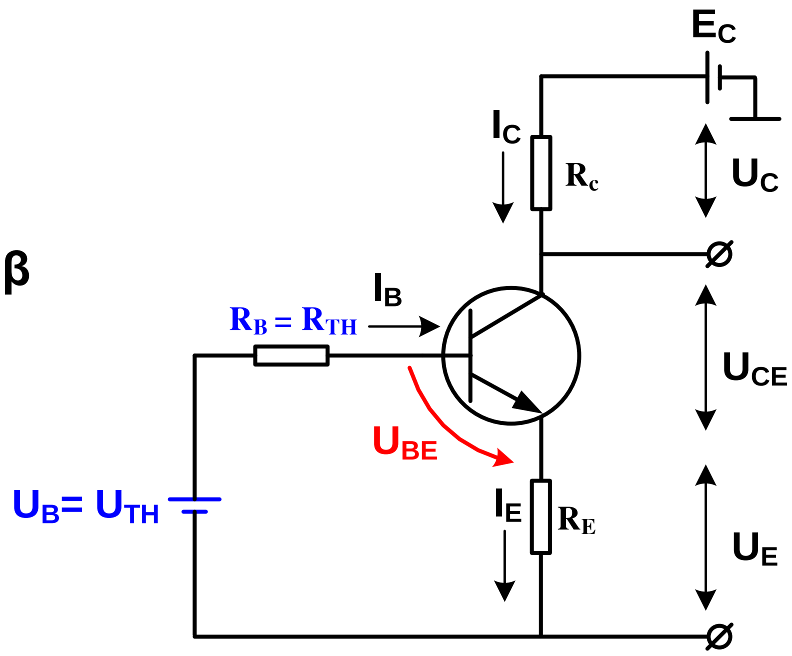
- Stability of Q-point: $I_E$ independent to β ➔ most stable

In practice: If $R_E >> R_B/\beta$ ➔ select $R_E$ at least 10 times greater than $R_B/\beta$

d) Emitter bias: Double bias sources $E_{CC}$ and $E_{EE}$ ➔ self reading

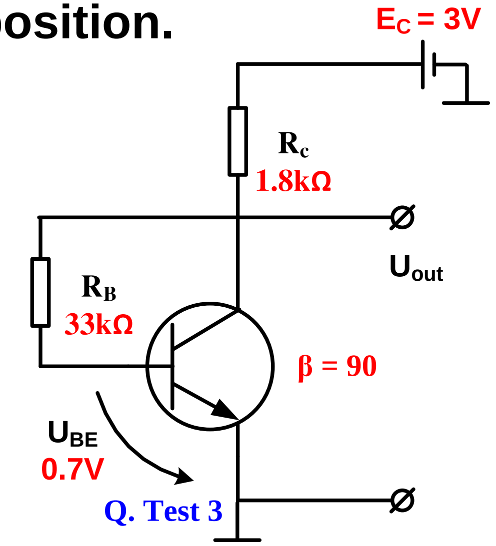
➢ $I_C = (E_{EE} - U_{BE})/(R_E + R_B/\beta)$

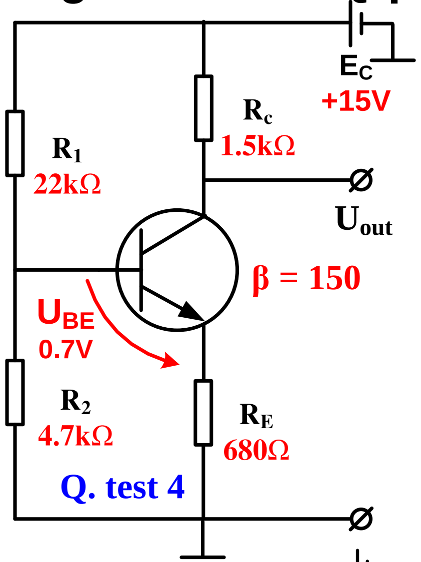
➢ $U_{CE} = E_{CC} + E_{EE} - I_C(R_C+R_E)$

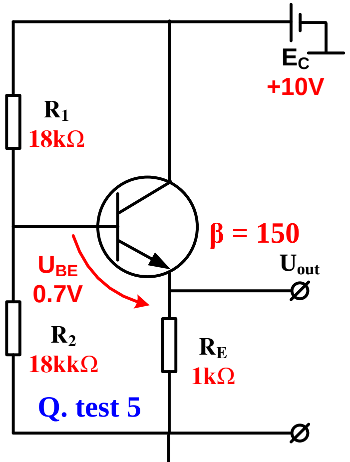


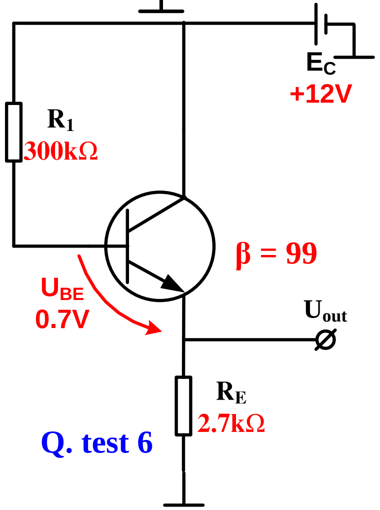
**Quick test 3:** Given a circuit in the figure below.

Determine DC mode. Investigate the Q-point position.




**Quick test 4:** Given a circuit in the figure below.

a) $\beta_{min}$ = ? in order to set up $R_{IN(base)} >> 10R_2$

b) If $R_2$ is replaced by 15kΩ potentiometer. What is the minimum resistance setting causes saturation?

c) Set $R_2$ at 2kΩ. Determine DC mode.

**Quick test 5:** Given a circuit in the figure below.

a) Determine type of amplifier

b) Investigate DC mode

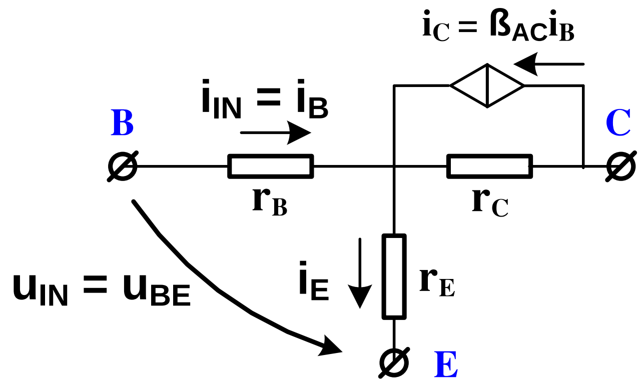
**Quick test 6:** Given a circuit in the figure below.

a) Determine type of amplifier

b) Investigate DC mode

## 2.2.5. BJT amplifier: AC mode

- What is AC mode: AC signal is amplified, once DC mode has been setup
- In AC mode: 1) Voltage gain $K_U$ (or $A_u$), 2)Current gain $K_i$ (or $A_i$), 3) AC load
- AC equivalent of a transistor:

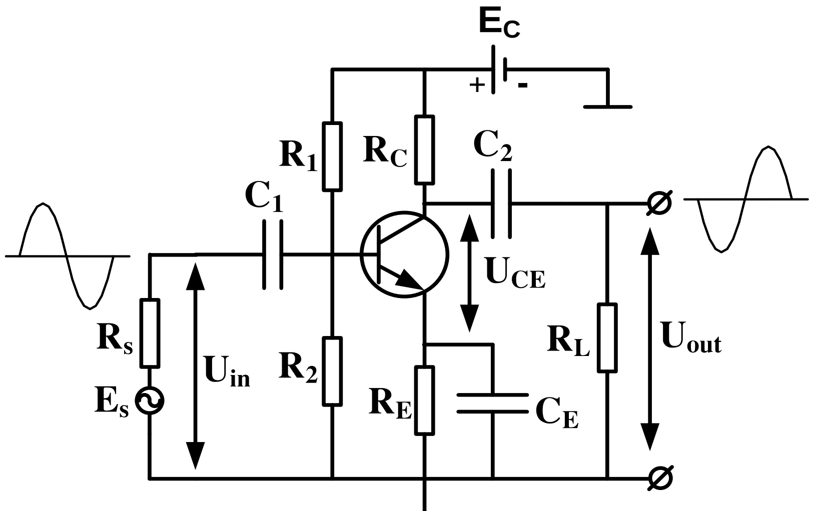



**a) EC amplifier:** voltage divider bias

- $C_1$, $C_2$: capacitively coupled; $C_E$: bypass
- In AC mode: $C_1$, $C_2$, $C_E$ replaced by shorts ($X_C \sim 0$)
- Effect of CE on voltage gain: $X_C \sim 0$ if:

$\leftrightarrow 10X_{CE} \leq R_E \leftrightarrow X_{CE} \leq R_E/10 \leftrightarrow 1/(\omega C_E) \leq R_E/10$

➔ $C_E \geq 10/(2\pi f R_E)$




- AC input voltage: $u_{IN} = u_{BE} = i_B r_B + i_E r_E = i_B[r_B + (1 + \beta_{AC})r_E]$

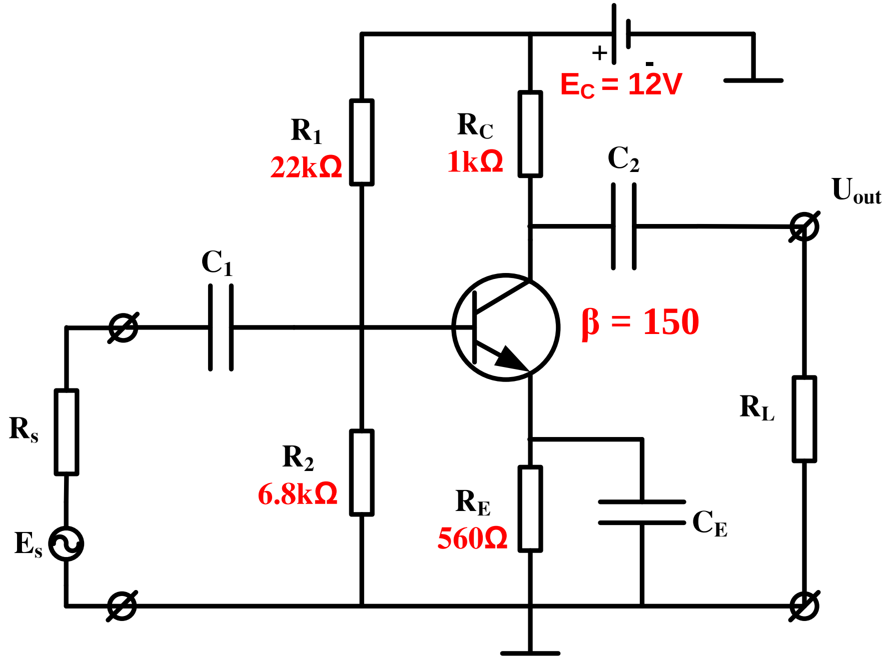
➔ AC input resistance: $r_{IN(base)} = u_{IN}/i_{IN} = U_{BE}/iB = r_B + (1 + \beta_{AC})r_E$

- $r_B$: small ➔ neglected and replaced by a short

  $r_C$: large (hundreds kΩ ➔ replaced by an open

  $r_E$: temperature dependent and $r_E = 0.25mV/I_E$ at 20°C

- **Examlple: DC analysis ➔ Q-point, DC load line, DC load**




➢ **Don't take into account AC components**

➢ **Q-point:**

✓ $R_{IN(base)} = \beta R_E = 150.560\Omega = 84k >> 10R_2 = 68k$

✓ $I_{EQ} = (U_B - U_{BE})/R_E$, where $U_B = E_C R_2/(R_1+R_2) = 2.83$ V

➔ $I_{CQ} \sim I_{EQ} = (2.83V – 0.7V)/560 = 3.8$ mA ➔ $I_{BQ} = I_{CQ}/\beta = 25.33$ μA

✓ $U_{CEQ} \sim E_C – I_C(R_C + R_E) = 12V - 3.8mA\ (1k +560) = 6.07V$

➢ **DC load line equation:** $U_{CEQ} \sim E_C – I_C(R_C + R_E)$; $R_{DCLoad} \sim R_C + R_E$

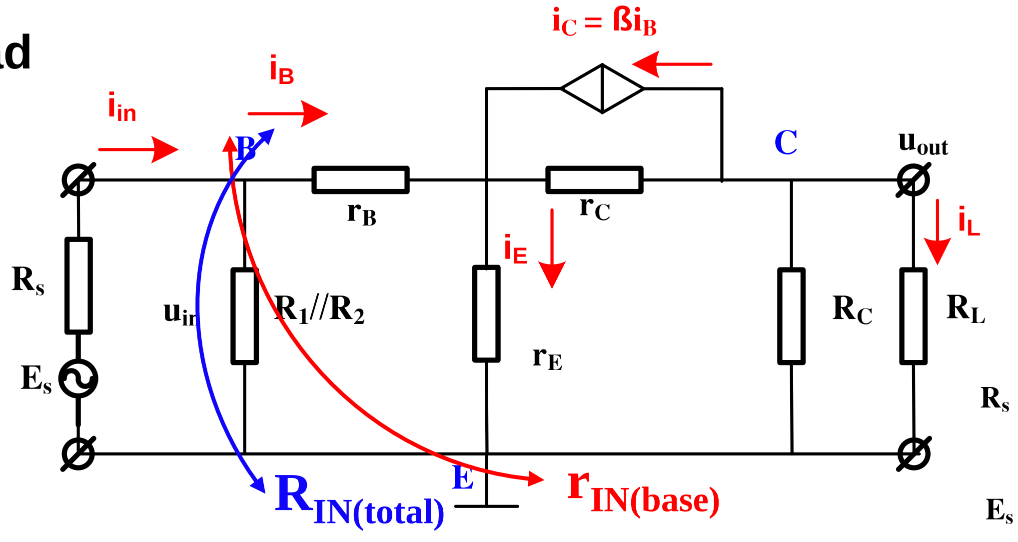
- **Examlple: If input signal with frequency f > 2kHz. Determine by$C_{Emin}$ so that $R_E$ is shorten**

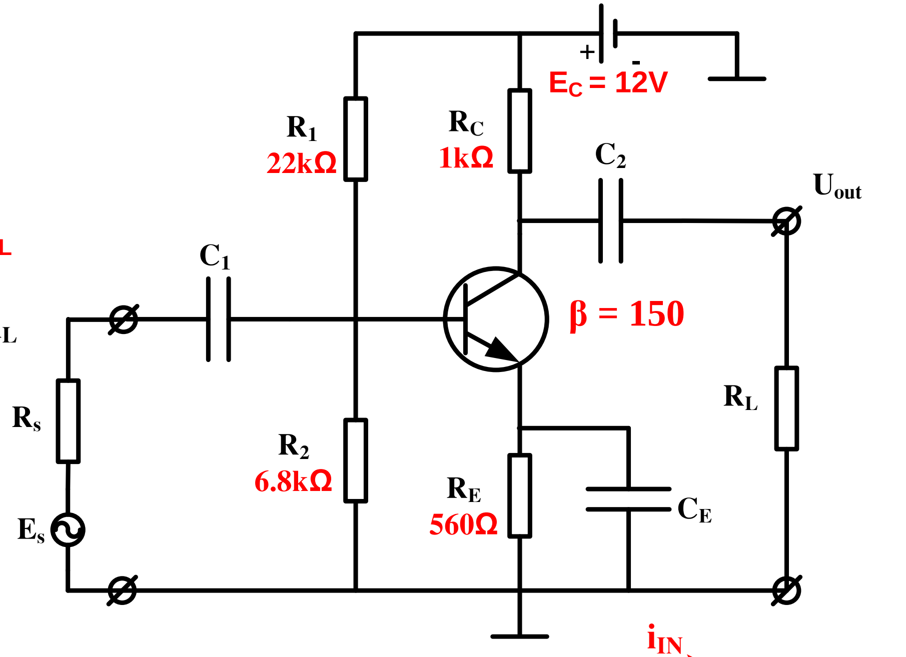
➢ $R_E$ shorten = 0 ➔ $R_E >> 10X_E$ since $R_E//X_{CE}$, where $X_{CE} = 1/(\omega C_E) = 1/(2\pi f C_E)$ is reactance of $C_E$

➢ $X_{CE} < 56$ ➔ $1/(2\pi f C_E) < 56$ ➔ $C_E > 1/(2\pi f.56) = 1.42$ μF ➔ $C_{Emin} = 1.42$ μF

- **AC analysis**: $K_u$, $K_i$, AC load

- AC equivalent:




- Input resistance of transistor at the base: $r_{IN(base)}$

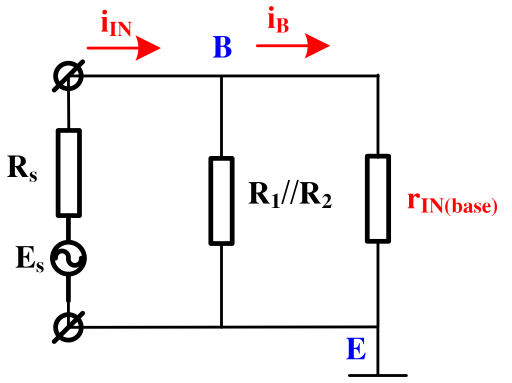
$r_{IN(base)} = U_{BE}/i_B = [i_B r_B + (1 + \beta_{AC}) i_B r_E]/i_B = r_B + (1 + \beta_{AC}) r_E \sim \beta_{AC} r_E$

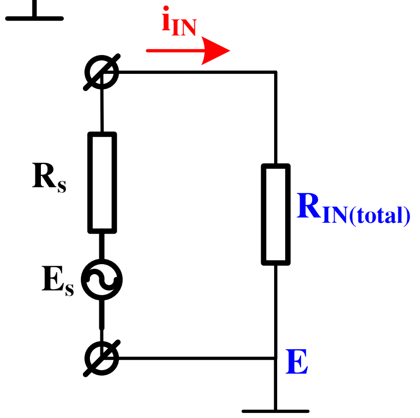
- Input resistance of amplifier: $R_{IN(total)} = R_1//R_2//r_{IN(base)} = R_1//R_2//\beta_{AC} r_E$

- Voltage gain (with $R_L$): $K_u = u_{out}/u_{IN}$

$u_{IN} = i_{IN}(R_s + R_{in(total)}) \sim I_B(R_s + R_{IN(total)})$, assuming $R_1//R_2 >> r_{IN(base)}$

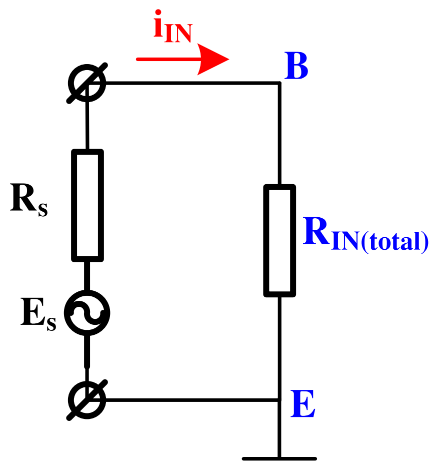
$u_{out} = i_L R_L = I_C R_C R_L/(R_L + R_C) = \beta_{AC} I_B (R_L//R_C) \rightarrow K_u = u_{out}/u_{IN} = \beta_{AC}(R_L//R_C) / (R_s + R_{IN(total)})$



- **Investigate without $R_L$:** $K_u = \beta_{AC}(R_L//R_C) / (R_s + R_{IN(total)}) \sim \beta_{AC}R_C/(\beta_{AC}r_E) = R_C/r_E$
- **Since $(R_C//R_L) < R_C$ ➔ $K_u$ reduced; If $R_L >> R_C$, $(R_C//R_L) \sim R_C$ ➔ $R_L$ no effect on gain**
- **In practice:** attenuation from source to base ➔ $U_B/E_s = R_{IN(total)}/(R_s + R_{IN(total)})$

➔ $K'_u = (U_B/E_S)K_u$



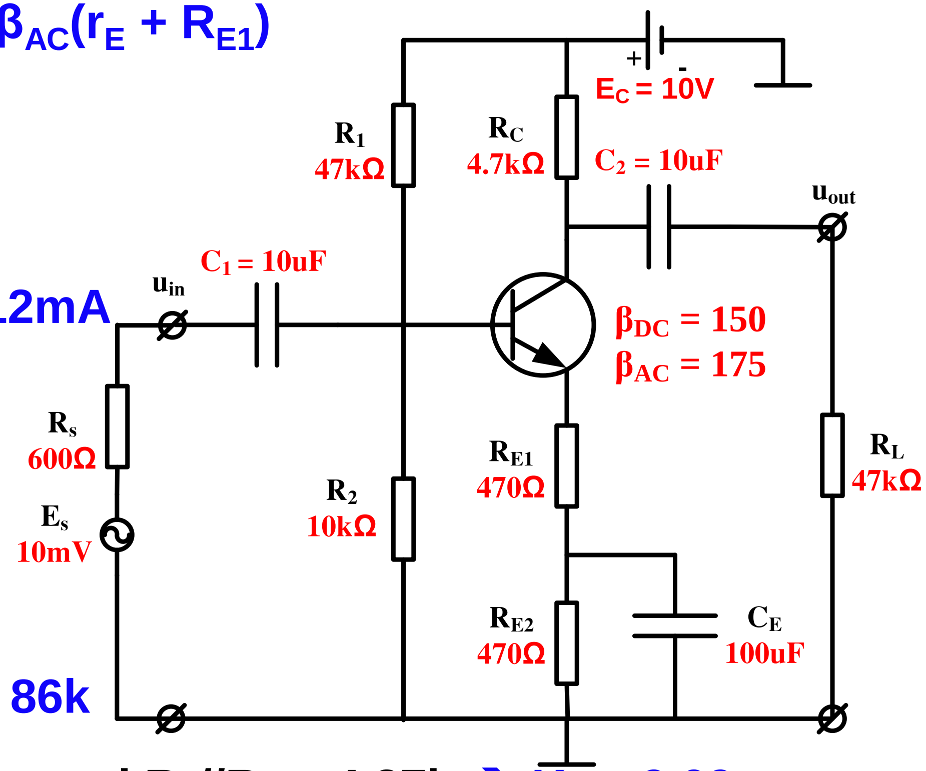

- **Current gain:** $K_i = i_{out}/i_{IN}$, where $i_{IN} \sim i_B$

$i_{out} = i_L = I_CR_C/(R_L+R_C) = \beta_{AC}i_B(R_L//R_C)/R_L$ ➔ $K_i = i_{out}/i_{IN} = \beta_{AC}(R_L//R_C) / R_L$

- **AC load:** $R_{LAC} = R_C//r_C$, however in fact $r_C >> R_C$ ➔ $R_{LAC} \sim R_C$

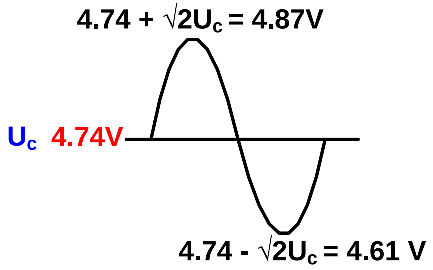
# Chapter 2. Semiconductor Devices (Cont.)

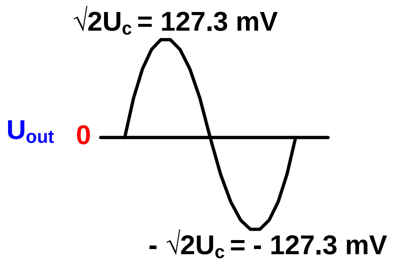
- **Example:** Given a circuit, $R_E$ is partially bypassed by $C_E$ ➔ $R_{in(base)} = \beta_{AC}(r_E + R_{E1})$




a) Determine DC $I_C$, $U_C$

- Since $RI_{N(base)} = \beta(R_{E1} + R_{E2}) = 150 \times 0.94k = 141k > 10R2 = 100k$
- $I_C \sim I_E = (U_B - U_{BE})/(R_{E1} + R_{E2})$; $U_B = E_C R_2/(R_1 + R_2) = 1.75V$ ➔ $I_{CQ} = 1.12mA$
- $U_C \sim E_C - I_C R_C = 4.74\ V$
- $I_{BQ} = I_{CQ}/\ \beta = 7.47\ \mu A$




b) Determine AC $i_C$, $u_C$

- With $C_2$: $R_{IN(base)} = \beta_{AC}(r_E + R_{E1})$, and $r_E = 25mV/I_E = 22\ \Omega$ ➔ $R_{IN(base)} = 86k$
- $K_u = \beta_{AC}(R_L//R_C)/(R_s + R_{IN(total)}) \sim \beta_{AC}(R_L//R_C)/\beta_{AC}(r_E + R_{E1}) = (R_L//R_C)/R_{E1}$ and $R_L//R_C = 4.27k$ ➔ $K_u \sim 9.09$

  ➔ $U_c = K_u E_s = 9.09 \times 10mV = 90mV$ and $R_{IN(total)} = R_1//R_2//r_{IN(base)} = 8.24k//86k = 7.53k$

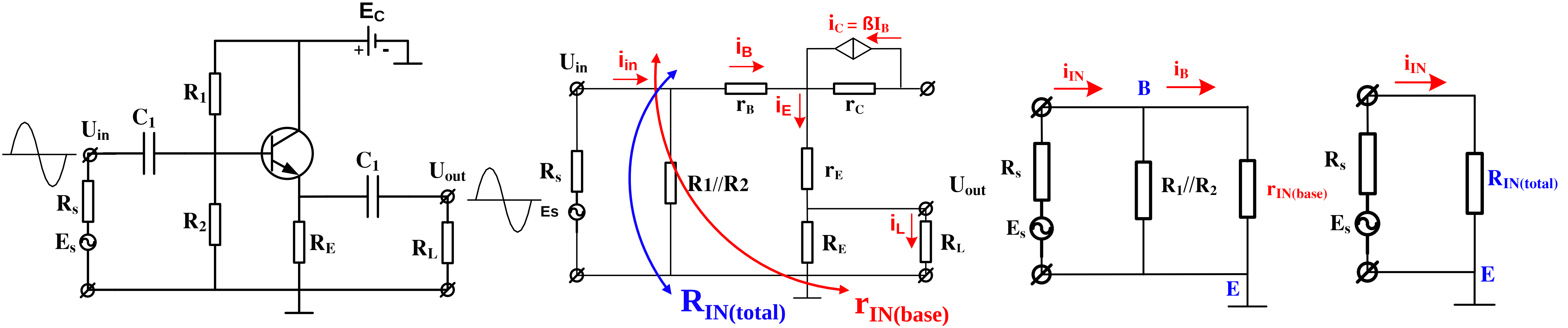
  With attenuation: $U_b = [R_{IN(total)}/(R_s + R_{IN(tota)}]$ and $U'_c = [(U_B/E_s)K_u]E_s$ ➔ $U'_c = 0.93 \times 9.09 \times 10mV = 84.5\ mv$

- $K_i = \beta_{AC}(R_L//R_C)/R_L = 175 \times 4.27k/47k = 15.9$ ➔ $i_C = K_i I_s = K_i E_C/(R_s + R_{IN(total)}) = 15.9 \times 10V/7.53k = 21.11\ mA$

c) Draw total input and output signals in two cases

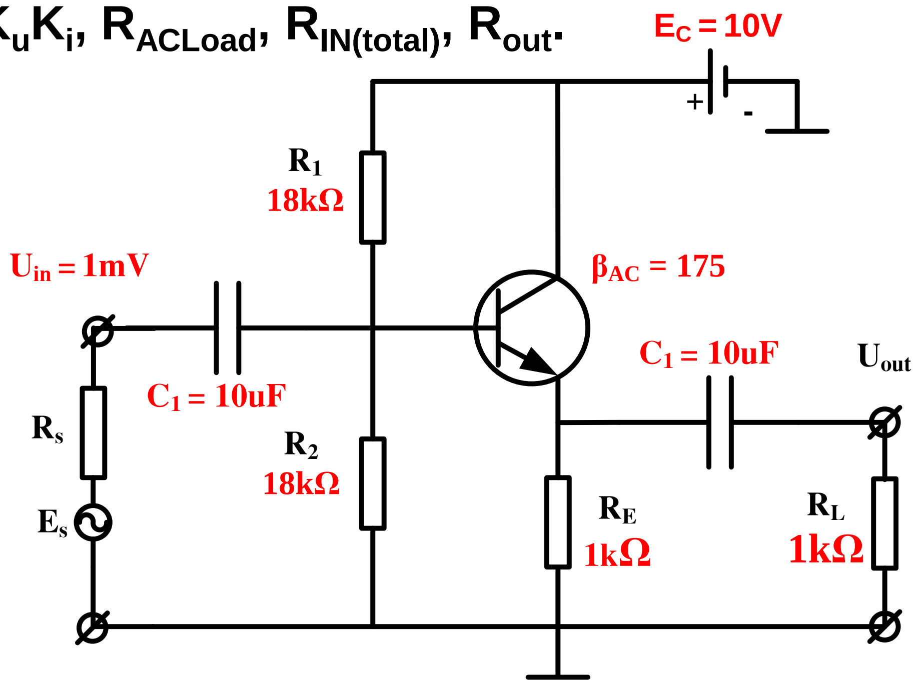
## b) CC amplifier:

- DC analysis: Q-point, DC load line, $R_{LDC}$
- AC analysis: AC equivalent, $K_u$, $K_i$, $R_{LAC.}$ **Note:** $R_E$ still included in AC mode since no bypass capacitor




- Input resistance to the base: $r_{IN(base)} = r_B + (1 + \beta_{AC})(r_E + R_E//R_L)$. If $r_B$ << ➔ $r_{IN(base)} \sim (1 + \beta_{AC})(r_E + R_E//R_L)$
- Input resistance of amplifier: $R_{IN(total)} = R_1//R_2//r_{IN(base)}$. If $R_1//R_2 >> r_{IN(base)}$ ➔ $R_{INtotal} \sim r_{INbase}$
- Voltage gain $K_u = (1 + \beta_{AC})(R_E//R_L)/(R_s + R_{INtotal})$. If $R_s = 0$, $r_E << R_E//R_L$ ➔ Ku ~ 1 ➔ No voltage amplification
- Current gain: $K_i = i_{out}/i_{IN} = i_E/i_{IN} =[u_{out}/(R_E//R_L)] / (U_{in}/R_{IN(total)})$; AC load $R_{LAC} = R_E//r_E$

- **Example:** Determine the DC mode of CC amplifier. Find $K_u$, $K_i$, $K_p = K_uK_i$, $R_{ACLoad}$, $R_{IN(total)}$, $R_{out}$.




➢ **DC mode:** By yourself

✓ $Q (I_{BQ}, I_{EQ}, U_{CEQ}) = (28.67\mu A, 4.3mA, 5.7V)$

✓ DC load line equation: $U_{CE} = E_C - I_ER_E$; $R_{LoadDC} = R_E = 1k$

➢ **AC mode:**

✓ $K_u = (1 + \beta_{AC})(R_E//R_L)/(R_s + R_{INtotal})$ ➔ $K_u \sim (R_E//R_L)/(r_E + R_E//R_L)$

✓ $r_E \sim 25mV/I_E = 5.8\ \Omega$; $R_E//R_L = 0.5k$; $r_{IN(base)} = (1 + \beta_{AC})(r_E + R_E//R_L) = 87.5k$

✓ $R_{IN(total)} = R_1//R_2//r_{IN(base)} \sim 9k//87.5k = 8.16k$

✓ $K_u \sim (R_E//R_L)/(r_E + R_E//R_L) = 0.5k/508.8\ \Omega \sim 0.989$

➢ $K_i = i_E/i_{IN} =[u_{out}/(R_E//R_L)] / (U_{in}/R_{IN(total)})$

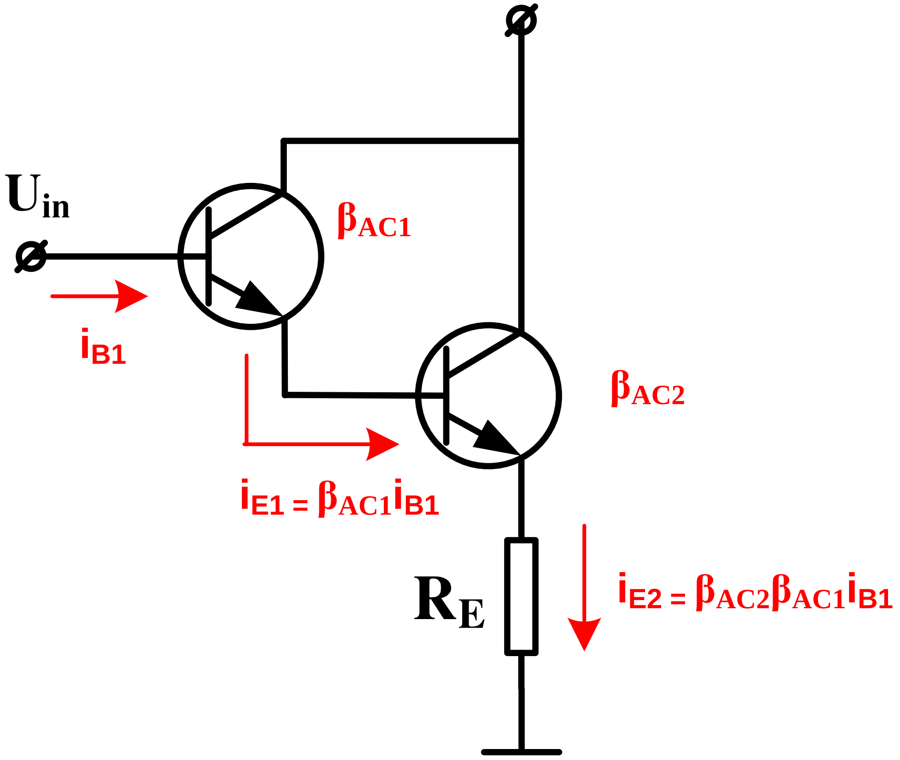
✓ $u_{out}/(R_E//R_L) = K_uu_{IN}/(R_E//R_L) = 1mV/0.5k = 2\mu A$; $u_{in}/R_{IN(total)} = 1mV/8.16k = 0.122\ \mu A$ ➔ $K_i = 2/0.122 = 16.39$

➢ $K_p = K_uKi = 0.989 \times 16.39 = 16.21$; $R_{ACLoad} = R_E//R_L = 0.5k$ ➔ Power dissipated on $R_L = 1/2K_p = 8.1$

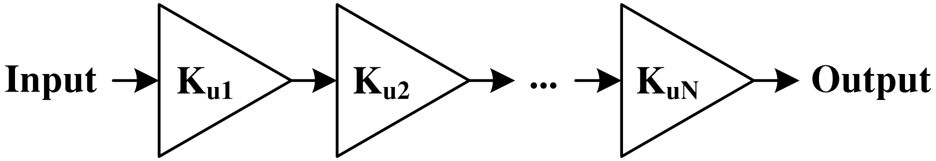
- **Darlington pair: for greater input resistance**

➢ **Effective current gain:** $\beta_{AC} = \beta_{AC1}\beta_{AC2}$

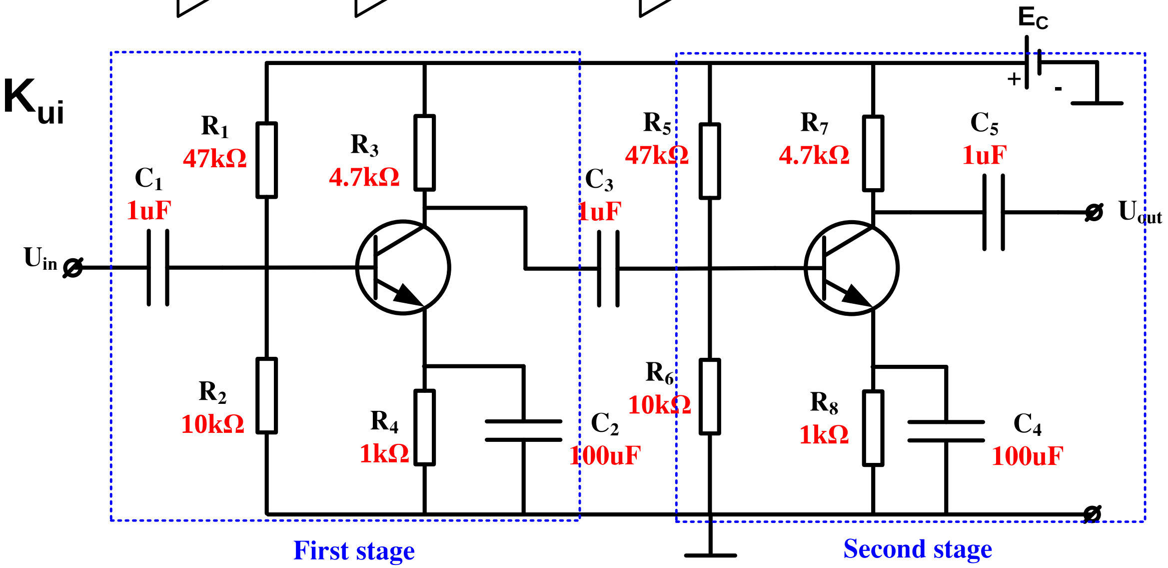
➢ **If** $r_E << R_E \Rightarrow R_{IN} = \beta_{AC}R_E$

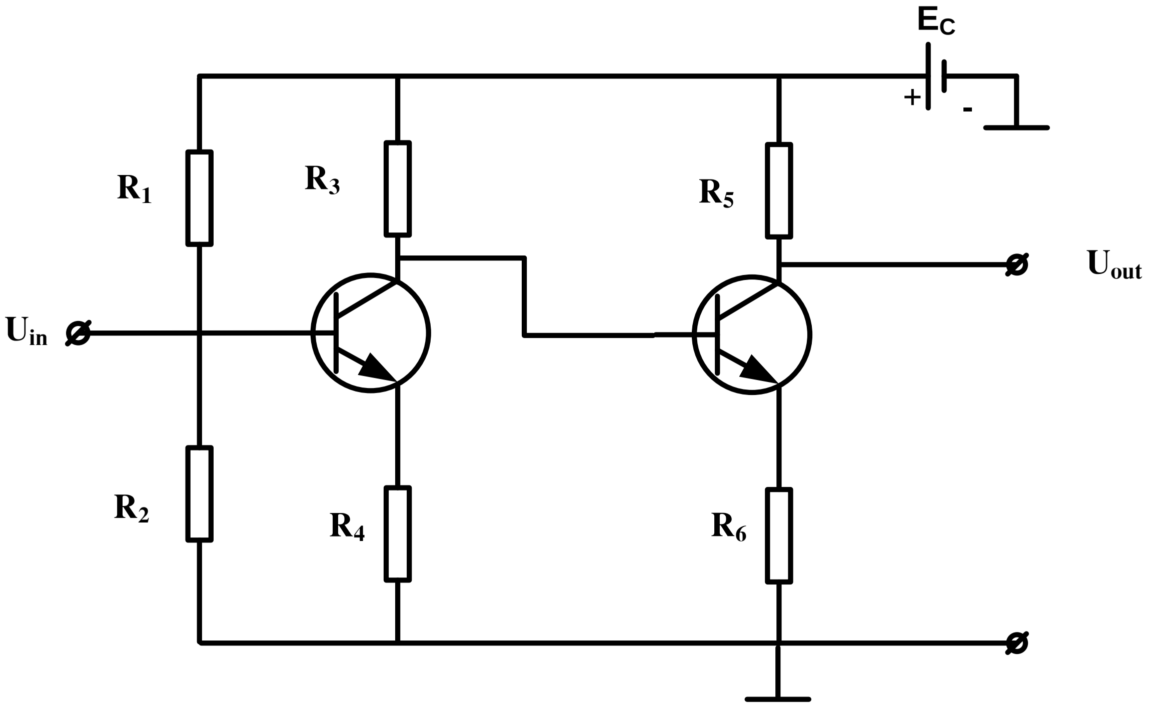


## 2.2.6. Multistage amplifier




- **Cascade arrangement for greater voltage gain**
- **Overall gain: $K_u = K_{u1}K_{u2}\ldots K_{uN}$. In decibels: $K_{ui,(DB)} = 20\log K_{ui}$**
- **Overall gain in DB: $K_{u,DB} = K_{u1,DB} + K_{u2,DB} + \ldots K_{uN,DB}$**
- **Capacitively coupled amplifier**




- **Direct-coupled amplifier:**

✓ **Better low-frequency response**

✓ **If using C, very high $R_{IN}$**

✓ **$R_{in}$ high reduces gain**

# Chapter 2. Semiconductor Devices (Cont.)

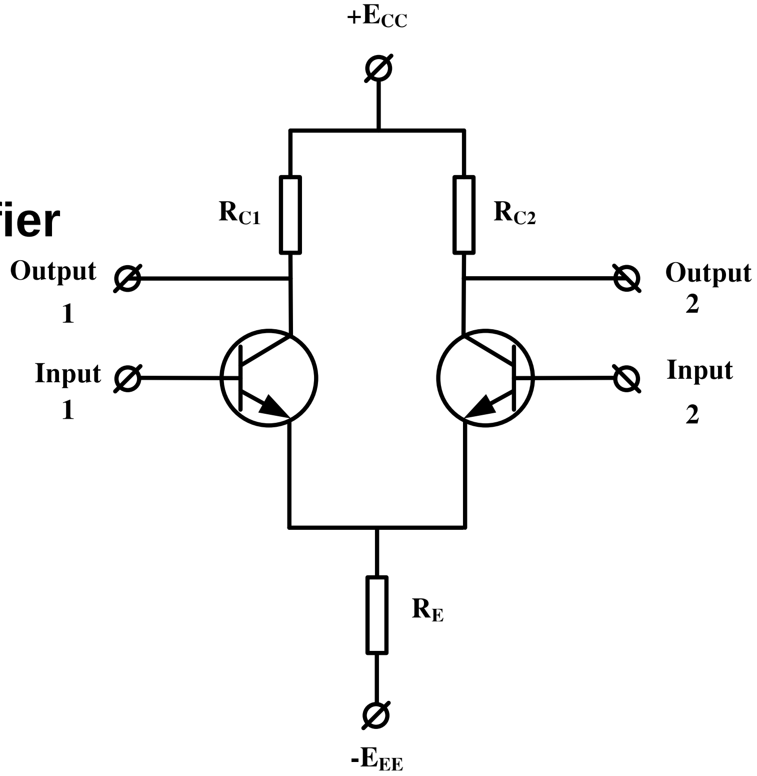
2.1. PN Junction - Diode and application

2.2. Bipolar Junction Transistor (BJT) and applications

**2.3. Operational amplifier (OPAM) and applications**

2.4. Voltage regulation

## 2.3.1. Differential amplifier




- 2 EC amplifiers with 2 bias sources
- Mutistage differential amplifiers + push-pull ➔ OPAM: operational amplifier
- $\Delta U_{out} = U_{out2} - U_{Out1} = K_{diff}\,\Delta I_{in}$

  or $\Delta U_{out} = K_{diff}(U_{in2}-U_{in1})$

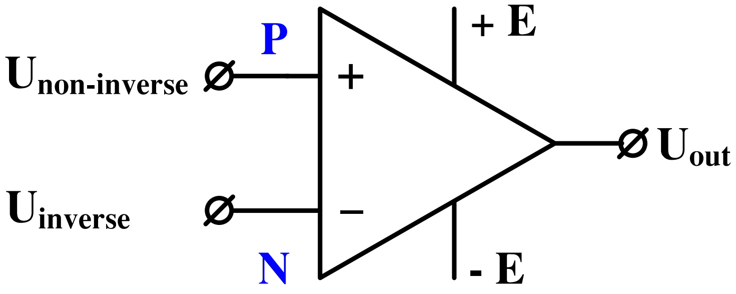
  ✓ If $U_{in1}$ = 0 (grounded): $\Delta u_{out} = K_{diff}U_{in2}$.

  If $U_{out1}$ grounded ➔ $U_{out2} = K_{diff}U_{in2}$ ➔ $U_{in1}$: Non-inverse input (P)

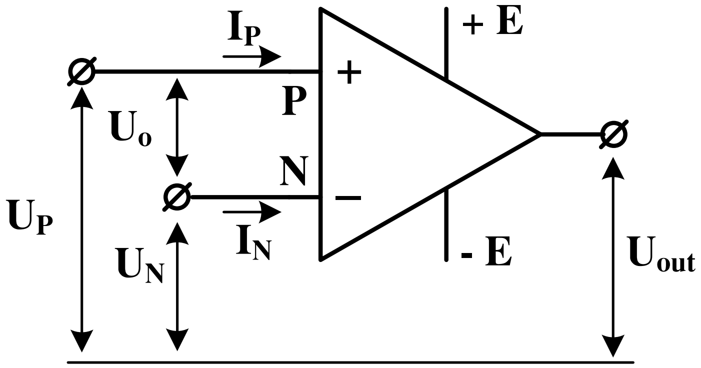
  ✓ If $U_{in2}$ = 0 (grounded): $\Delta u_{out} = - K_{diff}U_{in1}$.

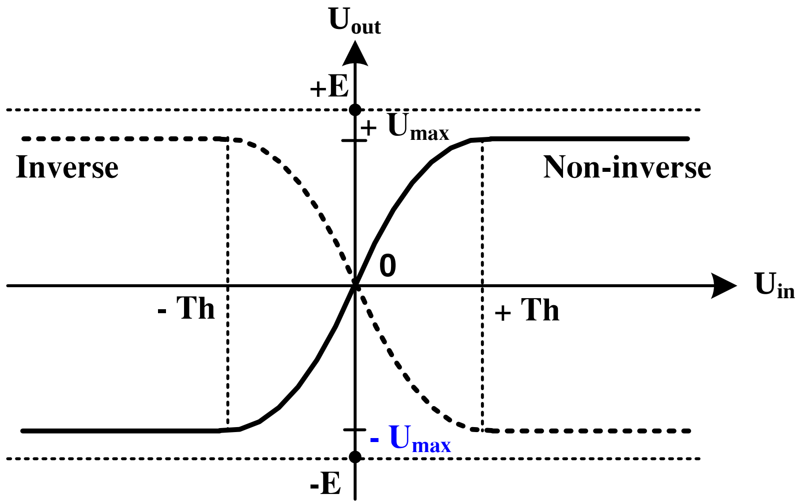
  If $U_{out1}$ grounded ➔ $U_{out2} = - K_{diff}U_{in1}$ ➔ $U_{in1}$: Inverse input (N)

- Input resistance: very large; Output resistance: very small
- Amplifier gain: $K_{OPAM} = 10^4 – 10^6$ (ideal: infinity)



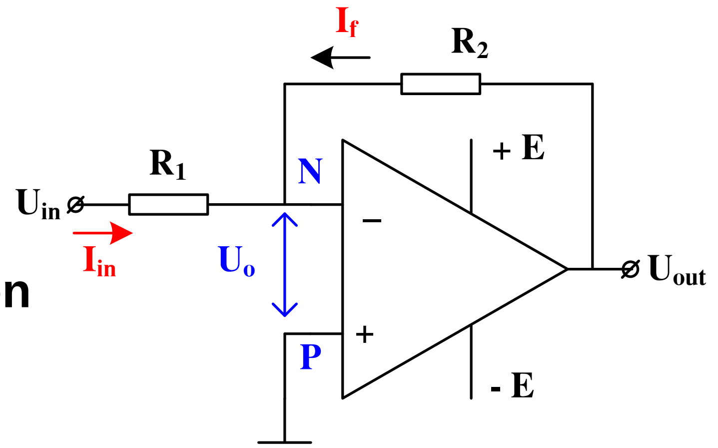
## 2.3.2. OPAM




- **Ideal OPAM:**
  - ✓ **If $U_{in} = 0$, $U_{out} = K_{OPAM}U_{in} = 0$**
  - ✓ **Rin = ∞ (open); Rout = 0 (**
  - ✓ **$K_{OPAM} = \infty$**
  - ✓ **$U_P - U_N = U_{out}/K_{OPAM} = 0 \Rightarrow U_P = U_N$**
  - ✓ **$I_P = I_N = 0$ (small base currents at inputs)**
- **Practical OPAM**
  - ✓ **$U_{out} \neq 0$ when $U_{in} = 0$ ➔ Define Input offset voltage $U_{os}$ (differential DC inputs) to forse $U_{out} = 0$**
  - ✓ **$I_{BIAS} = (I_P + I_N)/2$ ➔ DC current required by the inputs**
  - ✓ **Input offset current $I_{os}$: base currents at input of OPAM are not always equal**
- **Transfer characteristic: relation between input and output ➔ inverse and non-inverse characteristic**
  - ✓ **$+ U_{max}/ - U_{max}$: Max/min achievable output value (saturated output)**
  - ✓ **Linear amplification and saturation**

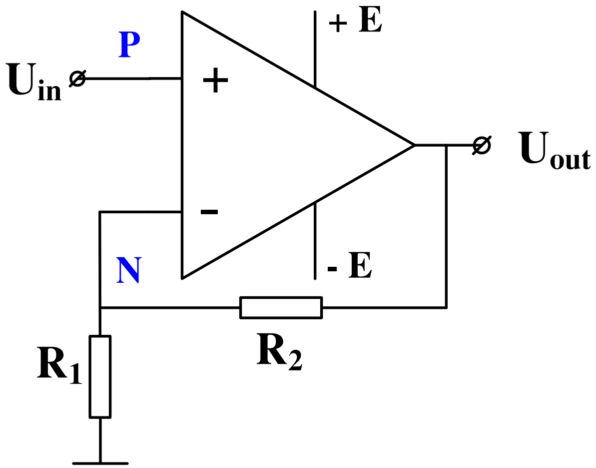
## 2.3.3. Applications of OPAM




a) Inverting amplifier: Input resistor $R_1$, feedback resistor $R_2$

- Negative feedback: Since KOPAM large ➔ NF to avoid saturation
- Node N: $I_{in} + I_f = 0$ (applying KCL, assuming $I_N = 0$)
- Ohm law: $I_{in} = (U_{in} – U_N)/I_{in}$; $I_f = (U_{out} – U_N)/R_2$ . Since $U_N = U_P = 0$ (Ideal OPAM) ➔ $U_{out} = - (R_2/R_1)U_{in}$
- Negative sign: Input and output signals out-of-phase

b) Non-Inverting amplifier: Input resistor $R_1$, feedback resistor $R_2$




- Negative feedback
- Node N: $U_N = R_1/(R_1 + R_2)U_{out} = U_P = U_{in}$

➔ $U_{out} = + R_1/(R_1 + R_2)U_{in}$

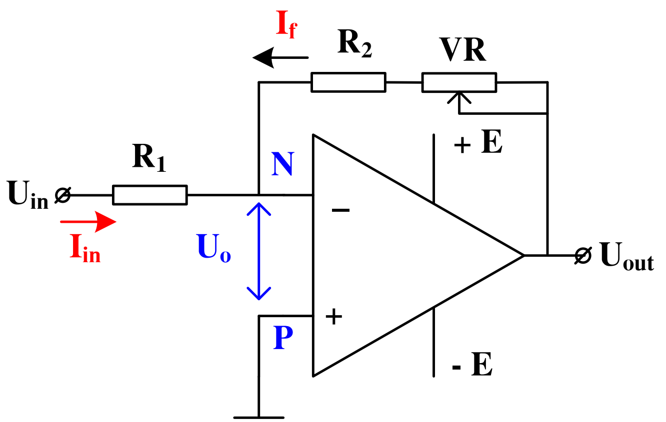
- Positive sign: Input and output signals in-phase

## Example 1

Add $VR_2$ – a potentiometer 120 KΩ to inverting amplifier. $U_{max}$ = ± 12 V $R_1$ = 1.5 KΩ, $R_2$ = 3.3 KΩ

a) Derive equation for $K_u$

b) If $U_{in}$ = 200mV, $V_R$ =? for linear operation

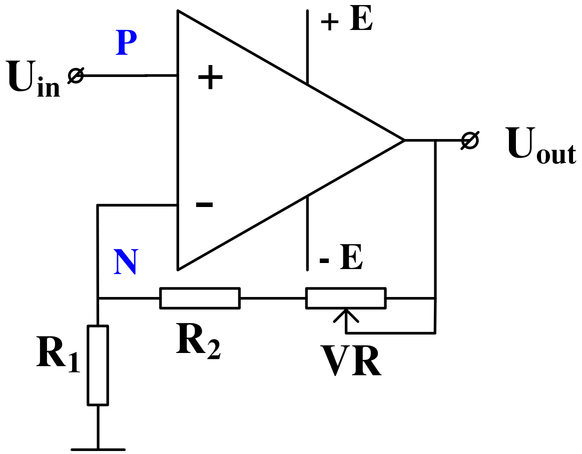



## Example 2

Replace $R_2$ = $VR_2$ - potentiometer 120 KΩ. $U_{max}$ = ±12 V $R_1$ = 1.5 KΩ, $R_2$ = 3.3 KΩ

a) Derive equation for $K_u$

b) If $U_{in}$ = 200mV, $V_R$ =? when saturation occurs

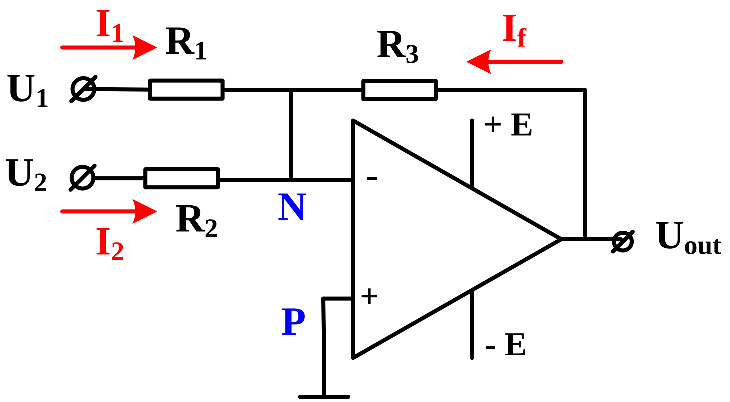


## c) Inverse summing amplifier

- Negative feed back
- Node N: $I_1 + I_2 = I_f$ (applying KCL, assuming $I_N = 0$)
- Ohm Law:

  $I_1 = (U_1 - U_N)/R_1$; $I_2 = (U_2 - U_N)/R_2$; $I_f = U_{out} - U_N)/R_f$
- Since $U_N = U_P = 0$ (ideal OPAM)

  ➔ $U_{out} = -(R_f/R_1)U_1 - (R_f/R_2)U_2$
- If $R_1 = R_2 = R_f$ ➔ $U_{out} = -(U_1 + U_2)$

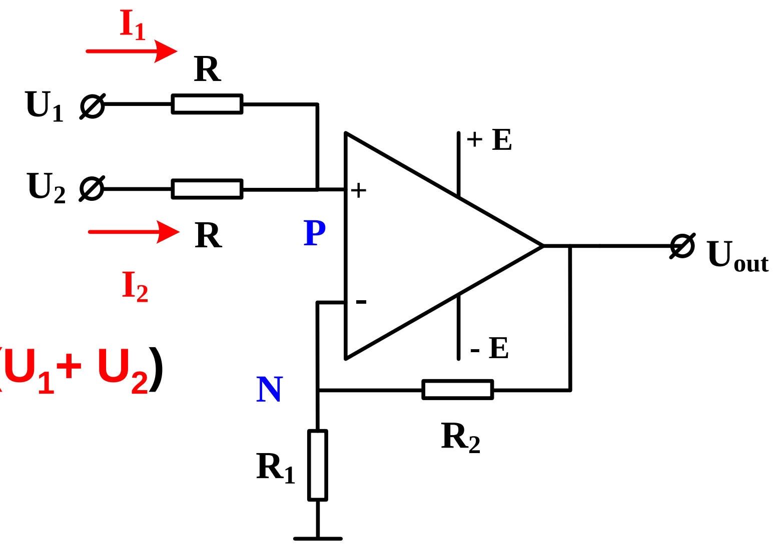



## d) Non-inverse summing amplifier

- Negative feed back
- Node N: $U_N = U_{out}R_1/(R_1 + R_2)$
- Node P: $I_1 = (U_1 - U_P)/R$; $I_2 = (U_2 - U_P)/R$ and $I_1 + I_2 = 0$

  ➔ $U_P = 1/_2(U1 + U_2)$
- Since: $U_N = U_P = U_{out}R_1/(R_1 + R_2)$

  ➔ $U_{out} = [(R_1 + R_2)/(2R_1)](U_1 + U_2)$

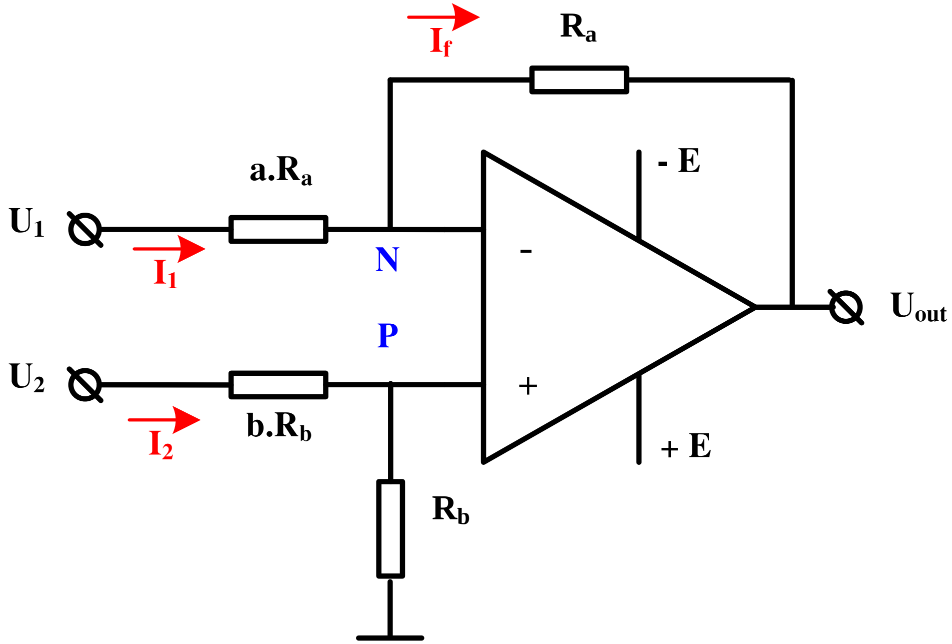



- If $R_1 = R_2$ ➔ $U_{out} = (U_1 + U_2)$

e) Subtracting amplifier:

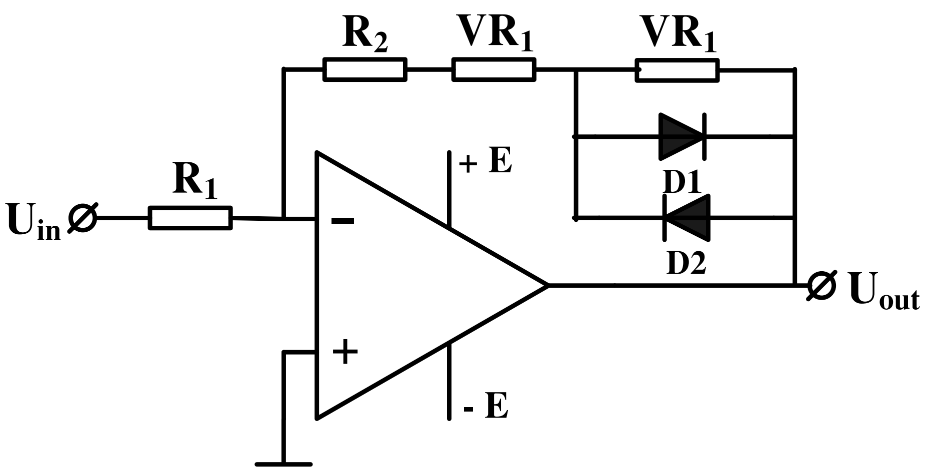
- Negative feed back
- Node N: $I_1 = (U_1 - U_N)/(aR_a)$; $I_f = (U_N - U_{out})/R_a$, and $I_1 - I_f = 0$ or $I_1 = I_f$

  ➔ $U_N = (aU_{out} + U_1)(a+1)$
- Node P: $U_P = U_2R_b/(R_b + bR_b) = U_2/(b+1)$
- Since $U_N = U_P$: $U_{out} = (a + 1)/[a(b + 1)]U_2 - U_1/a$
- If $(a = b)$: $U_{out} = 1/a(U_2 - U_1)$; and if $a = b = 1$ ➔ $U_{out} = U_2 - U_1$

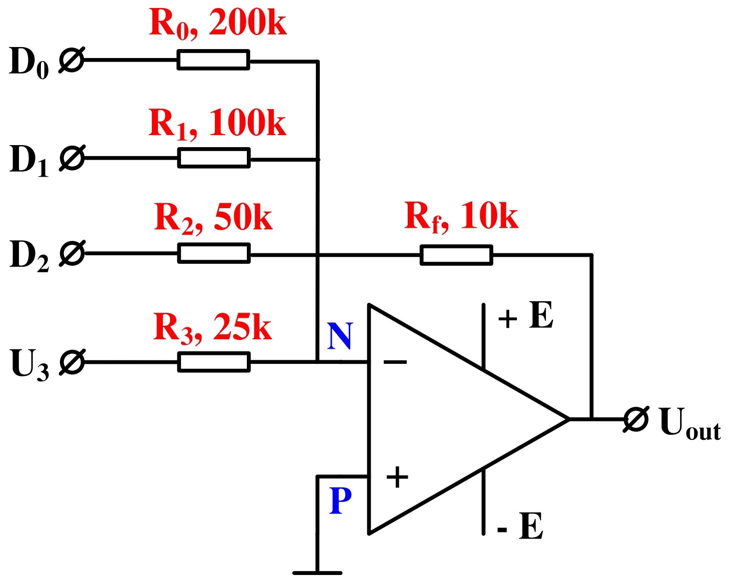


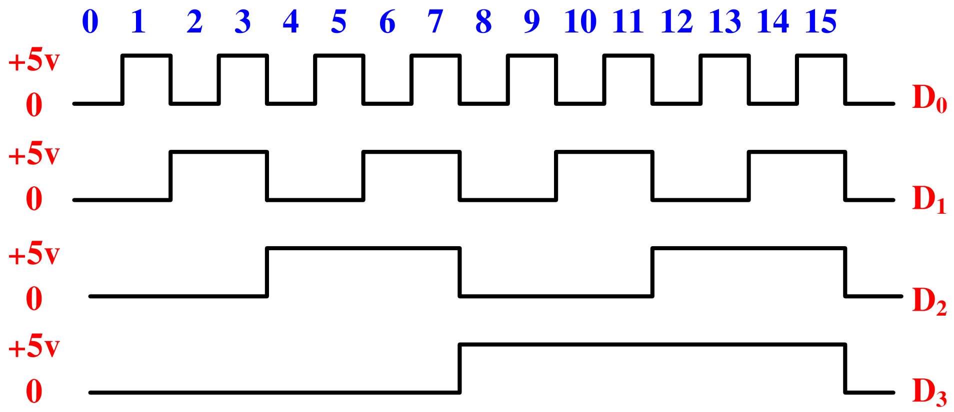
**Quick test 9**

**Explain the effect of D1, D2 added to an inverting amplifier given below**



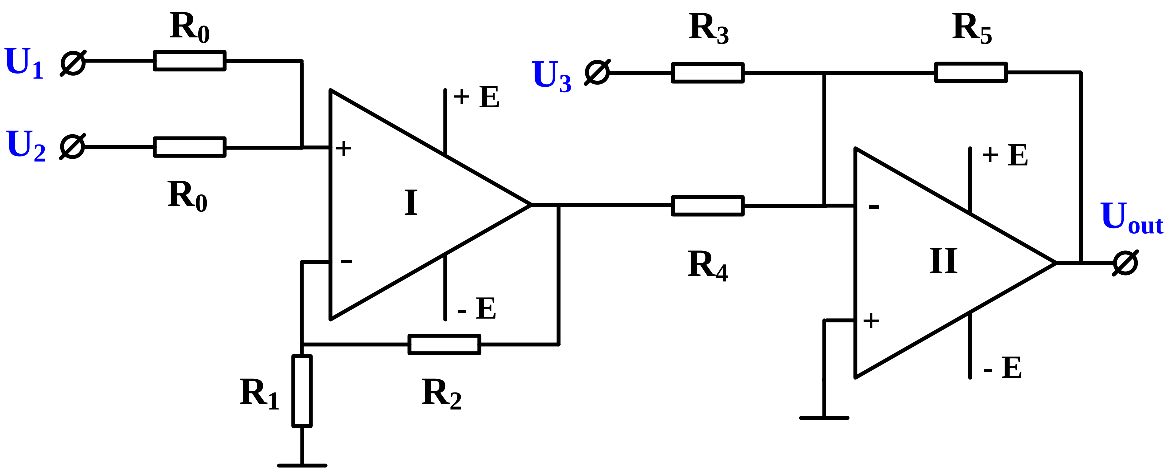

**Quick test 10:** **Demonstrate output DAC (Digital to Analog Converter) for 4-digit sequence given in waveforms of inputs $D_0$, $D_1$, $D_2$, $D_3$**



## Quick test 11

**Establish relation between output $U_{out}$ and inputs $U_1$, $U_2$, $U_3$ according to given circuit's elements**

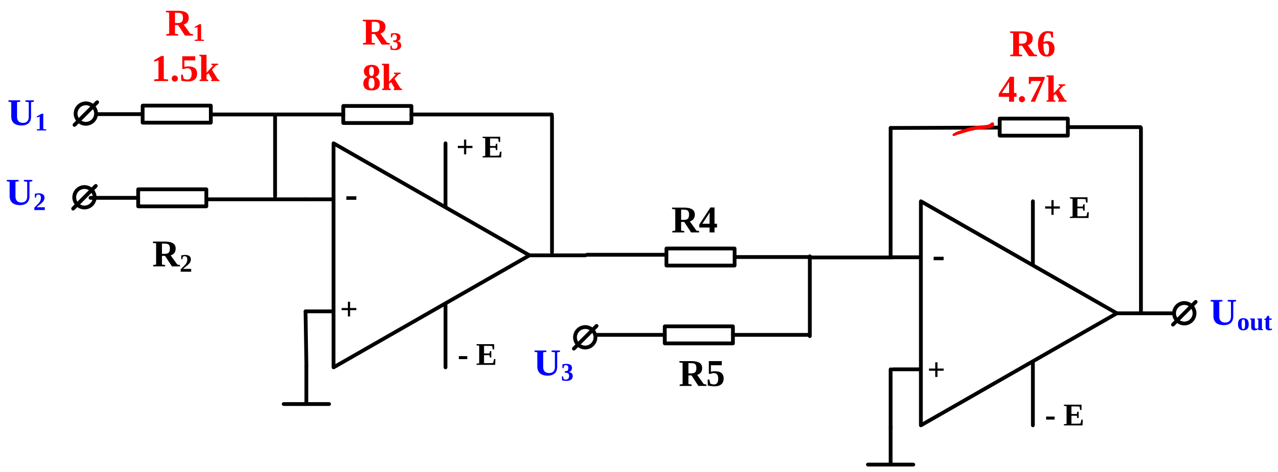



## Quick test 12

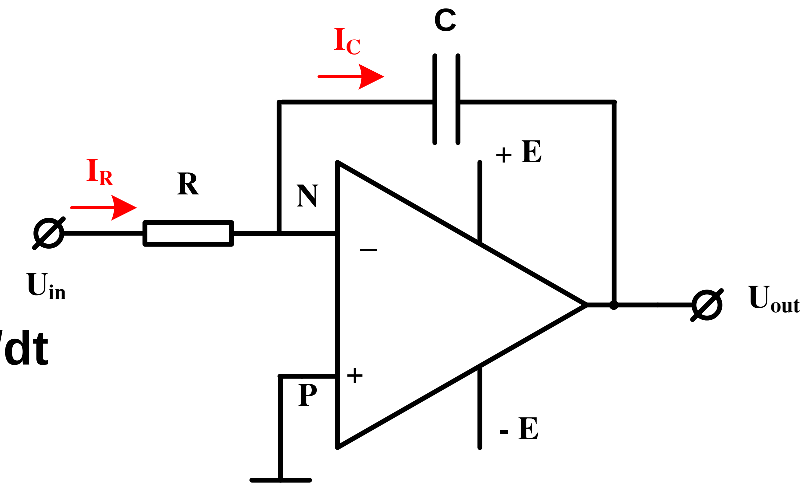
**a) Establish relation between output $U_{out}$ and inputs $U_1$, $U_2$, $U_3$ according to given circuit's elements**

**b) Determine $R_2$, $R_4$, $R_5$ for getting this equation:**

$$U_{out} = 2.5U_1 + 4.7U_2 - 4.1U_3$$



## f) Integrator:

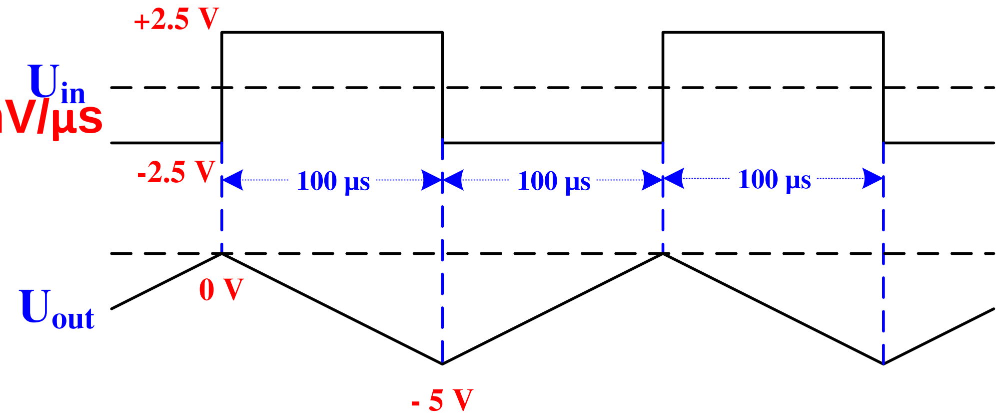



- Negative feed back
- Capacitor C: feedback resistor replaced by C, which operates in charged and discharged period
- Node N: $I_R - I_C = 0$, where $I_R = (U_{in} - U_N)/R$ and $I_C = Cd(U_C/dt) = C(U_N - U_{out})/dt$
- Since: $U_N = U_P = 0$ ➔ $U_{out} = -1/(RC) \int U_{in}dt + U_0$ ~ Rate of input change

  where $U_0$: initial potential on C before integration ➔ $U_0 = 0$?

  Here: T = RC – integral constant related to rate of change (RoC) at output according to the change of input

- Example: R = 10 kΩ, C = 0.01 µF ➔ T = RC = 0.1 ms



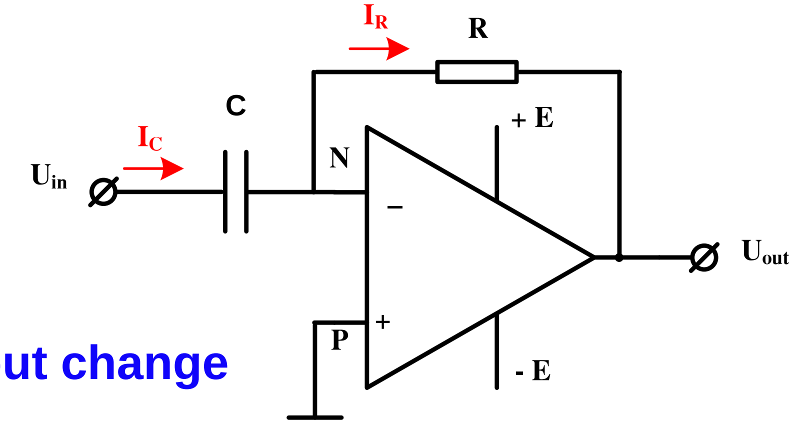

✓ RoC for negative ramp: $\Delta U_{out}/\Delta t = -U_{in}/(RC) = -5V/0.1$ ms = - 50 mV/µs

✓ RoC for positive ramp: $\Delta U_{out}/\Delta t = +50$ mV/µs, where $\Delta t = 100$ µs

✓ Therefore: $\Delta_{Uout} = 5V$ ➔ When $U_{in} = +2.5V$, $U_{out} = 0 \rightarrow -5V$;
When $U_{in} = -2.5V$, $U_{out} = -5V \rightarrow 0V$

✓ QUESTION: If $U_{out}$ changes 0 -> - 5 V with the same input in 50 µs ➔ What modification in the circuit?

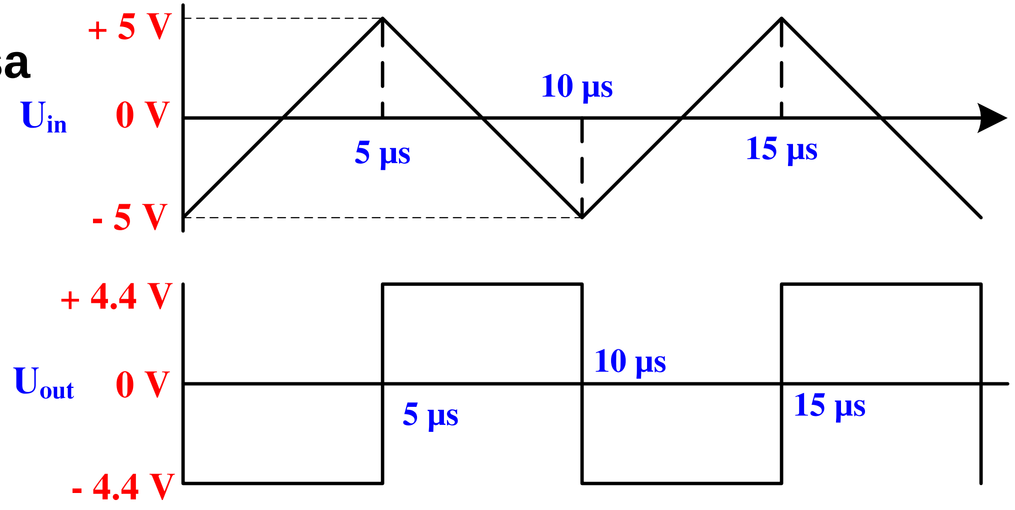
## g) Diffrentiator:




- Negative feed back;
- Capacitor C: Input resistor is replaced by C interval
- Node N: $I_C - I_R = 0$, where $I_C = Cd(U_{in} - U_N)/dt$ and $I_R = (U_N - U_{out})/R$
- Since $U_N = U_P = 0$ ➔ $CdU_{in}/dt = - U_{out}/R$ ➔ $U_{out} = - (RC)dU_{in}/dt$ ~ Rate of input change

Here: T = RC – differential constant related to the achieved value of output according to RoC of input

- Example: C = 0.001 μF, R = 2.2 kΩ ➔ T = RC = 2.2 μs




✓ RoC $U_C/t$ : $U_C$ changes from -5 V to + 5 V in 5 μs and vice versa

➔ $U_C/t$ = 10V/5μs = 2V/ μs

✓ Therefore: $U_{out} = - (U_C/t)RC$

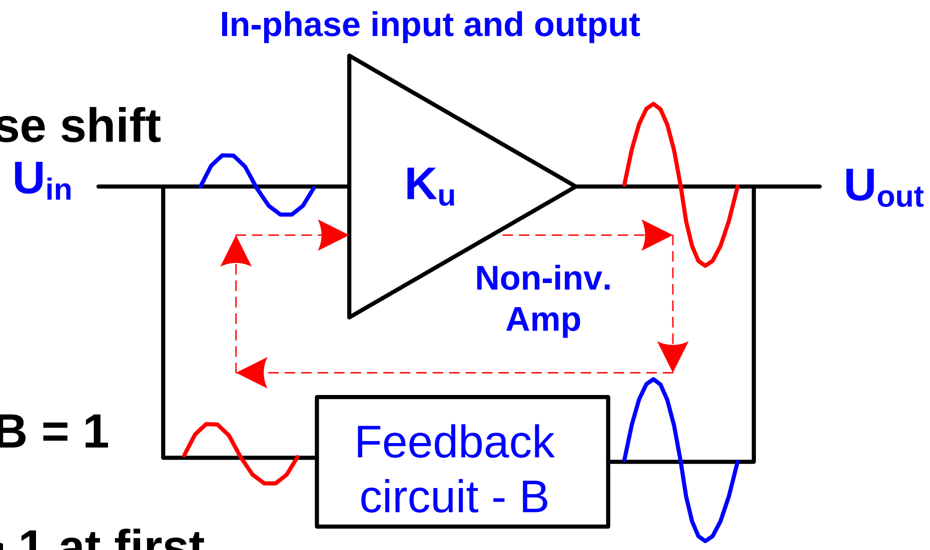
- ✓ Postive ramp: Uout = - 2V/μs x 2.2 μs = - 4.4 V
- ✓ Negative ramp: Uout = -(- 2V/μs) x 2.2 μs = + 4.4 V

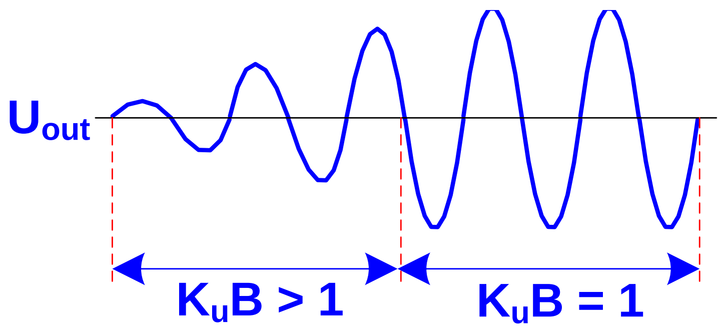
✓ QUESTION: If R = 3.3kΩ ➔ What is the output changed?

## 2.3.4. Signal oscillators

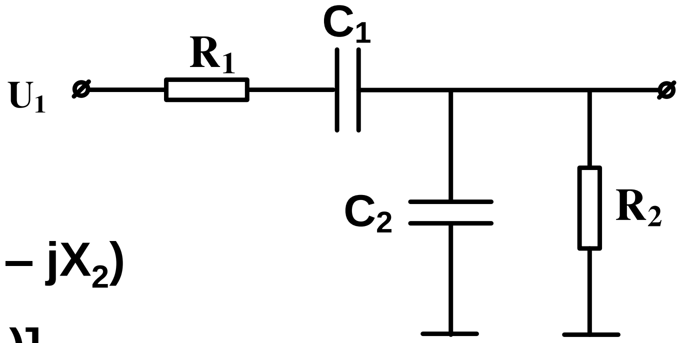
### a) Principle:

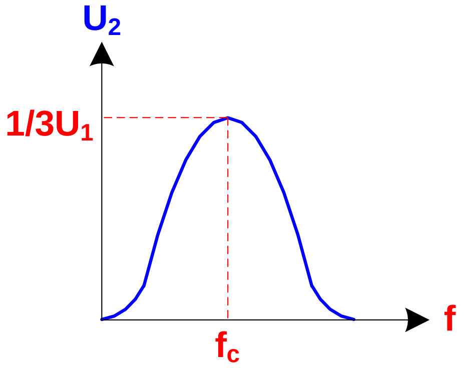
- **Positive feedback:** In-phase output is fed back to input with no phase shift
- **Close loop:** created by forward amplifier and feedback curcuit
- **Desired output:** sinusoidal signal
- **Condition for oscillation:** 1) Phase shift around feedback = 0; 2) $K_u.B = 1$
- **Start-up condition:** When DC supply is on, voltage gain should be > 1 at first to produce a desired output amplitude and oscillation is maintained



## b) Oscillator with RC feedback circuits



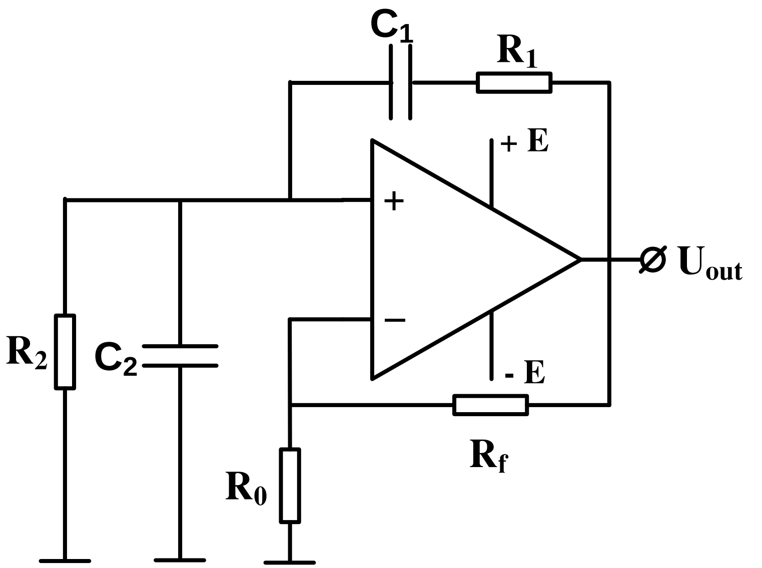




### b1. Wien – Robinson bridge oscillator

- Lead-leg circuit: $Z_{(R1\text{-}C1)} = R_1 - jX_1$; $Z_{(R2\text{-}C2)} = R_2(-jX_2)/(R_2 - jX_2)$

✓ if $R_1 = R_2 = R$, $C_1 = C_2 = C$ ➔ $U_2 = U_1[X_{R1\text{-}C1}/(Z_{R1\text{-}C1} + Z_{R2\text{-}C2})]$
➔ $U_2/U_1 = RX/[3RX + j(R - X)^2]$

✓ At resonance frequency $f_c$: $U_2/U_1 = 1/3$ or $U_2 = 1/3U_1$ since $R = X$ at $f_c$




- Wien – bridge oscillator: Utilization of led-lag circuit ➔ $U_{out} = U_1$, $U_P = U_2$

✓ Non-inverting amplifier gain: $K_u = 1 + R_f/R_0$, ➔ input – output are in-phase

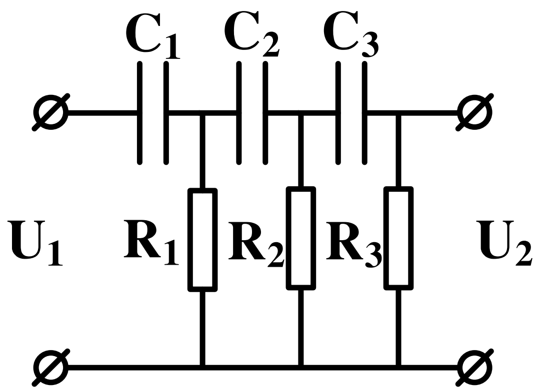
✓ Lead-leg feed back gain: $B = U_{out}/U_P = 1/3$

✓ Since $K_uB = 1$ ➔ $K_u = 3$ ➔ $R_f/R_0 = 2$ ➔ $R_f = 2R_0$

✓ Start-up condition: $K_u > 3$ ➔ $R_0$ replaced by a potentiometer, or back-to-back Zener diode

- Output signal frequency: resonance $f_c = 1/(2\pi RC)$

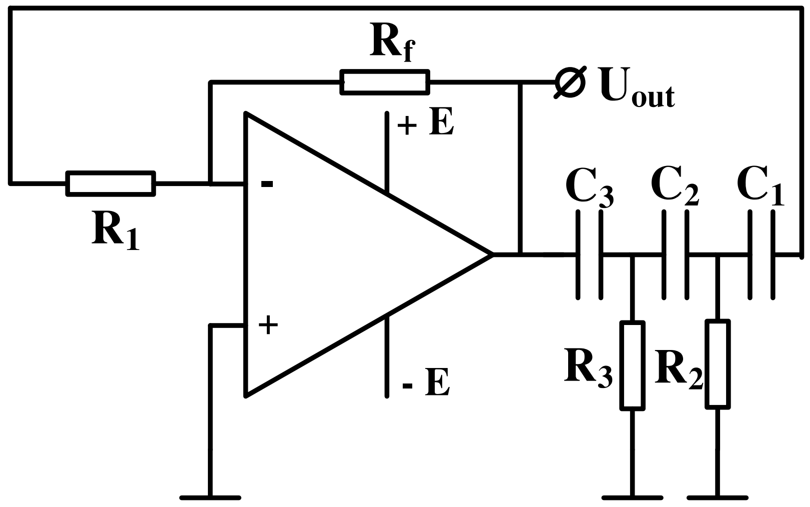
## b2. Phase-shift oscillator:




- **RC ladder:** Each RC shifts phase with max $90^0$. Oscillation occurs at frequency with total phase shift of $180^0$.
- If $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$: $U_2/U_1 = 1/29$
- **RC phase shift oscillator:** based on inverting amplifier ➔ Input and output out-of-phase ➔ After RC ladder, total phase shift is $360^0$ or $0^0$
- **Feedback RC ladder:** $B = U_2/U_1 = U_{out}/U_N = 1/29$

✓ **Since $K_uB = 1$:** $K_u = 1/29$ ➔ $R_f/R_0 = 29$ ➔ $R_f = 29R_0$

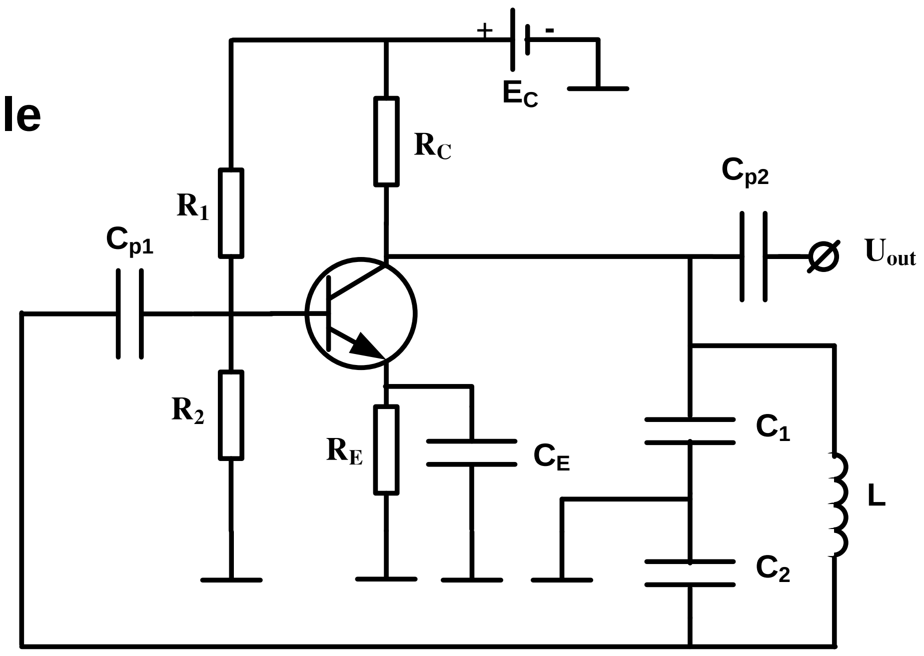
- **Output signal frequency:** resonance $f_c = 1/(2\pi\sqrt{6}RC)$



## b3. Colpitts oscillator

- **Feedback by $C_1$, $C_2$, L: Used for necessary phase shift and plays role of resonant filter to pass signal of desired frequency at oscillation**
- **Output signal frequency: resonance $f_r = 1/(2\pi\sqrt{LC_{equivalent}})$**

  **where $C_{equivalent} = C_1C_2/(C_1 + C_2)$**
- **$B = U_f/U_{out} = IX_{C1}/IX_{C2} = 1/(2\pi f_r C_1)/1/(2\pi f_r C_2)$ ➔ $B = C_2/C_1$**
- **Since $K_uB = 1$ ➔ $Ku = C_1/C_2$**
- **Start-up condition: Initially $K_uB > 1$**

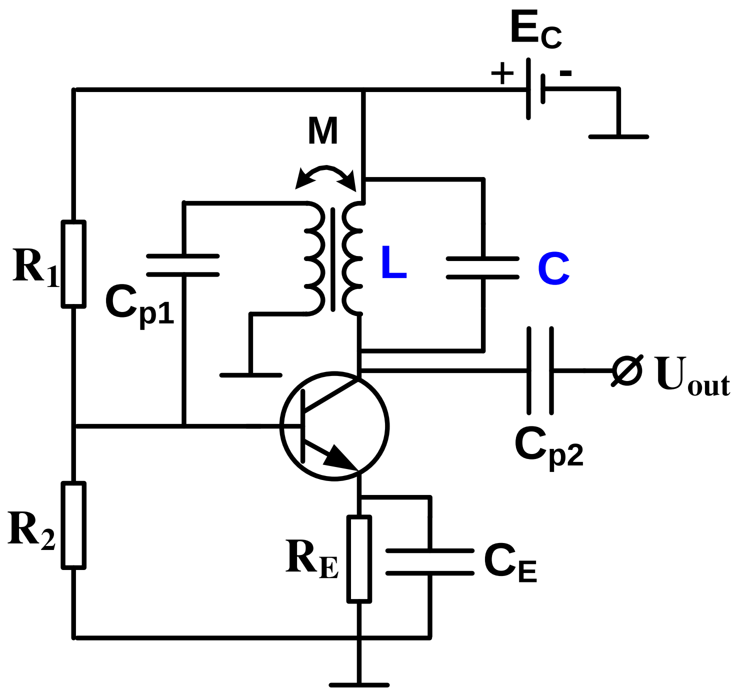


## b4. Maisne oscillator

- **Feedback by $C_1$, $C_2$, L: Used for necessary phase shift and plays role of resonant filter to pass signal of desired frequency at oscillation**

- **Output signal frequency: resonance $f_c = 1/(2\pi\sqrt{LC})$**

- **Less commonly used, because of high cost of transformer and size**



# Chapter 2. Semiconductor Devices (Cont.)

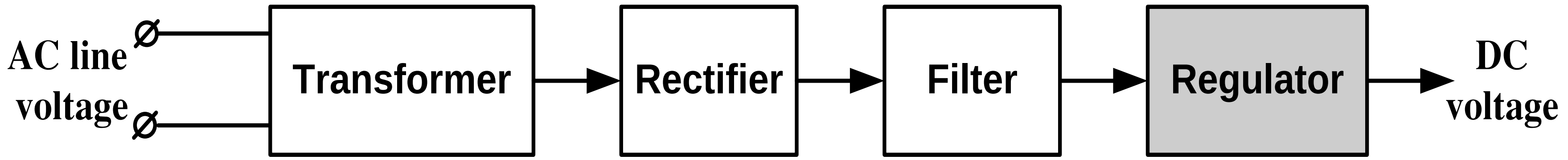
2.1. PN Junction - Diode and application

2.2. Bipolar Junction Transistor (BJT) and applications

2.3. Operational amplifier (OPAM) and applications

**2.4. Voltage regulation**

## 2.4.1. Basic concepts




- **Definition:** Line regulation, Load regulation

✓ **Line regulation:** $(\Delta U_{out} - \Delta U_{in})/\Delta U_{in}(100\%)$

✓ **Load regulation:** $(\Delta U_{NL} - \Delta U_{FL})/\Delta U_{FL}(100\%)$, where NL = No load, FL = Full load

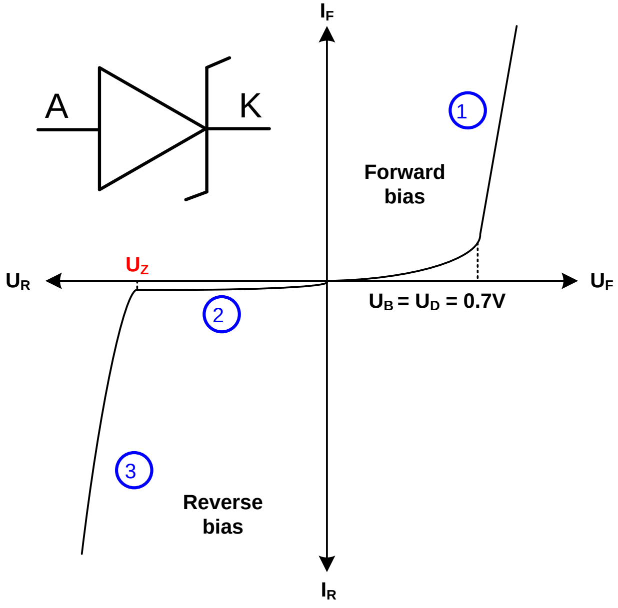
- **Classification:**

➢ **Use of a control element:** Zener diode, series regulators, parallel regulators (shunt), switching regulators

➢ **Linear output** (Zener diode, series regulators, parallel regulators (shunt)), **non-linear output** (switching regulators)

➢ **Integrated circuit (IC)** regulators

a) Zener diode




- **Key feature:** 1) designed to operate in breakdown region 3;

  2) Ability to keep reserve voltage across its terminal constant;

- **If Zener diode forward biased**: Operate as a normal diode.
- **Zener breakdown characteristic**:

➢ Breakdown effect begins at $I_{ZK}$, where $I_Z$ start increasing rapidly, internal impedance begin decreasing

➢ Down to bottom of knees, breakdown $U_Z$ is almost a constant as $I_Z$ increasing

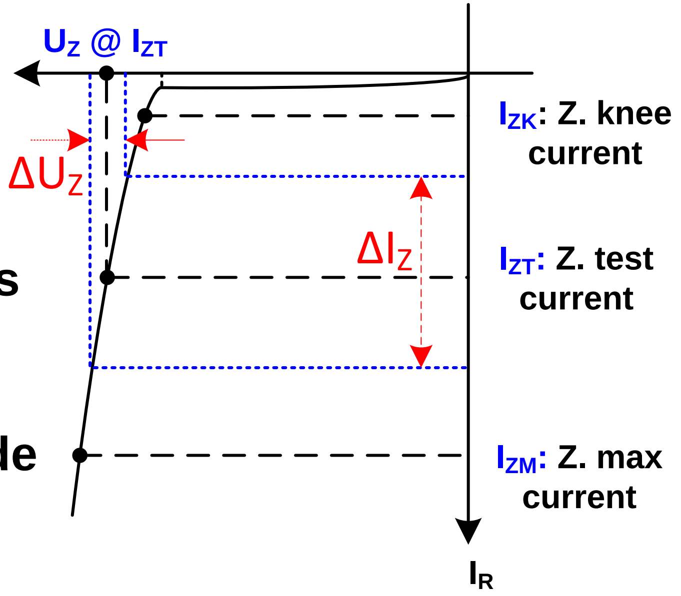
- **Zener diode operating at breakdown acts as a voltage regulator**: because it maintains a nearly constant voltage over a specific range of reverse current

➢ $I_Z$ should be maintained at $I_{ZK}$ (min value) to keep breakdown, o.w $U_Z$ decreases

➢ $I_Z$ should be less than $I_{ZM}$ (max value) to avoid damage

➢ Therefore $I_{ZK}$: nominal value of $I_Z$ typically specified on a dataset of Zener diode

➢ Zener impedance: $Z_Z = \Delta U_Z/\Delta I_Z$



**Example:** For a given Zener diode IN4736: $Z_T = 3.5\Omega$, $U_{ZT} = 6.8V$ at $I_{ZT} = 37mA$ and $I_{ZK} = 1mA$.

**What is $U_Z$ when $I_Z = 50mA$? When $I_Z = 25mA$?**

- $I_Z = 50mA$: $\Delta_{IZ} = 50 - 37 = 13mA \Rightarrow \Delta_{UZ} = \Delta_{IZ}R_Z = 13mA \times 3.5\Omega = +45.5mV \Rightarrow U_Z = U_{ZT} + \Delta_{UZ}$ ~ 6.85 V
- $I_Z = 25mA$: $\Delta_{IZ} = 25 - 37 = -12mA \Rightarrow \Delta_{UZ} = \Delta_{IZ}R_Z = -12mA \times 3.5\Omega = -42\ mV \Rightarrow U_Z = U_{ZT} + \Delta_{UZ}$ ~ 6.76 V

**Example:** For a voltage regulator using Zener diode: $U_Z = 12.7V$, $R_1 = 390\ \Omega$, $R_E = 12\ k\Omega$, $R_L = 240\ \Omega$, $\beta = 50$, $U_{BW} = 0.7\ V$. Rectified output a) $U_{in} = 21\ V$ when $I_L = 0$ (no load) and b) $U_{in} = 20\ V$ when $I_L = 50mA$ (with load).

**What is currents at E, B, C and $I_Z$ without and with load?**

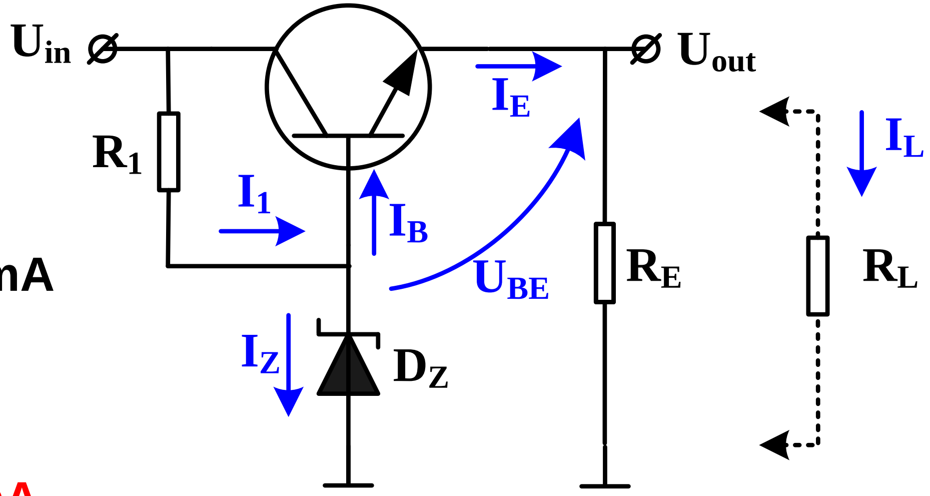
- **Without load:**

➢ $U_{out} = U_{RE} = U_Z - U_{BE} = 12.7V - 0.7V = 12V \Rightarrow I_E = U_{RE}/R_E = 12V/12k\Omega = 1mA \Rightarrow I_B = I_E/(1+\beta) \sim 20\mu A$; $I_C = \beta I_B \sim I_E$

➢ $U_{R1} = U_{in} - U_Z = 21V - 12.7V = 8.3V \Rightarrow I_1 = U_{R1}/R_1 = 8.3V/390\ \Omega \sim 21.3mA$ $\Rightarrow I_Z = I_1 - I_B = 21.3mA - 20\ \mu A \sim 21.3mA$

- **With load:** $I_E = U_{out}/(R_E//R_L) \sim 20V/235\Omega = 51.1mA$

➢ In similar manner: $I_B = 1mA$; $I_C \sim I_E = 51.1\ mA$; $I_1 = 18.7mA$, $I_Z = 17.7mA$



## b) Series regulator: based on OPAM

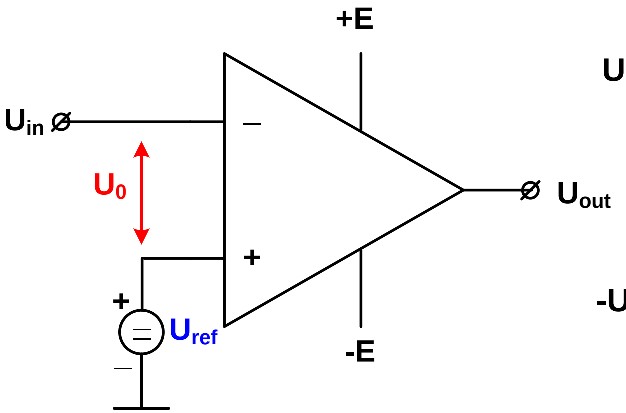
- **Comparator:** Inverse and non-inverse; operating in saturation mode, $U_{out} = \pm U_{max}$

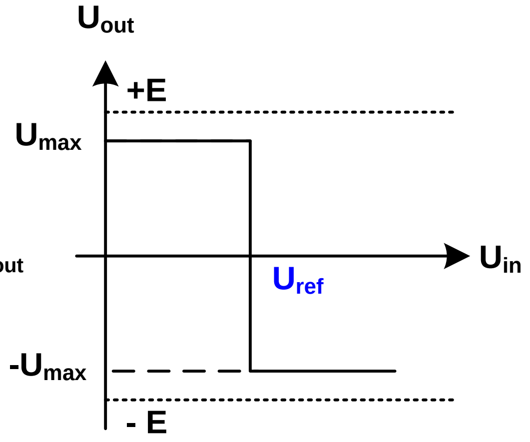
➢ **Inverse:** ( - ) input compared with $U_{ref}$ in (+) input

✓ If $U_0 = U_{ref} – U_{in} > 0$ ➔ $U_{in} < U_{ref}$ ➔ $U_{out}$ from + $U_{max}$ -> - $U_{max}$

✓ If $U_0 = U_{ref} – U_{in} < 0$ ➔ $U_{in} > U_{ref}$ ➔ $U_{out}$ from - $U_{max}$ -> + $U_{max}$

✓ Transfer characteristic: based on inverse amplifier



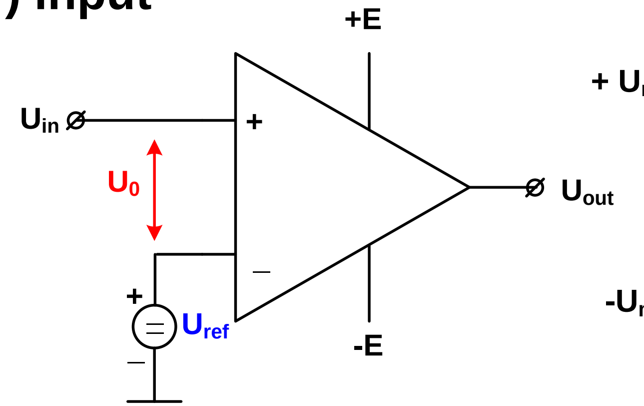



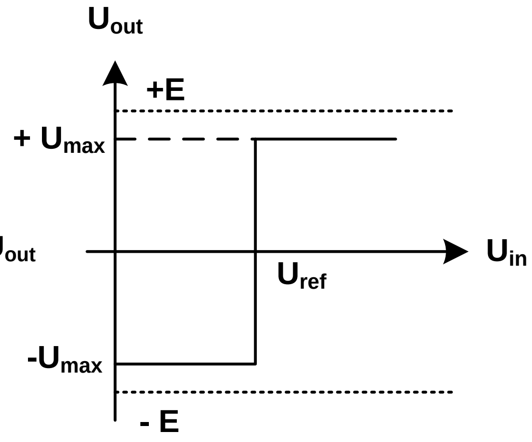

➢ **Non-Inverse:** Non-Inverse ( + ) input compared with $U_{ref}$ in (-) input

✓ If $U_0 = U_{in} – U_{ref} > 0$ ➔ $U_{in} > U_{ref}$ ➔ $U_{out}$ from - $U_{max}$ -> + $U_{max}$

✓ If $U_0 = U_{in} – U_{ref} < 0$ ➔ $U_{in} < U_{ref}$ ➔ $U_{out}$ from + $U_{max}$ -> - $U_{max}$

✓ Transfer characteristic: based on non-inverse amplifier



- **Schematic circuit:** Based on non-inverse comparator

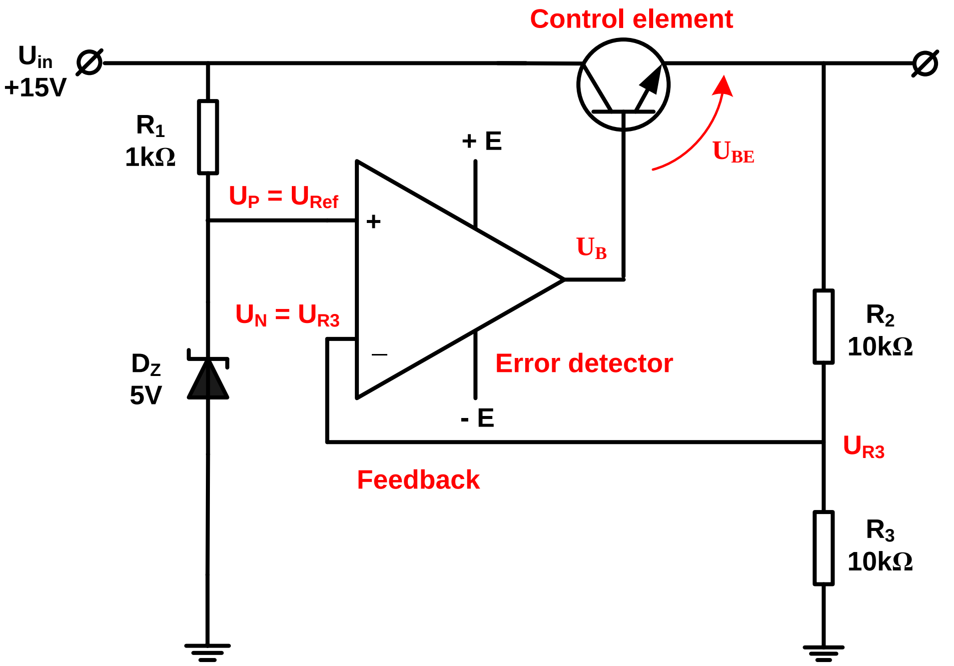
➢ Transitor as a control element switch connected in series with LOAD

➢ **Priciple:** Compared $U_{ref} = U_Z$ and $U_{R3} = U_{out}R_3/(R_2+R_3)$ fed back to N-input ➔ $U_{out} = U_{ref}(1+R_2/R_3)$ (neglect $U_{BE}$)

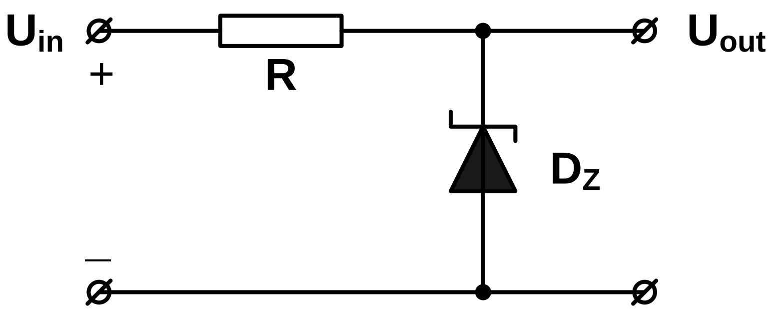
➢ If $U_0 = U_{ref} – U_{R3}$ zero-crossed, OPAM output $U_B$ opens transistor ➔ $U_{out}$ is adjusted accordingly to be const

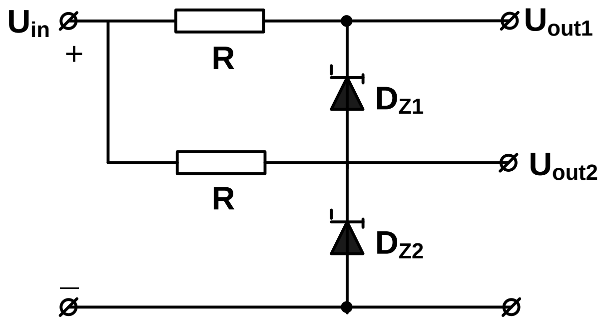
**Example:**

➢ $U_{ref} = U_z = 5V$ ➔ $U_{out} = U_z(1 + R_2/R_3) = 5V(1 + 10k/10k) = 10\ V$




**Quick test 13:**



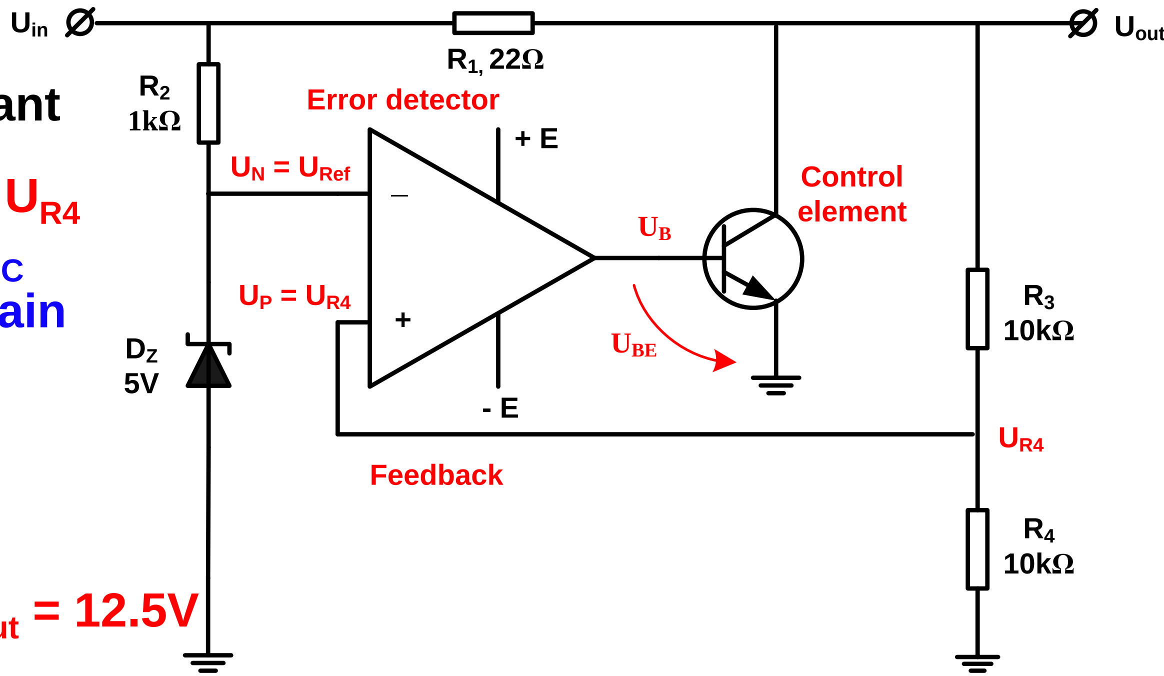




➢ $U_{out} = U_z$

➢ $U_{out2} = U_{z2}; U_{out1} = U_{z1} + U_{z1}$

c) Parallel regulator: based on OPAM (common name: SHUNT regulator)

- Transistor as a control element connected in parallel to the LOAD, and $R_1$ is series with LOAD
- Principle: Inverse comparator




➢ $r_{CE}$ and $R_1$ are voltage divider used to maintain $U_{out}$ constant

➢ If $U_{out}$ decreases/increases, sensed by $R_3$-$R_4$ ➔ $U_0 = U_{ref} – U_{R4}$ zero-crossed and $U_B$ decreased/increased ➔ $I_B$ and then $I_C$ decreased/increased ➔ $r_{CE}$ increased/decreased ➔ Maintain $U_{out}$ as a constant, with a voltage devider of $R_1$ and $r_{CE}$

Example: If max input $U_{in}$ = 12.5, what power rating for $R_1$?

➢ $U_{out}$ = 0 → $U_Z(1+R_3/R_4)$ = 0 → 10V, and in worse case $R_1$ is dissipated when short output or $U_{out}$ = 0 ➔ $U_{R1} = U_{in} – U_{out}$ = 12.5V

➢ Power rating: $P = UI = U_{R1}^2/R_1 = (12.5V)^2/22\Omega = 7.1$ W ➔ Select $R_1$ with power rating about > 10W for use

d) Switching regulator: based on OPAM

- **Principle:**

➢ More efficiency than linear types, because Transistor not always conducted

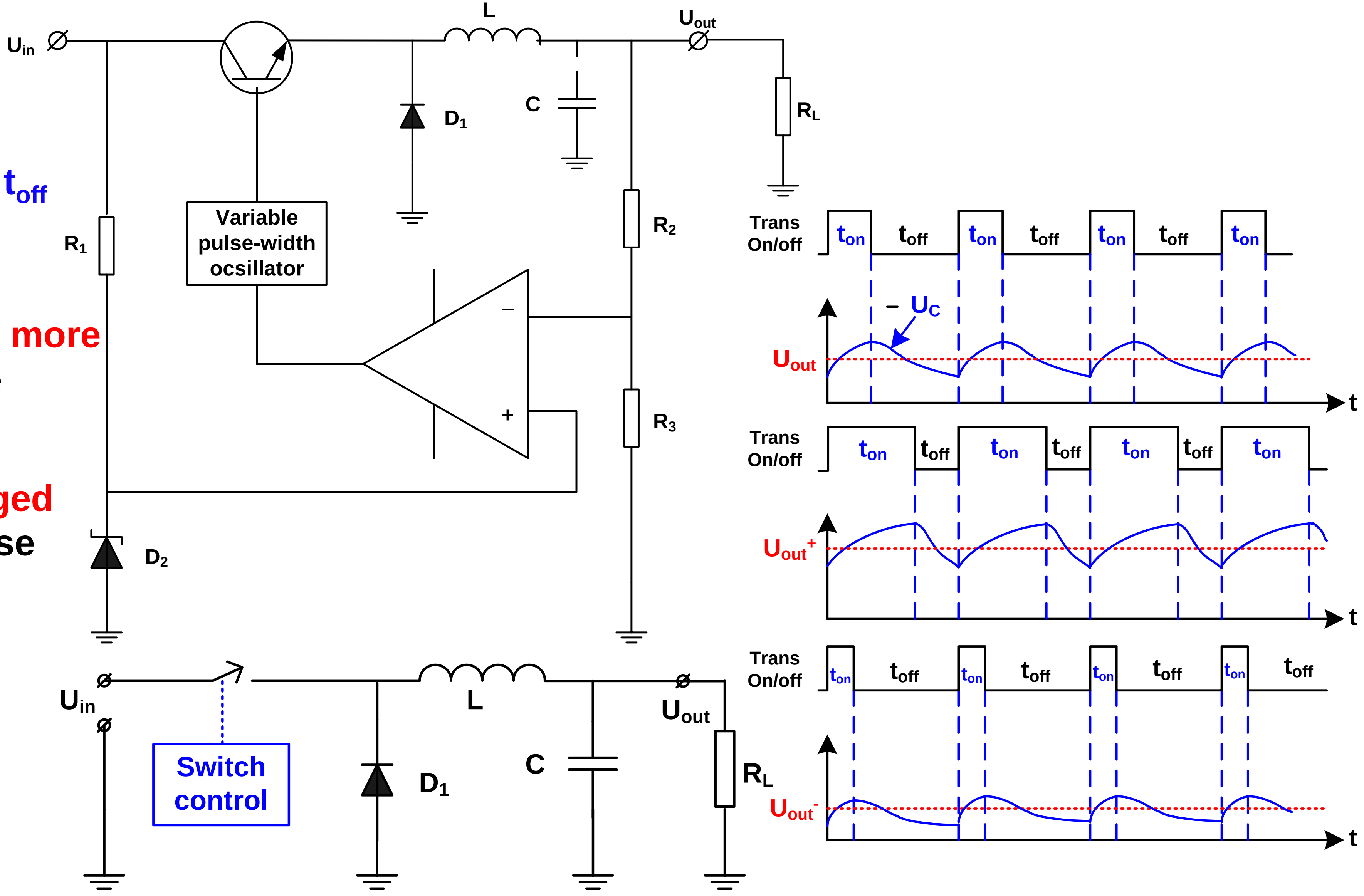
➢ More load current at low voltage than linear regulators, since the control transistor doesn't dissipate

- **Type:** step-down, step-up, inverter

## 1. Step-down regulator

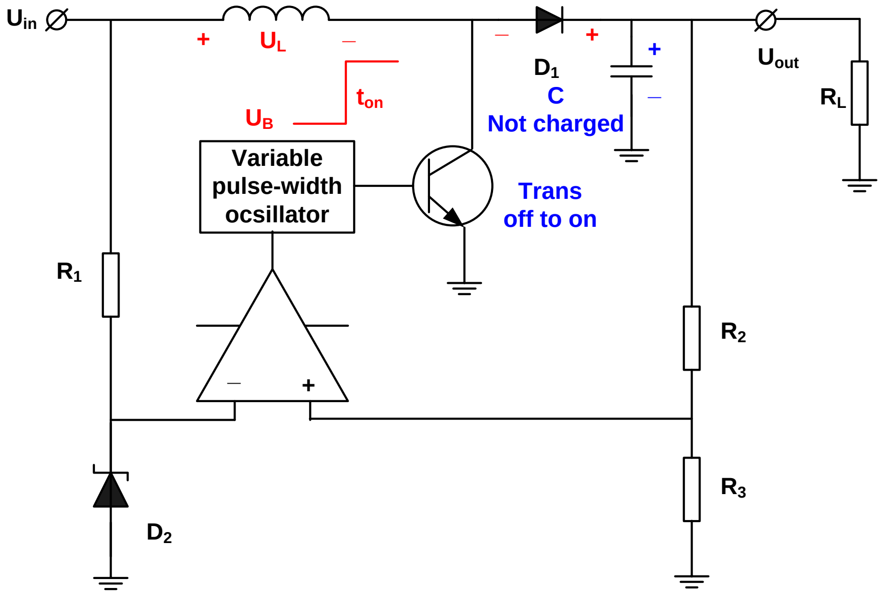
- ✓ Charge and discharge of C
- ✓ $U_{out} = (t_{on}/T)U_{in}$, where $T = t_{on} + t_{off}$
- ✓ $t_{on}/T$: duty cycle
- ✓ If $U_{out}\downarrow$ ➔ $t_{on}\uparrow$ ➔ C is charged more additionally to compensate the decrease ➔ $U_{out}\downarrow$
- ✓ If $U_{out}\uparrow$ ➔ $t_{on}\downarrow$ ➔ C is discharged enough inversely to the increase

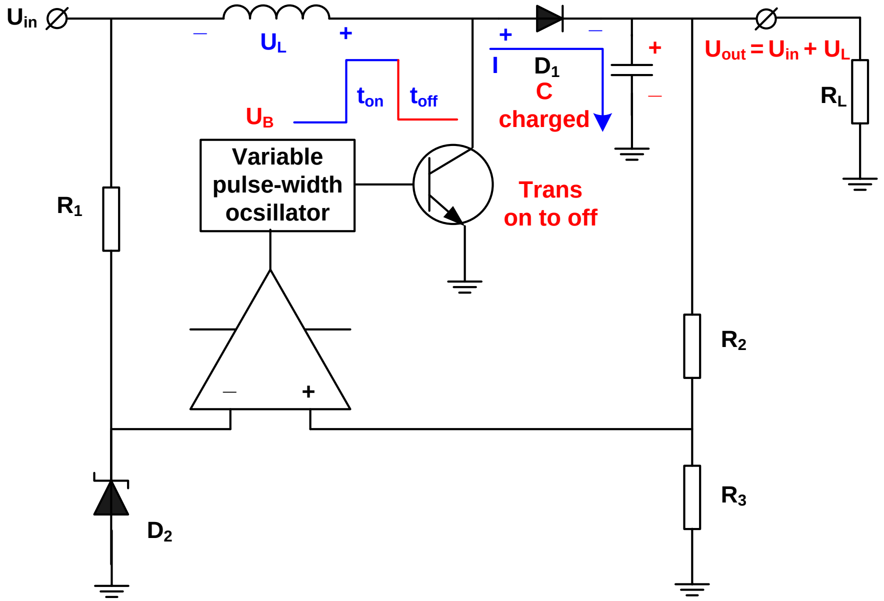
➔ $U_{out}\uparrow$



## 2. Step-up regulator

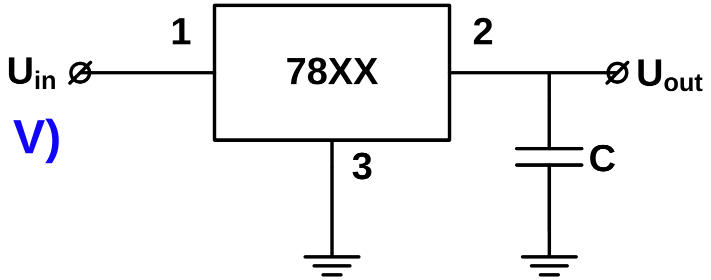
- ✓ When Transistor is on, $U_L$ jumps to $U_{in}$ (+ → -). During $t_{on}$, the induced voltage $U_L$ starts decreasing, $D_1$ is reverse biased, C discharged small amount to the load (C is not charged)
- ✓ When Transistor is off, $U_L$ changes polarity (- → +), $D_1$ if forward biased, and C is charged to $U_{in}$. During $t_{off}$ : $U_{out} = U_{in} + U_L$
- ✓ If $U_{out}$ ↑ ➔ $t_{on}$ ↓ ➔ decrease in the amount that C will charge
- ✓ If $U_{out}$ ↓ ➔ $t_{on}$ ↑ ➔ increase in the amount that C will discharge
- ✓ As the result: $U_{out}$ maintains constant value



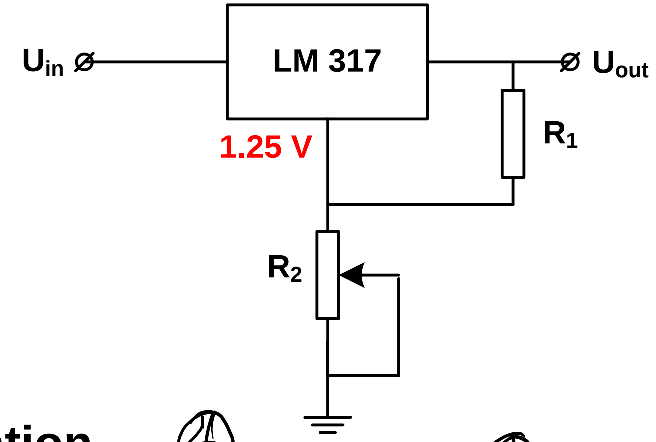

## 3. Voltage-inverter regulator: self-reading

e) Integrated circuit (IC) regulators

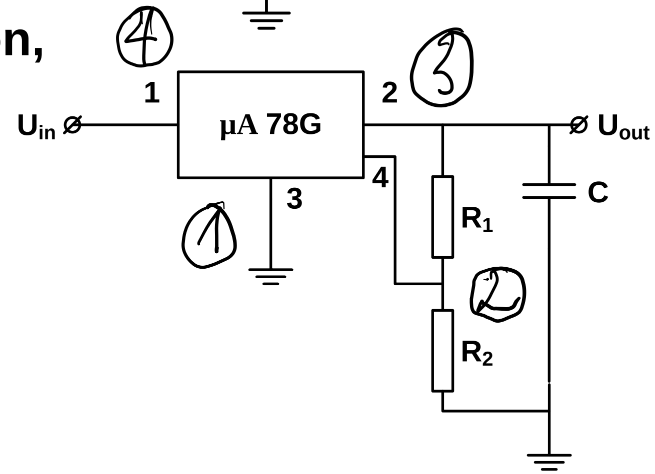



- **78XX:** XX = positive regulated voltage (+05, +06, +08, +09, +12, +15, +18, +24 V)
- **79XX:** XX = negative regulated voltage (-05, -06, -08, -09, -12, -15, -18, -24 V)
- **LM317:** precise $U_{out}$ = 1.25 V. R1-R2 voltage divider used for various $U_{out}$

  ➔ $U_{out} = 1.25\ V(1+ R_2/R_1)$




- **µA78G:** provide positive voltage output from +5 to +30 V
- **µA79G:** provide negative voltage output from -2.5 to -30 V
- **QUESTION:** Investigate applications of IC regulators (increase power dissipation, current limiting, )
- **Current regulators:** self-reading



## CHAPTER 2: SUMMARY

### 1. DIODE and applications

a. Forward bias, reverse bias, break down

b. Applications:

- Rectifiers: Half-wave, Full-wave, bridges, doubler
- Limiters: serial (upper, lower), parallel (upper, lower)

### 2. Transistors and applications

a. Basic equations, amplification mode, saturation mode, cut-off mode, basic amplifier schemes (EC, CC)

b. DC analysis: Q-point, DC load line, DC load

c. DC bias methods: based current, feedback current, emitter currents, DC equivalent (Thevenin's)

d. AC analysis: EC and CC

- AC equivalent model of transistor and amplifier
- Derivation of $K_u$, $K_i$, $K_P = K_u K_i$ , take note of  operation frequency range

d. Multistage amplifier: independent DC mode for a stage, $K_u = K_1 \ldots K_N$, C-coupled and direct coupled

## 3. OPAM and applications

**a. Linear and saturation mode of OPAM**

**b. Basic features: Transfer characteristic according to inverse and non-inverse inputs, $U_P = U_N$, $I_P = I_N = 0$**

**c. Applications: inverse and non-inverse amplifiers, summing and subtracting amplifiers, integrator and differentiators, function generators**

## 4. Oscillators

**e. Signal oscillators**

- **Oscillation conditions**
- **Based on RC feedback**
- **Based on use of OPAM and Transistors**
- **Signal frequency: resonance frequency**

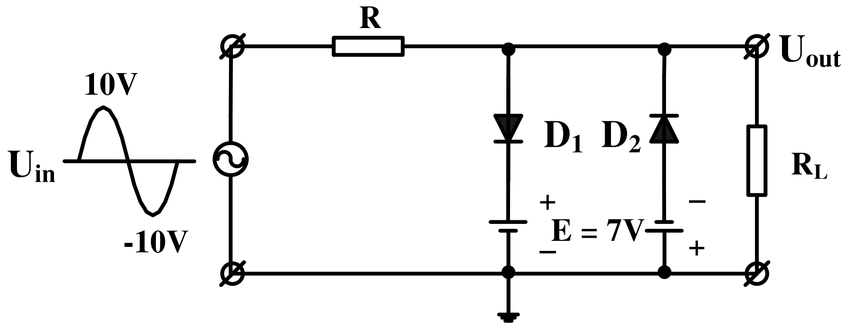
# Chapter 2. Semiconductor Devices (Cont.)

## 5. Voltage regulators

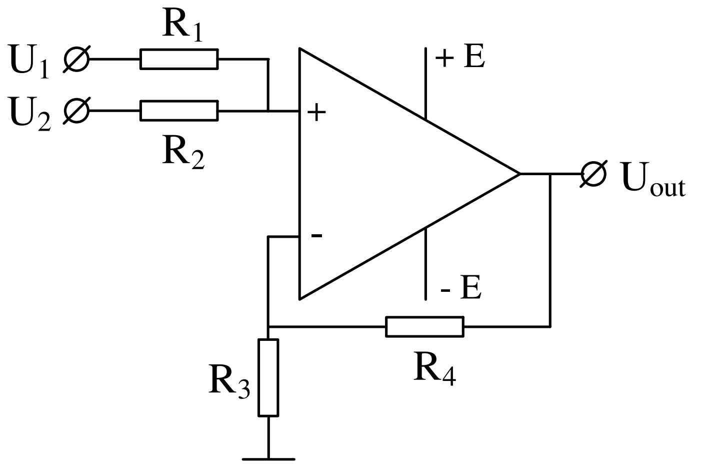
- **Zener diode: based on Zener effect**
- **Series: Control element in series with LOAD, based on non-inverse mechanism**
- **Parallel: Control element in parallel to LOAD, based on inverse mechanism**
- **Switching: non-linear compensation of output voltage, based on charge/discharge of C**
- **Integrated circuits (IC): 78XX, 79XX, LM317, uA78G, uA79G**

# Quick test Chapter 2

**Prob 1.** Given a circuit assuming that: R = 0Ω and $U_D$ = 0,7V.
a. State the function of the circuit and illustrate the output signal $U_{out}(t)$ and input signal $U_{in}(t)$ on the same coordinate system.
b. If the order of branches $D_1$-E and $D_2$-E are exchanged, is there any significant change in its function, and explain the reason?




**Prob 2.** Given a circuit, with saturated voltages of OPAM $\pm U_{max} = \pm 10V$.
a. State the function of the circuit and derive the equation for $U_{out}$ according to its parameters, assuming $R_1 = R_2$.
b. When $R_1 = R_2$ = 10KΩ, $U_1 = U_2$ = 1V. Determine the max value of R4/R3 so that the circuit keeps operating in a linear amplification.




**Prob 3.** Given a regulator circuit using Zener diode.
a. With $U_{in}$ = 12V, $U_{out}$ = 9V, test Zener current $I_{ZT}$ = 25 mA. Determine compensate resistor R.
b. With $U_{in}$ = 20V, $U_{out} = U_Z$ = 6V, max Zener current $I_{ZM}$ = 30mA, knees current $I_{ZK}$ = 0V, R=400Ω. Determine $R_t$ to work in regulation band.
c. If $U_{inNL}$= 12V without LOAD, and $U_{inL}$ = 10V with LOAD. Determine the voltage stability coefficient in %