

On the future of particle physics: Quality control

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I ABSTRACT

The upgrade of the ATLAS ITk strips detector for HL-LHC will use custom PCBs (powerboards) for on-module DC-DC conversion, HV switching, and monitoring. To ensure high reliability, quality control (QC) testing for the powerboards to be installed on ITk Strip barrel modules is necessary. This paper will present the QC procedure used for the powerboards. Before module assembly, each powerboard must pass QC tests, including thermal cycling, burn-in, and electrical tests of the low voltage (LV), high voltage (HV), and monitoring functions of the powerboard. The ATLAS group at LBNL developed a massive test crate that is able to perform electrical and thermal tests on 200 powerboards simultaneously. This test crate is crucial for the timely delivery of this component of the upgrade and is affixed with an inter-lock system to ensure the safety of powerboards in testing. The production procedure and QC test system has been tested with 500 powerboards during Pre-Production B Batches 4 and 5, and the system has been proven ready for production with the desired testing program, speed, safety, and cost. Unanticipated failures and abnormalities in powerboard test results are also presented.

II INTRODUCTION

ATLAS (A Toroidal LHC Apparatus) is a general-purpose detector at the LHC (Large Hadron Collider) that has been involved with fundamental discoveries in particle physics during the past few decades, including the detection of the Higgs boson in 2012. Sitting at an impressive 46m long, 25m in diameter, and 7000 tonnes, no particle detector has ever been larger in volume. It resides in a cavern 100m underground near the main CERN site in Switzerland. Particle beams accelerated by the LHC collide in the center of the ATLAS detector, breaking into new particles

that scatter in all directions. A series of detecting subsystem layers in the walls of ATLAS measure the momentum, energy, and path of the particles that hit it through a magnet system that bends the particle paths. Since the detector receives countless hits, it digests the particle data using a “trigger” system that identifies what events should be recorded. Data-acquisition (DAQ) and computing systems are then able to analyse the recorded collisions.¹

A major upgrade of the ATLAS detector is planned, with installation in the second half of the decade. The powerboards, shown in Figure 1, a component of the planned installation of the ATLAS ITk (Inner Tracker) Strip detector, are PCBs (printed circuit boards) built from a flexible polyamide core and loaded with SMDs and bare die components and chips. The heart of the powerboard is the bPOL12V buck converter, and a 500 nH air-core solenoid inductor is used, providing a switching frequency for DC-DC conversion at roughly 2 MHz. The bPOL12V is controlled and monitored by a custom AMAC chip (automatic monitor and control chip), which is powered by a linPOL12V linear regulator. The AMAC works with an HVMUX circuit based on a GaN FET device to control HV and measure current, and also controls and monitors the hybrids (flexible PCBs with front-end chips that read signals from the strips), including temperature and interlock monitoring². The PCB is shielded from the strong ATLAS magnetic field and electromagnetic induced noise transmitted to the sensor under the powerboard by a 1 mil thick aluminum shield box. LBNL is the lead institute in the design and production of the powerboards and will oversee the fabrication of a total of about 14,100 parts.³

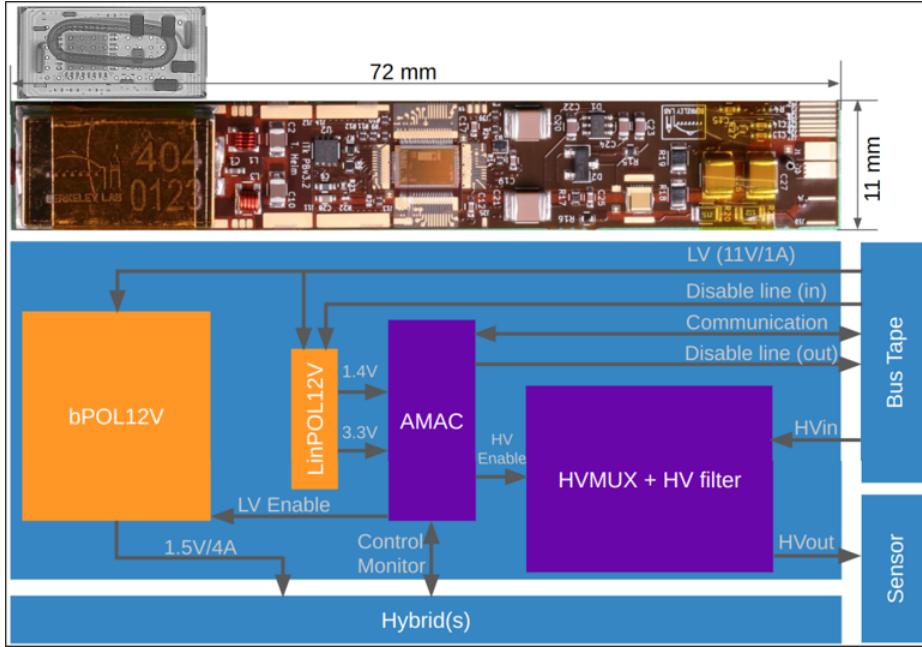


Figure 1: Top: a powerboard, with an X-ray image of the area under the shield box. Bottom: a simplified schematic diagram of the powerboard design

The ATLAS group at LBNL developed a massive test crate (Figure 2) that is able to perform electrical and thermal tests on 200 powerboards simultaneously. This test crate is crucial for the timely delivery of this component of the upgrade and is affixed with an interlock system to ensure the safety of powerboards in testing. Powerboards are produced and tested in flex array panels

containing 10 powerboards. After the powerboards are loaded with SMDs, they are loaded onto a carrier card for wirebonding. Following this, the powerboards will go through a series of QC (Quality Control) tests.



Figure 2: Massive test crate (active side)

III METHODS

A PROCEDURE

All powerboards go through the same QC procedure, detailed in Table I⁴. A majority of the procedure is managed through a custom GUI (Graphical User Interface).

B DATABASE REGISTRATION & UPLOADING

Database registration is done automatically via a script, which is constantly running. Once AmTech has filled in the information for a panel, the "Ready for DB register?" column can be

TABLE I: QC Operation Procedure

Database registration
Visual inspection
Load the crate. Turn on chiller, set to 20 °C
Electrical test (full) - warm
Upload test result
Cool down to -35 °C
Electrical test (full) - cold
Upload test result
Thermal cycle
Electrical test (full) - warm
Stage transition to “Thermal Cycle”
Upload test result
Burn-In
Electrical test (full) - warm
Stage transition to “Burn-In”
Upload test result
Cool down to -35 °C
Electrical test (full) - cold
Upload test result
Warm up to 20 °C and turn off chiller. Then unload the crate
Duration: appx. 60 hours of chiller on appx. 4.5 days of real time

changed from "No" to "Yes" and the registration script will be triggered. It may take a couple of hours before the script is finished.

Database uploading has two parts: stages and test results. To stage transition, the interactive GUI will allow you to input the powerboard's information and transition the stage. This should be done one at a time. To upload test results, the interactive GUI will allow you to do a similar procedure to stage transitioning, but for test result uploading; however, you can upload test results for multiple panels simultaneously. This will take around thirty minutes to complete.

C VISUAL INSPECTION

Powerboards start with a visual inspection, where high resolution pictures are taken of each board and inspected for missing/tombstoned components, missing/broken wirebonds, incomplete seams on the shield box, and solder splash on the bond pads. If a powerboard displays fundamental defects (e.g. missing/broken wirebonds), it is put to the side for repair and excluded from further testing. If a powerboards displays minor defects (e.g. solder splash on bond pads), it is noted and monitored during electrical tests.

D THERMAL CYCLING

After completing initial electrical tests, the powerboards are thermal cycled. During this process, the chiller temperatures is cycled between -35 °C and 40 °C three times. The cycles do not need to be performed consecutively, and each cycle takes roughly an hour and forty minutes to complete.

E BURN-IN

Load the DC-DC converter at 2 A for 24 hours without interruption. The crate should be set to 20 °C for the entire duration of the burn-in. It can be run overnight.

F ELECTRICAL TESTS

After visual inspection, thermal cycling, and burn-in, the boards undergo electrical tests at room temperature (20 °C) and/or cold temperature (-35 °C), which consist of powerboard functionality tests (e.g. LV and HV ON/OFF measurements and AMAC function) and characterization of LV, HV, and AMAC settings (e.g. scan of DC-DC converter efficiency/temperatures/currents at different loads). The powerboard functionality tests are compared to an acceptable range of values, detailed in Table II. The characterization graphs are compared to visual standards, displayed in Appendix A; any breaks in continuity of the graphed data can constitute failure, along with uncharacteristically low/high data values. A set of ten powerboards takes approximately four hours to fully test.

Once the initial electrical tests are completed, the boards will go through thermal cycling, where the temperature of the test crate is cycled between -35 °C and 40 °C (as measured by the temperature sensors on the powerboards) three times, and will complete another round of electrical testing upon thermal cycling completion. Finally, the boards will withstand a soak test, where the DC-DC converter is loaded at 2 A for 24 continuous hours at 20 °C, and received a final round of electrical testing afterwards. All QC steps are integrated in an all-in-one custom web-based GUI, which communicates with SoC (**System-on-Chip**) boards for electrical testing, with the chiller for thermal cycling, and with the ITk production database for uploading data, as well as monitors tables and graphs for testing results and crate status.

IV RESULTS & DISCUSSION

500 boards were tested in Pre-Production B. Nine of these boards failed, resulting in a 97.4% yield. All other boards passed with no issue. Typical failures include AMAC communication issues, unexpected DC-DC efficiencies at certain loads/temperatures, failure of other sensors (e.g. temperature) on the board. 20 boards skipped the burn-in stage due to low Novec coolant supply. These yields are within the anticipated range for Pre-Production B.

TABLE II: Basic Functionality Test Parameters

Test Name	Acceptable Warm Range	Acceptable Cold Range
BER	1.0	1.0
PADID	0	0
linPOLV [V] OFF	< 0.25	< 0.25
linPOLV [V] ON	> 1.3	> 1.3
DC/DC Out [V] OFF	< 0.25	< 0.25
DC/DC Out [V] ON	1.4 – 1.65	1.4 – 1.65
Efficiency	> 0.6	> 0.6
HV In Current [A] OFF	< HV In Current [A] ON - 0.8×10^{-3}	< HV In Current [A] ON - 0.8×10^{-3}
HV In Current [A] ON	> 0.8×10^{-3} + HV In Current [A] OFF	> 0.8×10^{-3} + HV In Current [A] OFF
HV Out Current [A] OFF	< 2×10^{-6}	< 2×10^{-6}
HV Out Current [A] ON	> 0.8×10^{-3}	> 0.8×10^{-3}
HVret [counts] OFF	< 200	< 200
HVret [counts] ON	> 300	> 300
OFout [V] OFF	-0.01 – 0.01	-0.01 – 0.01
OFout [V] ON	1.0 – 1.5	1.0 – 1.5
CALx [V] OFF	-0.1 – 0.1	-0.1 – 0.1
CALx [V] ON	0.75 – 1.0	0.75 – 1.0
CALy [V] OFF	-0.1 – 0.1	-0.1 – 0.1
CALy [V] ON	0.75 – 1.0	0.75 – 1.0
Shuntx [V] OFF	0.1 – 0.3	0.1 – 0.3
Shuntx [V] ON	0.95 – 1.2	0.95 – 1.2
Shunty [V] OFF	0.1 – 0.3	0.1 – 0.3
Shunty [V] ON	0.95 – 1.2	0.95 – 1.2
LDx0EN [V] OFF	-0.01 – 0.01	-0.01 – 0.01
LDx0EN [V] ON	1.0 – 1.5	1.0 – 1.5
LDx1EN [V] OFF	-0.01 – 0.01	-0.01 – 0.01
LDx1EN [V] ON	1.0 – 1.5	1.0 – 1.5
LDx2EN [V] OFF	-0.01 – 0.01	-0.01 – 0.01
LDx2EN [V] ON	1.0 – 1.5	1.0 – 1.5
LDy0EN [V] OFF	-0.01 – 0.01	-0.01 – 0.01
LDy0EN [V] ON	1.0 – 1.5	1.0 – 1.5
LDy1EN [V] OFF	-0.01 – 0.01	-0.01 – 0.01
LDy1EN [V] ON	1.0 – 1.5	1.0 – 1.5
LDy2EN [V] OFF	-0.01 – 0.01	-0.01 – 0.01
LDy2EN [V] ON	1.0 – 1.5	1.0 – 1.5
-13%	-12.3% – -14.3%	-12.3% – -14.3%
-6%	-5.67% – -7.67%	-5.67% – -7.67%
6%	5.67% – 7.67%	5.67% – 7.67%
NTCx [cnt]	600 – 850	550 – 850
NTCy [cnt]	600 – 850	550 – 850
NTCpb [cnt]	600 – 1000	500 – 1000
CTAT [cnt]	200 – 600	200 – 600
PTAT [cnt]	500 – 900	500 – 900
	6	

A DC-DC EFFICIENCY DROP-OFF AT 1 A DURING COLD ELECTRICAL TESTS (< -30 °C)

Three boards exhibited low efficiencies after 1 A at cold temperatures, causing them to fail. Figure 3 shows a graph of the DC-DC efficiency (in units of %) versus the output current (in units of A). The blue line is the efficiency at room temperature, and the orange line is the efficiency at cold temperature. The key feature is that, while the efficiency at higher temperatures is slightly lower than the efficiency at lower temperatures, the two lines are similar in shape, with no obvious discontinuities. Figure 4 shows the same graph, but from a board that failed due to exhibiting low efficiencies after 1 A at cold temperatures.

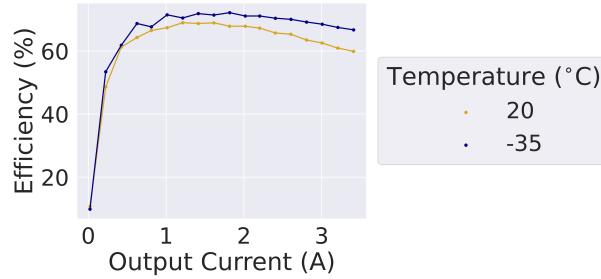


Figure 3: DC-DC efficiency [%] vs. IOUT [A] for a normal board

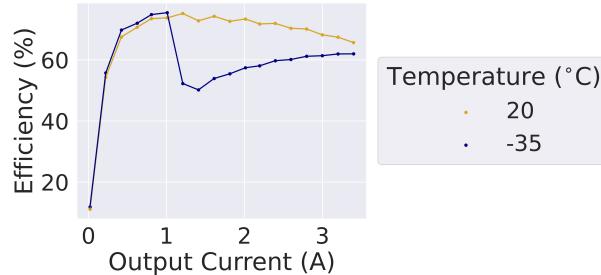


Figure 4: DC-DC efficiency [%] vs. IOUT [A] for an abnormal board

After analyzing the input current and output voltage with respect to output current and temperature, it is hypothesized that the efficiency drop is caused by abnormal behaviour in the input current starting at 1 A. Figure 5 demonstrates what a graph of input current vs. temperature vs. output current should look like, and Figure 6 shows the same graph, but from a board that failed due to exhibiting low efficiencies after 1 A at cold temperatures.

The DC-DC efficiency measured during the QC procedure is derived from the equation

$$EFF = \frac{VOUT \times IOUT}{VIN \times (IIN - IIN_{OFFSET})},$$

where EFF is the DC-DC efficiency, $VOUT$ is the output voltage, $IOUT$ is the output current, VIN is the input voltage, IIN is the input current, and IIN_{OFFSET} is the input current offset. Since Figure 6 shows the input current to increase more than Figure 5 at low temperatures, this increase in input current would cause the DC-DC efficiency to decrease. Additionally, abnormal behaviour in the

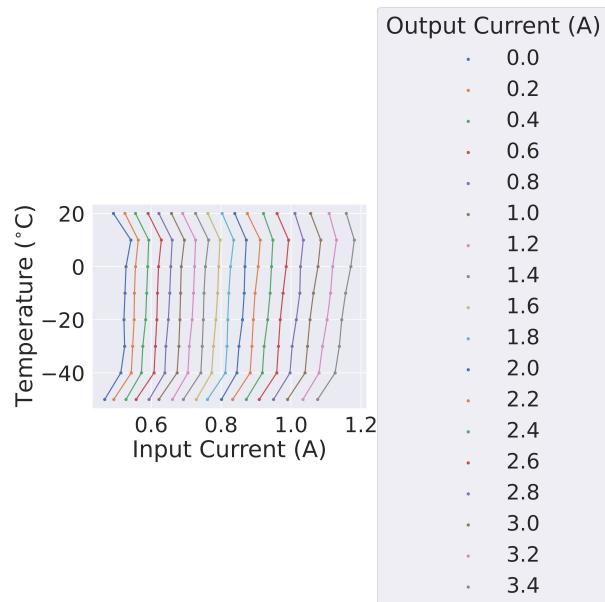


Figure 5: IIN [A] vs. Temperature [°C] vs. IOUT [A] for a normal board

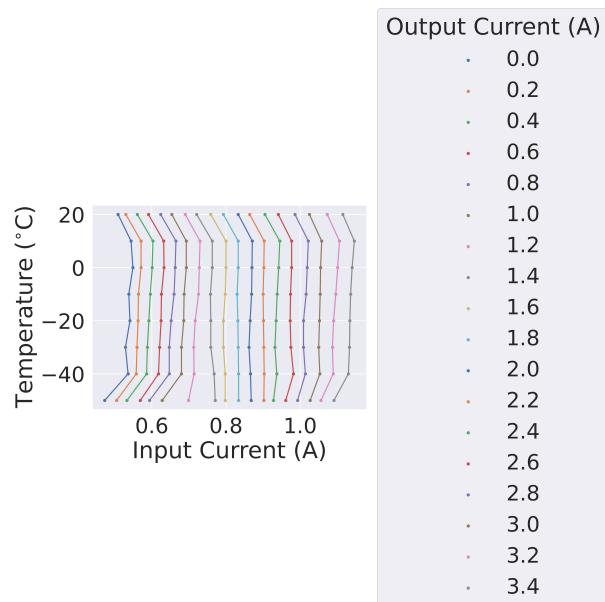


Figure 6: IIN [A] vs. Temperature [°C] vs. IOUT [A] for an abnormal board

output voltage was noted starting at 1 A, but not in a way significant to the efficiency calculation. These observations have since been communicated to the chip manufacturers.

B DISCONTINUITY AT 750 COUNTS IN AM RESPONSE GRAPHS DURING COLD ELECTRICAL TESTS (< -30 °C)

A significant number of boards exhibit discontinuity around 750 counts on the AM Response graphs during cold electrical tests. This is due to a technology transition in the AMAC chip, and was present in the prior version of the chip (AMACv2) but is much better in AMACstar documentation. This abnormality does not result in a QC failure. Since it was a persistent abnormality, the two types of discontinuity were documented during the QC procedure: "jump" and "stuck".

All boards with accessible data were analysed, which accounts for most of Pre-Production B, but not all. Of the 348 boards with accessible data, 171 (49%) has abnormalities in AM Response graphs during cold electrical tests (< -30 °C); in order for a board to qualify for this class of abnormality, it must exhibit continuous AM Response graphs during warm electrical tests. All electrical tests examined occurred after the burn-in completed.

B.1 "Stuck"

Of the 348 boards examined, 42 (12%) get "stuck" at 750 counts. Figure 7 shows the AM Response graph – the calibration of ADCs (Analog-to-Digital Converters) in the AMAC chip by injecting a known voltage (x-axis) and reading out ADC counts (y-axis) – during the warm and cold electrical tests for one of the "stuck" boards. The graph should be linear and continuous, in agreement with Appendix A.

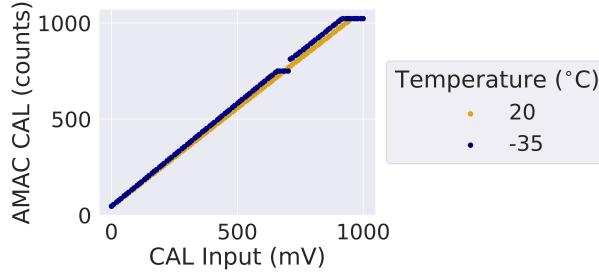


Figure 7: The AM Response graph from a "stuck" board

Two conditions had to be met for a board to qualify as "stuck":

1. Two or more consecutive measurements of 750 counts needed to be measured during the AM Response
2. This behaviour must not be present during warm electrical tests

B.2 "Jump"

Of the 306 boards examined (see below conditions for 24 excluded boards), 129 (42 %) "jump" over 750 counts. Figure 8 shows the AM Response graph during the warm and cold electrical tests

for one of the "jump" boards.

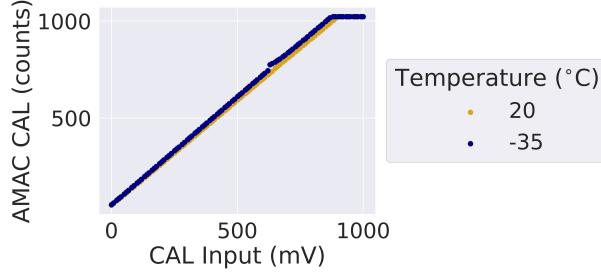


Figure 8: The AM Response graph from a "jump" board

Five conditions had to be met for a board to qualify as "jump":

1. Not a board previously flagged as getting "stuck" (excluding the 42 "stuck" boards)
2. The step between the n^{th} and $(n - 1)^{\text{th}}$ AMAC CAL value must be greater than double the step between the $(n-1)^{\text{th}}$ and $(n-2)^{\text{th}}$ AMAC CAL value
3. The $(n-2)^{\text{th}}$ AMAC CAL value must be greater than 750
4. The n^{th} AMAC CAL value must be less than 750
5. This behaviour must not be present during warm electrical tests

Condition 2 has the factor of two ("double") determined qualitatively, by visually examining what boards were being marked as "jump" and ensuring none of them exhibited an expected level of discontinuity in the AM Response graph.

V CONCLUSIONS

Pre-production has displayed a handful of concerns in the QC procedure, but as the ITk Strips team works to commission a new massive test crate, these issues are considered in design decisions and implementation. Additionally, an open line of communication exists between the AMAC chip designs and the ITk Strips team, and these functionality inquiries about the AMAC will help design the next chip following AMACstar.

With the confidence that the electronics of the powerboards can be safely tested en masse, the production of the replacement of the ATLAS Inner Tracker detector (ITk) can continue as planned. With Pre-Production concluding and Production looming on the horizon, the hard work of countless career scientists will be seen through in the next few months. Looking forward to the latter half of this decade, the HL-LHC upgrade will mark a new horizon for particle physics experimentation, and highlight the work of scientists across the globe to probe beyond the Standard Model.

VI ACKNOWLEDGEMENTS

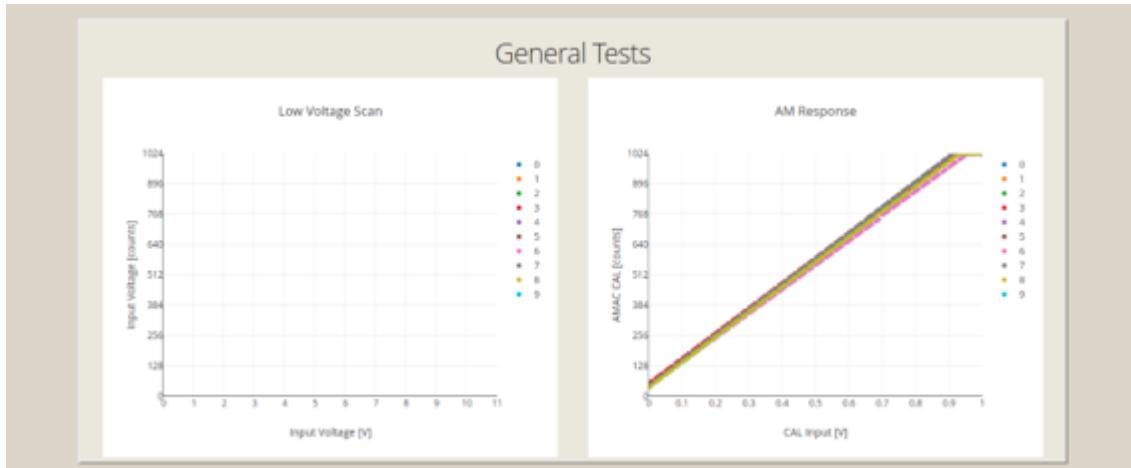
Astronomical thanks are owed to Timon Heim and Zhicai Zhang – along with the rest of the ATLAS ITk Strips team – for fostering an incredibly constructive place to experiment and grow, and for allowing me to harass them around the clock.

Thank you to my family, friends, instructors, and partner. Your support and love does not go unnoticed.

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VII APPENDIX

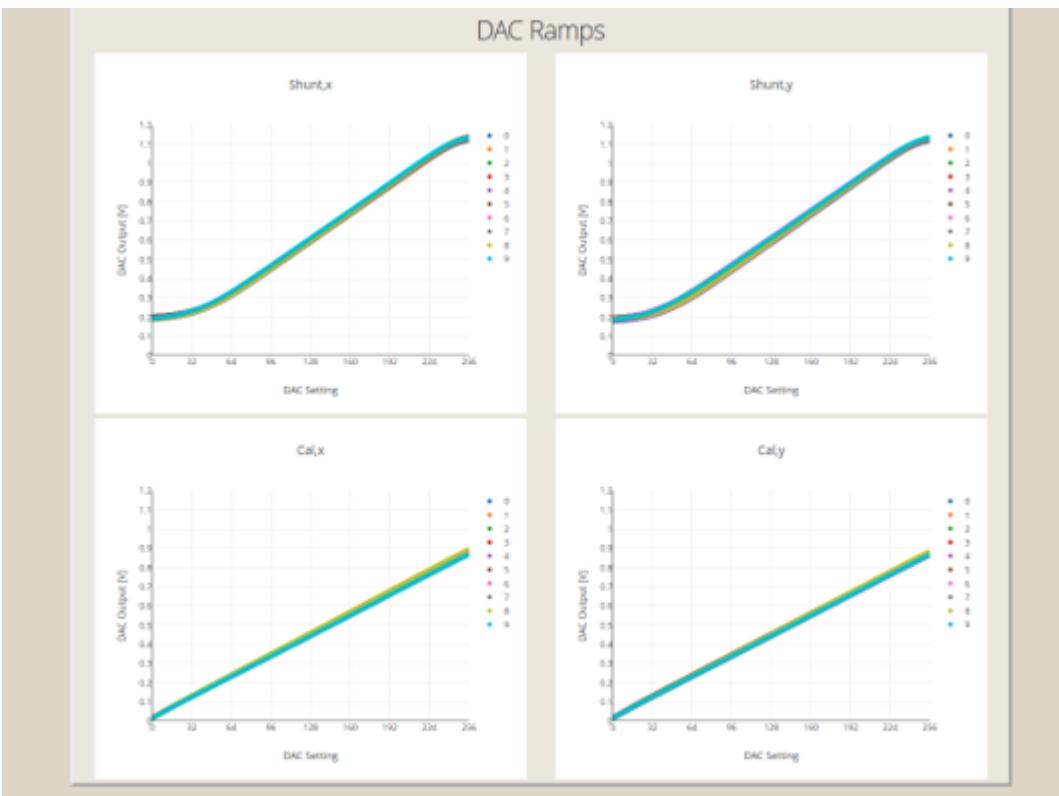
A CHARACTERIZATION GRAPHS

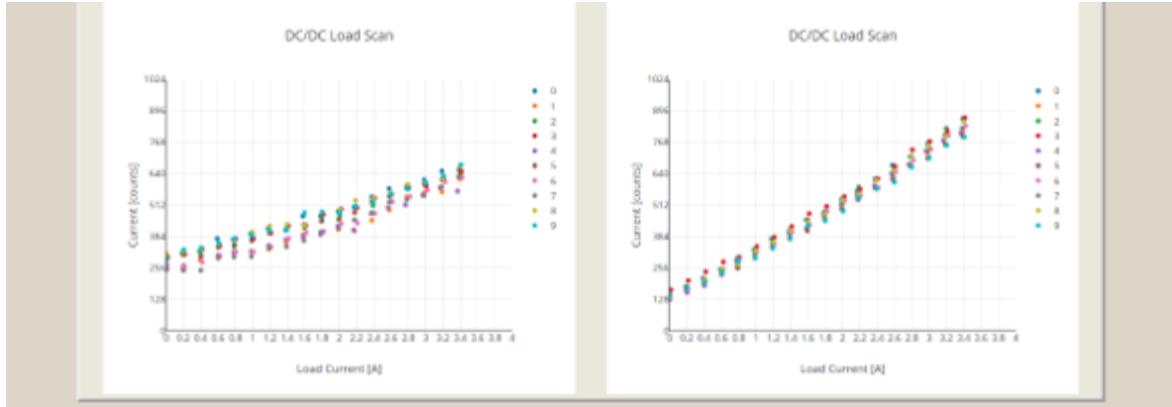


DC/DC Tests



DAC Ramps





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