Introduction to Digital Systems (21L)

ELab4: Static Random Access Memory (SRAM)

Please do not edit this report in Teams Files, download it locally on your computer.

Name: Student Number: Date:

Questions (0.6 pts)

Please answer these questions as shortly as possible (preferably one sentence)

1. What happens to the outputs of set/reset flip-flop (built of NAND gates) when both inputs are in the low state? **(0.1p)**
   Ans:
   a. Why? **(0.1p)**
   Ans:
2. What is the difference between a D-type latch and a D-type flip-flop? **(0.2p)**
   Ans:
3. Please fill all the remaining cells in Table 1. **(0.2p)**

Table 1. Functional description of typical SRAM (basing on Samsung KM62256C SRAM datasheet).
L – low state, H – high state, X – don't care, High-Z – high impedance state

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O Pin	Power
			Chip deselected		Standby
L	H	H			
				Data in	Active
			Read		

Falstad1. SRAM and tri-state buffer (1 pt + 0.7 bonus)

Please fill the underlined spaces.

To write digits 0-9 in SRAM I need _____ bits of data.

My Student Number has _____ digits, so I need _____ address bits to store its digits in SRAM.

The memory content is shown in Table 2.

Table 2. My Student Number and the corresponding digits stored under specified addresses (fill as many columns as you need).

My Student number	**SRAM address**	0	1	2	3	…	…	…	…	…
	SRAM data									

Falstad2. SRAM (read-only) and multiplex display

In Figure 1 I present my decoded message from task Falstad2.

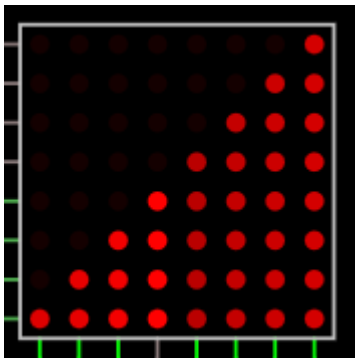

Figure 1. My decoded message visible on the LED array. [please edit that (delete this example picture)]

I declare that this piece of work which is the basis for recognition of achieving learning outcomes in the Introduction to Digital Systems course was completed on my own.