Introduction to Digital Systems (21L)

ELab4: Static Random Access Memory (SRAM)

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Questions (0.6 pts)

Please answer these questions as shortly as possible (preferably one sentence)

1. What happens to the outputs of set/reset flip-flop (built of NAND gates) when both inputs are in the low state? **(0.1p)**
   Ans: Both outputs will be in high state.
   a. Why? **(0.1p)**
      Ans: Because both AND gates will give 0 as outputs and inverted it will be 1, which means high state.
2. What is the difference between a D-type latch and a D-type flip-flop? **(0.2p)**
   Ans: D-type latch saves data when initially LE signal is on, while D-type flip-flop saves data when CLK signal is on after DATA signal is on
3. Please fill all the remaining cells in Table 1. **(0.2p)**

Table 1. Functional description of typical SRAM (basing on Samsung KM62256C SRAM datasheet). L – low state, H – high state, X – don't care, High-Z – high impedance state

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O Pin	Power
H	X	X	Chip deselected	High-Z	Standby
L	H	H	Output disabled	High-Z	Active
L	X	L	Write	Data in	Active
L	L	H	Read	Data out	Active

Falstad1. SRAM and tri-state buffer (1 pt + 0.7 bonus)

Please fill the underlined spaces.

To write digits 0-9 in SRAM I need 4 bits of data.

My Student Number has 6 digits, so I need 3 address bits to store its digits in SRAM.

The memory content is shown in Table 2.

Table 2. My Student Number and the corresponding digits stored under specified addresses.

My Student number	**SRAM address**	0	1	2	3	4	5	…	…	…
317304	**SRAM data**	4	0	3	7	1	3			

Falstad2. SRAM (read-only) and multiplex display

In Figure 1 I present my decoded message from task Falstad2.

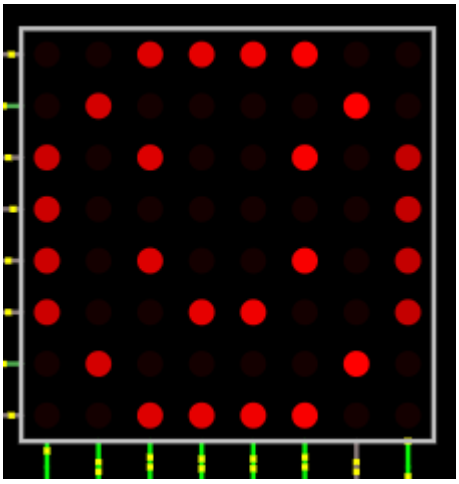

Figure 1. My decoded message visible on the LED array.

I declare that this piece of work which is the basis for recognition of achieving learning outcomes in the Introduction to Digital Systems course was completed on my own.