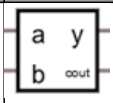
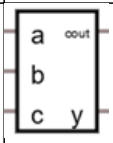
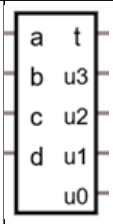
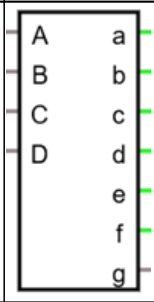
Introduction to Digital Systems, ELab2: 2-bit adder

All the files should be sent separately (not zipped) via Teams Assignments
Each exercise has its own assignment
Do not forget to click button "Turn in" to send files
Deadline 31.03.2021
Attachments that do not meet the requirements will not be accepted
We hope this information are consistent with those in movies, however, if any differences, this sheet is more valid

Content	
Combinational Logic pts 1-4	https://www.youtube.com/playlist?list=PL_WyEcCQBujS482G2jrlsCtQzVl-m7m09
Presentation [pptx]	on Teams
Presentation [pdf]	on Teams
Falstad Simulator	https://www.falstad.com/circuit/circuitjs.html
Falstad Simulator - how to start	https://www.youtube.com/playlist?list=PL_WyEcCQBujQmNXN6E-aQBW7M2Qhpue-2

Write your questions concerning the topic of Cominational Logic on YouTube as a comment. Add time stamp (e.g. 12:04 blah blah?)
Q&A 19.03.2021, 16:15 on Teams

task	program	what	explanation	name of file	subcircuit name	subcircuit diagram	pts
1	falstad	high-level circuit	we do it together	[lastname]_[index]_**1_HL**.circuitjs.txt			0,5
2	falstad	half adder	we do it together	[lastname]_[index]_**2_HA**.circuitjs.txt	my_ha		0,5
3	falstad	full adder	we do it together	[lastname]_[index]_**3_FA**.circuitjs.txt	my_fa		0,5
4	falstad	high-level circuit with your adders	we do it together	[lastname]_[index]_**4_HL**.circuitjs.txt			0,5
5	falstad	bin2bcd decoder	I did boolean functions and showed how to design 2 outputs with gates - rest for you, please finish subcircuit	[lastname]_[index]_**5_bin2bcd**. circuitjs.txt	my_bin2bcd		2
6	falstad	high-level circuit with your adders and bin2bcd decoder	**open** "[lastname]_[index]_**4_HL**. circuitjs.txt", save **a copy** with the new name "[lastname]_[index]_**6_HL**. circuitjs.txt", put here subcircuits from task 5 and second display	[lastname]_[index]_**6_HL**.circuitjs.txt			0,5
7	**paper & photos**	7 segment LED display driver	I did 4 diodes, you the 3 remaining ones - **c, e, f**: [truth table (0.2) + minimization (Karnaugh map; 0.8)] x 3 diodes	[lastname]_[index]_**7_a**.jpg [lastname]_[index]_**7_b**.jpg (example name convention for two pictures)			3
8	falstad	7 segment LED display driver	Please project the subcircuit of 7-segmend LED display driver. 0,5 pt * 7 + 0,5 pt for subcircuit	[lastname]_[index]_8_disp.circuitjs.txt	my_disp		4
9	falstad	high-level circuit with all your subcircuits	**open** "[lastname]_[index]_**6_HL**. circuitjs.txt", save **a copy** with the new name "[lastname]_[index]_**9_HL**. circuitjs.txt", put here subcircuit from task 7 for both displays	[lastname]_[index]_9_HL.circuitjs.txt			0,5

TOTAL 12

		EXTRA:	**open** "[lastname]_[index]_**1_HL**.circuitjs.txt", save **a copy** with the new name "[lastname]_[index]_**E_HL**.circuitjs.txt"				
E1	falstad	real input	one of input should be done with bi-stable switch and LED indicator	[lastname]_[index]_E_HL.circuitjs.txt			0,5
E2		real display	one of the displays should be used as Edit\Diodes\Common Cathode				1,5
						EXTRA TOTAL	2

FAQ

Q Why do I have to design so many high level circuits (tasks 1, 4, 6, 9)????

A You only modify it and save as - not much work. This is for you to have backups and when something goes wrong - you have last step to come back to. And it will be easier for us to check your workflow!

Q I can't make a subcircuit. Why?

A The problem can be caused by direct connection between input and output - Falstad Simulator doesn't like it. Place two inverters between input and output.

Q (4-bit bin2bcd decoder) is t=a(b+c) more optimal? And u2=b(sth)?

A yes