F2837xD Peripheral Driver Library 2.00.00.02

USER'S GUIDE

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Revision Information

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1 Introduction

The F2837xD Peripheral Driver Library is a set of drivers for accessing the peripherals found on the F2837xD microcontrollers. While they are not drivers in the pure operating system sense (that is, they do not have a common interface and do not connect into a global device driver infrastructure), they do provide a software layer to facilitate a slightly higher level of programming than direct register accesses.

The capabilities and organization of the drivers are governed by the following design goals:

- They are written entirely in C except where absolutely not possible.
- Where possible, computations that can be performed at compile time are done there instead of at run time.
- They are intended to make code more portable across other C2000 devices.
- Code written with these APIs will be more readable than code written using many direct register accesses.

Some consequences of this are that the drivers are not necessarily as efficient as they could be (from a code size and/or execution speed point of view). While the most efficient piece of code for operating a peripheral would be written in assembly and custom tailored to the specific requirements of the application, further size optimizations of the drivers would make them more difficult to understand.

For many applications, the drivers can be used as is. But in some cases, the drivers will have to be enhanced or rewritten in order to meet the functionality, memory, or processing requirements of the application. If so, the existing driver can be used as a reference on how to operate the peripheral.

Minimum Requirements: CCSv6.2.0.00050 and C2000 Compiler v16.9.1.LTS

Source Code Overview

The following is an overview of the organization of the peripheral driver library source code.

`driverlib/` This directory contains the source code for the drivers.

`driverlib/inc/` This directory holds the peripheral, interrupt, and register access header files used for the direct register access programming model.

`hw_*.h` Header files, one per peripheral, that describe all the registers and the bit fields within those registers for each peripheral. These header files are used by the drivers to directly access a peripheral, and can be used by application code to bypass the peripheral driver library API.

2 Revision History

v2.00.00.02

- IMPORTANT: This is the new upgraded version of the C2000ware
- Several bug fixes in driverlib - Limited details in release notes
- New enhancements in driverlib - Limited details in release notes
- Adding EABI support with new index libs for driverlib

v1.04.00.00

- IMPORTANT: hw_ints.h - Changed IPC interrupt numbering from 1, 2, 3 4 to 0, 1, 2 3.
- dac.c - Corrected DAC_tuneOffsetTrim() function. Removed references of key for lock register in DAC_lockRegister().
- can.c - Updated CAN_readMessage() function to use base instead of CANA$_{B}ASEparameterwhereeverhardcoded.cla.h-UpdatedCLAtriggerssources$

- epwm.h - Added APIs for DC Edge Filter configurations.
- hw_types.h - Added header guards for float types

v1.03.00.00

- IMPORTANT: can.h - Changed interrupt numbering from 1 and 2 to 0 and 1
- hrpwm.h - Removed HRPWM_enableSelfSync and HRPWM_disableSelfSync functions
- xbar.h - Corrected ASSERT values
- xbar.h - Corrected enum value from XBAR_INPUT_FLG_INPUT7 to XBAR_INPUT_FLG_INPUT6
- dac.h - New DAC_tuneOffsetTrim() function
- flash.h - Added pragmas for functions in RAM when building for C++
- epwm.h - New functions: EPWM_enableValleyCapture(), EPWM_disableValleyCapture(), EPWM_startValleyCapture(), EPWM_setValleyTriggerSource(), EPWM_setValleyTriggerEdgeCounts(), EPWM_enableValleyHWDelay(), EPWM_disableValleyHWDelay(), EPWM_setValleySWDelayValue(), EPWM_setValleyDelayDivider(), EPWM_getValleyEdgeStatus(), EPWM_getValleyCount(), EPWM_getValleyHWDelay()

v1.02.00.00

- IMPORTANT: sysctl.c - SysCtl_setClock() and SysCtl_setAuxClock() enhanced with slip bit monitor and SYSCLK frequency check
- can.c - Fixed issue when setting up, sending, or receiving CAN messages that message object 32 would get enabled. Additionally, this fixes issues when optimizing.
- adc.h - New temperature sensor functions: ADC_getTemperatureC(), ADC_getTemperatureK()
- emif.h - Corrected incorrect register name

v1.01.00.00

- IMPORTANT: sdfm.h and hw_sdfm.h - Renamed macros containing "SDIPARMx" to "SDDPARMx" and renamed "FILRESEN" to "SDSYNCEN"
- clapromcrc.h - Corrected return value for CLAPROMCRC_checkStatus()

- can.c - Fixed issue where CAN_readMessage() wasn't clearing the NewData bit field
- can.c - Removed clears to interface registers in CAN_setupMessageObject() causing optimization issues
- can.h - Removed macros for CAN_STATUS_PDA and CAN_STATUS_WAKE_UP
- hw_can.h - Removed Can Core Release register and bit fields. Also removed macros for PDR, WUBA, wake up pending, and PDA
- hw_can.h - Renamed incorrect "Name" field in the CAN_GLB_INT_FLG register to INT0_FLG

v1.00.00.00

- Initial release

3 Programming Model

3.1 Introduction

The peripheral driver library provides support for two programming models: the direct register access model and the software driver model. Each model can be used independently or combined, based on the needs of the application or the programming environment desired by the developer.

Each programming model has advantages and disadvantages. Use of the direct register access model generally results in smaller and more efficient code than using the software driver model. However, the direct register access model requires detailed knowledge of the operation of each register and bit field, as well as their interactions and any sequencing required for proper operation of the peripheral; the developer is somewhat more insulated from these details by the software driver model, generally requiring less time to develop applications. The software driver model also results in more readable code.

3.2 Direct Register Access Model

In the direct register access model, the peripherals are programmed by the application by writing values directly into the peripheral's registers. A set of macros is provided that simplifies this process. These macros are stored in several header files contained in the `inc` directory. By including the header files `inc/hw_types.h` and `inc/hw_memmap.h`, macros are available for accessing all registers. Individual bitfield accesses can easily be added by simply including the `inc/hw_peripheral.h` header file for the desired peripheral.

The defines used by the direct register access model follow a naming convention that makes it easier to know how to use a particular macro. The rules are as follows:

- Values that end in `_BASE` and are found in `inc/hw_memmap.h` are module instance base addresses. For example, `SPIA_BASE` and `SPIB_BASE` are the base addresses of instances A and B of the SPI module respectively.
- Values that contain an `_O_` are register address offsets used to access the value of a register. For example, `SPI_O_CCR` is used to access the `CCR` register in a SPI module. These can be added to the base address values to get the register address.
- Values that end in `_M` represent the mask for a multi-bit field in a register. For example, `SPI_CCR_SPICHAR_M` is a mask for the `SPICHAR` field in the `CCR` register. Note that fields that are the whole width of the register are not given masks.
- Values that end in `_S` represent the number of bits to shift a value in order to align it with a multi-bit field. These values match the macro with the same base name but ending with `_M`.
- All others are single-bit field masks. For example, `SPI_CCR_SPILBK` corresponds to the `SPILBK` bit in the `CCR` register.

The `inc\hw_types.h` file contains macros to access a register. They are as follows where `x` is the address to be accessed:

- `HWREG(x)` is used for 32-bit accesses, such as reading a value from a 32-bit counter register.
- `HWREGH(x)` is used for 16-bit accesses. This can be used to access a 16-bit register or the upper or lower words of a 32-bit register. This is usually the most efficient.
- `HWREGB(x)` is used for 8-bit accesses using the __byte() intrinsic (see the TMS320C28x Optimizing C/C++ Compiler User's Guide). It typically should only be used when an 8-bit access is required by the hardware. Otherwise, use `HWREGH()` and mask and shift out the unwanted bits.
- `HWREG_BP(x)` is another macro used for 32-bit accesses, but it uses the __byte_peripheral_32() compiler intrinsic. This is intended for use with peripherals that use a special addressing scheme to support byte accesses such as CAN or USB.

Given these definitions, the `CCR` register can be programmed as follows:

```
// Enable loopback mode on SPI A
HWREGH(SPIA_BASE + SPI_O_CCR) |= SPI_CCR_SPILBK;

// Change the number of bits that make up a character to 8
// - First clear the field
// - Then shift the new value into place and write it into the register
HWREGH(SPIA_BASE + SPI_O_CCR) &= ~SPI_CCR_SPICHAR_M;
HWREGH(SPIA_BASE + SPI_O_CCR) |= 8 << SPI_CCR_SPICHAR_S;
```

Extracting the value of the `SPICHAR` field in the `CCR` register is as follows:

```
x = (HWREGH(SPIA_BASE + SPI_O_CCR) & SPI_CCR_SPICHAR_M) >> SPI_CCR_SPICHAR_S;
```

3.3 Software Driver Model

In the software driver model, the API provided by the peripheral driver library is used by applications to control the peripherals. Because these drivers provide complete control of the peripherals in their normal mode of operation, it is possible to write an entire application without direct access to the hardware. This method provides for rapid development of the application without requiring detailed knowledge of the registers.

The following function call programs the `SPICHAR` field of `CCR` register mentioned in the direct register access model as well as a few other fields and registers.

```
    SPI_setConfig(SPIA_BASE,  100000000,  SPI_PROT_POL0PHA0,
                  SPI_MODE_MASTER,  500000,  16);
```

The drivers in the peripheral driver library are described in the remaining chapters in this document. They combine to form the software driver model.

3.4 Combining The Models

The direct register access model and software driver model can be used together in a single application, allowing the most appropriate model to be applied as needed to any particular situation within the application. For example, the software driver model can be used to configure the peripherals (because this is not performance critical) and the direct register access model can be used for operation of the peripheral (which may be more performance critical). Or, the software driver model can be used for peripherals that are not performance critical (such as SCI used for data logging) and the direct register access model for performance critical peripherals.

Additionally, the direct register access model can be used when there is no suitable driver library API for the desired task. Although an API may be available that performs a specific function on an individual bit or register, it could be more beneficial to use the direct register access programming model when performing tasks on entire registers or multiple bits at a given time. However, if there is an API available for the intended task it should be used as it will provide for more rapid development of the application without going into depth on programming the peripherals.

4 Driver Library Usage

4.1 Introduction

To develop with the peripheral driver library more efficiently, Code Composer Studio (CCS) offers several project and workspace features that can help maximize development time and device application execution. As previously discussed in the programming model chapter, there are advantages and disadvantages to each programming model. This chapter will explain optimization tips that should be used in conjuction with the APIs provided by the peripheral driver library to overcome and minimize those disadvantages.

4.2 Code Composer Studio Tips

This section will detail some Code Composer Studio (CCS) tips that can be used to help effectively use the driver library during development.

4.2.1 Content Assist

In CCS, the Content Assist feature can be used to offer suggestions for completing function and parameter names. This feature may be auto-activated while typing or it can be activated by hitting Ctrl+Space. To get the desired preferences, adjust the settings under C/C++ -> Editor -> Content Assist. The figure below shows the Content Assist in use.

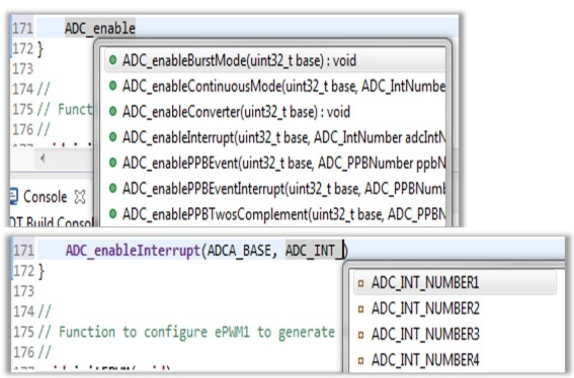

Figure 4.1: Content Assist

If you can't tell what an appropriate parameter is just from looking at the function prototype and the Content Assist list, hover over the function to view its description.

4.2.2 CCS Outline View

With a driver header file open, it is useful to take advantage of the CCS Outline view to get a complete list of functions, enumerations, and macros. The Outline view can be opened by selecting Window -> Show view -> Outline. The figure below shows the outline view in use.

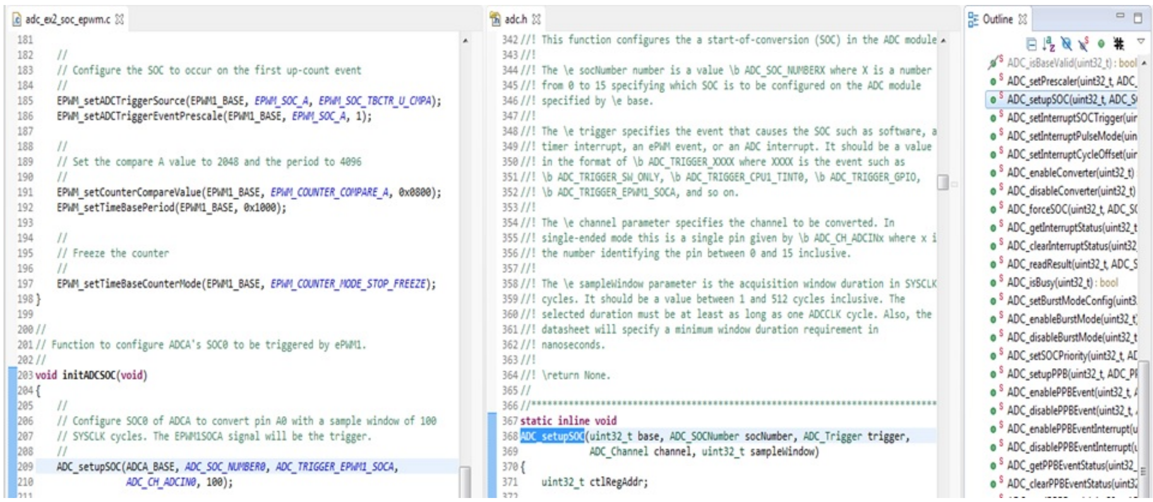

Figure 4.2: CCS Outline View

Similarly, you can split screen between application code and the API Reference Guide in the Resource Explorer.

Additionally, the function prototype in a driver header file can be viewed by holding Ctrl and clicking on the function name in the application code.

For more information on any of the tips provided, refer to the CCS Online Help section for details (CCS menu Help -> Help Contents and search for Content Assist).

4.3 ASSERT Macro

An ASSERT macro is defined in the `driverlib/debug.h` file as a method of checking the validity of function arguments and other error conditions. When the symbol DEBUG is defined, ASSERT(*expr*) will call a user-defined error function __error__() when Boolean expression *expr* is evaluated to false. To use the macro, an application must provide an __error__() function with the following prototype:

```
void __error__(char *filename, uint32_t line);
```

The *filename* and *line* parameters indicate which ASSERT resulted in the error condition. It is up to the application to decide what action the __error__() function should take to report the error.

The default Debug build configuration for the driverlib.lib project and the Driverlib example projects have turned on ASSERT by putting DEBUG in the projects' predefined symbols. Removing the DEBUG symbol from the projects will cause the ASSERT macro to compile to nothing, meaning it will add no code size or cycles to the application when it is turned off.

4.4 Driver Library Optimization

When using the software driver programming model it is important to note that there is a price to abstraction and making functions generic. Some of the drawbacks include the overhead time of the function call and the calculation time required to access a specific register offset or bit field within the register.

To help overcome these shortcomings, it is important to consider the use of inline functions. Using inline functions eliminates the need for function calls since the function is essentially treated like a macro. If constants are being passed into the function's parameters, much of its code may be evaluated at compile time. In order to utilize inline functions you must turn on optimization for it to take effect. If optimization is desired without the use of inline functions, use the –no_inling (-pi) option. This option can be set in the CCS project properties under Build -> C2000 Compiler -> Advanced Options -> Language Options.

In addition to inline functions, using the "generating function subsection" compiler option(–gen_func_subsections=on, -mo) is important. By default, the library project provided with the peripheral driver library project has this option turned on. When this option is selected, the compiler places each driver library function into its own subsection. This allows only the functions that are referenced in the application to be linked into the final executable. This can result in an overall code size reduction. This compiler option can be set by accessing the CCS project properties under Build -> C2000 Compiler -> Advanced Options -> Runtime Model Options.

The optimization options can be found in the CCS project properties which is accessed by right-clicking on the project in the project explorer and selecting properties. In the resulting window, the optimization settings are found in Build -> C2000 Compiler -> Optimization.

5 ADC Module

5.1 ADC Introduction

The analog to digital converter (ADC) API provides a set of functions for programming the digital circuits of the converter, referred to as the ADC wrapper. Functions are provided to configure the conversions, read the data conversion result registers, configure the post-processing blocks (PPB), and set up and handle interrupts and events.

5.2 API Functions

Enumerations

- enum ADC_ClkPrescale {
  ADC_CLK_DIV_1_0, ADC_CLK_DIV_2_0, ADC_CLK_DIV_2_5, ADC_CLK_DIV_3_0,
  ADC_CLK_DIV_3_5, ADC_CLK_DIV_4_0, ADC_CLK_DIV_4_5, ADC_CLK_DIV_5_0,
  ADC_CLK_DIV_5_5, ADC_CLK_DIV_6_0, ADC_CLK_DIV_6_5, ADC_CLK_DIV_7_0,
  ADC_CLK_DIV_7_5, ADC_CLK_DIV_8_0, ADC_CLK_DIV_8_5 }
- enum ADC_Resolution { ADC_RESOLUTION_12BIT, ADC_RESOLUTION_16BIT }
- enum ADC_SignalMode { ADC_MODE_SINGLE_ENDED, ADC_MODE_DIFFERENTIAL }
- enum ADC_Trigger {
  ADC_TRIGGER_SW_ONLY, ADC_TRIGGER_CPU1_TINT0,
  ADC_TRIGGER_CPU1_TINT1, ADC_TRIGGER_CPU1_TINT2,
  ADC_TRIGGER_GPIO, ADC_TRIGGER_EPWM1_SOCA,
  ADC_TRIGGER_EPWM1_SOCB, ADC_TRIGGER_EPWM2_SOCA,
  ADC_TRIGGER_EPWM2_SOCB, ADC_TRIGGER_EPWM3_SOCA,
  ADC_TRIGGER_EPWM3_SOCB, ADC_TRIGGER_EPWM4_SOCA,
  ADC_TRIGGER_EPWM4_SOCB, ADC_TRIGGER_EPWM5_SOCA,
  ADC_TRIGGER_EPWM5_SOCB, ADC_TRIGGER_EPWM6_SOCA,
  ADC_TRIGGER_EPWM6_SOCB, ADC_TRIGGER_EPWM7_SOCA,
  ADC_TRIGGER_EPWM7_SOCB, ADC_TRIGGER_EPWM8_SOCA,
  ADC_TRIGGER_EPWM8_SOCB, ADC_TRIGGER_EPWM9_SOCA,
  ADC_TRIGGER_EPWM9_SOCB, ADC_TRIGGER_EPWM10_SOCA,
  ADC_TRIGGER_EPWM10_SOCB, ADC_TRIGGER_EPWM11_SOCA,
  ADC_TRIGGER_EPWM11_SOCB, ADC_TRIGGER_EPWM12_SOCA,
  ADC_TRIGGER_EPWM12_SOCB, ADC_TRIGGER_CPU2_TINT0,
  ADC_TRIGGER_CPU2_TINT1, ADC_TRIGGER_CPU2_TINT2 }
- enum ADC_Channel {
  ADC_CH_ADCIN0, ADC_CH_ADCIN1, ADC_CH_ADCIN2, ADC_CH_ADCIN3,
  ADC_CH_ADCIN4, ADC_CH_ADCIN5, ADC_CH_ADCIN6, ADC_CH_ADCIN7,
  ADC_CH_ADCIN8, ADC_CH_ADCIN9, ADC_CH_ADCIN10, ADC_CH_ADCIN11,
  ADC_CH_ADCIN12, ADC_CH_ADCIN13, ADC_CH_ADCIN14, ADC_CH_ADCIN15,
  ADC_CH_ADCIN0_ADCIN1, ADC_CH_ADCIN2_ADCIN3, ADC_CH_ADCIN4_ADCIN5,

ADC_CH_ADCIN6_ADCIN7,
ADC_CH_ADCIN8_ADCIN9, ADC_CH_ADCIN10_ADCIN11,
ADC_CH_ADCIN12_ADCIN13, ADC_CH_ADCIN14_ADCIN15 }
- enum ADC_PulseMode { ADC_PULSE_END_OF_ACQ_WIN,
  ADC_PULSE_END_OF_CONV }
- enum ADC_IntNumber { ADC_INT_NUMBER1, ADC_INT_NUMBER2,
  ADC_INT_NUMBER3, ADC_INT_NUMBER4 }
- enum ADC_PPBNumber { ADC_PPB_NUMBER1, ADC_PPB_NUMBER2,
  ADC_PPB_NUMBER3, ADC_PPB_NUMBER4 }
- enum ADC_SOCNumber {
  ADC_SOC_NUMBER0, ADC_SOC_NUMBER1, ADC_SOC_NUMBER2,
  ADC_SOC_NUMBER3,
  ADC_SOC_NUMBER4, ADC_SOC_NUMBER5, ADC_SOC_NUMBER6,
  ADC_SOC_NUMBER7,
  ADC_SOC_NUMBER8, ADC_SOC_NUMBER9, ADC_SOC_NUMBER10,
  ADC_SOC_NUMBER11,
  ADC_SOC_NUMBER12, ADC_SOC_NUMBER13, ADC_SOC_NUMBER14,
  ADC_SOC_NUMBER15 }
- enum ADC_IntSOCTrigger { ADC_INT_SOC_TRIGGER_NONE,
  ADC_INT_SOC_TRIGGER_ADCINT1, ADC_INT_SOC_TRIGGER_ADCINT2 }
- enum ADC_PriorityMode {
  ADC_PRI_ALL_ROUND_ROBIN, ADC_PRI_SOC0_HIPRI, ADC_PRI_THRU_SOC1_HIPRI,
  ADC_PRI_THRU_SOC2_HIPRI,
  ADC_PRI_THRU_SOC3_HIPRI, ADC_PRI_THRU_SOC4_HIPRI,
  ADC_PRI_THRU_SOC5_HIPRI, ADC_PRI_THRU_SOC6_HIPRI,
  ADC_PRI_THRU_SOC7_HIPRI, ADC_PRI_THRU_SOC8_HIPRI,
  ADC_PRI_THRU_SOC9_HIPRI, ADC_PRI_THRU_SOC10_HIPRI,
  ADC_PRI_THRU_SOC11_HIPRI, ADC_PRI_THRU_SOC12_HIPRI,
  ADC_PRI_THRU_SOC13_HIPRI, ADC_PRI_THRU_SOC14_HIPRI,
  ADC_PRI_ALL_HIPRI }

Functions

- static void ADC_setPrescaler (uint32_t base, ADC_ClkPrescale clkPrescale)
- static void ADC_setupSOC (uint32_t base, ADC_SOCNumber socNumber, ADC_Trigger trigger, ADC_Channel channel, uint32_t sampleWindow)
- static void ADC_setInterruptSOCTrigger (uint32_t base, ADC_SOCNumber socNumber, ADC_IntSOCTrigger trigger)
- static void ADC_setInterruptPulseMode (uint32_t base, ADC_PulseMode pulseMode)
- static void ADC_enableConverter (uint32_t base)
- static void ADC_disableConverter (uint32_t base)
- static void ADC_forceSOC (uint32_t base, ADC_SOCNumber socNumber)
- static bool ADC_getInterruptStatus (uint32_t base, ADC_IntNumber adcIntNum)
- static void ADC_clearInterruptStatus (uint32_t base, ADC_IntNumber adcIntNum)
- static bool ADC_getInterruptOverflowStatus (uint32_t base, ADC_IntNumber adcIntNum)
- static void ADC_clearInterruptOverflowStatus (uint32_t base, ADC_IntNumber adcIntNum)
- static uint16_t ADC_readResult (uint32_t resultBase, ADC_SOCNumber socNumber)
- static bool ADC_isBusy (uint32_t base)
- static void ADC_setBurstModeConfig (uint32_t base, ADC_Trigger trigger, uint16_t burstSize)
- static void ADC_enableBurstMode (uint32_t base)
- static void ADC_disableBurstMode (uint32_t base)
- static void ADC_setSOCPriority (uint32_t base, ADC_PriorityMode priMode)
- static void ADC_setupPPB (uint32_t base, ADC_PPBNumber ppbNumber, ADC_SOCNumber socNumber)

- static void ADC_enablePPBEvent (uint32_t base, ADC_PPBNumber ppbNumber, uint16_t evtFlags)
- static void ADC_disablePPBEvent (uint32_t base, ADC_PPBNumber ppbNumber, uint16_t evtFlags)
- static void ADC_enablePPBEventInterrupt (uint32_t base, ADC_PPBNumber ppbNumber, uint16_t intFlags)
- static void ADC_disablePPBEventInterrupt (uint32_t base, ADC_PPBNumber ppbNumber, uint16_t intFlags)
- static uint16_t ADC_getPPBEventStatus (uint32_t base, ADC_PPBNumber ppbNumber)
- static void ADC_clearPPBEventStatus (uint32_t base, ADC_PPBNumber ppbNumber, uint16_t evtFlags)
- static int32_t ADC_readPPBResult (uint32_t resultBase, ADC_PPBNumber ppbNumber)
- static uint16_t ADC_getPPBDelayTimeStamp (uint32_t base, ADC_PPBNumber ppbNumber)
- static void ADC_setPPBCalibrationOffset (uint32_t base, ADC_PPBNumber ppbNumber, int16_t offset)
- static void ADC_setPPBReferenceOffset (uint32_t base, ADC_PPBNumber ppbNumber, uint16_t offset)
- static void ADC_enablePPBTwosComplement (uint32_t base, ADC_PPBNumber ppbNumber)
- static void ADC_disablePPBTwosComplement (uint32_t base, ADC_PPBNumber ppbNumber)
- static void ADC_enableInterrupt (uint32_t base, ADC_IntNumber adcIntNum)
- static void ADC_disableInterrupt (uint32_t base, ADC_IntNumber adcIntNum)
- static void ADC_setInterruptSource (uint32_t base, ADC_IntNumber adcIntNum, ADC_SOCNumber socNumber)
- static void ADC_enableContinuousMode (uint32_t base, ADC_IntNumber adcIntNum)
- static void ADC_disableContinuousMode (uint32_t base, ADC_IntNumber adcIntNum)
- static int16_t ADC_getTemperatureC (uint16_t tempResult, float32_t vref)
- static int16_t ADC_getTemperatureK (uint16_t tempResult, float32_t vref)
- void ADC_setMode (uint32_t base, ADC_Resolution resolution, ADC_SignalMode signalMode)
- void ADC_setPPBTripLimits (uint32_t base, ADC_PPBNumber ppbNumber, int32_t tripHiLimit, int32_t tripLoLimit)

5.2.1 Detailed Description

The code for this module is contained in `driverlib/adc.c`, with `driverlib/adc.h` containing the API declarations for use by applications.

5.2.2 Enumeration Type Documentation

5.2.2.1 enum **ADC_ClkPrescale**

Values that can be passed to ADC_setPrescaler() as the *clkPrescale* parameter.

Enumerator

ADC_CLK_DIV_1_0 ADCCLK = (input clock) / 1.0.

ADC_CLK_DIV_2_0 ADCCLK = (input clock) / 2.0.

ADC_CLK_DIV_2_5 ADCCLK = (input clock) / 2.5.

ADC_CLK_DIV_3_0 ADCCLK = (input clock) / 3.0.

ADC_CLK_DIV_3_5 ADCCLK = (input clock) / 3.5.
ADC_CLK_DIV_4_0 ADCCLK = (input clock) / 4.0.
ADC_CLK_DIV_4_5 ADCCLK = (input clock) / 4.5.
ADC_CLK_DIV_5_0 ADCCLK = (input clock) / 5.0.
ADC_CLK_DIV_5_5 ADCCLK = (input clock) / 5.5.
ADC_CLK_DIV_6_0 ADCCLK = (input clock) / 6.0.
ADC_CLK_DIV_6_5 ADCCLK = (input clock) / 6.5.
ADC_CLK_DIV_7_0 ADCCLK = (input clock) / 7.0.
ADC_CLK_DIV_7_5 ADCCLK = (input clock) / 7.5.
ADC_CLK_DIV_8_0 ADCCLK = (input clock) / 8.0.
ADC_CLK_DIV_8_5 ADCCLK = (input clock) / 8.5.

5.2.2.2 enum **ADC_Resolution**

Values that can be passed to ADC_setMode() as the *resolution* parameter.

Enumerator
ADC_RESOLUTION_12BIT 12-bit conversion resolution
ADC_RESOLUTION_16BIT 16-bit conversion resolution

5.2.2.3 enum **ADC_SignalMode**

Values that can be passed to ADC_setMode() as the *signalMode* parameter.

Enumerator
ADC_MODE_SINGLE_ENDED Sample on single pin with VREFLO.
ADC_MODE_DIFFERENTIAL Sample on pair of pins.

5.2.2.4 enum **ADC_Trigger**

Values that can be passed to ADC_setupSOC() as the *trigger* parameter to specify the event that will trigger a conversion to start. It is also used with ADC_setBurstModeConfig().

Enumerator
ADC_TRIGGER_SW_ONLY Software only.
ADC_TRIGGER_CPU1_TINT0 CPU1 Timer 0, TINT0.
ADC_TRIGGER_CPU1_TINT1 CPU1 Timer 1, TINT1.
ADC_TRIGGER_CPU1_TINT2 CPU1 Timer 2, TINT2.
ADC_TRIGGER_GPIO GPIO, ADCEXTSOC.
ADC_TRIGGER_EPWM1_SOCA ePWM1, ADCSOCA
ADC_TRIGGER_EPWM1_SOCB ePWM1, ADCSOCB
ADC_TRIGGER_EPWM2_SOCA ePWM2, ADCSOCA
ADC_TRIGGER_EPWM2_SOCB ePWM2, ADCSOCB
ADC_TRIGGER_EPWM3_SOCA ePWM3, ADCSOCA
ADC_TRIGGER_EPWM3_SOCB ePWM3, ADCSOCB

ADC_TRIGGER_EPWM4_SOCA ePWM4, ADCSOCA
ADC_TRIGGER_EPWM4_SOCB ePWM4, ADCSOCB
ADC_TRIGGER_EPWM5_SOCA ePWM5, ADCSOCA
ADC_TRIGGER_EPWM5_SOCB ePWM5, ADCSOCB
ADC_TRIGGER_EPWM6_SOCA ePWM6, ADCSOCA
ADC_TRIGGER_EPWM6_SOCB ePWM6, ADCSOCB
ADC_TRIGGER_EPWM7_SOCA ePWM7, ADCSOCA
ADC_TRIGGER_EPWM7_SOCB ePWM7, ADCSOCB
ADC_TRIGGER_EPWM8_SOCA ePWM8, ADCSOCA
ADC_TRIGGER_EPWM8_SOCB ePWM8, ADCSOCB
ADC_TRIGGER_EPWM9_SOCA ePWM9, ADCSOCA
ADC_TRIGGER_EPWM9_SOCB ePWM9, ADCSOCB
ADC_TRIGGER_EPWM10_SOCA ePWM10, ADCSOCA
ADC_TRIGGER_EPWM10_SOCB ePWM10, ADCSOCB
ADC_TRIGGER_EPWM11_SOCA ePWM11, ADCSOCA
ADC_TRIGGER_EPWM11_SOCB ePWM11, ADCSOCB
ADC_TRIGGER_EPWM12_SOCA ePWM12, ADCSOCA
ADC_TRIGGER_EPWM12_SOCB ePWM12, ADCSOCB
ADC_TRIGGER_CPU2_TINT0 CPU2 Timer 0, TINT0.
ADC_TRIGGER_CPU2_TINT1 CPU2 Timer 1, TINT1.
ADC_TRIGGER_CPU2_TINT2 CPU2 Timer 2, TINT2.

5.2.2.5 enum **ADC_Channel**

Values that can be passed to ADC_setupSOC() as the *channel* parameter. This is the input pin on which the signal to be converted is located.

Enumerator

ADC_CH_ADCIN0 single-ended, ADCIN0
ADC_CH_ADCIN1 single-ended, ADCIN1
ADC_CH_ADCIN2 single-ended, ADCIN2
ADC_CH_ADCIN3 single-ended, ADCIN3
ADC_CH_ADCIN4 single-ended, ADCIN4
ADC_CH_ADCIN5 single-ended, ADCIN5
ADC_CH_ADCIN6 single-ended, ADCIN6
ADC_CH_ADCIN7 single-ended, ADCIN7
ADC_CH_ADCIN8 single-ended, ADCIN8
ADC_CH_ADCIN9 single-ended, ADCIN9
ADC_CH_ADCIN10 single-ended, ADCIN10
ADC_CH_ADCIN11 single-ended, ADCIN11
ADC_CH_ADCIN12 single-ended, ADCIN12
ADC_CH_ADCIN13 single-ended, ADCIN13
ADC_CH_ADCIN14 single-ended, ADCIN14
ADC_CH_ADCIN15 single-ended, ADCIN15
ADC_CH_ADCIN0_ADCIN1 differential, ADCIN0 and ADCIN1
ADC_CH_ADCIN2_ADCIN3 differential, ADCIN2 and ADCIN3

ADC_CH_ADCIN4_ADCIN5 differential, ADCIN4 and ADCIN5
ADC_CH_ADCIN6_ADCIN7 differential, ADCIN6 and ADCIN7
ADC_CH_ADCIN8_ADCIN9 differential, ADCIN8 and ADCIN9
ADC_CH_ADCIN10_ADCIN11 differential, ADCIN10 and ADCIN11
ADC_CH_ADCIN12_ADCIN13 differential, ADCIN12 and ADCIN13
ADC_CH_ADCIN14_ADCIN15 differential, ADCIN14 and ADCIN15

5.2.2.6 enum **ADC_PulseMode**

Values that can be passed to ADC_setInterruptPulseMode() as the *pulseMode* parameter.

Enumerator

ADC_PULSE_END_OF_ACQ_WIN Occurs at the end of the acquisition window.
ADC_PULSE_END_OF_CONV Occurs at the end of the conversion.

5.2.2.7 enum **ADC_IntNumber**

Values that can be passed to ADC_enableInterrupt(), ADC_disableInterrupt(), and ADC_getInterruptStatus() as the *adcIntNum* parameter.

Enumerator

ADC_INT_NUMBER1 ADCINT1 Interrupt.
ADC_INT_NUMBER2 ADCINT2 Interrupt.
ADC_INT_NUMBER3 ADCINT3 Interrupt.
ADC_INT_NUMBER4 ADCINT4 Interrupt.

5.2.2.8 enum **ADC_PPBNumber**

Values that can be passed in as the *ppbNumber* parameter for several functions.

Enumerator

ADC_PPB_NUMBER1 Post-processing block 1.
ADC_PPB_NUMBER2 Post-processing block 2.
ADC_PPB_NUMBER3 Post-processing block 3.
ADC_PPB_NUMBER4 Post-processing block 4.

5.2.2.9 enum **ADC_SOCNumber**

Values that can be passed in as the *socNumber* parameter for several functions. This value identifies the start-of-conversion (SOC) that a function is configuring or accessing. Note that in some cases (for example, ADC_setInterruptSource()) *socNumber* is used to refer to the corresponding end-of-conversion (EOC).

Enumerator

ADC_SOC_NUMBER0 SOC/EOC number 0.
ADC_SOC_NUMBER1 SOC/EOC number 1.

ADC_SOC_NUMBER2 SOC/EOC number 2.
ADC_SOC_NUMBER3 SOC/EOC number 3.
ADC_SOC_NUMBER4 SOC/EOC number 4.
ADC_SOC_NUMBER5 SOC/EOC number 5.
ADC_SOC_NUMBER6 SOC/EOC number 6.
ADC_SOC_NUMBER7 SOC/EOC number 7.
ADC_SOC_NUMBER8 SOC/EOC number 8.
ADC_SOC_NUMBER9 SOC/EOC number 9.
ADC_SOC_NUMBER10 SOC/EOC number 10.
ADC_SOC_NUMBER11 SOC/EOC number 11.
ADC_SOC_NUMBER12 SOC/EOC number 12.
ADC_SOC_NUMBER13 SOC/EOC number 13.
ADC_SOC_NUMBER14 SOC/EOC number 14.
ADC_SOC_NUMBER15 SOC/EOC number 15.

5.2.2.10 enum **ADC_IntSOCTrigger**

Values that can be passed in as the *trigger* parameter for the ADC_setInterruptSOCTrigger() function.

Enumerator

ADC_INT_SOC_TRIGGER_NONE No ADCINT will trigger the SOC.
ADC_INT_SOC_TRIGGER_ADCINT1 ADCINT1 will trigger the SOC.
ADC_INT_SOC_TRIGGER_ADCINT2 ADCINT2 will trigger the SOC.

5.2.2.11 enum **ADC_PriorityMode**

Values that can be passed to ADC_setSOCPriority() as the *priMode* parameter.

Enumerator

ADC_PRI_ALL_ROUND_ROBIN Round robin mode is used for all.
ADC_PRI_SOC0_HIPRI SOC 0 hi pri, others in round robin.
ADC_PRI_THRU_SOC1_HIPRI SOC 0-1 hi pri, others in round robin.
ADC_PRI_THRU_SOC2_HIPRI SOC 0-2 hi pri, others in round robin.
ADC_PRI_THRU_SOC3_HIPRI SOC 0-3 hi pri, others in round robin.
ADC_PRI_THRU_SOC4_HIPRI SOC 0-4 hi pri, others in round robin.
ADC_PRI_THRU_SOC5_HIPRI SOC 0-5 hi pri, others in round robin.
ADC_PRI_THRU_SOC6_HIPRI SOC 0-6 hi pri, others in round robin.
ADC_PRI_THRU_SOC7_HIPRI SOC 0-7 hi pri, others in round robin.
ADC_PRI_THRU_SOC8_HIPRI SOC 0-8 hi pri, others in round robin.
ADC_PRI_THRU_SOC9_HIPRI SOC 0-9 hi pri, others in round robin.
ADC_PRI_THRU_SOC10_HIPRI SOC 0-10 hi pri, others in round robin.
ADC_PRI_THRU_SOC11_HIPRI SOC 0-11 hi pri, others in round robin.
ADC_PRI_THRU_SOC12_HIPRI SOC 0-12 hi pri, others in round robin.
ADC_PRI_THRU_SOC13_HIPRI SOC 0-13 hi pri, others in round robin.
ADC_PRI_THRU_SOC14_HIPRI SOC 0-14 hi pri, SOC15 in round robin.
ADC_PRI_ALL_HIPRI All priorities based on SOC number.

5.2.3 Function Documentation

5.2.3.1 static void ADC_setPrescaler (uint32_t *base*, **ADC_ClkPrescale** *clkPrescale*) `[inline]`, `[static]`

Configures the analog-to-digital converter module prescaler.

Parameters

base	is the base address of the ADC module.
clkPrescale	is the ADC clock prescaler.

This function configures the ADC module's ADCCLK.

The *clkPrescale* parameter specifies the value by which the input clock is divided to make the ADCCLK. The value can be specified with the value **ADC_CLK_DIV_1_0**, **ADC_CLK_DIV_2_0**, **ADC_CLK_DIV_2_5**, ..., **ADC_CLK_DIV_7_5**, **ADC_CLK_DIV_8_0**, or **ADC_CLK_DIV_8_5**.

Returns

None.

5.2.3.2 static void ADC_setupSOC (uint32_t *base,* **ADC_SOCNumber** *socNumber,* **ADC_Trigger** *trigger,* **ADC_Channel** *channel,* uint32_t *sampleWindow*) `[inline]`, `[static]`

Configures a start-of-conversion (SOC) in the ADC.

Parameters

base	is the base address of the ADC module.
socNumber	is the number of the start-of-conversion.
trigger	the source that will cause the SOC.
channel	is the number associated with the input signal.
sampleWindow	is the acquisition window duration.

This function configures the a start-of-conversion (SOC) in the ADC module.

The *socNumber* number is a value **ADC_SOC_NUMBERX** where X is a number from 0 to 15 specifying which SOC is to be configured on the ADC module specified by *base*.

The *trigger* specifies the event that causes the SOC such as software, a timer interrupt, an ePWM event, or an ADC interrupt. It should be a value in the format of **ADC_TRIGGER_XXXX** where XXXX is the event such as **ADC_TRIGGER_SW_ONLY**, **ADC_TRIGGER_CPU1_TINT0**, **ADC_TRIGGER_GPIO**, **ADC_TRIGGER_EPWM1_SOCA**, and so on.

The *channel* parameter specifies the channel to be converted. In single-ended mode this is a single pin given by **ADC_CH_ADCINx** where x is the number identifying the pin between 0 and 15 inclusive. In differential mode, two pins are used as inputs and are passed in the *channel* parameter as **ADC_CH_ADCIN0_ADCIN1**, **ADC_CH_ADCIN2_ADCIN3**, ..., or **ADC_CH_ADCIN14_ADCIN15**.

The *sampleWindow* parameter is the acquisition window duration in SYSCLK cycles. It should be a value between 1 and 512 cycles inclusive. The selected duration must be at least as long as one ADCCLK cycle. Also, the datasheet will specify a minimum window duration requirement in nanoseconds.

Returns
None.

5.2.3.3 static void ADC_setInterruptSOCTrigger (uint32_t *base,* **ADC_SOCNumber** *socNumber,* **ADC_IntSOCTrigger** *trigger*) `[inline]`, `[static]`

Configures the interrupt SOC trigger of an SOC.

Parameters

base	is the base address of the ADC module.
socNumber	is the number of the start-of-conversion.
trigger	the interrupt source that will cause the SOC.

This function configures the interrupt start-of-conversion trigger in the ADC module.

The *socNumber* number is a value **ADC_SOC_NUMBERX** where X is a number from 0 to 15 specifying which SOC is to be configured on the ADC module specified by *base*.

The *trigger* specifies the interrupt that causes a start of conversion or none. It should be one of the following values.

- **ADC_INT_SOC_TRIGGER_NONE**
- **ADC_INT_SOC_TRIGGER_ADCINT1**
- **ADC_INT_SOC_TRIGGER_ADCINT2**

This functionality is useful for creating continuous conversions.

Returns

None.

5.2.3.4 static void ADC_setInterruptPulseMode (uint32_t *base*, **ADC_PulseMode** *pulseMode*) `[inline]`, `[static]`

Sets the timing of the end-of-conversion pulse

Parameters

base	is the base address of the ADC module.
pulseMode	is the generation mode of the EOC pulse.

This function configures the end-of-conversion (EOC) pulse generated by ADC. This pulse will be generated either at the end of the acquisition window (pass **ADC_PULSE_END_OF_ACQ_WIN** into *pulseMode*) or at the end of the voltage conversion, one cycle prior to the ADC result latching into it's result register (pass **ADC_PULSE_END_OF_CONV** into *pulseMode*).

Returns

None.

5.2.3.5 static void ADC_enableConverter (uint32_t *base*) `[inline]`, `[static]`

Powers up the analog-to-digital converter core.

Parameters

base	is the base address of the ADC module.

This function powers up the analog circuitry inside the analog core.

Note

Allow at least a 500us delay before sampling after calling this API. If you enable multiple ADCs, you can delay after they all have begun powering up.

Returns
None.

5.2.3.6 static void ADC_disableConverter (uint32_t *base*) [inline], [static]

Powers down the analog-to-digital converter module.

Parameters

base	is the base address of the ADC module.

This function powers down the analog circuitry inside the analog core.

Returns
None.

5.2.3.7 static void ADC_forceSOC (uint32_t *base*, **ADC_SOCNumber** *socNumber*) [inline], [static]

Forces a SOC flag to a 1 in the analog-to-digital converter.

Parameters

base	is the base address of the ADC module.
socNumber	is the number of the start-of-conversion.

This function forces the SOC flag associated with the SOC specified by *socNumber*. This initiates a conversion once that SOC is given priority. This software trigger can be used whether or not the SOC has been configured to accept some other specific trigger.

Returns
None.

5.2.3.8 static bool ADC_getInterruptStatus (uint32_t *base*, **ADC_IntNumber** *adcIntNum*) [inline], [static]

Gets the current ADC interrupt status.

Parameters

base	is the base address of the ADC module.
adcIntNum	is interrupt number within the ADC wrapper.

This function returns the interrupt status for the analog-to-digital converter.

adcIntNum takes a one of the values **ADC_INT_NUMBER1**, **ADC_INT_NUMBER2**, **ADC_INT_NUMBER3**, or **ADC_INT_NUMBER4** to express which of the four interrupts of the ADC module should be cleared.

Returns
true if the interrupt flag for the specified interrupt number is set and **false** if it is not.

5.2.3.9 static void ADC_clearInterruptStatus (uint32_t *base*, **ADC_IntNumber** *adcIntNum*) `[inline]`, `[static]`

Clears ADC interrupt sources.

Parameters

base	is the base address of the ADC module.
adcIntNum	is interrupt number within the ADC wrapper.

This function clears the specified ADC interrupt sources so that they no longer assert. If not in continuous mode, this function must be called before any further interrupt pulses may occur.

adcIntNum takes a one of the values **ADC_INT_NUMBER1**, **ADC_INT_NUMBER2**, **ADC_INT_NUMBER3**, or **ADC_INT_NUMBER4** to express which of the four interrupts of the ADC module should be cleared.

Returns
None.

5.2.3.10 static bool ADC_getInterruptOverflowStatus (uint32_t *base*, **ADC_IntNumber** *adcIntNum*) [inline], [static]

Gets the current ADC interrupt overflow status.

Parameters

base	is the base address of the ADC module.
adcIntNum	is interrupt number within the ADC wrapper.

This function returns the interrupt overflow status for the analog-to-digital converter. An overflow condition is generated irrespective of the continuous mode.

adcIntNum takes a one of the values **ADC_INT_NUMBER1**, **ADC_INT_NUMBER2**, **ADC_INT_NUMBER3**, or **ADC_INT_NUMBER4** to express which of the four interrupts of the ADC module should be cleared.

Returns
true if the interrupt overflow flag for the specified interrupt number is set and **false** if it is not.

5.2.3.11 static void ADC_clearInterruptOverflowStatus (uint32_t *base*, **ADC_IntNumber** *adcIntNum*) [inline], [static]

Clears ADC interrupt overflow sources.

Parameters

base	is the base address of the ADC module.
adcIntNum	is interrupt number within the ADC wrapper.

This function clears the specified ADC interrupt overflow sources so that they no longer assert. If software tries to clear the overflow in the same cycle that hardware tries to set the overflow, then hardware has priority.

adcIntNum takes a one of the values **ADC_INT_NUMBER1**, **ADC_INT_NUMBER2**, **ADC_INT_NUMBER3**, or **ADC_INT_NUMBER4** to express which of the four interrupts of the ADC module should be cleared.

Returns
None.

5.2.3.12 static uint16_t ADC_readResult (uint32_t *resultBase*, **ADC_SOCNumber** *socNumber*) `[inline]`, `[static]`

Reads the conversion result.

Parameters

resultBase	is the base address of the ADC results.
socNumber	is the number of the start-of-conversion.

This function returns the conversion result that corresponds to the base address passed into *resultBase* and the SOC passed into *socNumber*.

The *socNumber* number is a value **ADC_SOC_NUMBERX** where X is a number from 0 to 15 specifying which SOC's result is to be read.

Note

Take care that you are using a base address for the result registers (ADCxRESULT_BASE) and not a base address for the control registers.

Returns

Returns the conversion result.

5.2.3.13 static bool ADC_isBusy (uint32_t *base*) [inline], [static]

Determines whether the ADC is busy or not.

Parameters

base	is the base address of the ADC.

This function allows the caller to determine whether or not the ADC is busy and can sample another channel.

Returns

Returns **true** if the ADC is sampling or **false** if all samples are complete.

5.2.3.14 static void ADC_setBurstModeConfig (uint32_t *base*, **ADC_Trigger** *trigger*, uint16_t *burstSize*) [inline], [static]

Set SOC burst mode.

Parameters

base	is the base address of the ADC.
trigger	the source that will cause the burst conversion sequence.
burstSize	is the number of SOCs converted during a burst sequence.

This function configures the burst trigger and burstSize of an ADC module. Burst mode allows a single trigger to walk through the round-robin SOCs one or more at a time. When burst mode is enabled, the trigger selected by the ADC_setupSOC() API will no longer have an effect on the SOCs in round-robin mode. Instead, the source specified through the *trigger* parameter will cause a burst of *burstSize* conversions to occur.

The *trigger* parameter takes the same values as the ADC_setupSOC() API The *burstSize* parameter should be a value between 1 and 16 inclusive.

Returns

None.

5.2.3.15 static void ADC_enableBurstMode (uint32_t *base*) [inline], [static]

Enables SOC burst mode.

Parameters

base	is the base address of the ADC.

This function enables SOC burst mode operation of the ADC. Burst mode allows a single trigger to walk through the round-robin SOCs one or more at a time. When burst mode is enabled, the trigger selected by the ADC_setupSOC() API will no longer have an effect on the SOCs in round-robin mode. Use ADC_setBurstMode() to configure the burst trigger and size.

Returns
None.

5.2.3.16 static void ADC_disableBurstMode (uint32_t *base*) [inline], [static]

Disables SOC burst mode.

Parameters

base	is the base address of the ADC.

This function disables SOC burst mode operation of the ADC. SOCs in round-robin mode will be triggered by the trigger configured using the ADC_setupSOC() API.

Returns
None.

5.2.3.17 static void ADC_setSOCPriority (uint32_t *base,* **ADC_PriorityMode** *priMode*) [inline], [static]

Sets the priority mode of the SOCs.

Parameters

base	is the base address of the ADC.
priMode	is the priority mode of the SOCs.

This function sets the priority mode of the SOCs. There are three main modes that can be passed in the *priMode* parameter

- All SOCs are in round-robin mode. This means no SOC has an inherent higher priority over another. This is selected by passing in the value **ADC_PRI_ALL_ROUND_ROBIN**.
- All priorities are in high priority mode. This means that the priority of the SOC is determined by its SOC number. This option is selected by passing in the value **ADC_PRI_ALL_HIPRI**.
- A range of SOCs are assigned high priority, with all others in round robin mode. High priority mode means that an SOC with high priority will interrupt the round robin wheel and insert itself as the next conversion. Passing in the value **ADC_PRI_SOC0_HIPRI** will make SOC0 highest priority, **ADC_PRI_THRU_SOC1_HIPRI** will put SOC0 and SOC 1 in high priority, and so on up to **ADC_PRI_THRU_SOC14_HIPRI** where SOCs 0 through 14 are in high priority.

Returns
None.

5.2.3.18 static void ADC_setupPPB (uint32_t *base*, **ADC_PPBNumber** *ppbNumber*, **ADC_SOCNumber** *socNumber*) [inline], [static]

Configures a post-processing block (PPB) in the ADC.

Parameters

base	is the base address of the ADC module.
ppbNumber	is the number of the post-processing block.
socNumber	is the number of the start-of-conversion.

This function associates a post-processing block with a SOC.

The *ppbNumber* is a value **ADC_PPB_NUMBERX** where X is a value from 1 to 4 inclusive that identifies a PPB to be configured. The *socNumber* number is a value **ADC_SOC_NUMBERX** where X is a number from 0 to 15 specifying which SOC is to be configured on the ADC module specified by *base*.

Note

You can have more that one PPB associated with the same SOC, but a PPB can only be configured to correspond to one SOC at a time. Also note that when you have multiple PPBs for the same SOC, the calibration offset that actually gets applied will be that of the PPB with the highest number. Since SOC0 is the default for all PPBs, look out for unintentional overwriting of a lower numbered PPB's offset.

Returns

None.

5.2.3.19 static void ADC_enablePPBEvent (uint32_t *base,* **ADC_PPBNumber** *ppbNumber,* uint16_t *evtFlags*) `[inline]`, `[static]`

Enables individual ADC PPB event sources.

Parameters

base	is the base address of the ADC module.
ppbNumber	is the number of the post-processing block.
evtFlags	is a bit mask of the event sources to be enabled.

This function enables the indicated ADC PPB event sources. This will allow the specified events to propagate through the X-BAR to a pin or to an ePWM module. The *evtFlags* parameter can be any of the **ADC_EVT_TRIPHI**, **ADC_EVT_TRIPLO**, or **ADC_EVT_ZERO** values.

Returns

None.

5.2.3.20 static void ADC_disablePPBEvent (uint32_t *base,* **ADC_PPBNumber** *ppbNumber,* uint16_t *evtFlags*) `[inline]`, `[static]`

Disables individual ADC PPB event sources.

Parameters

base	is the base address of the ADC module.

ppbNumber	is the number of the post-processing block.
evtFlags	is a bit mask of the event sources to be enabled.

This function disables the indicated ADC PPB event sources. This will stop the specified events from propagating through the X-BAR to other modules. The *evtFlags* parameter can be any of the **ADC_EVT_TRIPHI**, **ADC_EVT_TRIPLO**, or **ADC_EVT_ZERO** values.

Returns
None.

5.2.3.21 static void ADC_enablePPBEventInterrupt (uint32_t *base*, **ADC_PPBNumber** *ppbNumber*, uint16_t *intFlags*) [inline], [static]

Enables individual ADC PPB event interrupt sources.

Parameters

base	is the base address of the ADC module.
ppbNumber	is the number of the post-processing block.
intFlags	is a bit mask of the interrupt sources to be enabled.

This function enables the indicated ADC PPB interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt. Disabled sources have no effect on the processor. The *intFlags* parameter can be any of the **ADC_EVT_TRIPHI**, **ADC_EVT_TRIPLO**, or **ADC_EVT_ZERO** values.

Returns
None.

5.2.3.22 static void ADC_disablePPBEventInterrupt (uint32_t *base*, **ADC_PPBNumber** *ppbNumber*, uint16_t *intFlags*) [inline], [static]

Disables individual ADC PPB event interrupt sources.

Parameters

base	is the base address of the ADC module.
ppbNumber	is the number of the post-processing block.
intFlags	is a bit mask of the interrupt source to be disabled.

This function disables the indicated ADC PPB interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt. Disabled sources have no effect on the processor. The *intFlags* parameter can be any of the **ADC_EVT_TRIPHI**, **ADC_EVT_TRIPLO**, or **ADC_EVT_ZERO** values.

Returns
None.

5.2.3.23 static uint16_t ADC_getPPBEventStatus (uint32_t *base*, **ADC_PPBNumber** *ppbNumber*) [inline], [static]

Gets the current ADC event status.

Parameters

base	is the base address of the ADC module.
ppbNumber	is the number of the post-processing block.

This function returns the event status for the analog-to-digital converter.

Returns

Returns the current event status, enumerated as a bit field of **ADC_EVT_TRIPHI**, **ADC_EVT_TRIPLO**, and **ADC_EVT_ZERO**.

5.2.3.24 static void ADC_clearPPBEventStatus (uint32_t *base,* **ADC_PPBNumber** *ppbNumber,* uint16_t *evtFlags*) [inline], [static]

Clears ADC event flags.

Parameters

base	is the base address of the ADC module.
ppbNumber	is the number of the post-processing block.
evtFlags	is a bit mask of the event source to be cleared.

This function clears the indicated ADC PPB event flags. After an event occurs this function must be called to allow additional events to be produced. The *evtFlags* parameter can be any of the **ADC_EVT_TRIPHI**, **ADC_EVT_TRIPLO**, or **ADC_EVT_ZERO** values.

Returns

None.

5.2.3.25 static int32_t ADC_readPPBResult (uint32_t *resultBase,* **ADC_PPBNumber** *ppbNumber*) [inline], [static]

Reads the processed conversion result from the PPB.

Parameters

resultBase	is the base address of the ADC results.
ppbNumber	is the number of the post-processing block.

This function returns the processed conversion result that corresponds to the base address passed into *resultBase* and the PPB passed into *ppbNumber*.

Note

Take care that you are using a base address for the result registers (ADCxRESULT_BASE) and not a base address for the control registers.

Returns

Returns the signed 32-bit conversion result.

5.2.3.26 static uint16_t ADC_getPPBDelayTimeStamp (uint32_t *base*, **ADC_PPBNumber** *ppbNumber*) [inline], [static]

Reads sample delay time stamp from a PPB.

Parameters

base	is the base address of the ADC module.
ppbNumber	is the number of the post-processing block.

This function returns the sample delay time stamp. This delay is the number of system clock cycles between the SOC being triggered and when it began converting.

Returns

Returns the delay time stamp.

5.2.3.27 static void ADC_setPPBCalibrationOffset (uint32_t *base*, **ADC_PPBNumber** *ppbNumber*, int16_t *offset*) [inline], [static]

Sets the post processing block offset correction.

Parameters

base	is the base address of the ADC module.
ppbNumber	is the number of the post-processing block.
offset	is the 10-bit signed value subtracted from ADC the output.

This function sets the PPB offset correction value. This value can be used to digitally remove any system-level offset inherent in the ADCIN circuit before it is stored in the appropriate result register. The *offset* parameter is **subtracted** from the ADC output and is a signed value from -512 to 511 inclusive. For example, when *offset* = 1, ADCRESULT = ADC output - 1. When *offset* = -512, ADCRESULT = ADC output - (-512) or ADC output + 512.

Passing a zero in to the *offset* parameter will effectively disable the calculation, allowing the raw ADC result to be passed unchanged into the result register.

Note

If multiple PPBs are applied to the same SOC, the offset that will be applied will be that of the PPB with the highest number.

Returns

None

5.2.3.28 static void ADC_setPPBReferenceOffset (uint32_t *base*, **ADC_PPBNumber** *ppbNumber*, uint16_t *offset*) [inline], [static]

Sets the post processing block reference offset.

Parameters

base	is the base address of the ADC module.
ppbNumber	is the number of the post-processing block.
offset	is the 16-bit unsigned value subtracted from ADC the output.

This function sets the PPB reference offset value. This can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. The result will be stored in the appropriate PPB result register which can be read using ADC_readPPBResult().

Passing a zero in to the *offset* parameter will effectively disable the calculation and will pass the ADC result to the PPB result register unchanged.

Note

If in 12-bit mode, you may only pass a 12-bit value into the *offset* parameter.

Returns

None

5.2.3.29 static void ADC_enablePPBTwosComplement (uint32_t *base*, **ADC_PPBNumber** *ppbNumber*) `[inline]`, `[static]`

Enables two's complement capability in the PPB.

Parameters

base	is the base address of the ADC module.
ppbNumber	is the number of the post-processing block.

This function enables two's complement in the post-processing block specified by the *ppbNumber* parameter. When enabled, a two's complement will be performed on the output of the offset subtraction before it is stored in the appropriate PPB result register. In other words, the PPB result will be the reference offset value minus the the ADC result value (ADCPPBxRESULT = ADCSOCxOFFREF - ADCRESULTx).

Returns

None

5.2.3.30 static void ADC_disablePPBTwosComplement (uint32_t *base*, **ADC_PPBNumber** *ppbNumber*) `[inline]`, `[static]`

Disables two's complement capability in the PPB.

Parameters

base	is the base address of the ADC module.
ppbNumber	is the number of the post-processing block.

This function disables two's complement in the post-processing block specified by the *ppbNumber* parameter. When disabled, a two's complement will **NOT** be performed on the output of the offset subtraction before it is stored in the appropriate PPB result register. In other words, the PPB result will be the ADC result value minus the reference offset value (ADCPPBxRESULT = ADCRESULTx - ADCSOCxOFFREF).

Returns

None

5.2.3.31 static void ADC_enableInterrupt (uint32_t *base*, **ADC_IntNumber** *adcIntNum*) `[inline]`, `[static]`

Enables an ADC interrupt source.

Parameters

base	is the base address of the ADC module.
adcIntNum	is interrupt number within the ADC wrapper.

This function enables the indicated ADC interrupt source. Only the sources that are enabled can be reflected to the processor interrupt. Disabled sources have no effect on the processor.

adcIntNum can take the value **ADC_INT_NUMBER1**, **ADC_INT_NUMBER2**, **ADC_INT_NUMBER3**, or **ADC_INT_NUMBER4** to express which of the four interrupts of the ADC module should be enabled.

Returns
None.

5.2.3.32 static void ADC_disableInterrupt (uint32_t *base*, **ADC_IntNumber** *adcIntNum*) [inline], [static]

Disables an ADC interrupt source.

Parameters

base	is the base address of the ADC module.
adcIntNum	is interrupt number within the ADC wrapper.

This function disables the indicated ADC interrupt source. Only the sources that are enabled can be reflected to the processor interrupt. Disabled sources have no effect on the processor.

adcIntNum can take the value **ADC_INT_NUMBER1**, **ADC_INT_NUMBER2**, **ADC_INT_NUMBER3**, or **ADC_INT_NUMBER4** to express which of the four interrupts of the ADC module should be disabled.

Returns
None.

5.2.3.33 static void ADC_setInterruptSource (uint32_t *base*, **ADC_IntNumber** *adcIntNum*, **ADC_SOCNumber** *socNumber*) [inline], [static]

Sets the source EOC for an analog-to-digital converter interrupt.

Parameters

base	is the base address of the ADC module.
adcIntNum	is interrupt number within the ADC wrapper.
socNumber	is the number of the start-of-conversion.

This function sets which conversion is the source of an ADC interrupt.

The *socNumber* number is a value **ADC_SOC_NUMBERX** where X is a number from 0 to 15 specifying which EOC is to be configured on the ADC module specified by *base*.

adcIntNum can take the value **ADC_INT_NUMBER1**, **ADC_INT_NUMBER2**, **ADC_INT_NUMBER3**, or **ADC_INT_NUMBER4** to express which of the four interrupts of the ADC module is being configured.

Returns

None.

5.2.3.34 static void ADC_enableContinuousMode (uint32_t *base,* **ADC_IntNumber** *adcIntNum*) [inline], [static]

Enables continuous mode for an ADC interrupt.

Parameters

base	is the base address of the ADC.
adcIntNum	is interrupt number within the ADC wrapper.

This function enables continuous mode for the ADC interrupt passed into *adcIntNum*. This means that pulses will be generated for the specified ADC interrupt whenever an EOC pulse is generated irrespective of whether or not the flag bit is set.

adcIntNum can take the value **ADC_INT_NUMBER1**, **ADC_INT_NUMBER2**, **ADC_INT_NUMBER3**, or **ADC_INT_NUMBER4** to express which of the four interrupts of the ADC module is being configured.

Returns

None.

5.2.3.35 static void ADC_disableContinuousMode (uint32_t *base,* **ADC_IntNumber** *adcIntNum*) [inline], [static]

Disables continuous mode for an ADC interrupt.

Parameters

base	is the base address of the ADC.
adcIntNum	is interrupt number within the ADC wrapper.

This function disables continuous mode for the ADC interrupt passed into *adcIntNum*. This means that pulses will not be generated for the specified ADC interrupt until the corresponding interrupt flag for the previous interrupt occurrence has been cleared using ADC_clearInterruptStatus().

adcIntNum can take the value **ADC_INT_NUMBER1**, **ADC_INT_NUMBER2**, **ADC_INT_NUMBER3**, or **ADC_INT_NUMBER4** to express which of the four interrupts of the ADC module is being configured.

Returns

None.

5.2.3.36 static int16_t ADC_getTemperatureC (uint16_t *tempResult,* float32_t *vref*) [inline], [static]

Converts temperature from sensor reading to degrees C

Parameters

tempResult	is the raw ADC A conversion result from the temp sensor.
vref	is the reference voltage being used (for example 3.3 for 3.3V).

This function converts temperature from temp sensor reading to degrees C. Temp sensor values in production test are derived with 2.5V reference. The **vref** argument in the function is used to scale the temp sensor reading accordingly if temp sensor value is read at a different VREF setting.

Returns

Returns the temperature sensor reading converted to degrees C.

5.2.3.37 static int16_t ADC_getTemperatureK (uint16_t *tempResult,* float32_t *vref*) `[inline]`, `[static]`

Converts temperature from sensor reading to degrees K

Parameters

tempResult	is the raw ADC A conversion result from the temp sensor.
vref	is the reference voltage being used (for example 3.3 for 3.3V).

This function converts temperature from temp sensor reading to degrees K. Temp sensor values in production test are derived with 2.5V reference. The **vref** argument in the function is used to scale the temp sensor reading accordingly if temp sensor value is read at a different VREF setting.

Returns

Returns the temperature sensor reading converted to degrees K.

5.2.3.38 void ADC_setMode (uint32_t *base,* **ADC_Resolution** *resolution,* **ADC_SignalMode** *signalMode*)

Configures the analog-to-digital converter resolution and signal mode.

Parameters

base	is the base address of the ADC module.
resolution	is the resolution of the converter (12 or 16 bits).
signalMode	is the input signal mode of the converter.

This function configures the ADC module's conversion resolution and input signal mode and ensures that the corresponding trims are loaded.

The *resolution* parameter specifies the resolution of the conversion. It can be 12-bit or 16-bit specified by **ADC_RESOLUTION_12BIT** or **ADC_RESOLUTION_16BIT**.

The *signalMode* parameter specifies the signal mode. In single-ended mode, which is indicated by **ADC_MODE_SINGLE_ENDED**, the input voltage is sampled on a single pin referenced to VREFLO. In differential mode, which is indicated by **ADC_MODE_DIFFERENTIAL**, the input voltage to the converter is sampled on a pair of input pins, a positive and a negative.

Note: In this device, single-ended signal conversions are supported only in 12-bit resolution mode and differential signal conversions are supported only in 16-bit resolution mode.

Returns

None.

References ADC_MODE_DIFFERENTIAL, ADC_MODE_SINGLE_ENDED, ADC_RESOLUTION_12BIT, and ADC_RESOLUTION_16BIT.

5.2.3.39 void ADC_setPPBTripLimits (uint32_t *base,* **ADC_PPBNumber** *ppbNumber,* int32_t *tripHiLimit,* int32_t *tripLoLimit*)

Sets the windowed trip limits for a PPB.

Parameters

base	is the base address of the ADC module.
ppbNumber	is the number of the post-processing block.
tripHiLimit	is the value is the digital comparator trip high limit.
tripLoLimit	is the value is the digital comparator trip low limit.

This function sets the windowed trip limits for a PPB. These values set the digital comparator so that when one of the values is exceeded, either a high or low trip event will occur.

The *ppbNumber* is a value **ADC_PPB_NUMBERX** where X is a value from 1 to 4 inclusive that identifies a PPB to be configured.

If using 16-bit mode, you may pass a 17-bit number into the *tripHiLimit* and *tripLoLimit* parameters where the 17th bit is the sign bit (that is a value from -65536 and 65535). In 12-bit mode, only bits 12:0 will be compared against bits 12:0 of the PPB result.

Note

On some devices, signed trip values do not work properly. See the silicon errata for details.

Returns

None.

6 ASysCtl Module

6.1 ASysCtl Introduction

The ASysCtl or Analog System Control driver provides functions to enable, disable and lock the temperature sensor on the device. It will also provide additional functionality if available for that device.

6.2 API Functions

Functions

- static void ASysCtl_enableTemperatureSensor (void)
- static void ASysCtl_disableTemperatureSensor (void)
- static void ASysCtl_lockTemperatureSensor (void)

6.2.1 Detailed Description

The code for this module is contained in `driverlib/asysctl.c`, with `driverlib/asysctl.h` containing the API declarations for use by applications.

6.2.2 Function Documentation

6.2.2.1 static void ASysCtl_enableTemperatureSensor (void) `[inline]`, `[static]`

Enable temperature sensor.

This function enables the temperature sensor output to the ADC.

Returns
None.

6.2.2.2 static void ASysCtl_disableTemperatureSensor (void) `[inline]`, `[static]`

Disable temperature sensor.

This function disables the temperature sensor output to the ADC.

Returns
None.

6.2.2.3 static void ASysCtl_lockTemperatureSensor (void) [inline], [static]

Locks the temperature sensor control register.

Returns
None.

7 CAN Module

7.1 CAN Introduction

The controller area network (CAN) API provides a set of functions for configuring and using the CAN module, a serial communications protocol. Functions are provided to setup and configure the module operating options, setup the different types of message objects, send and read messages, and setup and handle interrupts and events.

7.2 API Functions

Enumerations

- enum CAN_MsgFrameType { CAN_MSG_FRAME_STD, CAN_MSG_FRAME_EXT }
- enum CAN_MsgObjType { CAN_MSG_OBJ_TYPE_TX, CAN_MSG_OBJ_TYPE_TX_REMOTE, CAN_MSG_OBJ_TYPE_RX, CAN_MSG_OBJ_TYPE_RXTX_REMOTE }
- enum CAN_ClockSource { CAN_CLOCK_SOURCE_SYS, CAN_CLOCK_SOURCE_XTAL, CAN_CLOCK_SOURCE_AUX }

Functions

- static void CAN_initRAM (uint32_t base)
- static void CAN_selectClockSource (uint32_t base, CAN_ClockSource source)
- static void CAN_startModule (uint32_t base)
- static void CAN_enableController (uint32_t base)
- static void CAN_disableController (uint32_t base)
- static void CAN_enableTestMode (uint32_t base, uint16_t mode)
- static void CAN_disableTestMode (uint32_t base)
- static uint32_t CAN_getBitTiming (uint32_t base)
- static void CAN_enableMemoryAccessMode (uint32_t base)
- static void CAN_disableMemoryAccessMode (uint32_t base)
- static void CAN_setInterruptionDebugMode (uint32_t base, bool enable)
- static void CAN_disableAutoBusOn (uint32_t base)
- static void CAN_enableAutoBusOn (uint32_t base)
- static void CAN_setAutoBusOnTime (uint32_t base, uint32_t time)
- static void CAN_enableInterrupt (uint32_t base, uint32_t intFlags)
- static void CAN_disableInterrupt (uint32_t base, uint32_t intFlags)
- static uint32_t CAN_getInterruptMux (uint32_t base)
- static void CAN_setInterruptMux (uint32_t base, uint32_t mux)
- static void CAN_enableRetry (uint32_t base)
- static void CAN_disableRetry (uint32_t base)
- static bool CAN_isRetryEnabled (uint32_t base)
- static bool CAN_getErrorCount (uint32_t base, uint32_t *rxCount, uint32_t *txCount)
- static uint16_t CAN_getStatus (uint32_t base)

- static uint32_t CAN_getTxRequests (uint32_t base)
- static uint32_t CAN_getNewDataFlags (uint32_t base)
- static uint32_t CAN_getValidMessageObjects (uint32_t base)
- static uint32_t CAN_getInterruptCause (uint32_t base)
- static uint32_t CAN_getInterruptMessageSource (uint32_t base)
- static void CAN_enableGlobalInterrupt (uint32_t base, uint16_t intFlags)
- static void CAN_disableGlobalInterrupt (uint32_t base, uint16_t intFlags)
- static void CAN_clearGlobalInterruptStatus (uint32_t base, uint16_t intFlags)
- static bool CAN_getGlobalInterruptStatus (uint32_t base, uint16_t intFlags)
- void CAN_initModule (uint32_t base)
- void CAN_setBitRate (uint32_t base, uint32_t clock, uint32_t bitRate, uint16_t bitTime)
- void CAN_setBitTiming (uint32_t base, uint16_t prescaler, uint16_t prescalerExtension, uint16_t tSeg1, uint16_t tSeg2, uint16_t sjw)
- void CAN_clearInterruptStatus (uint32_t base, uint32_t intClr)
- void CAN_setupMessageObject (uint32_t base, uint32_t objID, uint32_t msgID, CAN_MsgFrameType frame, CAN_MsgObjType msgType, uint32_t msgIDMask, uint32_t flags, uint16_t msgLen)
- void CAN_sendMessage (uint32_t base, uint32_t objID, uint16_t msgLen, const uint16_t ∗msgData)
- bool CAN_readMessage (uint32_t base, uint32_t objID, uint16_t ∗msgData)
- void CAN_clearMessage (uint32_t base, uint32_t objID)

7.2.1 Detailed Description

The following describes important details and recommendations when using the CAN API.

Once system control enables the CAN module, **CAN_initModule()** needs to be called with the desired CAN module base to put the controller in the init state, initialize the message RAM, and enable access to the configuration registers. Next, use **CAN_setBitRate()** to set the CAN bit timing values for the bit rate and timing parameters. For tighter timing requirements, use **CAN_setBitTiming()** instead.

To setup any of the types of message objects, use **CAN_setupMessageObject()**.

Once all of the module configurations are setup, **CAN_startModule()** starts the CAN module's operations and disables access to the configuration registers.

If the application needs to disable message processing on the CAN controller, use **CAN_disableController()** to disable the message processing. Message processing can be re-enabled using **CAN_enableController()**.

The code for this module is contained in `driverlib/can.c`, with `driverlib/can.h` containing the API declarations for use by applications.

7.2.2 Enumeration Type Documentation

7.2.2.1 enum **CAN_MsgFrameType**

This data type is used to identify the interrupt status register. This is used when calling the CAN_setupMessageObject() function.

Enumerator

CAN_MSG_FRAME_STD Set the message ID frame to standard.

CAN_MSG_FRAME_EXT Set the message ID frame to extended.

7.2.2.2 enum **CAN_MsgObjType**

This definition is used to determine the type of message object that will be set up via a call to the CAN_setupMessageObject() API.

Enumerator

CAN_MSG_OBJ_TYPE_TX Transmit message object.

CAN_MSG_OBJ_TYPE_TX_REMOTE Transmit remote request message object.

CAN_MSG_OBJ_TYPE_RX Receive message object.

CAN_MSG_OBJ_TYPE_RXTX_REMOTE Remote frame receive remote, with auto-transmit message object.

7.2.2.3 enum **CAN_ClockSource**

This definition is used to determine the clock source that will be set up via a call to the CAN_selectClockSource() API.

Enumerator

CAN_CLOCK_SOURCE_SYS Peripheral System Clock Source.

CAN_CLOCK_SOURCE_XTAL External Oscillator Clock Source.

CAN_CLOCK_SOURCE_AUX Auxiliary Clock Input Source.

7.2.3 Function Documentation

7.2.3.1 static void CAN_initRAM (uint32_t *base*) [inline], [static]

Initializes the CAN controller's RAM.

Parameters

base	is the base address of the CAN controller.

Performs the initialization of the RAM used for the CAN message objects.

Returns

None.

Referenced by CAN_initModule().

7.2.3.2 static void CAN_selectClockSource (uint32_t *base*, **CAN_ClockSource** *source*) [inline], [static]

Select CAN Clock Source

Parameters

base	is the base address of the CAN controller.
source	is the clock source to use for the CAN controller.

This function selects the specified clock source for the CAN controller.

The *source* parameter can be any one of the following:

- **CAN_CLOCK_SOURCE_SYS** - Peripheral System Clock
- **CAN_CLOCK_SOURCE_XTAL** - External Oscillator
- **CAN_CLOCK_SOURCE_AUX** - Auxiliary Clock Input from GPIO

Returns
None.

7.2.3.3 static void CAN_startModule (uint32_t *base*) [inline], [static]

Starts the CAN Module's Operations

Parameters

base	is the base address of the CAN controller.

This function starts the CAN module's operations after initialization, which includes the CAN protocol controller state machine of the CAN core and the message handler state machine to begin controlling the CAN's internal data flow.

Returns
None.

7.2.3.4 static void CAN_enableController (uint32_t *base*) [inline], [static]

Enables the CAN controller.

Parameters

base	is the base address of the CAN controller to enable.

Enables the CAN controller for message processing. Once enabled, the controller will automatically transmit any pending frames, and process any received frames. The controller can be stopped by calling CAN_disableController().

Returns
None.

7.2.3.5 static void CAN_disableController (uint32_t *base*) [inline], [static]

Disables the CAN controller.

Parameters

base	is the base address of the CAN controller to disable.

Disables the CAN controller for message processing. When disabled, the controller will no longer automatically process data on the CAN bus. The controller can be restarted by calling CAN_enableController(). The state of the CAN controller and the message objects in the controller are left as they were before this call was made.

Returns

None.

7.2.3.6 static void CAN_enableTestMode (uint32_t *base,* uint16_t *mode*) `[inline]`, `[static]`

Enables the test modes of the CAN controller.

Parameters

base	is the base address of the CAN controller.
mode	are the the test modes to enable.

Enables test modes within the controller. The following valid options for *mode* can be OR'ed together:

- **CAN_TEST_SILENT** - Silent Mode
- **CAN_TEST_LBACK** - Loopback Mode
- **CAN_TEST_EXL** - External Loopback Mode

Note

Loopback mode and external loopback mode **can not** be enabled at the same time.

Returns

None.

7.2.3.7 static void CAN_disableTestMode (uint32_t *base*) `[inline]`, `[static]`

Disables the test modes of the CAN controller.

Parameters

base	is the base address of the CAN controller.

Disables test modes within the controller and clears the test bits.

Returns

None.

7.2.3.8 static uint32_t CAN_getBitTiming (uint32_t *base*) `[inline]`, `[static]`

Get the current settings for the CAN controller bit timing.

Parameters

base	is the base address of the CAN controller.

This function reads the current configuration of the CAN controller bit clock timing.

Returns

Returns the value of the bit timing register.

7.2.3.9 static void CAN_enableMemoryAccessMode (uint32_t *base*) [inline], [static]

Enables direct access to the RAM.

Parameters

base	is the base address of the CAN controller.

Enables direct access to the RAM while in Test mode.

Note

Test Mode must first be enabled to use this function.

Returns

None.

7.2.3.10 static void CAN_disableMemoryAccessMode (uint32_t *base*) [inline], [static]

Disables direct access to the RAM.

Parameters

base	is the base address of the CAN controller.

Disables direct access to the RAM while in Test mode.

Returns

None.

7.2.3.11 static void CAN_setInterruptionDebugMode (uint32_t *base,* bool *enable*) [inline], [static]

Sets the interruption debug mode of the CAN controller.

Parameters

base	is the base address of the CAN controller.

enable	is a flag to enable or disable the interruption debug mode.

This function sets the interruption debug mode of the CAN controller. When the *enable* parameter is **true**, CAN will be configured to interrupt any transmission or reception and enter debug mode immediately after it is requested. When **false**, CAN will wait for a started transmission or reception to be completed before entering debug mode.

Returns

None.

7.2.3.12 static void CAN_disableAutoBusOn (uint32_t *base*) `[inline]`, `[static]`

Disables Auto-Bus-On.

Parameters

base	is the base address of the CAN controller.

Disables the Auto-Bus-On feature of the CAN controller.

Returns

None.

7.2.3.13 static void CAN_enableAutoBusOn (uint32_t *base*) `[inline]`, `[static]`

Enables Auto-Bus-On.

Parameters

base	is the base address of the CAN controller.

Enables the Auto-Bus-On feature of the CAN controller. Be sure to also configure the Auto-Bus-On time using the CAN_setAutoBusOnTime function.

Returns

None.

7.2.3.14 static void CAN_setAutoBusOnTime (uint32_t *base,* uint32_t *time*) `[inline]`, `[static]`

Sets the time before a Bus-Off recovery sequence is started.

Parameters

base	is the base address of the CAN controller.
time	is number of clock cycles before a Bus-Off recovery sequence is started.

This function sets the number of clock cycles before a Bus-Off recovery sequence is started by clearing the Init bit.

Note

To enable this functionality, use CAN_enableAutoBusOn().

Returns
None.

7.2.3.15 static void CAN_enableInterrupt (uint32_t *base,* uint32_t *intFlags*) [inline], [static]

Enables individual CAN controller interrupt sources.

Parameters

base	is the base address of the CAN controller.
intFlags	is the bit mask of the interrupt sources to be enabled.

Enables specific interrupt sources of the CAN controller. Only enabled sources will cause a processor interrupt.

The *intFlags* parameter is the logical OR of any of the following:

- **CAN_INT_ERROR** - a controller error condition has occurred
- **CAN_INT_STATUS** - a message transfer has completed, or a bus error has been detected
- **CAN_INT_IE0** - allow CAN controller to generate interrupts on interrupt line 0
- **CAN_INT_IE1** - allow CAN controller to generate interrupts on interrupt line 1

Returns
None.

7.2.3.16 static void CAN_disableInterrupt (uint32_t *base,* uint32_t *intFlags*) [inline], [static]

Disables individual CAN controller interrupt sources.

Parameters

base	is the base address of the CAN controller.
intFlags	is the bit mask of the interrupt sources to be disabled.

Disables the specified CAN controller interrupt sources. Only enabled interrupt sources can cause a processor interrupt.

The *intFlags* parameter has the same definition as in the CAN_enableInterrupt() function.

Returns
None.

7.2.3.17 static uint32_t CAN_getInterruptMux (uint32_t *base*) [inline], [static]

Get the CAN controller Interrupt Line set for each mailbox

Parameters

base	is the base address of the CAN controller.

Gets which interrupt line each message object should assert when an interrupt occurs. Bit 0 corresponds to message object 32 and then bits 1 to 31 correspond to message object 1 through 31 respectively. Bits that are asserted indicate the message object should generate an interrupt on interrupt line 1, while bits that are not asserted indicate the message object should generate an interrupt on line 0.

Returns

Returns the value of the interrupt muxing register.

7.2.3.18 static void CAN_setInterruptMux (uint32_t *base*, uint32_t *mux*) `[inline]`, `[static]`

Set the CAN controller Interrupt Line for each mailbox

Parameters

base	is the base address of the CAN controller.
mux	bit packed representation of which message objects should generate an interrupt on a given interrupt line.

Selects which interrupt line each message object should assert when an interrupt occurs. Bit 0 corresponds to message object 32 and then bits 1 to 31 correspond to message object 1 through 31 respectively. Bits that are asserted indicate the message object should generate an interrupt on interrupt line 1, while bits that are not asserted indicate the message object should generate an interrupt on line 0.

Returns

None.

7.2.3.19 static void CAN_enableRetry (uint32_t *base*) `[inline]`, `[static]`

Enables the CAN controller automatic retransmission behavior.

Parameters

base	is the base address of the CAN controller.

Enables the automatic retransmission of messages with detected errors.

Returns

None.

7.2.3.20 static void CAN_disableRetry (uint32_t *base*) `[inline]`, `[static]`

Disables the CAN controller automatic retransmission behavior.

Parameters

base	is the base address of the CAN controller.

Disables the automatic retransmission of messages with detected errors.

Returns
None.

7.2.3.21 static bool CAN_isRetryEnabled (uint32_t *base*) [inline], [static]

Returns the current setting for automatic retransmission.

Parameters

base	is the base address of the CAN controller.

Reads the current setting for the automatic retransmission in the CAN controller and returns it to the caller.

Returns
Returns **true** if automatic retransmission is enabled, **false** otherwise.

7.2.3.22 static bool CAN_getErrorCount (uint32_t *base,* uint32_t * *rxCount,* uint32_t * *txCount*) [inline], [static]

Reads the CAN controller error counter register.

Parameters

base	is the base address of the CAN controller.
rxCount	is a pointer to storage for the receive error counter.
txCount	is a pointer to storage for the transmit error counter.

Reads the error counter register and returns the transmit and receive error counts to the caller along with a flag indicating if the controller receive counter has reached the error passive limit. The values of the receive and transmit error counters are returned through the pointers provided as parameters.

After this call, *rxCount* will hold the current receive error count and *txCount* will hold the current transmit error count.

Returns
Returns **true** if the receive error count has reached the error passive limit, and **false** if the error count is below the error passive limit.

7.2.3.23 static uint16_t CAN_getStatus (uint32_t *base*) [inline], [static]

Reads the CAN controller error and status register.

Parameters

base	is the base address of the CAN controller.

Reads the error and status register of the CAN controller.

Returns

Returns the value of the register.

7.2.3.24 static uint32_t CAN_getTxRequests (uint32_t *base*) `[inline]`, `[static]`

Reads the CAN controller TX request register.

Parameters

base	is the base address of the CAN controller.

Reads the TX request register of the CAN controller.

Returns

Returns the value of the register.

7.2.3.25 static uint32_t CAN_getNewDataFlags (uint32_t *base*) `[inline]`, `[static]`

Reads the CAN controller new data status register.

Parameters

base	is the base address of the CAN controller.

Reads the new data status register of the CAN controller for all message objects.

Returns

Returns the value of the register.

7.2.3.26 static uint32_t CAN_getValidMessageObjects (uint32_t *base*) `[inline]`, `[static]`

Reads the CAN controller valid message object register.

Parameters

base	is the base address of the CAN controller.

Reads the valid message object register of the CAN controller.

Returns

Returns the value of the register.

7.2.3.27 static uint32_t CAN_getInterruptCause (uint32_t *base*) `[inline]`, `[static]`

Get the CAN controller interrupt cause.

Parameters

base	is the base address of the CAN controller.

This function returns the value of the interrupt register that indicates the cause of the interrupt.

Returns

Returns the value of the interrupt register.

7.2.3.28 static uint32_t CAN_getInterruptMessageSource (uint32_t *base*) [inline], [static]

Get the CAN controller pending interrupt message source.

Parameters

base	is the base address of the CAN controller.

Returns the value of the pending interrupts register that indicates which messages are the source of pending interrupts.

Returns

Returns the value of the pending interrupts register.

7.2.3.29 static void CAN_enableGlobalInterrupt (uint32_t *base*, uint16_t *intFlags*) [inline], [static]

CAN Global interrupt Enable function.

Parameters

base	is the base address of the CAN controller.
intFlags	is the bit mask of the interrupt sources to be enabled.

Enables specific CAN interrupt in the global interrupt enable register

The *intFlags* parameter is the logical OR of any of the following:

- **CAN_GLOBAL_INT_CANINT0** - Global Interrupt Enable bit for CAN INT0
- **CAN_GLOBAL_INT_CANINT1** - Global Interrupt Enable bit for CAN INT1

Returns

None.

7.2.3.30 static void CAN_disableGlobalInterrupt (uint32_t *base*, uint16_t *intFlags*) [inline], [static]

CAN Global interrupt Disable function.

Parameters

base	is the base address of the CAN controller.
intFlags	is the bit mask of the interrupt sources to be disabled.

Disables the specific CAN interrupt in the global interrupt enable register

The *intFlags* parameter is the logical OR of any of the following:

- **CAN_GLOBAL_INT_CANINT0** - Global Interrupt bit for CAN INT0
- **CAN_GLOBAL_INT_CANINT1** - Global Interrupt bit for CAN INT1

Returns
None.

7.2.3.31 static void CAN_clearGlobalInterruptStatus (uint32_t *base,* uint16_t *intFlags*) [inline], [static]

CAN Global interrupt Clear function.

Parameters

base	is the base address of the CAN controller.
intFlags	is the bit mask of the interrupt sources to be cleared.

Clear the specific CAN interrupt bit in the global interrupt flag register.

The *intFlags* parameter is the logical OR of any of the following:

- **CAN_GLOBAL_INT_CANINT0** - Global Interrupt bit for CAN INT0
- **CAN_GLOBAL_INT_CANINT1** - Global Interrupt bit for CAN INT1

Returns
None.

7.2.3.32 static bool CAN_getGlobalInterruptStatus (uint32_t *base,* uint16_t *intFlags*) [inline], [static]

Get the CAN Global Interrupt status.

Parameters

base	is the base address of the CAN controller.
intFlags	is the bit mask of the interrupt sources to be enabled.

Check if any interrupt bit is set in the global interrupt flag register.

The *intFlags* parameter is the logical OR of any of the following:

- **CAN_GLOBAL_INT_CANINT0** - Global Interrupt bit for CAN INT0
- **CAN_GLOBAL_INT_CANINT1** - Global Interrupt bit for CAN INT1

Returns
True if any of the requested interrupt bits are set. False, if none of the requested bits are set.

7.2.3.33 void CAN_initModule (uint32_t *base*)

Initializes the CAN controller

Parameters

base	is the base address of the CAN controller.

This function initializes the message RAM, which also clears all the message objects, and places the CAN controller in an init state. Write access to the configuration registers is available as a result, allowing the bit timing and message objects to be setup.

Note

To exit the initialization mode and start the CAN module, use the CAN_startModule() function.

Returns

None.

References CAN_initRAM(), and SysCtl_delay().

7.2.3.34 void CAN_setBitRate (uint32_t *base,* uint32_t *clock,* uint32_t *bitRate,* uint16_t *bitTime*)

Sets the CAN Bit Timing based on requested Bit Rate.

Parameters

base	is the base address of the CAN controller.
clock	is the CAN module clock frequency before the bit rate prescaler (Hertz)
bitRate	is the desired bit rate (bits/sec)
bitTime	is the number of time quanta per bit required for desired bit time (Tq) and must be in the range from 8 to 25

This function sets the CAN bit timing values for the bit rate passed in the *bitRate* and *bitTime* parameters based on the *clock* parameter. The CAN bit clock is calculated to be an average timing value that should work for most systems. If tighter timing requirements are needed, then the CAN_setBitTiming() function is available for full customization of all of the CAN bit timing values.

Note

The CANBTR register values calculated by the function CAN_setBitRate may not be suitable for your network parameters. If this is the case and you have computed the correct values for your network, you could directly write those parameters in CANBTR register using the function CAN_setBitTiming.

Returns

None.

References CAN_setBitTiming().

7.2.3.35 void CAN_setBitTiming (uint32_t *base,* uint16_t *prescaler,* uint16_t *prescalerExtension,* uint16_t *tSeg1,* uint16_t *tSeg2,* uint16_t *sjw*)

Manually set the CAN controller bit timing.

Parameters

base	is the base address of the CAN controller.
prescaler	is the baud rate prescaler
prescalerExtension	is the baud rate prescaler extension
tSeg1	is the time segment 1
tSeg2	is the time segment 2
sjw	is the synchronization jump width

This function sets the various timing parameters for the CAN bus bit timing: baud rate prescaler, prescaler extension, time segment 1, time segment 2, and the Synchronization Jump Width.

Returns
None.

Referenced by CAN_setBitRate().

7.2.3.36 void CAN_clearInterruptStatus (uint32_t *base,* uint32_t *intClr*)

Clears a CAN interrupt source.

Parameters

base	is the base address of the CAN controller.
intClr	is a value indicating which interrupt source to clear.

This function can be used to clear a specific interrupt source. The *intClr* parameter should be either a number from 1 to 32 to clear a specific message object interrupt or can be the following:

- **CAN_INT_INT0ID_STATUS** - Clears a status interrupt.

It is not necessary to use this function to clear an interrupt. This should only be used if the application wants to clear an interrupt source without taking the normal interrupt action.

Returns
None.

7.2.3.37 void CAN_setupMessageObject (uint32_t *base,* uint32_t *objID,* uint32_t *msgID,* **CAN_MsgFrameType** *frame,* **CAN_MsgObjType** *msgType,* uint32_t *msgIDMask,* uint32_t *flags,* uint16_t *msgLen*)

Setup a Message Object

Parameters

base	is the base address of the CAN controller.
objID	is the message object number to configure (1-32).
msgID	is the CAN message identifier used for the 11 or 29 bit identifiers

frame	is the CAN ID frame type
msgType	is the message object type
msgIDMask	is the CAN message identifier mask used when identifier filtering is enabled
flags	is the various flags and settings to be set for the message object
msgLen	is the number of bytes of data in the message object (0-8)

This function sets the various values required for a message object.

The *frame* parameter can be one of the following values:

- **CAN_MSG_FRAME_STD** - Standard 11 bit identifier
- **CAN_MSG_FRAME_EXT** - Extended 29 bit identifier

The *msgType* parameter can be one of the following values:

- **CAN_MSG_OBJ_TYPE_TX** - Transmit Message
- **CAN_MSG_OBJ_TYPE_TX_REMOTE** - Transmit Remote Message
- **CAN_MSG_OBJ_TYPE_RX** - Receive Message
- **CAN_MSG_OBJ_TYPE_RXTX_REMOTE** - Receive Remote message with auto-transmit

The *flags* parameter can be set as **CAN_MSG_OBJ_NO_FLAGS** if no flags are required or the parameter can be a logical OR of any of the following values:

- **CAN_MSG_OBJ_TX_INT_ENABLE** - Enable Transmit Interrupts
- **CAN_MSG_OBJ_RX_INT_ENABLE** - Enable Receive Interrupts
- **CAN_MSG_OBJ_USE_ID_FILTER** - Use filtering based on the Message ID
- **CAN_MSG_OBJ_USE_EXT_FILTER** - Use filtering based on the Extended Message ID
- **CAN_MSG_OBJ_USE_DIR_FILTER** - Use filtering based on the direction of the transfer
- **CAN_MSG_OBJ_FIFO** - Message object is part of a FIFO structure and isn't the final message object in FIFO

Note

The **msgLen** Parameter for the Receive Message Object is a "don't care" but its value should be between 0-8 due to the assert.

Returns

None.

References CAN_MSG_FRAME_EXT, CAN_MSG_OBJ_TYPE_RXTX_REMOTE, and CAN_MSG_OBJ_TYPE_TX.

7.2.3.38 void CAN_sendMessage (uint32_t *base,* uint32_t *objID,* uint16_t *msgLen,* const uint16_t ∗ *msgData*)

Sends a Message Object

Parameters

base	is the base address of the CAN controller.
objID	is the object number to configure (1-32).
msgLen	is the number of bytes of data in the message object (0-8)
msgData	is a pointer to the message object's data

This function is used to transmit a message object and the message data, if applicable.

Note

The message object requested by the *objID* must first be setup using the CAN_setupMessageObject() function.

Returns

None.

7.2.3.39 bool CAN_readMessage (uint32_t *base,* uint32_t *objID,* uint16_t * *msgData*)

Reads the data in a Message Object

Parameters

base	is the base address of the CAN controller.
objID	is the object number to read (1-32).
msgData	is a pointer to the array to store the message data

This function is used to read the data contents of the specified message object in the CAN controller. The data returned is stored in the *msgData* parameter.

Note

1. The message object requested by the *objID* must first be setup using the CAN_setupMessageObject() function.
2. If the DLC of the received message is larger than the *msgData* buffer provided, then it is possible for a buffer overflow to occur.

Returns

Returns **true** if new data was retrieved, else returns **false** to indicate no new data was retrieved.

7.2.3.40 void CAN_clearMessage (uint32_t *base,* uint32_t *objID*)

Clears a message object so that it is no longer used.

Parameters

base	is the base address of the CAN controller.
objID	is the message object number to disable (1-32).

This function frees the specified message object from use. Once a message object has been cleared, it will no longer automatically send or receive messages, or generate interrupts.

Returns

None.

8 CLA Module

8.1 CLA Introduction

The Control Law Accelerator (CLA) API provides a set of functions to configure the CLA. The CLA is an independent accelerator with its own buses, ALU and register set. It does share memory, both program and data, with the main processor; it comes out of a power reset with no memory assets and therefore the C28x must configure how the CLA runs, which memory spaces it uses, and when code must run.

The primary use of the CLA is to implement small, fast control loops that run periodically, responding to specific trigger sources like the PWM or an ADC conversion in a deterministic (fixed and low latency) fashion.

8.2 API Functions

Macros

- #define CLA_TASKFLAG_1
- #define CLA_TASKFLAG_2
- #define CLA_TASKFLAG_3
- #define CLA_TASKFLAG_4
- #define CLA_TASKFLAG_5
- #define CLA_TASKFLAG_6
- #define CLA_TASKFLAG_7
- #define CLA_TASKFLAG_8
- #define CLA_TASKFLAG_ALL

Enumerations

- enum CLA_TaskNumber {
  CLA_TASK_1, CLA_TASK_2, CLA_TASK_3, CLA_TASK_4,
  CLA_TASK_5, CLA_TASK_6, CLA_TASK_7, CLA_TASK_8 }
- enum CLA_MVECTNumber {
  CLA_MVECT_1, CLA_MVECT_2, CLA_MVECT_3, CLA_MVECT_4,
  CLA_MVECT_5, CLA_MVECT_6, CLA_MVECT_7, CLA_MVECT_8 }
- enum CLA_Trigger {
  CLA_TRIGGER_SOFTWARE, CLA_TRIGGER_ADCA1, CLA_TRIGGER_ADCA2,
  CLA_TRIGGER_ADCA3,
  CLA_TRIGGER_ADCA4, CLA_TRIGGER_ADCAEVT, CLA_TRIGGER_ADCB1,
  CLA_TRIGGER_ADCB2,
  CLA_TRIGGER_ADCB3, CLA_TRIGGER_ADCB4, CLA_TRIGGER_ADCBEVT,
  CLA_TRIGGER_ADCC1,
  CLA_TRIGGER_ADCC2, CLA_TRIGGER_ADCC3, CLA_TRIGGER_ADCC4,

CLA_TRIGGER_ADCCEVT,
CLA_TRIGGER_ADCD1, CLA_TRIGGER_ADCD2, CLA_TRIGGER_ADCD3,
CLA_TRIGGER_ADCD4,
CLA_TRIGGER_ADCDEVT, CLA_TRIGGER_XINT1, CLA_TRIGGER_XINT2,
CLA_TRIGGER_XINT3,
CLA_TRIGGER_XINT4, CLA_TRIGGER_XINT5, CLA_TRIGGER_EPWM1INT,
CLA_TRIGGER_EPWM2INT,
CLA_TRIGGER_EPWM3INT, CLA_TRIGGER_EPWM4INT, CLA_TRIGGER_EPWM5INT,
CLA_TRIGGER_EPWM6INT,
CLA_TRIGGER_EPWM7INT, CLA_TRIGGER_EPWM8INT, CLA_TRIGGER_EPWM9INT,
CLA_TRIGGER_EPWM10INT,
CLA_TRIGGER_EPWM11INT, CLA_TRIGGER_EPWM12INT, CLA_TRIGGER_TINT0,
CLA_TRIGGER_TINT1,
CLA_TRIGGER_TINT2, CLA_TRIGGER_MXINTA, CLA_TRIGGER_MRINTA,
CLA_TRIGGER_MXINTB,
CLA_TRIGGER_MRINTB, CLA_TRIGGER_ECAP1INT, CLA_TRIGGER_ECAP2INT,
CLA_TRIGGER_ECAP3INT,
CLA_TRIGGER_ECAP4INT, CLA_TRIGGER_ECAP5INT, CLA_TRIGGER_ECAP6INT,
CLA_TRIGGER_EQEP1INT,
CLA_TRIGGER_EQEP2INT, CLA_TRIGGER_EQEP3INT, CLA_TRIGGER_SDFM1INT,
CLA_TRIGGER_SDFM2INT,
CLA_TRIGGER_UPP1INT, CLA_TRIGGER_SPITXAINT, CLA_TRIGGER_SPIRXAINT,
CLA_TRIGGER_SPITXBINT,
CLA_TRIGGER_SPIRXBINT, CLA_TRIGGER_SPITXCINT, CLA_TRIGGER_SPIRXCINT }

Functions

- static void CLA_mapTaskVector (uint32_t base, CLA_MVECTNumber claIntVect, uint16_t claTaskAddr)
- static void CLA_performHardReset (uint32_t base)
- static void CLA_performSoftReset (uint32_t base)
- static void CLA_enableIACK (uint32_t base)
- static void CLA_disableIACK (uint32_t base)
- static bool CLA_getPendingTaskFlag (uint32_t base, CLA_TaskNumber taskNumber)
- static uint16_t CLA_getAllPendingTaskFlags (uint32_t base)
- static bool CLA_getTaskOverflowFlag (uint32_t base, CLA_TaskNumber taskNumber)
- static uint16_t CLA_getAllTaskOverflowFlags (uint32_t base)
- static void CLA_clearTaskFlags (uint32_t base, uint16_t taskFlags)
- static void CLA_forceTasks (uint32_t base, uint16_t taskFlags)
- static void CLA_enableTasks (uint32_t base, uint16_t taskFlags)
- static void CLA_disableTasks (uint32_t base, uint16_t taskFlags)
- static bool CLA_getTaskRunStatus (uint32_t base, CLA_TaskNumber taskNumber)
- static uint16_t CLA_getAllTaskRunStatus (uint32_t base)
- static void CLA_enableSoftwareInterrupt (uint32_t base, uint16_t taskFlags)
- static void CLA_disableSoftwareInterrupt (uint32_t base, uint16_t taskFlags)
- static void CLA_forceSoftwareInterrupt (uint32_t base, uint16_t taskFlags)
- void CLA_setTriggerSource (CLA_TaskNumber taskNumber, CLA_Trigger trigger)

8.2.1 Detailed Description

This module is used for configurating CLA. The next few paragraphs describe configuration options that are accessible via the main processor (the C28x).

The CLA code is broken up into a main background task and a set of 7 tasks, each of which requires a trigger source either from a hardware peripheral or software. Each task begins at an address that is given by its vector register. The vector for the background task can be configured using the **CLA_mapBackgroundTaskVector()**, and the task's vector is set using **CLA_mapTaskVector()**. The trigger source for all the tasks can be set with **CLA_setTriggerSource()**. If using a software trigger, the user must first enable the feature with **CLA_enableIACK()**, and then trigger the task with the assembly instruction,

```
__asm(" IACK #<Task>");
```

Task refers to the task to trigger; it is one less than the actual task. For example, if attempting to trigger task 1 you would issue,

```
__asm(" IACK #0");
```

A task will only start to execute if it is globally enabled. This is done through **CLA_enableTasks()**. Once enabled, a task will respond to a peripheral trigger (if configured to do so), a software force (with the IACK instruction), or through **CLA_forceTasks()**.

In this type of CLA, a background task is always running. It is enabled using **CLA_enableBackgroundTask()** and subsequently kicked off by **CLA_startBackgroundTask()**, or through a peripheral trigger (it takes the same trigger as task 8 on older CLAs). The user may enable the background task peripheral trigger feature using **CLA_enableHardwareTrigger()**.

The tasks (1 to 7) have a fixed priority, with 1 being the highest and 7 the lowest. They will interrupt the background task, when triggered, in priority order. The user may query the status of all tasks with **CLA_getAllTaskRunStatus()** or a particular task with **CLA_getTaskRunStatus()** to determine if its pending, running or idle.

Each task (1 through 7) can issue an interrupt to the main CPU after it completes execution. This is configured through the PIE module, and registering the handler (ISR) for each end-of-task interrupt with **CLA_registerEndOfTaskInterrupt()**.

The CLA can undergo a soft reset with **CLA_performSoftReset()** or emulate a power cycle or hard reset with **CLA_performHardReset()**.

The CLA can access and configure a few configuration registers (the C28x can read but not alter these registers). A task can force another's end-of-task interrupt to the main CPU by enabling that task's software interrupt using **CLA_enableSoftwareInterrupt()** and subsequently forcing it using **CLA_forceSoftwareInterrupt()**. Its important to keep in mind that enabling a software interrupt for a given task disables its ability to generate an interrupt to the main CPU once it completes execution.

The code for this module is contained in `driverlib/cla.c`, with `driverlib/cla.h` containing the API declarations for use by applications.

8.2.2 Enumeration Type Documentation

8.2.2.1 enum **CLA_TaskNumber**

Values that can be passed to CLA_getPendingTaskFlag(), CLA_getTaskOverflowFlag(), CLA_getTaskRunStatus(), CLA_setTriggerSource(), CLA_registerEndOfTaskInterrupt(), and CLA_unregisterEndOfTaskInterrupt() as the taskNumber parameter.

Enumerator

CLA_TASK_1 CLA Task 1.
CLA_TASK_2 CLA Task 2.
CLA_TASK_3 CLA Task 3.
CLA_TASK_4 CLA Task 4.
CLA_TASK_5 CLA Task 5.
CLA_TASK_6 CLA Task 6.
CLA_TASK_7 CLA Task 7.
CLA_TASK_8 CLA Task 8.

8.2.2.2 enum **CLA_MVECTNumber**

Values that can be passed to CLA_mapTaskVector() as the *claIntVect* parameter.

Enumerator

CLA_MVECT_1 Task Interrupt Vector 1.
CLA_MVECT_2 Task Interrupt Vector 2.
CLA_MVECT_3 Task Interrupt Vector 3.
CLA_MVECT_4 Task Interrupt Vector 4.
CLA_MVECT_5 Task Interrupt Vector 5.
CLA_MVECT_6 Task Interrupt Vector 6.
CLA_MVECT_7 Task Interrupt Vector 7.
CLA_MVECT_8 Task Interrupt Vector 8.

8.2.2.3 enum **CLA_Trigger**

Values that can be passed to CLA_setTriggerSource() as the *trigger* parameter.

Enumerator

CLA_TRIGGER_SOFTWARE CLA Task Trigger Source is Software.
CLA_TRIGGER_ADCA1 CLA Task Trigger Source is ADCA1.
CLA_TRIGGER_ADCA2 CLA Task Trigger Source is ADCA2.
CLA_TRIGGER_ADCA3 CLA Task Trigger Source is ADCA3.
CLA_TRIGGER_ADCA4 CLA Task Trigger Source is ADCA4.
CLA_TRIGGER_ADCAEVT CLA Task Trigger Source is ADCAEVT.
CLA_TRIGGER_ADCB1 CLA Task Trigger Source is ADCB1.
CLA_TRIGGER_ADCB2 CLA Task Trigger Source is ADCB2.
CLA_TRIGGER_ADCB3 CLA Task Trigger Source is ADCB3.
CLA_TRIGGER_ADCB4 CLA Task Trigger Source is ADCB4.
CLA_TRIGGER_ADCBEVT CLA Task Trigger Source is ADCBEVT.
CLA_TRIGGER_ADCC1 CLA Task Trigger Source is ADCC1.
CLA_TRIGGER_ADCC2 CLA Task Trigger Source is ADCC2.
CLA_TRIGGER_ADCC3 CLA Task Trigger Source is ADCC3.
CLA_TRIGGER_ADCC4 CLA Task Trigger Source is ADCC4.
CLA_TRIGGER_ADCCEVT CLA Task Trigger Source is ADCCEVT.
CLA_TRIGGER_ADCD1 CLA Task Trigger Source is ADCD1.

CLA_TRIGGER_ADCD2 CLA Task Trigger Source is ADCD2.
CLA_TRIGGER_ADCD3 CLA Task Trigger Source is ADCD3.
CLA_TRIGGER_ADCD4 CLA Task Trigger Source is ADCD4.
CLA_TRIGGER_ADCDEVT CLA Task Trigger Source is ADCDEVT.
CLA_TRIGGER_XINT1 CLA Task Trigger Source is XINT1.
CLA_TRIGGER_XINT2 CLA Task Trigger Source is XINT2.
CLA_TRIGGER_XINT3 CLA Task Trigger Source is XINT3.
CLA_TRIGGER_XINT4 CLA Task Trigger Source is XINT4.
CLA_TRIGGER_XINT5 CLA Task Trigger Source is XINT5.
CLA_TRIGGER_EPWM1INT CLA Task Trigger Source is EPWM1INT.
CLA_TRIGGER_EPWM2INT CLA Task Trigger Source is EPWM2INT.
CLA_TRIGGER_EPWM3INT CLA Task Trigger Source is EPWM3INT.
CLA_TRIGGER_EPWM4INT CLA Task Trigger Source is EPWM4INT.
CLA_TRIGGER_EPWM5INT CLA Task Trigger Source is EPWM5INT.
CLA_TRIGGER_EPWM6INT CLA Task Trigger Source is EPWM6INT.
CLA_TRIGGER_EPWM7INT CLA Task Trigger Source is EPWM7INT.
CLA_TRIGGER_EPWM8INT CLA Task Trigger Source is EPWM8INT.
CLA_TRIGGER_EPWM9INT CLA Task Trigger Source is EPWM9INT.
CLA_TRIGGER_EPWM10INT CLA Task Trigger Source is EPWM10INT.
CLA_TRIGGER_EPWM11INT CLA Task Trigger Source is EPWM11INT.
CLA_TRIGGER_EPWM12INT CLA Task Trigger Source is EPWM12INT.
CLA_TRIGGER_TINT0 CLA Task Trigger Source is TINT0.
CLA_TRIGGER_TINT1 CLA Task Trigger Source is TINT1.
CLA_TRIGGER_TINT2 CLA Task Trigger Source is TINT2.
CLA_TRIGGER_MXINTA CLA Task Trigger Source is MXINTA.
CLA_TRIGGER_MRINTA CLA Task Trigger Source is MRINTA.
CLA_TRIGGER_MXINTB CLA Task Trigger Source is MXINTB.
CLA_TRIGGER_MRINTB CLA Task Trigger Source is MRINTB.
CLA_TRIGGER_ECAP1INT CLA Task Trigger Source is ECAP1INT.
CLA_TRIGGER_ECAP2INT CLA Task Trigger Source is ECAP2INT.
CLA_TRIGGER_ECAP3INT CLA Task Trigger Source is ECAP3INT.
CLA_TRIGGER_ECAP4INT CLA Task Trigger Source is ECAP4INT.
CLA_TRIGGER_ECAP5INT CLA Task Trigger Source is ECAP5INT.
CLA_TRIGGER_ECAP6INT CLA Task Trigger Source is ECAP6INT.
CLA_TRIGGER_EQEP1INT CLA Task Trigger Source is EQEP1INT.
CLA_TRIGGER_EQEP2INT CLA Task Trigger Source is EQEP2INT.
CLA_TRIGGER_EQEP3INT CLA Task Trigger Source is EQEP3INT.
CLA_TRIGGER_SDFM1INT CLA Task Trigger Source is SDFM1INT.
CLA_TRIGGER_SDFM2INT CLA Task Trigger Source is SDFM2INT.
CLA_TRIGGER_UPP1INT CLA Task Trigger Source is UPP1INT.
CLA_TRIGGER_SPITXAINT CLA Task Trigger Source is SPITXAINT.
CLA_TRIGGER_SPIRXAINT CLA Task Trigger Source is SPIRXAINT.
CLA_TRIGGER_SPITXBINT CLA Task Trigger Source is SPITXBINT.
CLA_TRIGGER_SPIRXBINT CLA Task Trigger Source is SPIRXBINT.
CLA_TRIGGER_SPITXCINT CLA Task Trigger Source is SPITXCINT.
CLA_TRIGGER_SPIRXCINT CLA Task Trigger Source is SPIRXCINT.

8.2.3 Function Documentation

8.2.3.1 static void CLA_mapTaskVector (uint32_t *base*, **CLA_MVECTNumber** *claIntVect*, uint16_t *claTaskAddr*) `[inline]`, `[static]`

Map CLA Task Interrupt Vector

Parameters

base	is the base address of the CLA controller.
claIntVect	is CLA interrupt vector (MVECT1 to MVECT8) the value of claIntVect can be any of the following: ■ **CLA_MVECT_1** - Task Interrupt Vector 1 ■ **CLA_MVECT_2** - Task Interrupt Vector 2 ■ **CLA_MVECT_3** - Task Interrupt Vector 3 ■ **CLA_MVECT_4** - Task Interrupt Vector 4 ■ **CLA_MVECT_5** - Task Interrupt Vector 5 ■ **CLA_MVECT_6** - Task Interrupt Vector 6 ■ **CLA_MVECT_7** - Task Interrupt Vector 7 ■ **CLA_MVECT_8** - Task Interrupt Vector 8
claTaskAddr	is the start address of the code for task

Each CLA Task (1 to 8) has its own MVECTx register. When a task is triggered, the CLA loads the MVECTx register of the task in question to the MPC (CLA program counter) and begins execution from that point. The CLA has a 16-bit address bus, and can therefore, access the lower 64 KW space. The MVECTx registers take an address anywhere in this space.

Returns

None.

8.2.3.2 static void CLA_performHardReset (uint32_t *base*) [inline], [static]

Hard Reset

Parameters

base	is the base address of the CLA controller.

This function will cause a hard reset of the CLA and set all CLA registers to their default state.

Returns

None.

8.2.3.3 static void CLA_performSoftReset (uint32_t *base*) [inline], [static]

Soft Reset

Parameters

base	is the base address of the CLA controller.

This function will cause a soft reset of the CLA. This will stop the current task, clear the MIRUN flag and clear all bits in the MIER register.

Returns

None.

8.2.3.4 static void CLA_enableIACK (uint32_t *base*) [inline], [static]

IACK enable

Parameters

base	is the base address of the CLA controller.

This function enables the main CPU to use the IACK #16bit instruction to set MIFR bits in the same manner as writing to the MIFRC register.

Returns
None.

8.2.3.5 static void CLA_disableIACK (uint32_t *base*) [inline], [static]

IACK disable

Parameters

base	is the base address of the CLA controller.

This function disables the main CPU to use the IACK #16bit instruction to set MIFR bits in the same manner as writing to the MIFRC register.

Returns
None.

8.2.3.6 static bool CLA_getPendingTaskFlag (uint32_t *base*, **CLA_TaskNumber** *taskNumber*) [inline], [static]

Query task N to see if it is flagged and pending execution

Parameters

base	is the base address of the CLA controller.
taskNumber	is the number of the task CLA_TASK_N where N is a number from 1 to 8. Do not use CLA_TASKFLAG_ALL.

This function gets the status of each bit in the interrupt flag register corresponds to a CLA task. The corresponding bit is automatically set when the task is triggered (either from a peripheral, through software, or through the MIFRC register). The bit gets cleared when the CLA starts to execute the flagged task.

Returns
True if the queried task has been triggered but pending execution.

8.2.3.7 static uint16_t CLA_getAllPendingTaskFlags (uint32_t *base*) [inline], [static]

Get status of All Task Interrupt Flag

Parameters

base	is the base address of the CLA controller.

This function gets the value of the interrupt flag register (MIFR)

Returns

the value of Interrupt Flag Register (MIFR)

8.2.3.8 static bool CLA_getTaskOverflowFlag (uint32_t *base,* **CLA_TaskNumber** *taskNumber*) [inline], [static]

Get status of Task n Interrupt Overflow Flag

Parameters

base	is the base address of the CLA controller.
taskNumber	is the number of the task CLA_TASK_N where N is a number from 1 to 8. Do not use CLA_TASKFLAG_ALL.

This function gets the status of each bit in the overflow flag register corresponds to a CLA task, This bit is set when an interrupt overflow event has occurred for the specific task.

Returns

True if any of task interrupt overflow has occurred.

8.2.3.9 static uint16_t CLA_getAllTaskOverflowFlags (uint32_t *base*) [inline], [static]

Get status of All Task Interrupt Overflow Flag

Parameters

base	is the base address of the CLA controller.

This function gets the value of the Interrupt Overflow Flag Register

Returns

the value of Interrupt Overflow Flag Register(MIOVF)

8.2.3.10 static void CLA_clearTaskFlags (uint32_t *base,* uint16_t *taskFlags*) [inline], [static]

Clear the task interrupt flag

Parameters

base	is the base address of the CLA controller.

taskFlags	is the bitwise OR of the tasks' flags to be cleared CLA_TASKFLAG_N where N is the task number from 1 to 8, or CLA_TASKFLAG_ALL to clear all flags.

This function is used to manually clear bits in the interrupt flag (MIFR) register

Returns
None.

8.2.3.11 static void CLA_forceTasks (uint32_t *base,* uint16_t *taskFlags*) [inline], [static]

Force a CLA Task

Parameters

base	is the base address of the CLA controller.
taskFlags	is the bitwise OR of the tasks' flags to be forced CLA_TASKFLAG_N where N is the task number from 1 to 8, or CLA_TASKFLAG_ALL to force all tasks.

This function forces a task through software.

Returns
None.

8.2.3.12 static void CLA_enableTasks (uint32_t *base,* uint16_t *taskFlags*) [inline], [static]

Enable CLA task(s)

Parameters

base	is the base address of the CLA controller.
taskFlags	is the bitwise OR of the tasks' flags to be enabled CLA_TASKFLAG_N where N is the task number from 1 to 8, or CLA_TASKFLAG_ALL to enable all tasks

This function allows an incoming interrupt or main CPU software to start the corresponding CLA task.

Returns
None.

8.2.3.13 static void CLA_disableTasks (uint32_t *base,* uint16_t *taskFlags*) [inline], [static]

Disable CLA task interrupt

Parameters

base	is the base address of the CLA controller.
taskFlags	is the bitwise OR of the tasks' flags to be disabled CLA_TASKFLAG_N where N is the task number from 1 to 8, or CLA_TASKFLAG_ALL to disable all tasks

This function disables CLA task interrupt by setting the MIER register bit to 0, while the corresponding task is executing this will have no effect on the task. The task will continue to run until it hits the MSTOP instruction.

Returns
None.

8.2.3.14 static bool CLA_getTaskRunStatus (uint32_t *base,* **CLA_TaskNumber** *taskNumber*) [inline], [static]

Get the value of a task run status

Parameters

base	is the base address of the CLA controller.
taskNumber	is the number of the task CLA_TASK_N where N is a number from 1 to 8. Do not use CLA_TASKFLAG_ALL.

This function gets the status of each bit in the Interrupt Run Status Register which indicates whether the task is currently executing

Returns
True if the task is executing.

8.2.3.15 static uint16_t CLA_getAllTaskRunStatus (uint32_t *base*) [inline], [static]

Get the value of all task run status

Parameters

base	is the base address of the CLA controller.

This function indicates which task is currently executing.

Returns
the value of Interrupt Run Status Register (MIRUN)

8.2.3.16 static void CLA_enableSoftwareInterrupt (uint32_t *base,* uint16_t *taskFlags*) [inline], [static]

Enable the Software Interrupt for a given CLA Task

Parameters

base	is the base address of the CLA controller.
taskFlags	is the bitwise OR of the tasks for which software interrupts are to be enabled, CLA_TASKFLAG_N where N is the task number from 1 to 8, or CLA_TASKFLAG_ALL to enable software interrupts of all tasks

This function enables the Software Interrupt for a single, or set of, CLA task(s). It does this by writing a 1 to the task's bit in the CLA1SOFTINTEN register. By setting a task's SOFTINT bit, you disable its ability to generate an end-of-task interrupt For example, if we enable Task 2's SOFTINT bit, we disable its ability to generate an end-of-task interrupt, but now any running CLA task has the ability to force task 2's interrupt (through the CLA1INTFRC register) to the main CPU. This interrupt will be handled by the End-of-Task 2 interrupt handler even though the interrupt was not caused by Task 2 running to completion. This allows programmers to generate interrupts while a control task is running.

Note

1. The CLA1SOFTINTEN and CLA1INTFRC are only writable from the CLA.
2. Enabling a given task's software interrupt enable bit disables that task's ability to generate an End-of-Task interrupt to the main CPU, however, should another task force its interrupt (through the CLA1INTFRC register), it will be handled by that task's End-of-Task Interrupt Handler.

Returns

None.

8.2.3.17 static void CLA_disableSoftwareInterrupt (uint32_t *base,* uint16_t *taskFlags*) [inline], [static]

Disable the Software Interrupt for a given CLA Task

Parameters

base	is the base address of the CLA controller.
taskFlags	is the bitwise OR of the tasks for which software interrupts are to be disabled, CLA_TASKFLAG_N where N is the task number from 1 to 8, or CLA_TASKFLAG_ALL to disable software interrupts of all tasks

This function disables the Software Interrupt for a single, or set of, CLA task(s). It does this by writing a 0 to the task's bit in the CLA1SOFTINTEN register.

Note

1. The CLA1SOFTINTEN and CLA1INTFRC are only writable from the CLA.
2. Disabling a given task's software interrupt ability allows that task to generate an End-of-Task interrupt to the main CPU.

Returns
None.

8.2.3.18 static void CLA_forceSoftwareInterrupt (uint32_t *base,* uint16_t *taskFlags*) [inline], [static]

Force a particular Task's Software Interrupt

Parameters

base	is the base address of the CLA controller.
taskFlags	is the bitwise OR of the task's whose software interrupts are to be forced, CLA_TASKFLAG_N where N is the task number from 1 to 8, or CLA_TASKFLAG_ALL to force software interrupts for all tasks

This function forces the Software Interrupt for a single, or set of, CLA task(s). It does this by writing a 1 to the task's bit in the CLA1INTFRC register. For example, if we enable Task 2's SOFTINT bit, we disable its ability to generate an end-of-task interrupt, but now any running CLA task has the ability to force task 2's interrupt (through the CLA1INTFRC register) to the main CPU. This interrupt will be handled by the End-of-Task 2 interrupt handler even though the interrupt was not caused by Task 2 running to completion. This allows programmers to generate interrupts while a control task is running.

Note

1. The CLA1SOFTINTEN and CLA1INTFRC are only writable from the CLA.
2. Enabling a given task's software interrupt enable bit disables that task's ability to generate an End-of-Task interrupt to the main CPU, however, should another task force its interrupt (through the CLA1INTFRC register), it will be handled by that task's End-of-Task Interrupt Handler.
3. This function will set the INTFRC bit for a task, but does not check that its SOFTINT bit is set. It falls to the user to ensure that software interrupt for a given task is enabled before it can be forced.

Returns

None.

8.2.3.19 void CLA_setTriggerSource (**CLA_TaskNumber** *taskNumber,* **CLA_Trigger** *trigger*)

Configures CLA task triggers.

Parameters

taskNumber	is the number of the task CLA_TASK_N where N is a number from 1 to 8.
trigger	is the trigger source to be assigned to the selected task.

This function configures the trigger source of a CLA task. The *taskNumber* parameter indicates which task is being configured, and the *trigger* parameter is the interrupt source from a specific peripheral interrupt (or software) that will trigger the task.

Returns

None.

References CLA_TASK_4.

9 CMPSS Module

9.1 CMPSS Introduction

The comparator subsystem (CMPSS) API provides a set of functions for programming the digital circuits of a pair of analog comparators. Functions are provided to configure each comparator and its corresponding 12-bit DAC and digital filter and to get both the latched and unlatched status of their output. There are also functions to configure the optional ramp generator circuit and to route incoming sync signals from the ePWM module.

The output signals of the CMPSS (referred to as CTRIPH, CTRIPOUTH, CTRIPL, and CTRIPOUTL) may be routed to GPIOs or other internal destinations using the X-BARs. See the X-BAR driver for details.

9.2 API Functions

Functions

- static void CMPSS_enableModule (uint32_t base)
- static void CMPSS_disableModule (uint32_t base)
- static void CMPSS_configHighComparator (uint32_t base, uint16_t config)
- static void CMPSS_configLowComparator (uint32_t base, uint16_t config)
- static void CMPSS_configOutputsHigh (uint32_t base, uint16_t config)
- static void CMPSS_configOutputsLow (uint32_t base, uint16_t config)
- static uint16_t CMPSS_getStatus (uint32_t base)
- static void CMPSS_configDAC (uint32_t base, uint16_t config)
- static void CMPSS_setDACValueHigh (uint32_t base, uint16_t value)
- static void CMPSS_setDACValueLow (uint32_t base, uint16_t value)
- static void CMPSS_initFilterHigh (uint32_t base)
- static void CMPSS_initFilterLow (uint32_t base)
- static uint16_t CMPSS_getDACValueHigh (uint32_t base)
- static uint16_t CMPSS_getDACValueLow (uint32_t base)
- static void CMPSS_clearFilterLatchHigh (uint32_t base)
- static void CMPSS_clearFilterLatchLow (uint32_t base)
- static void CMPSS_setMaxRampValue (uint32_t base, uint16_t value)
- static uint16_t CMPSS_getMaxRampValue (uint32_t base)
- static void CMPSS_setRampDecValue (uint32_t base, uint16_t value)
- static uint16_t CMPSS_getRampDecValue (uint32_t base)
- static void CMPSS_setRampDelayValue (uint32_t base, uint16_t value)
- static uint16_t CMPSS_getRampDelayValue (uint32_t base)
- static void CMPSS_setHysteresis (uint32_t base, uint16_t value)
- void CMPSS_configFilterHigh (uint32_t base, uint16_t samplePrescale, uint16_t sampleWindow, uint16_t threshold)
- void CMPSS_configFilterLow (uint32_t base, uint16_t samplePrescale, uint16_t sampleWindow, uint16_t threshold)
- void CMPSS_configLatchOnPWMSYNC (uint32_t base, bool highEnable, bool lowEnable)
- void CMPSS_configRamp (uint32_t base, uint16_t maxRampVal, uint16_t decrementVal, uint16_t delayVal, uint16_t pwmSyncSrc, bool useRampValShdw)

9.2.1 Detailed Description

The two comparators are referred to as the high comparator and the low comparator. Accordingly, many API functions come in pairs with both a "High" and a "Low" version. See the device's Technical Reference Manual for diagrams showing what resources the comparators share and what they contain separately.

The code for this module is contained in `driverlib/cmpss.c`, with `driverlib/cmpss.h` containing the API declarations for use by applications.

9.2.2 Function Documentation

9.2.2.1 static void CMPSS_enableModule (uint32_t *base*) `[inline]`, `[static]`

Enables the CMPSS module.

Parameters

base	is the base address of the CMPSS module.

This function enables the CMPSS module passed into the *base* parameter.

Returns
None.

9.2.2.2 static void CMPSS_disableModule (uint32_t *base*) `[inline]`, `[static]`

Disables the CMPSS module.

Parameters

base	is the base address of the CMPSS module.

This function disables the CMPSS module passed into the *base* parameter.

Returns
None.

9.2.2.3 static void CMPSS_configHighComparator (uint32_t *base,* uint16_t *config*) `[inline]`, `[static]`

Sets the configuration for the high comparator.

Parameters

base	is the base address of the CMPSS module.
config	is the configuration of the high comparator.

This function configures a comparator. The *config* parameter is the result of a logical OR operation between a **CMPSS_INSRC_xxx** value and if desired, **CMPSS_INV_INVERTED** and **CMPSS_OR_ASYNC_OUT_W_FILT** values.

The **CMPSS_INSRC_xxx** term can take on the following values to specify the high comparator negative input source:

- **CMPSS_INSRC_DAC** - The internal DAC.
- **CMPSS_INSRC_PIN** - An external pin.

CMPSS_INV_INVERTED may be ORed into *config* if the comparator output should be inverted.

CMPSS_OR_ASYNC_OUT_W_FILT may be ORed into *config* if the asynchronous comparator output should be fed into an OR gate with the latched digital filter output before it is made available for CTRIPH or CTRIPOUTH.

Returns
None.

9.2.2.4 static void CMPSS_configLowComparator (uint32_t *base*, uint16_t *config*) [inline], [static]

Sets the configuration for the low comparator.

Parameters

base	is the base address of the CMPSS module.
config	is the configuration of the low comparator.

This function configures a comparator. The *config* parameter is the result of a logical OR operation between a **CMPSS_INSRC_xxx** value and if desired, **CMPSS_INV_INVERTED** and **CMPSS_OR_ASYNC_OUT_W_FILT** values.

The **CMPSS_INSRC_xxx** term can take on the following values to specify the low comparator negative input source:

- **CMPSS_INSRC_DAC** - The internal DAC.
- **CMPSS_INSRC_PIN** - An external pin.

CMPSS_INV_INVERTED may be ORed into *config* if the comparator output should be inverted.

CMPSS_OR_ASYNC_OUT_W_FILT may be ORed into *config* if the asynchronous comparator output should be fed into an OR gate with the latched digital filter output before it is made available for CTRIPL or CTRIPOUTL.

Returns
None.

9.2.2.5 static void CMPSS_configOutputsHigh (uint32_t *base*, uint16_t *config*) [inline], [static]

Sets the output signal configuration for the high comparator.

Parameters

base	is the base address of the CMPSS module.
config	is the configuration of the high comparator output signals.

This function configures a comparator's output signals CTRIP and CTRIPOUT. The *config* parameter is the result of a logical OR operation between the **CMPSS_TRIPOUT_xxx** and **CMPSS_TRIP_xxx** values.

The **CMPSS_TRIPOUT_xxx** term can take on the following values to specify which signal drives CTRIPOUTH:

- **CMPSS_TRIPOUT_ASYNC_COMP** - The asynchronous comparator output.
- **CMPSS_TRIPOUT_SYNC_COMP** - The synchronous comparator output.
- **CMPSS_TRIPOUT_FILTER** - The output of the digital filter.
- **CMPSS_TRIPOUT_LATCH** - The latched output of the digital filter.

The **CMPSS_TRIP_xxx** term can take on the following values to specify which signal drives CTRIPH:

- **CMPSS_TRIP_ASYNC_COMP** - The asynchronous comparator output.
- **CMPSS_TRIP_SYNC_COMP** - The synchronous comparator output.
- **CMPSS_TRIP_FILTER** - The output of the digital filter.
- **CMPSS_TRIP_LATCH** - The latched output of the digital filter.

Returns
None.

9.2.2.6 static void CMPSS_configOutputsLow (uint32_t *base,* uint16_t *config*) [inline], [static]

Sets the output signal configuration for the low comparator.

Parameters

base	is the base address of the CMPSS module.
config	is the configuration of the low comparator output signals.

This function configures a comparator's output signals CTRIP and CTRIPOUT. The *config* parameter is the result of a logical OR operation between the **CMPSS_TRIPOUT_xxx** and **CMPSS_TRIP_xxx** values.

The **CMPSS_TRIPOUT_xxx** term can take on the following values to specify which signal drives CTRIPOUTL:

- **CMPSS_TRIPOUT_ASYNC_COMP** - The asynchronous comparator output.
- **CMPSS_TRIPOUT_SYNC_COMP** - The synchronous comparator output.
- **CMPSS_TRIPOUT_FILTER** - The output of the digital filter.
- **CMPSS_TRIPOUT_LATCH** - The latched output of the digital filter.

The **CMPSS_TRIP_xxx** term can take on the following values to specify which signal drives CTRIPL:

- **CMPSS_TRIP_ASYNC_COMP** - The asynchronous comparator output.
- **CMPSS_TRIP_SYNC_COMP** - The synchronous comparator output.
- **CMPSS_TRIP_FILTER** - The output of the digital filter.
- **CMPSS_TRIP_LATCH** - The latched output of the digital filter.

Returns
None.

9.2.2.7 static uint16_t CMPSS_getStatus (uint32_t *base*) [inline], [static]

Gets the current comparator status.

Parameters

base	is the base address of the comparator module.

This function returns the current status for the comparator, specifically the digital filter output and latched digital filter output.

Returns

Returns the current interrupt status, enumerated as a bit field of the following values:

- **CMPSS_STS_HI_FILTOUT** - High digital filter output
- **CMPSS_STS_HI_LATCHFILTOUT** - Latched value of high digital filter output
- **CMPSS_STS_LO_FILTOUT** - Low digital filter output
- **CMPSS_STS_LO_LATCHFILTOUT** - Latched value of low digital filter output

9.2.2.8 static void CMPSS_configDAC (uint32_t *base,* uint16_t *config*) [inline], [static]

Sets the configuration for the internal comparator DACs.

Parameters

base	is the base address of the CMPSS module.
config	is the configuration of the internal DAC.

This function configures the comparator's internal DAC. The *config* parameter is the result of a logical OR operation between the **CMPSS_DACVAL_xxx**, **CMPSS_DACREF_xxx**, and **CMPSS_DACSRC_xxx**.

The **CMPSS_DACVAL_xxx** term can take on the following values to specify when the DAC value is loaded from its shadow register:

- **CMPSS_DACVAL_SYSCLK** - Value register updated on system clock.
- **CMPSS_DACVAL_PWMSYNC** - Value register updated on PWM sync.

The **CMPSS_DACREF_xxx** term can take on the following values to specify which voltage supply is used as reference for the DACs:

- **CMPSS_DACREF_VDDA** - VDDA is the voltage reference for the DAC.
- **CMPSS_DACREF_VDAC** - VDAC is the voltage reference for the DAC.

The **CMPSS_DACSRC_xxx** term can take on the following values to specify the DAC value source for the high comparator's internal DAC:

- **CMPSS_DACSRC_SHDW** - The user-programmed DACVALS register.
- **CMPSS_DACSRC_RAMP** - The ramp generator RAMPSTS register

Note

The **CMPSS_DACVAL_xxx** and **CMPSS_DACREF_xxx** terms apply to both the high and low comparators. **CMPSS_DACSRC_xxx** will only affect the high comparator's internal DAC.

Returns

None.

9.2.2.9 static void CMPSS_setDACValueHigh (uint32_t *base,* uint16_t *value*) [inline], [static]

Sets the value of the internal DAC of the high comparator.

Parameters

base	is the base address of the comparator module.
value	is the value actively driven by the DAC.

This function sets the 12-bit value driven by the internal DAC of the high comparator. This function will load the value into the shadow register from which the actual DAC value register will be loaded. To configure which event causes this shadow load to take place, use CMPSS_configDAC().

Returns

None.

9.2.2.10 static void CMPSS_setDACValueLow (uint32_t *base,* uint16_t *value*) [inline], [static]

Sets the value of the internal DAC of the low comparator.

Parameters

base	is the base address of the comparator module.
value	is the value actively driven by the DAC.

This function sets the 12-bit value driven by the internal DAC of the low comparator. This function will load the value into the shadow register from which the actual DAC value register will be loaded. To configure which event causes this shadow load to take place, use CMPSS_configDAC().

Returns

None.

9.2.2.11 static void CMPSS_initFilterHigh (uint32_t *base*) [inline], [static]

Initializes the digital filter of the high comparator.

Parameters

base	is the base address of the comparator module.

This function initializes all the samples in the high comparator digital filter to the filter input value.

Note

See CMPSS_configFilterHigh() for the proper initialization sequence to avoid glitches.

Returns

None.

9.2.2.12 static void CMPSS_initFilterLow (uint32_t *base*) [inline], [static]

Initializes the digital filter of the low comparator.

Parameters

base	is the base address of the comparator module.

This function initializes all the samples in the low comparator digital filter to the filter input value.

Note

See CMPSS_configFilterLow() for the proper initialization sequence to avoid glitches.

Returns

None.

9.2.2.13 static uint16_t CMPSS_getDACValueHigh (uint32_t *base*) `[inline]`, `[static]`

Gets the value of the internal DAC of the high comparator.

Parameters

base	is the base address of the comparator module.

This function gets the value of the internal DAC of the high comparator. The value is read from the *active* register–not the shadow register to which CMPSS_setDACValueHigh() writes.

Returns

Returns the value driven by the internal DAC of the high comparator.

9.2.2.14 static uint16_t CMPSS_getDACValueLow (uint32_t *base*) `[inline]`, `[static]`

Gets the value of the internal DAC of the low comparator.

Parameters

base	is the base address of the comparator module.

This function gets the value of the internal DAC of the low comparator. The value is read from the *active* register–not the shadow register to which CMPSS_setDACValueLow() writes.

Returns

Returns the value driven by the internal DAC of the low comparator.

9.2.2.15 static void CMPSS_clearFilterLatchHigh (uint32_t *base*) `[inline]`, `[static]`

Causes a software reset of the high comparator digital filter output latch.

Parameters

base	is the base address of the comparator module.

This function causes a software reset of the high comparator digital filter output latch. It will generate a single pulse of the latch reset signal.

Returns

None.

9.2.2.16 static void CMPSS_clearFilterLatchLow (uint32_t *base*) [inline], [static]

Causes a software reset of the low comparator digital filter output latch.

Parameters

base	is the base address of the comparator module.

This function causes a software reset of the low comparator digital filter output latch. It will generate a single pulse of the latch reset signal.

Returns

None.

9.2.2.17 static void CMPSS_setMaxRampValue (uint32_t *base,* uint16_t *value*) [inline], [static]

Sets the ramp generator maximum reference value.

Parameters

base	is the base address of the comparator module.
value	the ramp maximum reference value.

This function sets the ramp maximum reference value that will be loaded into the ramp generator.

Returns

None.

9.2.2.18 static uint16_t CMPSS_getMaxRampValue (uint32_t *base*) [inline], [static]

Gets the ramp generator maximum reference value.

Parameters

base	is the base address of the comparator module.

Returns

Returns the latched ramp maximum reference value that will be loaded into the ramp generator.

9.2.2.19 static void CMPSS_setRampDecValue (uint32_t *base*, uint16_t *value*) `[inline]`, `[static]`

Sets the ramp generator decrement value.

Parameters

base	is the base address of the comparator module.
value	is the ramp decrement value.

This function sets the value that is subtracted from the ramp value on every system clock cycle.

Returns
None.

9.2.2.20 static uint16_t CMPSS_getRampDecValue (uint32_t *base*) [inline], [static]

Gets the ramp generator decrement value.

Parameters

base	is the base address of the comparator module.

Returns
Returns the latched ramp decrement value that is subtracted from the ramp value on every system clock cycle.

9.2.2.21 static void CMPSS_setRampDelayValue (uint32_t *base,* uint16_t *value*) [inline], [static]

Sets the ramp generator delay value.

Parameters

base	is the base address of the comparator module.
value	is the 13-bit ramp delay value.

This function sets the value that configures the number of system clock cycles to delay the start of the ramp generator decrementer after a PWMSYNC event is received. Delay value can be no greater than 8191.

Returns
None.

9.2.2.22 static uint16_t CMPSS_getRampDelayValue (uint32_t *base*) [inline], [static]

Gets the ramp generator delay value.

Parameters

base	is the base address of the comparator module.

Returns

Returns the latched ramp delay value that is subtracted from the ramp value on every system clock cycle.

9.2.2.23 static void CMPSS_setHysteresis (uint32_t *base,* uint16_t *value*) [inline], [static]

Sets the comparator hysteresis settings.

Parameters

base	is the base address of the comparator module.
value	is the amount of hysteresis on the comparator inputs.

This function sets the amount of hysteresis on the comparator inputs. The *value* parameter indicates the amount of hysteresis desired. Passing in 0 results in none, passing in 1 results in typical hysteresis, passing in 2 results in 2x of typical hysteresis, and so on where *value* x of typical hysteresis is the amount configured.

Returns

None.

9.2.2.24 void CMPSS_configFilterHigh (uint32_t *base,* uint16_t *samplePrescale,* uint16_t *sampleWindow,* uint16_t *threshold*)

Configures the digital filter of the high comparator.

Parameters

base	is the base address of the comparator module.
samplePrescale	is the number of system clock cycles between samples.
sampleWindow	is the number of FIFO samples to monitor.
threshold	is the majority threshold of samples to change state.

This function configures the operation of the digital filter of the high comparator.

The *samplePrescale* parameter specifies the number of system clock cycles between samples. It is a 10-bit value so a number higher than 1023 should not be passed as this parameter. The prescale used by digital filter is 1 more than *samplePrescale* value. So, the input provided should be 1 less than the expected prescale.

The *sampleWindow* parameter configures the size of the window of FIFO samples taken from the input that will be monitored to determine when to change the filter output. This sample window may be no larger than 32 samples.

The threshold used by digital filter is 1 more than *threshold* parameter value. So, the input provided should be 1 less than the expected threshold.

The filter output resolves to the majority value of the sample window where majority is defined by the value passed into the *threshold* parameter. For proper operation, the value of *threshold* must be greater than sampleWindow / 2.

To ensure proper operation of the filter, the following is the recommended function call sequence for initialization:

1. Configure and enable the comparator using CMPSS_configHighComparator() and CMPSS_enableModule()
2. Configure the digital filter using CMPSS_configFilterHigh()
3. Initialize the sample values using CMPSS_initFilterHigh()
4. Configure the module output signals CTRIP and CTRIPOUT using CMPSS_configOutputsHigh()

Returns

None.

9.2.2.25 void CMPSS_configFilterLow (uint32_t *base,* uint16_t *samplePrescale,* uint16_t *sampleWindow,* uint16_t *threshold*)

Configures the digital filter of the low comparator.

Parameters

base	is the base address of the comparator module.
samplePrescale	is the number of system clock cycles between samples.
sampleWindow	is the number of FIFO samples to monitor.
threshold	is the majority threshold of samples to change state.

This function configures the operation of the digital filter of the low comparator.

The *samplePrescale* parameter specifies the number of system clock cycles between samples. It is a 10-bit value so a number higher than 1023 should not be passed as this parameter. The prescale used by digital filter is 1 more than *samplePrescale* value. So, the input provided should be 1 less than the expected prescale.

The *sampleWindow* parameter configures the size of the window of FIFO samples taken from the input that will be monitored to determine when to change the filter output. This sample window may be no larger than 32 samples.

The threshold used by digital filter is 1 more than *threshold* parameter value. So, the input provided should be 1 less than the expected threshold.

The filter output resolves to the majority value of the sample window where majority is defined by the value passed into the *threshold* parameter. For proper operation, the value of *threshold* must be greater than sampleWindow / 2.

To ensure proper operation of the filter, the following is the recommended function call sequence for initialization:

1. Configure and enable the comparator using CMPSS_configLowComparator() and CMPSS_enableModule()
2. Configure the digital filter using CMPSS_configFilterLow()
3. Initialize the sample values using CMPSS_initFilterLow()
4. Configure the module output signals CTRIP and CTRIPOUT using CMPSS_configOutputsLow()

Returns

None.

9.2.2.26 void CMPSS_configLatchOnPWMSYNC (uint32_t *base,* bool *highEnable,* bool *lowEnable*)

Configures whether or not the digital filter latches are reset by PWMSYNC

Parameters

base	is the base address of the comparator module.
highEnable	indicates filter latch settings in the high comparator.
lowEnable	indicates filter latch settings in the low comparator.

This function configures whether or not the digital filter latches in both the high and low comparators should be reset by PWMSYNC. If the *highEnable* parameter is **true**, the PWMSYNC will be allowed to reset the high comparator's digital filter latch. If it is false, the ability of the PWMSYNC to reset the latch will be disabled. The *lowEnable* parameter has the same effect on the low comparator's digital filter latch.

Returns

None.

9.2.2.27 void CMPSS_configRamp (uint32_t *base*, uint16_t *maxRampVal*, uint16_t *decrementVal*, uint16_t *delayVal*, uint16_t *pwmSyncSrc*, bool *useRampValShdw*)

Configures the comparator subsystem's ramp generator.

Parameters

base	is the base address of the comparator module.
maxRampVal	is the ramp maximum reference value.
decrementVal	value is the ramp decrement value.
delayVal	is the ramp delay value.
pwmSyncSrc	is the number of the PWMSYNC source.
useRampVal-Shdw	indicates if the max ramp shadow should be used.

This function configures many of the main settings of the comparator subsystem's ramp generator. The *maxRampVal* parameter should be passed the ramp maximum reference value that will be loaded into the ramp generator. The *decrementVal* parameter should be passed the decrement value that will be subtracted from the ramp generator on each system clock cycle. The *delayVal* parameter should be passed the 13-bit number of system clock cycles the ramp generator should delay before beginning to decrement the ramp generator after a PWMSYNC signal is received.

These three values may be be set individually using the CMPSS_setMaxRampValue(), CMPSS_setRampDecValue(), and CMPSS_setRampDelayValue() APIs.

The number of the PWMSYNC signal to be used to reset the ramp generator should be specified by passing it into the *pwmSyncSrc* parameter. For instance, passing a 2 into *pwmSyncSrc* will select PWMSYNC2.

To indicate whether the ramp generator should reset with the value from the ramp max reference value shadow register or with the latched ramp max reference value, use the *useRampValShdw* parameter. Passing it **true** will result in the latched value being bypassed. The ramp generator will be loaded right from the shadow register. A value of **false** will load the ramp generator from the latched value.

Returns

None.

10 CPU Timer

10.1 CPU Timer Introduction

The CPU timer API provides a set of functions for configuring and using the CPU Timer module. Functions are provided to setup and configure the timer module operating conditions along with functions to get the status of the module and to clear overflow flag.

10.2 API Functions

Enumerations

- enum CPUTimer_EmulationMode { CPUTIMER_EMULATIONMODE_STOPAFTERNEXTDECREMENT, CPUTIMER_EMULATIONMODE_STOPATZERO, CPUTIMER_EMULATIONMODE_RUNFREE }
- enum CPUTimer_ClockSource { CPUTIMER_CLOCK_SOURCE_SYS, CPUTIMER_CLOCK_SOURCE_INTOSC1, CPUTIMER_CLOCK_SOURCE_INTOSC2, CPUTIMER_CLOCK_SOURCE_XTAL, CPUTIMER_CLOCK_SOURCE_AUX }
- enum CPUTimer_Prescaler { CPUTIMER_CLOCK_PRESCALER_1, CPUTIMER_CLOCK_PRESCALER_2, CPUTIMER_CLOCK_PRESCALER_4, CPUTIMER_CLOCK_PRESCALER_8, CPUTIMER_CLOCK_PRESCALER_16 }

Functions

- static void CPUTimer_clearOverflowFlag (uint32_t base)
- static void CPUTimer_disableInterrupt (uint32_t base)
- static void CPUTimer_enableInterrupt (uint32_t base)
- static void CPUTimer_reloadTimerCounter (uint32_t base)
- static void CPUTimer_stopTimer (uint32_t base)
- static void CPUTimer_resumeTimer (uint32_t base)
- static void CPUTimer_startTimer (uint32_t base)
- static void CPUTimer_setPeriod (uint32_t base, uint32_t periodCount)
- static uint32_t CPUTimer_getTimerCount (uint32_t base)
- static void CPUTimer_setPreScaler (uint32_t base, uint16_t prescaler)
- static bool CPUTimer_getTimerOverflowStatus (uint32_t base)
- static void CPUTimer_selectClockSource (uint32_t base, CPUTimer_ClockSource source, CPUTimer_Prescaler prescaler)
- void CPUTimer_setEmulationMode (uint32_t base, CPUTimer_EmulationMode mode)

10.2.1 Detailed Description

The code for this module is contained in `driverlib/cputimer.c`, with `driverlib/cputimer.h` containing the API declarations for use by applications.

10.2.2 Enumeration Type Documentation

10.2.2.1 enum **CPUTimer_EmulationMode**

Values that can be passed to CPUTimer_setEmulationMode() as the *mode* parameter.

Enumerator

CPUTIMER_EMULATIONMODE_STOPAFTERNEXTDECREMENT Denotes that the timer will stop after the next decrement.

CPUTIMER_EMULATIONMODE_STOPATZERO Denotes that the timer will stop when it reaches zero.

CPUTIMER_EMULATIONMODE_RUNFREE Denotes that the timer will run free.

10.2.2.2 enum **CPUTimer_ClockSource**

The following are values that can be passed to CPUTimer_selectClockSource() as the *source* parameter.

Enumerator

CPUTIMER_CLOCK_SOURCE_SYS System Clock Source.

CPUTIMER_CLOCK_SOURCE_INTOSC1 Internal Oscillator 1 Clock Source.

CPUTIMER_CLOCK_SOURCE_INTOSC2 Internal Oscillator 2 Clock Source.

CPUTIMER_CLOCK_SOURCE_XTAL External Clock Source.

CPUTIMER_CLOCK_SOURCE_AUX Auxiliary PLL Clock Source.

10.2.2.3 enum **CPUTimer_Prescaler**

The following are values that can be passed to CPUTimer_selectClockSource() as the *prescaler* parameter.

Enumerator

CPUTIMER_CLOCK_PRESCALER_1 Prescaler value of / 1.

CPUTIMER_CLOCK_PRESCALER_2 Prescaler value of / 2.

CPUTIMER_CLOCK_PRESCALER_4 Prescaler value of / 4.

CPUTIMER_CLOCK_PRESCALER_8 Prescaler value of / 8.

CPUTIMER_CLOCK_PRESCALER_16 Prescaler value of / 16.

10.2.3 Function Documentation

10.2.3.1 static void CPUTimer_clearOverflowFlag (uint32_t *base*) `[inline]`, `[static]`

Clears CPU timer overflow flag.

Parameters

base	is the base address of the timer module.

This function clears the CPU timer overflow flag.

Returns
None.

10.2.3.2 static void CPUTimer_disableInterrupt (uint32_t *base*) [inline], [static]

Disables CPU timer interrupt.

Parameters

base	is the base address of the timer module.

This function disables the CPU timer interrupt.

Returns
None.

10.2.3.3 static void CPUTimer_enableInterrupt (uint32_t *base*) [inline], [static]

Enables CPU timer interrupt.

Parameters

base	is the base address of the timer module.

This function enables the CPU timer interrupt.

Returns
None.

10.2.3.4 static void CPUTimer_reloadTimerCounter (uint32_t *base*) [inline], [static]

Reloads CPU timer counter.

Parameters

base	is the base address of the timer module.

This function reloads the CPU timer counter with the values contained in the CPU timer period register.

Returns
None.

10.2.3.5 static void CPUTimer_stopTimer (uint32_t *base*) [inline], [static]

Stops CPU timer.

Parameters

base	is the base address of the timer module.

This function stops the CPU timer.

Returns
None.

10.2.3.6 static void CPUTimer_resumeTimer (uint32_t *base*) [inline], [static]

Starts(restarts) CPU timer.

Parameters

base	is the base address of the timer module.

This function starts (restarts) the CPU timer.

Note: This function doesn't reset the timer counter.

Returns
None.

10.2.3.7 static void CPUTimer_startTimer (uint32_t *base*) [inline], [static]

Starts(restarts) CPU timer.

Parameters

base	is the base address of the timer module.

This function starts (restarts) the CPU timer.

Note: This function reloads the timer counter.

Returns
None.

10.2.3.8 static void CPUTimer_setPeriod (uint32_t *base,* uint32_t *periodCount*) [inline], [static]

Sets CPU timer period.

Parameters

base	is the base address of the timer module.
periodCount	is the CPU timer period count.

This function sets the CPU timer period count.

Returns
None.

10.2.3.9 static uint32_t CPUTimer_getTimerCount (uint32_t *base*) `[inline]`, `[static]`

Returns the current CPU timer counter value.

Parameters

base	is the base address of the timer module.

This function returns the current CPU timer counter value.

Returns

Returns the current CPU timer count value.

10.2.3.10 static void CPUTimer_setPreScaler (uint32_t *base,* uint16_t *prescaler*) [inline], [static]

Set CPU timer pre-scaler value.

Parameters

base	is the base address of the timer module.
prescaler	is the CPU timer pre-scaler value.

This function sets the pre-scaler value for the CPU timer. For every value of (prescaler + 1), the CPU timer counter decrements by 1.

Returns

None.

10.2.3.11 static bool CPUTimer_getTimerOverflowStatus (uint32_t *base*) [inline], [static]

Return the CPU timer overflow status.

Parameters

base	is the base address of the timer module.

This function returns the CPU timer overflow status.

Returns

Returns true if the CPU timer has overflowed, false if not.

10.2.3.12 static void CPUTimer_selectClockSource (uint32_t *base,* **CPUTimer_ClockSource** *source,* **CPUTimer_Prescaler** *prescaler*) [inline], [static]

Select CPU Timer 2 Clock Source and Prescaler

Parameters

base	is the base address of the timer module.

source	is the clock source to use for CPU Timer 2
prescaler	is the value that configures the selected clock source relative to the system clock

This function selects the specified clock source and prescaler value for the CPU timer (CPU timer 2 only).

The *source* parameter can be any one of the following:

- **CPUTIMER_CLOCK_SOURCE_SYS** - System Clock
- **CPUTIMER_CLOCK_SOURCE_INTOSC1** - Internal Oscillator 1 Clock
- **CPUTIMER_CLOCK_SOURCE_INTOSC2** - Internal Oscillator 2 Clock
- **CPUTIMER_CLOCK_SOURCE_XTAL** - External Clock
- **CPUTIMER_CLOCK_SOURCE_AUX** - Auxiliary PLL Clock

The *prescaler* parameter can be any one of the following:

- **CPUTIMER_CLOCK_PRESCALER_1** - Prescaler value of / 1
- **CPUTIMER_CLOCK_PRESCALER_2** - Prescaler value of / 2
- **CPUTIMER_CLOCK_PRESCALER_4** - Prescaler value of / 4
- **CPUTIMER_CLOCK_PRESCALER_8** - Prescaler value of / 8
- **CPUTIMER_CLOCK_PRESCALER_16** - Prescaler value of / 16

Returns

None.

10.2.3.13 void CPUTimer_setEmulationMode (uint32_t *base*, **CPUTimer_EmulationMode** *mode*)

Sets Emulation mode for CPU timer.

Parameters

base	is the base address of the timer module.
mode	is the emulation mode of the timer.

This function sets the behaviour of CPU timer during emulation. Valid values mode are: CPUTIMER_EMULATIONMODE_STOPAFTERNEXTDECREMENT, CPUTIMER_EMULATIONMODE_STOPATZERO and CPUTIMER_EMULATIONMODE_RUNFREE.

Returns

None.

11 DAC Module

11.1 DAC Introduction

The buffered digital to analog converter (DAC) API provides a set of functions for programming the digital circuits of the DAC. Functions are provided to set the reference voltage, the synchronization mode, the internal 12-bit DAC value, and set the state of the DAC output.

11.2 API Functions

Macros

- #define DAC_REG_BYTE_MASK
- #define DAC_LOCK_KEY

Enumerations

- enum DAC_ReferenceVoltage { DAC_REF_VDAC, DAC_REF_ADC_VREFHI }
- enum DAC_LoadMode { DAC_LOAD_SYSCLK, DAC_LOAD_PWMSYNC }

Functions

- static uint16_t DAC_getRevision (uint32_t base)
- static void DAC_setReferenceVoltage (uint32_t base, DAC_ReferenceVoltage source)
- static void DAC_setLoadMode (uint32_t base, DAC_LoadMode mode)
- static void DAC_setPWMSyncSignal (uint32_t base, uint16_t signal)
- static uint16_t DAC_getActiveValue (uint32_t base)
- static void DAC_setShadowValue (uint32_t base, uint16_t value)
- static uint16_t DAC_getShadowValue (uint32_t base)
- static void DAC_enableOutput (uint32_t base)
- static void DAC_disableOutput (uint32_t base)
- static void DAC_setOffsetTrim (uint32_t base, int16_t offset)
- static int16_t DAC_getOffsetTrim (uint32_t base)
- static void DAC_lockRegister (uint32_t base, uint16_t reg)
- static bool DAC_isRegisterLocked (uint32_t base, uint16_t reg)
- void DAC_tuneOffsetTrim (uint32_t base, float32_t referenceVoltage)

11.2.1 Detailed Description

The code for this module is contained in `driverlib/dac.c`, with `driverlib/dac.h` containing the API declarations for use by applications.

11.2.2 Enumeration Type Documentation

11.2.2.1 enum **DAC_ReferenceVoltage**

Values that can be passed to DAC_setReferenceVoltage() as the *source* parameter.

Enumerator

DAC_REF_VDAC VDAC reference voltage.

DAC_REF_ADC_VREFHI ADC VREFHI reference voltage.

11.2.2.2 enum **DAC_LoadMode**

Values that can be passed to DAC_setLoadMode() as the *mode* parameter.

Enumerator

DAC_LOAD_SYSCLK Load on next SYSCLK.

DAC_LOAD_PWMSYNC Load on next PWMSYNC specified by SYNCSEL.

11.2.3 Function Documentation

11.2.3.1 static uint16_t DAC_getRevision (uint32_t *base*) `[inline]`, `[static]`

Get the DAC Revision value

Parameters

base	is the DAC module base address

This function gets the DAC revision value.

Returns

Returns the DAC revision value.

11.2.3.2 static void DAC_setReferenceVoltage (uint32_t *base*, **DAC_ReferenceVoltage** *source*) `[inline]`, `[static]`

Sets the DAC Reference Voltage

Parameters

base	is the DAC module base address
source	is the selected reference voltage

This function sets the DAC reference voltage.

The *source* parameter can have one of two values:

- **DAC_REF_VDAC** - The VDAC reference voltage
- **DAC_REF_ADC_VREFHI** - The ADC VREFHI reference voltage

Returns
None.

11.2.3.3 static void DAC_setLoadMode (uint32_t *base*, **DAC_LoadMode** *mode*) [inline], [static]

Sets the DAC Load Mode

Parameters

base	is the DAC module base address
mode	is the selected load mode

This function sets the DAC load mode.

The *mode* parameter can have one of two values:

- **DAC_LOAD_SYSCLK** - Load on next SYSCLK
- **DAC_LOAD_PWMSYNC** - Load on next PWMSYNC specified by SYNCSEL

Returns
None.

11.2.3.4 static void DAC_setPWMSyncSignal (uint32_t *base*, uint16_t *signal*) [inline], [static]

Sets the DAC PWMSYNC Signal

Parameters

base	is the DAC module base address
signal	is the selected PWM signal

This function sets the DAC PWMSYNC signal.

The *signal* parameter must be set to a number that represents the PWM signal that will be set. For instance, passing 2 into *signal* will select PWM sync signal 2.

Returns
None.

11.2.3.5 static uint16_t DAC_getActiveValue (uint32_t *base*) [inline], [static]

Get the DAC Active Output Value

Parameters

base	is the DAC module base address

This function gets the DAC active output value.

Returns
Returns the DAC active output value.

11.2.3.6 static void DAC_setShadowValue (uint32_t *base*, uint16_t *value*) [inline], [static]

Set the DAC Shadow Output Value

Parameters

base	is the DAC module base address
value	is the 12-bit code to be loaded into the active value register

This function sets the DAC shadow output value.

Returns
None.

11.2.3.7 static uint16_t DAC_getShadowValue (uint32_t *base*) [inline], [static]

Get the DAC Shadow Output Value

Parameters

base	is the DAC module base address

This function gets the DAC shadow output value.

Returns
Returns the DAC shadow output value.

11.2.3.8 static void DAC_enableOutput (uint32_t *base*) [inline], [static]

Enable the DAC Output

Parameters

base	is the DAC module base address

This function enables the DAC output.

Note
A delay is required after enabling the DAC. Further details regarding the exact delay time length can be found in the device datasheet.

Returns
None.

11.2.3.9 static void DAC_disableOutput (uint32_t *base*) [inline], [static]

Disable the DAC Output

Parameters

base	is the DAC module base address

This function disables the DAC output.

Returns
None.

11.2.3.10 static void DAC_setOffsetTrim (uint32_t *base,* int16_t *offset*) `[inline]`, `[static]`

Set DAC Offset Trim

Parameters

base	is the DAC module base address
offset	is the specified value for the offset trim

This function sets the DAC offset trim. The *offset* value should be a signed number in the range of -128 to 127.

Note

The offset should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the offset value could cause this module to operate outside of the datasheet specifications.

Returns

None.

11.2.3.11 static int16_t DAC_getOffsetTrim (uint32_t *base*) [inline], [static]

Get DAC Offset Trim

Parameters

base	is the DAC module base address

This function gets the DAC offset trim value.

Returns

None.

References DAC_REG_BYTE_MASK.

11.2.3.12 static void DAC_lockRegister (uint32_t *base,* uint16_t *reg*) [inline], [static]

Lock write-access to DAC Register

Parameters

base	is the DAC module base address
reg	is the selected DAC registers

This function locks the write-access to the specified DAC register. Only a system reset can unlock the register once locked.

The *reg* parameter can be an ORed combination of any of the following values:

- **DAC_LOCK_CONTROL** - Lock the DAC control register
- **DAC_LOCK_SHADOW** - Lock the DAC shadow value register
- **DAC_LOCK_OUTPUT** - Lock the DAC output enable/disable register

Returns

None.

11.2.3.13 static bool DAC_isRegisterLocked (uint32_t *base*, uint16_t *reg*) `[inline]`, `[static]`

Check if DAC Register is locked

Parameters

base	is the DAC module base address
reg	is the selected DAC register locks to check

This function checks if write-access has been locked on the specified DAC register.

The *reg* parameter can be an ORed combination of any of the following values:

- **DAC_LOCK_CONTROL** - Lock the DAC control register
- **DAC_LOCK_SHADOW** - Lock the DAC shadow value register
- **DAC_LOCK_OUTPUT** - Lock the DAC output enable/disable register

Returns

Returns **true** if any of the registers specified are locked, and **false** if all specified registers aren't locked.

11.2.3.14 void DAC_tuneOffsetTrim (uint32_t *base*, float32_t *referenceVoltage*)

Tune DAC Offset Trim

Parameters

base	is the DAC module base address
referenceVoltage	is the reference voltage the DAC module is operating at.

This function adjusts/tunes the DAC offset trim. The *referenceVoltage* value should be a floating point number in the range specified in the device data manual.

Note

Use this function to adjust the DAC offset trim if operating at a reference voltage other than 2.5v. Since this function modifies the DAC offset trim register, it should only be called once after Device_cal. If it is called multiple times after Device_cal, the offset value scaled would be the wrong value.

Returns

None.

References DAC_REG_BYTE_MASK.

12 DCSM Module

12.1 DCSM Introduction

The DCSM driver accesses the DCSM COMMON registers. In order to configure the Dual Code Security Module, the user must program the Linkpointer in DCSM OTP as well as the security configuration registers of the Zone Select Blocks in DCSM OTP. The DCSM driver provides functions which secure and unsecure each zone and return the ownership, security status, EXEONLY status of specific RAM modules or Flash sectors. Included are two functions which can claim and release the Flash pump to operate on a specific zone.

12.2 API Functions

Data Structures

- struct DCSM_CSMPasswordKey

Macros

- #define DCSM_O_Z1_CSMPSWD0
- #define DCSM_O_Z1_CSMPSWD1
- #define DCSM_O_Z1_CSMPSWD2
- #define DCSM_O_Z1_CSMPSWD3
- #define DCSM_O_Z2_CSMPSWD0
- #define DCSM_O_Z2_CSMPSWD1
- #define DCSM_O_Z2_CSMPSWD2
- #define DCSM_O_Z2_CSMPSWD3
- #define FLSEM_KEY
- #define DCSM_ALLZERO
- #define DCSM_ALLONE
- #define DCSM_UNSECURE
- #define DCSM_ARMED

Enumerations

- enum DCSM_MemoryStatus { DCSM_MEMORY_INACCESSIBLE, DCSM_MEMORY_ZONE1, DCSM_MEMORY_ZONE2, DCSM_MEMORY_FULL_ACCESS }
- enum DCSM_SemaphoreZone { DCSM_FLSEM_ZONE1, DCSM_FLSEM_ZONE2 }
- enum DCSM_SecurityStatus { DCSM_STATUS_SECURE, DCSM_STATUS_UNSECURE, DCSM_STATUS_LOCKED }
- enum DCSM_EXEOnlyStatus { DCSM_PROTECTED, DCSM_UNPROTECTED, DCSM_INCORRECT_ZONE }

- enum DCSM_RAMModule {
  DCSM_RAMLS0, DCSM_RAMLS1, DCSM_RAMLS2, DCSM_RAMLS3,
  DCSM_RAMLS4, DCSM_RAMLS5, DCSM_RAMD0, DCSM_RAMD1,
  DCSM_CLA }
- enum DCSM_Sector {
  DCSM_SECTOR_A, DCSM_SECTOR_B, DCSM_SECTOR_C, DCSM_SECTOR_D,
  DCSM_SECTOR_E, DCSM_SECTOR_F, DCSM_SECTOR_G, DCSM_SECTOR_H,
  DCSM_SECTOR_I, DCSM_SECTOR_J, DCSM_SECTOR_K, DCSM_SECTOR_L,
  DCSM_SECTOR_M, DCSM_SECTOR_N }

Functions

- static void DCSM_secureZone1 (void)
- static void DCSM_secureZone2 (void)
- static DCSM_SecurityStatus DCSM_getZone1CSMSecurityStatus (void)
- static DCSM_SecurityStatus DCSM_getZone2CSMSecurityStatus (void)
- static uint16_t DCSM_getZone1ControlStatus (void)
- static uint16_t DCSM_getZone2ControlStatus (void)
- static DCSM_MemoryStatus DCSM_getRAMZone (DCSM_RAMModule module)
- static DCSM_MemoryStatus DCSM_getFlashSectorZone (DCSM_Sector sector)
- static uint32_t DCSM_getZone1LinkPointerError (void)
- static uint32_t DCSM_getZone2LinkPointerError (void)
- void DCSM_unlockZone1CSM (const DCSM_CSMPasswordKey ∗const psCMDKey)
- void DCSM_unlockZone2CSM (const DCSM_CSMPasswordKey ∗const psCMDKey)
- DCSM_EXEOnlyStatus DCSM_getZone1FlashEXEStatus (DCSM_Sector sector)
- DCSM_EXEOnlyStatus DCSM_getZone1RAMEXEStatus (DCSM_RAMModule module)
- DCSM_EXEOnlyStatus DCSM_getZone2FlashEXEStatus (DCSM_Sector sector)
- DCSM_EXEOnlyStatus DCSM_getZone2RAMEXEStatus (DCSM_RAMModule module)
- bool DCSM_claimZoneSemaphore (DCSM_SemaphoreZone zone)
- bool DCSM_releaseZoneSemaphore (void)

12.2.1 Detailed Description

The code for this module is contained in `driverlib/dcsm.c`, with `driverlib/dcsm.h` containing the API declarations for use by applications.

12.2.2 Enumeration Type Documentation

12.2.2.1 enum **DCSM_MemoryStatus**

Values to distinguish the status of RAM or FLASH sectors. These values describe which zone the memory location belongs too. These values can be returned from DCSM_getRAMZone(), DCSM_getFlashSectorZone().

Enumerator

DCSM_MEMORY_INACCESSIBLE Inaccessible.

DCSM_MEMORY_ZONE1 Zone 1.

DCSM_MEMORY_ZONE2 Zone 2.

DCSM_MEMORY_FULL_ACCESS Full access.

12.2.2.2 enum **DCSM_SemaphoreZone**

Values to pass to DCSM_claimZoneSemaphore(). These values are used to describe the zone that can write to Flash Wrapper registers.

Enumerator

DCSM_FLSEM_ZONE1 Flash semaphore Zone 1.

DCSM_FLSEM_ZONE2 Flash semaphore Zone 2.

12.2.2.3 enum **DCSM_SecurityStatus**

Values to distinguish the security status of the zones. These values can be returned from DCSM_getZone1CSMSecurityStatus(), DCSM_getZone2CSMSecurityStatus().

Enumerator

DCSM_STATUS_SECURE Secure.

DCSM_STATUS_UNSECURE Unsecure.

DCSM_STATUS_LOCKED Locked.

12.2.2.4 enum **DCSM_EXEOnlyStatus**

Values to decribe the EXEONLY Status. These values are returned from to DCSM_getZone1RAMEXEStatus(), DCSM_getZone2RAMEXEStatus(), DCSM_getZone1FlashEXEStatus(), DCSM_getZone2FlashEXEStatus().

Enumerator

DCSM_PROTECTED Protected.

DCSM_UNPROTECTED Unprotected.

DCSM_INCORRECT_ZONE Incorrect Zone.

12.2.2.5 enum **DCSM_RAMModule**

Values to distinguish RAM Module. These values can be passed to DCSM_getZone1RAMEXEStatus() DCSM_getZone2RAMEXEStatus(), DCSM_getRAMZone().

Enumerator

DCSM_RAMLS0 RAMLS0.

DCSM_RAMLS1 RAMLS1.

DCSM_RAMLS2 RAMLS2.

DCSM_RAMLS3 RAMLS3.

DCSM_RAMLS4 RAMLS4.

DCSM_RAMLS5 RAMLS5.

DCSM_RAMD0 RAMD0.

DCSM_RAMD1 RAMD1.

DCSM_CLA Offset of CLA field in in RAMSTAT divided by two.

12.2.2.6 enum **DCSM_Sector**

Values to distinguish Flash Sector. These values can be passed to
DCSM_getZone1FlashEXEStatus() DCSM_getZone2FlashEXEStatus(),
DCSM_getFlashSectorZone().

Enumerator

DCSM_SECTOR_A Sector A.
DCSM_SECTOR_B Sector B.
DCSM_SECTOR_C Sector C.
DCSM_SECTOR_D Sector D.
DCSM_SECTOR_E Sector E.
DCSM_SECTOR_F Sector F.
DCSM_SECTOR_G Sector G.
DCSM_SECTOR_H Sector H.
DCSM_SECTOR_I Sector I.
DCSM_SECTOR_J Sector J.
DCSM_SECTOR_K Sector K.
DCSM_SECTOR_L Sector L.
DCSM_SECTOR_M Sector M.
DCSM_SECTOR_N Sector N.

12.2.3 Function Documentation

12.2.3.1 static void DCSM_secureZone1 (void) `[inline]`, `[static]`

Secures zone 1 by setting the FORCESEC bit of Z1_CR register

This function resets the state of the zone. If the zone is unlocked, it will lock(secure) the zone and also reset all the bits in the Control Register.

Returns

None.

12.2.3.2 static void DCSM_secureZone2 (void) `[inline]`, `[static]`

Secures zone 2 by setting the FORCESEC bit of Z2_CR register

This function resets the state of the zone. If the zone is unlocked, it will lock(secure) the zone and also reset all the bits in the Control Register.

Returns

None.

12.2.3.3 static **DCSM_SecurityStatus** DCSM_getZone1CSMSecurityStatus (void) `[inline]`, `[static]`

Returns the CSM security status of zone 1

This function returns the security status of zone 1 CSM

Returns
Returns security status as an enumerated type DCSM_SecurityStatus.

References DCSM_STATUS_LOCKED, DCSM_STATUS_SECURE, and DCSM_STATUS_UNSECURE.

12.2.3.4 static **DCSM_SecurityStatus** DCSM_getZone2CSMSecurityStatus (void) `[inline]`, `[static]`

Returns the CSM security status of zone 2

This function returns the security status of zone 2 CSM

Returns
Returns security status as an enumerated type DCSM_SecurityStatus.

References DCSM_STATUS_LOCKED, DCSM_STATUS_SECURE, and DCSM_STATUS_UNSECURE.

12.2.3.5 static uint16_t DCSM_getZone1ControlStatus (void) `[inline]`, `[static]`

Returns the Control Status of zone 1

This function returns the Control Status of zone 1 CSM

Returns
Returns the contents of the Control Register which can be used with provided defines.

12.2.3.6 static uint16_t DCSM_getZone2ControlStatus (void) `[inline]`, `[static]`

Returns the Control Status of zone 2

This function returns the Control Status of zone 2 CSM

Returns
Returns the contents of the Control Register which can be used with the provided defines.

12.2.3.7 static **DCSM_MemoryStatus** DCSM_getRAMZone (**DCSM_RAMModule** *module*) `[inline]`, `[static]`

Returns the security zone a RAM section belongs to

Parameters

module	is the RAM module value. Valid values are type DCSM_RAMModule C28x RAMs : ■ **DCSM_RAMLS0** ■ **DCSM_RAMLS1** ■ **DCSM_RAMLS2** ■ **DCSM_RAMLS3** ■ **DCSM_RAMLS4** ■ **DCSM_RAMLS5** ■ **DCSM_RAMD0** ■ **DCSM_RAMD1**

This function returns the security zone a RAM section belongs to.

Returns

Returns DCSM_MEMORY_INACCESSIBLE if the section is inaccessible, DCSM_MEMORY_ZONE1 if the section belongs to zone 1, DCSM_MEMORY_ZONE2 if the section belongs to zone 2 and DCSM_MEMORY_FULL_ACCESS if the section doesn't belong to any zone (or if the section is unsecure).

Referenced by DCSM_getZone1RAMEXEStatus(), and DCSM_getZone2RAMEXEStatus().

12.2.3.8 static **DCSM_MemoryStatus** DCSM_getFlashSectorZone (**DCSM_Sector** *sector*) [inline], [static]

Returns the security zone a flash sector belongs to

Parameters

sector	is the flash sector value. Use DCSM_Sector type.

This function returns the security zone a flash sector belongs to.

Returns

Returns DCSM_MEMORY_INACCESSIBLE if the section is inaccessible , DCSM_MEMORY_ZONE1 if the section belongs to zone 1, DCSM_MEMORY_ZONE2 if the section belongs to zone 2 and DCSM_MEMORY_FULL_ACCESS if the section doesn't belong to any zone (or if the section is unsecure)..

Referenced by DCSM_getZone1FlashEXEStatus(), and DCSM_getZone2FlashEXEStatus().

12.2.3.9 static uint32_t DCSM_getZone1LinkPointerError (void) [inline], [static]

Read Zone 1 Link Pointer Error

A non-zero value indicates an error on the bit position that is set to 1.

Returns

Returns the value of the Zone 1 Link Pointer error.

12.2.3.10 static uint32_t DCSM_getZone2LinkPointerError (void) [inline], [static]

Read Zone 2 Link Pointer Error

A non-zero value indicates an error on the bit position that is set to 1.

Returns

Returns the value of the Zone 2 Link Pointer error.

12.2.3.11 void DCSM_unlockZone1CSM (const **DCSM_CSMPasswordKey** *const *psCMDKey*)

Unlocks Zone 1 CSM.

Parameters

psCMDKey	is a pointer to the DCSM_CSMPasswordKey struct that has the CSM password for zone 1.

This function unlocks the CSM password. It first reads the four password locations in the User OTP. If any of the password values is different from 0xFFFFFFFF, it unlocks the device by writing the provided passwords into CSM Key registers

Returns

None.

References DCSM_O_Z1_CSMPSWD0, DCSM_O_Z1_CSMPSWD1, DCSM_O_Z1_CSMPSWD2, and DCSM_O_Z1_CSMPSWD3.

12.2.3.12 void DCSM_unlockZone2CSM (const **DCSM_CSMPasswordKey** *const *psCMDKey*)

Unlocks Zone 2 CSM.

Parameters

psCMDKey	is a pointer to the CSMPSWDKEY that has the CSM password for zone 2.

This function unlocks the CSM password. It first reads the four password locations in the User OTP. If any of the password values is different from 0xFFFFFFFF, it unlocks the device by writing the provided passwords into CSM Key registers

Returns

None.

References DCSM_O_Z2_CSMPSWD0, DCSM_O_Z2_CSMPSWD1, DCSM_O_Z2_CSMPSWD2, and DCSM_O_Z2_CSMPSWD3.

12.2.3.13 **DCSM_EXEOnlyStatus** DCSM_getZone1FlashEXEStatus (**DCSM_Sector** *sector*)

Returns the EXE-ONLY status of zone 1 for a flash sector

Parameters

sector	is the flash sector value. Use DCSM_Sector type.

This function takes in a valid sector value and returns the status of EXE ONLY security protection for the sector.

Returns

Returns DCSM_PROTECTED if the sector is EXE-ONLY protected, DCSM_UNPROTECTED if the sector is not EXE-ONLY protected, DCSM_INCORRECT_ZONE if sector does not belong to this zone.

References DCSM_getFlashSectorZone(), DCSM_INCORRECT_ZONE, and DCSM_MEMORY_ZONE1.

12.2.3.14 **DCSM_EXEOnlyStatus** DCSM_getZone1RAMEXEStatus (**DCSM_RAMModule** *module*)

Returns the EXE-ONLY status of zone 1 for a RAM module

Parameters

module	is the RAM module value. Valid values are type DCSM_RAMModule C28x RAMs : ■ **DCSM_RAMLS0** ■ **DCSM_RAMLS1** ■ **DCSM_RAMLS2** ■ **DCSM_RAMLS3** ■ **DCSM_RAMLS4** ■ **DCSM_RAMLS5** ■ **DCSM_RAMD0** ■ **DCSM_RAMD1**

This function takes in a valid module value and returns the status of EXE ONLY security protection for that module. DCSM_CLA is an invalid module value. There is no EXE-ONLY available for DCSM_CLA.

Returns

Returns DCSM_PROTECTED if the module is EXE-ONLY protected, DCSM_UNPROTECTED if the module is not EXE-ONLY protected, DCSM_INCORRECT_ZONE if module does not belong to this zone.

References DCSM_CLA, DCSM_getRAMZone(), DCSM_INCORRECT_ZONE, and DCSM_MEMORY_ZONE1.

12.2.3.15 **DCSM_EXEOnlyStatus** DCSM_getZone2FlashEXEStatus (**DCSM_Sector** *sector*)

Returns the EXE-ONLY status of zone 2 for a flash sector

Parameters

sector	is the flash sector value. Use DCSM_Sector type.

This function takes in a valid sector value and returns the status of EXE ONLY security protection for the sector.

Returns

Returns DCSM_PROTECTED if the sector is EXE-ONLY protected,
DCSM_UNPROTECTED if the sector is not EXE-ONLY protected,
DCSM_INCORRECT_ZONE if sector does not belong to this zone.

References DCSM_getFlashSectorZone(), DCSM_INCORRECT_ZONE, and DCSM_MEMORY_ZONE2.

12.2.3.16 **DCSM_EXEOnlyStatus** DCSM_getZone2RAMEXEStatus (**DCSM_RAMModule** *module*)

Returns the EXE-ONLY status of zone 2 for a RAM module

Parameters

module	is the RAM module value. Valid values are type DCSM_RAMModule C28x RAMs : ■ **DCSM_RAMLS0** ■ **DCSM_RAMLS1** ■ **DCSM_RAMLS2** ■ **DCSM_RAMLS3** ■ **DCSM_RAMLS4** ■ **DCSM_RAMLS5** ■ **DCSM_RAMD0** ■ **DCSM_RAMD1**

This function takes in a valid module value and returns the status of EXE ONLY security protection for that module. DCSM_CLA is an invalid module value. There is no EXE-ONLY available for DCSM_CLA.

Returns

Returns DCSM_PROTECTED if the module is EXE-ONLY protected,
DCSM_UNPROTECTED if the module is not EXE-ONLY protected,
DCSM_INCORRECT_ZONE if module does not belong to this zone.

References DCSM_CLA, DCSM_getRAMZone(), DCSM_INCORRECT_ZONE, and DCSM_MEMORY_ZONE2.

12.2.3.17 bool DCSM_claimZoneSemaphore (**DCSM_SemaphoreZone** *zone*)

Claims the zone semaphore which allows access to the Flash Wrapper register for that zone.

Parameters

zone	is the zone which is trying to claim the semaphore which allows access to the Flash Wrapper registers.

Returns

Returns true for a successful semaphore capture, false if it was unable to capture the semaphore.

References FLSEM_KEY.

12.2.3.18 bool DCSM_releaseZoneSemaphore (void)

Releases the zone semaphore.

Returns

Returns true if it was successful in releasing the zone semaphore and false if it was unsuccessful in releasing the zone semaphore.

Note

If the calling function is not in the right zone to be able to access this register, it will return a false.

References FLSEM_KEY.

13 DMA Module

13.1 DMA Introduction

The direct memory access (DMA) API provides a set of functions to configure transfers of data between peripherals or memory using the device's six-channel DMA module. Functions are provided to configure which event triggers a DMA transfer, to configure the locations, sizes, and behaviors of the transfers, and to set up and handle interrupts.

13.2 API Functions

Macros

- #define DMA_CFG_ONESHOT_DISABLE
- #define DMA_CFG_ONESHOT_ENABLE
- #define DMA_CFG_CONTINUOUS_DISABLE
- #define DMA_CFG_CONTINUOUS_ENABLE
- #define DMA_CFG_SIZE_16BIT
- #define DMA_CFG_SIZE_32BIT

Enumerations

- enum DMA_Trigger
- enum DMA_InterruptMode { DMA_INT_AT_BEGINNING, DMA_INT_AT_END }
- enum DMA_EmulationMode { DMA_EMULATION_STOP, DMA_EMULATION_FREE_RUN }

Functions

- static void DMA_initController (void)
- static void DMA_setEmulationMode (DMA_EmulationMode mode)
- static void DMA_enableTrigger (uint32_t base)
- static void DMA_disableTrigger (uint32_t base)
- static void DMA_forceTrigger (uint32_t base)
- static void DMA_clearTriggerFlag (uint32_t base)
- static bool DMA_getTriggerFlagStatus (uint32_t base)
- static void DMA_startChannel (uint32_t base)
- static void DMA_stopChannel (uint32_t base)
- static void DMA_enableInterrupt (uint32_t base)
- static void DMA_disableInterrupt (uint32_t base)
- static void DMA_enableOverrunInterrupt (uint32_t base)
- static void DMA_disableOverrunInterrupt (uint32_t base)
- static void DMA_clearErrorFlag (uint32_t base)
- static void DMA_setInterruptMode (uint32_t base, DMA_InterruptMode mode)

- static void DMA_setPriorityMode (bool ch1IsHighPri)
- static void DMA_configSourceAddress (uint32_t base, const void *srcAddr)
- static void DMA_configDestAddress (uint32_t base, const void *destAddr)
- void DMA_configAddresses (uint32_t base, const void *destAddr, const void *srcAddr)
- void DMA_configBurst (uint32_t base, uint16_t size, int16_t srcStep, int16_t destStep)
- void DMA_configTransfer (uint32_t base, uint32_t transferSize, int16_t srcStep, int16_t destStep)
- void DMA_configWrap (uint32_t base, uint32_t srcWrapSize, int16_t srcStep, uint32_t destWrapSize, int16_t destStep)
- void DMA_configMode (uint32_t base, DMA_Trigger trigger, uint32_t config)

13.2.1 Detailed Description

This module is used for DMA configurations. The DMA API includes functions that configure the module as a whole and functions that configure the individual channels. Functions that fall into the former category are DMA_initController(), DMA_setEmulationMode(), and DMA_setPriorityMode(). The functions that can be configured by channel can easily be identified as they take a base address as their first parameter.

The DMA_configMode() function is used to configure the event that triggers a DMA transfer as well as several other properties of a transfer for the specified channel. Other functions that can be used to control the trigger from within the DMA module are DMA_enableTrigger(), DMA_disableTrigger(), DMA_forceTrigger(), DMA_clearTriggerFlag(), and DMA_getTriggerFlagStatus(). Note that DMA_forceTrigger() is used to trigger a transfer from software.

DMA_configAddresses() is used to write to both the beginning and current address pointer registers. The manner in which these addresses are incremented and decremented as bursts and transfers complete is configured using DMA_configBurst(), DMA_configTransfer(), and DMA_configWrap(). All sizes are in terms of 16-bit words.

DMA_enableInterrupt(), DMA_disableInterrupt(), and DMA_setInterruptMode() configure a channel interrupt that will be generated either at the beginning or the end of a transfer. An additional overrun error interrupt that is ORed into the channel interrupt signal can be configured using DMA_enableOverrunInterrupt(), and DMA_disableOverrunInterrupt(). This error can be cleared using DMA_clearErrorFlag().

When configuration is complete, DMA_startChannel() can be called to start the DMA channel running and it will wait for the first trigger. To halt the operation of the channel DMA_stopChannel() may be used.

The code for this module is contained in `driverlib/dma.c`, with `driverlib/dma.h` containing the API declarations for use by applications.

13.2.2 Enumeration Type Documentation

13.2.2.1 enum **DMA_InterruptMode**

Values that can be passed to DMA_setInterruptMode() as the *mode* parameter.

Enumerator

DMA_INT_AT_BEGINNING DMA interrupt is generated at the beginning of a transfer.

DMA_INT_AT_END DMA interrupt is generated at the end of a transfer.

13.2.2.2 enum **DMA_EmulationMode**

Values that can be passed to DMA_setEmulationMode() as the *mode* parameter.

Enumerator

DMA_EMULATION_STOP Transmission stops after current read-write access is completed.

DMA_EMULATION_FREE_RUN Continue DMA operation regardless of emulation suspend.

13.2.3 Function Documentation

13.2.3.1 static void DMA_initController (void) `[inline]`, `[static]`

Initializes the DMA controller to a known state.

This function configures does a hard reset of the DMA controller in order to put it into a known state. The function also sets the DMA to run free during an emulation suspend (see the field DEBUGCTRL.FREE for more info).

Returns

None.

13.2.3.2 static void DMA_setEmulationMode (**DMA_EmulationMode** *mode*) `[inline]`, `[static]`

Sets DMA emulation mode.

Parameters

mode	is the emulation mode to be selected.

This function sets the behavior of the DMA operation when an emulation suspend occurs. The *mode* parameter can be one of the following:

- **DMA_EMULATION_STOP** - DMA runs until the current read-write access is completed.
- **DMA_EMULATION_FREE_RUN** - DMA operation continues regardless of a the suspend.

Returns

None.

References DMA_EMULATION_STOP.

13.2.3.3 static void DMA_enableTrigger (uint32_t *base*) `[inline]`, `[static]`

Enables peripherals to trigger a DMA transfer.

Parameters

base	is the base address of the DMA channel control registers.

This function enables the selected peripheral trigger to start a DMA transfer on the specified channel.

Returns
None.

13.2.3.4 static void DMA_disableTrigger (uint32_t *base*) [inline], [static]

Disables peripherals from triggering a DMA transfer.

Parameters

base	is the base address of the DMA channel control registers.

This function disables the selected peripheral trigger from starting a DMA transfer on the specified channel. This also disables the use of the software force using the DMA_forceTrigger() API.

Returns
None.

13.2.3.5 static void DMA_forceTrigger (uint32_t *base*) [inline], [static]

Force a peripheral trigger to a DMA channel.

Parameters

base	is the base address of the DMA channel control registers.

This function sets the peripheral trigger flag and if triggering a DMA burst is enabled (see DMA_enableTrigger()), a DMA burst transfer will be forced.

Returns
None.

13.2.3.6 static void DMA_clearTriggerFlag (uint32_t *base*) [inline], [static]

Clears a DMA channel's peripheral trigger flag.

Parameters

base	is the base address of the DMA channel control registers.

This function clears the peripheral trigger flag. Normally, you would use this function when initializing the DMA for the first time. The flag is cleared automatically when the DMA starts the first burst of a transfer.

Returns
None.

13.2.3.7 static bool DMA_getTriggerFlagStatus (uint32_t *base*) `[inline]`, `[static]`

Gets the status of a DMA channel's peripheral trigger flag.

Parameters

base	is the base address of the DMA channel control registers.

This function returns **true** if a peripheral trigger event has occurred The flag is automatically cleared when the first burst transfer begins, but if needed, it can be cleared using DMA_clearTriggerFlag().

Returns

Returns **true** if a peripheral trigger event has occurred and its flag is set. Returns **false** otherwise.

13.2.3.8 static void DMA_startChannel (uint32_t *base*) [inline], [static]

Starts a DMA channel.

Parameters

base	is the base address of the DMA channel control registers.

This function starts the DMA running, typically after you have configured it. It will wait for the first trigger event to start operation. To halt the channel use DMA_stopChannel().

Returns

None.

13.2.3.9 static void DMA_stopChannel (uint32_t *base*) [inline], [static]

Halts a DMA channel.

Parameters

base	is the base address of the DMA channel control registers.

This function halts the DMA at its current state and any current read-write access is completed. To start the channel again use DMA_startChannel().

Returns

None.

13.2.3.10 static void DMA_enableInterrupt (uint32_t *base*) [inline], [static]

Enables a DMA channel interrupt source.

Parameters

base	is the base address of the DMA channel control registers.

This function enables the indicated DMA channel interrupt source.

Returns

None.

13.2.3.11 static void DMA_disableInterrupt (uint32_t *base*) [inline], [static]

Disables a DMA channel interrupt source.

Parameters

base	is the base address of the DMA channel control registers.

This function disables the indicated DMA channel interrupt source.

Returns

None.

13.2.3.12 static void DMA_enableOverrunInterrupt (uint32_t *base*) [inline], [static]

Enables the DMA channel overrun interrupt.

Parameters

base	is the base address of the DMA channel control registers.

This function enables the indicated DMA channel's ability to generate an interrupt upon the detection of an overrun. An overrun is when a peripheral event trigger is received by the DMA before a previous trigger on that channel had been serviced and its flag had been cleared.

Note that this is the same interrupt signal as the interrupt that gets generated at the beginning/end of a transfer. That interrupt must first be enabled using DMA_enableInterrupt() in order for the overrun interrupt to be generated.

Returns

None.

13.2.3.13 static void DMA_disableOverrunInterrupt (uint32_t *base*) [inline], [static]

Disables the DMA channel overrun interrupt.

Parameters

base	is the base address of the DMA channel control registers.

This function disables the indicated DMA channel's ability to generate an interrupt upon the detection of an overrun.

Returns

None.

13.2.3.14 static void DMA_clearErrorFlag (uint32_t *base*) [inline], [static]

Clears the DMA channel error flags.

Parameters

base	is the base address of the DMA channel control registers.

This function clears both the DMA channel's sync error flag and its overrun error flag.

Returns

None.

13.2.3.15 static void DMA_setInterruptMode (uint32_t *base*, **DMA_InterruptMode** *mode*) [inline], [static]

Sets the interrupt generation mode of a DMA channel interrupt.

Parameters

base	is the base address of the DMA channel control registers.
mode	is a flag to indicate the channel interrupt mode.

This function sets the channel interrupt mode. When the *mode* parameter is **DMA_INT_AT_END**, the DMA channel interrupt will be generated at the end of the transfer. If **DMA_INT_AT_BEGINNING**, the interrupt will be generated at the beginning of a new transfer. Generating at the beginning of a new transfer is the default behavior.

Returns

None.

References DMA_INT_AT_END.

13.2.3.16 static void DMA_setPriorityMode (bool *ch1IsHighPri*) [inline], [static]

Sets the DMA channel priority mode.

Parameters

ch1IsHighPri	is a flag to indicate the channel interrupt mode.

This function sets the channel interrupt mode. When the *ch1IsHighPri* parameter is **false**, the DMA channels are serviced in round-robin mode. This is the default behavior.

If **true**, channel 1 will be given higher priority than the other channels. This means that if a channel 1 trigger occurs, the current word transfer on any other channel is completed and channel 1 is serviced for the complete burst count. The lower-priority channel's interrupted transfer will then resume.

Returns

None.

13.2.3.17 static void DMA_configSourceAddress (uint32_t *base*, const void ∗ *srcAddr*) [inline], [static]

Configures the source address for the DMA channel

Parameters

base	is the base address of the DMA channel control registers.
∗*srcAddr*	is a source address.

This function configures the source address of a DMA channel.

Returns

None.

13.2.3.18 static void DMA_configDestAddress (uint32_t *base*, const void ∗ *destAddr*) [inline], [static]

Configures the destination address for the DMA channel

Parameters

base	is the base address of the DMA channel control registers.
∗*destAddr*	is the destination address.

This function configures the destinaton address of a DMA channel.

Returns

None.

13.2.3.19 void DMA_configAddresses (uint32_t *base*, const void ∗ *destAddr*, const void ∗ *srcAddr*)

Configures the DMA channel

Parameters

base	is the base address of the DMA channel control registers.
∗*destAddr*	is the destination address.
∗*srcAddr*	is a source address.

This function configures the source and destination addresses of a DMA channel. The parameters are pointers to the data to be transferred.

Returns

None.

13.2.3.20 void DMA_configBurst (uint32_t *base*, uint16_t *size*, int16_t *srcStep*, int16_t *destStep*)

Configures the DMA channel's burst settings.

Parameters

base	is the base address of the DMA channel control registers.
size	is the number of words transferred per burst.
srcStep	is the amount to increment or decrement the source address after each word of a burst.
destStep	is the amount to increment or decrement the destination address after each word of a burst.

This function configures the size of each burst and the address step size.

The *size* parameter is the number of words that will be transferred during a single burst. Possible amounts range from 1 word to 32 words.

The *srcStep* and *destStep* parameters specify the address step that should be added to the source and destination addresses after each transferred word of a burst. Only signed values from -4096 to 4095 are valid.

Note

Note that regardless of what data size (configured by DMA_configMode()) is used, parameters are in terms of 16-bits words.

Returns

None.

13.2.3.21 void DMA_configTransfer (uint32_t *base,* uint32_t *transferSize,* int16_t *srcStep,* int16_t *destStep*)

Configures the DMA channel's transfer settings.

Parameters

base	is the base address of the DMA channel control registers.
transferSize	is the number of bursts per transfer.
srcStep	is the amount to increment or decrement the source address after each burst of a transfer unless a wrap occurs.
destStep	is the amount to increment or decrement the destination address after each burst of a transfer unless a wrap occurs.

This function configures the transfer size and the address step that is made after each burst.

The *transferSize* parameter is the number of bursts per transfer. If DMA channel interrupts are enabled, they will occur after this number of bursts have completed. The maximum number of bursts is 65536.

The *srcStep* and *destStep* parameters specify the address step that should be added to the source and destination addresses after each transferred burst of a transfer. Only signed values from -4096 to 4095 are valid. If a wrap occurs, these step values will be ignored. Wrapping is configured with DMA_configWrap().

Note

Note that regardless of what data size (configured by DMA_configMode()) is used, parameters are in terms of 16-bits words.

Returns

None.

13.2.3.22 void DMA_configWrap (uint32_t *base,* uint32_t *srcWrapSize,* int16_t *srcStep,* uint32_t *destWrapSize,* int16_t *destStep*)

Configures the DMA channel's wrap settings.

Parameters

base	is the base address of the DMA channel control registers.
srcWrapSize	is the number of bursts to be transferred before a wrap of the source address occurs.
srcStep	is the amount to increment or decrement the source address after each burst of a transfer unless a wrap occurs.
destWrapSize	is the number of bursts to be transferred before a wrap of the destination address occurs.
destStep	is the amount to increment or decrement the destination address after each burst of a transfer unless a wrap occurs.

This function configures the DMA channel's wrap settings.

The *srcWrapSize* and *destWrapSize* parameters are the number of bursts that are to be transferred before their respective addresses are wrapped. The maximum wrap size is 65536 bursts.

The *srcStep* and *destStep* parameters specify the address step that should be added to the source and destination addresses when the wrap occurs. Only signed values from -4096 to 4095 are valid.

Note

Note that regardless of what data size (configured by DMA_configMode()) is used, parameters are in terms of 16-bits words.

Returns

None.

13.2.3.23 void DMA_configMode (uint32_t *base,* **DMA_Trigger** *trigger,* uint32_t *config*)

Configures the DMA channel trigger and mode.

Parameters

base	is the base address of the DMA channel control registers.
trigger	is the interrupt source that triggers a DMA transfer.
config	is a bit field of several configuration selections.

This function configures the DMA channel's trigger and mode.

The *trigger* parameter is the interrupt source that will trigger the start of a DMA transfer.

The *config* parameter is the logical OR of the following values:

- **DMA_CFG_ONESHOT_DISABLE** or **DMA_CFG_ONESHOT_ENABLE**. If enabled, the subsequent burst transfers occur without additional event triggers after the first event trigger. If disabled, only one burst transfer is performed per event trigger.

- **DMA_CFG_CONTINUOUS_DISABLE** or **DMA_CFG_CONTINUOUS_ENABLE**. If enabled the DMA reinitializes when the transfer count is zero and waits for the next interrupt event trigger. If disabled, the DMA stops and clears the run status bit.
- **DMA_CFG_SIZE_16BIT** or **DMA_CFG_SIZE_32BIT**. This setting selects whether the databus width is 16 or 32 bits.

Returns

None.

14 ECAP Module

14.1 ECAP Introduction

The Enhanced Capture (eCAP) API provides a set of functions for configuring and using the eCAP module. Functions are provided to utilize both the capture and PWM capability of the eCAP module. The APIs allow for the selection and characterization of the input signal to be captured. A provision is also made to provide DMA trigger sources based on the eCAP events. The necessary APIs are also provided for PWM mode of operation.

14.2 API Functions

Macros

- #define ECAP_ISR_SOURCE_CAPTURE_EVENT_1
- #define ECAP_ISR_SOURCE_CAPTURE_EVENT_2
- #define ECAP_ISR_SOURCE_CAPTURE_EVENT_3
- #define ECAP_ISR_SOURCE_CAPTURE_EVENT_4
- #define ECAP_ISR_SOURCE_COUNTER_OVERFLOW
- #define ECAP_ISR_SOURCE_COUNTER_PERIOD
- #define ECAP_ISR_SOURCE_COUNTER_COMPARE

Enumerations

- enum ECAP_EmulationMode { ECAP_EMULATION_STOP, ECAP_EMULATION_RUN_TO_ZERO, ECAP_EMULATION_FREE_RUN }
- enum ECAP_CaptureMode { ECAP_CONTINUOUS_CAPTURE_MODE, ECAP_ONE_SHOT_CAPTURE_MODE }
- enum ECAP_Events { ECAP_EVENT_1, ECAP_EVENT_2, ECAP_EVENT_3, ECAP_EVENT_4 }
- enum ECAP_SyncOutMode { ECAP_SYNC_OUT_SYNCI, ECAP_SYNC_OUT_COUNTER_PRD, ECAP_SYNC_OUT_DISABLED }
- enum ECAP_APWMPolarity { ECAP_APWM_ACTIVE_HIGH, ECAP_APWM_ACTIVE_LOW }
- enum ECAP_EventPolarity { ECAP_EVNT_RISING_EDGE, ECAP_EVNT_FALLING_EDGE }

Functions

- static void ECAP_setEventPrescaler (uint32_t base, uint16_t preScalerValue)
- static void ECAP_setEventPolarity (uint32_t base, ECAP_Events event, ECAP_EventPolarity polarity)
- static void ECAP_setCaptureMode (uint32_t base, ECAP_CaptureMode mode, ECAP_Events event)

- static void ECAP_reArm (uint32_t base)
- static void ECAP_enableInterrupt (uint32_t base, uint16_t intFlags)
- static void ECAP_disableInterrupt (uint32_t base, uint16_t intFlags)
- static uint16_t ECAP_getInterruptSource (uint32_t base)
- static bool ECAP_getGlobalInterruptStatus (uint32_t base)
- static void ECAP_clearInterrupt (uint32_t base, uint16_t intFlags)
- static void ECAP_clearGlobalInterrupt (uint32_t base)
- static void ECAP_forceInterrupt (uint32_t base, uint16_t intFlags)
- static void ECAP_enableCaptureMode (uint32_t base)
- static void ECAP_enableAPWMMode (uint32_t base)
- static void ECAP_enableCounterResetOnEvent (uint32_t base, ECAP_Events event)
- static void ECAP_disableCounterResetOnEvent (uint32_t base, ECAP_Events event)
- static void ECAP_enableTimeStampCapture (uint32_t base)
- static void ECAP_disableTimeStampCapture (uint32_t base)
- static void ECAP_setPhaseShiftCount (uint32_t base, uint32_t shiftCount)
- static void ECAP_enableLoadCounter (uint32_t base)
- static void ECAP_disableLoadCounter (uint32_t base)
- static void ECAP_loadCounter (uint32_t base)
- static void ECAP_setSyncOutMode (uint32_t base, ECAP_SyncOutMode mode)
- static void ECAP_stopCounter (uint32_t base)
- static void ECAP_startCounter (uint32_t base)
- static void ECAP_setAPWMPolarity (uint32_t base, ECAP_APWMPolarity polarity)
- static void ECAP_setAPWMPeriod (uint32_t base, uint32_t periodCount)
- static void ECAP_setAPWMCompare (uint32_t base, uint32_t compareCount)
- static void ECAP_setAPWMShadowPeriod (uint32_t base, uint32_t periodCount)
- static void ECAP_setAPWMShadowCompare (uint32_t base, uint32_t compareCount)
- static uint32_t ECAP_getTimeBaseCounter (uint32_t base)
- static uint32_t ECAP_getEventTimeStamp (uint32_t base, ECAP_Events event)
- void ECAP_setEmulationMode (uint32_t base, ECAP_EmulationMode mode)

14.2.1 Detailed Description

The code for this module is contained in `driverlib/ecap.c`, with `driverlib/ecap.h` containing the API declarations for use by applications.

14.2.2 Macro Definition Documentation

14.2.2.1 #define ECAP_ISR_SOURCE_CAPTURE_EVENT_1

Event 1 ISR source

Referenced by ECAP_clearInterrupt(), ECAP_disableInterrupt(), ECAP_enableInterrupt(), and ECAP_forceInterrupt().

14.2.2.2 #define ECAP_ISR_SOURCE_CAPTURE_EVENT_2

Event 2 ISR source

Referenced by ECAP_clearInterrupt(), ECAP_disableInterrupt(), ECAP_enableInterrupt(), and ECAP_forceInterrupt().

14.2.2.3 #define ECAP_ISR_SOURCE_CAPTURE_EVENT_3

Event 3 ISR source

Referenced by ECAP_clearInterrupt(), ECAP_disableInterrupt(), ECAP_enableInterrupt(), and ECAP_forceInterrupt().

14.2.2.4 #define ECAP_ISR_SOURCE_CAPTURE_EVENT_4

Event 4 ISR source

Referenced by ECAP_clearInterrupt(), ECAP_disableInterrupt(), ECAP_enableInterrupt(), and ECAP_forceInterrupt().

14.2.2.5 #define ECAP_ISR_SOURCE_COUNTER_OVERFLOW

Counter overflow ISR source

Referenced by ECAP_clearInterrupt(), ECAP_disableInterrupt(), ECAP_enableInterrupt(), and ECAP_forceInterrupt().

14.2.2.6 #define ECAP_ISR_SOURCE_COUNTER_PERIOD

Counter equals period ISR source

Referenced by ECAP_clearInterrupt(), ECAP_disableInterrupt(), ECAP_enableInterrupt(), and ECAP_forceInterrupt().

14.2.2.7 #define ECAP_ISR_SOURCE_COUNTER_COMPARE

Counter equals compare ISR source

Referenced by ECAP_clearInterrupt(), ECAP_disableInterrupt(), ECAP_enableInterrupt(), and ECAP_forceInterrupt().

14.2.3 Enumeration Type Documentation

14.2.3.1 enum **ECAP_EmulationMode**

Values that can be passed to ECAP_setEmulationMode() as the *mode* parameter.

Enumerator

ECAP_EMULATION_STOP TSCTR is stopped on emulation suspension.

ECAP_EMULATION_RUN_TO_ZERO TSCTR runs until 0 before stopping on emulation suspension.

ECAP_EMULATION_FREE_RUN TSCTR is not affected by emulation suspension.

14.2.3.2 enum **ECAP_CaptureMode**

Values that can be passed to ECAP_setCaptureMode() as the *mode* parameter.

Enumerator

ECAP_CONTINUOUS_CAPTURE_MODE eCAP operates in continuous capture mode

ECAP_ONE_SHOT_CAPTURE_MODE eCAP operates in one shot capture mode

14.2.3.3 enum **ECAP_Events**

Values that can be passed to ECAP_setEventPolarity(), ECAP_setCaptureMode(), ECAP_enableCounterResetOnEvent(), ECAP_disableCounterResetOnEvent(), ECAP_getEventTimeStamp(), ECAP_setDMASource() as the *event* parameter.

Enumerator

ECAP_EVENT_1 eCAP event 1

ECAP_EVENT_2 eCAP event 2

ECAP_EVENT_3 eCAP event 3

ECAP_EVENT_4 eCAP event 4

14.2.3.4 enum **ECAP_SyncOutMode**

Values that can be passed to ECAP_setSyncOutMode() as the *mode* parameter.

Enumerator

ECAP_SYNC_OUT_SYNCI sync out on the sync in signal and software force

ECAP_SYNC_OUT_COUNTER_PRD sync out on counter equals period

ECAP_SYNC_OUT_DISABLED Disable sync out signal.

14.2.3.5 enum **ECAP_APWMPolarity**

Values that can be passed to ECAP_setAPWMPolarity() as the *polarity* parameter.

Enumerator

ECAP_APWM_ACTIVE_HIGH APWM is active high.

ECAP_APWM_ACTIVE_LOW APWM is active low.

14.2.3.6 enum **ECAP_EventPolarity**

Values that can be passed to ECAP_setEventPolarity() as the *polarity* parameter.

Enumerator

ECAP_EVNT_RISING_EDGE Rising edge polarity.

ECAP_EVNT_FALLING_EDGE Falling edge polarity.

14.2.4 Function Documentation

14.2.4.1 static void ECAP_setEventPrescaler (uint32_t *base,* uint16_t *preScalerValue*) [inline], [static]

Sets the input prescaler.

Parameters

base	is the base address of the ECAP module.
preScalerValue	is the pre scaler value for ECAP input

This function divides the ECAP input scaler. The pre scale value is doubled inside the module. For example a preScalerValue of 5 will divide the scaler by 10. Use a value of 1 to divide the pre scaler by 1. The value of preScalerValue should be less than **ECAP_MAX_PRESCALER_VALUE**.

Returns
None.

14.2.4.2 static void ECAP_setEventPolarity (uint32_t *base*, **ECAP_Events** *event*, **ECAP_EventPolarity** *polarity*) [inline], [static]

Sets the Capture event polarity.

Parameters

base	is the base address of the ECAP module.
event	is the event number.
polarity	is the polarity of the event.

This function sets the polarity of a given event. The value of event is between **ECAP_EVENT_1** and **ECAP_EVENT_4** inclusive corresponding to the four available events.For each event the polarity value determines the edge on which the capture is activated. For a rising edge use a polarity value of **ECAP_EVNT_RISING_EDGE** and for a falling edge use a polarity of **ECAP_EVNT_FALLING_EDGE**.

Returns
None.

14.2.4.3 static void ECAP_setCaptureMode (uint32_t *base*, **ECAP_CaptureMode** *mode*, **ECAP_Events** *event*) [inline], [static]

Sets the capture mode.

Parameters

base	is the base address of the ECAP module.
mode	is the capture mode.
event	is the event number at which the counter stops or wraps.

This function sets the eCAP module to a continuous or one-shot mode. The value of mode should be either **ECAP_CONTINUOUS_CAPTURE_MODE** or **ECAP_ONE_SHOT_CAPTURE_MODE** corresponding to continuous or one-shot mode respectively.

The value of event determines the event number at which the counter stops (in one-shot mode) or the counter wraps (in continuous mode). The value of event should be between **ECAP_EVENT_1** and **ECAP_EVENT_4** corresponding to the valid event numbers.

Returns
None.

14.2.4.4 static void ECAP_reArm (uint32_t *base*) [inline], [static]

Re-arms the eCAP module.

Parameters

base	is the base address of the ECAP module.

This function re-arms the eCAP module.

Returns

None.

14.2.4.5 static void ECAP_enableInterrupt (uint32_t *base*, uint16_t *intFlags*) [inline], [static]

Enables interrupt source.

Parameters

base	is the base address of the ECAP module.
intFlags	is the interrupt source to be enabled.

This function sets and enables eCAP interrupt source. The following are valid interrupt sources.

- ECAP_ISR_SOURCE_CAPTURE_EVENT_1 - Event 1 generates interrupt
- ECAP_ISR_SOURCE_CAPTURE_EVENT_2 - Event 2 generates interrupt
- ECAP_ISR_SOURCE_CAPTURE_EVENT_3 - Event 3 generates interrupt
- ECAP_ISR_SOURCE_CAPTURE_EVENT_4 - Event 4 generates interrupt
- ECAP_ISR_SOURCE_COUNTER_OVERFLOW - Counter overflow generates interrupt
- ECAP_ISR_SOURCE_COUNTER_PERIOD - Counter equal period generates interrupt
- ECAP_ISR_SOURCE_COUNTER_COMPARE - Counter equal compare generates interrupt

Returns

None.

References ECAP_ISR_SOURCE_CAPTURE_EVENT_1, ECAP_ISR_SOURCE_CAPTURE_EVENT_2, ECAP_ISR_SOURCE_CAPTURE_EVENT_3, ECAP_ISR_SOURCE_CAPTURE_EVENT_4, ECAP_ISR_SOURCE_COUNTER_COMPARE, ECAP_ISR_SOURCE_COUNTER_OVERFLOW, and ECAP_ISR_SOURCE_COUNTER_PERIOD.

14.2.4.6 static void ECAP_disableInterrupt (uint32_t *base*, uint16_t *intFlags*) [inline], [static]

Disables interrupt source.

Parameters

base	is the base address of the ECAP module.
intFlags	is the interrupt source to be disabled.

This function clears and disables eCAP interrupt source. The following are valid interrupt sources.

- ECAP_ISR_SOURCE_CAPTURE_EVENT_1 - Event 1 generates interrupt
- ECAP_ISR_SOURCE_CAPTURE_EVENT_2 - Event 2 generates interrupt

- ECAP_ISR_SOURCE_CAPTURE_EVENT_3 - Event 3 generates interrupt
- ECAP_ISR_SOURCE_CAPTURE_EVENT_4 - Event 4 generates interrupt
- ECAP_ISR_SOURCE_COUNTER_OVERFLOW - Counter overflow generates interrupt
- ECAP_ISR_SOURCE_COUNTER_PERIOD - Counter equal period generates interrupt
- ECAP_ISR_SOURCE_COUNTER_COMPARE - Counter equal compare generates interrupt

Returns

None.

References ECAP_ISR_SOURCE_CAPTURE_EVENT_1, ECAP_ISR_SOURCE_CAPTURE_EVENT_2, ECAP_ISR_SOURCE_CAPTURE_EVENT_3, ECAP_ISR_SOURCE_CAPTURE_EVENT_4, ECAP_ISR_SOURCE_COUNTER_COMPARE, ECAP_ISR_SOURCE_COUNTER_OVERFLOW, and ECAP_ISR_SOURCE_COUNTER_PERIOD.

14.2.4.7 static uint16_t ECAP_getInterruptSource (uint32_t *base*) [inline], [static]

Returns the interrupt flag.

Parameters

base	is the base address of the ECAP module.

This function returns the eCAP interrupt flag. The following are valid interrupt sources corresponding to the eCAP interrupt flag.

Returns

Returns the eCAP interrupt that has occurred. The following are valid return values.

- ECAP_ISR_SOURCE_CAPTURE_EVENT_1 - Event 1 generates interrupt
- ECAP_ISR_SOURCE_CAPTURE_EVENT_2 - Event 2 generates interrupt
- ECAP_ISR_SOURCE_CAPTURE_EVENT_3 - Event 3 generates interrupt
- ECAP_ISR_SOURCE_CAPTURE_EVENT_4 - Event 4 generates interrupt
- ECAP_ISR_SOURCE_COUNTER_OVERFLOW - Counter overflow generates interrupt
- ECAP_ISR_SOURCE_COUNTER_PERIOD - Counter equal period generates interrupt
- ECAP_ISR_SOURCE_COUNTER_COMPARE - Counter equal compare generates interrupt

Note

- User can check if a combination of various interrupts have occurred by ORing the above return values.

14.2.4.8 static bool ECAP_getGlobalInterruptStatus (uint32_t *base*) [inline], [static]

Returns the Global interrupt flag.

Parameters

base	is the base address of the ECAP module.

This function returns the eCAP Global interrupt flag.

Returns

Returns true if there is a global eCAP interrupt, false otherwise.

14.2.4.9 static void ECAP_clearInterrupt (uint32_t *base,* uint16_t *intFlags*) [inline], [static]

Clears interrupt flag.

Parameters

base	is the base address of the ECAP module.
intFlags	is the interrupt source.

This function clears eCAP interrupt flags. The following are valid interrupt sources.

- ECAP_ISR_SOURCE_CAPTURE_EVENT_1 - Event 1 generates interrupt
- ECAP_ISR_SOURCE_CAPTURE_EVENT_2 - Event 2 generates interrupt
- ECAP_ISR_SOURCE_CAPTURE_EVENT_3 - Event 3 generates interrupt
- ECAP_ISR_SOURCE_CAPTURE_EVENT_4 - Event 4 generates interrupt
- ECAP_ISR_SOURCE_COUNTER_OVERFLOW - Counter overflow generates interrupt
- ECAP_ISR_SOURCE_COUNTER_PERIOD - Counter equal period generates interrupt
- ECAP_ISR_SOURCE_COUNTER_COMPARE - Counter equal compare generates interrupt

Returns

None.

References ECAP_ISR_SOURCE_CAPTURE_EVENT_1, ECAP_ISR_SOURCE_CAPTURE_EVENT_2, ECAP_ISR_SOURCE_CAPTURE_EVENT_3, ECAP_ISR_SOURCE_CAPTURE_EVENT_4, ECAP_ISR_SOURCE_COUNTER_COMPARE, ECAP_ISR_SOURCE_COUNTER_OVERFLOW, and ECAP_ISR_SOURCE_COUNTER_PERIOD.

14.2.4.10 static void ECAP_clearGlobalInterrupt (uint32_t *base*) [inline], [static]

Clears global interrupt flag

Parameters

base	is the base address of the ECAP module.

This function clears the global interrupt bit.

Returns

None.

14.2.4.11 static void ECAP_forceInterrupt (uint32_t *base,* uint16_t *intFlags*) [inline], [static]

Forces interrupt source.

Parameters

base	is the base address of the ECAP module.
intFlags	is the interrupt source.

This function forces and enables eCAP interrupt source. The following are valid interrupt sources.

- ECAP_ISR_SOURCE_CAPTURE_EVENT_1 - Event 1 generates interrupt
- ECAP_ISR_SOURCE_CAPTURE_EVENT_2 - Event 2 generates interrupt
- ECAP_ISR_SOURCE_CAPTURE_EVENT_3 - Event 3 generates interrupt
- ECAP_ISR_SOURCE_CAPTURE_EVENT_4 - Event 4 generates interrupt
- ECAP_ISR_SOURCE_COUNTER_OVERFLOW - Counter overflow generates interrupt
- ECAP_ISR_SOURCE_COUNTER_PERIOD - Counter equal period generates interrupt
- ECAP_ISR_SOURCE_COUNTER_COMPARE - Counter equal compare generates interrupt

Returns

None.

References ECAP_ISR_SOURCE_CAPTURE_EVENT_1, ECAP_ISR_SOURCE_CAPTURE_EVENT_2, ECAP_ISR_SOURCE_CAPTURE_EVENT_3, ECAP_ISR_SOURCE_CAPTURE_EVENT_4, ECAP_ISR_SOURCE_COUNTER_COMPARE, ECAP_ISR_SOURCE_COUNTER_OVERFLOW, and ECAP_ISR_SOURCE_COUNTER_PERIOD.

14.2.4.12 static void ECAP_enableCaptureMode (uint32_t *base*) `[inline]`, `[static]`

Sets eCAP in Capture mode.

Parameters

base	is the base address of the ECAP module.

This function sets the eCAP module to operate in Capture mode.

Returns

None.

14.2.4.13 static void ECAP_enableAPWMMode (uint32_t *base*) `[inline]`, `[static]`

Sets eCAP in APWM mode.

Parameters

base	is the base address of the ECAP module.

This function sets the eCAP module to operate in APWM mode.

Returns

None.

14.2.4.14 static void ECAP_enableCounterResetOnEvent (uint32_t *base*, **ECAP_Events** *event*) [inline], [static]

Enables counter reset on an event.

Parameters

base	is the base address of the ECAP module.
event	is the event number the time base gets reset.

This function enables the base timer, TSCTR, to be reset on capture event provided by the variable event. Valid inputs for event are **ECAP_EVENT_1** to **ECAP_EVENT_4**.

Returns
None.

14.2.4.15 static void ECAP_disableCounterResetOnEvent (uint32_t *base*, **ECAP_Events** *event*) [inline], [static]

Disables counter reset on events.

Parameters

base	is the base address of the ECAP module.
event	is the event number the time base gets reset.

This function disables the base timer, TSCTR, from being reset on capture event provided by the variable event. Valid inputs for event are **ECAP_EVENT_1** to **ECAP_EVENT_4**.

Returns
None.

14.2.4.16 static void ECAP_enableTimeStampCapture (uint32_t *base*) [inline], [static]

Enables time stamp capture.

Parameters

base	is the base address of the ECAP module.

This function enables time stamp count to be captured

Returns
None.

14.2.4.17 static void ECAP_disableTimeStampCapture (uint32_t *base*) [inline], [static]

Disables time stamp capture.

Parameters

base	is the base address of the ECAP module.

This function disables time stamp count to be captured

Returns
None.

14.2.4.18 static void ECAP_setPhaseShiftCount (uint32_t *base*, uint32_t *shiftCount*) [inline], [static]

Sets a phase shift value count.

Parameters

base	is the base address of the ECAP module.
shiftCount	is the phase shift value.

This function writes a phase shift value to be loaded into the main time stamp counter.

Returns
None.

14.2.4.19 static void ECAP_enableLoadCounter (uint32_t *base*) [inline], [static]

Enable counter loading with phase shift value.

Parameters

base	is the base address of the ECAP module.

This function enables loading of the counter with the value present in the phase shift counter as defined by the ECAP_setPhaseShiftCount() function.

Returns
None.

14.2.4.20 static void ECAP_disableLoadCounter (uint32_t *base*) [inline], [static]

Disable counter loading with phase shift value.

Parameters

base	is the base address of the ECAP module.

This function disables loading of the counter with the value present in the phase shift counter as defined by the ECAP_setPhaseShiftCount() function.

Returns
None.

14.2.4.21 static void ECAP_loadCounter (uint32_t *base*) [inline], [static]

Load time stamp counter

Parameters

base	is the base address of the ECAP module.

This function forces the value in the phase shift counter register to be loaded into Time stamp counter register. Make sure to enable loading of Time stamp counter by calling ECAP_enableLoadCounter() function before calling this function.

Returns

None.

14.2.4.22 static void ECAP_setSyncOutMode (uint32_t *base*, **ECAP_SyncOutMode** *mode*) [inline], [static]

Configures Sync out signal mode.

Parameters

base	is the base address of the ECAP module.
mode	is the sync out mode.

This function sets the sync out mode. Valid parameters for mode are:

- ECAP_SYNC_OUT_SYNCI - Trigger sync out on sync-in event.
- ECAP_SYNC_OUT_COUNTER_PRD - Trigger sync out when counter equals period.
- ECAP_SYNC_OUT_DISABLED - Disable sync out.

Returns

None.

14.2.4.23 static void ECAP_stopCounter (uint32_t *base*) [inline], [static]

Stops Time stamp counter.

Parameters

base	is the base address of the ECAP module.

This function stops the time stamp counter.

Returns

None.

14.2.4.24 static void ECAP_startCounter (uint32_t *base*) [inline], [static]

Starts Time stamp counter.

Parameters

base	is the base address of the ECAP module.

This function starts the time stamp counter.

Returns
None.

14.2.4.25 static void ECAP_setAPWMPolarity (uint32_t *base*, **ECAP_APWMPolarity** *polarity*) [inline], [static]

Set eCAP APWM polarity.

Parameters

base	is the base address of the ECAP module.
polarity	is the polarity of APWM

This function sets the polarity of the eCAP in APWM mode. Valid inputs for polarity are:

- ECAP_APWM_ACTIVE_HIGH - For active high.
- ECAP_APWM_ACTIVE_LOW - For active low.

Returns
None.

14.2.4.26 static void ECAP_setAPWMPeriod (uint32_t *base*, uint32_t *periodCount*) [inline], [static]

Set eCAP APWM period.

Parameters

base	is the base address of the ECAP module.
periodCount	is the period count for APWM.

This function sets the period count of the APWM waveform. periodCount takes the actual count which is written to the register. The user is responsible for converting the desired frequency or time into the period count.

Returns
None.

14.2.4.27 static void ECAP_setAPWMCompare (uint32_t *base*, uint32_t *compareCount*) [inline], [static]

Set eCAP APWM on or off time count.

Parameters

base	is the base address of the ECAP module.
compareCount	is the on or off count for APWM.

This function sets the on or off time count of the APWM waveform depending on the polarity of the output. If the output , as set by ECAP_setAPWMPolarity(), is active high then compareCount determines the on time. If the output is active low then compareCount determines the off time. compareCount takes the actual count which is written to the register. The user is responsible for converting the desired frequency or time into the appropriate count value.

Returns

None.

14.2.4.28 static void ECAP_setAPWMShadowPeriod (uint32_t *base,* uint32_t *periodCount*) [inline], [static]

Load eCAP APWM shadow period.

Parameters

base	is the base address of the ECAP module.
periodCount	is the shadow period count for APWM.

This function sets the shadow period count of the APWM waveform. periodCount takes the actual count which is written to the register. The user is responsible for converting the desired frequency or time into the period count.

Returns

None.

14.2.4.29 static void ECAP_setAPWMShadowCompare (uint32_t *base,* uint32_t *compareCount*) [inline], [static]

Set eCAP APWM shadow on or off time count.

Parameters

base	is the base address of the ECAP module.
compareCount	is the on or off count for APWM.

This function sets the shadow on or off time count of the APWM waveform depending on the polarity of the output. If the output , as set by ECAP_setAPWMPolarity() , is active high then compareCount determines the on time. If the output is active low then compareCount determines the off time. compareCount takes the actual count which is written to the register. The user is responsible for converting the desired frequency or time into the appropriate count value.

Returns

None.

14.2.4.30 static uint32_t ECAP_getTimeBaseCounter (uint32_t *base*) [static]

Returns the time base counter value.

Parameters

base	is the base address of the ECAP module.

This function returns the time base counter value.

Returns

Returns the time base counter value.

14.2.4.31 static uint32_t ECAP_getEventTimeStamp (uint32_t *base*, **ECAP_Events** *event*) [inline], [static]

Returns event time stamp.

Parameters

base	is the base address of the ECAP module.
event	is the event number.

This function returns the current time stamp count of the given event. Valid values for event are **ECAP_EVENT_1** to **ECAP_EVENT_4**.

Returns

Event time stamp value or 0 if *event* is invalid.

References ECAP_EVENT_1, ECAP_EVENT_2, ECAP_EVENT_3, and ECAP_EVENT_4.

14.2.4.32 void ECAP_setEmulationMode (uint32_t *base*, **ECAP_EmulationMode** *mode*)

Configures emulation mode.

Parameters

base	is the base address of the ECAP module.
mode	is the emulation mode.

This function configures the eCAP counter, TSCTR, to the desired emulation mode when emulation suspension occurs. Valid inputs for mode are:

- ECAP_EMULATION_STOP - Counter is stopped immediately.
- ECAP_EMULATION_RUN_TO_ZERO - Counter runs till it reaches 0.
- ECAP_EMULATION_FREE_RUN - Counter is not affected.

Returns

None.

15 EMIF Module

15.1 EMIF Introduction

The external memory interface (EMIF) API provides a set of functions to configure device's EMIF module. The driver provides functions to initialize the module, configure external memory parameters, obtain status information and to manage interrupts. APIs for both asynchronous and synchronous modes are supported.

15.2 API Functions

Data Structures

- struct EMIF_AsyncTimingParams
- struct EMIF_SyncConfig
- struct EMIF_SyncTimingParams

Macros

- #define EMIF_ACCPROT0_FETCHPROT
- #define EMIF_ACCPROT0_CPUWRPROT
- #define EMIF_ACCPROT0_DMAWRPROT
- #define EMIF_ASYNC_INT_AT
- #define EMIF_ASYNC_INT_LT
- #define EMIF_ASYNC_INT_WR

Enumerations

- enum EMIF_AsyncCSOffset { EMIF_ASYNC_CS2_OFFSET, EMIF_ASYNC_CS3_OFFSET, EMIF_ASYNC_CS4_OFFSET }
- enum EMIF_AsyncDataWidth { EMIF_ASYNC_DATA_WIDTH_8, EMIF_ASYNC_DATA_WIDTH_16, EMIF_ASYNC_DATA_WIDTH_32 }
- enum EMIF_AsyncMode { EMIF_ASYNC_STROBE_MODE, EMIF_ASYNC_NORMAL_MODE }
- enum EMIF_AsyncWaitPolarity { EMIF_ASYNC_WAIT_POLARITY_LOW, EMIF_ASYNC_WAIT_POLARITY_HIGH }
- enum EMIF_MasterSelect { EMIF_MASTER_CPU1_NG, EMIF_MASTER_CPU1_G, EMIF_MASTER_CPU2_G, EMIF_MASTER_CPU1_NG2 }
- enum EMIF_SyncNarrowMode { EMIF_SYNC_NARROW_MODE_TRUE, EMIF_SYNC_NARROW_MODE_FALSE }
- enum EMIF_SyncBank { EMIF_SYNC_BANK_1, EMIF_SYNC_BANK_2, EMIF_SYNC_BANK_4 }
- enum EMIF_SyncCASLatency { EMIF_SYNC_CAS_LAT_2, EMIF_SYNC_CAS_LAT_3 }

- enum EMIF_SyncPageSize { EMIF_SYNC_COLUMN_WIDTH_8, EMIF_SYNC_COLUMN_WIDTH_9, EMIF_SYNC_COLUMN_WIDTH_10, EMIF_SYNC_COLUMN_WIDTH_11 }

Functions

- static void EMIF_selectMaster (uint32_t configBase, EMIF_MasterSelect select)
- static void EMIF_setAccessProtection (uint32_t configBase, uint16_t access)
- static void EMIF_commitAccessConfig (uint32_t configBase)
- static void EMIF_lockAccessConfig (uint32_t configBase)
- static void EMIF_unlockAccessConfig (uint32_t configBase)
- static void EMIF_setAsyncMode (uint32_t base, EMIF_AsyncCSOffset offset, EMIF_AsyncMode mode)
- static void EMIF_enableAsyncExtendedWait (uint32_t base, EMIF_AsyncCSOffset offset)
- static void EMIF_disableAsyncExtendedWait (uint32_t base, EMIF_AsyncCSOffset offset)
- static void EMIF_setAsyncWaitPolarity (uint32_t base, EMIF_AsyncWaitPolarity polarity)
- static void EMIF_setAsyncMaximumWaitCycles (uint32_t base, uint16_t value)
- static void EMIF_setAsyncTimingParams (uint32_t base, EMIF_AsyncCSOffset offset, const EMIF_AsyncTimingParams ∗tParam)
- static void EMIF_setAsyncDataBusWidth (uint32_t base, EMIF_AsyncCSOffset offset, EMIF_AsyncDataWidth width)
- static void EMIF_enableAsyncInterrupt (uint32_t base, uint16_t intFlags)
- static void EMIF_disableAsyncInterrupt (uint32_t base, uint16_t intFlags)
- static uint16_t EMIF_getAsyncInterruptStatus (uint32_t base)
- static void EMIF_clearAsyncInterruptStatus (uint32_t base, uint16_t intFlags)
- static void EMIF_setSyncTimingParams (uint32_t base, const EMIF_SyncTimingParams ∗tParam)
- static void EMIF_setSyncSelfRefreshExitTmng (uint32_t base, uint16_t tXs)
- static void EMIF_setSyncRefreshRate (uint32_t base, uint16_t refRate)
- static void EMIF_setSyncMemoryConfig (uint32_t base, const EMIF_SyncConfig ∗config)
- static void EMIF_enableSyncSelfRefresh (uint32_t base)
- static void EMIF_disableSyncSelfRefresh (uint32_t base)
- static void EMIF_enableSyncPowerDown (uint32_t base)
- static void EMIF_disableSyncPowerDown (uint32_t base)
- static void EMIF_enableSyncRefreshInPowerDown (uint32_t base)
- static void EMIF_disableSyncRefreshInPowerDown (uint32_t base)
- static uint32_t EMIF_getSyncTotalAccesses (uint32_t base)
- static uint32_t EMIF_getSyncTotalActivateAccesses (uint32_t base)

15.2.1 Detailed Description

The EMIF API include functions to select master for EMIF module, set, lock/unlock, commit access configuration, set external asynchronous and synchronous memory configuration parameters and to manage asynchronous interrupts.

For interfacing asynchronous memories, functions are provided to configure EMIF registers to set mode of operation to strobe or normal mode, set enable/disable extended wait mode, set wait polarity, set maximum wait cycles, set async memory timing parameters, set memory data bus width as per the external memory to be interfaced and enable/disable, clear and get status for interrupts.

For interfacing synchronous memories, functions are provided to configure EMIF registers to set timing parameters, set self refresh exit timing, set refresh rate, set other memory specific parameters based on the external memory to be interfaced, enable/disable self refresh mode, enable/disable power down mode, enable/disable refresh in power down mode and to get total number of SDRAM accesses.

The code for this module is contained in `driverlib/emif.c`, with `driverlib/emif.h` containing the API declarations for use by applications.

15.2.2 Macro Definition Documentation

15.2.2.1 #define EMIF_ACCPROT0_FETCHPROT

This flag is used to specify whether CPU fetches are allowed/blocked for EMIF.

15.2.2.2 #define EMIF_ACCPROT0_CPUWRPROT

This flag is used to specify whether CPU writes are allowed/blocked for EMIF.

15.2.2.3 #define EMIF_ACCPROT0_DMAWRPROT

This flag is used to specify whether DMA writes are allowed/blocked for EMIF. It is valid only for EMIF1 instance.

15.2.2.4 #define EMIF_ASYNC_INT_AT

This flag is used to allow/block EMIF to generate Masked Asynchronous Timeout interrupt.

15.2.2.5 #define EMIF_ASYNC_INT_LT

This flag is used to allow/block EMIF to generate Masked Line Trap interrupt.

15.2.2.6 #define EMIF_ASYNC_INT_WR

This flag is used to allow/block EMIF to generate Masked Wait Rise interrupt.

15.2.3 Enumeration Type Documentation

15.2.3.1 enum **EMIF_AsyncCSOffset**

Values that can be passed to EMIF_setAsyncMode(), EMIF_setAsyncTimingParams(), EMIF_setAsyncDataBusWidth(), EMIF_enableAsyncExtendedWait() and EMIF_disableAsyncExtendedWait() as the *offset* parameter. Three chip selects are available in asynchronous memory interface so there are three configuration registers available for each EMIF instance. All the three chip select offsets are valid for EMIF1 while only EMIF_ASYNC_CS2_OFFSET is valid for EMIF2.

Enumerator

EMIF_ASYNC_CS2_OFFSET Async chip select 2 offset.

EMIF_ASYNC_CS3_OFFSET Async chip select 3 offset.

EMIF_ASYNC_CS4_OFFSET Async chip select 4 offset.

15.2.3.2 enum **EMIF_AsyncDataWidth**

Values that can be passed to EMIF_setAsyncDataBusWidth() as the *width* parameter.

Enumerator

EMIF_ASYNC_DATA_WIDTH_8 ASRAM/FLASH with 8 bit data bus.

EMIF_ASYNC_DATA_WIDTH_16 ASRAM/FLASH with 16 bit data bus.

EMIF_ASYNC_DATA_WIDTH_32 ASRAM/FLASH with 32 bit data bus.

15.2.3.3 enum **EMIF_AsyncMode**

Values that can be passed to EMIF_setAsyncMode() as the *mode* parameter.

Enumerator

EMIF_ASYNC_STROBE_MODE Enables ASRAM/FLASH strobe mode.

EMIF_ASYNC_NORMAL_MODE Disables ASRAM/FLASH strobe mode.

15.2.3.4 enum **EMIF_AsyncWaitPolarity**

Values that can be passed to EMIF_setAsyncWaitPolarity() as the *polarity* parameter.

Enumerator

EMIF_ASYNC_WAIT_POLARITY_LOW EMxWAIT pin polarity is low.

EMIF_ASYNC_WAIT_POLARITY_HIGH EMxWAIT pin polarity is high.

15.2.3.5 enum **EMIF_MasterSelect**

Values that can be passed to EMIF_selectMaster() as the *select* parameter.

Enumerator

EMIF_MASTER_CPU1_NG CPU1 is master but not grabbed.

EMIF_MASTER_CPU1_G CPU1 is master & grabbed.

EMIF_MASTER_CPU2_G CPU2 is master & grabbed.

EMIF_MASTER_CPU1_NG2 CPU1 is master but not grabbed.

15.2.3.6 enum **EMIF_SyncNarrowMode**

Values that can be passed to EMIF_setSyncMemoryConfig() as the *config* parameter member.

Enumerator

EMIF_SYNC_NARROW_MODE_TRUE MemBusWidth=SystemBusWidth/2.

EMIF_SYNC_NARROW_MODE_FALSE MemBusWidth=SystemBusWidth.

15.2.3.7 enum **EMIF_SyncBank**

Values that can be passed to EMIF_setSyncMemoryConfig() as the *config* parameter member.

Enumerator

EMIF_SYNC_BANK_1 1 Bank SDRAM device

EMIF_SYNC_BANK_2 2 Bank SDRAM device

EMIF_SYNC_BANK_4 4 Bank SDRAM device

15.2.3.8 enum **EMIF_SyncCASLatency**

Values that can be passed to EMIF_setSyncMemoryConfig() as the *config* parameter member.

Enumerator

EMIF_SYNC_CAS_LAT_2 SDRAM with CAS Latency 2.

EMIF_SYNC_CAS_LAT_3 SDRAM with CAS Latency 3.

15.2.3.9 enum **EMIF_SyncPageSize**

Values that can be passed to EMIF_setSyncMemoryConfig() as the *config* parameter member.

Enumerator

EMIF_SYNC_COLUMN_WIDTH_8 256-word pages in SDRAM

EMIF_SYNC_COLUMN_WIDTH_9 512-word pages in SDRAM

EMIF_SYNC_COLUMN_WIDTH_10 1024-word pages in SDRAM

EMIF_SYNC_COLUMN_WIDTH_11 2048-word pages in SDRAM

15.2.4 Function Documentation

15.2.4.1 static void EMIF_selectMaster (uint32_t *configBase,* **EMIF_MasterSelect** *select*) `[inline]`, `[static]`

Selects the EMIF Master.

Parameters

configBase	is the configuration address of the EMIF instance used.
select	is the required master configuration for EMIF1.

This function selects the master for an EMIF1 instance among CPU1 or CPU2. *It is valid only for EMIF1 instance and not for EMIF2 instance. Valid value for configBase parameter is EMIF1CONFIG_BASE.* Valid values for select parameter can be *EMIF_MASTER_CPU1_NG*, *EMIF_MASTER_CPU1_G*, *EMIF_MASTER_CPU2_G* or *EMIF_MASTER_CPU1_NG2*.

Returns

None.

15.2.4.2 static void EMIF_setAccessProtection (uint32_t *configBase,* uint16_t *access*) [inline], [static]

Sets the access protection.

Parameters

configBase	is the configuration address of the EMIF instance used.
access	is the required access protection configuration.

This function sets the access protection for an EMIF instance from CPU and DMA. The *access* parameter can be any of **EMIF_ACCPROT0_FETCHPROT**, **EMIF_ACCPROT0_CPUWRPROT** **EMIF_ACCPROT0_DMAWRPROT** values or their combination.
EMIF_ACCPROT0_DMAWRPROT value is valid as access parameter for EMIF1 instance only .

Returns

None.

15.2.4.3 static void EMIF_commitAccessConfig (uint32_t *configBase*) [inline], [static]

Commits the lock configuration.

Parameters

configBase	is the configuration address of the EMIF instance used.

This function commits the access protection for an EMIF instance from CPU & DMA.

Returns

None.

15.2.4.4 static void EMIF_lockAccessConfig (uint32_t *configBase*) [inline], [static]

Locks the write to access configuration fields.

Parameters

configBase	is the configuration address of the EMIF instance used.

This function locks the write to access configuration fields i.e ACCPROT0 & Mselect fields, for an EMIF instance.

Returns
None.

15.2.4.5 static void EMIF_unlockAccessConfig (uint32_t *configBase*) [inline], [static]

Unlocks the write to access configuration fields.

Parameters

configBase	is the configuration address of the EMIF instance used.

This function unlocks the write to access configuration fields i.e. ACCPROT0 & Mselect fields, for an EMIF instance.

Returns
None.

15.2.4.6 static void EMIF_setAsyncMode (uint32_t *base*, **EMIF_AsyncCSOffset** *offset*, **EMIF_AsyncMode** *mode*) [inline], [static]

Selects the asynchronous mode of operation.

Parameters

base	is the base address of the EMIF instance used.
offset	is the offset of asynchronous chip select of EMIF instance.
mode	is the desired mode of operation for external memory.

This function sets the mode of operation for asynchronous memory between Normal or Strobe mode. Valid values for param *offset* can be *EMIF_ASYNC_CS2_OFFSET*, *EMIF_ASYNC_CS3_OFFSET* & *EMIF_ASYNC_C43_OFFSET* for EMIF1 and *EMIF_ASYNC_CS2_OFFSET* for EMIF2. Valid values for param *mode* can be *EMIF_ASYNC_STROBE_MODE* or *EMIF_ASYNC_NORMAL_MODE*.

Returns
None.

References EMIF_ASYNC_CS2_OFFSET.

15.2.4.7 static void EMIF_enableAsyncExtendedWait (uint32_t *base*, **EMIF_AsyncCSOffset** *offset*) [inline], [static]

Enables the Extended Wait Mode.

Parameters

base	is the base address of the EMIF instance used.
offset	is the offset of asynchronous chip select of the EMIF instance

This function enables the extended wait mode for an asynchronous external memory.Valid values for param *offset* can be *EMIF_ASYNC_CS2_OFFSET*, *EMIF_ASYNC_CS3_OFFSET* & *EMIF_ASYNC_C43_OFFSET* for EMIF1 and *EMIF_ASYNC_CS2_OFFSET* for EMIF2.

Returns

None.

References EMIF_ASYNC_CS2_OFFSET.

15.2.4.8 static void EMIF_disableAsyncExtendedWait (uint32_t *base*, **EMIF_AsyncCSOffset** *offset*) [inline], [static]

Disables the Extended Wait Mode.

Parameters

base	is the base address of the EMIF instance used.
offset	is the offset of asynchronous chip select of EMIF instance.

This function disables the extended wait mode for an asynchronous external memory.Valid values for param *offset* can be *EMIF_ASYNC_CS2_OFFSET*, *EMIF_ASYNC_CS3_OFFSET* & *EMIF_ASYNC_C43_OFFSET* for EMIF1 and *EMIF_ASYNC_CS2_OFFSET* for EMIF2.

Returns

None.

References EMIF_ASYNC_CS2_OFFSET.

15.2.4.9 static void EMIF_setAsyncWaitPolarity (uint32_t *base*, **EMIF_AsyncWaitPolarity** *polarity*) [inline], [static]

Sets the wait polarity.

Parameters

base	is the base address of the EMIF instance used.
polarity	is desired wait polarity.

This function sets the wait polarity for an asynchronous external memory. Valid values for param *polarity* can be *EMIF_ASYNC_WAIT_POLARITY_LOW* or *EMIF_ASYNC_WAIT_POLARITY_HIGH*.

Returns

None.

15.2.4.10 static void EMIF_setAsyncMaximumWaitCycles (uint32_t *base*, uint16_t *value*) [inline], [static]

Sets the Maximum Wait Cycles.

Parameters

base	is the base address of the EMIF instance used.
value	is the desired maximum wait cycles.

This function sets the maximum wait cycles for extended asynchronous cycle. Valid values for parameter *value* lies b/w 0x0U-0xFFU or 0-255.

Returns

None.

15.2.4.11 static void EMIF_setAsyncTimingParams (uint32_t *base*, **EMIF_AsyncCSOffset** *offset*, const **EMIF_AsyncTimingParams** ∗ *tParam*) [inline], [static]

Sets the Asynchronous Memory Timing Characteristics.

Parameters

base	is the base address of the EMIF instance used.
offset	is the offset of asynchronous chip select of EMIF instance.
tParam	is the desired timing parameters.

This function sets timing characteristics for an external asynchronous memory to be interfaced. Valid values for param *offset* can be *EMIF_ASYNC_CS2_OFFSET*, *EMIF_ASYNC_CS3_OFFSET* and *EMIF_ASYNC_C43_OFFSET* for EMIF1 & EMIF_ASYNC_CS2_OFFSET for EMIF2.

Returns

None.

References EMIF_ASYNC_CS2_OFFSET, EMIF_AsyncTimingParams::rHold, EMIF_AsyncTimingParams::rSetup, EMIF_AsyncTimingParams::rStrobe, EMIF_AsyncTimingParams::turnArnd, EMIF_AsyncTimingParams::wHold, EMIF_AsyncTimingParams::wSetup, and EMIF_AsyncTimingParams::wStrobe.

15.2.4.12 static void EMIF_setAsyncDataBusWidth (uint32_t *base*, **EMIF_AsyncCSOffset** *offset*, **EMIF_AsyncDataWidth** *width*) [inline], [static]

Sets the Asynchronous Data Bus Width.

Parameters

base	is the base address of the EMIF instance used.
offset	is the offset of asynchronous chip select of EMIF instance.
width	is the data bus width of the memory.

This function sets the data bus size for an external asynchronous memory to be interfaced. Valid values for param *offset* can be *EMIF_ASYNC_CS2_OFFSET*, *EMIF_ASYNC_CS3_OFFSET* & *EMIF_ASYNC_C43_OFFSET* for EMIF1 and *EMIF_ASYNC_CS2_OFFSET* for EMIF2. Valid values of param *width* can be *EMIF_ASYNC_DATA_WIDTH_8*, *EMIF_ASYNC_DATA_WIDTH_16* or *EMIF_ASYNC_DATA_WIDTH_32*.

Returns

None.

References EMIF_ASYNC_CS2_OFFSET.

15.2.4.13 static void EMIF_enableAsyncInterrupt (uint32_t *base,* uint16_t *intFlags*) [inline], [static]

Enables the Asynchronous Memory Interrupts.

Parameters

base	is the base address of the EMIF instance used.
intFlags	is the mask for desired interrupts.

This function enables the desired interrupts for an external asynchronous memory interface. Valid values for param *intFlags* can be **EMIF_ASYNC_INT_AT**, **EMIF_ASYNC_INT_LT**, **EMIF_ASYNC_INT_WR** or their combination.

Returns
None.

15.2.4.14 static void EMIF_disableAsyncInterrupt (uint32_t *base,* uint16_t *intFlags*) [inline], [static]

Disables the Asynchronous Memory Interrupts.

Parameters

base	is the base address of the EMIF instance used.
intFlags	is the mask for interrupts to be disabled.

This function disables the desired interrupts for an external asynchronous memory interface. Valid values for param *intFlags* can be **EMIF_ASYNC_INT_AT**, **EMIF_ASYNC_INT_LT**, **EMIF_ASYNC_INT_WR** or their combination.

Returns
None.

15.2.4.15 static uint16_t EMIF_getAsyncInterruptStatus (uint32_t *base*) [inline], [static]

Gets the interrupt status.

Parameters

base	is the base address of the EMIF instance used.

This function gets the interrupt status for an EMIF instance.

Returns
Returns the current interrupt status.

15.2.4.16 static void EMIF_clearAsyncInterruptStatus (uint32_t *base,* uint16_t *intFlags*) [inline], [static]

Clears the interrupt status for an EMIF instance.

Parameters

base	is the base address of the EMIF instance used.
intFlags	is the mask for the interrupt status to be cleared.

This function clears the interrupt status for an EMIF instance. The *intFlags* parameter can be any of **EMIF_INT_MSK_SET_AT_MASK_SET**, **EMIF_INT_MSK_SET_LT_MASK_SET**, or **EMIF_INT_MSK_SET_WR_MASK_SET_M** values or their combination.

Returns

None.

15.2.4.17 static void EMIF_setSyncTimingParams (uint32_t *base*, const **EMIF_SyncTimingParams** ∗ *tParam*) [inline], [static]

Sets the Synchronous Memory Timing Parameters.

Parameters

base	is the base address of an EMIF instance.
tParam	is parameters from memory datasheet in *ns*.

This function sets the timing characteristics for an external synchronous memory to be interfaced.

Returns

None.

References EMIF_SyncTimingParams::tRas, EMIF_SyncTimingParams::tRc, EMIF_SyncTimingParams::tRcd, EMIF_SyncTimingParams::tRfc, EMIF_SyncTimingParams::tRp, EMIF_SyncTimingParams::tRrd, and EMIF_SyncTimingParams::tWr.

15.2.4.18 static void EMIF_setSyncSelfRefreshExitTmng (uint32_t *base*, uint16_t *tXs*) [inline], [static]

Sets the SDRAM Self Refresh Exit Timing.

Parameters

base	is the base address of an EMIF instance.
tXs	is the desired timing value.

This function sets the self refresh exit timing for an external synchronous memory to be interfaced. tXs values must lie between 0x0U-0x1FU or 0-31.

Returns

None.

15.2.4.19 static void EMIF_setSyncRefreshRate (uint32_t *base*, uint16_t *refRate*) [inline], [static]

Sets the SDR Refresh Rate.

Parameters

base	is the base address of an EMIF instance.
refRate	is the refresh rate.

This function sets the refresh rate for an external synchronous memory to be interfaced. Valid values for refRate lies b/w 0x0U-0x1FFFU or 0-8191.

Returns

None.

15.2.4.20 static void EMIF_setSyncMemoryConfig (uint32_t *base*, const **EMIF_SyncConfig** ∗ *config*) [inline], [static]

Sets the Synchronous Memory configuration parameters.

Parameters

base	is the base address of the EMIF instance used.
config	is the desired configuration parameters.

This function sets configuration parameters like CL, NM, IBANK and PAGESIZE for an external synchronous memory to be interfaced.

Returns

None.

References EMIF_SyncConfig::casLatency, EMIF_SyncConfig::iBank, EMIF_SyncConfig::narrowMode, and EMIF_SyncConfig::pageSize.

15.2.4.21 static void EMIF_enableSyncSelfRefresh (uint32_t *base*) [inline], [static]

Enables Self Refresh.

Parameters

base	is the base address of the EMIF instance used.

This function enables Self Refresh Mode for EMIF.

Returns

None.

15.2.4.22 static void EMIF_disableSyncSelfRefresh (uint32_t *base*) [inline], [static]

Disables Self Refresh.

Parameters

base	is the base address of the EMIF instance used.

This function disables Self Refresh Mode for EMIF.

Returns
None.

15.2.4.23 static void EMIF_enableSyncPowerDown (uint32_t *base*) [inline], [static]

Enables Power Down.

Parameters

base	is the base address of the EMIF instance used.

This function Enables Power Down Mode for synchronous memory to be interfaced.

Returns
None.

15.2.4.24 static void EMIF_disableSyncPowerDown (uint32_t *base*) [inline], [static]

Disables Power Down.

Parameters

base	is the base address of the EMIF instance used.

This function disables Power Down Mode for synchronous memory to be interfaced.

Returns
None.

15.2.4.25 static void EMIF_enableSyncRefreshInPowerDown (uint32_t *base*) [inline], [static]

Enables Refresh in Power Down.

Parameters

base	is the base address of the EMIF instance used.

This function enables Refresh in Power Down Mode for synchronous memory to be interfaced.

Returns
None.

15.2.4.26 static void EMIF_disableSyncRefreshInPowerDown (uint32_t *base*) [inline], [static]

Disables Refresh in Power Down.

Parameters

base	is the base address of the EMIF instance used.

This function disables Refresh in Power Down Mode for synchronous memory to be interfaced.

Returns

None.

15.2.4.27 static uint32_t EMIF_getSyncTotalAccesses (uint32_t *base*) [inline], [static]

Gets total number of SDRAM accesses.

Parameters

base	is the base address of the EMIF instance used.

This function returns total number of SDRAM accesses from a master(CPUx/CPUx.DMA).

Returns

Returns total number of accesses to SDRAM.

15.2.4.28 static uint32_t EMIF_getSyncTotalActivateAccesses (uint32_t *base*) [inline], [static]

Gets total number of SDRAM accesses which require activate command.

Parameters

base	is the base address of the EMIF instance used.

This function returns total number of accesses to SDRAM which require activate command.

Returns

Returns total number of accesses to SDRAM which require activate.

16 EPWM Module

16.1 EPWM Introduction

The ePWM (enhanced Pulse width Modulator) API provides a set of functions for configuring and using the ePWM module. The provided functions provide the capability to generate and alter PWM wave forms by providing access to the following ePWM sub-modules.

- Time Base
- Counter Compare
- Action Qualifier
- Dead Band Generator
- Trip Zone
- Event Trigger
- Digital Compare

16.2 API Functions

Macros

- #define EPWM_TIME_BASE_STATUS_COUNT_UP
- #define EPWM_TIME_BASE_STATUS_COUNT_DOWN
- #define EPWM_DB_INPUT_EPWMA
- #define EPWM_DB_INPUT_EPWMB
- #define EPWM_DB_INPUT_DB_RED
- #define EPWM_TZ_SIGNAL_CBC1
- #define EPWM_TZ_SIGNAL_CBC2
- #define EPWM_TZ_SIGNAL_CBC3
- #define EPWM_TZ_SIGNAL_CBC4
- #define EPWM_TZ_SIGNAL_CBC5
- #define EPWM_TZ_SIGNAL_CBC6
- #define EPWM_TZ_SIGNAL_DCAEVT2
- #define EPWM_TZ_SIGNAL_DCBEVT2
- #define EPWM_TZ_SIGNAL_OSHT1
- #define EPWM_TZ_SIGNAL_OSHT2
- #define EPWM_TZ_SIGNAL_OSHT3
- #define EPWM_TZ_SIGNAL_OSHT4
- #define EPWM_TZ_SIGNAL_OSHT5
- #define EPWM_TZ_SIGNAL_OSHT6
- #define EPWM_TZ_SIGNAL_DCAEVT1
- #define EPWM_TZ_SIGNAL_DCBEVT1
- #define EPWM_TZ_INTERRUPT_CBC
- #define EPWM_TZ_INTERRUPT_OST
- #define EPWM_TZ_INTERRUPT_DCAEVT1

- #define EPWM_TZ_INTERRUPT_DCAEVT2
- #define EPWM_TZ_INTERRUPT_DCBEVT1
- #define EPWM_TZ_INTERRUPT_DCBEVT2
- #define EPWM_TZ_FLAG_CBC
- #define EPWM_TZ_FLAG_OST
- #define EPWM_TZ_FLAG_DCAEVT1
- #define EPWM_TZ_FLAG_DCAEVT2
- #define EPWM_TZ_FLAG_DCBEVT1
- #define EPWM_TZ_FLAG_DCBEVT2
- #define EPWM_TZ_INTERRUPT
- #define EPWM_TZ_CBC_FLAG_1
- #define EPWM_TZ_CBC_FLAG_2
- #define EPWM_TZ_CBC_FLAG_3
- #define EPWM_TZ_CBC_FLAG_4
- #define EPWM_TZ_CBC_FLAG_5
- #define EPWM_TZ_CBC_FLAG_6
- #define EPWM_TZ_CBC_FLAG_DCAEVT2
- #define EPWM_TZ_CBC_FLAG_DCBEVT2
- #define EPWM_TZ_OST_FLAG_OST1
- #define EPWM_TZ_OST_FLAG_OST2
- #define EPWM_TZ_OST_FLAG_OST3
- #define EPWM_TZ_OST_FLAG_OST4
- #define EPWM_TZ_OST_FLAG_OST5
- #define EPWM_TZ_OST_FLAG_OST6
- #define EPWM_TZ_OST_FLAG_DCAEVT1
- #define EPWM_TZ_OST_FLAG_DCBEVT1
- #define EPWM_TZ_FORCE_EVENT_CBC
- #define EPWM_TZ_FORCE_EVENT_OST
- #define EPWM_TZ_FORCE_EVENT_DCAEVT1
- #define EPWM_TZ_FORCE_EVENT_DCAEVT2
- #define EPWM_TZ_FORCE_EVENT_DCBEVT1
- #define EPWM_TZ_FORCE_EVENT_DCBEVT2
- #define EPWM_INT_TBCTR_ZERO
- #define EPWM_INT_TBCTR_PERIOD
- #define EPWM_INT_TBCTR_ZERO_OR_PERIOD
- #define EPWM_INT_TBCTR_U_CMPA
- #define EPWM_INT_TBCTR_U_CMPC
- #define EPWM_INT_TBCTR_D_CMPA
- #define EPWM_INT_TBCTR_D_CMPC
- #define EPWM_INT_TBCTR_U_CMPB
- #define EPWM_INT_TBCTR_U_CMPD
- #define EPWM_INT_TBCTR_D_CMPB
- #define EPWM_INT_TBCTR_D_CMPD
- #define EPWM_DC_COMBINATIONAL_TRIPIN1
- #define EPWM_DC_COMBINATIONAL_TRIPIN2
- #define EPWM_DC_COMBINATIONAL_TRIPIN3
- #define EPWM_DC_COMBINATIONAL_TRIPIN4
- #define EPWM_DC_COMBINATIONAL_TRIPIN5
- #define EPWM_DC_COMBINATIONAL_TRIPIN6
- #define EPWM_DC_COMBINATIONAL_TRIPIN7
- #define EPWM_DC_COMBINATIONAL_TRIPIN8
- #define EPWM_DC_COMBINATIONAL_TRIPIN9
- #define EPWM_DC_COMBINATIONAL_TRIPIN10
- #define EPWM_DC_COMBINATIONAL_TRIPIN11
- #define EPWM_DC_COMBINATIONAL_TRIPIN12
- #define EPWM_DC_COMBINATIONAL_TRIPIN14
- #define EPWM_DC_COMBINATIONAL_TRIPIN15
- #define EPWM_GL_REGISTER_TBPRD_TBPRDHR

- #define EPWM_GL_REGISTER_CMPA_CMPAHR
- #define EPWM_GL_REGISTER_CMPB_CMPBHR
- #define EPWM_GL_REGISTER_CMPC
- #define EPWM_GL_REGISTER_CMPD
- #define EPWM_GL_REGISTER_DBRED_DBREDHR
- #define EPWM_GL_REGISTER_DBFED_DBFEDHR
- #define EPWM_GL_REGISTER_DBCTL
- #define EPWM_GL_REGISTER_AQCTLA_AQCTLA2
- #define EPWM_GL_REGISTER_AQCTLB_AQCTLB2
- #define EPWM_GL_REGISTER_AQCSFRC

Enumerations

- enum EPWM_EmulationMode { EPWM_EMULATION_STOP_AFTER_NEXT_TB, EPWM_EMULATION_STOP_AFTER_FULL_CYCLE, EPWM_EMULATION_FREE_RUN }
- enum EPWM_SyncCountMode { EPWM_COUNT_MODE_DOWN_AFTER_SYNC, EPWM_COUNT_MODE_UP_AFTER_SYNC }
- enum EPWM_ClockDivider { EPWM_CLOCK_DIVIDER_1, EPWM_CLOCK_DIVIDER_2, EPWM_CLOCK_DIVIDER_4, EPWM_CLOCK_DIVIDER_8, EPWM_CLOCK_DIVIDER_16, EPWM_CLOCK_DIVIDER_32, EPWM_CLOCK_DIVIDER_64, EPWM_CLOCK_DIVIDER_128 }
- enum EPWM_HSClockDivider { EPWM_HSCLOCK_DIVIDER_1, EPWM_HSCLOCK_DIVIDER_2, EPWM_HSCLOCK_DIVIDER_4, EPWM_HSCLOCK_DIVIDER_6, EPWM_HSCLOCK_DIVIDER_8, EPWM_HSCLOCK_DIVIDER_10, EPWM_HSCLOCK_DIVIDER_12, EPWM_HSCLOCK_DIVIDER_14 }
- enum EPWM_SyncOutPulseMode { EPWM_SYNC_OUT_PULSE_ON_SOFTWARE, EPWM_SYNC_OUT_PULSE_ON_EPWMxSYNCIN, EPWM_SYNC_OUT_PULSE_ON_COUNTER_ZERO, EPWM_SYNC_OUT_PULSE_ON_COUNTER_COMPARE_B, EPWM_SYNC_OUT_PULSE_DISABLED, EPWM_SYNC_OUT_PULSE_ON_COUNTER_COMPARE_C, EPWM_SYNC_OUT_PULSE_ON_COUNTER_COMPARE_D }
- enum EPWM_PeriodLoadMode { EPWM_PERIOD_SHADOW_LOAD, EPWM_PERIOD_DIRECT_LOAD }
- enum EPWM_TimeBaseCountMode { EPWM_COUNTER_MODE_UP, EPWM_COUNTER_MODE_DOWN, EPWM_COUNTER_MODE_UP_DOWN, EPWM_COUNTER_MODE_STOP_FREEZE }
- enum EPWM_PeriodShadowLoadMode { EPWM_SHADOW_LOAD_MODE_COUNTER_ZERO, EPWM_SHADOW_LOAD_MODE_COUNTER_SYNC, EPWM_SHADOW_LOAD_MODE_SYNC }
- enum EPWM_CurrentLink { EPWM_LINK_WITH_EPWM_1, EPWM_LINK_WITH_EPWM_2, EPWM_LINK_WITH_EPWM_3, EPWM_LINK_WITH_EPWM_4, EPWM_LINK_WITH_EPWM_5, EPWM_LINK_WITH_EPWM_6, EPWM_LINK_WITH_EPWM_7, EPWM_LINK_WITH_EPWM_8, EPWM_LINK_WITH_EPWM_9, EPWM_LINK_WITH_EPWM_10, EPWM_LINK_WITH_EPWM_11, EPWM_LINK_WITH_EPWM_12 }

- enum EPWM_LinkComponent {
  EPWM_LINK_TBPRD, EPWM_LINK_COMP_A, EPWM_LINK_COMP_B,
  EPWM_LINK_COMP_C,
  EPWM_LINK_COMP_D, EPWM_LINK_GLDCTL2 }
- enum EPWM_CounterCompareModule { EPWM_COUNTER_COMPARE_A,
  EPWM_COUNTER_COMPARE_B, EPWM_COUNTER_COMPARE_C,
  EPWM_COUNTER_COMPARE_D }
- enum EPWM_CounterCompareLoadMode {
  EPWM_COMP_LOAD_ON_CNTR_ZERO, EPWM_COMP_LOAD_ON_CNTR_PERIOD,
  EPWM_COMP_LOAD_ON_CNTR_ZERO_PERIOD, EPWM_COMP_LOAD_FREEZE,
  EPWM_COMP_LOAD_ON_SYNC_CNTR_ZERO,
  EPWM_COMP_LOAD_ON_SYNC_CNTR_PERIOD,
  EPWM_COMP_LOAD_ON_SYNC_CNTR_ZERO_PERIOD,
  EPWM_COMP_LOAD_ON_SYNC_ONLY }
- enum EPWM_ActionQualifierModule { EPWM_ACTION_QUALIFIER_A,
  EPWM_ACTION_QUALIFIER_B }
- enum EPWM_ActionQualifierLoadMode {
  EPWM_AQ_LOAD_ON_CNTR_ZERO, EPWM_AQ_LOAD_ON_CNTR_PERIOD,
  EPWM_AQ_LOAD_ON_CNTR_ZERO_PERIOD, EPWM_AQ_LOAD_FREEZE,
  EPWM_AQ_LOAD_ON_SYNC_CNTR_ZERO,
  EPWM_AQ_LOAD_ON_SYNC_CNTR_PERIOD,
  EPWM_AQ_LOAD_ON_SYNC_CNTR_ZERO_PERIOD,
  EPWM_AQ_LOAD_ON_SYNC_ONLY }
- enum EPWM_ActionQualifierTriggerSource {
  EPWM_AQ_TRIGGER_EVENT_TRIG_DCA_1,
  EPWM_AQ_TRIGGER_EVENT_TRIG_DCA_2,
  EPWM_AQ_TRIGGER_EVENT_TRIG_DCB_1,
  EPWM_AQ_TRIGGER_EVENT_TRIG_DCB_2,
  EPWM_AQ_TRIGGER_EVENT_TRIG_TZ_1, EPWM_AQ_TRIGGER_EVENT_TRIG_TZ_2,
  EPWM_AQ_TRIGGER_EVENT_TRIG_TZ_3,
  EPWM_AQ_TRIGGER_EVENT_TRIG_EPWM_SYNCIN }
- enum EPWM_ActionQualifierOutputEvent {
  EPWM_AQ_OUTPUT_ON_TIMEBASE_ZERO,
  EPWM_AQ_OUTPUT_ON_TIMEBASE_PERIOD,
  EPWM_AQ_OUTPUT_ON_TIMEBASE_UP_CMPA,
  EPWM_AQ_OUTPUT_ON_TIMEBASE_DOWN_CMPA,
  EPWM_AQ_OUTPUT_ON_TIMEBASE_UP_CMPB,
  EPWM_AQ_OUTPUT_ON_TIMEBASE_DOWN_CMPB,
  EPWM_AQ_OUTPUT_ON_T1_COUNT_UP,
  EPWM_AQ_OUTPUT_ON_T1_COUNT_DOWN,
  EPWM_AQ_OUTPUT_ON_T2_COUNT_UP,
  EPWM_AQ_OUTPUT_ON_T2_COUNT_DOWN }
- enum EPWM_ActionQualifierOutput { EPWM_AQ_OUTPUT_NO_CHANGE,
  EPWM_AQ_OUTPUT_LOW, EPWM_AQ_OUTPUT_HIGH, EPWM_AQ_OUTPUT_TOGGLE
  }
- enum EPWM_ActionQualifierSWOutput { EPWM_AQ_SW_DISABLED,
  EPWM_AQ_SW_OUTPUT_LOW, EPWM_AQ_SW_OUTPUT_HIGH }
- enum EPWM_ActionQualifierEventAction {
  EPWM_AQ_OUTPUT_NO_CHANGE_ZERO, EPWM_AQ_OUTPUT_LOW_ZERO,
  EPWM_AQ_OUTPUT_HIGH_ZERO, EPWM_AQ_OUTPUT_TOGGLE_ZERO,
  EPWM_AQ_OUTPUT_NO_CHANGE_PERIOD, EPWM_AQ_OUTPUT_LOW_PERIOD,
  EPWM_AQ_OUTPUT_HIGH_PERIOD, EPWM_AQ_OUTPUT_TOGGLE_PERIOD,
  EPWM_AQ_OUTPUT_NO_CHANGE_UP_CMPA, EPWM_AQ_OUTPUT_LOW_UP_CMPA,

EPWM_AQ_OUTPUT_HIGH_UP_CMPA, EPWM_AQ_OUTPUT_TOGGLE_UP_CMPA, EPWM_AQ_OUTPUT_NO_CHANGE_DOWN_CMPA, EPWM_AQ_OUTPUT_LOW_DOWN_CMPA, EPWM_AQ_OUTPUT_HIGH_DOWN_CMPA, EPWM_AQ_OUTPUT_TOGGLE_DOWN_CMPA, EPWM_AQ_OUTPUT_NO_CHANGE_UP_CMPB, EPWM_AQ_OUTPUT_LOW_UP_CMPB, EPWM_AQ_OUTPUT_HIGH_UP_CMPB, EPWM_AQ_OUTPUT_TOGGLE_UP_CMPB, EPWM_AQ_OUTPUT_NO_CHANGE_DOWN_CMPB, EPWM_AQ_OUTPUT_LOW_DOWN_CMPB, EPWM_AQ_OUTPUT_HIGH_DOWN_CMPB, EPWM_AQ_OUTPUT_TOGGLE_DOWN_CMPB }
- enum EPWM_AdditionalActionQualifierEventAction { EPWM_AQ_OUTPUT_NO_CHANGE_UP_T1, EPWM_AQ_OUTPUT_LOW_UP_T1, EPWM_AQ_OUTPUT_HIGH_UP_T1, EPWM_AQ_OUTPUT_TOGGLE_UP_T1, EPWM_AQ_OUTPUT_NO_CHANGE_DOWN_T1, EPWM_AQ_OUTPUT_LOW_DOWN_T1, EPWM_AQ_OUTPUT_HIGH_DOWN_T1, EPWM_AQ_OUTPUT_TOGGLE_DOWN_T1, EPWM_AQ_OUTPUT_NO_CHANGE_UP_T2, EPWM_AQ_OUTPUT_LOW_UP_T2, EPWM_AQ_OUTPUT_HIGH_UP_T2, EPWM_AQ_OUTPUT_TOGGLE_UP_T2, EPWM_AQ_OUTPUT_NO_CHANGE_DOWN_T2, EPWM_AQ_OUTPUT_LOW_DOWN_T2, EPWM_AQ_OUTPUT_HIGH_DOWN_T2, EPWM_AQ_OUTPUT_TOGGLE_DOWN_T2 }
- enum EPWM_ActionQualifierOutputModule { EPWM_AQ_OUTPUT_A, EPWM_AQ_OUTPUT_B }
- enum EPWM_ActionQualifierContForce { EPWM_AQ_SW_SH_LOAD_ON_CNTR_ZERO, EPWM_AQ_SW_SH_LOAD_ON_CNTR_PERIOD, EPWM_AQ_SW_SH_LOAD_ON_CNTR_ZERO_PERIOD, EPWM_AQ_SW_IMMEDIATE_LOAD }
- enum EPWM_DeadBandOutput { EPWM_DB_OUTPUT_A, EPWM_DB_OUTPUT_B }
- enum EPWM_DeadBandDelayMode { EPWM_DB_RED, EPWM_DB_FED }
- enum EPWM_DeadBandPolarity { EPWM_DB_POLARITY_ACTIVE_HIGH, EPWM_DB_POLARITY_ACTIVE_LOW }
- enum EPWM_DeadBandControlLoadMode { EPWM_DB_LOAD_ON_CNTR_ZERO, EPWM_DB_LOAD_ON_CNTR_PERIOD, EPWM_DB_LOAD_ON_CNTR_ZERO_PERIOD, EPWM_DB_LOAD_FREEZE }
- enum EPWM_RisingEdgeDelayLoadMode { EPWM_RED_LOAD_ON_CNTR_ZERO, EPWM_RED_LOAD_ON_CNTR_PERIOD, EPWM_RED_LOAD_ON_CNTR_ZERO_PERIOD, EPWM_RED_LOAD_FREEZE }
- enum EPWM_FallingEdgeDelayLoadMode { EPWM_FED_LOAD_ON_CNTR_ZERO, EPWM_FED_LOAD_ON_CNTR_PERIOD, EPWM_FED_LOAD_ON_CNTR_ZERO_PERIOD, EPWM_FED_LOAD_FREEZE }
- enum EPWM_DeadBandClockMode { EPWM_DB_COUNTER_CLOCK_FULL_CYCLE, EPWM_DB_COUNTER_CLOCK_HALF_CYCLE }
- enum EPWM_TripZoneDigitalCompareOutput { EPWM_TZ_DC_OUTPUT_A1, EPWM_TZ_DC_OUTPUT_A2, EPWM_TZ_DC_OUTPUT_B1, EPWM_TZ_DC_OUTPUT_B2 }
- enum EPWM_TripZoneDigitalCompareOutputEvent { EPWM_TZ_EVENT_DC_DISABLED, EPWM_TZ_EVENT_DCXH_LOW, EPWM_TZ_EVENT_DCXH_HIGH, EPWM_TZ_EVENT_DCXL_LOW, EPWM_TZ_EVENT_DCXL_HIGH, EPWM_TZ_EVENT_DCXL_HIGH_DCXH_LOW }
- enum EPWM_TripZoneEvent { EPWM_TZ_ACTION_EVENT_TZA, EPWM_TZ_ACTION_EVENT_TZB, EPWM_TZ_ACTION_EVENT_DCAEVT1, EPWM_TZ_ACTION_EVENT_DCAEVT2, EPWM_TZ_ACTION_EVENT_DCBEVT1, EPWM_TZ_ACTION_EVENT_DCBEVT2 }
- enum EPWM_TripZoneAction { EPWM_TZ_ACTION_HIGH_Z, EPWM_TZ_ACTION_HIGH, EPWM_TZ_ACTION_LOW, EPWM_TZ_ACTION_DISABLE }
- enum EPWM_TripZoneAdvancedEvent { EPWM_TZ_ADV_ACTION_EVENT_TZB_D, EPWM_TZ_ADV_ACTION_EVENT_TZB_U, EPWM_TZ_ADV_ACTION_EVENT_TZA_D, EPWM_TZ_ADV_ACTION_EVENT_TZA_U }

- enum EPWM_TripZoneAdvancedAction { EPWM_TZ_ADV_ACTION_HIGH_Z, EPWM_TZ_ADV_ACTION_HIGH, EPWM_TZ_ADV_ACTION_LOW, EPWM_TZ_ADV_ACTION_TOGGLE, EPWM_TZ_ADV_ACTION_DISABLE }
- enum EPWM_TripZoneAdvDigitalCompareEvent { EPWM_TZ_ADV_ACTION_EVENT_DCxEVT1_U, EPWM_TZ_ADV_ACTION_EVENT_DCxEVT1_D, EPWM_TZ_ADV_ACTION_EVENT_DCxEVT2_U, EPWM_TZ_ADV_ACTION_EVENT_DCxEVT2_D }
- enum EPWM_CycleByCycleTripZoneClearMode { EPWM_TZ_CBC_PULSE_CLR_CNTR_ZERO, EPWM_TZ_CBC_PULSE_CLR_CNTR_PERIOD, EPWM_TZ_CBC_PULSE_CLR_CNTR_ZERO_PERIOD }
- enum EPWM_ADCStartOfConversionType { EPWM_SOC_A, EPWM_SOC_B }
- enum EPWM_ADCStartOfConversionSource { EPWM_SOC_DCxEVT1, EPWM_SOC_TBCTR_ZERO, EPWM_SOC_TBCTR_PERIOD, EPWM_SOC_TBCTR_ZERO_OR_PERIOD, EPWM_SOC_TBCTR_U_CMPA, EPWM_SOC_TBCTR_U_CMPC, EPWM_SOC_TBCTR_D_CMPA, EPWM_SOC_TBCTR_D_CMPC, EPWM_SOC_TBCTR_U_CMPB, EPWM_SOC_TBCTR_U_CMPD, EPWM_SOC_TBCTR_D_CMPB, EPWM_SOC_TBCTR_D_CMPD }
- enum EPWM_DigitalCompareType { EPWM_DC_TYPE_DCAH, EPWM_DC_TYPE_DCAL, EPWM_DC_TYPE_DCBH, EPWM_DC_TYPE_DCBL }
- enum EPWM_DigitalCompareTripInput { EPWM_DC_TRIP_TRIPIN1, EPWM_DC_TRIP_TRIPIN2, EPWM_DC_TRIP_TRIPIN3, EPWM_DC_TRIP_TRIPIN4, EPWM_DC_TRIP_TRIPIN5, EPWM_DC_TRIP_TRIPIN6, EPWM_DC_TRIP_TRIPIN7, EPWM_DC_TRIP_TRIPIN8, EPWM_DC_TRIP_TRIPIN9, EPWM_DC_TRIP_TRIPIN10, EPWM_DC_TRIP_TRIPIN11, EPWM_DC_TRIP_TRIPIN12, EPWM_DC_TRIP_TRIPIN14, EPWM_DC_TRIP_TRIPIN15, EPWM_DC_TRIP_COMBINATION }
- enum EPWM_DigitalCompareBlankingPulse { EPWM_DC_WINDOW_START_TBCTR_PERIOD, EPWM_DC_WINDOW_START_TBCTR_ZERO, EPWM_DC_WINDOW_START_TBCTR_ZERO_PERIOD }
- enum EPWM_DigitalCompareFilterInput { EPWM_DC_WINDOW_SOURCE_DCAEVT1, EPWM_DC_WINDOW_SOURCE_DCAEVT2, EPWM_DC_WINDOW_SOURCE_DCBEVT1, EPWM_DC_WINDOW_SOURCE_DCBEVT2 }
- enum EPWM_DigitalCompareModule { EPWM_DC_MODULE_A, EPWM_DC_MODULE_B }
- enum EPWM_DigitalCompareEvent { EPWM_DC_EVENT_1, EPWM_DC_EVENT_2 }
- enum EPWM_DigitalCompareEventSource { EPWM_DC_EVENT_SOURCE_ORIG_SIGNAL, EPWM_DC_EVENT_SOURCE_FILT_SIGNAL }
- enum EPWM_DigitalCompareSyncMode { EPWM_DC_EVENT_INPUT_SYNCED, EPWM_DC_EVENT_INPUT_NOT_SYNCED }
- enum EPWM_GlobalLoadTrigger { EPWM_GL_LOAD_PULSE_CNTR_ZERO, EPWM_GL_LOAD_PULSE_CNTR_PERIOD, EPWM_GL_LOAD_PULSE_CNTR_ZERO_PERIOD, EPWM_GL_LOAD_PULSE_SYNC, EPWM_GL_LOAD_PULSE_SYNC_OR_CNTR_ZERO, EPWM_GL_LOAD_PULSE_SYNC_OR_CNTR_PERIOD, EPWM_GL_LOAD_PULSE_SYNC_CNTR_ZERO_PERIOD, EPWM_GL_LOAD_PULSE_GLOBAL_FORCE }

- enum EPWM_ValleyTriggerSource {
  EPWM_VALLEY_TRIGGER_EVENT_SOFTWARE,
  EPWM_VALLEY_TRIGGER_EVENT_CNTR_ZERO,
  EPWM_VALLEY_TRIGGER_EVENT_CNTR_PERIOD,
  EPWM_VALLEY_TRIGGER_EVENT_CNTR_ZERO_PERIOD,
  EPWM_VALLEY_TRIGGER_EVENT_DCAEVT1,
  EPWM_VALLEY_TRIGGER_EVENT_DCAEVT2,
  EPWM_VALLEY_TRIGGER_EVENT_DCBEVT1,
  EPWM_VALLEY_TRIGGER_EVENT_DCBEVT2 }
- enum EPWM_ValleyCounterEdge { EPWM_VALLEY_COUNT_START_EDGE,
  EPWM_VALLEY_COUNT_STOP_EDGE }
- enum EPWM_ValleyDelayMode {
  EPWM_VALLEY_DELAY_MODE_SW_DELAY,
  EPWM_VALLEY_DELAY_MODE_VCNT_DELAY_SW_DELAY,
  EPWM_VALLEY_DELAY_MODE_VCNT_DELAY_SHIFT_1_SW_DELAY,
  EPWM_VALLEY_DELAY_MODE_VCNT_DELAY_SHIFT_2_SW_DELAY,
  EPWM_VALLEY_DELAY_MODE_VCNT_DELAY_SHIFT_4_SW_DELAY }
- enum EPWM_DigitalCompareEdgeFilterMode { EPWM_DC_EDGEFILT_MODE_RISING,
  EPWM_DC_EDGEFILT_MODE_FALLING, EPWM_DC_EDGEFILT_MODE_BOTH }
- enum EPWM_DigitalCompareEdgeFilterEdgeCount {
  EPWM_DC_EDGEFILT_EDGECNT_0, EPWM_DC_EDGEFILT_EDGECNT_1,
  EPWM_DC_EDGEFILT_EDGECNT_2, EPWM_DC_EDGEFILT_EDGECNT_3,
  EPWM_DC_EDGEFILT_EDGECNT_4, EPWM_DC_EDGEFILT_EDGECNT_5,
  EPWM_DC_EDGEFILT_EDGECNT_6, EPWM_DC_EDGEFILT_EDGECNT_7 }
- enum EPWM_LockRegisterGroup { EPWM_REGISTER_GROUP_GLOBAL_LOAD,
  EPWM_REGISTER_GROUP_TRIP_ZONE,
  EPWM_REGISTER_GROUP_TRIP_ZONE_CLEAR,
  EPWM_REGISTER_GROUP_DIGITAL_COMPARE }

Functions

- static void EPWM_setTimeBaseCounter (uint32_t base, uint16_t count)
- static void EPWM_setCountModeAfterSync (uint32_t base, EPWM_SyncCountMode mode)
- static void EPWM_setClockPrescaler (uint32_t base, EPWM_ClockDivider prescaler, EPWM_HSClockDivider highSpeedPrescaler)
- static void EPWM_forceSyncPulse (uint32_t base)
- static void EPWM_setSyncOutPulseMode (uint32_t base, EPWM_SyncOutPulseMode mode)
- static void EPWM_setPeriodLoadMode (uint32_t base, EPWM_PeriodLoadMode loadMode)
- static void EPWM_enablePhaseShiftLoad (uint32_t base)
- static void EPWM_disablePhaseShiftLoad (uint32_t base)
- static void EPWM_setTimeBaseCounterMode (uint32_t base, EPWM_TimeBaseCountMode counterMode)
- static void EPWM_selectPeriodLoadEvent (uint32_t base, EPWM_PeriodShadowLoadMode shadowLoadMode)
- static void EPWM_enableOneShotSync (uint32_t base)
- static void EPWM_disableOneShotSync (uint32_t base)
- static void EPWM_startOneShotSync (uint32_t base)
- static uint16_t EPWM_getTimeBaseCounterValue (uint32_t base)
- static bool EPWM_getTimeBaseCounterOverflowStatus (uint32_t base)
- static void EPWM_clearTimeBaseCounterOverflowEvent (uint32_t base)
- static bool EPWM_getSyncStatus (uint32_t base)
- static void EPWM_clearSyncEvent (uint32_t base)
- static uint16_t EPWM_getTimeBaseCounterDirection (uint32_t base)

- static void EPWM_setPhaseShift (uint32_t base, uint16_t phaseCount)
- static void EPWM_setTimeBasePeriod (uint32_t base, uint16_t periodCount)
- static uint16_t EPWM_getTimeBasePeriod (uint32_t base)
- static void EPWM_setupEPWMLinks (uint32_t base, EPWM_CurrentLink epwmLink, EPWM_LinkComponent linkComp)
- static void EPWM_setCounterCompareShadowLoadMode (uint32_t base, EPWM_CounterCompareModule compModule, EPWM_CounterCompareLoadMode loadMode)
- static void EPWM_disableCounterCompareShadowLoadMode (uint32_t base, EPWM_CounterCompareModule compModule)
- static void EPWM_setCounterCompareValue (uint32_t base, EPWM_CounterCompareModule compModule, uint16_t compCount)
- static uint16_t EPWM_getCounterCompareValue (uint32_t base, EPWM_CounterCompareModule compModule)
- static bool EPWM_getCounterCompareShadowStatus (uint32_t base, EPWM_CounterCompareModule compModule)
- static void EPWM_setActionQualifierShadowLoadMode (uint32_t base, EPWM_ActionQualifierModule aqModule, EPWM_ActionQualifierLoadMode loadMode)
- static void EPWM_disableActionQualifierShadowLoadMode (uint32_t base, EPWM_ActionQualifierModule aqModule)
- static void EPWM_setActionQualifierT1TriggerSource (uint32_t base, EPWM_ActionQualifierTriggerSource trigger)
- static void EPWM_setActionQualifierT2TriggerSource (uint32_t base, EPWM_ActionQualifierTriggerSource trigger)
- static void EPWM_setActionQualifierAction (uint32_t base, EPWM_ActionQualifierOutputModule epwmOutput, EPWM_ActionQualifierOutput output, EPWM_ActionQualifierOutputEvent event)
- static void EPWM_setActionQualifierActionComplete (uint32_t base, EPWM_ActionQualifierOutputModule epwmOutput, EPWM_ActionQualifierEventAction action)
- static void EPWM_setAdditionalActionQualifierActionComplete (uint32_t base, EPWM_ActionQualifierOutputModule epwmOutput, EPWM_AdditionalActionQualifierEventAction action)
- static void EPWM_setActionQualifierContSWForceShadowMode (uint32_t base, EPWM_ActionQualifierContForce mode)
- static void EPWM_setActionQualifierContSWForceAction (uint32_t base, EPWM_ActionQualifierOutputModule epwmOutput, EPWM_ActionQualifierSWOutput output)
- static void EPWM_setActionQualifierSWAction (uint32_t base, EPWM_ActionQualifierOutputModule epwmOutput, EPWM_ActionQualifierOutput output)
- static void EPWM_forceActionQualifierSWAction (uint32_t base, EPWM_ActionQualifierOutputModule epwmOutput)
- static void EPWM_setDeadBandOutputSwapMode (uint32_t base, EPWM_DeadBandOutput output, bool enableSwapMode)
- static void EPWM_setDeadBandDelayMode (uint32_t base, EPWM_DeadBandDelayMode delayMode, bool enableDelayMode)
- static void EPWM_setDeadBandDelayPolarity (uint32_t base, EPWM_DeadBandDelayMode delayMode, EPWM_DeadBandPolarity polarity)
- static void EPWM_setRisingEdgeDeadBandDelayInput (uint32_t base, uint16_t input)
- static void EPWM_setFallingEdgeDeadBandDelayInput (uint32_t base, uint16_t input)
- static void EPWM_setDeadBandControlShadowLoadMode (uint32_t base, EPWM_DeadBandControlLoadMode loadMode)
- static void EPWM_disableDeadBandControlShadowLoadMode (uint32_t base)
- static void EPWM_setRisingEdgeDelayCountShadowLoadMode (uint32_t base, EPWM_RisingEdgeDelayLoadMode loadMode)
- static void EPWM_disableRisingEdgeDelayCountShadowLoadMode (uint32_t base)

- static void EPWM_setFallingEdgeDelayCountShadowLoadMode (uint32_t base, EPWM_FallingEdgeDelayLoadMode loadMode)
- static void EPWM_disableFallingEdgeDelayCountShadowLoadMode (uint32_t base)
- static void EPWM_setDeadBandCounterClock (uint32_t base, EPWM_DeadBandClockMode clockMode)
- static void EPWM_setRisingEdgeDelayCount (uint32_t base, uint16_t redCount)
- static void EPWM_setFallingEdgeDelayCount (uint32_t base, uint16_t fedCount)
- static void EPWM_enableChopper (uint32_t base)
- static void EPWM_disableChopper (uint32_t base)
- static void EPWM_setChopperDutyCycle (uint32_t base, uint16_t dutyCycleCount)
- static void EPWM_setChopperFreq (uint32_t base, uint16_t freqDiv)
- static void EPWM_setChopperFirstPulseWidth (uint32_t base, uint16_t firstPulseWidth)
- static void EPWM_enableTripZoneSignals (uint32_t base, uint16_t tzSignal)
- static void EPWM_disableTripZoneSignals (uint32_t base, uint16_t tzSignal)
- static void EPWM_setTripZoneDigitalCompareEventCondition (uint32_t base, EPWM_TripZoneDigitalCompareOutput dcType, EPWM_TripZoneDigitalCompareOutputEvent dcEvent)
- static void EPWM_enableTripZoneAdvAction (uint32_t base)
- static void EPWM_disableTripZoneAdvAction (uint32_t base)
- static void EPWM_setTripZoneAction (uint32_t base, EPWM_TripZoneEvent tzEvent, EPWM_TripZoneAction tzAction)
- static void EPWM_setTripZoneAdvAction (uint32_t base, EPWM_TripZoneAdvancedEvent tzAdvEvent, EPWM_TripZoneAdvancedAction tzAdvAction)
- static void EPWM_setTripZoneAdvDigitalCompareActionA (uint32_t base, EPWM_TripZoneAdvDigitalCompareEvent tzAdvDCEvent, EPWM_TripZoneAdvancedAction tzAdvDCAction)
- static void EPWM_setTripZoneAdvDigitalCompareActionB (uint32_t base, EPWM_TripZoneAdvDigitalCompareEvent tzAdvDCEvent, EPWM_TripZoneAdvancedAction tzAdvDCAction)
- static void EPWM_enableTripZoneInterrupt (uint32_t base, uint16_t tzInterrupt)
- static void EPWM_disableTripZoneInterrupt (uint32_t base, uint16_t tzInterrupt)
- static uint16_t EPWM_getTripZoneFlagStatus (uint32_t base)
- static uint16_t EPWM_getCycleByCycleTripZoneFlagStatus (uint32_t base)
- static uint16_t EPWM_getOneShotTripZoneFlagStatus (uint32_t base)
- static void EPWM_selectCycleByCycleTripZoneClearEvent (uint32_t base, EPWM_CycleByCycleTripZoneClearMode clearEvent)
- static void EPWM_clearTripZoneFlag (uint32_t base, uint16_t tzFlags)
- static void EPWM_clearCycleByCycleTripZoneFlag (uint32_t base, uint16_t tzCBCFlags)
- static void EPWM_clearOneShotTripZoneFlag (uint32_t base, uint16_t tzOSTFlags)
- static void EPWM_forceTripZoneEvent (uint32_t base, uint16_t tzForceEvent)
- static void EPWM_enableInterrupt (uint32_t base)
- static void EPWM_disableInterrupt (uint32_t base)
- static void EPWM_setInterruptSource (uint32_t base, uint16_t interruptSource)
- static void EPWM_setInterruptEventCount (uint32_t base, uint16_t eventCount)
- static bool EPWM_getEventTriggerInterruptStatus (uint32_t base)
- static void EPWM_clearEventTriggerInterruptFlag (uint32_t base)
- static void EPWM_enableInterruptEventCountInit (uint32_t base)
- static void EPWM_disableInterruptEventCountInit (uint32_t base)
- static void EPWM_forceInterruptEventCountInit (uint32_t base)
- static void EPWM_setInterruptEventCountInitValue (uint32_t base, uint16_t eventCount)
- static uint16_t EPWM_getInterruptEventCount (uint32_t base)
- static void EPWM_forceEventTriggerInterrupt (uint32_t base)
- static void EPWM_enableADCTrigger (uint32_t base, EPWM_ADCStartOfConversionType adcSOCType)
- static void EPWM_disableADCTrigger (uint32_t base, EPWM_ADCStartOfConversionType adcSOCType)

- static void EPWM_setADCTriggerSource (uint32_t base, EPWM_ADCStartOfConversionType adcSOCType, EPWM_ADCStartOfConversionSource socSource)
- static void EPWM_setADCTriggerEventPrescale (uint32_t base, EPWM_ADCStartOfConversionType adcSOCType, uint16_t preScaleCount)
- static bool EPWM_getADCTriggerFlagStatus (uint32_t base, EPWM_ADCStartOfConversionType adcSOCType)
- static void EPWM_clearADCTriggerFlag (uint32_t base, EPWM_ADCStartOfConversionType adcSOCType)
- static void EPWM_enableADCTriggerEventCountInit (uint32_t base, EPWM_ADCStartOfConversionType adcSOCType)
- static void EPWM_disableADCTriggerEventCountInit (uint32_t base, EPWM_ADCStartOfConversionType adcSOCType)
- static void EPWM_forceADCTriggerEventCountInit (uint32_t base, EPWM_ADCStartOfConversionType adcSOCType)
- static void EPWM_setADCTriggerEventCountInitValue (uint32_t base, EPWM_ADCStartOfConversionType adcSOCType, uint16_t eventCount)
- static uint16_t EPWM_getADCTriggerEventCount (uint32_t base, EPWM_ADCStartOfConversionType adcSOCType)
- static void EPWM_forceADCTrigger (uint32_t base, EPWM_ADCStartOfConversionType adcSOCType)
- static void EPWM_selectDigitalCompareTripInput (uint32_t base, EPWM_DigitalCompareTripInput tripSource, EPWM_DigitalCompareType dcType)
- static void EPWM_enableDigitalCompareBlankingWindow (uint32_t base)
- static void EPWM_disableDigitalCompareBlankingWindow (uint32_t base)
- static void EPWM_enableDigitalCompareWindowInverseMode (uint32_t base)
- static void EPWM_disableDigitalCompareWindowInverseMode (uint32_t base)
- static void EPWM_setDigitalCompareBlankingEvent (uint32_t base, EPWM_DigitalCompareBlankingPulse blankingPulse)
- static void EPWM_setDigitalCompareFilterInput (uint32_t base, EPWM_DigitalCompareFilterInput filterInput)
- static void EPWM_enableDigitalCompareEdgeFilter (uint32_t base)
- static void EPWM_disableDigitalCompareEdgeFilter (uint32_t base)
- static void EPWM_setDigitalCompareEdgeFilterMode (uint32_t base, EPWM_DigitalCompareEdgeFilterMode edgeMode)
- static void EPWM_setDigitalCompareEdgeFilterEdgeCount (uint32_t base, uint16_t edgeCount)
- static uint16_t EPWM_getDigitalCompareEdgeFilterEdgeCount (uint32_t base)
- static uint16_t EPWM_getDigitalCompareEdgeFilterEdgeStatus (uint32_t base)
- static void EPWM_setDigitalCompareWindowOffset (uint32_t base, uint16_t windowOffsetCount)
- static void EPWM_setDigitalCompareWindowLength (uint32_t base, uint16_t windowLengthCount)
- static uint16_t EPWM_getDigitalCompareBlankingWindowOffsetCount (uint32_t base)
- static uint16_t EPWM_getDigitalCompareBlankingWindowLengthCount (uint32_t base)
- static void EPWM_setDigitalCompareEventSource (uint32_t base, EPWM_DigitalCompareModule dcModule, EPWM_DigitalCompareEvent dcEvent, EPWM_DigitalCompareEventSource dcEventSource)
- static void EPWM_setDigitalCompareEventSyncMode (uint32_t base, EPWM_DigitalCompareModule dcModule, EPWM_DigitalCompareEvent dcEvent, EPWM_DigitalCompareSyncMode syncMode)
- static void EPWM_enableDigitalCompareADCTrigger (uint32_t base, EPWM_DigitalCompareModule dcModule)
- static void EPWM_disableDigitalCompareADCTrigger (uint32_t base, EPWM_DigitalCompareModule dcModule)

- static void EPWM_enableDigitalCompareSyncEvent (uint32_t base, EPWM_DigitalCompareModule dcModule)
- static void EPWM_disableDigitalCompareSyncEvent (uint32_t base, EPWM_DigitalCompareModule dcModule)
- static void EPWM_enableDigitalCompareCounterCapture (uint32_t base)
- static void EPWM_disableDigitalCompareCounterCapture (uint32_t base)
- static void EPWM_setDigitalCompareCounterShadowMode (uint32_t base, bool enableShadowMode)
- static bool EPWM_getDigitalCompareCaptureStatus (uint32_t base)
- static uint16_t EPWM_getDigitalCompareCaptureCount (uint32_t base)
- static void EPWM_enableDigitalCompareTripCombinationInput (uint32_t base, uint16_t tripInput, EPWM_DigitalCompareType dcType)
- static void EPWM_disableDigitalCompareTripCombinationInput (uint32_t base, uint16_t tripInput, EPWM_DigitalCompareType dcType)
- static void EPWM_enableValleyCapture (uint32_t base)
- static void EPWM_disableValleyCapture (uint32_t base)
- static void EPWM_startValleyCapture (uint32_t base)
- static void EPWM_setValleyTriggerSource (uint32_t base, EPWM_ValleyTriggerSource trigger)
- static void EPWM_setValleyTriggerEdgeCounts (uint32_t base, uint16_t startCount, uint16_t stopCount)
- static void EPWM_enableValleyHWDelay (uint32_t base)
- static void EPWM_disableValleyHWDelay (uint32_t base)
- static void EPWM_setValleySWDelayValue (uint32_t base, uint16_t delayOffsetValue)
- static void EPWM_setValleyDelayDivider (uint32_t base, EPWM_ValleyDelayMode delayMode)
- static bool EPWM_getValleyEdgeStatus (uint32_t base, EPWM_ValleyCounterEdge edge)
- static uint16_t EPWM_getValleyCount (uint32_t base)
- static uint16_t EPWM_getValleyHWDelay (uint32_t base)
- static void EPWM_enableGlobalLoad (uint32_t base)
- static void EPWM_disableGlobalLoad (uint32_t base)
- static void EPWM_setGlobalLoadTrigger (uint32_t base, EPWM_GlobalLoadTrigger loadTrigger)
- static void EPWM_setGlobalLoadEventPrescale (uint32_t base, uint16_t prescalePulseCount)
- static uint16_t EPWM_getGlobalLoadEventCount (uint32_t base)
- static void EPWM_disableGlobalLoadOneShotMode (uint32_t base)
- static void EPWM_enableGlobalLoadOneShotMode (uint32_t base)
- static void EPWM_setGlobalLoadOneShotLatch (uint32_t base)
- static void EPWM_forceGlobalLoadOneShotEvent (uint32_t base)
- static void EPWM_enableGlobalLoadRegisters (uint32_t base, uint16_t loadRegister)
- static void EPWM_disableGlobalLoadRegisters (uint32_t base, uint16_t loadRegister)
- void EPWM_setEmulationMode (uint32_t base, EPWM_EmulationMode emulationMode)

16.2.1 Detailed Description

The code for this module is contained in `driverlib/epwm.c`, with `driverlib/epwm.h` containing the API declarations for use by applications.

16.2.2 Macro Definition Documentation

16.2.2.1 #define EPWM_TIME_BASE_STATUS_COUNT_UP

Time base counter is counting up

16.2.2.2 #define EPWM_TIME_BASE_STATUS_COUNT_DOWN

Time base counter is counting down

16.2.2.3 #define EPWM_DB_INPUT_EPWMA

Input signal is ePWMA

Referenced by EPWM_setFallingEdgeDeadBandDelayInput(), and EPWM_setRisingEdgeDeadBandDelayInput().

16.2.2.4 #define EPWM_DB_INPUT_EPWMB

Input signal is ePWMB

Referenced by EPWM_setFallingEdgeDeadBandDelayInput(), and EPWM_setRisingEdgeDeadBandDelayInput().

16.2.2.5 #define EPWM_DB_INPUT_DB_RED

Input signal is the output of Rising Edge delay

Referenced by EPWM_setFallingEdgeDeadBandDelayInput().

16.2.2.6 #define EPWM_TZ_SIGNAL_CBC1

TZ1 Cycle By Cycle

16.2.2.7 #define EPWM_TZ_SIGNAL_CBC2

TZ2 Cycle By Cycle

16.2.2.8 #define EPWM_TZ_SIGNAL_CBC3

TZ3 Cycle By Cycle

16.2.2.9 #define EPWM_TZ_SIGNAL_CBC4

TZ4 Cycle By Cycle

16.2.2.10 #define EPWM_TZ_SIGNAL_CBC5

TZ5 Cycle By Cycle

16.2.2.11 #define EPWM_TZ_SIGNAL_CBC6

TZ6 Cycle By Cycle

16.2.2.12 #define EPWM_TZ_SIGNAL_DCAEVT2

DCAEVT2 Cycle By Cycle

16.2.2.13 #define EPWM_TZ_SIGNAL_DCBEVT2

DCBEVT2 Cycle By Cycle

16.2.2.14 #define EPWM_TZ_SIGNAL_OSHT1

One-shot TZ1

16.2.2.15 #define EPWM_TZ_SIGNAL_OSHT2

One-shot TZ2

16.2.2.16 #define EPWM_TZ_SIGNAL_OSHT3

One-shot TZ3

16.2.2.17 #define EPWM_TZ_SIGNAL_OSHT4

One-shot TZ4

16.2.2.18 #define EPWM_TZ_SIGNAL_OSHT5

One-shot TZ5

16.2.2.19 #define EPWM_TZ_SIGNAL_OSHT6

One-shot TZ6

16.2.2.20 #define EPWM_TZ_SIGNAL_DCAEVT1

One-shot DCAEVT1

16.2.2.21 #define EPWM_TZ_SIGNAL_DCBEVT1

One-shot DCBEVT1

16.2.2.22 #define EPWM_TZ_INTERRUPT_CBC

Trip Zones Cycle By Cycle interrupt

16.2.2.23 #define EPWM_TZ_INTERRUPT_OST

Trip Zones One Shot interrupt

16.2.2.24 #define EPWM_TZ_INTERRUPT_DCAEVT1

Digital Compare A Event 1 interrupt

16.2.2.25 #define EPWM_TZ_INTERRUPT_DCAEVT2

Digital Compare A Event 2 interrupt

16.2.2.26 #define EPWM_TZ_INTERRUPT_DCBEVT1

Digital Compare B Event 1 interrupt

16.2.2.27 #define EPWM_TZ_INTERRUPT_DCBEVT2

Digital Compare B Event 2 interrupt

16.2.2.28 #define EPWM_TZ_FLAG_CBC

Trip Zones Cycle By Cycle flag

16.2.2.29 #define EPWM_TZ_FLAG_OST

Trip Zones One Shot flag

16.2.2.30 #define EPWM_TZ_FLAG_DCAEVT1

Digital Compare A Event 1 flag

16.2.2.31 #define EPWM_TZ_FLAG_DCAEVT2

Digital Compare A Event 2 flag

16.2.2.32 #define EPWM_TZ_FLAG_DCBEVT1

Digital Compare B Event 1 flag

16.2.2.33 #define EPWM_TZ_FLAG_DCBEVT2

Digital Compare B Event 2 flag

16.2.2.34 #define EPWM_TZ_INTERRUPT

Trip Zone interrupt

16.2.2.35 #define EPWM_TZ_CBC_FLAG_1

CBC flag 1

16.2.2.36 #define EPWM_TZ_CBC_FLAG_2

CBC flag 2

16.2.2.37 #define EPWM_TZ_CBC_FLAG_3

CBC flag 3

16.2.2.38 #define EPWM_TZ_CBC_FLAG_4

CBC flag 4

16.2.2.39 #define EPWM_TZ_CBC_FLAG_5

CBC flag 5

16.2.2.40 #define EPWM_TZ_CBC_FLAG_6

CBC flag 6

16.2.2.41 #define EPWM_TZ_CBC_FLAG_DCAEVT2

CBC flag Digital compare event A2

16.2.2.42 #define EPWM_TZ_CBC_FLAG_DCBEVT2

CBC flag Digital compare event B2

16.2.2.43 #define EPWM_TZ_OST_FLAG_OST1

OST flag OST1

16.2.2.44 #define EPWM_TZ_OST_FLAG_OST2

OST flag OST2

16.2.2.45 #define EPWM_TZ_OST_FLAG_OST3

OST flag OST3

16.2.2.46 #define EPWM_TZ_OST_FLAG_OST4

OST flag OST4

16.2.2.47 #define EPWM_TZ_OST_FLAG_OST5

OST flag OST5

16.2.2.48 #define EPWM_TZ_OST_FLAG_OST6

OST flag OST6

16.2.2.49 #define EPWM_TZ_OST_FLAG_DCAEVT1

OST flag Digital compare event A1

16.2.2.50 #define EPWM_TZ_OST_FLAG_DCBEVT1

OST flag Digital compare event B1

16.2.2.51 #define EPWM_TZ_FORCE_EVENT_CBC

Force Cycle By Cycle trip event

16.2.2.52 #define EPWM_TZ_FORCE_EVENT_OST

Force a One-Shot Trip Event

16.2.2.53 #define EPWM_TZ_FORCE_EVENT_DCAEVT1

ForceDigital Compare Output A Event 1

16.2.2.54 #define EPWM_TZ_FORCE_EVENT_DCAEVT2

ForceDigital Compare Output A Event 2

16.2.2.55 #define EPWM_TZ_FORCE_EVENT_DCBEVT1

ForceDigital Compare Output B Event 1

16.2.2.56 #define EPWM_TZ_FORCE_EVENT_DCBEVT2

ForceDigital Compare Output B Event 2

16.2.2.57 #define EPWM_INT_TBCTR_ZERO

Time-base counter equal to zero

16.2.2.58 #define EPWM_INT_TBCTR_PERIOD

Time-base counter equal to period

16.2.2.59 #define EPWM_INT_TBCTR_ZERO_OR_PERIOD

Time-base counter equal to zero or period

16.2.2.60 #define EPWM_INT_TBCTR_U_CMPA

time-base counter equal to CMPA when the timer is incrementing

Referenced by EPWM_setInterruptSource().

16.2.2.61 #define EPWM_INT_TBCTR_U_CMPC

time-base counter equal to CMPC when the timer is incrementing

Referenced by EPWM_setInterruptSource().

16.2.2.62 #define EPWM_INT_TBCTR_D_CMPA

time-base counter equal to CMPA when the timer is decrementing

Referenced by EPWM_setInterruptSource().

16.2.2.63 #define EPWM_INT_TBCTR_D_CMPC

time-base counter equal to CMPC when the timer is decrementing

Referenced by EPWM_setInterruptSource().

16.2.2.64 #define EPWM_INT_TBCTR_U_CMPB

time-base counter equal to CMPB when the timer is incrementing

Referenced by EPWM_setInterruptSource().

16.2.2.65 #define EPWM_INT_TBCTR_U_CMPD

time-base counter equal to CMPD when the timer is incrementing

Referenced by EPWM_setInterruptSource().

16.2.2.66 #define EPWM_INT_TBCTR_D_CMPB

time-base counter equal to CMPB when the timer is decrementing

Referenced by EPWM_setInterruptSource().

16.2.2.67 #define EPWM_INT_TBCTR_D_CMPD

time-base counter equal to CMPD when the timer is decrementing

Referenced by EPWM_setInterruptSource().

16.2.2.68 #define EPWM_DC_COMBINATIONAL_TRIPIN1

Combinational Trip 1 input

16.2.2.69 #define EPWM_DC_COMBINATIONAL_TRIPIN2

Combinational Trip 2 input

16.2.2.70 #define EPWM_DC_COMBINATIONAL_TRIPIN3

Combinational Trip 3 input

16.2.2.71 #define EPWM_DC_COMBINATIONAL_TRIPIN4

Combinational Trip 4 input

16.2.2.72 #define EPWM_DC_COMBINATIONAL_TRIPIN5

Combinational Trip 5 input

16.2.2.73 #define EPWM_DC_COMBINATIONAL_TRIPIN6

Combinational Trip 6 input

16.2.2.74 #define EPWM_DC_COMBINATIONAL_TRIPIN7

Combinational Trip 7 input

16.2.2.75 #define EPWM_DC_COMBINATIONAL_TRIPIN8

Combinational Trip 8 input

16.2.2.76 #define EPWM_DC_COMBINATIONAL_TRIPIN9

Combinational Trip 9 input

16.2.2.77 #define EPWM_DC_COMBINATIONAL_TRIPIN10

Combinational Trip 10 input

16.2.2.78 #define EPWM_DC_COMBINATIONAL_TRIPIN11

Combinational Trip 11 input

16.2.2.79 #define EPWM_DC_COMBINATIONAL_TRIPIN12

Combinational Trip 12 input

16.2.2.80 #define EPWM_DC_COMBINATIONAL_TRIPIN14

Combinational Trip 14 input

16.2.2.81 #define EPWM_DC_COMBINATIONAL_TRIPIN15

Combinational Trip 15 input

16.2.2.82 #define EPWM_GL_REGISTER_TBPRD_TBPRDHR

Global load TBPRD:TBPRDHR

16.2.2.83 #define EPWM_GL_REGISTER_CMPA_CMPAHR

Global load CMPA:CMPAHR

16.2.2.84 #define EPWM_GL_REGISTER_CMPB_CMPBHR

Global load CMPB:CMPBHR

16.2.2.85 #define EPWM_GL_REGISTER_CMPC

Global load CMPC

16.2.2.86 #define EPWM_GL_REGISTER_CMPD

Global load CMPD

16.2.2.87 #define EPWM_GL_REGISTER_DBRED_DBREDHR

Global load DBRED:DBREDHR

16.2.2.88 #define EPWM_GL_REGISTER_DBFED_DBFEDHR

Global load DBFED:DBFEDHR

16.2.2.89 #define EPWM_GL_REGISTER_DBCTL

Global load DBCTL

16.2.2.90 #define EPWM_GL_REGISTER_AQCTLA_AQCTLA2

Global load AQCTLA/A2

16.2.2.91 #define EPWM_GL_REGISTER_AQCTLB_AQCTLB2

Global load AQCTLB/B2

16.2.2.92 #define EPWM_GL_REGISTER_AQCSFRC

Global load AQCSFRC

16.2.3 Enumeration Type Documentation

16.2.3.1 enum **EPWM_EmulationMode**

Values that can be passed to EPWM_setEmulationMode() as the *emulationMode* parameter.

Enumerator

EPWM_EMULATION_STOP_AFTER_NEXT_TB Stop after next Time Base counter increment or decrement.

EPWM_EMULATION_STOP_AFTER_FULL_CYCLE Stop when counter completes whole cycle.

EPWM_EMULATION_FREE_RUN Free run.

16.2.3.2 enum **EPWM_SyncCountMode**

Values that can be passed to EPWM_setCountModeAfterSync() as the *mode* parameter.

Enumerator

EPWM_COUNT_MODE_DOWN_AFTER_SYNC Count down after sync event.

EPWM_COUNT_MODE_UP_AFTER_SYNC Count up after sync event.

16.2.3.3 enum **EPWM_ClockDivider**

Values that can be passed to EPWM_setClockPrescaler() as the *prescaler* parameter.

Enumerator

EPWM_CLOCK_DIVIDER_1 Divide clock by 1.

EPWM_CLOCK_DIVIDER_2 Divide clock by 2.

EPWM_CLOCK_DIVIDER_4 Divide clock by 4.
EPWM_CLOCK_DIVIDER_8 Divide clock by 8.
EPWM_CLOCK_DIVIDER_16 Divide clock by 16.
EPWM_CLOCK_DIVIDER_32 Divide clock by 32.
EPWM_CLOCK_DIVIDER_64 Divide clock by 64.
EPWM_CLOCK_DIVIDER_128 Divide clock by 128.

16.2.3.4 enum **EPWM_HSClockDivider**

Values that can be passed to EPWM_setClockPrescaler() as the *highSpeedPrescaler* parameter.

Enumerator

EPWM_HSCLOCK_DIVIDER_1 Divide clock by 1.
EPWM_HSCLOCK_DIVIDER_2 Divide clock by 2.
EPWM_HSCLOCK_DIVIDER_4 Divide clock by 4.
EPWM_HSCLOCK_DIVIDER_6 Divide clock by 6.
EPWM_HSCLOCK_DIVIDER_8 Divide clock by 8.
EPWM_HSCLOCK_DIVIDER_10 Divide clock by 10.
EPWM_HSCLOCK_DIVIDER_12 Divide clock by 12.
EPWM_HSCLOCK_DIVIDER_14 Divide clock by 14.

16.2.3.5 enum **EPWM_SyncOutPulseMode**

Values that can be passed to EPWM_setSyncOutPulseMode() as the *mode* parameter.

Enumerator

EPWM_SYNC_OUT_PULSE_ON_SOFTWARE sync pulse is generated by software
EPWM_SYNC_OUT_PULSE_ON_EPWMxSYNCIN sync pulse is passed from EPWMxSYNCIN
EPWM_SYNC_OUT_PULSE_ON_COUNTER_ZERO sync pulse is generated when time base counter equals zero
EPWM_SYNC_OUT_PULSE_ON_COUNTER_COMPARE_B sync pulse is generated when time base counter equals compare B value.
EPWM_SYNC_OUT_PULSE_DISABLED sync pulse is disabled
EPWM_SYNC_OUT_PULSE_ON_COUNTER_COMPARE_C sync pulse is generated when time base counter equals compare D value.
EPWM_SYNC_OUT_PULSE_ON_COUNTER_COMPARE_D sync pulse is disabled.

16.2.3.6 enum **EPWM_PeriodLoadMode**

Values that can be passed to EPWM_setPeriodLoadMode() as the *loadMode* parameter.

Enumerator

EPWM_PERIOD_SHADOW_LOAD PWM Period register access is through shadow register.

EPWM_PERIOD_DIRECT_LOAD PWM Period register access is directly.

16.2.3.7 enum **EPWM_TimeBaseCountMode**

Values that can be passed to EPWM_setTimeBaseCounterMode() as the *counterMode* parameter.

Enumerator

EPWM_COUNTER_MODE_UP Up - count mode.
EPWM_COUNTER_MODE_DOWN Down - count mode.
EPWM_COUNTER_MODE_UP_DOWN Up - down - count mode.
EPWM_COUNTER_MODE_STOP_FREEZE Stop - Freeze counter.

16.2.3.8 enum **EPWM_PeriodShadowLoadMode**

Values that can be passed to EPWM_selectPeriodLoadEvent() as the *shadowLoadMode* parameter.

Enumerator

EPWM_SHADOW_LOAD_MODE_COUNTER_ZERO shadow to active load occurs when time base counter reaches 0.
EPWM_SHADOW_LOAD_MODE_COUNTER_SYNC shadow to active load occurs when time base counter reaches 0 and a SYNC occurs
EPWM_SHADOW_LOAD_MODE_SYNC shadow to active load occurs only when a SYNC occurs

16.2.3.9 enum **EPWM_CurrentLink**

Values that can be passed to EPWM_setupEPWMLinks() as the *epwmLink* parameter.

Enumerator

EPWM_LINK_WITH_EPWM_1 link current ePWM with ePWM1
EPWM_LINK_WITH_EPWM_2 link current ePWM with ePWM2
EPWM_LINK_WITH_EPWM_3 link current ePWM with ePWM3
EPWM_LINK_WITH_EPWM_4 link current ePWM with ePWM4
EPWM_LINK_WITH_EPWM_5 link current ePWM with ePWM5
EPWM_LINK_WITH_EPWM_6 link current ePWM with ePWM6
EPWM_LINK_WITH_EPWM_7 link current ePWM with ePWM7
EPWM_LINK_WITH_EPWM_8 link current ePWM with ePWM8
EPWM_LINK_WITH_EPWM_9 link current ePWM with ePWM9
EPWM_LINK_WITH_EPWM_10 link current ePWM with ePWM10
EPWM_LINK_WITH_EPWM_11 link current ePWM with ePWM11
EPWM_LINK_WITH_EPWM_12 link current ePWM with ePWM12

16.2.3.10 enum **EPWM_LinkComponent**

Values that can be passed to EPWM_setupEPWMLinks() as the *linkComp* parameter.

Enumerator

EPWM_LINK_TBPRD link TBPRD:TBPRDHR registers

EPWM_LINK_COMP_A link COMPA registers

EPWM_LINK_COMP_B link COMPB registers

EPWM_LINK_COMP_C link COMPC registers

EPWM_LINK_COMP_D link COMPD registers

EPWM_LINK_GLDCTL2 link GLDCTL2 registers

16.2.3.11 enum **EPWM_CounterCompareModule**

Values that can be passed to the EPWM_getCounterCompareShadowStatus(), EPWM_setCounterCompareValue(), EPWM_setCounterCompareShadowLoadMode(), EPWM_disableCounterCompareShadowLoadMode() as the *compModule* parameter.

Enumerator

EPWM_COUNTER_COMPARE_A counter compare A

EPWM_COUNTER_COMPARE_B counter compare B

EPWM_COUNTER_COMPARE_C counter compare C

EPWM_COUNTER_COMPARE_D counter compare D

16.2.3.12 enum **EPWM_CounterCompareLoadMode**

Values that can be passed to EPWM_setCounterCompareShadowLoadMode() as the *loadMode* parameter.

Enumerator

EPWM_COMP_LOAD_ON_CNTR_ZERO load when counter equals zero

EPWM_COMP_LOAD_ON_CNTR_PERIOD load when counter equals period

EPWM_COMP_LOAD_ON_CNTR_ZERO_PERIOD load when counter equals zero or period

EPWM_COMP_LOAD_FREEZE Freeze shadow to active load.

EPWM_COMP_LOAD_ON_SYNC_CNTR_ZERO load when counter equals zero

EPWM_COMP_LOAD_ON_SYNC_CNTR_PERIOD load when counter equals period

EPWM_COMP_LOAD_ON_SYNC_CNTR_ZERO_PERIOD load when counter equals zero or period

EPWM_COMP_LOAD_ON_SYNC_ONLY load on sync only

16.2.3.13 enum **EPWM_ActionQualifierModule**

Values that can be passed to EPWM_setActionQualifierShadowLoadMode() and EPWM_disableActionQualifierShadowLoadMode() as the *aqModule* parameter.

Enumerator

EPWM_ACTION_QUALIFIER_A Action Qualifier A.

EPWM_ACTION_QUALIFIER_B Action Qualifier B.

16.2.3.14 enum **EPWM_ActionQualifierLoadMode**

Values that can be passed to EPWM_setActionQualifierShadowLoadMode() as the *loadMode* parameter.

Enumerator

EPWM_AQ_LOAD_ON_CNTR_ZERO load when counter equals zero

EPWM_AQ_LOAD_ON_CNTR_PERIOD load when counter equals period

EPWM_AQ_LOAD_ON_CNTR_ZERO_PERIOD load when counter equals zero or period

EPWM_AQ_LOAD_FREEZE Freeze shadow to active load.

EPWM_AQ_LOAD_ON_SYNC_CNTR_ZERO load on sync or when counter equals zero

EPWM_AQ_LOAD_ON_SYNC_CNTR_PERIOD load on sync or when counter equals period

EPWM_AQ_LOAD_ON_SYNC_CNTR_ZERO_PERIOD load on sync or when counter equals zero or period

EPWM_AQ_LOAD_ON_SYNC_ONLY load on sync only

16.2.3.15 enum **EPWM_ActionQualifierTriggerSource**

Values that can be passed to EPWM_setActionQualifierT1TriggerSource() and EPWM_setActionQualifierT2TriggerSource() as the *trigger* parameter.

Enumerator

EPWM_AQ_TRIGGER_EVENT_TRIG_DCA_1 Digital compare event A 1.

EPWM_AQ_TRIGGER_EVENT_TRIG_DCA_2 Digital compare event A 2.

EPWM_AQ_TRIGGER_EVENT_TRIG_DCB_1 Digital compare event B 1.

EPWM_AQ_TRIGGER_EVENT_TRIG_DCB_2 Digital compare event B 2.

EPWM_AQ_TRIGGER_EVENT_TRIG_TZ_1 Trip zone 1.

EPWM_AQ_TRIGGER_EVENT_TRIG_TZ_2 Trip zone 2.

EPWM_AQ_TRIGGER_EVENT_TRIG_TZ_3 Trip zone 3.

EPWM_AQ_TRIGGER_EVENT_TRIG_EPWM_SYNCIN ePWM sync

16.2.3.16 enum **EPWM_ActionQualifierOutputEvent**

Values that can be passed to EPWM_setActionQualifierAction() as the *event* parameter.

Enumerator

EPWM_AQ_OUTPUT_ON_TIMEBASE_ZERO Time base counter equals zero.

EPWM_AQ_OUTPUT_ON_TIMEBASE_PERIOD Time base counter equals period.

EPWM_AQ_OUTPUT_ON_TIMEBASE_UP_CMPA Time base counter up equals COMPA.

EPWM_AQ_OUTPUT_ON_TIMEBASE_DOWN_CMPA Time base counter down equals COMPA.

EPWM_AQ_OUTPUT_ON_TIMEBASE_UP_CMPB Time base counter up equals COMPB.

EPWM_AQ_OUTPUT_ON_TIMEBASE_DOWN_CMPB Time base counter down equals COMPB.

EPWM_AQ_OUTPUT_ON_T1_COUNT_UP T1 event on count up.

EPWM_AQ_OUTPUT_ON_T1_COUNT_DOWN T1 event on count down.

EPWM_AQ_OUTPUT_ON_T2_COUNT_UP T2 event on count up.
EPWM_AQ_OUTPUT_ON_T2_COUNT_DOWN T2 event on count down.

16.2.3.17 enum **EPWM_ActionQualifierOutput**

Values that can be passed to EPWM_setActionQualifierSWAction(), EPWM_setActionQualifierAction() as the *outPut* parameter.

Enumerator

EPWM_AQ_OUTPUT_NO_CHANGE No change in the output pins.
EPWM_AQ_OUTPUT_LOW Set output pins to low.
EPWM_AQ_OUTPUT_HIGH Set output pins to High.
EPWM_AQ_OUTPUT_TOGGLE Toggle the output pins.

16.2.3.18 enum **EPWM_ActionQualifierSWOutput**

Values that can be passed to EPWM_setActionQualifierContSWForceAction() as the *outPut* parameter.

Enumerator

EPWM_AQ_SW_DISABLED Software forcing disabled.
EPWM_AQ_SW_OUTPUT_LOW Set output pins to low.
EPWM_AQ_SW_OUTPUT_HIGH Set output pins to High.

16.2.3.19 enum **EPWM_ActionQualifierEventAction**

Values that can be passed to EPWM_setActionQualifierActionComplete() as the *action* parameter.

Enumerator

EPWM_AQ_OUTPUT_NO_CHANGE_ZERO Time base counter equals zero and no change in the output pins.
EPWM_AQ_OUTPUT_LOW_ZERO Time base counter equals zero and set output pins to low.
EPWM_AQ_OUTPUT_HIGH_ZERO Time base counter equals zero and set output pins to high.
EPWM_AQ_OUTPUT_TOGGLE_ZERO Time base counter equals zero and toggle the output pins.
EPWM_AQ_OUTPUT_NO_CHANGE_PERIOD Time base counter equals period and no change in the output pins.
EPWM_AQ_OUTPUT_LOW_PERIOD Time base counter equals period and set output pins to low.
EPWM_AQ_OUTPUT_HIGH_PERIOD Time base counter equals period and set output pins to high.
EPWM_AQ_OUTPUT_TOGGLE_PERIOD Time base counter equals period and toggle the output pins.

EPWM_AQ_OUTPUT_NO_CHANGE_UP_CMPA Time base counter up equals COMPA and no change in the output pins.
EPWM_AQ_OUTPUT_LOW_UP_CMPA Time base counter up equals COMPA and set output pins to low.
EPWM_AQ_OUTPUT_HIGH_UP_CMPA Time base counter up equals COMPA and set output pins to high.
EPWM_AQ_OUTPUT_TOGGLE_UP_CMPA Time base counter up equals COMPA and toggle the output pins.
EPWM_AQ_OUTPUT_NO_CHANGE_DOWN_CMPA Time base counter down equals COMPA and no change in the output pins.
EPWM_AQ_OUTPUT_LOW_DOWN_CMPA Time base counter down equals COMPA and set output pins to low.
EPWM_AQ_OUTPUT_HIGH_DOWN_CMPA Time base counter down equals COMPA and set output pins to high.
EPWM_AQ_OUTPUT_TOGGLE_DOWN_CMPA Time base counter down equals COMPA and toggle the output pins.
EPWM_AQ_OUTPUT_NO_CHANGE_UP_CMPB Time base counter up equals COMPB and no change in the output pins.
EPWM_AQ_OUTPUT_LOW_UP_CMPB Time base counter up equals COMPB and set output pins to low.
EPWM_AQ_OUTPUT_HIGH_UP_CMPB Time base counter up equals COMPB and set output pins to high.
EPWM_AQ_OUTPUT_TOGGLE_UP_CMPB Time base counter up equals COMPB and toggle the output pins.
EPWM_AQ_OUTPUT_NO_CHANGE_DOWN_CMPB Time base counter down equals COMPB and no change in the output pins.
EPWM_AQ_OUTPUT_LOW_DOWN_CMPB Time base counter down equals COMPB and set output pins to low.
EPWM_AQ_OUTPUT_HIGH_DOWN_CMPB Time base counter down equals COMPB and set output pins to high.
EPWM_AQ_OUTPUT_TOGGLE_DOWN_CMPB Time base counter down equals COMPB and toggle the output pins.

16.2.3.20 enum **EPWM_AdditionalActionQualifierEventAction**

Values that can be passed to EPWM_setAdditionalActionQualifierActionComplete() as the *action* parameter.

Enumerator

EPWM_AQ_OUTPUT_NO_CHANGE_UP_T1 T1 event on count up and no change in the output pins.
EPWM_AQ_OUTPUT_LOW_UP_T1 T1 event on count up and set output pins to low.
EPWM_AQ_OUTPUT_HIGH_UP_T1 T1 event on count up and set output pins to high.
EPWM_AQ_OUTPUT_TOGGLE_UP_T1 T1 event on count up and toggle the output pins.
EPWM_AQ_OUTPUT_NO_CHANGE_DOWN_T1 T1 event on count down and no change in the output pins.
EPWM_AQ_OUTPUT_LOW_DOWN_T1 T1 event on count down and set output pins to low.
EPWM_AQ_OUTPUT_HIGH_DOWN_T1 T1 event on count down and set output pins to high.

EPWM_AQ_OUTPUT_TOGGLE_DOWN_T1 T1 event on count down and toggle the output pins.
EPWM_AQ_OUTPUT_NO_CHANGE_UP_T2 T2 event on count up and no change in the output pins.
EPWM_AQ_OUTPUT_LOW_UP_T2 T2 event on count up and set output pins to low.
EPWM_AQ_OUTPUT_HIGH_UP_T2 T2 event on count up and set output pins to high.
EPWM_AQ_OUTPUT_TOGGLE_UP_T2 T2 event on count up and toggle the output pins.
EPWM_AQ_OUTPUT_NO_CHANGE_DOWN_T2 T2 event on count down and no change in the output pins.
EPWM_AQ_OUTPUT_LOW_DOWN_T2 T2 event on count down and set output pins to low.
EPWM_AQ_OUTPUT_HIGH_DOWN_T2 T2 event on count down and set output pins to high.
EPWM_AQ_OUTPUT_TOGGLE_DOWN_T2 T2 event on count down and toggle the output pins.

16.2.3.21 enum **EPWM_ActionQualifierOutputModule**

Values that can be passed to EPWM_forceActionQualifierSWAction(), EPWM_setActionQualifierSWAction(), EPWM_setActionQualifierAction() EPWM_setActionQualifierContSWForceAction() as the *epwmOutput* parameter.

Enumerator

EPWM_AQ_OUTPUT_A ePWMxA output
EPWM_AQ_OUTPUT_B ePWMxB output

16.2.3.22 enum **EPWM_ActionQualifierContForce**

Values that can be passed to EPWM_setActionQualifierContSWForceShadowMode() as the *mode* parameter.

Enumerator

EPWM_AQ_SW_SH_LOAD_ON_CNTR_ZERO shadow mode load when counter equals zero
EPWM_AQ_SW_SH_LOAD_ON_CNTR_PERIOD shadow mode load when counter equals period
EPWM_AQ_SW_SH_LOAD_ON_CNTR_ZERO_PERIOD shadow mode load when counter equals zero or period
EPWM_AQ_SW_IMMEDIATE_LOAD No shadow load mode. Immediate mode only.

16.2.3.23 enum **EPWM_DeadBandOutput**

Values that can be passed to EPWM_setDeadBandOutputSwapMode() as the *output* parameter.

Enumerator

EPWM_DB_OUTPUT_A DB output is ePWMA.
EPWM_DB_OUTPUT_B DB output is ePWMB.

16.2.3.24 enum **EPWM_DeadBandDelayMode**

Values that can be passed to EPWM_setDeadBandDelayPolarity(), EPWM_setDeadBandDelayMode() as the *delayMode* parameter.

Enumerator

EPWM_DB_RED DB RED (Rising Edge Delay) mode.

EPWM_DB_FED DB FED (Falling Edge Delay) mode.

16.2.3.25 enum **EPWM_DeadBandPolarity**

Values that can be passed to EPWM_setDeadBandDelayPolarity as the *polarity* parameter.

Enumerator

EPWM_DB_POLARITY_ACTIVE_HIGH DB polarity is not inverted.

EPWM_DB_POLARITY_ACTIVE_LOW DB polarity is inverted.

16.2.3.26 enum **EPWM_DeadBandControlLoadMode**

Values that can be passed to EPWM_setDeadBandControlShadowLoadMode() as the *loadMode* parameter.

Enumerator

EPWM_DB_LOAD_ON_CNTR_ZERO load when counter equals zero

EPWM_DB_LOAD_ON_CNTR_PERIOD load when counter equals period

EPWM_DB_LOAD_ON_CNTR_ZERO_PERIOD load when counter equals zero or period

EPWM_DB_LOAD_FREEZE Freeze shadow to active load.

16.2.3.27 enum **EPWM_RisingEdgeDelayLoadMode**

Values that can be passed to EPWM_setRisingEdgeDelayCountShadowLoadMode() as the *loadMode* parameter.

Enumerator

EPWM_RED_LOAD_ON_CNTR_ZERO load when counter equals zero

EPWM_RED_LOAD_ON_CNTR_PERIOD load when counter equals period

EPWM_RED_LOAD_ON_CNTR_ZERO_PERIOD load when counter equals zero or period

EPWM_RED_LOAD_FREEZE Freeze shadow to active load.

16.2.3.28 enum **EPWM_FallingEdgeDelayLoadMode**

Values that can be passed to EPWM_setFallingEdgeDelayCountShadowLoadMode() as the *loadMode* parameter.

Enumerator

EPWM_FED_LOAD_ON_CNTR_ZERO load when counter equals zero

EPWM_FED_LOAD_ON_CNTR_PERIOD load when counter equals period
EPWM_FED_LOAD_ON_CNTR_ZERO_PERIOD load when counter equals zero or period
EPWM_FED_LOAD_FREEZE Freeze shadow to active load.

16.2.3.29 enum **EPWM_DeadBandClockMode**

Values that can be passed to EPWM_setDeadBandCounterClock() as the *clockMode* parameter.

Enumerator
EPWM_DB_COUNTER_CLOCK_FULL_CYCLE Dead band counter runs at TBCLK rate.
EPWM_DB_COUNTER_CLOCK_HALF_CYCLE Dead band counter runs at 2∗TBCLK rate.

16.2.3.30 enum **EPWM_TripZoneDigitalCompareOutput**

Values that can be passed to EPWM_setTripZoneDigitalCompareEventCondition() as the *dcType* parameter.

Enumerator
EPWM_TZ_DC_OUTPUT_A1 Digital Compare output 1 A.
EPWM_TZ_DC_OUTPUT_A2 Digital Compare output 2 A.
EPWM_TZ_DC_OUTPUT_B1 Digital Compare output 1 B.
EPWM_TZ_DC_OUTPUT_B2 Digital Compare output 2 B.

16.2.3.31 enum **EPWM_TripZoneDigitalCompareOutputEvent**

Values that can be passed to EPWM_setTripZoneDigitalCompareEventCondition() as the *dcEvent* parameter.

Enumerator
EPWM_TZ_EVENT_DC_DISABLED Event is disabled.
EPWM_TZ_EVENT_DCXH_LOW Event when DCxH low.
EPWM_TZ_EVENT_DCXH_HIGH Event when DCxH high.
EPWM_TZ_EVENT_DCXL_LOW Event when DCxL low.
EPWM_TZ_EVENT_DCXL_HIGH Event when DCxL high.
EPWM_TZ_EVENT_DCXL_HIGH_DCXH_LOW Event when DCxL high DCxH low.

16.2.3.32 enum **EPWM_TripZoneEvent**

Values that can be passed to EPWM_setTripZoneAction() as the *tzEvent* parameter.

Enumerator
EPWM_TZ_ACTION_EVENT_TZA TZ1 - TZ6, DCAEVT2, DCAEVT1.
EPWM_TZ_ACTION_EVENT_TZB TZ1 - TZ6, DCBEVT2, DCBEVT1.
EPWM_TZ_ACTION_EVENT_DCAEVT1 DCAEVT1 (Digital Compare A event 1)
EPWM_TZ_ACTION_EVENT_DCAEVT2 DCAEVT2 (Digital Compare A event 2)

EPWM_TZ_ACTION_EVENT_DCBEVT1 DCBEVT1 (Digital Compare B event 1)
EPWM_TZ_ACTION_EVENT_DCBEVT2 DCBEVT2 (Digital Compare B event 2)

16.2.3.33 enum **EPWM_TripZoneAction**

Values that can be passed to EPWM_setTripZoneAction() as the *tzAction* parameter.

Enumerator

EPWM_TZ_ACTION_HIGH_Z high impedance output
EPWM_TZ_ACTION_HIGH high voltage state
EPWM_TZ_ACTION_LOW low voltage state
EPWM_TZ_ACTION_DISABLE disable action

16.2.3.34 enum **EPWM_TripZoneAdvancedEvent**

Values that can be passed to EPWM_setTripZoneAdvAction() as the *tzAdvEvent* parameter.

Enumerator

EPWM_TZ_ADV_ACTION_EVENT_TZB_D TZ1 - TZ6, DCBEVT2, DCBEVT1 while counting down.
EPWM_TZ_ADV_ACTION_EVENT_TZB_U TZ1 - TZ6, DCBEVT2, DCBEVT1 while counting up.
EPWM_TZ_ADV_ACTION_EVENT_TZA_D TZ1 - TZ6, DCAEVT2, DCAEVT1 while counting down.
EPWM_TZ_ADV_ACTION_EVENT_TZA_U TZ1 - TZ6, DCAEVT2, DCAEVT1 while counting up.

16.2.3.35 enum **EPWM_TripZoneAdvancedAction**

Values that can be passed to EPWM_setTripZoneAdvDigitalCompareActionA(), EPWM_setTripZoneAdvDigitalCompareActionB(), EPWM_setTripZoneAdvAction() as the *tzAdvDCAction* parameter.

Enumerator

EPWM_TZ_ADV_ACTION_HIGH_Z high impedance output
EPWM_TZ_ADV_ACTION_HIGH high voltage state
EPWM_TZ_ADV_ACTION_LOW low voltage state
EPWM_TZ_ADV_ACTION_TOGGLE toggle the output
EPWM_TZ_ADV_ACTION_DISABLE disable action

16.2.3.36 enum **EPWM_TripZoneAdvDigitalCompareEvent**

Values that can be passed to EPWM_setTripZoneAdvDigitalCompareActionA() and EPWM_setTripZoneAdvDigitalCompareActionB() as the *tzAdvDCEvent* parameter.

Enumerator

EPWM_TZ_ADV_ACTION_EVENT_DCxEVT1_U Digital Compare event A/B 1 while counting up.

EPWM_TZ_ADV_ACTION_EVENT_DCxEVT1_D Digital Compare event A/B 1 while counting down.

EPWM_TZ_ADV_ACTION_EVENT_DCxEVT2_U Digital Compare event A/B 2 while counting up.

EPWM_TZ_ADV_ACTION_EVENT_DCxEVT2_D Digital Compare event A/B 2 while counting down.

16.2.3.37 enum **EPWM_CycleByCycleTripZoneClearMode**

Values that can be passed to EPWM_selectCycleByCycleTripZoneClearEvent() as the *clearMode* parameter.

Enumerator

EPWM_TZ_CBC_PULSE_CLR_CNTR_ZERO Clear CBC pulse when counter equals zero.

EPWM_TZ_CBC_PULSE_CLR_CNTR_PERIOD Clear CBC pulse when counter equals period.

EPWM_TZ_CBC_PULSE_CLR_CNTR_ZERO_PERIOD Clear CBC pulse when counter equals zero or period.

16.2.3.38 enum **EPWM_ADCStartOfConversionType**

Values that can be passed to EPWM_enableADCTrigger(), EPWM_disableADCTrigger(), EPWM_setADCTriggerSource(), EPWM_setADCTriggerEventPrescale(), EPWM_getADCTriggerFlagStatus(), EPWM_clearADCTriggerFlag(), EPWM_enableADCTriggerEventCountInit(), EPWM_disableADCTriggerEventCountInit(), EPWM_forceADCTriggerEventCountInit(), EPWM_setADCTriggerEventCountInitValue(), EPWM_getADCTriggerEventCount(), EPWM_forceADCTrigger() as the *adcSOCType* parameter

Enumerator

EPWM_SOC_A SOC A.

EPWM_SOC_B SOC B.

16.2.3.39 enum **EPWM_ADCStartOfConversionSource**

Values that can be passed to EPWM_setADCTriggerSource() as the *socSource* parameter.

Enumerator

EPWM_SOC_DCxEVT1 Event is based on DCxEVT1.

EPWM_SOC_TBCTR_ZERO Time-base counter equal to zero.

EPWM_SOC_TBCTR_PERIOD Time-base counter equal to period.

EPWM_SOC_TBCTR_ZERO_OR_PERIOD Time-base counter equal to zero or period.

EPWM_SOC_TBCTR_U_CMPA time-base counter equal to CMPA when the timer is incrementing

EPWM_SOC_TBCTR_U_CMPC time-base counter equal to CMPC when the timer is incrementing

EPWM_SOC_TBCTR_D_CMPA time-base counter equal to CMPA when the timer is decrementing

EPWM_SOC_TBCTR_D_CMPC time-base counter equal to CMPC when the timer is decrementing

EPWM_SOC_TBCTR_U_CMPB time-base counter equal to CMPB when the timer is incrementing

EPWM_SOC_TBCTR_U_CMPD time-base counter equal to CMPD when the timer is incrementing

EPWM_SOC_TBCTR_D_CMPB time-base counter equal to CMPB when the timer is decrementing

EPWM_SOC_TBCTR_D_CMPD time-base counter equal to CMPD when the timer is decrementing

16.2.3.40 enum **EPWM_DigitalCompareType**

Values that can be passed to EPWM_selectDigitalCompareTripInput(), EPWM_enableDigitalCompareTripCombinationInput(), EPWM_disableDigitalCompareTripCombinationInput() as the *dcType* parameter.

Enumerator

EPWM_DC_TYPE_DCAH Digital Compare A High.

EPWM_DC_TYPE_DCAL Digital Compare A Low.

EPWM_DC_TYPE_DCBH Digital Compare B High.

EPWM_DC_TYPE_DCBL Digital Compare B Low.

16.2.3.41 enum **EPWM_DigitalCompareTripInput**

Values that can be passed to EPWM_selectDigitalCompareTripInput() as the *tripSource* parameter.

Enumerator

EPWM_DC_TRIP_TRIPIN1 Trip 1.

EPWM_DC_TRIP_TRIPIN2 Trip 2.

EPWM_DC_TRIP_TRIPIN3 Trip 3.

EPWM_DC_TRIP_TRIPIN4 Trip 4.

EPWM_DC_TRIP_TRIPIN5 Trip 5.

EPWM_DC_TRIP_TRIPIN6 Trip 6.

EPWM_DC_TRIP_TRIPIN7 Trip 7.

EPWM_DC_TRIP_TRIPIN8 Trip 8.

EPWM_DC_TRIP_TRIPIN9 Trip 9.

EPWM_DC_TRIP_TRIPIN10 Trip 10.

EPWM_DC_TRIP_TRIPIN11 Trip 11.

EPWM_DC_TRIP_TRIPIN12 Trip 12.

EPWM_DC_TRIP_TRIPIN14 Trip 14.

EPWM_DC_TRIP_TRIPIN15 Trip 15.

EPWM_DC_TRIP_COMBINATION All Trips (Trip1 - Trip 15) are selected.

16.2.3.42 enum **EPWM_DigitalCompareBlankingPulse**

Values that can be passed to EPWM_setDigitalCompareBlankingEvent() as the the *blankingPulse* parameter.

Enumerator

EPWM_DC_WINDOW_START_TBCTR_PERIOD Time base counter equals period.

EPWM_DC_WINDOW_START_TBCTR_ZERO Time base counter equals zero.

EPWM_DC_WINDOW_START_TBCTR_ZERO_PERIOD Time base counter equals zero.

16.2.3.43 enum **EPWM_DigitalCompareFilterInput**

Values that can be passed to EPWM_setDigitalCompareFilterInput() as the *filterInput* parameter.

Enumerator

EPWM_DC_WINDOW_SOURCE_DCAEVT1 DC filter signal source is DCAEVT1.

EPWM_DC_WINDOW_SOURCE_DCAEVT2 DC filter signal source is DCAEVT2.

EPWM_DC_WINDOW_SOURCE_DCBEVT1 DC filter signal source is DCBEVT1.

EPWM_DC_WINDOW_SOURCE_DCBEVT2 DC filter signal source is DCBEVT2.

16.2.3.44 enum **EPWM_DigitalCompareModule**

Values that can be assigned to EPWM_setDigitalCompareEventSource(), EPWM_setDigitalCompareEventSyncMode(), EPWM_enableDigitalCompareSyncEvent() EPWM_enableDigitalCompareADCTrigger(), EPWM_disableDigitalCompareSyncEvent() EPWM_disableDigitalCompareADCTrigger() as the *dcModule* parameter.

Enumerator

EPWM_DC_MODULE_A Digital Compare Module A.

EPWM_DC_MODULE_B Digital Compare Module B.

16.2.3.45 enum **EPWM_DigitalCompareEvent**

Values that can be passed to EPWM_setDigitalCompareEventSource(), EPWM_setDigitalCompareEventSyncMode as the *dcEvent* parameter.

Enumerator

EPWM_DC_EVENT_1 Digital Compare Event number 1.

EPWM_DC_EVENT_2 Digital Compare Event number 2.

16.2.3.46 enum **EPWM_DigitalCompareEventSource**

Values that can be passed to EPWM_setDigitalCompareEventSource() as the *dcEventSource* parameter.

Enumerator

EPWM_DC_EVENT_SOURCE_ORIG_SIGNAL signal source is unfiltered (DCAEVT1/2)

EPWM_DC_EVENT_SOURCE_FILT_SIGNAL signal source is filtered (DCEVTFILT)

16.2.3.47 enum **EPWM_DigitalCompareSyncMode**

Values that can be passed to EPWM_setDigitalCompareEventSyncMode() as the *syncMode* parameter.

Enumerator

EPWM_DC_EVENT_INPUT_SYNCED DC input signal is synced with TBCLK.

EPWM_DC_EVENT_INPUT_NOT_SYNCED DC input signal is not synced with TBCLK.

16.2.3.48 enum **EPWM_GlobalLoadTrigger**

Values that can be passed to EPWM_setGlobalLoadTrigger() as the *loadTrigger* parameter.

Enumerator

EPWM_GL_LOAD_PULSE_CNTR_ZERO load when counter is equal to zero

EPWM_GL_LOAD_PULSE_CNTR_PERIOD load when counter is equal to period

EPWM_GL_LOAD_PULSE_CNTR_ZERO_PERIOD load when counter is equal to zero or period

EPWM_GL_LOAD_PULSE_SYNC load on sync event

EPWM_GL_LOAD_PULSE_SYNC_OR_CNTR_ZERO load on sync event or when counter is equal to zero

EPWM_GL_LOAD_PULSE_SYNC_OR_CNTR_PERIOD load on sync event or when counter is equal to period

EPWM_GL_LOAD_PULSE_SYNC_CNTR_ZERO_PERIOD load on sync event or when counter is equal to period or zero

EPWM_GL_LOAD_PULSE_GLOBAL_FORCE load on global force

16.2.3.49 enum **EPWM_ValleyTriggerSource**

Values that can be passed to EPWM_setValleyTriggerSource() as the *trigger* parameter.

Enumerator

EPWM_VALLEY_TRIGGER_EVENT_SOFTWARE Valley capture trigged by software.

EPWM_VALLEY_TRIGGER_EVENT_CNTR_ZERO Valley capture trigged by when counter is equal to zero.

EPWM_VALLEY_TRIGGER_EVENT_CNTR_PERIOD Valley capture trigged by when counter is equal period.

EPWM_VALLEY_TRIGGER_EVENT_CNTR_ZERO_PERIOD Valley capture trigged when counter is equal to zero or period.

EPWM_VALLEY_TRIGGER_EVENT_DCAEVT1 Valley capture trigged by DCAEVT1 (Digital Compare A event 1)

EPWM_VALLEY_TRIGGER_EVENT_DCAEVT2 Valley capture trigged by DCAEVT2 (Digital Compare A event 2)

EPWM_VALLEY_TRIGGER_EVENT_DCBEVT1 Valley capture trigged by DCBEVT1 (Digital Compare B event 1)

EPWM_VALLEY_TRIGGER_EVENT_DCBEVT2 Valley capture trigged by DCBEVT2 (Digital Compare B event 2)

16.2.3.50 enum **EPWM_ValleyCounterEdge**

Values that can be passed to EPWM_getValleyCountEdgeStatus() as the *edge* parameter.

Enumerator

EPWM_VALLEY_COUNT_START_EDGE Valley count start edge.

EPWM_VALLEY_COUNT_STOP_EDGE Valley count stop edge.

16.2.3.51 enum **EPWM_ValleyDelayMode**

Values that can be passed to EPWM_setValleyDelayValue() as the *delayMode* parameter.

Enumerator

EPWM_VALLEY_DELAY_MODE_SW_DELAY Delay value equals the offset value defines by software.

EPWM_VALLEY_DELAY_MODE_VCNT_DELAY_SW_DELAY Delay value equals the sum of the Hardware counter value and the offset value defines by software

EPWM_VALLEY_DELAY_MODE_VCNT_DELAY_SHIFT_1_SW_DELAY Delay value equals the the Hardware counter shifted by (1 + the offset value defines by software)

EPWM_VALLEY_DELAY_MODE_VCNT_DELAY_SHIFT_2_SW_DELAY Delay value equals the the Hardware counter shifted by (2 + the offset value defines by software)

EPWM_VALLEY_DELAY_MODE_VCNT_DELAY_SHIFT_4_SW_DELAY Delay value equals the the Hardware counter shifted by (4 + the offset value defines by software)

16.2.3.52 enum **EPWM_DigitalCompareEdgeFilterMode**

Values that can be passed to EPWM_setDigitalCompareEdgeFilterMode() as the *edgeMode* parameter.

Enumerator

EPWM_DC_EDGEFILT_MODE_RISING Digital Compare Edge filter low to high edge mode

EPWM_DC_EDGEFILT_MODE_FALLING Digital Compare Edge filter high to low edge mode

EPWM_DC_EDGEFILT_MODE_BOTH Digital Compare Edge filter both edges mode

16.2.3.53 enum **EPWM_DigitalCompareEdgeFilterEdgeCount**

Values that can be passed to EPWM_setDigitalCompareEdgeFilterEdgeCount() as the *edgeCount* parameter.

Enumerator

EPWM_DC_EDGEFILT_EDGECNT_0 Digital Compare Edge filter edge count = 0

EPWM_DC_EDGEFILT_EDGECNT_1 Digital Compare Edge filter edge count = 1
EPWM_DC_EDGEFILT_EDGECNT_2 Digital Compare Edge filter edge count = 2
EPWM_DC_EDGEFILT_EDGECNT_3 Digital Compare Edge filter edge count = 3
EPWM_DC_EDGEFILT_EDGECNT_4 Digital Compare Edge filter edge count = 4
EPWM_DC_EDGEFILT_EDGECNT_5 Digital Compare Edge filter edge count = 5
EPWM_DC_EDGEFILT_EDGECNT_6 Digital Compare Edge filter edge count = 6
EPWM_DC_EDGEFILT_EDGECNT_7 Digital Compare Edge filter edge count = 7

16.2.3.54 enum **EPWM_LockRegisterGroup**

Values that can be passed to EPWM_lockRegisters() as the *registerGroup* parameter.

Enumerator

EPWM_REGISTER_GROUP_GLOBAL_LOAD Global load register group.
EPWM_REGISTER_GROUP_TRIP_ZONE Trip zone register group.
EPWM_REGISTER_GROUP_TRIP_ZONE_CLEAR Trip zone clear group.
EPWM_REGISTER_GROUP_DIGITAL_COMPARE Digital compare group.

16.2.4 Function Documentation

16.2.4.1 static void EPWM_setTimeBaseCounter (uint32_t *base*, uint16_t *count*) [inline], [static]

Set the time base count

Parameters

base	is the base address of the EPWM module.
count	is the time base count value.

This function sets the 16 bit counter value of the time base counter.

Returns

None.

16.2.4.2 static void EPWM_setCountModeAfterSync (uint32_t *base*, **EPWM_SyncCountMode** *mode*) [inline], [static]

Set count mode after phase shift sync

Parameters

base	is the base address of the EPWM module.
mode	is the count mode.

This function sets the time base count to count up or down after a new phase value set by the EPWM_setPhaseShift(). The count direction is determined by the variable mode. Valid inputs for mode are:

- EPWM_COUNT_MODE_UP_AFTER_SYNC - Count up after sync

- EPWM_COUNT_MODE_DOWN_AFTER_SYNC - Count down after sync

Returns
None.

References EPWM_COUNT_MODE_UP_AFTER_SYNC.

16.2.4.3 static void EPWM_setClockPrescaler (uint32_t *base*, **EPWM_ClockDivider** *prescaler*, **EPWM_HSClockDivider** *highSpeedPrescaler*) [inline], [static]

Set the time base clock and the high speed time base clock count pre-scaler

Parameters

base	is the base address of the EPWM module.
prescaler	is the time base count pre scale value.
highSpeed-Prescaler	is the high speed time base count pre scale value.

This function sets the pre scaler(divider)value for the time base clock counter and the high speed time base clock counter. Valid values for pre-scaler and highSpeedPrescaler are EPWM_CLOCK_DIVIDER_X, where X is 1, 2, 4, 8, 16, 32, 64 or 128. The actual numerical values for these macros represent values 0, 1...7. The equation for the output clock is: TBCLK = EPWMCLK/(highSpeedPrescaler $*$ pre-scaler)

Note: EPWMCLK is a scaled version of SYSCLK. At reset EPWMCLK is half SYSCLK.

Returns
None.

16.2.4.4 static void EPWM_forceSyncPulse (uint32_t *base*) [inline], [static]

Force a software sync pulse

Parameters

base	is the base address of the EPWM module.

This function causes a single software initiated sync pulse. Make sure the appropriate mode is selected using EPWM_setupSyncOutputMode() before using this function.

Returns
None.

16.2.4.5 static void EPWM_setSyncOutPulseMode (uint32_t *base*, **EPWM_SyncOutPulseMode** *mode*) [inline], [static]

Set up the sync out pulse event

Parameters

base	is the base address of the EPWM module.
mode	is the sync out mode.

This function set the sync out pulse mode. Valid values for mode are:

- EPWM_SYNC_OUT_PULSE_ON_SOFTWARE - sync pulse is generated by software when EPWM_forceSyncPulse() function is called or by EPWMxSYNCI signal.
- EPWM_SYNC_OUT_PULSE_ON_COUNTER_ZERO - sync pulse is generated when time base counter equals zero.
- EPWM_SYNC_OUT_PULSE_ON_COUNTER_COMPARE_B - sync pulse is generated when time base counter equals compare B value.
- EPWM_SYNC_OUT_PULSE_ON_COUNTER_COMPARE_C - sync pulse is generated when time base counter equals compare C value.
- EPWM_SYNC_OUT_PULSE_ON_COUNTER_COMPARE_D - sync pulse is generated when time base counter equals compare D value.
- EPWM_SYNC_OUT_PULSE_DISABLED - sync pulse is disabled.

Returns

None.

References EPWM_SYNC_OUT_PULSE_DISABLED.

16.2.4.6 static void EPWM_setPeriodLoadMode (uint32_t *base*, **EPWM_PeriodLoadMode** *loadMode*) [inline], [static]

Set PWM period load mode.

Parameters

base	is the base address of the EPWM module.
loadMode	is the PWM period load mode.

This function sets the load mode for the PWM period. If loadMode is set to EPWM_PERIOD_SHADOW_LOAD, a write or read to the TBPRD (PWM Period count register) accesses the shadow register. If loadMode is set to EPWM_PERIOD_DIRECT_LOAD, a write or read to the TBPRD register accesses the register directly.

Returns

None.

References EPWM_PERIOD_SHADOW_LOAD.

16.2.4.7 static void EPWM_enablePhaseShiftLoad (uint32_t *base*) [inline], [static]

Enable phase shift load

Parameters

base	is the base address of the EPWM module.

This function enables loading of phase shift when the appropriate sync event occurs.

Returns
None.

16.2.4.8 static void EPWM_disablePhaseShiftLoad (uint32_t *base*) [inline], [static]

Disable phase shift load

Parameters

base	is the base address of the EPWM module.

This function disables loading of phase shift.

Returns
None.

16.2.4.9 static void EPWM_setTimeBaseCounterMode (uint32_t *base*, **EPWM_TimeBaseCountMode** *counterMode*) [inline], [static]

Set time base counter mode

Parameters

base	is the base address of the EPWM module.
counterMode	is the time base counter mode.

This function sets up the time base counter mode. Valid values for counterMode are:

- EPWM_COUNTER_MODE_UP - Up - count mode.
- EPWM_COUNTER_MODE_DOWN - Down - count mode.
- EPWM_COUNTER_MODE_UP_DOWN - Up - down - count mode.
- EPWM_COUNTER_MODE_STOP_FREEZE - Stop - Freeze counter.

Returns
None.

16.2.4.10 static void EPWM_selectPeriodLoadEvent (uint32_t *base*, **EPWM_PeriodShadowLoadMode** *shadowLoadMode*) [inline], [static]

Set shadow to active period load on sync mode

Parameters

base	is the base address of the EPWM module.
shadowLoad-Mode	is the shadow to active load mode.

This function sets up the shadow to active Period register load mode with respect to a sync event. Valid values for shadowLoadMode are:

- EPWM_SHADOW_LOAD_MODE_COUNTER_ZERO - shadow to active load occurs when time base counter reaches 0.
- EPWM_SHADOW_LOAD_MODE_COUNTER_SYNC - shadow to active load occurs when time base counter reaches 0 and a SYNC occurs.
- EPWM_SHADOW_LOAD_MODE_SYNC - shadow to active load occurs only when a SYNC occurs.

Returns

None.

16.2.4.11 static void EPWM_enableOneShotSync (uint32_t *base*) [inline], [static]

Enable one shot sync mode

Parameters

base	is the base address of the EPWM module.

This function enables one shot sync mode.

Returns

None.

16.2.4.12 static void EPWM_disableOneShotSync (uint32_t *base*) [inline], [static]

Disable one shot sync mode

Parameters

base	is the base address of the EPWM module.

This function disables one shot sync mode.

Returns

None.

16.2.4.13 static void EPWM_startOneShotSync (uint32_t *base*) [inline], [static]

Start one shot sync mode

Parameters

base	is the base address of the EPWM module.

This function propagates a one shot sync pulse.

Returns
None.

16.2.4.14 static uint16_t EPWM_getTimeBaseCounterValue (uint32_t *base*) [inline], [static]

Returns time base counter value.

Parameters

base	is the base address of the EPWM module.

This function returns the current value of the time base counter.

Returns
returns time base counter value

16.2.4.15 static bool EPWM_getTimeBaseCounterOverflowStatus (uint32_t *base*) [inline], [static]

Return time base counter maximum status.

Parameters

base	is the base address of the EPWM module.

This function returns the status of the time base max counter.

Returns
Returns true if the counter has reached 0xFFFF. Returns false if the counter hasn't reached 0xFFFF.

16.2.4.16 static void EPWM_clearTimeBaseCounterOverflowEvent (uint32_t *base*) [inline], [static]

Clear max time base counter event.

Parameters

base	is the base address of the EPWM module.

This function clears the max time base counter latch event. The latch event occurs when the time base counter reaches its maximum value of 0xFFFF.

Returns
None.

16.2.4.17 static bool EPWM_getSyncStatus (uint32_t *base*) `[inline]`, `[static]`

Return external sync signal status.

Parameters

base	is the base address of the EPWM module.

This function returns the external sync signal status.

Returns

Returns true if if an external sync signal event Returns false if there is no event.

16.2.4.18 static void EPWM_clearSyncEvent (uint32_t *base*) [inline], [static]

Clear external sync signal event.

Parameters

base	is the base address of the EPWM module.

This function clears the external sync signal latch event.

Returns

None.

16.2.4.19 static uint16_t EPWM_getTimeBaseCounterDirection (uint32_t *base*) [inline], [static]

Return time base counter direction.

Parameters

base	is the base address of the EPWM module.

This function returns the direction of the time base counter.

Returns

returns EPWM_TIME_BASE_STATUS_COUNT_UP if the counter is counting up or EPWM_TIME_BASE_STATUS_COUNT_DOWN if the counter is counting down.

16.2.4.20 static void EPWM_setPhaseShift (uint32_t *base,* uint16_t *phaseCount*) [inline], [static]

Sets the phase shift offset counter value.

Parameters

base	is the base address of the EPWM module.
phaseCount	is the phase shift count value.

This function sets the 16 bit time-base counter phase of the ePWM relative to the time-base that is supplying the synchronization input signal. Call the EPWM_enablePhaseShiftLoad() function to enable loading of the phaseCount phase shift value when a sync event occurs.

Returns

None.

16.2.4.21 static void EPWM_setTimeBasePeriod (uint32_t *base,* uint16_t *periodCount*) [inline], [static]

Sets the PWM period count.

Parameters

base	is the base address of the EPWM module.
periodCount	is period count value.

This function sets the period of the PWM count. The value of periodCount is the value written to the register. User should map the desired period or frequency of the waveform into the correct periodCount. Invoke the function EPWM_selectPeriodLoadEvent() with the appropriate parameter to set the load mode of the Period count. periodCount has a maximum valid value of 0xFFFF

Returns

None.

16.2.4.22 static uint16_t EPWM_getTimeBasePeriod (uint32_t *base*) [inline], [static]

Gets the PWM period count.

Parameters

base	is the base address of the EPWM module.

This function gets the period of the PWM count.

Returns

The period count value.

16.2.4.23 static void EPWM_setupEPWMLinks (uint32_t *base*, **EPWM_CurrentLink** *epwmLink*, **EPWM_LinkComponent** *linkComp*) [inline], [static]

Sets the EPWM links.

Parameters

base	is the base address of the EPWM module.
epwmLink	is the ePWM instance to link with.
linkComp	is the ePWM component to link.

This function links the component defined in linkComp in the current ePWM instance with the linkComp component of the ePWM instance defined by epwmLink. A change (a write) in the value of linkComp component of epwmLink instance, causes a change in the current ePWM linkComp component. For example if the current ePWM is ePWM3 and the values of epwmLink and linkComp are EPWM_LINK_WITH_EPWM_1 and EPWM_LINK_COMP_C respectively, then a write to COMPC register in ePWM1, will result in a simultaneous write to COMPC register in ePWM3. Valid values for epwmLink are:

- EPWM_LINK_WITH_EPWM_1 - link current ePWM with ePWM1
- EPWM_LINK_WITH_EPWM_2 - link current ePWM with ePWM2
- EPWM_LINK_WITH_EPWM_3 - link current ePWM with ePWM3
- EPWM_LINK_WITH_EPWM_4 - link current ePWM with ePWM4
- EPWM_LINK_WITH_EPWM_5 - link current ePWM with ePWM5
- EPWM_LINK_WITH_EPWM_6 - link current ePWM with ePWM6

- EPWM_LINK_WITH_EPWM_7 - link current ePWM with ePWM7
- EPWM_LINK_WITH_EPWM_8 - link current ePWM with ePWM8
- EPWM_LINK_WITH_EPWM_9 - link current ePWM with ePWM9
- EPWM_LINK_WITH_EPWM_10 - link current ePWM with ePWM10
- EPWM_LINK_WITH_EPWM_11 - link current ePWM with ePWM11
- EPWM_LINK_WITH_EPWM_12 - link current ePWM with ePWM12

Valid values for linkComp are:

- EPWM_LINK_TBPRD - link TBPRD:TBPRDHR registers
- EPWM_LINK_COMP_A - link COMPA registers
- EPWM_LINK_COMP_B - link COMPB registers
- EPWM_LINK_COMP_C - link COMPC registers
- EPWM_LINK_COMP_D - link COMPD registers
- EPWM_LINK_GLDCTL2 - link GLDCTL2 registers

Returns
None.

16.2.4.24 static void EPWM_setCounterCompareShadowLoadMode (uint32_t *base*, **EPWM_CounterCompareModule** *compModule*, **EPWM_CounterCompareLoadMode** *loadMode*) [inline], [static]

Sets up the Counter Compare shadow load mode

Parameters

base	is the base address of the EPWM module.
compModule	is the counter compare module.
loadMode	is the shadow to active load mode.

This function enables and sets up the counter compare shadow load mode. Valid values for the variables are:

- compModule
  - EPWM_COUNTER_COMPARE_A - counter compare A.
  - EPWM_COUNTER_COMPARE_B - counter compare B.
  - EPWM_COUNTER_COMPARE_C - counter compare C.
  - EPWM_COUNTER_COMPARE_D - counter compare D.
- loadMode
  - EPWM_COMP_LOAD_ON_CNTR_ZERO - load when counter equals zero
  - EPWM_COMP_LOAD_ON_CNTR_PERIOD - load when counter equals period
  - EPWM_COMP_LOAD_ON_CNTR_ZERO_PERIOD - load when counter equals zero or period
  - EPWM_COMP_LOAD_FREEZE - Freeze shadow to active load
  - EPWM_COMP_LOAD_ON_SYNC_CNTR_ZERO - load when counter equals zero
  - EPWM_COMP_LOAD_ON_SYNC_CNTR_PERIOD -load when counter equals period

- EPWM_COMP_LOAD_ON_SYNC_CNTR_ZERO_PERIOD - load when counter equals zero or period
- EPWM_COMP_LOAD_ON_SYNC_ONLY - load on sync only

Returns

None.

References EPWM_COUNTER_COMPARE_A, and EPWM_COUNTER_COMPARE_C.

16.2.4.25 static void EPWM_disableCounterCompareShadowLoadMode (uint32_t *base*, **EPWM_CounterCompareModule** *compModule*) [inline], [static]

Disable Counter Compare shadow load mode

Parameters

base	is the base address of the EPWM module.
compModule	is the counter compare module.

This function disables counter compare shadow load mode. Valid values for the variables are:

- compModule
  - EPWM_COUNTER_COMPARE_A - counter compare A.
  - EPWM_COUNTER_COMPARE_B - counter compare B.
  - EPWM_COUNTER_COMPARE_C - counter compare C.
  - EPWM_COUNTER_COMPARE_D - counter compare D.

Returns

None.

References EPWM_COUNTER_COMPARE_A, and EPWM_COUNTER_COMPARE_C.

16.2.4.26 static void EPWM_setCounterCompareValue (uint32_t *base*, **EPWM_CounterCompareModule** *compModule*, uint16_t *compCount*) [inline], [static]

Set counter compare values.

Parameters

base	is the base address of the EPWM module.
compModule	is the Counter Compare value module.
compCount	is the counter compare count value.

This function sets the counter compare value for counter compare registers. The maximum value for compCount is 0xFFFF. Valid values for compModule are:

- EPWM_COUNTER_COMPARE_A - counter compare A.
- EPWM_COUNTER_COMPARE_B - counter compare B.
- EPWM_COUNTER_COMPARE_C - counter compare C.
- EPWM_COUNTER_COMPARE_D - counter compare D.

Returns
None.

References EPWM_COUNTER_COMPARE_A, and EPWM_COUNTER_COMPARE_B.

16.2.4.27 static uint16_t EPWM_getCounterCompareValue (uint32_t *base*, **EPWM_CounterCompareModule** *compModule*) [inline], [static]

Get counter compare values.

Parameters

base	is the base address of the EPWM module.
compModule	is the Counter Compare value module.

This function gets the counter compare value for counter compare registers. Valid values for compModule are:

- EPWM_COUNTER_COMPARE_A - counter compare A.
- EPWM_COUNTER_COMPARE_B - counter compare B.
- EPWM_COUNTER_COMPARE_C - counter compare C.
- EPWM_COUNTER_COMPARE_D - counter compare D.

Returns
The counter compare count value.

References EPWM_COUNTER_COMPARE_A, and EPWM_COUNTER_COMPARE_B.

16.2.4.28 static bool EPWM_getCounterCompareShadowStatus (uint32_t *base*, **EPWM_CounterCompareModule** *compModule*) [inline], [static]

Return the counter compare shadow register full status.

Parameters

base	is the base address of the EPWM module.
compModule	is the Counter Compare value module.

This function returns the counter Compare shadow register full status flag. Valid values for compModule are:

- EPWM_COUNTER_COMPARE_A - counter compare A.
- EPWM_COUNTER_COMPARE_B - counter compare B.

Returns
Returns true if the shadow register is full. Returns false if the shadow register is not full.

16.2.4.29 static void EPWM_setActionQualifierShadowLoadMode (uint32_t *base*, **EPWM_ActionQualifierModule** *aqModule*, **EPWM_ActionQualifierLoadMode** *loadMode*) [inline], [static]

Sets the Action Qualifier shadow load mode

Parameters

base	is the base address of the EPWM module.
aqModule	is the Action Qualifier module value.
loadMode	is the shadow to active load mode.

This function enables and sets the Action Qualifier shadow load mode. Valid values for the variables are:

- aqModule
  - EPWM_ACTION_QUALIFIER_A - Action Qualifier A.
  - EPWM_ACTION_QUALIFIER_B - Action Qualifier B.
- loadMode
  - EPWM_AQ_LOAD_ON_CNTR_ZERO - load when counter equals zero
  - EPWM_AQ_LOAD_ON_CNTR_PERIOD - load when counter equals period
  - EPWM_AQ_LOAD_ON_CNTR_ZERO_PERIOD - load when counter equals zero or period
  - EPWM_AQ_LOAD_FREEZE - Freeze shadow to active load
  - EPWM_AQ_LOAD_ON_SYNC_CNTR_ZERO - load on sync or when counter equals zero
  - EPWM_AQ_LOAD_ON_SYNC_CNTR_PERIOD - load on sync or when counter equals period
  - EPWM_AQ_LOAD_ON_SYNC_CNTR_ZERO_PERIOD - load on sync or when counter equals zero or period
  - EPWM_AQ_LOAD_ON_SYNC_ONLY - load on sync only

Returns

None.

16.2.4.30 static void EPWM_disableActionQualifierShadowLoadMode (uint32_t *base*, **EPWM_ActionQualifierModule** *aqModule*) [inline], [static]

Disable Action Qualifier shadow load mode

Parameters

base	is the base address of the EPWM module.
aqModule	is the Action Qualifier module value.

This function disables the Action Qualifier shadow load mode. Valid values for the variables are:

- aqModule
  - EPWM_ACTION_QUALIFIER_A - Action Qualifier A.
  - EPWM_ACTION_QUALIFIER_B - Action Qualifier B.

Returns

None.

16.2.4.31 static void EPWM_setActionQualifierT1TriggerSource (uint32_t *base*, **EPWM_ActionQualifierTriggerSource** *trigger*) [inline], [static]

Set up Action qualifier trigger source for event T1

Parameters

base	is the base address of the EPWM module.
trigger	sources for Action Qualifier triggers.

This function sets up the sources for Action Qualifier event T1. Valid values for trigger are:

- EPWM_AQ_TRIGGER_EVENT_TRIG_DCA_1 - Digital compare event A 1
- EPWM_AQ_TRIGGER_EVENT_TRIG_DCA_2 - Digital compare event A 2
- EPWM_AQ_TRIGGER_EVENT_TRIG_DCB_1 - Digital compare event B 1
- EPWM_AQ_TRIGGER_EVENT_TRIG_DCB_2 - Digital compare event B 2
- EPWM_AQ_TRIGGER_EVENT_TRIG_TZ_1 - Trip zone 1
- EPWM_AQ_TRIGGER_EVENT_TRIG_TZ_2 - Trip zone 2
- EPWM_AQ_TRIGGER_EVENT_TRIG_TZ_3 - Trip zone 3
- EPWM_AQ_TRIGGER_EVENT_TRIG_EPWM_SYNCIN - ePWM sync

Returns

None.

16.2.4.32 static void EPWM_setActionQualifierT2TriggerSource (uint32_t *base*, **EPWM_ActionQualifierTriggerSource** *trigger*) [inline], [static]

Set up Action qualifier trigger source for event T2

Parameters

base	is the base address of the EPWM module.
trigger	sources for Action Qualifier triggers.

This function sets up the sources for Action Qualifier event T2. Valid values for trigger are:

- EPWM_AQ_TRIGGER_EVENT_TRIG_DCA_1 - Digital compare event A 1
- EPWM_AQ_TRIGGER_EVENT_TRIG_DCA_2 - Digital compare event A 2
- EPWM_AQ_TRIGGER_EVENT_TRIG_DCB_1 - Digital compare event B 1
- EPWM_AQ_TRIGGER_EVENT_TRIG_DCB_2 - Digital compare event B 2
- EPWM_AQ_TRIGGER_EVENT_TRIG_TZ_1 - Trip zone 1
- EPWM_AQ_TRIGGER_EVENT_TRIG_TZ_2 - Trip zone 2
- EPWM_AQ_TRIGGER_EVENT_TRIG_TZ_3 - Trip zone 3
- EPWM_AQ_TRIGGER_EVENT_TRIG_EPWM_SYNCIN - ePWM sync

Returns

None.

16.2.4.33 static void EPWM_setActionQualifierAction (uint32_t *base*, **EPWM_ActionQualifierOutputModule** *epwmOutput*, **EPWM_ActionQualifierOutput** *output*, **EPWM_ActionQualifierOutputEvent** *event*) [inline], [static]

Set up Action qualifier outputs

Parameters

base	is the base address of the EPWM module.
epwmOutput	is the ePWM pin type.
output	is the Action Qualifier output.
event	is the event that causes a change in output.

This function sets up the Action Qualifier output on ePWM A or ePWMB, depending on the value of epwmOutput, to a value specified by outPut based on the input events - specified by event. The following are valid values for the parameters.

- epwmOutput
  - EPWM_AQ_OUTPUT_A - ePWMxA output
  - EPWM_AQ_OUTPUT_B - ePWMxB output
- output
  - EPWM_AQ_OUTPUT_NO_CHANGE - No change in the output pins
  - EPWM_AQ_OUTPUT_LOW - Set output pins to low
  - EPWM_AQ_OUTPUT_HIGH - Set output pins to High
  - EPWM_AQ_OUTPUT_TOGGLE - Toggle the output pins
- event
  - EPWM_AQ_OUTPUT_ON_TIMEBASE_ZERO - Time base counter equals zero
  - EPWM_AQ_OUTPUT_ON_TIMEBASE_PERIOD - Time base counter equals period
  - EPWM_AQ_OUTPUT_ON_TIMEBASE_UP_CMPA - Time base counter up equals COMPA
  - EPWM_AQ_OUTPUT_ON_TIMEBASE_DOWN_CMPA - Time base counter down equals COMPA
  - EPWM_AQ_OUTPUT_ON_TIMEBASE_UP_CMPB - Time base counter up equals COMPB
  - EPWM_AQ_OUTPUT_ON_TIMEBASE_DOWN_CMPB - Time base counter down equals COMPB
  - EPWM_AQ_OUTPUT_ON_T1_COUNT_UP - T1 event on count up
  - EPWM_AQ_OUTPUT_ON_T1_COUNT_DOWN - T1 event on count down
  - EPWM_AQ_OUTPUT_ON_T2_COUNT_UP - T2 event on count up
  - EPWM_AQ_OUTPUT_ON_T2_COUNT_DOWN - T2 event on count down

Returns

None.

16.2.4.34 static void EPWM_setActionQualifierActionComplete (uint32_t *base*, **EPWM_ActionQualifierOutputModule** *epwmOutput*, **EPWM_ActionQualifierEventAction** *action*) [inline], [static]

Set up Action qualifier event outputs

Parameters

base	is the base address of the EPWM module.
epwmOutput	is the ePWM pin type.
action	is the desired action when the specified event occurs

This function sets up the Action Qualifier output on ePWMA or ePWMB, depending on the value of epwmOutput, to a value specified by action The following are valid values for the parameters.

- epwmOutput
  - EPWM_AQ_OUTPUT_A - ePWMxA output
  - EPWM_AQ_OUTPUT_B - ePWMxB output
- action
  - EPWM_AQ_OUTPUT_NO_CHANGE_ZERO - Time base counter equals zero and no change in output pins
  - EPWM_AQ_OUTPUT_LOW_ZERO - Time base counter equals zero and set output pins to low
  - EPWM_AQ_OUTPUT_HIGH_ZERO - Time base counter equals zero and set output pins to high
  - EPWM_AQ_OUTPUT_TOGGLE_ZERO - Time base counter equals zero and toggle the output pins
  - EPWM_AQ_OUTPUT_NO_CHANGE_PERIOD - Time base counter equals period and no change in output pins
  - EPWM_AQ_OUTPUT_LOW_PERIOD - Time base counter equals period and set output pins to low
  - EPWM_AQ_OUTPUT_HIGH_PERIOD - Time base counter equals period and set output pins to high
  - EPWM_AQ_OUTPUT_TOGGLE_PERIOD - Time base counter equals period and toggle the output pins
  - EPWM_AQ_OUTPUT_NO_CHANGE_UP_CMPA - Time base counter up equals COMPA and no change in the output pins
  - EPWM_AQ_OUTPUT_LOW_UP_CMPA - Time base counter up equals COMPA and set output pins low
  - EPWM_AQ_OUTPUT_HIGH_UP_CMPA - Time base counter up equals COMPA and set output pins high
  - EPWM_AQ_OUTPUT_TOGGLE_UP_CMPA - Time base counter up equals COMPA and toggle output pins
  - EPWM_AQ_OUTPUT_NO_CHANGE_DOWN_CMPA- Time base counter down equals COMPA and no change in the output pins
  - EPWM_AQ_OUTPUT_LOW_DOWN_CMPA - Time base counter down equals COMPA and set output pins low
  - EPWM_AQ_OUTPUT_HIGH_DOWN_CMPA - Time base counter down equals COMPA and set output pins high
  - EPWM_AQ_OUTPUT_TOGGLE_DOWN_CMPA - Time base counter down equals COMPA and toggle output pins
  - EPWM_AQ_OUTPUT_NO_CHANGE_UP_CMPB - Time base counter up equals COMPB and no change in the output pins
  - EPWM_AQ_OUTPUT_LOW_UP_CMPB - Time base counter up equals COMPB and set output pins low

- EPWM_AQ_OUTPUT_HIGH_UP_CMPB - Time base counter up equals COMPB and set output pins high
- EPWM_AQ_OUTPUT_TOGGLE_UP_CMPB - Time base counter up equals COMPB and toggle output pins
- EPWM_AQ_OUTPUT_NO_CHANGE_DOWN_CMPB- Time base counter down equals COMPB and no change in the output pins
- EPWM_AQ_OUTPUT_LOW_DOWN_CMPB - Time base counter down equals COMPB and set output pins low
- EPWM_AQ_OUTPUT_HIGH_DOWN_CMPB - Time base counter down equals COMPB and set output pins high
- EPWM_AQ_OUTPUT_TOGGLE_DOWN_CMPB - Time base counter down equals COMPB and toggle output pins

Returns
None.

16.2.4.35 static void EPWM_setAdditionalActionQualifierActionComplete (uint32_t *base*, **EPWM_ActionQualifierOutputModule** *epwmOutput*, **EPWM_AdditionalActionQualifierEventAction** *action*) [inline], [static]

Set up Additional action qualifier event outputs

Parameters

base	is the base address of the EPWM module.
epwmOutput	is the ePWM pin type.
action	is the desired action when the specified event occurs

This function sets up the Additional Action Qualifier output on ePWMA or ePWMB depending on the value of epwmOutput, to a value specified by action The following are valid values for the parameters.

- epwmOutput
  - EPWM_AQ_OUTPUT_A - ePWMxA output
  - EPWM_AQ_OUTPUT_B - ePWMxB output
- action
  - EPWM_AQ_OUTPUT_NO_CHANGE_UP_TI - T1 event on count up and no change in output pins
  - EPWM_AQ_OUTPUT_LOW_UP_TI - T1 event on count up and set output pins to low
  - EPWM_AQ_OUTPUT_HIGH_UP_TI - T1 event on count up and set output pins to high
  - EPWM_AQ_OUTPUT_TOGGLE_UP_TI - T1 event on count up and toggle the output pins
  - EPWM_AQ_OUTPUT_NO_CHANGE_DOWN_TI- T1 event on count down and no change in output pins
  - EPWM_AQ_OUTPUT_LOW_DOWN_TI - T1 event on count down and set output pins to low
  - EPWM_AQ_OUTPUT_HIGH_DOWN_TI - T1 event on count down and set output pins to high

- EPWM_AQ_OUTPUT_TOGGLE_DOWN_TI - T1 event on count down and toggle the output pins
- EPWM_AQ_OUTPUT_NO_CHANGE_UP_T2 - T2 event on count up and no change in output pins
- EPWM_AQ_OUTPUT_LOW_UP_T2 - T2 event on count up and set output pins to low
- EPWM_AQ_OUTPUT_HIGH_UP_T2 - T2 event on count up and set output pins to high
- EPWM_AQ_OUTPUT_TOGGLE_UP_T2 - T2 event on count up and toggle the output pins
- EPWM_AQ_OUTPUT_NO_CHANGE_DOWN_T2- T2 event on count down and no change in output pins
- EPWM_AQ_OUTPUT_LOW_DOWN_T2 - T2 event on count down and set output pins to low
- EPWM_AQ_OUTPUT_HIGH_DOWN_T2 - T2 event on count down and set output pins to high
- EPWM_AQ_OUTPUT_TOGGLE_DOWN_T2 - T2 event on count down and toggle the output pins

Returns

None.

16.2.4.36 static void EPWM_setActionQualifierContSWForceShadowMode (uint32_t *base*, **EPWM_ActionQualifierContForce** *mode*) [inline], [static]

Sets up Action qualifier continuous software load mode.

Parameters

base	is the base address of the EPWM module.
mode	is the mode for shadow to active load mode.

This function sets up the AQCFRSC register load mode for continuous software force reload mode. The software force actions are determined by the EPWM_setActionQualifierContSWForceAction() function. Valid values for mode are:

- EPWM_AQ_SW_SH_LOAD_ON_CNTR_ZERO - shadow mode load when counter equals zero
- EPWM_AQ_SW_SH_LOAD_ON_CNTR_PERIOD - shadow mode load when counter equals period
- EPWM_AQ_SW_SH_LOAD_ON_CNTR_ZERO_PERIOD - shadow mode load when counter equals zero or period
- EPWM_AQ_SW_IMMEDIATE_LOAD - immediate mode load only

Returns

None.

16.2.4.37 static void EPWM_setActionQualifierContSWForceAction (uint32_t *base*, **EPWM_ActionQualifierOutputModule** *epwmOutput*, **EPWM_ActionQualifierSWOutput** *output*) [inline], [static]

Triggers a continuous software forced event.

Parameters

base	is the base address of the EPWM module.
epwmOutput	is the ePWM pin type.
output	is the Action Qualifier output.

This function triggers a continuous software forced Action Qualifier output on ePWM A or B based on the value of epwmOutput. Valid values for the parameters are:

- epwmOutput
  - EPWM_AQ_OUTPUT_A - ePWMxA output
  - EPWM_AQ_OUTPUT_B - ePWMxB output
- output
  - EPWM_AQ_SW_DISABLED - Software forcing disabled.
  - EPWM_AQ_OUTPUT_LOW - Set output pins to low
  - EPWM_AQ_OUTPUT_HIGH - Set output pins to High

Returns

None.

References EPWM_AQ_OUTPUT_A.

16.2.4.38 static void EPWM_setActionQualifierSWAction (uint32_t *base*, **EPWM_ActionQualifierOutputModule** *epwmOutput*, **EPWM_ActionQualifierOutput** *output*) [inline], [static]

Set up one time software forced Action qualifier outputs

Parameters

base	is the base address of the EPWM module.
epwmOutput	is the ePWM pin type.
output	is the Action Qualifier output.

This function sets up the one time software forced Action Qualifier output on ePWM A or ePWMB, depending on the value of epwmOutput to a value specified by outPut. The following are valid values for the parameters.

- epwmOutput
  - EPWM_AQ_OUTPUT_A - ePWMxA output
  - EPWM_AQ_OUTPUT_B - ePWMxB output
- output
  - EPWM_AQ_OUTPUT_NO_CHANGE - No change in the output pins
  - EPWM_AQ_OUTPUT_LOW - Set output pins to low
  - EPWM_AQ_OUTPUT_HIGH - Set output pins to High
  - EPWM_AQ_OUTPUT_TOGGLE - Toggle the output pins

Returns

None.

References EPWM_AQ_OUTPUT_A.

16.2.4.39 static void EPWM_forceActionQualifierSWAction (uint32_t *base*, **EPWM_ActionQualifierOutputModule** *epwmOutput*) [inline], [static]

Triggers a one time software forced event on Action qualifier

Parameters

base	is the base address of the EPWM module.
epwmOutput	is the ePWM pin type.

This function triggers a one time software forced Action Qualifier event on ePWM A or B based on the value of epwmOutput. Valid values for epwmOutput are:

- EPWM_AQ_OUTPUT_A - ePWMxA output
- EPWM_AQ_OUTPUT_B - ePWMxB output

Returns

None.

References EPWM_AQ_OUTPUT_A.

16.2.4.40 static void EPWM_setDeadBandOutputSwapMode (uint32_t *base*, **EPWM_DeadBandOutput** *output*, bool *enableSwapMode*) [inline], [static]

Sets Dead Band signal output swap mode.

Parameters

base	is the base address of the EPWM module.
output	is the ePWM Dead Band output.
enableSwap-Mode	is the output swap mode.

This function sets up the output signal swap mode. For example if the output variable is set to EPWM_DB_OUTPUT_A and enableSwapMode is true, then the ePWM A output gets its signal from the ePWM B signal path. Valid values for the input variables are:

- output
  - EPWM_DB_OUTPUT_A - ePWM output A
  - EPWM_DB_OUTPUT_B - ePWM output B
- enableSwapMode
  - true - the output is swapped
  - false - the output and the signal path are the same.

Returns

None.

16.2.4.41 static void EPWM_setDeadBandDelayMode (uint32_t *base*, **EPWM_DeadBandDelayMode** *delayMode*, bool *enableDelayMode*) [inline], [static]

Sets Dead Band signal output mode.

Parameters

base	is the base address of the EPWM module.
delayMode	is the Dead Band delay type.
enableDelayMode	is the dead band delay mode.

This function sets up the dead band delay mode. The delayMode variable determines if the applied delay is Rising Edge or Falling Edge. The enableDelayMode determines if a dead band delay should be applied. Valid values for the variables are:

- delayMode
  - EPWM_DB_RED - Rising Edge delay
  - EPWM_DB_FED - Falling Edge delay
- enableDelayMode
  - true - Falling edge or Rising edge delay is applied.
  - false - Dead Band delay is bypassed.

Returns

None.

16.2.4.42 static void EPWM_setDeadBandDelayPolarity (uint32_t *base*, **EPWM_DeadBandDelayMode** *delayMode*, **EPWM_DeadBandPolarity** *polarity*) [inline], [static]

Sets Dead Band delay polarity.

Parameters

base	is the base address of the EPWM module.
delayMode	is the Dead Band delay type.
polarity	is the polarity of the delayed signal.

This function sets up the polarity as determined by the variable polarity of the Falling Edge or Rising Edge delay depending on the value of delayMode. Valid values for the variables are:

- delayMode
  - EPWM_DB_RED - Rising Edge delay
  - EPWM_DB_FED - Falling Edge delay
- polarity
  - EPWM_DB_POLARITY_ACTIVE_HIGH - polarity is not inverted.
  - EPWM_DB_POLARITY_ACTIVE_LOW - polarity is inverted.

Returns

None.

16.2.4.43 static void EPWM_setRisingEdgeDeadBandDelayInput (uint32_t *base*, uint16_t *input*) [inline], [static]

Sets Rising Edge Dead Band delay input.

Parameters

base	is the base address of the EPWM module.
input	is the input signal to the dead band.

This function sets up the rising Edge delay input signal. Valid values for input are:

- EPWM_DB_INPUT_EPWMA - Input signal is ePWMA(Valid for both Falling Edge and Rising Edge)
- EPWM_DB_INPUT_EPWMB - Input signal is ePWMB(Valid for both Falling Edge and Rising Edge)

Returns
None.

References EPWM_DB_INPUT_EPWMA, and EPWM_DB_INPUT_EPWMB.

16.2.4.44 static void EPWM_setFallingEdgeDeadBandDelayInput (uint32_t *base,* uint16_t *input*) [inline], [static]

Sets Dead Band delay input.

Parameters

base	is the base address of the EPWM module.
input	is the input signal to the dead band.

This function sets up the rising Edge delay input signal. Valid values for input are:

- EPWM_DB_INPUT_EPWMA - Input signal is ePWMA(Valid for both Falling Edge and Rising Edge)
- EPWM_DB_INPUT_EPWMB - Input signal is ePWMB(Valid for both Falling Edge and Rising Edge)
- EPWM_DB_INPUT_DB_RED - Input signal is the output of Rising Edge delay. (Valid only for Falling Edge delay)

Returns
None.

References EPWM_DB_INPUT_DB_RED, EPWM_DB_INPUT_EPWMA, and EPWM_DB_INPUT_EPWMB.

16.2.4.45 static void EPWM_setDeadBandControlShadowLoadMode (uint32_t *base,* **EPWM_DeadBandControlLoadMode** *loadMode*) [inline], [static]

Set the Dead Band control shadow load mode.

Parameters

base	is the base address of the EPWM module.
loadMode	is the shadow to active load mode.

This function enables and sets the Dead Band control register shadow load mode. Valid values for the *loadMode* parameter are:

- EPWM_DB_LOAD_ON_CNTR_ZERO - load when counter equals zero.
- EPWM_DB_LOAD_ON_CNTR_PERIOD - load when counter equals period.
- EPWM_DB_LOAD_ON_CNTR_ZERO_PERIOD - load when counter equals zero or period.
- EPWM_DB_LOAD_FREEZE - Freeze shadow to active load.

Returns
None.

16.2.4.46 static void EPWM_disableDeadBandControlShadowLoadMode (uint32_t *base*) [inline], [static]

Disable Dead Band control shadow load mode.

Parameters

base	is the base address of the EPWM module.

This function disables the Dead Band control register shadow load mode.

Returns
None.

16.2.4.47 static void EPWM_setRisingEdgeDelayCountShadowLoadMode (uint32_t *base*, **EPWM_RisingEdgeDelayLoadMode** *loadMode*) [inline], [static]

Set the RED (Rising Edge Delay) shadow load mode.

Parameters

base	is the base address of the EPWM module.
loadMode	is the shadow to active load event.

This function sets the Rising Edge Delay register shadow load mode. Valid values for the *loadMode* parameter are:

- EPWM_RED_LOAD_ON_CNTR_ZERO - load when counter equals zero.
- EPWM_RED_LOAD_ON_CNTR_PERIOD - load when counter equals period.
- EPWM_RED_LOAD_ON_CNTR_ZERO_PERIOD - load when counter equals zero or period.
- EPWM_RED_LOAD_FREEZE - Freeze shadow to active load.

Returns
None.

16.2.4.48 static void EPWM_disableRisingEdgeDelayCountShadowLoadMode (uint32_t *base*) [inline], [static]

Disable the RED (Rising Edge Delay) shadow load mode.

Parameters

base	is the base address of the EPWM module.

This function disables the Rising Edge Delay register shadow load mode.

Returns

None.

16.2.4.49 static void EPWM_setFallingEdgeDelayCountShadowLoadMode (uint32_t *base*, **EPWM_FallingEdgeDelayLoadMode** *loadMode*) [inline], [static]

Set the FED (Falling Edge Delay) shadow load mode.

Parameters

base	is the base address of the EPWM module.
loadMode	is the shadow to active load event.

This function enables and sets the Falling Edge Delay register shadow load mode. Valid values for the *loadMode* parameters are:

- EPWM_FED_LOAD_ON_CNTR_ZERO - load when counter equals zero.
- EPWM_FED_LOAD_ON_CNTR_PERIOD - load when counter equals period.
- EPWM_FED_LOAD_ON_CNTR_ZERO_PERIOD - load when counter equals zero or period.
- EPWM_FED_LOAD_FREEZE - Freeze shadow to active load.

Returns

None.

16.2.4.50 static void EPWM_disableFallingEdgeDelayCountShadowLoadMode (uint32_t *base*) [inline], [static]

Disables the FED (Falling Edge Delay) shadow load mode.

Parameters

base	is the base address of the EPWM module.

This function disables the Falling Edge Delay register shadow load mode. Valid values for the parameters are:

Returns

None.

16.2.4.51 static void EPWM_setDeadBandCounterClock (uint32_t *base*, **EPWM_DeadBandClockMode** *clockMode*) [inline], [static]

Sets Dead Band Counter clock rate.

Parameters

base	is the base address of the EPWM module.
clockMode	is the Dead Band counter clock mode.

This function sets up the Dead Band counter clock rate with respect to TBCLK (ePWM time base counter). Valid values for clockMode are:

- EPWM_DB_COUNTER_CLOCK_FULL_CYCLE -Dead band counter runs at TBCLK (ePWM Time Base Counter) rate.
- EPWM_DB_COUNTER_CLOCK_HALF_CYCLE -Dead band counter runs at 2∗TBCLK (twice ePWM Time Base Counter)rate.

Returns
None.

16.2.4.52 static void EPWM_setRisingEdgeDelayCount (uint32_t *base,* uint16_t *redCount*) [inline], [static]

Set ePWM RED count

Parameters

base	is the base address of the EPWM module.
redCount	is the RED(Rising Edge Delay) count.

This function sets the RED (Rising Edge Delay) count value. The value of redCount should be less than 0x4000U.

Returns
None.

16.2.4.53 static void EPWM_setFallingEdgeDelayCount (uint32_t *base,* uint16_t *fedCount*) [inline], [static]

Set ePWM FED count

Parameters

base	is the base address of the EPWM module.
fedCount	is the FED(Falling Edge Delay) count.

This function sets the FED (Falling Edge Delay) count value. The value of fedCount should be less than 0x4000U.

Returns
None.

16.2.4.54 static void EPWM_enableChopper (uint32_t *base*) [inline], [static]

Enable chopper mode

Parameters

base	is the base address of the EPWM module.

This function enables ePWM chopper module.

Returns
None.

16.2.4.55 static void EPWM_disableChopper (uint32_t *base*) [inline], [static]

Disable chopper mode

Parameters

base	is the base address of the EPWM module.

This function disables ePWM chopper module.

Returns
None.

16.2.4.56 static void EPWM_setChopperDutyCycle (uint32_t *base*, uint16_t *dutyCycleCount*) [inline], [static]

Set chopper duty cycle.

Parameters

base	is the base address of the EPWM module.
dutyCycleCount	is the chopping clock duty cycle count.

This function sets the chopping clock duty cycle. The value of dutyCycleCount should be less than 7. The dutyCycleCount value is converted to the actual chopper duty cycle value base on the following equation: chopper duty cycle = (dutyCycleCount + 1) / 8

Returns
None.

16.2.4.57 static void EPWM_setChopperFreq (uint32_t *base*, uint16_t *freqDiv*) [inline], [static]

Set chopper clock frequency scaler.

Parameters

base	is the base address of the EPWM module.
freqDiv	is the chopping clock frequency divider.

This function sets the scaler for the chopping clock frequency. The value of freqDiv should be less than 8. The chopping clock frequency is altered based on the following equation. chopper clock frequency = SYSCLKOUT / (1 + freqDiv)

Returns
None.

16.2.4.58 static void EPWM_setChopperFirstPulseWidth (uint32_t *base,* uint16_t *firstPulseWidth*) [inline], [static]

Set chopper clock frequency scaler.

Parameters

base	is the base address of the EPWM module.
firstPulseWidth	is the width of the first pulse.

This function sets the first pulse width of chopper output waveform. The value of firstPulseWidth should be less than 0x10. The value of the first pulse width in seconds is given using the following equation: first pulse width = 1 / (((firstPulseWidth + 1) $*$ SYSCLKOUT)/8)

Returns
None.

16.2.4.59 static void EPWM_enableTripZoneSignals (uint32_t *base,* uint16_t *tzSignal*) [inline], [static]

Enables Trip Zone signal.

Parameters

base	is the base address of the EPWM module.
tzSignal	is the Trip Zone signal.

This function enables the Trip Zone signals specified by tzSignal as a source for the Trip Zone module. Valid values for tzSignal are:

- EPWM_TZ_SIGNAL_CBC1 - TZ1 Cycle By Cycle
- EPWM_TZ_SIGNAL_CBC2 - TZ2 Cycle By Cycle
- EPWM_TZ_SIGNAL_CBC3 - TZ3 Cycle By Cycle
- EPWM_TZ_SIGNAL_CBC4 - TZ4 Cycle By Cycle
- EPWM_TZ_SIGNAL_CBC5 - TZ5 Cycle By Cycle
- EPWM_TZ_SIGNAL_CBC6 - TZ6 Cycle By Cycle
- EPWM_TZ_SIGNAL_DCAEVT2 - DCAEVT2 Cycle By Cycle
- EPWM_TZ_SIGNAL_DCBEVT2 - DCBEVT2 Cycle By Cycle
- EPWM_TZ_SIGNAL_OSHT1 - One-shot TZ1
- EPWM_TZ_SIGNAL_OSHT2 - One-shot TZ2
- EPWM_TZ_SIGNAL_OSHT3 - One-shot TZ3
- EPWM_TZ_SIGNAL_OSHT4 - One-shot TZ4
- EPWM_TZ_SIGNAL_OSHT5 - One-shot TZ5
- EPWM_TZ_SIGNAL_OSHT6 - One-shot TZ6
- EPWM_TZ_SIGNAL_DCAEVT1 - One-shot DCAEVT1

- EPWM_TZ_SIGNAL_DCBEVT1 - One-shot DCBEVT1

note: A logical OR of the valid values can be passed as the tzSignal parameter.

Returns
None.

16.2.4.60 static void EPWM_disableTripZoneSignals (uint32_t *base,* uint16_t *tzSignal*) [inline], [static]

Disables Trip Zone signal.

Parameters

base	is the base address of the EPWM module.
tzSignal	is the Trip Zone signal.

This function disables the Trip Zone signal specified by tzSignal as a source for the Trip Zone module. Valid values for tzSignal are:

- EPWM_TZ_SIGNAL_CBC1 - TZ1 Cycle By Cycle
- EPWM_TZ_SIGNAL_CBC2 - TZ2 Cycle By Cycle
- EPWM_TZ_SIGNAL_CBC3 - TZ3 Cycle By Cycle
- EPWM_TZ_SIGNAL_CBC4 - TZ4 Cycle By Cycle
- EPWM_TZ_SIGNAL_CBC5 - TZ5 Cycle By Cycle
- EPWM_TZ_SIGNAL_CBC6 - TZ6 Cycle By Cycle
- EPWM_TZ_SIGNAL_DCAEVT2 - DCAEVT2 Cycle By Cycle
- EPWM_TZ_SIGNAL_DCBEVT2 - DCBEVT2 Cycle By Cycle
- EPWM_TZ_SIGNAL_OSHT1 - One-shot TZ1
- EPWM_TZ_SIGNAL_OSHT2 - One-shot TZ2
- EPWM_TZ_SIGNAL_OSHT3 - One-shot TZ3
- EPWM_TZ_SIGNAL_OSHT4 - One-shot TZ4
- EPWM_TZ_SIGNAL_OSHT5 - One-shot TZ5
- EPWM_TZ_SIGNAL_OSHT6 - One-shot TZ6
- EPWM_TZ_SIGNAL_DCAEVT1 - One-shot DCAEVT1
- EPWM_TZ_SIGNAL_DCBEVT1 - One-shot DCBEVT1

note: A logical OR of the valid values can be passed as the tzSignal parameter.

Returns
None.

16.2.4.61 static void EPWM_setTripZoneDigitalCompareEventCondition (uint32_t *base,* **EPWM_TripZoneDigitalCompareOutput** *dcType,* **EPWM_TripZoneDigitalCompareOutputEvent** *dcEvent*) [inline], [static]

Set Digital compare conditions that cause Trip Zone event.

Parameters

base	is the base address of the EPWM module.
dcType	is the Digital compare output type.
dcEvent	is the Digital Compare output event.

This function sets up the Digital Compare output Trip Zone event sources. The dcType variable specifies the event source to be whether Digital Compare output A or Digital Compare output B. The dcEvent parameter specifies the event that causes Trip Zone. Valid values for the parameters are:

- dcType
  - EPWM_TZ_DC_OUTPUT_A1 - Digital Compare output 1 A
  - EPWM_TZ_DC_OUTPUT_A2 - Digital Compare output 2 A
  - EPWM_TZ_DC_OUTPUT_B1 - Digital Compare output 1 B
  - EPWM_TZ_DC_OUTPUT_B2 - Digital Compare output 2 B
- dcEvent
  - EPWM_TZ_EVENT_DC_DISABLED - Event Trigger is disabled
  - EPWM_TZ_EVENT_DCXH_LOW - Trigger event when DCxH low
  - EPWM_TZ_EVENT_DCXH_HIGH - Trigger event when DCxH high
  - EPWM_TZ_EVENT_DCXL_LOW - Trigger event when DCxL low
  - EPWM_TZ_EVENT_DCXL_HIGH - Trigger event when DCxL high
  - EPWM_TZ_EVENT_DCXL_HIGH_DCXH_LOW - Trigger event when DCxL high DCxH low

Note

x in DCxH/DCxL represents DCAH/DCAL or DCBH/DCBL

Returns

None.

16.2.4.62 static void EPWM_enableTripZoneAdvAction (uint32_t *base*) `[inline]`, `[static]`

Enable advanced Trip Zone event Action.

Parameters

base	is the base address of the EPWM module.

This function enables the advanced actions of the Trip Zone events. The advanced features combine the trip zone events with the direction of the counter.

Returns

None.

16.2.4.63 static void EPWM_disableTripZoneAdvAction (uint32_t *base*) `[inline]`, `[static]`

Disable advanced Trip Zone event Action.

Parameters

base	is the base address of the EPWM module.

This function disables the advanced actions of the Trip Zone events.

Returns

None.

16.2.4.64 static void EPWM_setTripZoneAction (uint32_t *base*, **EPWM_TripZoneEvent** *tzEvent*, **EPWM_TripZoneAction** *tzAction*) [inline], [static]

Set Trip Zone Action.

Parameters

base	is the base address of the EPWM module.
tzEvent	is the Trip Zone event type.
tzAction	is the Trip zone Action.

This function sets the Trip Zone Action to be taken when a Trip Zone event occurs. Valid values for the parameters are:

- tzEvent
  - EPWM_TZ_ACTION_EVENT_DCBEVT2 - DCBEVT2 (Digital Compare B event 2)
  - EPWM_TZ_ACTION_EVENT_DCBEVT1 - DCBEVT1 (Digital Compare B event 1)
  - EPWM_TZ_ACTION_EVENT_DCAEVT2 - DCAEVT2 (Digital Compare A event 2)
  - EPWM_TZ_ACTION_EVENT_DCAEVT1 - DCAEVT1 (Digital Compare A event 1)
  - EPWM_TZ_ACTION_EVENT_TZB - TZ1 - TZ6, DCBEVT2, DCBEVT1
  - EPWM_TZ_ACTION_EVENT_TZA - TZ1 - TZ6, DCAEVT2, DCAEVT1
- tzAction
  - EPWM_TZ_ACTION_HIGH_Z - high impedance output
  - EPWM_TZ_ACTION_HIGH - high output
  - EPWM_TZ_ACTION_LOW - low low
  - EPWM_TZ_ACTION_DISABLE - disable action

Note

Disable the advanced Trip Zone event using EPWM_disableTripZoneAdvAction() before calling this function.
This function operates on both ePWMA and ePWMB depending on the tzEvent parameter.

Returns

None.

16.2.4.65 static void EPWM_setTripZoneAdvAction (uint32_t *base*, **EPWM_TripZoneAdvancedEvent** *tzAdvEvent*, **EPWM_TripZoneAdvancedAction** *tzAdvAction*) [inline], [static]

Set Advanced Trip Zone Action.

Parameters

base	is the base address of the EPWM module.
tzAdvEvent	is the Trip Zone event type.
tzAdvAction	is the Trip zone Action.

This function sets the Advanced Trip Zone Action to be taken when an advanced Trip Zone event occurs.

Valid values for the parameters are:

- tzAdvEvent
  - EPWM_TZ_ADV_ACTION_EVENT_TZB_D - TZ1 - TZ6, DCBEVT2, DCBEVT1 while counting down
  - EPWM_TZ_ADV_ACTION_EVENT_TZB_U - TZ1 - TZ6, DCBEVT2, DCBEVT1 while counting up
  - EPWM_TZ_ADV_ACTION_EVENT_TZA_D - TZ1 - TZ6, DCAEVT2, DCAEVT1 while counting down
  - EPWM_TZ_ADV_ACTION_EVENT_TZA_U - TZ1 - TZ6, DCAEVT2, DCAEVT1 while counting up
- tzAdvAction
  - EPWM_TZ_ADV_ACTION_HIGH_Z - high impedance output
  - EPWM_TZ_ADV_ACTION_HIGH - high voltage state
  - EPWM_TZ_ADV_ACTION_LOW - low voltage state
  - EPWM_TZ_ADV_ACTION_TOGGLE - Toggle output
  - EPWM_TZ_ADV_ACTION_DISABLE - disable action

Note

This function enables the advanced Trip Zone event.
This function operates on both ePWMA and ePWMB depending on the tzAdvEvent parameter.
Advanced Trip Zone events take into consideration the direction of the counter in addition to Trip Zone events.

Returns

None.

16.2.4.66 static void EPWM_setTripZoneAdvDigitalCompareActionA (uint32_t *base*, **EPWM_TripZoneAdvDigitalCompareEvent** *tzAdvDCEvent*, **EPWM_TripZoneAdvancedAction** *tzAdvDCAction*) `[inline]`, `[static]`

Set Advanced Digital Compare Trip Zone Action on ePWMA.

Parameters

base	is the base address of the EPWM module.

tzAdvDCEvent	is the Digital Compare Trip Zone event type.
tzAdvDCAction	is the Digital Compare Trip zone Action.

This function sets the Digital Compare (DC) Advanced Trip Zone Action to be taken on ePWMA when an advanced Digital Compare Trip Zone A event occurs. Valid values for the parameters are:

- tzAdvDCEvent
  - EPWM_TZ_ADV_ACTION_EVENT_DCxEVT2_D - Digital Compare event A2 while counting down
  - EPWM_TZ_ADV_ACTION_EVENT_DCxEVT2_U - Digital Compare event A2 while counting up
  - EPWM_TZ_ADV_ACTION_EVENT_DCxEVT1_D - Digital Compare event A1 while counting down
  - EPWM_TZ_ADV_ACTION_EVENT_DCxEVT1_U - Digital Compare event A1 while counting up
- tzAdvDCAction
  - EPWM_TZ_ADV_ACTION_HIGH_Z - high impedance output
  - EPWM_TZ_ADV_ACTION_HIGH - high voltage state
  - EPWM_TZ_ADV_ACTION_LOW - low voltage state
  - EPWM_TZ_ADV_ACTION_TOGGLE - Toggle output
  - EPWM_TZ_ADV_ACTION_DISABLE - disable action

Note

This function enables the advanced Trip Zone event.
Advanced Trip Zone events take into consideration the direction of the counter in addition to Digital Compare Trip Zone events.

Returns

None.

16.2.4.67 static void EPWM_setTripZoneAdvDigitalCompareActionB (uint32_t *base*, **EPWM_TripZoneAdvDigitalCompareEvent** *tzAdvDCEvent*, **EPWM_TripZoneAdvancedAction** *tzAdvDCAction*) [inline], [static]

Set Advanced Digital Compare Trip Zone Action on ePWMB.

Parameters

base	is the base address of the EPWM module.
tzAdvDCEvent	is the Digital Compare Trip Zone event type.
tzAdvDCAction	is the Digital Compare Trip zone Action.

This function sets the Digital Compare (DC) Advanced Trip Zone Action to be taken on ePWMB when an advanced Digital Compare Trip Zone B event occurs. Valid values for the parameters are:

- tzAdvDCEvent
  - EPWM_TZ_ADV_ACTION_EVENT_DCxEVT2_D - Digital Compare event B2 while counting down
  - EPWM_TZ_ADV_ACTION_EVENT_DCxEVT2_U - Digital Compare event B2 while counting up

- EPWM_TZ_ADV_ACTION_EVENT_DCxEVT1_D - Digital Compare event B1 while counting down
- EPWM_TZ_ADV_ACTION_EVENT_DCxEVT1_U - Digital Compare event B1 while counting up

■ tzAdvDCAction

- EPWM_TZ_ADV_ACTION_HIGH_Z - high impedance output
- EPWM_TZ_ADV_ACTION_HIGH - high voltage state
- EPWM_TZ_ADV_ACTION_LOW - low voltage state
- EPWM_TZ_ADV_ACTION_TOGGLE - Toggle output
- EPWM_TZ_ADV_ACTION_DISABLE - disable action

Note

This function enables the advanced Trip Zone event.
Advanced Trip Zone events take into consideration the direction of the counter in addition to Digital Compare Trip Zone events.

Returns

None.

16.2.4.68 static void EPWM_enableTripZoneInterrupt (uint32_t *base,* uint16_t *tzInterrupt*) [inline], [static]

Enable Trip Zone interrupts.

Parameters

base	is the base address of the EPWM module.
tzInterrupt	is the Trip Zone interrupt.

This function enables the Trip Zone interrupts. Valid values for tzInterrupt are:

- EPWM_TZ_INTERRUPT_CBC - Trip Zones Cycle By Cycle interrupt
- EPWM_TZ_INTERRUPT_OST - Trip Zones One Shot interrupt
- EPWM_TZ_INTERRUPT_DCAEVT1 - Digital Compare A Event 1 interrupt
- EPWM_TZ_INTERRUPT_DCAEVT2 - Digital Compare A Event 2 interrupt
- EPWM_TZ_INTERRUPT_DCBEVT1 - Digital Compare B Event 1 interrupt
- EPWM_TZ_INTERRUPT_DCBEVT2 - Digital Compare B Event 2 interrupt

note: A logical OR of the valid values can be passed as the tzInterrupt parameter.

Returns

None.

16.2.4.69 static void EPWM_disableTripZoneInterrupt (uint32_t *base,* uint16_t *tzInterrupt*) [inline], [static]

Disable Trip Zone interrupts.

Parameters

base	is the base address of the EPWM module.
tzInterrupt	is the Trip Zone interrupt.

This function disables the Trip Zone interrupts. Valid values for tzInterrupt are:

- EPWM_TZ_INTERRUPT_CBC - Trip Zones Cycle By Cycle interrupt
- EPWM_TZ_INTERRUPT_OST - Trip Zones One Shot interrupt
- EPWM_TZ_INTERRUPT_DCAEVT1 - Digital Compare A Event 1 interrupt
- EPWM_TZ_INTERRUPT_DCAEVT2 - Digital Compare A Event 2 interrupt
- EPWM_TZ_INTERRUPT_DCBEVT1 - Digital Compare B Event 1 interrupt
- EPWM_TZ_INTERRUPT_DCBEVT2 - Digital Compare B Event 2 interrupt

note: A logical OR of the valid values can be passed as the tzInterrupt parameter.

Returns

None.

16.2.4.70 static uint16_t EPWM_getTripZoneFlagStatus (uint32_t *base*) `[inline]`, `[static]`

Gets the Trip Zone status flag

Parameters

base	is the base address of the EPWM module.

This function returns the Trip Zone status flag.

Returns

The function returns the following or the bitwise OR value of the following values.

- EPWM_TZ_INTERRUPT - Trip Zone interrupt was generated due to the following TZ events.
- EPWM_TZ_FLAG_CBC - Trip Zones Cycle By Cycle event status flag
- EPWM_TZ_FLAG_OST - Trip Zones One Shot event status flag
- EPWM_TZ_FLAG_DCAEVT1 - Digital Compare A Event 1 status flag
- EPWM_TZ_FLAG_DCAEVT2 - Digital Compare A Event 2 status flag
- EPWM_TZ_FLAG_DCBEVT1 - Digital Compare B Event 1 status flag
- EPWM_TZ_FLAG_DCBEVT2 - Digital Compare B Event 2 status flag

16.2.4.71 static uint16_t EPWM_getCycleByCycleTripZoneFlagStatus (uint32_t *base*) `[inline]`, `[static]`

Gets the Trip Zone Cycle by Cycle flag status

Parameters

base	is the base address of the EPWM module.

This function returns the specific Cycle by Cycle Trip Zone flag status.

Returns

The function returns the following values.

- EPWM_TZ_CBC_FLAG_1 - CBC 1 status flag
- EPWM_TZ_CBC_FLAG_2 - CBC 2 status flag
- EPWM_TZ_CBC_FLAG_3 - CBC 3 status flag
- EPWM_TZ_CBC_FLAG_4 - CBC 4 status flag
- EPWM_TZ_CBC_FLAG_5 - CBC 5 status flag
- EPWM_TZ_CBC_FLAG_6 - CBC 6 status flag
- EPWM_TZ_CBC_FLAG_DCAEVT2 - CBC status flag for Digital compare event A2
- EPWM_TZ_CBC_FLAG_DCBEVT2 - CBC status flag for Digital compare event B2

16.2.4.72 static uint16_t EPWM_getOneShotTripZoneFlagStatus (uint32_t *base*) [inline], [static]

Gets the Trip Zone One Shot flag status

Parameters

base	is the base address of the EPWM module.

This function returns the specific One Shot Trip Zone flag status.

Returns

The function returns the bitwise OR of the following flags.

- EPWM_TZ_OST_FLAG_OST1 - OST status flag for OST1
- EPWM_TZ_OST_FLAG_OST2 - OST status flag for OST2
- EPWM_TZ_OST_FLAG_OST3 - OST status flag for OST3
- EPWM_TZ_OST_FLAG_OST4 - OST status flag for OST4
- EPWM_TZ_OST_FLAG_OST5 - OST status flag for OST5
- EPWM_TZ_OST_FLAG_OST6 - OST status flag for OST6
- EPWM_TZ_OST_FLAG_DCAEVT1 - OST status flag for Digital compare event A1
- EPWM_TZ_OST_FLAG_DCBEVT1 - OST status flag for Digital compare event B1

16.2.4.73 static void EPWM_selectCycleByCycleTripZoneClearEvent (uint32_t *base,* **EPWM_CycleByCycleTripZoneClearMode** *clearEvent*) [inline], [static]

Set the Trip Zone CBC pulse clear event.

Parameters

base	is the base address of the EPWM module.
clearEvent	is the CBC trip zone clear event.

This function set the event which automatically clears the CBC (Cycle by Cycle) latch. Valid values for clearEvent are:

- EPWM_TZ_CBC_PULSE_CLR_CNTR_ZERO - Clear CBC pulse when counter equals zero
- EPWM_TZ_CBC_PULSE_CLR_CNTR_PERIOD - Clear CBC pulse when counter equals period
- EPWM_TZ_CBC_PULSE_CLR_CNTR_ZERO_PERIOD - Clear CBC pulse when counter equals zero or period

Returns

None.

16.2.4.74 static void EPWM_clearTripZoneFlag (uint32_t *base,* uint16_t *tzFlags*) [inline], [static]

Clear Trip Zone flag

Parameters

base	is the base address of the EPWM module.
tzFlags	is the Trip Zone flags.

This function clears the Trip Zone flags Valid values for tzFlags are:

- EPWM_TZ_INTERRUPT - Global Trip Zone interrupt flag
- EPWM_TZ_FLAG_CBC - Trip Zones Cycle By Cycle flag
- EPWM_TZ_FLAG_OST - Trip Zones One Shot flag
- EPWM_TZ_FLAG_DCAEVT1 - Digital Compare A Event 1 flag
- EPWM_TZ_FLAG_DCAEVT2 - Digital Compare A Event 2 flag
- EPWM_TZ_FLAG_DCBEVT1 - Digital Compare B Event 1 flag
- EPWM_TZ_FLAG_DCBEVT2 - Digital Compare B Event 2 flag

note: A bitwise OR of the valid values can be passed as the tzFlags parameter.

Returns

None.

16.2.4.75 static void EPWM_clearCycleByCycleTripZoneFlag (uint32_t *base,* uint16_t *tzCBCFlags*) [inline], [static]

Clear the Trip Zone Cycle by Cycle flag.

Parameters

base	is the base address of the EPWM module.
tzCBCFlags	is the CBC flag to be cleared.

This function clears the specific Cycle by Cycle Trip Zone flag. The following are valid values for tzCBCFlags.

- EPWM_TZ_CBC_FLAG_1 - CBC 1 flag
- EPWM_TZ_CBC_FLAG_2 - CBC 2 flag
- EPWM_TZ_CBC_FLAG_3 - CBC 3 flag
- EPWM_TZ_CBC_FLAG_4 - CBC 4 flag
- EPWM_TZ_CBC_FLAG_5 - CBC 5 flag
- EPWM_TZ_CBC_FLAG_6 - CBC 6 flag
- EPWM_TZ_CBC_FLAG_DCAEVT2 - CBC flag Digital compare event A2
- EPWM_TZ_CBC_FLAG_DCBEVT2 - CBC flag Digital compare event B2

Returns
None.

16.2.4.76 static void EPWM_clearOneShotTripZoneFlag (uint32_t *base,* uint16_t *tzOSTFlags*) [inline], [static]

Clear the Trip Zone One Shot flag.

Parameters

base	is the base address of the EPWM module.
tzOSTFlags	is the OST flags to be cleared.

This function clears the specific One Shot (OST) Trip Zone flag. The following are valid values for tzOSTFlags.

- EPWM_TZ_OST_FLAG_OST1 - OST flag for OST1
- EPWM_TZ_OST_FLAG_OST2 - OST flag for OST2
- EPWM_TZ_OST_FLAG_OST3 - OST flag for OST3
- EPWM_TZ_OST_FLAG_OST4 - OST flag for OST4
- EPWM_TZ_OST_FLAG_OST5 - OST flag for OST5
- EPWM_TZ_OST_FLAG_OST6 - OST flag for OST6
- EPWM_TZ_OST_FLAG_DCAEVT1 - OST flag for Digital compare event A1
- EPWM_TZ_OST_FLAG_DCBEVT1 - OST flag for Digital compare event B1

Returns
None.

16.2.4.77 static void EPWM_forceTripZoneEvent (uint32_t *base,* uint16_t *tzForceEvent*) [inline], [static]

Force Trip Zone events.

Parameters

base	is the base address of the EPWM module.
tzForceEvent	is the forced Trip Zone event.

This function forces a Trip Zone event. Valid values for tzForceEvent are:

- EPWM_TZ_FORCE_EVENT_CBC - Force Trip Zones Cycle By Cycle event
- EPWM_TZ_FORCE_EVENT_OST - Force Trip Zones One Shot Event
- EPWM_TZ_FORCE_EVENT_DCAEVT1 - Force Digital Compare A Event 1
- EPWM_TZ_FORCE_EVENT_DCAEVT2 - Force Digital Compare A Event 2
- EPWM_TZ_FORCE_EVENT_DCBEVT1 - Force Digital Compare B Event 1
- EPWM_TZ_FORCE_EVENT_DCBEVT2 - Force Digital Compare B Event 2

Returns
None.

16.2.4.78 static void EPWM_enableInterrupt (uint32_t *base*) [inline], [static]

Enable ePWM interrupt.

Parameters

base	is the base address of the EPWM module.

This function enables the ePWM interrupt.

Returns
None.

16.2.4.79 static void EPWM_disableInterrupt (uint32_t *base*) [inline], [static]

disable ePWM interrupt.

Parameters

base	is the base address of the EPWM module.

This function disables the ePWM interrupt.

Returns
None.

16.2.4.80 static void EPWM_setInterruptSource (uint32_t *base,* uint16_t *interruptSource*) [inline], [static]

Sets the ePWM interrupt source.

Parameters

base	is the base address of the EPWM module.
interruptSource	is the ePWM interrupt source.

This function sets the ePWM interrupt source. Valid values for interruptSource are:

- EPWM_INT_TBCTR_ZERO - Time-base counter equal to zero
- EPWM_INT_TBCTR_PERIOD - Time-base counter equal to period
- EPWM_INT_TBCTR_ZERO_OR_PERIOD - Time-base counter equal to zero or period
- EPWM_INT_TBCTR_U_CMPx - Where x is A, B, C or D Time-base counter equal to CMPA, CMPB, CMPC or CMPD (depending the value of x) when the timer is incrementing
- EPWM_INT_TBCTR_D_CMPx - Where x is A, B, C or D Time-base counter equal to CMPA, CMPB, CMPC or CMPD (depending the value of x) when the timer is decrementing

Returns

None.

References EPWM_INT_TBCTR_D_CMPA, EPWM_INT_TBCTR_D_CMPB, EPWM_INT_TBCTR_D_CMPC, EPWM_INT_TBCTR_D_CMPD, EPWM_INT_TBCTR_U_CMPA, EPWM_INT_TBCTR_U_CMPB, EPWM_INT_TBCTR_U_CMPC, and EPWM_INT_TBCTR_U_CMPD.

16.2.4.81 static void EPWM_setInterruptEventCount (uint32_t *base,* uint16_t *eventCount*) [inline], [static]

Sets the ePWM interrupt event counts.

Parameters

base	is the base address of the EPWM module.
eventCount	is the event count for interrupt scale

This function sets the interrupt event count that determines the number of events that have to occur before an interrupt is issued. Maximum value for eventCount is 15.

Returns

None.

16.2.4.82 static bool EPWM_getEventTriggerInterruptStatus (uint32_t *base*) [inline], [static]

Return the interrupt status.

Parameters

base	is the base address of the EPWM module.

This function returns the ePWM interrupt status. **Note** This function doesn't return the Trip Zone status.

Returns

Returns true if ePWM interrupt was generated. Returns false if no interrupt was generated

16.2.4.83 static void EPWM_clearEventTriggerInterruptFlag (uint32_t *base*) [inline], [static]

Clear interrupt flag.

Parameters

base	is the base address of the EPWM module.

This function clears the ePWM interrupt flag.

Returns
None

16.2.4.84 static void EPWM_enableInterruptEventCountInit (uint32_t *base*) [inline], [static]

Enable Pre-interrupt count load.

Parameters

base	is the base address of the EPWM module.

This function enables the ePWM interrupt counter to be pre-interrupt loaded with a count value.

Note
This is valid only for advanced/expanded interrupt mode

Returns
None.

16.2.4.85 static void EPWM_disableInterruptEventCountInit (uint32_t *base*) [inline], [static]

Disable interrupt count load.

Parameters

base	is the base address of the EPWM module.

This function disables the ePWM interrupt counter from being loaded with pre-interrupt count value.

Returns
None.

16.2.4.86 static void EPWM_forceInterruptEventCountInit (uint32_t *base*) [inline], [static]

Force a software pre interrupt event counter load.

Parameters

base	is the base address of the EPWM module.

This function forces the ePWM interrupt counter to be loaded with the contents set by EPWM_setPreInterruptEventCount().

Note

make sure the EPWM_enablePreInterruptEventCountLoad() function is is called before invoking this function.

Returns

None.

16.2.4.87 static void EPWM_setInterruptEventCountInitValue (uint32_t *base*, uint16_t *eventCount*) [inline], [static]

Set interrupt count.

Parameters

base	is the base address of the EPWM module.
eventCount	is the ePWM interrupt count value.

This function sets the ePWM interrupt count. eventCount is the value of the pre-interrupt value that is to be loaded. The maximum value of eventCount is 15.

Returns

None.

16.2.4.88 static uint16_t EPWM_getInterruptEventCount (uint32_t *base*) [inline], [static]

Get the interrupt count.

Parameters

base	is the base address of the EPWM module.

This function returns the ePWM interrupt event count.

Returns

The interrupt event counts that have occurred.

16.2.4.89 static void EPWM_forceEventTriggerInterrupt (uint32_t *base*) [inline], [static]

Force ePWM interrupt.

Parameters

base	is the base address of the EPWM module.

This function forces an ePWM interrupt.

Returns

None

16.2.4.90 static void EPWM_enableADCTrigger (uint32_t *base*, **EPWM_ADCStartOfConversionType** *adcSOCType*) [inline], [static]

Enable ADC SOC event.

Parameters

base	is the base address of the EPWM module.
adcSOCType	is the ADC SOC type.

This function enables the ePWM module to trigger an ADC SOC event. Valid values for adcSOCType are:

- EPWM_SOC_A - SOC A
- EPWM_SOC_B - SOC B

Returns
None.

References EPWM_SOC_A.

16.2.4.91 static void EPWM_disableADCTrigger (uint32_t *base*, **EPWM_ADCStartOfConversionType** *adcSOCType*) [inline], [static]

Disable ADC SOC event.

Parameters

base	is the base address of the EPWM module.
adcSOCType	is the ADC SOC type.

This function disables the ePWM module from triggering an ADC SOC event. Valid values for adcSOCType are:

- EPWM_SOC_A - SOC A
- EPWM_SOC_B - SOC B

Returns
None.

References EPWM_SOC_A.

16.2.4.92 static void EPWM_setADCTriggerSource (uint32_t *base*, **EPWM_ADCStartOfConversionType** *adcSOCType*, **EPWM_ADCStartOfConversionSource** *socSource*) [inline], [static]

Sets the ePWM SOC source.

Parameters

base	is the base address of the EPWM module.
adcSOCType	is the ADC SOC type.
socSource	is the SOC source.

This function sets the ePWM ADC SOC source. Valid values for socSource are:

- adcSOCType

- EPWM_SOC_A - SOC A
- EPWM_SOC_B - SOC B

- socSource
  - EPWM_SOC_DCxEVT1 - Event is based on DCxEVT1
  - EPWM_SOC_TBCTR_ZERO - Time-base counter equal to zero
  - EPWM_SOC_TBCTR_PERIOD - Time-base counter equal to period
  - EPWM_SOC_TBCTR_ZERO_OR_PERIOD - Time-base counter equal to zero or period
  - EPWM_SOC_TBCTR_U_CMPx - Where x is A, B, C or D Time-base counter equal to CMPA, CMPB, CMPC or CMPD(depending the value of x) when the timer is incrementing
  - EPWM_SOC_TBCTR_D_CMPx - Where x is A, B, C or D Time-base counter equal to CMPA, CMPB, CMPC or CMPD(depending the value of x) when the timer is decrementing

Returns

None.

References EPWM_SOC_A, EPWM_SOC_TBCTR_D_CMPA, EPWM_SOC_TBCTR_D_CMPB, EPWM_SOC_TBCTR_D_CMPC, EPWM_SOC_TBCTR_D_CMPD, EPWM_SOC_TBCTR_U_CMPA, EPWM_SOC_TBCTR_U_CMPB, EPWM_SOC_TBCTR_U_CMPC, and EPWM_SOC_TBCTR_U_CMPD.

16.2.4.93 static void EPWM_setADCTriggerEventPrescale (uint32_t *base*, **EPWM_ADCStartOfConversionType** *adcSOCType*, uint16_t *preScaleCount*) [inline], [static]

Sets the ePWM SOC event counts.

Parameters

base	is the base address of the EPWM module.
adcSOCType	is the ADC SOC type.
preScaleCount	is the event count number.

This function sets the SOC event count that determines the number of events that have to occur before an SOC is issued. Valid values for the parameters are:

- adcSOCType
  - EPWM_SOC_A - SOC A
  - EPWM_SOC_B - SOC B
- preScaleCount
  - [1 - 15] - Generate SOC pulse every preScaleCount up to 15 events.

Note

A preScaleCount value of 0 disables the prescale.

Returns

None.

References EPWM_SOC_A.

16.2.4.94 static bool EPWM_getADCTriggerFlagStatus (uint32_t *base*, **EPWM_ADCStartOfConversionType** *adcSOCType*) `[inline]`, `[static]`

Return the SOC event status.

Parameters

base	is the base address of the EPWM module.
adcSOCType	is the ADC SOC type.

This function returns the ePWM SOC status. Valid values for adcSOCType are:

- EPWM_SOC_A - SOC A
- EPWM_SOC_B - SOC B

Returns

Returns true if the selected adcSOCType SOC was generated. Returns false if the selected adcSOCType SOC was not generated.

16.2.4.95 static void EPWM_clearADCTriggerFlag (uint32_t *base*, **EPWM_ADCStartOfConversionType** *adcSOCType*) [inline], [static]

Clear SOC flag.

Parameters

base	is the base address of the EPWM module.
adcSOCType	is the ADC SOC type.

This function clears the ePWM SOC flag. Valid values for adcSOCType are:

- EPWM_SOC_A - SOC A
- EPWM_SOC_B - SOC B

Returns

None

16.2.4.96 static void EPWM_enableADCTriggerEventCountInit (uint32_t *base*, **EPWM_ADCStartOfConversionType** *adcSOCType*) [inline], [static]

Enable Pre-SOC event count load.

Parameters

base	is the base address of the EPWM module.
adcSOCType	is the ADC SOC type.

This function enables the ePWM SOC event counter which is set by the EPWM_setADCTriggerEventCountInitValue() function to be loaded before an SOC event. Valid values for adcSOCType are:

- EPWM_SOC_A - SOC A
- EPWM_SOC_B - SOC B

Note

This is valid only for advanced/expanded SOC mode

Returns
None.

16.2.4.97 static void EPWM_disableADCTriggerEventCountInit (uint32_t *base*, **EPWM_ADCStartOfConversionType** *adcSOCType*) [inline], [static]

Disable Pre-SOC event count load.

Parameters

base	is the base address of the EPWM module.
adcSOCType	is the ADC SOC type.

This function disables the ePWM SOC event counter from being loaded before an SOC event (only an SOC event causes an increment of the counter value). Valid values for adcSOCType are:

- EPWM_SOC_A - SOC A
- EPWM_SOC_B - SOC B

Note
This is valid only for advanced/expanded SOC mode

Returns
None.

16.2.4.98 static void EPWM_forceADCTriggerEventCountInit (uint32_t *base*, **EPWM_ADCStartOfConversionType** *adcSOCType*) [inline], [static]

Force a software pre SOC event counter load.

Parameters

base	is the base address of the EPWM module.
adcSOCType	is the ADC SOC type

This function forces the ePWM SOC counter to be loaded with the contents set by EPWM_setPreADCStartOfConversionEventCount().

Note
make sure the EPWM_enableADCTriggerEventCountInit() function is called before invoking this function.

Returns
None.

16.2.4.99 static void EPWM_setADCTriggerEventCountInitValue (uint32_t *base*, **EPWM_ADCStartOfConversionType** *adcSOCType*, uint16_t *eventCount*) [inline], [static]

Set ADC Trigger count values.

Parameters

base	is the base address of the EPWM module.
adcSOCType	is the ADC SOC type.
eventCount	is the ePWM interrupt count value.

This function sets the ePWM ADC Trigger count values. Valid values for adcSOCType are:

- EPWM_SOC_A - SOC A
- EPWM_SOC_B - SOC B The eventCount has a maximum value of 15.

Returns
None.

References EPWM_SOC_A.

16.2.4.100 static uint16_t EPWM_getADCTriggerEventCount (uint32_t *base*, **EPWM_ADCStartOfConversionType** *adcSOCType*) [inline], [static]

Get the SOC event count.

Parameters

base	is the base address of the EPWM module.
adcSOCType	is the ADC SOC type.

This function returns the ePWM SOC event count. Valid values for adcSOCType are:

- EPWM_SOC_A - SOC A
- EPWM_SOC_B - SOC B

Returns
The SOC event counts that have occurred.

References EPWM_SOC_A.

16.2.4.101 static void EPWM_forceADCTrigger (uint32_t *base*, **EPWM_ADCStartOfConversionType** *adcSOCType*) [inline], [static]

Force SOC event.

Parameters

base	is the base address of the EPWM module.
adcSOCType	is the ADC SOC type.

This function forces an ePWM SOC event. Valid values for adcSOCType are:

- EPWM_SOC_A - SOC A
- EPWM_SOC_B - SOC B

Returns
None

16.2.4.102 static void EPWM_selectDigitalCompareTripInput (uint32_t *base*, **EPWM_DigitalCompareTripInput** *tripSource*, **EPWM_DigitalCompareType** *dcType*) [inline], [static]

Set the DC trip input.

Parameters

base	is the base address of the EPWM module.
tripSource	is the tripSource.
dcType	is the Digital Compare type.

This function sets the trip input to the Digital Compare (DC). For a given dcType the function sets the tripSource to be the input to the DC. Valid values for the parameter are:

- tripSource
  - EPWM_DC_TRIP_TRIPINx - Trip x, where x ranges from 1 to 15 excluding 13
  - EPWM_DC_TRIP_COMBINATION - selects all the Trip signals whose input is enabled by the following function EPWM_enableDigitalCompareTripCombinationInput()
- dcType
  - EPWM_DC_TYPE_DCAH - Digital Compare A High
  - EPWM_DC_TYPE_DCAL - Digital Compare A Low
  - EPWM_DC_TYPE_DCBH - Digital Compare B High
  - EPWM_DC_TYPE_DCBL - Digital Compare B Low

Returns
None

16.2.4.103 static void EPWM_enableDigitalCompareBlankingWindow (uint32_t *base*) [inline], [static]

Enable DC filter blanking window.

Parameters

base	is the base address of the EPWM module.

This function enables the DC filter blanking window.

Returns
None

16.2.4.104 static void EPWM_disableDigitalCompareBlankingWindow (uint32_t *base*) [inline], [static]

Disable DC filter blanking window.

Parameters

base	is the base address of the EPWM module.

This function disables the DC filter blanking window.

Returns
None

16.2.4.105 static void EPWM_enableDigitalCompareWindowInverseMode (uint32_t *base*) [inline], [static]

Enable Digital Compare Window inverse mode.

Parameters

base	is the base address of the EPWM module.

This function enables the Digital Compare Window inverse mode. This will invert the blanking window.

Returns
None

16.2.4.106 static void EPWM_disableDigitalCompareWindowInverseMode (uint32_t *base*) [inline], [static]

Disable Digital Compare Window inverse mode.

Parameters

base	is the base address of the EPWM module.

This function disables the Digital Compare Window inverse mode.

Returns
None

16.2.4.107 static void EPWM_setDigitalCompareBlankingEvent (uint32_t *base*, **EPWM_DigitalCompareBlankingPulse** *blankingPulse*) [inline], [static]

Set the Digital Compare filter blanking pulse.

Parameters

base	is the base address of the EPWM module.
blankingPulse	is Pulse that starts blanking window.

This function sets the input pulse that starts the Digital Compare blanking window. Valid values for blankingPulse are:

- EPWM_DC_WINDOW_START_TBCTR_PERIOD - Time base counter equals period
- EPWM_DC_WINDOW_START_TBCTR_ZERO - Time base counter equals zero

- EPWM_DC_WINDOW_START_TBCTR_ZERO_PERIOD - Time base counter equals zero or period.

Returns
None

16.2.4.108 static void EPWM_setDigitalCompareFilterInput (uint32_t *base*, **EPWM_DigitalCompareFilterInput** *filterInput*) [inline], [static]

Set up the Digital Compare filter input.

Parameters

base	is the base address of the EPWM module.
filterInput	is Digital Compare signal source.

This function sets the signal input source that will be filtered by the Digital Compare module. Valid values for filterInput are:

- EPWM_DC_WINDOW_SOURCE_DCAEVT1 - DC filter signal source is DCAEVT1
- EPWM_DC_WINDOW_SOURCE_DCAEVT2 - DC filter signal source is DCAEVT2
- EPWM_DC_WINDOW_SOURCE_DCBEVT1 - DC filter signal source is DCBEVT1
- EPWM_DC_WINDOW_SOURCE_DCBEVT2 - DC filter signal source is DCBEVT2

Returns
None

16.2.4.109 static void EPWM_enableDigitalCompareEdgeFilter (uint32_t *base*) [inline], [static]

Enable Digital Compare Edge Filter.

Parameters

base	is the base address of the EPWM module.

This function enables the Digital Compare Edge filter to generate event after configured number of edges.

Returns
None

16.2.4.110 static void EPWM_disableDigitalCompareEdgeFilter (uint32_t *base*) [inline], [static]

Disable Digital Compare Edge Filter.

Parameters

base	is the base address of the EPWM module.

This function disables the Digital Compare Edge filter.

Returns

None

16.2.4.111 static void EPWM_setDigitalCompareEdgeFilterMode (uint32_t *base*, **EPWM_DigitalCompareEdgeFilterMode** *edgeMode*) [inline], [static]

Set the Digital Compare Edge Filter Mode.

Parameters

base	is the base address of the EPWM module.
edgeMode	is Digital Compare Edge filter mode.

This function sets the Digital Compare Event filter mode. Valid values for edgeMode are:

- EPWM_DC_EDGEFILT_MODE_RISING - DC edge filter mode is rising edge
- EPWM_DC_EDGEFILT_MODE_FALLING - DC edge filter mode is falling edge
- EPWM_DC_EDGEFILT_MODE_BOTH - DC edge filter mode is both edges

Returns

None

16.2.4.112 static void EPWM_setDigitalCompareEdgeFilterEdgeCount (uint32_t *base*, uint16_t *edgeCount*) [inline], [static]

Set the Digital Compare Edge Filter Edge Count.

Parameters

base	is the base address of the EPWM module.
edgeCount	is Digital Compare event filter count

This function sets the Digital Compare Event filter Edge Count to generate events. Valid values for edgeCount can be:

- EPWM_DC_EDGEFILT_EDGECNT_0 - No edge is required to generate event
- EPWM_DC_EDGEFILT_EDGECNT_1 - 1 edge is required for event generation
- EPWM_DC_EDGEFILT_EDGECNT_2 - 2 edges are required for event generation
- EPWM_DC_EDGEFILT_EDGECNT_3 - 3 edges are required for event generation
- EPWM_DC_EDGEFILT_EDGECNT_4 - 4 edges are required for event generation
- EPWM_DC_EDGEFILT_EDGECNT_5 - 5 edges are required for event generation
- EPWM_DC_EDGEFILT_EDGECNT_6 - 6 edges are required for event generation
- EPWM_DC_EDGEFILT_EDGECNT_7 - 7 edges are required for event generation

Returns
None

16.2.4.113 static uint16_t EPWM_getDigitalCompareEdgeFilterEdgeCount (uint32_t *base*) [inline], [static]

Returns the Digital Compare Edge Filter Edge Count.

Parameters

base	is the base address of the EPWM module.

This function returns the configured Digital Compare Edge filter edge count required to generate events. It can return values from 0-7.

Returns
Returns the configured DigitalCompare Edge filter edge count.

16.2.4.114 static uint16_t EPWM_getDigitalCompareEdgeFilterEdgeStatus (uint32_t *base*) [inline], [static]

Returns the Digital Compare Edge filter captured edge count status.

Parameters

base	is the base address of the EPWM module.

This function returns the count of edges captured by Digital Compare Edge filter. It can return values from 0-7.

Returns
Returns the count of captured edges

16.2.4.115 static void EPWM_setDigitalCompareWindowOffset (uint32_t *base,* uint16_t *windowOffsetCount*) [inline], [static]

Set up the Digital Compare filter window offset

Parameters

base	is the base address of the EPWM module.
windowOffset-Count	is blanking window offset length.

This function sets the offset between window start pulse and blanking window in TBCLK count. The function take a 16bit count value for the offset value.

Returns
None

16.2.4.116 static void EPWM_setDigitalCompareWindowLength (uint32_t *base*, uint16_t *windowLengthCount*) [inline], [static]

Set up the Digital Compare filter window length

Parameters

base	is the base address of the EPWM module.
windowLength-Count	is blanking window length.

This function sets up the Digital Compare filter blanking window length in TBCLK count.The function takes a 16bit count value for the window length.

Returns
None

16.2.4.117 static uint16_t EPWM_getDigitalCompareBlankingWindowOffsetCount (uint32_t *base*) [inline], [static]

Return DC filter blanking window offset count.

Parameters

base	is the base address of the EPWM module.

This function returns DC filter blanking window offset count.

Returns
None

16.2.4.118 static uint16_t EPWM_getDigitalCompareBlankingWindowLengthCount (uint32_t *base*) [inline], [static]

Return DC filter blanking window length count.

Parameters

base	is the base address of the EPWM module.

This function returns DC filter blanking window length count.

Returns
None

16.2.4.119 static void EPWM_setDigitalCompareEventSource (uint32_t *base*, **EPWM_DigitalCompareModule** *dcModule*, **EPWM_DigitalCompareEvent** *dcEvent*, **EPWM_DigitalCompareEventSource** *dcEventSource*) [inline], [static]

Set up the Digital Compare Event source.

Parameters

base	is the base address of the EPWM module.
dcModule	is the Digital Compare module.
dcEvent	is the Digital Compare Event number.
dcEventSource	is the - Digital Compare Event source.

This function sets up the Digital Compare module Event sources. The following are valid values for the parameters.

- dcModule
  - EPWM_DC_MODULE_A - Digital Compare Module A
  - EPWM_DC_MODULE_B - Digital Compare Module B
- dcEvent
  - EPWM_DC_EVENT_1 - Digital Compare Event number 1
  - EPWM_DC_EVENT_2 - Digital Compare Event number 2
- dcEventSource
  - EPWM_DC_EVENT_SOURCE_FILT_SIGNAL - signal source is filtered

    Note

    The signal source for this option is DCxEVTy, where the value of x is dependent on dcModule and the value of y is dependent on dcEvent. Possible signal sources are DCAEVT1, DCBEVT1, DCAEVT2 or DCBEVT2 depending on the value of both dcModule and dcEvent.
  - EPWM_DC_EVENT_SOURCE_ORIG_SIGNAL - signal source is unfiltered The signal source for this option is DCEVTFILT.

    Returns

    None

References EPWM_DC_EVENT_1.

16.2.4.120 static void EPWM_setDigitalCompareEventSyncMode (uint32_t *base*, **EPWM_DigitalCompareModule** *dcModule*, **EPWM_DigitalCompareEvent** *dcEvent*, **EPWM_DigitalCompareSyncMode** *syncMode*) [inline], [static]

Set up the Digital Compare input sync mode.

Parameters

base	is the base address of the EPWM module.
dcModule	is the Digital Compare module.
dcEvent	is the Digital Compare Event number.
syncMode	is the Digital Compare Event sync mode.

This function sets up the Digital Compare module Event sources. The following are valid values for the parameters.

- dcModule
  - EPWM_DC_MODULE_A - Digital Compare Module A
  - EPWM_DC_MODULE_B - Digital Compare Module B
- dcEvent

  - EPWM_DC_EVENT_1 - Digital Compare Event number 1
  - EPWM_DC_EVENT_2 - Digital Compare Event number 2
- syncMode
  - EPWM_DC_EVENT_INPUT_SYNCED - DC input signal is synced with TBCLK
  - EPWM_DC_EVENT_INPUT_NOT SYNCED - DC input signal is not synced with TBCLK

Returns

None

References EPWM_DC_EVENT_1.

16.2.4.121 static void EPWM_enableDigitalCompareADCTrigger (uint32_t *base*, **EPWM_DigitalCompareModule** *dcModule*) [inline], [static]

Enable Digital Compare to generate Start of Conversion.

Parameters

base	is the base address of the EPWM module.
dcModule	is the Digital Compare module.

This function enables the Digital Compare Event 1 to generate Start of Conversion. The following are valid values for the *dcModule* parameter.

- EPWM_DC_MODULE_A - Digital Compare Module A
- EPWM_DC_MODULE_B - Digital Compare Module B

Returns

None

16.2.4.122 static void EPWM_disableDigitalCompareADCTrigger (uint32_t *base*, **EPWM_DigitalCompareModule** *dcModule*) [inline], [static]

Disable Digital Compare from generating Start of Conversion.

Parameters

base	is the base address of the EPWM module.
dcModule	is the Digital Compare module.

This function disables the Digital Compare Event 1 from generating Start of Conversion. The following are valid values for the *dcModule* parameter.

- EPWM_DC_MODULE_A - Digital Compare Module A
- EPWM_DC_MODULE_B - Digital Compare Module B

Returns

None

16.2.4.123 static void EPWM_enableDigitalCompareSyncEvent (uint32_t *base*, **EPWM_DigitalCompareModule** *dcModule*) [inline], [static]

Enable Digital Compare to generate sync out pulse.

Parameters

base	is the base address of the EPWM module.
dcModule	is the Digital Compare module.

This function enables the Digital Compare Event 1 to generate sync out pulse The following are valid values for the *dcModule* parameter.

- EPWM_DC_MODULE_A - Digital Compare Module A
- EPWM_DC_MODULE_B - Digital Compare Module B

Returns
None

16.2.4.124 static void EPWM_disableDigitalCompareSyncEvent (uint32_t *base*, **EPWM_DigitalCompareModule** *dcModule*) [inline], [static]

Disable Digital Compare from generating Start of Conversion.

Parameters

base	is the base address of the EPWM module.
dcModule	is the Digital Compare module.

This function disables the Digital Compare Event 1 from generating synch out pulse. The following are valid values for the *dcModule* parameters.

- EPWM_DC_MODULE_A - Digital Compare Module A
- EPWM_DC_MODULE_B - Digital Compare Module B

Returns
None

16.2.4.125 static void EPWM_enableDigitalCompareCounterCapture (uint32_t *base*) [inline], [static]

Enables the Time Base Counter Capture controller.

Parameters

base	is the base address of the EPWM module.

This function enables the time Base Counter Capture.

Returns
None.

16.2.4.126 static void EPWM_disableDigitalCompareCounterCapture (uint32_t *base*) [inline], [static]

Disables the Time Base Counter Capture controller.

Parameters

base	is the base address of the EPWM module.

This function disable the time Base Counter Capture.

Returns
None.

16.2.4.127 static void EPWM_setDigitalCompareCounterShadowMode (uint32_t *base,* bool *enableShadowMode*) [inline], [static]

Set the Time Base Counter Capture mode.

Parameters

base	is the base address of the EPWM module.
enableShadow-Mode	is the shadow read mode flag.

This function sets the mode the Time Base Counter value is read from. If enableShadowMode is true, CPU reads of the DCCAP register will return the shadow register contents.If enableShadowMode is false, CPU reads of the DCCAP register will return the active register contents.

Returns
None.

16.2.4.128 static bool EPWM_getDigitalCompareCaptureStatus (uint32_t *base*) [inline], [static]

Return the DC Capture event status.

Parameters

base	is the base address of the EPWM module.

This function returns the DC capture event status.

Returns
Returns true if a DC capture event has occurs. Returns false if no DC Capture event has occurred.
None.

16.2.4.129 static uint16_t EPWM_getDigitalCompareCaptureCount (uint32_t *base*) [inline], [static]

Return the DC Time Base Counter capture value.

Parameters

base	is the base address of the EPWM module.

This function returns the DC Time Base Counter capture value. The value read is determined by the mode as set in the EPWM_setTimeBaseCounterReadMode() function.

Returns

Returns the DC Time Base Counter Capture count value.

16.2.4.130 static void EPWM_enableDigitalCompareTripCombinationInput (uint32_t *base*, uint16_t *tripInput*, **EPWM_DigitalCompareType** *dcType*) `[inline]`, `[static]`

Enable DC TRIP combinational input.

Parameters

base	is the base address of the EPWM module.
tripInput	is the Trip number.
dcType	is the Digital Compare module.

This function enables the specified Trip input. Valid values for the parameters are:

- tripInput
  - EPWM_DC_COMBINATIONAL_TRIPINx, where x is 1, 2, ...12, 14, 15
- dcType
  - EPWM_DC_TYPE_DCAH - Digital Compare A High
  - EPWM_DC_TYPE_DCAL - Digital Compare A Low
  - EPWM_DC_TYPE_DCBH - Digital Compare B High
  - EPWM_DC_TYPE_DCBL - Digital Compare B Low

Returns

None.

16.2.4.131 static void EPWM_disableDigitalCompareTripCombinationInput (uint32_t *base*, uint16_t *tripInput*, **EPWM_DigitalCompareType** *dcType*) `[inline]`, `[static]`

Disable DC TRIP combinational input.

Parameters

base	is the base address of the EPWM module.
tripInput	is the Trip number.
dcType	is the Digital Compare module.

This function disables the specified Trip input. Valid values for the parameters are:

- tripInput
  - EPWM_DC_COMBINATIONAL_TRIPINx, where x is 1, 2, ...12, 14, 15

- dcType
  - EPWM_DC_TYPE_DCAH - Digital Compare A High
  - EPWM_DC_TYPE_DCAL - Digital Compare A Low
  - EPWM_DC_TYPE_DCBH - Digital Compare B High
  - EPWM_DC_TYPE_DCBL - Digital Compare B Low

Returns
None.

16.2.4.132 static void EPWM_enableValleyCapture (uint32_t *base*) [inline], [static]

Enable valley capture mode.

Parameters

base	is the base address of the EPWM module.

This function enables Valley Capture mode.

Returns
None.

16.2.4.133 static void EPWM_disableValleyCapture (uint32_t *base*) [inline], [static]

Disable valley capture mode.

Parameters

base	is the base address of the EPWM module.

This function disables Valley Capture mode.

Returns
None.

16.2.4.134 static void EPWM_startValleyCapture (uint32_t *base*) [inline], [static]

Start valley capture mode.

Parameters

base	is the base address of the EPWM module.

This function starts Valley Capture sequence.

Make sure you invoke EPWM_setValleyTriggerSource with the trigger variable set to EPWM_VALLEY_TRIGGER_EVENT_SOFTWARE before calling this function.

Returns
None.

16.2.4.135 static void EPWM_setValleyTriggerSource (uint32_t *base*, **EPWM_ValleyTriggerSource** *trigger*) [inline], [static]

Set valley capture trigger.

Parameters

base	is the base address of the EPWM module.
trigger	is the Valley counter trigger.

This function sets the trigger value that initiates Valley Capture sequence

Set the number of Trigger source events for starting and stopping the valley capture using EPWM_setValleyTriggerEdgeCounts().

Returns

None.

16.2.4.136 static void EPWM_setValleyTriggerEdgeCounts (uint32_t *base,* uint16_t *startCount,* uint16_t *stopCount*) [inline], [static]

Set valley capture trigger source count.

Parameters

base	is the base address of the EPWM module.
startCount	
stopCount	This function sets the number of trigger events required to start and stop the valley capture count. Maximum values for both startCount and stopCount is 15 corresponding to the 15th edge of the trigger event.

Note: A startCount value of 0 prevents starting the valley counter. A stopCount value of 0 prevents the valley counter from stopping.

Returns

None.

16.2.4.137 static void EPWM_enableValleyHWDelay (uint32_t *base*) [inline], [static]

Enable valley switching delay.

Parameters

base	is the base address of the EPWM module.

This function enables Valley switching delay.

Returns

None.

16.2.4.138 static void EPWM_disableValleyHWDelay (uint32_t *base*) [inline], [static]

Disable valley switching delay.

Parameters

base	is the base address of the EPWM module.

This function disables Valley switching delay.

Returns

None.

16.2.4.139 static void EPWM_setValleySWDelayValue (uint32_t *base,* uint16_t *delayOffsetValue*) [inline], [static]

Set Valley delay values.

Parameters

base	is the base address of the EPWM module.
delayOffset-Value	is the software defined delay offset value.

This function sets the Valley delay value.

Returns

None.

16.2.4.140 static void EPWM_setValleyDelayDivider (uint32_t *base,* **EPWM_ValleyDelayMode** *delayMode*) [inline], [static]

Set Valley delay mode.

Parameters

base	is the base address of the EPWM module.
delayMode	is the Valley delay mode.

This function sets the Valley delay mode values.

Returns

None.

16.2.4.141 static bool EPWM_getValleyEdgeStatus (uint32_t *base,* **EPWM_ValleyCounterEdge** *edge*) [inline], [static]

Get the valley edge status bit.

Parameters

base	is the base address of the EPWM module.
edge	is the start or stop edge.

This function returns the status of the start or stop valley status depending on the value of edge. If a start or stop edge has occurred, the function returns true, if not it returns false.

Returns

Returns true if the specified edge has occurred, Returns false if the specified edge has not occurred.

References EPWM_VALLEY_COUNT_START_EDGE.

16.2.4.142 static uint16_t EPWM_getValleyCount (uint32_t *base*) [inline], [static]

Get the Valley Counter value.

Parameters

base	is the base address of the EPWM module.

This function returns the valley time base count value which is captured upon occurrence of the stop edge condition selected by EPWM_setValleyTriggerSource() and by the stopCount variable of the EPWM_setValleyTriggerEdgeCounts() function.

Returns

Returns the valley base time count.

16.2.4.143 static uint16_t EPWM_getValleyHWDelay (uint32_t *base*) [inline], [static]

Get the Valley delay value.

Parameters

base	is the base address of the EPWM module.

This function returns the hardware valley delay count.

Returns

Returns the valley delay count.

16.2.4.144 static void EPWM_enableGlobalLoad (uint32_t *base*) [inline], [static]

Enable Global shadow load mode.

Parameters

base	is the base address of the EPWM module.

This function enables Global shadow to active load mode of registers. The trigger source for loading shadow to active is determined by EPWM_setGlobalLoadTrigger() function.

Returns

None.

16.2.4.145 static void EPWM_disableGlobalLoad (uint32_t *base*) [inline], [static]

Disable Global shadow load mode.

Parameters

base	is the base address of the EPWM module.

This function disables Global shadow to active load mode of registers. Loading shadow to active is determined individually.

Returns
None.

16.2.4.146 static void EPWM_setGlobalLoadTrigger (uint32_t *base*, **EPWM_GlobalLoadTrigger** *loadTrigger*) [inline], [static]

Set the Global shadow load pulse.

Parameters

base	is the base address of the EPWM module.
loadTrigger	is the pulse that causes global shadow load.

This function sets the pulse that causes Global shadow to active load. Valid values for the loadTrigger parameter are:

- EPWM_GL_LOAD_PULSE_CNTR_ZERO - load when counter is equal to zero
- EPWM_GL_LOAD_PULSE_CNTR_PERIOD - load when counter is equal to period
- EPWM_GL_LOAD_PULSE_CNTR_ZERO_PERIOD - load when counter is equal to zero or period
- EPWM_GL_LOAD_PULSE_SYNC - load on sync event
- EPWM_GL_LOAD_PULSE_SYNC_OR_CNTR_ZERO - load on sync event or when counter is equal to zero
- EPWM_GL_LOAD_PULSE_SYNC_OR_CNTR_PERIOD - load on sync event or when counter is equal to period
- EPWM_GL_LOAD_PULSE_SYNC_CNTR_ZERO_PERIOD - load on sync event or when counter is equal to period or zero
- EPWM_GL_LOAD_PULSE_GLOBAL_FORCE - load on global force

Returns
None.

16.2.4.147 static void EPWM_setGlobalLoadEventPrescale (uint32_t *base*, uint16_t *prescalePulseCount*) [inline], [static]

Set the number of Global load pulse event counts

Parameters

base	is the base address of the EPWM module.
prescalePulseCount	is the pulse event counts.

This function sets the number of Global Load pulse events that have to occurred before a global load pulse is issued. Valid values for prescaleCount range from 0 to 7. 0 being no event (disables counter), and 7 representing 7 events.

Returns
None.

16.2.4.148 static uint16_t EPWM_getGlobalLoadEventCount (uint32_t *base*) [inline], [static]

Return the number of Global load pulse event counts

Parameters

base	is the base address of the EPWM module.

This function returns the number of Global Load pulse events that have occurred. These pulse events are set by the EPWM_setGlobalLoadTrigger() function.

Returns
None.

16.2.4.149 static void EPWM_disableGlobalLoadOneShotMode (uint32_t *base*) [inline], [static]

Enable continuous global shadow to active load.

Parameters

base	is the base address of the EPWM module.

This function enables global continuous shadow to active load. Register load happens every time the event set by the EPWM_setGlobalLoadTrigger() occurs.

Returns
None.

16.2.4.150 static void EPWM_enableGlobalLoadOneShotMode (uint32_t *base*) [inline], [static]

Enable One shot global shadow to active load.

Parameters

base	is the base address of the EPWM module.

This function enables a one time global shadow to active load. Register load happens every time the event set by the EPWM_setGlobalLoadTrigger() occurs.

Returns
None.

16.2.4.151 static void EPWM_setGlobalLoadOneShotLatch (uint32_t *base*) [inline], [static]

Set One shot global shadow to active load pulse.

Parameters

base	is the base address of the EPWM module.

This function sets a one time global shadow to active load pulse. The pulse propagates to generate a load signal if any of the events set by EPWM_setGlobalLoadTrigger() occur.

Returns

None.

16.2.4.152 static void EPWM_forceGlobalLoadOneShotEvent (uint32_t *base*) [inline], [static]

Force a software One shot global shadow to active load pulse.

Parameters

base	is the base address of the EPWM module.

This function forces a software a one time global shadow to active load pulse.

Returns

None.

16.2.4.153 static void EPWM_enableGlobalLoadRegisters (uint32_t *base*, uint16_t *loadRegister*) [inline], [static]

Enable a register to be loaded Globally.

Parameters

base	is the base address of the EPWM module.
loadRegister	is the register.

This function enables the register specified by loadRegister to be globally loaded. Valid values for loadRegister are:

- EPWM_GL_REGISTER_TBPRD_TBPRDHR - Register TBPRD:TBPRDHR
- EPWM_GL_REGISTER_CMPA_CMPAHR - Register CMPA:CMPAHR
- EPWM_GL_REGISTER_CMPB_CMPBHR - Register CMPB:CMPBHR
- EPWM_GL_REGISTER_CMPC - Register CMPC
- EPWM_GL_REGISTER_CMPD - Register CMPD
- EPWM_GL_REGISTER_DBRED_DBREDHR - Register DBRED:DBREDHR
- EPWM_GL_REGISTER_DBFED_DBFEDHR - Register DBFED:DBFEDHR
- EPWM_GL_REGISTER_DBCTL - Register DBCTL
- EPWM_GL_REGISTER_AQCTLA_AQCTLA2 - Register AQCTLA/A2
- EPWM_GL_REGISTER_AQCTLB_AQCTLB2 - Register AQCTLB/B2
- EPWM_GL_REGISTER_AQCSFRC - Register AQCSFRC

Returns

None.

16.2.4.154 static void EPWM_disableGlobalLoadRegisters (uint32_t *base*, uint16_t *loadRegister*) [inline], [static]

Disable a register to be loaded Globally.

Parameters

base	is the base address of the EPWM module.
loadRegister	is the register.

This function disables the register specified by loadRegister from being loaded globally. The shadow to active load happens as specified by the register control Valid values for loadRegister are:

- EPWM_GL_REGISTER_TBPRD_TBPRDHR - Register TBPRD:TBPRDHR
- EPWM_GL_REGISTER_CMPA_CMPAHR - Register CMPA:CMPAHR
- EPWM_GL_REGISTER_CMPB_CMPBHR - Register CMPB:CMPBHR
- EPWM_GL_REGISTER_CMPC - Register CMPC
- EPWM_GL_REGISTER_CMPD - Register CMPD
- EPWM_GL_REGISTER_DBRED_DBREDHR - Register DBRED:DBREDHR
- EPWM_GL_REGISTER_DBFED_DBFEDHR - Register DBFED:DBFEDHR
- EPWM_GL_REGISTER_DBCTL - Register DBCTL
- EPWM_GL_REGISTER_AQCTLA_AQCTLA2 - Register AQCTLA/A2
- EPWM_GL_REGISTER_AQCTLB_AQCTLB2 - Register AQCTLB/B2
- EPWM_GL_REGISTER_AQCSFRC - Register AQCSFRC

Returns

None.

16.2.4.155 void EPWM_setEmulationMode (uint32_t *base*, **EPWM_EmulationMode** *emulationMode*)

Set emulation mode

Parameters

base	is the base address of the EPWM module.
emulationMode	is the emulation mode.

This function sets the emulation behaviours of the time base counter. Valid values for emulationMode are:

- EPWM_EMULATION_STOP_AFTER_NEXT_TB - Stop after next Time Base counter increment or decrement.
- EPWM_EMULATION_STOP_AFTER_FULL_CYCLE - Stop when counter completes whole cycle.
- EPWM_EMULATION_FREE_RUN - Free run.

Returns

None.

17 HRPWM Module

17.1 HRPWM Introduction

The HRPWM (High Resolution Pulse width Modulator) API provides a set of functions for configuring and using the HRPWM module. The functions provided give access to the HRPWM module which extends the time resolution capability of the ePWM module thus achieving a finer resolution than would be attainable just using the main CPU clock. */

17.2 API Functions

Enumerations

- enum HRPWM_Channel { HRPWM_CHANNEL_A, HRPWM_CHANNEL_B }
- enum HRPWM_MEPEdgeMode { HRPWM_MEP_CTRL_DISABLE, HRPWM_MEP_CTRL_RISING_EDGE, HRPWM_MEP_CTRL_FALLING_EDGE, HRPWM_MEP_CTRL_RISING_AND_FALLING_EDGE }
- enum HRPWM_MEPCtrlMode { HRPWM_MEP_DUTY_PERIOD_CTRL, HRPWM_MEP_PHASE_CTRL }
- enum HRPWM_LoadMode { HRPWM_LOAD_ON_CNTR_ZERO, HRPWM_LOAD_ON_CNTR_PERIOD, HRPWM_LOAD_ON_CNTR_ZERO_PERIOD }
- enum HRPWM_ChannelBOutput { HRPWM_OUTPUT_ON_B_NORMAL, HRPWM_OUTPUT_ON_B_INV_A }
- enum HRPWM_SyncPulseSource { HRPWM_PWMSYNC_SOURCE_PERIOD, HRPWM_PWMSYNC_SOURCE_ZERO, HRPWM_PWMSYNC_SOURCE_COMPC_UP, HRPWM_PWMSYNC_SOURCE_COMPC_DOWN, HRPWM_PWMSYNC_SOURCE_COMPD_UP, HRPWM_PWMSYNC_SOURCE_COMPD_DOWN }
- enum HRPWM_CounterCompareModule { HRPWM_COUNTER_COMPARE_A, HRPWM_COUNTER_COMPARE_B }
- enum HRPWM_MEPDeadBandEdgeMode { HRPWM_DB_MEP_CTRL_DISABLE, HRPWM_DB_MEP_CTRL_RED, HRPWM_DB_MEP_CTRL_FED, HRPWM_DB_MEP_CTRL_RED_FED }
- enum HRPWM_LockRegisterGroup { HRPWM_REGISTER_GROUP_HRPWM, HRPWM_REGISTER_GROUP_GLOBAL_LOAD, HRPWM_REGISTER_GROUP_TRIP_ZONE, HRPWM_REGISTER_GROUP_TRIP_ZONE_CLEAR, HRPWM_REGISTER_GROUP_DIGITAL_COMPARE }

Functions

- static void HRPWM_setPhaseShift (uint32_t base, uint32_t phaseCount)

- static void HRPWM_setHiResPhaseShiftOnly (uint32_t base, uint16_t hrPhaseCount)
- static void HRPWM_setTimeBasePeriod (uint32_t base, uint32_t periodCount)
- static void HRPWM_setHiResTimeBasePeriodOnly (uint32_t base, uint16_t hrPeriodCount)
- static uint32_t HRPWM_getTimeBasePeriod (uint32_t base)
- static uint16_t HRPWM_getHiResTimeBasePeriodOnly (uint32_t base)
- static void HRPWM_setMEPEdgeSelect (uint32_t base, HRPWM_Channel channel, HRPWM_MEPEdgeMode mepEdgeMode)
- static void HRPWM_setMEPControlMode (uint32_t base, HRPWM_Channel channel, HRPWM_MEPCtrlMode mepCtrlMode)
- static void HRPWM_setCounterCompareShadowLoadEvent (uint32_t base, HRPWM_Channel channel, HRPWM_LoadMode loadEvent)
- static void HRPWM_setOutputSwapMode (uint32_t base, bool enableOutputSwap)
- static void HRPWM_setChannelBOutputPath (uint32_t base, HRPWM_ChannelBOutput outputOnB)
- static void HRPWM_enableAutoConversion (uint32_t base)
- static void HRPWM_disableAutoConversion (uint32_t base)
- static void HRPWM_enablePeriodControl (uint32_t base)
- static void HRPWM_disablePeriodControl (uint32_t base)
- static void HRPWM_enablePhaseShiftLoad (uint32_t base)
- static void HRPWM_disablePhaseShiftLoad (uint32_t base)
- static void HRPWM_setSyncPulseSource (uint32_t base, HRPWM_SyncPulseSource syncPulseSource)
- static void HRPWM_setTranslatorRemainder (uint32_t base, uint16_t trremVal)
- static void HRPWM_setCounterCompareValue (uint32_t base, HRPWM_CounterCompareModule compModule, uint32_t compCount)
- static void HRPWM_setHiResCounterCompareValueOnly (uint32_t base, HRPWM_CounterCompareModule compModule, uint16_t hrCompCount)
- static uint32_t HRPWM_getCounterCompareValue (uint32_t base, HRPWM_CounterCompareModule compModule)
- static uint16_t HRPWM_getHiResCounterCompareValueOnly (uint32_t base, HRPWM_CounterCompareModule compModule)
- static void HRPWM_setRisingEdgeDelay (uint32_t base, uint32_t redCount)
- static void HRPWM_setHiResRisingEdgeDelayOnly (uint32_t base, uint16_t hrRedCount)
- static void HRPWM_setFallingEdgeDelay (uint32_t base, uint32_t fedCount)
- static void HRPWM_setHiResFallingEdgeDelayOnly (uint32_t base, uint16_t hrFedCount)
- static void HRPWM_setMEPStep (uint32_t base, uint16_t mepCount)
- static void HRPWM_setDeadbandMEPEdgeSelect (uint32_t base, HRPWM_MEPDeadBandEdgeMode mepDBEdge)
- static void HRPWM_setRisingEdgeDelayLoadMode (uint32_t base, HRPWM_LoadMode loadEvent)
- static void HRPWM_setFallingEdgeDelayLoadMode (uint32_t base, HRPWM_LoadMode loadEvent)

17.2.1 Detailed Description

The code for this module is contained in `driverlib/hrpwm.c`, with `driverlib/hrpwm.h` containing the API declarations for use by applications.

17.2.2 Enumeration Type Documentation

17.2.2.1 enum **HRPWM_Channel**

Values that can be passed to HRPWM_setMEPEdgeSelect(), HRPWM_setMEPControlMode(), HRPWM_setCounterCompareShadowLoadEvent() as the *channel* parameter.

Enumerator

HRPWM_CHANNEL_A HRPWM A.

HRPWM_CHANNEL_B HRPWM B.

17.2.2.2 enum **HRPWM_MEPEdgeMode**

Values that can be passed to HRPWM_setMEPEdgeSelect() as the *mepEdgeMode* parameter.

Enumerator

HRPWM_MEP_CTRL_DISABLE HRPWM is disabled.

HRPWM_MEP_CTRL_RISING_EDGE MEP controls rising edge.

HRPWM_MEP_CTRL_FALLING_EDGE MEP controls falling edge.

HRPWM_MEP_CTRL_RISING_AND_FALLING_EDGE MEP controls both rising and falling edge.

17.2.2.3 enum **HRPWM_MEPCtrlMode**

Values that can be passed to HRPWM_setHRMEPCtrlMode() as the *parameter*.

Enumerator

HRPWM_MEP_DUTY_PERIOD_CTRL CMPAHR/CMPBHR or TBPRDHR controls MEP edge.

HRPWM_MEP_PHASE_CTRL TBPHSHR controls MEP edge.

17.2.2.4 enum **HRPWM_LoadMode**

Values that can be passed to HRPWM_setCounterCompareShadowLoadEvent(), HRPWM_setRisingEdgeDelayLoadMode() and HRPWM_setFallingEdgeDelayLoadMode as the *loadEvent* parameter.

Enumerator

HRPWM_LOAD_ON_CNTR_ZERO load when counter equals zero

HRPWM_LOAD_ON_CNTR_PERIOD load when counter equals period

HRPWM_LOAD_ON_CNTR_ZERO_PERIOD load when counter equals zero or period

17.2.2.5 enum **HRPWM_ChannelBOutput**

Values that can be passed to HRPWM_setChannelBOutputPath() as the *outputOnB* parameter.

Enumerator

HRPWM_OUTPUT_ON_B_NORMAL ePWMxB output is normal.

HRPWM_OUTPUT_ON_B_INV_A ePWMxB output is inverted version of ePWMxA signal

17.2.2.6 enum **HRPWM_SyncPulseSource**

Values that can be passed to HRPWM_setSyncPulseSource() as the *syncPulseSource* parameter.

Enumerator

HRPWM_PWMSYNC_SOURCE_PERIOD Counter equals Period.

HRPWM_PWMSYNC_SOURCE_ZERO Counter equals zero.

HRPWM_PWMSYNC_SOURCE_COMPC_UP Counter equals COMPC when counting up.

HRPWM_PWMSYNC_SOURCE_COMPC_DOWN Counter equals COMPC when counting down.

HRPWM_PWMSYNC_SOURCE_COMPD_UP Counter equals COMPD when counting up.

HRPWM_PWMSYNC_SOURCE_COMPD_DOWN Counter equals COMPD when counting down.

17.2.2.7 enum **HRPWM_CounterCompareModule**

Values that can be passed to HRPWM_setCounterCompareValue() as the *compModule* parameter.

Enumerator

HRPWM_COUNTER_COMPARE_A counter compare A

HRPWM_COUNTER_COMPARE_B counter compare B

17.2.2.8 enum **HRPWM_MEPDeadBandEdgeMode**

Values that can be passed to HRPWM_setDeadbandMEPEdgeSelect() as the *mepDBEdge*.

Enumerator

HRPWM_DB_MEP_CTRL_DISABLE HRPWM is disabled.

HRPWM_DB_MEP_CTRL_RED MEP controls Rising Edge Delay.

HRPWM_DB_MEP_CTRL_FED MEP controls Falling Edge Delay.

HRPWM_DB_MEP_CTRL_RED_FED MEP controls both Falling and Rising edge delay.

17.2.2.9 enum **HRPWM_LockRegisterGroup**

Values that can be passed to HRPWM_lockRegisters() as the *registerGroup* parameter.

Enumerator

HRPWM_REGISTER_GROUP_HRPWM HRPWM register group.

HRPWM_REGISTER_GROUP_GLOBAL_LOAD Global load register group.

HRPWM_REGISTER_GROUP_TRIP_ZONE Trip zone register group.

HRPWM_REGISTER_GROUP_TRIP_ZONE_CLEAR Trip zone clear group.

HRPWM_REGISTER_GROUP_DIGITAL_COMPARE Digital compare group.

17.2.3 Function Documentation

17.2.3.1 static void HRPWM_setPhaseShift (uint32_t *base*, uint32_t *phaseCount*) `[inline]`, `[static]`

Sets the consolidated phase shift value in high resolution mode.

Parameters

base	is the base address of the EPWM module.
phaseCount	is the consolidated phase shift count value.

This function sets the consolidated phase shift value i.e. both TBPHS and TBPHSHR values are configured together.

Call EPWM_enablePhaseShiftLoad & HRPWM_enableHRPhaseShiftLoad() functions to enable loading of the phaseCount in high resolution mode.

Note: phaseCount is a 24-bit value. **Note:** For configuring TBPHS = 0x3C, TBPHSHR = 0x2; phaseCount = 0x3C02

Returns

None.

17.2.3.2 static void HRPWM_setHiResPhaseShiftOnly (uint32_t *base,* uint16_t *hrPhaseCount*) [inline], [static]

Sets only the high resolution phase shift value.

Parameters

base	is the base address of the EPWM module.
hrPhaseCount	is the high resolution phase shift count value.

This function sets only the high resolution phase shift(TBPHSHR) value. Call the HRPWM_enableHRPhaseShiftLoad() function to enable loading of the hrPhaseCount.

Note: hrPhaseCount is an 8-bit value.

Returns

None.

17.2.3.3 static void HRPWM_setTimeBasePeriod (uint32_t *base,* uint32_t *periodCount*) [inline], [static]

Sets the consolidated period of time base counter used in HR mode.

Parameters

base	is the base address of the EPWM module.
periodCount	is the consolidated period count value.

This function sets the consolidated period of time base counter value (TBPRD:TBPRDHR) required in high resolution mode.

User should map the desired period or frequency of the waveform into the correct periodCount.

Note: periodCount is a 24 bit value. **Note:** For configuring TBPRD = 0x3C, TBPRDHR = 0xA; periodCount = 0x3C0A

Returns

None.

17.2.3.4 static void HRPWM_setHiResTimeBasePeriodOnly (uint32_t *base*, uint16_t *hrPeriodCount*) [inline], [static]

Sets only the high resolution time base counter.

Parameters

base	is the base address of the EPWM module.
hrPeriodCount	is the high resolution period count value.

This function sets only the high resolution time base counter(TBPRDHR) value.

User should map the desired period or frequency of the waveform into the correct hrPeriodCount.

Note: hrPeriodCount is an 8-bit value.

Returns
None.

17.2.3.5 static uint32_t HRPWM_getTimeBasePeriod (uint32_t *base*) [inline], [static]

Gets the consolidated time base period count used in HR mode

Parameters

base	is the base address of the EPWM module.

This function gets the consolidated time base period(TBPRD:TBPRDHR) value used in high resolution mode.

Returns
The consolidated time base period count value.

17.2.3.6 static uint16_t HRPWM_getHiResTimeBasePeriodOnly (uint32_t *base*) [inline], [static]

Gets the only the high resolution time base period count.

Parameters

base	is the base address of the EPWM module.

This function gets only the high resolution time base period(TBPRDHR) value.

Returns
The high resolution time base period count value.

17.2.3.7 static void HRPWM_setMEPEdgeSelect (uint32_t *base,* **HRPWM_Channel** *channel,* **HRPWM_MEPEdgeMode** *mepEdgeMode*) [inline], [static]

Sets the high resolution edge controlled by MEP (Micro Edge Positioner).

Parameters

base	is the base address of the EPWM module.
channel	is high resolution period module.
mepEdgeMode	edge of the PWM that is controlled by MEP (Micro Edge Positioner).

This function sets the edge of the PWM that is controlled by MEP (Micro Edge Positioner). Valid values for the parameters are:

- channel
  - HRPWM_CHANNEL_A - HRPWM A
  - HRPWM_CHANNEL_B - HRPWM B
- mepEdgeMode
  - HRPWM_MEP_CTRL_DISABLE - HRPWM is disabled
  - HRPWM_MEP_CTRL_RISING_EDGE - MEP (Micro Edge Positioner) controls rising edge.
  - HRPWM_MEP_CTRL_FALLING_EDGE - MEP (Micro Edge Positioner) controls falling edge.
  - HRPWM_MEP_CTRL_RISING_AND_FALLING_EDGE - MEP (Micro Edge Positioner) controls both edges.

Returns
None.

17.2.3.8 static void HRPWM_setMEPControlMode (uint32_t *base*, **HRPWM_Channel** *channel*, **HRPWM_MEPCtrlMode** *mepCtrlMode*) `[inline]`, `[static]`

Sets the MEP (Micro Edge Positioner) control mode.

Parameters

base	is the base address of the EPWM module.
channel	is high resolution period module.
mepCtrlMode	is the MEP (Micro Edge Positioner) control mode.

This function sets the mode (register type) the MEP (Micro Edge Positioner) will control. Valid values for the parameters are:

- channel
  - HRPWM_CHANNEL_A - HRPWM A
  - HRPWM_CHANNEL_B - HRPWM B
- mepCtrlMode
  - HRPWM_MEP_DUTY_PERIOD_CTRL - MEP (Micro Edge Positioner) is controlled by value of CMPAHR/ CMPBHR(depending on the value of channel) or TBPRDHR.
  - HRPWM_MEP_PHASE_CTRL - MEP (Micro Edge Positioner) is controlled by TBPHSHR.

Returns
None.

17.2.3.9 static void HRPWM_setCounterCompareShadowLoadEvent (uint32_t *base*, **HRPWM_Channel** *channel*, **HRPWM_LoadMode** *loadEvent*) [inline], [static]

Sets the high resolution comparator load mode.

Parameters

base	is the base address of the EPWM module.
channel	is high resolution period module.
loadEvent	is the MEP (Micro Edge Positioner) control mode.

This function sets the shadow load mode of the high resolution comparator. The function sets the COMPA or COMPB register depending on the channel variable. Valid values for the parameters are:

- channel
  - HRPWM_CHANNEL_A - HRPWM A
  - HRPWM_CHANNEL_B - HRPWM B
- loadEvent
  - HRPWM_LOAD_ON_CNTR_ZERO - load when counter equals zero
  - HRPWM_LOAD_ON_CNTR_PERIOD - load when counter equals period
  - HRPWM_LOAD_ON_CNTR_ZERO_PERIOD - load when counter equals zero or period

Returns

None.

17.2.3.10 static void HRPWM_setOutputSwapMode (uint32_t *base,* bool *enableOutputSwap*) `[inline]`, `[static]`

Sets the high resolution output swap mode.

Parameters

base	is the base address of the EPWM module.
enableOutputSwap	is the output swap flag.

This function sets the HRPWM output swap mode. If enableOutputSwap is true, ePWMxA signal appears on ePWMxB output and ePWMxB signal appears on ePWMxA output. If it is false ePWMxA and ePWMxB outputs are unchanged.

Returns

None.

17.2.3.11 static void HRPWM_setChannelBOutputPath (uint32_t *base,* **HRPWM_ChannelBOutput** *outputOnB*) `[inline]`, `[static]`

Sets the high resolution output on ePWMxB

Parameters

base	is the base address of the EPWM module.

outputOnB	is the output signal on ePWMxB.

This function sets the HRPWM output signal on ePWMxB. If outputOnB is HRPWM_OUTPUT_ON_B_INV_A, ePWMxB output is an inverted version of ePWMxA. If outputOnB is HRPWM_OUTPUT_ON_B_NORMAL, ePWMxB output is ePWMxB.

Returns
None.

17.2.3.12 static void HRPWM_enableAutoConversion (uint32_t *base*) [inline], [static]

Enables MEP (Micro Edge Positioner) automatic scale mode.

Parameters

base	is the base address of the EPWM module.

This function enables the MEP (Micro Edge Positioner) to automatically scale HRMSTEP.

Returns
None.

17.2.3.13 static void HRPWM_disableAutoConversion (uint32_t *base*) [inline], [static]

Disables MEP automatic scale mode.

Parameters

base	is the base address of the EPWM module.

This function disables the MEP (Micro Edge Positioner) from automatically scaling HRMSTEP.

Returns
None.

17.2.3.14 static void HRPWM_enablePeriodControl (uint32_t *base*) [inline], [static]

Enable high resolution period feature.

Parameters

base	is the base address of the EPWM module.

This function enables the high resolution period feature.

Returns
None.

17.2.3.15 static void HRPWM_disablePeriodControl (uint32_t *base*) [inline], [static]

Disable high resolution period feature.

Parameters

base	is the base address of the EPWM module.

This function disables the high resolution period feature.

Returns
None.

17.2.3.16 static void HRPWM_enablePhaseShiftLoad (uint32_t *base*) [inline], [static]

Enable high resolution phase load

Parameters

base	is the base address of the EPWM module.

This function enables loading of high resolution phase shift value which is set by the function HRPWM_setPhaseShift().

Returns
None.

17.2.3.17 static void HRPWM_disablePhaseShiftLoad (uint32_t *base*) [inline], [static]

Disable high resolution phase load

Parameters

base	is the base address of the EPWM module.

This function disables loading of high resolution phase shift value.

Returns

17.2.3.18 static void HRPWM_setSyncPulseSource (uint32_t *base,* **HRPWM_SyncPulseSource** *syncPulseSource*) [inline], [static]

Set high resolution PWMSYNC source.

Parameters

base	is the base address of the EPWM module.
syncPulseSource	is the PWMSYNC source.

This function sets the high resolution PWMSYNC pulse source. Valid values for syncPulseSource are:

- HRPWM_PWMSYNC_SOURCE_PERIOD - Counter equals Period.

- HRPWM_PWMSYNC_SOURCE_ZERO - Counter equals zero.
- HRPWM_PWMSYNC_SOURCE_COMPC_UP - Counter equals COMPC when counting up.
- HRPWM_PWMSYNC_SOURCE_COMPC_DOWN - Counter equals COMPC when counting down.
- HRPWM_PWMSYNC_SOURCE_COMPD_UP - Counter equals COMPD when counting up.
- HRPWM_PWMSYNC_SOURCE_COMPD_DOWN - Counter equals COMPD when counting down.

Returns
None.

References HRPWM_PWMSYNC_SOURCE_COMPC_UP.

17.2.3.19 static void HRPWM_setTranslatorRemainder (uint32_t *base*, uint16_t *trremVal*) [inline], [static]

Sets the Translator Remainder value.

Parameters

base	is the base address of the EPWM module.
trremVal	is the translator remainder value.

This function sets the Translator Remainder value.

Returns
None.

17.2.3.20 static void HRPWM_setCounterCompareValue (uint32_t *base*, **HRPWM_CounterCompareModule** *compModule*, uint32_t *compCount*) [inline], [static]

Sets the consolidated counter compare values in HR mode.

Parameters

base	is the base address of the EPWM module.
compModule	is the Counter Compare module.
compCount	is the consolidated counter compare count value.

This function sets the consolidated counter compare(CMPx:CMPxHR) value required in high resolution mode for counter compare registers. Valid values for compModule are:

- HRPWM_COUNTER_COMPARE_A - counter compare A.
- HRPWM_COUNTER_COMPARE_B - counter compare B.

Note: compCount is a 24 bit value. **Note:** For configuring CMPA = 0xB4, CMPAHR = 0x64; value of compCount = 0xB464

Returns
None.

References HRPWM_COUNTER_COMPARE_A.

17.2.3.21 static void HRPWM_setHiResCounterCompareValueOnly (uint32_t *base*, **HRPWM_CounterCompareModule** *compModule*, uint16_t *hrCompCount*) [inline], [static]

Sets only the high resolution counter compare value.

Parameters

base	is the base address of the EPWM module.
compModule	is the Counter Compare module.
hrCompCount	is the high resolution counter compare count value.

This function sets the high resolution counter compare value(CMPxHR) for counter compare registers. Valid values for compModule are:

- HRPWM_COUNTER_COMPARE_A - counter compare A.
- HRPWM_COUNTER_COMPARE_B - counter compare B.

Note: hrCompCount is an 8-bit value.

Returns
None.

References HRPWM_COUNTER_COMPARE_A.

17.2.3.22 static uint32_t HRPWM_getCounterCompareValue (uint32_t *base*, **HRPWM_CounterCompareModule** *compModule*) [inline], [static]

Gets the consolidated counter compare values.

Parameters

base	is the base address of the EPWM module.
compModule	is the Counter Compare module value.

This function gets the consolidated counter compare(CMPx:CMPxHR) value used in high resolution for the counter compare module specified. Valid values for compModule are:

- HRPWM_COUNTER_COMPARE_A - counter compare A.
- HRPWM_COUNTER_COMPARE_B - counter compare B.

Returns
None.

References HRPWM_COUNTER_COMPARE_A.

17.2.3.23 static uint16_t HRPWM_getHiResCounterCompareValueOnly (uint32_t *base*, **HRPWM_CounterCompareModule** *compModule*) [inline], [static]

Gets only the high resolution counter compare values.

Parameters

base	is the base address of the EPWM module.
compModule	is the Counter Compare module value.

This function gets only the high resolution counter compare(CMPxHR) value for the counter compare module specified. Valid values for compModule are:

- HRPWM_COUNTER_COMPARE_A - counter compare A.

- HRPWM_COUNTER_COMPARE_B - counter compare B.

Returns
None.

References HRPWM_COUNTER_COMPARE_A.

17.2.3.24 static void HRPWM_setRisingEdgeDelay (uint32_t *base,* uint32_t *redCount*) [inline], [static]

Sets the consolidated RED count in high resolution mode.

Parameters

base	is the base address of the EPWM module.
redCount	is the high resolution RED count.

This function sets the consolidated RED (Rising Edge Delay) count (DBRED:DBREDHR) value used in high resolution mode. The value of redCount should be less than 0x200000.

Note: redCount is a 21 bit value. **Note:** For configuring DBRED = 0x4, DBREDHR = 0x1; value of redCount = ((0x4 << 7) | 0x1) = 0x201

Returns
None.

17.2.3.25 static void HRPWM_setHiResRisingEdgeDelayOnly (uint32_t *base,* uint16_t *hrRedCount*) [inline], [static]

Sets the high resolution RED count only.

Parameters

base	is the base address of the EPWM module.
hrRedCount	is the high resolution RED count.

This function sets only the high resolution RED (Rising Edge Delay) count(DBREDHR) value. The value of hrRedCount should be less than 128.

Note: hrRedCount is a 7-bit value.

Returns
None.

17.2.3.26 static void HRPWM_setFallingEdgeDelay (uint32_t *base,* uint32_t *fedCount*) [inline], [static]

Sets the consolidated FED value in high resolution mode.

Parameters

base	is the base address of the EPWM module.
fedCount	is the high resolution FED count.

This function sets the consolidated FED (Falling Edge Delay) count (DBFED: DBFEDHR) value used in high resolution mode. The value of fedCount should be less than 0x200000.

Note: fedCount is a 21 bit value. **Note:** For configuring DBFED = 0x4, DBFEDHR = 0x1; value of fedCount = ((0x4 << 7) | 0x1) = 0x201

Returns
None.

17.2.3.27 static void HRPWM_setHiResFallingEdgeDelayOnly (uint32_t *base,* uint16_t *hrFedCount*) [inline], [static]

Sets high resolution FED count only.

Parameters

base	is the base address of the EPWM module.
hrFedCount	is the high resolution FED count.

This function sets only the high resolution FED (Falling Edge Delay) count (DBFEDHR)value. The value of hrFedCount should be less than 128.

Note: hrFedCount is a 7-bit value.

Returns
None.

17.2.3.28 static void HRPWM_setMEPStep (uint32_t *base,* uint16_t *mepCount*) [inline], [static]

Set high resolution MEP (Micro Edge Positioner) step.

Parameters

base	is the base address of the EPWM module.
mepCount	is the high resolution MEP (Micro Edge Positioner) step count.

This function sets the high resolution MEP (Micro Edge Positioner) step count. The maximum value for the MEP count step is 255.

Returns
None.

17.2.3.29 static void HRPWM_setDeadbandMEPEdgeSelect (uint32_t *base,* **HRPWM_MEPDeadBandEdgeMode** *mepDBEdge*) [inline], [static]

Set high resolution Dead Band MEP (Micro Edge Positioner) control.

Parameters

base	is the base address of the EPWM module.
mepDBEdge	is the high resolution MEP (Micro Edge Positioner) control edge.

This function sets the high resolution Dead Band edge that the MEP (Micro Edge Positioner) controls Valid values for mepDBEdge are:

- HRPWM_DB_MEP_CTRL_DISABLE - HRPWM is disabled
- HRPWM_DB_MEP_CTRL_RED - MEP (Micro Edge Positioner) controls Rising Edge Delay
- HRPWM_DB_MEP_CTRL_FED - MEP (Micro Edge Positioner) controls Falling Edge Delay
- HRPWM_DB_MEP_CTRL_RED_FED - MEP (Micro Edge Positioner) controls both Falling and Rising edge delays

Returns
None.

17.2.3.30 static void HRPWM_setRisingEdgeDelayLoadMode (uint32_t *base,* **HRPWM_LoadMode** *loadEvent*) [inline], [static]

Set the high resolution Dead Band RED load mode.

Parameters

base	is the base address of the EPWM module.
loadEvent	is the shadow to active load event.

This function sets the high resolution Rising Edge Delay(RED)Dead Band count load mode. Valid values for loadEvent are:

- HRPWM_LOAD_ON_CNTR_ZERO - load when counter equals zero.
- HRPWM_LOAD_ON_CNTR_PERIOD - load when counter equals period
- HRPWM_LOAD_ON_CNTR_ZERO_PERIOD - load when counter equals zero or period.

Returns
None.

17.2.3.31 static void HRPWM_setFallingEdgeDelayLoadMode (uint32_t *base,* **HRPWM_LoadMode** *loadEvent*) [inline], [static]

Set the high resolution Dead Band FED load mode.

Parameters

base	is the base address of the EPWM module.
loadEvent	is the shadow to active load event.

This function sets the high resolution Falling Edge Delay(FED) Dead Band count load mode. Valid values for loadEvent are:

- HRPWM_LOAD_ON_CNTR_ZERO - load when counter equals zero.

- HRPWM_LOAD_ON_CNTR_PERIOD - load when counter equals period
- HRPWM_LOAD_ON_CNTR_ZERO_PERIOD - load when counter equals zero or period.

Returns

None.

18 EQEP Module

18.1 EQEP Introduction

The enhanced quadrature encoder pulse (eQEP) API provides a set of functions to configure an interface to an encoder. The functions provide the ability to configure the device's eQEP module to properly decode incoming pulse signals, to configure module outputs, and to get direction, position, and speed information. There are also APIs to setup the possible interrupt events that the module can generate.

18.2 API Functions

Enumerations

- enum EQEP_PositionResetMode { EQEP_POSITION_RESET_IDX, EQEP_POSITION_RESET_MAX_POS, EQEP_POSITION_RESET_1ST_IDX, EQEP_POSITION_RESET_UNIT_TIME_OUT }
- enum EQEP_CAPCLKPrescale { EQEP_CAPTURE_CLK_DIV_1, EQEP_CAPTURE_CLK_DIV_2, EQEP_CAPTURE_CLK_DIV_4, EQEP_CAPTURE_CLK_DIV_8, EQEP_CAPTURE_CLK_DIV_16, EQEP_CAPTURE_CLK_DIV_32, EQEP_CAPTURE_CLK_DIV_64, EQEP_CAPTURE_CLK_DIV_128 }
- enum EQEP_UPEVNTPrescale { EQEP_UNIT_POS_EVNT_DIV_1, EQEP_UNIT_POS_EVNT_DIV_2, EQEP_UNIT_POS_EVNT_DIV_4, EQEP_UNIT_POS_EVNT_DIV_8, EQEP_UNIT_POS_EVNT_DIV_16, EQEP_UNIT_POS_EVNT_DIV_32, EQEP_UNIT_POS_EVNT_DIV_64, EQEP_UNIT_POS_EVNT_DIV_128, EQEP_UNIT_POS_EVNT_DIV_256, EQEP_UNIT_POS_EVNT_DIV_512, EQEP_UNIT_POS_EVNT_DIV_1024, EQEP_UNIT_POS_EVNT_DIV_2048 }
- enum EQEP_EmulationMode { EQEP_EMULATIONMODE_STOPIMMEDIATELY, EQEP_EMULATIONMODE_STOPATROLLOVER, EQEP_EMULATIONMODE_RUNFREE }

Functions

- static void EQEP_enableModule (uint32_t base)
- static void EQEP_disableModule (uint32_t base)
- static void EQEP_setDecoderConfig (uint32_t base, uint16_t config)
- static void EQEP_setPositionCounterConfig (uint32_t base, EQEP_PositionResetMode mode, uint32_t maxPosition)
- static uint32_t EQEP_getPosition (uint32_t base)
- static void EQEP_setPosition (uint32_t base, uint32_t position)
- static int16_t EQEP_getDirection (uint32_t base)
- static void EQEP_enableInterrupt (uint32_t base, uint16_t intFlags)
- static void EQEP_disableInterrupt (uint32_t base, uint16_t intFlags)

- static uint16_t EQEP_getInterruptStatus (uint32_t base)
- static void EQEP_clearInterruptStatus (uint32_t base, uint16_t intFlags)
- static void EQEP_forceInterrupt (uint32_t base, uint16_t intFlags)
- static bool EQEP_getError (uint32_t base)
- static uint16_t EQEP_getStatus (uint32_t base)
- static void EQEP_clearStatus (uint32_t base, uint16_t statusFlags)
- static void EQEP_setCaptureConfig (uint32_t base, EQEP_CAPCLKPrescale capPrescale, EQEP_UPEVNTPrescale evntPrescale)
- static void EQEP_enableCapture (uint32_t base)
- static void EQEP_disableCapture (uint32_t base)
- static uint16_t EQEP_getCapturePeriod (uint32_t base)
- static uint16_t EQEP_getCaptureTimer (uint32_t base)
- static void EQEP_enableCompare (uint32_t base)
- static void EQEP_disableCompare (uint32_t base)
- static void EQEP_setComparePulseWidth (uint32_t base, uint16_t cycles)
- static void EQEP_loadUnitTimer (uint32_t base, uint32_t period)
- static void EQEP_enableUnitTimer (uint32_t base, uint32_t period)
- static void EQEP_disableUnitTimer (uint32_t base)
- static void EQEP_enableWatchdog (uint32_t base, uint16_t period)
- static void EQEP_disableWatchdog (uint32_t base)
- static void EQEP_setWatchdogTimerValue (uint32_t base, uint16_t value)
- static uint16_t EQEP_getWatchdogTimerValue (uint32_t base)
- static void EQEP_setPositionInitMode (uint32_t base, uint16_t initMode)
- static void EQEP_setSWPositionInit (uint32_t base, bool initialize)
- static void EQEP_setInitialPosition (uint32_t base, uint32_t position)
- static void EQEP_setLatchMode (uint32_t base, uint32_t latchMode)
- static uint32_t EQEP_getIndexPositionLatch (uint32_t base)
- static uint32_t EQEP_getStrobePositionLatch (uint32_t base)
- static uint32_t EQEP_getPositionLatch (uint32_t base)
- static uint16_t EQEP_getCaptureTimerLatch (uint32_t base)
- static uint16_t EQEP_getCapturePeriodLatch (uint32_t base)
- static void EQEP_setEmulationMode (uint32_t base, EQEP_EmulationMode emuMode)
- void EQEP_setCompareConfig (uint32_t base, uint16_t config, uint32_t compareValue, uint16_t cycles)
- void EQEP_setInputPolarity (uint32_t base, bool invertQEPA, bool invertQEPB, bool invertIndex, bool invertStrobe)

18.2.1 Detailed Description

The code for this module is contained in `driverlib/eqep.c`, with `driverlib/eqep.h` containing the API declarations for use by applications.

18.2.2 Enumeration Type Documentation

18.2.2.1 enum **EQEP_PositionResetMode**

Values that can be passed to EQEP_setPositionCounterConfig() as the *mode* parameter.

Enumerator

EQEP_POSITION_RESET_IDX Reset position on index pulse.

EQEP_POSITION_RESET_MAX_POS Reset position on maximum position.

EQEP_POSITION_RESET_1ST_IDX Reset position on the first index pulse.

EQEP_POSITION_RESET_UNIT_TIME_OUT Reset position on a unit time event.

18.2.2.2 enum **EQEP_CAPCLKPrescale**

Values that can be passed to EQEP_setCaptureConfig() as the *capPrescale* parameter. CAPCLK is the capture timer clock frequency.

Enumerator

EQEP_CAPTURE_CLK_DIV_1 CAPCLK = SYSCLKOUT/1.
EQEP_CAPTURE_CLK_DIV_2 CAPCLK = SYSCLKOUT/2.
EQEP_CAPTURE_CLK_DIV_4 CAPCLK = SYSCLKOUT/4.
EQEP_CAPTURE_CLK_DIV_8 CAPCLK = SYSCLKOUT/8.
EQEP_CAPTURE_CLK_DIV_16 CAPCLK = SYSCLKOUT/16.
EQEP_CAPTURE_CLK_DIV_32 CAPCLK = SYSCLKOUT/32.
EQEP_CAPTURE_CLK_DIV_64 CAPCLK = SYSCLKOUT/64.
EQEP_CAPTURE_CLK_DIV_128 CAPCLK = SYSCLKOUT/128.

18.2.2.3 enum **EQEP_UPEVNTPrescale**

Values that can be passed to EQEP_setCaptureConfig() as the *evntPrescale* parameter. UPEVNT is the unit position event frequency.

Enumerator

EQEP_UNIT_POS_EVNT_DIV_1 UPEVNT = QCLK/1.
EQEP_UNIT_POS_EVNT_DIV_2 UPEVNT = QCLK/2.
EQEP_UNIT_POS_EVNT_DIV_4 UPEVNT = QCLK/4.
EQEP_UNIT_POS_EVNT_DIV_8 UPEVNT = QCLK/8.
EQEP_UNIT_POS_EVNT_DIV_16 UPEVNT = QCLK/16.
EQEP_UNIT_POS_EVNT_DIV_32 UPEVNT = QCLK/32.
EQEP_UNIT_POS_EVNT_DIV_64 UPEVNT = QCLK/64.
EQEP_UNIT_POS_EVNT_DIV_128 UPEVNT = QCLK/128.
EQEP_UNIT_POS_EVNT_DIV_256 UPEVNT = QCLK/256.
EQEP_UNIT_POS_EVNT_DIV_512 UPEVNT = QCLK/512.
EQEP_UNIT_POS_EVNT_DIV_1024 UPEVNT = QCLK/1024.
EQEP_UNIT_POS_EVNT_DIV_2048 UPEVNT = QCLK/2048.

18.2.2.4 enum **EQEP_EmulationMode**

Values that can be passed to EQEP_setEmulationMode() as the *emuMode* parameter.

Enumerator

EQEP_EMULATIONMODE_STOPIMMEDIATELY Counters stop immediately.
EQEP_EMULATIONMODE_STOPATROLLOVER Counters stop at period rollover.
EQEP_EMULATIONMODE_RUNFREE Counter unaffected by suspend.

18.2.3 Function Documentation

18.2.3.1 static void EQEP_enableModule (uint32_t *base*) [inline], [static]

Enables the eQEP module.

Parameters

base	is the base address of the eQEP module.

This function enables operation of the enhanced quadrature encoder pulse (eQEP) module. The module must be configured before it is enabled.

See Also
EQEP_setConfig()

Returns
None.

18.2.3.2 static void EQEP_disableModule (uint32_t *base*) [inline], [static]

Disables the eQEP module.

Parameters

base	is the base address of the enhanced quadrature encoder pulse (eQEP) module

This function disables operation of the eQEP module.

Returns
None.

18.2.3.3 static void EQEP_setDecoderConfig (uint32_t *base,* uint16_t *config*) [inline], [static]

Configures eQEP module's quadrature decoder unit.

Parameters

base	is the base address of the eQEP module.
config	is the configuration for the eQEP module decoder unit.

This function configures the operation of the eQEP module's quadrature decoder unit. The *config* parameter provides the configuration of the decoder and is the logical OR of several values:

- **EQEP_CONFIG_2X_RESOLUTION** or **EQEP_CONFIG_1X_RESOLUTION** specify if both rising and falling edges should be counted or just rising edges.
- **EQEP_CONFIG_QUADRATURE**, **EQEP_CONFIG_CLOCK_DIR**, **EQEP_CONFIG_UP_COUNT**, or **EQEP_CONFIG_DOWN_COUNT** specify if quadrature signals are being provided on QEPA and QEPB, if a direction signal and a clock are being provided, or if the direction should be hard-wired for a single direction with QEPA used for input.
- **EQEP_CONFIG_NO_SWAP** or **EQEP_CONFIG_SWAP** to specify if the signals provided on QEPA and QEPB should be swapped before being processed.

Returns
None.

18.2.3.4 static void EQEP_setPositionCounterConfig (uint32_t *base*, **EQEP_PositionResetMode** *mode*, uint32_t *maxPosition*) `[inline]`, `[static]`

Configures eQEP module position counter unit.

Parameters

base	is the base address of the eQEP module.
mode	is the configuration for the eQEP module position counter.
maxPosition	specifies the maximum position value.

This function configures the operation of the eQEP module position counter. The *mode* parameter determines the event on which the position counter gets reset. It should be passed one of the following values: **EQEP_POSITION_RESET_IDX**, **EQEP_POSITION_RESET_MAX_POS**, **EQEP_POSITION_RESET_1ST_IDX**, or **EQEP_POSITION_RESET_UNIT_TIME_OUT**.

maxPosition is the maximum value of the position counter and is the value used to reset the position capture when moving in the reverse (negative) direction.

Returns
None.

18.2.3.5 static uint32_t EQEP_getPosition (uint32_t *base*) [inline], [static]

Gets the current encoder position.

Parameters

base	is the base address of the eQEP module.

This function returns the current position of the encoder. Depending upon the configuration of the encoder, and the incident of an index pulse, this value may or may not contain the expected data (that is, if in reset on index mode, if an index pulse has not been encountered, the position counter is not yet aligned with the index pulse).

Returns
The current position of the encoder.

18.2.3.6 static void EQEP_setPosition (uint32_t *base,* uint32_t *position*) [inline], [static]

Sets the current encoder position.

Parameters

base	is the base address of the eQEP module.
position	is the new position for the encoder.

This function sets the current position of the encoder; the encoder position is then measured relative to this value.

Returns
None.

18.2.3.7 static int16_t EQEP_getDirection (uint32_t *base*) [inline], [static]

Gets the current direction of rotation.

Parameters

base	is the base address of the eQEP module.

This function returns the current direction of rotation. In this case, current means the most recently detected direction of the encoder; it may not be presently moving but this is the direction it last moved before it stopped.

Returns

Returns 1 if moving in the forward direction or -1 if moving in the reverse direction.

18.2.3.8 static void EQEP_enableInterrupt (uint32_t *base,* uint16_t *intFlags*) [inline], [static]

Enables individual eQEP module interrupt sources.

Parameters

base	is the base address of the eQEP module.
intFlags	is a bit mask of the interrupt sources to be enabled.

This function enables eQEP module interrupt sources. The *intFlags* parameter can be any of the following values OR'd together:

- **EQEP_INT_POS_CNT_ERROR** - Position counter error
- **EQEP_INT_PHASE_ERROR** - Quadrature phase error
- **EQEP_INT_DIR_CHANGE** - Quadrature direction change
- **EQEP_INT_WATCHDOG** - Watchdog time-out
- **EQEP_INT_UNDERFLOW** - Position counter underflow
- **EQEP_INT_OVERFLOW** - Position counter overflow
- **EQEP_INT_POS_COMP_READY** - Position-compare ready
- **EQEP_INT_POS_COMP_MATCH** - Position-compare match
- **EQEP_INT_STROBE_EVNT_LATCH** - Strobe event latch
- **EQEP_INT_INDEX_EVNT_LATCH** - Index event latch
- **EQEP_INT_UNIT_TIME_OUT** - Unit time-out

Returns

None.

18.2.3.9 static void EQEP_disableInterrupt (uint32_t *base,* uint16_t *intFlags*) [inline], [static]

Disables individual eQEP module interrupt sources.

Parameters

base	is the base address of the eQEP module.
intFlags	is a bit mask of the interrupt sources to be disabled.

This function disables eQEP module interrupt sources. The *intFlags* parameter can be any of the following values OR'd together:

- **EQEP_INT_POS_CNT_ERROR** - Position counter error
- **EQEP_INT_PHASE_ERROR** - Quadrature phase error
- **EQEP_INT_DIR_CHANGE** - Quadrature direction change
- **EQEP_INT_WATCHDOG** - Watchdog time-out
- **EQEP_INT_UNDERFLOW** - Position counter underflow
- **EQEP_INT_OVERFLOW** - Position counter overflow
- **EQEP_INT_POS_COMP_READY** - Position-compare ready
- **EQEP_INT_POS_COMP_MATCH** - Position-compare match
- **EQEP_INT_STROBE_EVNT_LATCH** - Strobe event latch
- **EQEP_INT_INDEX_EVNT_LATCH** - Index event latch
- **EQEP_INT_UNIT_TIME_OUT** - Unit time-out

Returns

None.

18.2.3.10 static uint16_t EQEP_getInterruptStatus (uint32_t *base*) `[inline]`, `[static]`

Gets the current interrupt status.

Parameters

base	is the base address of the eQEP module.

This function returns the interrupt status for the eQEP module module.

Returns

Returns the current interrupt status, enumerated as a bit field of the following values:

- **EQEP_INT_GLOBAL** - Global interrupt flag
- **EQEP_INT_POS_CNT_ERROR** - Position counter error
- **EQEP_INT_PHASE_ERROR** - Quadrature phase error
- **EQEP_INT_DIR_CHANGE** - Quadrature direction change
- **EQEP_INT_WATCHDOG** - Watchdog time-out
- **EQEP_INT_UNDERFLOW** - Position counter underflow
- **EQEP_INT_OVERFLOW** - Position counter overflow
- **EQEP_INT_POS_COMP_READY** - Position-compare ready
- **EQEP_INT_POS_COMP_MATCH** - Position-compare match
- **EQEP_INT_STROBE_EVNT_LATCH** - Strobe event latch
- **EQEP_INT_INDEX_EVNT_LATCH** - Index event latch
- **EQEP_INT_UNIT_TIME_OUT** - Unit time-out

18.2.3.11 static void EQEP_clearInterruptStatus (uint32_t *base,* uint16_t *intFlags*) [inline], [static]

Clears eQEP module interrupt sources.

Parameters

base	is the base address of the eQEP module.
intFlags	is a bit mask of the interrupt sources to be cleared.

This function clears eQEP module interrupt flags. The *intFlags* parameter can be any of the following values OR'd together:

- **EQEP_INT_GLOBAL** - Global interrupt flag
- **EQEP_INT_POS_CNT_ERROR** - Position counter error
- **EQEP_INT_PHASE_ERROR** - Quadrature phase error
- **EQEP_INT_DIR_CHANGE** - Quadrature direction change
- **EQEP_INT_WATCHDOG** - Watchdog time-out
- **EQEP_INT_UNDERFLOW** - Position counter underflow
- **EQEP_INT_OVERFLOW** - Position counter overflow
- **EQEP_INT_POS_COMP_READY** - Position-compare ready
- **EQEP_INT_POS_COMP_MATCH** - Position-compare match
- **EQEP_INT_STROBE_EVNT_LATCH** - Strobe event latch
- **EQEP_INT_INDEX_EVNT_LATCH** - Index event latch
- **EQEP_INT_UNIT_TIME_OUT** - Unit time-out

Note that the **EQEP_INT_GLOBAL** value is the global interrupt flag. In order to get any further eQEP interrupts, this flag must be cleared.

Returns
None.

18.2.3.12 static void EQEP_forceInterrupt (uint32_t *base,* uint16_t *intFlags*) [inline], [static]

Forces individual eQEP module interrupts.

Parameters

base	is the base address of the eQEP module.
intFlags	is a bit mask of the interrupt sources to be forced.

This function forces eQEP module interrupt flags. The *intFlags* parameter can be any of the following values OR'd together:

- **EQEP_INT_POS_CNT_ERROR**
- **EQEP_INT_PHASE_ERROR**
- **EQEP_INT_DIR_CHANGE**
- **EQEP_INT_WATCHDOG**
- **EQEP_INT_UNDERFLOW**
- **EQEP_INT_OVERFLOW**
- **EQEP_INT_POS_COMP_READY**
- **EQEP_INT_POS_COMP_MATCH**

- **EQEP_INT_STROBE_EVNT_LATCH**
- **EQEP_INT_INDEX_EVNT_LATCH**
- **EQEP_INT_UNIT_TIME_OUT**

Returns
None.

18.2.3.13 static bool EQEP_getError (uint32_t *base*) [inline], [static]

Gets the encoder error indicator.

Parameters

base	is the base address of the eQEP module.

This function returns the error indicator for the eQEP module. It is an error for both of the signals of the quadrature input to change at the same time.

Returns
Returns **true** if an error has occurred and **false** otherwise.

18.2.3.14 static uint16_t EQEP_getStatus (uint32_t *base*) [inline], [static]

Returns content of the eQEP module status register

Parameters

base	is the base address of the eQEP module.

This function returns the contents of the status register. The value it returns is an OR of the following values:

- **EQEP_STS_UNIT_POS_EVNT** - Unit position event detected
- **EQEP_STS_DIR_ON_1ST_IDX** - If set, clockwise rotation (forward movement) occurred on the first index event
- **EQEP_STS_DIR_FLAG** - If set, movement is clockwise rotation
- **EQEP_STS_DIR_LATCH** - If set, clockwise rotation occurred on last index event marker
- **EQEP_STS_CAP_OVRFLW_ERROR** - Overflow occurred in eQEP capture timer
- **EQEP_STS_CAP_DIR_ERROR** - Direction change occurred between position capture events
- **EQEP_STS_1ST_IDX_FLAG** - Set by the occurrence of the first index pulse
- **EQEP_STS_POS_CNT_ERROR** - Position counter error occurred

Returns
Returns the value of the QEP status register.

18.2.3.15 static void EQEP_clearStatus (uint32_t *base,* uint16_t *statusFlags*) [inline], [static]

Clears selected fields of the eQEP module status register

Parameters

base	is the base address of the eQEP module.
statusFlags	is the bit mask of the status flags to be cleared.

This function clears the status register fields indicated by *statusFlags*. The *statusFlags* parameter is the logical OR of any of the following:

- **EQEP_STS_UNIT_POS_EVNT** - Unit position event detected
- **EQEP_STS_CAP_OVRFLW_ERROR** - Overflow occurred in eQEP capture timer
- **EQEP_STS_CAP_DIR_ERROR** - Direction change occurred between position capture events
- **EQEP_STS_1ST_IDX_FLAG** - Set by the occurrence of the first index pulse

Note

Only the above status fields can be cleared. All others are read-only, non-sticky fields.

Returns

None.

18.2.3.16 static void EQEP_setCaptureConfig (uint32_t *base,* **EQEP_CAPCLKPrescale** *capPrescale,* **EQEP_UPEVNTPrescale** *evntPrescale*) [inline], [static]

Configures eQEP module edge-capture unit.

Parameters

base	is the base address of the eQEP module.
capPrescale	is the prescaler setting of the eQEP capture timer clk.
evntPrescale	is the prescaler setting of the unit position event frequency.

This function configures the operation of the eQEP module edge-capture unit. The *capPrescale* parameter provides the configuration of the eQEP capture timer clock rate. It determines by which power of 2 between 1 and 128 inclusive SYSCLKOUT is divided. The macros for this parameter are in the format of EQEP_CAPTURE_CLK_DIV_X, where X is the divide value. For example, **EQEP_CAPTURE_CLK_DIV_32** will give a capture timer clock frequency that is SYSCLKOUT/32.

The *evntPrescale* parameter determines how frequently a unit position event occurs. The macro that can be passed this parameter is in the format EQEP_UNIT_POS_EVNT_DIV_X, where X is the number of quadrature clock periods between unit position events. For example, **EQEP_UNIT_POS_EVNT_DIV_16** will result in a unit position event frequency of QCLK/16.

Returns

None.

18.2.3.17 static void EQEP_enableCapture (uint32_t *base*) [inline], [static]

Enables the eQEP module edge-capture unit.

Parameters

base	is the base address of the eQEP module.

This function enables operation of the eQEP module's edge-capture unit.

Returns

None.

18.2.3.18 static void EQEP_disableCapture (uint32_t *base*) [inline], [static]

Disables the eQEP module edge-capture unit.

Parameters

base	is the base address of the eQEP module.

This function disables operation of the eQEP module's edge-capture unit.

Returns

None.

18.2.3.19 static uint16_t EQEP_getCapturePeriod (uint32_t *base*) [inline], [static]

Gets the encoder capture period.

Parameters

base	is the base address of the eQEP module.

This function returns the period count value between the last successive eQEP position events.

Returns

The period count value between the last successive position events.

18.2.3.20 static uint16_t EQEP_getCaptureTimer (uint32_t *base*) [inline], [static]

Gets the encoder capture timer value.

Parameters

base	is the base address of the eQEP module.

This function returns the time base for the edge capture unit.

Returns

The capture timer value.

18.2.3.21 static void EQEP_enableCompare (uint32_t *base*) [inline], [static]

Enables the eQEP module position-compare unit.

Parameters

base	is the base address of the eQEP module.

This function enables operation of the eQEP module's position-compare unit.

Returns

None.

18.2.3.22 static void EQEP_disableCompare (uint32_t *base*) [inline], [static]

Disables the eQEP module position-compare unit.

Parameters

base	is the base address of the eQEP module.

This function disables operation of the eQEP module's position-compare unit.

Returns

None.

18.2.3.23 static void EQEP_setComparePulseWidth (uint32_t *base*, uint16_t *cycles*) [inline], [static]

Configures the position-compare unit's sync output pulse width.

Parameters

base	is the base address of the eQEP module.
cycles	is the width of the pulse that can be generated on a position-compare event. It is in units of 4 SYSCLKOUT cycles.

This function configures the width of the sync output pulse. The width of the pulse will be *cycles* $*$ 4 $*$ the width of a SYSCLKOUT cycle. The maximum width is 4096 $*$ 4 $*$ SYSCLKOUT cycles.

Returns

None.

18.2.3.24 static void EQEP_loadUnitTimer (uint32_t *base*, uint32_t *period*) [inline], [static]

Loads the eQEP module unit timer period as number of SYSCLK cycles.

Parameters

base	is the base address of the eQEP module.
period	is period value at which a unit time-out interrupt is set.

This function sets the unit time-out interrupt when it matches the value specified by *period* The unit timer is clocked by SYSCLKOUT

Returns
None.

18.2.3.25 static void EQEP_enableUnitTimer (uint32_t *base,* uint32_t *period*) [inline], [static]

Enables the eQEP module unit timer.

Parameters

base	is the base address of the eQEP module.
period	is period value at which a unit time-out interrupt is set.

This function enables operation of the eQEP module's peripheral unit timer. The unit timer is clocked by SYSCLKOUT and will set the unit time-out interrupt when it matches the value specified by *period*.

Returns
None.

18.2.3.26 static void EQEP_disableUnitTimer (uint32_t *base*) [inline], [static]

Disables the eQEP module unit timer.

Parameters

base	is the base address of the eQEP module.

This function disables operation of the eQEP module's peripheral unit timer.

Returns
None.

18.2.3.27 static void EQEP_enableWatchdog (uint32_t *base,* uint16_t *period*) [inline], [static]

Enables the eQEP module watchdog timer.

Parameters

base	is the base address of the eQEP module.
period	is watchdog period value at which a time-out will occur if no quadrature-clock event is detected.

This function enables operation of the eQEP module's peripheral watchdog timer.

Note
When selecting *period*, note that the watchdog timer is clocked from SYSCLKOUT/64.

Returns
None.

18.2.3.28 static void EQEP_disableWatchdog (uint32_t *base*) [inline], [static]

Disables the eQEP module watchdog timer.

Parameters

base	is the base address of the eQEP module.

This function disables operation of the eQEP module's peripheral watchdog timer.

Returns

None.

18.2.3.29 static void EQEP_setWatchdogTimerValue (uint32_t *base*, uint16_t *value*) [inline], [static]

Sets the eQEP module watchdog timer value.

Parameters

base	is the base address of the eQEP module.
value	is the value to be written to the watchdog timer.

This function sets the eQEP module's watchdog timer value.

Returns

None.

18.2.3.30 static uint16_t EQEP_getWatchdogTimerValue (uint32_t *base*) [inline], [static]

Gets the eQEP module watchdog timer value.

Parameters

base	is the base address of the eQEP module.

Returns

Returns the current watchdog timer value.

18.2.3.31 static void EQEP_setPositionInitMode (uint32_t *base*, uint16_t *initMode*) [inline], [static]

Configures the mode in which the position counter is initialized.

Parameters

base	is the base address of the eQEP module.
initMode	is the configuration for initializing the position count. See below for a description of this parameter.

This function configures the events on which the position count can be initialized. The *initMode* parameter provides the mode as either **EQEP_INIT_DO_NOTHING** (no action configured) or one of the following strobe events, index events, or a logical OR of both a strobe event and an index event.

- **EQEP_INIT_RISING_STROBE** or **EQEP_INIT_EDGE_DIR_STROBE** specify which strobe event will initialize the position counter.
- **EQEP_INIT_RISING_INDEX** or **EQEP_INIT_FALLING_INDEX** specify which index event will initialize the position counter.

Use EQEP_setSWPositionInit() to cause a software initialization and EQEP_setInitialPosition() to set the value that gets loaded into the position counter upon initialization.

Returns

None.

18.2.3.32 static void EQEP_setSWPositionInit (uint32_t *base*, bool *initialize*) [inline], [static]

Sets the software initialization of the encoder position counter.

Parameters

base	is the base address of the eQEP module.
initialize	is a flag to specify if software initialization of the position counter is enabled.

This function does a software initialization of the position counter when the *initialize* parameter is **true**. When **false**, the QEPCTL[SWI] bit is cleared and no action is taken.

The init value to be loaded into the position counter can be set with EQEP_setInitialPosition(). Additional initialization causes can be configured with EQEP_setPositionInitMode().

Returns

None.

18.2.3.33 static void EQEP_setInitialPosition (uint32_t *base*, uint32_t *position*) [inline], [static]

Sets the init value for the encoder position counter.

Parameters

base	is the base address of the eQEP module.
position	is the value to be written to the position counter upon. initialization.

This function sets the init value for position of the encoder. See EQEP_setPositionInitMode() to set the initialization cause or EQEP_setSWPositionInit() to cause a software initialization.

Returns

None.

18.2.3.34 static void EQEP_setLatchMode (uint32_t *base*, uint32_t *latchMode*) [inline], [static]

Configures the quadrature modes in which the position count can be latched.

Parameters

base	is the base address of the eQEP module.
latchMode	is the configuration for latching of the position count and several other registers. See below for a description of this parameter.

This function configures the events on which the position count and several other registers can be latched. The *latchMode* parameter provides the mode as the logical OR of several values.

- **EQEP_LATCH_CNT_READ_BY_CPU** or **EQEP_LATCH_UNIT_TIME_OUT** specify the event that latches the position counter. This latch register can be read using EQEP_getPositionLatch(). The capture timer and capture period are also latched based on this setting, and can be read using EQEP_getCaptureTimerLatch() and EQEP_getCapturePeriodLatch().
- **EQEP_LATCH_RISING_STROBE** or **EQEP_LATCH_EDGE_DIR_STROBE** specify which strobe event will latch the position counter into the strobe position latch register. This register can be read with EQEP_getStrobePositionLatch().
- **EQEP_LATCH_RISING_INDEX**, **EQEP_LATCH_FALLING_INDEX**, or **EQEP_LATCH_SW_INDEX_MARKER** specify which index event will latch the position counter into the index position latch register. This register can be read with EQEP_getIndexPositionLatch().

Returns

None.

18.2.3.35 static uint32_t EQEP_getIndexPositionLatch (uint32_t *base*) [inline], [static]

Gets the encoder position that was latched on an index event.

Parameters

base	is the base address of the eQEP module.

This function returns the value in the index position latch register. The position counter is latched into this register on either a rising index edge, a falling index edge, or a software index marker. This is configured using EQEP_setLatchMode().

Returns

The position count latched on an index event.

18.2.3.36 static uint32_t EQEP_getStrobePositionLatch (uint32_t *base*) [inline], [static]

Gets the encoder position that was latched on a strobe event.

Parameters

base	is the base address of the eQEP module.

This function returns the value in the strobe position latch register. The position counter can be configured to be latched into this register on rising strobe edges only or on rising strobe edges while moving clockwise and falling strobe edges while moving counter-clockwise. This is configured using EQEP_setLatchMode().

Returns

The position count latched on a strobe event.

18.2.3.37 static uint32_t EQEP_getPositionLatch (uint32_t *base*) [inline], [static]

Gets the encoder position that was latched on a unit time-out event.

Parameters

base	is the base address of the eQEP module.

This function returns the value in the position latch register. The position counter is latched into this register either on a unit time-out event.

Returns

The position count latch register value.

18.2.3.38 static uint16_t EQEP_getCaptureTimerLatch (uint32_t *base*) [inline], [static]

Gets the encoder capture timer latch.

Parameters

base	is the base address of the eQEP module.

This function returns the value in the capture timer latch register. The capture timer value is latched into this register either on a unit time-out event or upon the CPU reading the eQEP position counter. This is configured using EQEP_setLatchMode().

Returns

The edge-capture timer latch value.

18.2.3.39 static uint16_t EQEP_getCapturePeriodLatch (uint32_t *base*) [inline], [static]

Gets the encoder capture period latch.

Parameters

base	is the base address of the eQEP module.

This function returns the value in the capture period latch register. The capture period value is latched into this register either on a unit time-out event or upon the CPU reading the eQEP position counter. This is configured using EQEP_setLatchMode().

Returns

The edge-capture period latch value.

18.2.3.40 static void EQEP_setEmulationMode (uint32_t *base*, **EQEP_EmulationMode** *emuMode*) [inline], [static]

Set the emulation mode of the eQEP module.

Parameters

base	is the base address of the eQEP module.
emuMode	is the mode operation upon an emulation suspend.

This function sets the eQEP module's emulation mode. This mode determines how the timers are affected by an emulation suspend. Valid values for the *emuMode* parameter are the following:

- **EQEP_EMULATIONMODE_STOPIMMEDIATELY** - The position counter, watchdog counter, unit timer, and capture timer all stop immediately.
- **EQEP_EMULATIONMODE_STOPATROLLOVER** - The position counter, watchdog counter, unit timer all count until period rollover. The capture timer counts until the next unit period event.
- **EQEP_EMULATIONMODE_RUNFREE** - The position counter, watchdog counter, unit timer, and capture timer are all unaffected by an emulation suspend.

Returns

None.

18.2.3.41 void EQEP_setCompareConfig (uint32_t *base,* uint16_t *config,* uint32_t *compareValue,* uint16_t *cycles*)

Configures eQEP module position-compare unit.

Parameters

base	is the base address of the eQEP module.
config	is the configuration for the eQEP module position-compare unit. See below for a description of this parameter.
compareValue	is the value to which the position count value is compared for a position-compare event.
cycles	is the width of the pulse that can be generated on a position-compare event. It is in units of 4 SYSCLKOUT cycles.

This function configures the operation of the eQEP module position-compare unit. The *config* parameter provides the configuration of the position-compare unit and is the logical OR of several values:

- **EQEP_COMPARE_NO_SYNC_OUT**, **EQEP_COMPARE_IDX_SYNC_OUT**, or **EQEP_COMPARE_STROBE_SYNC_OUT** specify if there is a sync output pulse and which pin should be used.
- **EQEP_COMPARE_NO_SHADOW**, **EQEP_COMPARE_LOAD_ON_ZERO**, or **EQEP_COMPARE_LOAD_ON_MATCH** specify if a shadow is enabled and when should the load should occur–QPOSCNT = 0 or QPOSCNT = QPOSCOMP.

The *cycles* is used to select the width of the sync output pulse. The width of the resulting pulse will be *cycles* $* 4 *$ the width of a SYSCLKOUT cycle. The maximum width is $4096 * 4 *$ SYSCLKOUT cycles.

Note

You can set the sync pulse width independently using the EQEP_setComparePulseWidth() function.

Returns

None.

18.2.3.42 void EQEP_setInputPolarity (uint32_t *base,* bool *invertQEPA,* bool *invertQEPB,* bool *invertIndex,* bool *invertStrobe*)

Sets the polarity of the eQEP module's input signals.

Parameters

base	is the base address of the eQEP module.
invertQEPA	is the flag to negate the QEPA input.
invertQEPB	is the flag to negate the QEPA input.
invertIndex	is the flag to negate the index input.
invertStrobe	is the flag to negate the strobe input.

This function configures the polarity of the inputs to the eQEP module. To negate the polarity of any of the input signals, pass **true** into its corresponding parameter in this function. Pass **false** to leave it as-is.

Returns

None.

19 Flash Module

19.1 Flash Introduction

The Flash driver provides functions to configure the fallback power modes and the active grace periods of flash banks and pump, and the pump wake-up time. This driver also provides functions to configure the flash wait-states, prefetch, cache and ECC features. It also provides functions to access the Flash ECC test mode registers and the Flash ECC error status registers.

19.2 API Functions

Macros

- #define FLASH_FAIL_0_CLR
- #define FLASH_FAIL_1_CLR
- #define FLASH_UNC_ERR_CLR
- #define FLASH_NO_ERROR
- #define FLASH_SINGLE_ERROR
- #define FLASH_UNC_ERROR
- #define FLASH_PUMP_KEY

Enumerations

- enum Flash_BankNumber { FLASH_BANK }
- enum Flash_PumpOwnership { FLASH_CPU1_WRAPPER, FLASH_CPU2_WRAPPER }
- enum Flash_BankPowerMode { FLASH_BANK_PWR_SLEEP, FLASH_BANK_PWR_STANDBY, FLASH_BANK_PWR_ACTIVE }
- enum Flash_PumpPowerMode { FLASH_PUMP_PWR_SLEEP, FLASH_PUMP_PWR_ACTIVE }
- enum Flash_ErrorStatus { FLASH_NO_ERR, FLASH_FAIL_0, FLASH_FAIL_1, FLASH_UNC_ERR }
- enum Flash_ErrorType { FLASH_DATA_ERR, FLASH_ECC_ERR }
- enum Flash_SingleBitErrorIndicator { FLASH_DATA_BITS, FLASH_CHECK_BITS }

Functions

- static void Flash_setWaitstates (uint32_t ctrlBase, uint16_t waitstates)
- static void Flash_setBankPowerMode (uint32_t ctrlBase, Flash_BankNumber bank, Flash_BankPowerMode powerMode)
- static void Flash_setPumpPowerMode (uint32_t ctrlBase, Flash_PumpPowerMode powerMode)
- static void Flash_enablePrefetch (uint32_t ctrlBase)
- static void Flash_disablePrefetch (uint32_t ctrlBase)

- static void Flash_enableCache (uint32_t ctrlBase)
- static void Flash_disableCache (uint32_t ctrlBase)
- static void Flash_enableECC (uint32_t eccBase)
- static void Flash_disableECC (uint32_t eccBase)
- static void Flash_setBankPowerUpDelay (uint32_t ctrlBase, uint16_t delay)
- static void Flash_setPumpWakeupTime (uint32_t ctrlBase, uint16_t sysclkCycles)
- static bool Flash_isBankReady (uint32_t ctrlBase, Flash_BankNumber bank)
- static bool Flash_isPumpReady (uint32_t ctrlBase)
- static uint32_t Flash_getSingleBitErrorAddressLow (uint32_t eccBase)
- static uint32_t Flash_getSingleBitErrorAddressHigh (uint32_t eccBase)
- static uint32_t Flash_getUncorrectableErrorAddressLow (uint32_t eccBase)
- static uint32_t Flash_getUncorrectableErrorAddressHigh (uint32_t eccBase)
- static Flash_ErrorStatus Flash_getLowErrorStatus (uint32_t eccBase)
- static Flash_ErrorStatus Flash_getHighErrorStatus (uint32_t eccBase)
- static uint32_t Flash_getLowErrorPosition (uint32_t eccBase)
- static uint32_t Flash_getHighErrorPosition (uint32_t eccBase)
- static Flash_ErrorType Flash_getLowErrorType (uint32_t eccBase)
- static Flash_ErrorType Flash_getHighErrorType (uint32_t eccBase)
- static void Flash_clearLowErrorStatus (uint32_t eccBase, uint16_t errorStatus)
- static void Flash_clearHighErrorStatus (uint32_t eccBase, uint16_t errorStatus)
- static uint32_t Flash_getErrorCount (uint32_t eccBase)
- static void Flash_setErrorThreshold (uint32_t eccBase, uint16_t threshold)
- static uint32_t Flash_getInterruptFlag (uint32_t eccBase)
- static void Flash_clearSingleErrorInterruptFlag (uint32_t eccBase)
- static void Flash_clearUncorrectableInterruptFlag (uint32_t eccBase)
- static void Flash_setDataLowECCTest (uint32_t eccBase, uint32_t data)
- static void Flash_setDataHighECCTest (uint32_t eccBase, uint32_t data)
- static void Flash_setECCTestAddress (uint32_t eccBase, uint32_t address)
- static void Flash_setECCTestECCBits (uint32_t eccBase, uint16_t ecc)
- static void Flash_enableECCTestMode (uint32_t eccBase)
- static void Flash_disableECCTestMode (uint32_t eccBase)
- static void Flash_selectLowECCBlock (uint32_t eccBase)
- static void Flash_selectHighECCBlock (uint32_t eccBase)
- static void Flash_performECCCalculation (uint32_t eccBase)
- static uint32_t Flash_getTestDataOutHigh (uint32_t eccBase)
- static uint32_t Flash_getTestDataOutLow (uint32_t eccBase)
- static uint32_t Flash_getECCTestStatus (uint32_t eccBase)
- static uint32_t Flash_getECCTestErrorPosition (uint32_t eccBase)
- static Flash_SingleBitErrorIndicator Flash_getECCTestSingleBitErrorType (uint32_t eccBase)
- static void Flash_claimPumpSemaphore (uint32_t pumpSemBase, Flash_PumpOwnership wrapper)
- static void Flash_releasePumpSemaphore (uint32_t pumpSemBase)
- void Flash_initModule (uint32_t ctrlBase, uint32_t eccBase, uint16_t waitstates)
- void Flash_powerDown (uint32_t ctrlBase)

19.2.1 Detailed Description

The code for this module is contained in `driverlib/flash.c`, with `driverlib/flash.h` containing the API declarations for use by applications.

19.2.2 Enumeration Type Documentation

19.2.2.1 enum **Flash_BankNumber**

Values that can be passed to Flash_setBankPowerMode() as the bank parameter.

Enumerator
- ***FLASH_BANK*** Bank.

19.2.2.2 enum **Flash_PumpOwnership**

Values that can be passed to Flash_claimPumpSemaphore() in order to claim the pump semaphore.

Enumerator
- ***FLASH_CPU1_WRAPPER*** CPU1 Wrapper.
- ***FLASH_CPU2_WRAPPER*** CPU2 Wrapper.

19.2.2.3 enum **Flash_BankPowerMode**

Values that can be passed to Flash_setBankPowerMode() as the powerMode parameter.

Enumerator
- ***FLASH_BANK_PWR_SLEEP*** Sleep fallback mode.
- ***FLASH_BANK_PWR_STANDBY*** Standby fallback mode.
- ***FLASH_BANK_PWR_ACTIVE*** Active fallback mode.

19.2.2.4 enum **Flash_PumpPowerMode**

Values that can be passed to Flash_setPumpPowerMode() as the powerMode parameter.

Enumerator
- ***FLASH_PUMP_PWR_SLEEP*** Sleep fallback mode.
- ***FLASH_PUMP_PWR_ACTIVE*** Active fallback mode.

19.2.2.5 enum **Flash_ErrorStatus**

Type that correspond to values returned from Flash_getLowErrorStatus() and Flash_getHighErrorStatus() determining the error status code.

Enumerator
- ***FLASH_NO_ERR*** No error.
- ***FLASH_FAIL_0*** Fail on 0.
- ***FLASH_FAIL_1*** Fail on 1.
- ***FLASH_UNC_ERR*** Uncorrectable error.

19.2.2.6 enum **Flash_ErrorType**

Values that can be returned from Flash_getLowErrorType() and Flash_getHighErrorType() determining the error type.

Enumerator

FLASH_DATA_ERR Data error.

FLASH_ECC_ERR ECC error.

19.2.2.7 enum **Flash_SingleBitErrorIndicator**

Values that can be returned from Flash_getECCTestSingleBitErrorType().

Enumerator

FLASH_DATA_BITS Data bits.

FLASH_CHECK_BITS ECC bits.

19.2.3 Function Documentation

19.2.3.1 static void Flash_setWaitstates (uint32_t *ctrlBase,* uint16_t *waitstates*) `[inline]`, `[static]`

Sets the random read wait state amount.

Parameters

ctrlBase	is the base address of the flash wrapper control registers.
waitstates	is the wait-state value.

This function sets the number of wait states for a flash read access. The *waitstates* parameter is a number between 0 and 15. It is **important** to look at your device's datasheet for information about what the required minimum flash wait-state is for your selected SYSCLK frequency.

By default the wait state amount is configured to the maximum 15.

Returns

None.

Referenced by Flash_initModule().

19.2.3.2 static void Flash_setBankPowerMode (uint32_t *ctrlBase,* **Flash_BankNumber** *bank,* **Flash_BankPowerMode** *powerMode*) `[inline]`, `[static]`

Sets the fallback power mode of a flash bank.

Parameters

ctrlBase	is the base address of the flash wrapper registers.
bank	is the flash bank that is being configured.
powerMode	is the power mode to be entered.

This function sets the fallback power mode of the flash bank specified by them *bank* parameter. The power mode is specified by the *powerMode* parameter with one of the following values:

- **FLASH_BANK_PWR_SLEEP** - Sense amplifiers and sense reference disabled.
- **FLASH_BANK_PWR_STANDBY** - Sense amplifiers disabled but sense reference enabled.
- **FLASH_BANK_PWR_ACTIVE** - Sense amplifiers and sense reference enabled.

Note: There is only one Flash_BankNumber value on this device (FLASH_BANK).

Returns

None.

Referenced by Flash_initModule(), and Flash_powerDown().

19.2.3.3 static void Flash_setPumpPowerMode (uint32_t *ctrlBase,* **Flash_PumpPowerMode** *powerMode*) [inline], [static]

Sets the fallback power mode of the charge pump.

Parameters

ctrlBase	is the base address of the flash wrapper control registers.
powerMode	is the power mode to be entered.

This function sets the fallback power mode flash charge pump.

- **FLASH_PUMP_PWR_SLEEP** - All circuits disabled.
- **FLASH_PUMP_PWR_ACTIVE** - All pump circuits active.

Returns

None.

Referenced by Flash_initModule(), and Flash_powerDown().

19.2.3.4 static void Flash_enablePrefetch (uint32_t *ctrlBase*) [inline], [static]

Enables prefetch mechanism.

Parameters

ctrlBase	is the base address of the flash wrapper control registers.

Returns

None.

Referenced by Flash_initModule().

19.2.3.5 static void Flash_disablePrefetch (uint32_t *ctrlBase*) [inline], [static]

Disables prefetch mechanism.

Parameters

ctrlBase	is the base address of the flash wrapper control registers.

Returns

None.

Referenced by Flash_initModule().

19.2.3.6 static void Flash_enableCache (uint32_t *ctrlBase*) [inline], [static]

Enables data cache.

Parameters

ctrlBase	is the base address of the flash wrapper control registers.

Returns

None.

Referenced by Flash_initModule().

19.2.3.7 static void Flash_disableCache (uint32_t *ctrlBase*) [inline], [static]

Disables data cache.

Parameters

ctrlBase	is the base address of the flash wrapper control registers.

Returns

None.

Referenced by Flash_initModule().

19.2.3.8 static void Flash_enableECC (uint32_t *eccBase*) [inline], [static]

Enables flash error correction code (ECC) protection.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

Returns

None.

Referenced by Flash_initModule().

19.2.3.9 static void Flash_disableECC (uint32_t *eccBase*) [inline], [static]

Disables flash error correction code (ECC) protection.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

Returns

None.

19.2.3.10 static void Flash_setBankPowerUpDelay (uint32_t *ctrlBase*, uint16_t *delay*) [inline], [static]

Sets the bank power up delay.

Parameters

ctrlBase	is the base address of the flash wrapper control registers.
delay	is the number of HCLK cycles.

This function sets the VREADST delay to ensure that the requisite delay is introduced for the flash pump/bank to come out of low-power mode, so that the flash/OTP is ready for CPU access.

Note: Refer to TRM before configuring VREADST.

Returns

None.

Referenced by Flash_initModule(), and Flash_powerDown().

19.2.3.11 static void Flash_setPumpWakeupTime (uint32_t *ctrlBase*, uint16_t *sysclkCycles*) [inline], [static]

Sets the pump wake up time.

Parameters

ctrlBase	is the base address of the flash wrapper control registers.
sysclkCycles	is the number of SYSCLK cycles it takes for the pump to wakeup.

This function sets the wakeup time with *sysclkCycles* parameter. The *sysclkCycles* is a value between 0 and 8190. When the charge pump exits sleep power mode, it will take sysclkCycles to wakeup.

Returns

None.

19.2.3.12 static bool Flash_isBankReady (uint32_t *ctrlBase*, **Flash_BankNumber** *bank*) [inline], [static]

Reads the bank active power state.

Parameters

ctrlBase	is the base address of the flash wrapper control registers.
bank	is the flash bank that is being used.

Returns

Returns **true** if the Bank is in Active power state and **false** otherwise.

19.2.3.13 static bool Flash_isPumpReady (uint32_t *ctrlBase*) `[inline]`, `[static]`

Reads the pump active power state.

Parameters

ctrlBase	is the base address of the flash wrapper control registers.

Returns

Returns **true** if the Pump is in Active power state and **false** otherwise.

19.2.3.14 static uint32_t Flash_getSingleBitErrorAddressLow (uint32_t *eccBase*) `[inline]`, `[static]`

Gets the single error address low.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

This function returns the 32-bit address of the single bit error that occurred in the lower 64-bits of a 128-bit memory-aligned data. The returned address is to that 64-bit aligned data.

Returns

Returns the 32 bits of a 64-bit aligned address where a single bit error occurred.

19.2.3.15 static uint32_t Flash_getSingleBitErrorAddressHigh (uint32_t *eccBase*) `[inline]`, `[static]`

Gets the single error address high.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

This function returns the 32-bit address of the single bit error that occurred in the upper 64-bits of a 128-bit memory-aligned data. The returned address is to that 64-bit aligned data.

Returns

Returns the 32 bits of a 64-bit aligned address where a single bit error occurred.

19.2.3.16 static uint32_t Flash_getUncorrectableErrorAddressLow (uint32_t *eccBase*) [inline], [static]

Gets the uncorrectable error address low.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

This function returns the 32-bit address of the uncorrectable error that occurred in the lower 64-bits of a 128-bit memory-aligned data. The returned address is to that 64-bit aligned data.

Returns

Returns the 32 bits of a 64-bit aligned address where an uncorrectable error occurred.

19.2.3.17 static uint32_t Flash_getUncorrectableErrorAddressHigh (uint32_t *eccBase*) [inline], [static]

Gets the uncorrectable error address high.

Parameters

eccBase	is the base address of the flash wrapper ECC base.

This function returns the 32-bit address of the uncorrectable error that occurred in the upper 64-bits of a 128-bit memory-aligned data. The returned address is to that 64-bit aligned data.

Returns

Returns the 32 bits of a 64-bit aligned address where an uncorrectable error occurred.

19.2.3.18 static **Flash_ErrorStatus** Flash_getLowErrorStatus (uint32_t *eccBase*) [inline], [static]

Gets the error status of the Lower 64-bits.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

This function returns the error status of the lower 64-bits of a 128-bit aligned address.

Returns

Returns value of the low error status bits which can be used with Flash_ErrorStatus type.

19.2.3.19 static **Flash_ErrorStatus** Flash_getHighErrorStatus (uint32_t *eccBase*) [inline], [static]

Gets the error status of the Upper 64-bits.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

This function returns the error status of the upper 64-bits of a 128-bit aligned address.

Returns

Returns value of the high error status bits which can be used with Flash_ErrorStatus type.

19.2.3.20 static uint32_t Flash_getLowErrorPosition (uint32_t *eccBase*) [inline], [static]

Gets the error position of the lower 64-bits for a single bit error.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

This function returns the error position of the lower 64-bits. If the error type is FLASH_ECC_ERR, the position ranges from 0-7 else it ranges from 0-63 for FLASH_DATA_ERR.

Returns

Returns the position of the lower error bit.

19.2.3.21 static uint32_t Flash_getHighErrorPosition (uint32_t *eccBase*) [inline], [static]

Gets the error position of the upper 64-bits for a single bit error.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

This function returns the error position of the upper 64-bits. If the error type is FLASH_ECC_ERR, the position ranges from 0-7 else it ranges from 0-63 for FLASH_DATA_ERR.

Returns

Returns the position of the upper error bit.

19.2.3.22 static **Flash_ErrorType** Flash_getLowErrorType (uint32_t *eccBase*) [inline], [static]

Gets the error type of the lower 64-bits.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

This function returns the error type of the lower 64-bits. The error type can be FLASH_ECC_ERR or FLASH_DATA_ERR.

Returns

Returns the type of the lower 64-bit error.

References FLASH_DATA_ERR, and FLASH_ECC_ERR.

19.2.3.23 static **Flash_ErrorType** Flash_getHighErrorType (uint32_t *eccBase*) [inline], [static]

Gets the error type of the upper 64-bits.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

This function returns the error type of the upper 64-bits. The error type can be FLASH_ECC_ERR or FLASH_DATA_ERR.

Returns

Returns the type of the upper 64-bit error.

References FLASH_DATA_ERR, and FLASH_ECC_ERR.

19.2.3.24 static void Flash_clearLowErrorStatus (uint32_t *eccBase,* uint16_t *errorStatus*) [inline], [static]

Clears the errors status of the lower 64-bits.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.
errorStatus	is the error status to clear. errorStatus is a uint16_t. errorStatus is a bitwise OR of the following value: ■ **FLASH_FAIL_0_CLR** ■ **FLASH_FAIL_1_CLR** ■ **FLASH_UNC_ERR_CLR**

Returns

None.

19.2.3.25 static void Flash_clearHighErrorStatus (uint32_t *eccBase,* uint16_t *errorStatus*) [inline], [static]

Clears the errors status of the upper 64-bits.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.
errorStatus	is the error status to clear. errorStatus is a uint16_t. errorStatus is a bitwise OR of the following value: ■ **FLASH_FAIL_0_CLR** ■ **FLASH_FAIL_1_CLR** ■ **FLASH_UNC_ERR_CLR**

Returns
None.

19.2.3.26 static uint32_t Flash_getErrorCount (uint32_t *eccBase*) [inline], [static]

Gets the single bit error count.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

Returns
Returns the single bit error count.

19.2.3.27 static void Flash_setErrorThreshold (uint32_t *eccBase,* uint16_t *threshold*) [inline], [static]

Sets the single bit error threshold.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.
threshold	is the single bit error threshold. Valid ranges are from 0-65535.

Returns
None.

19.2.3.28 static uint32_t Flash_getInterruptFlag (uint32_t *eccBase*) [inline], [static]

Gets the error interrupt.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

This function returns the type of error interrupt that occurred. The values can be used with

- **FLASH_NO_ERROR**
- **FLASH_SINGLE_ERROR**
- **FLASH_UNC_ERROR**

Returns
Returns the interrupt flag.

19.2.3.29 static void Flash_clearSingleErrorInterruptFlag (uint32_t *eccBase*) [inline], [static]

Clears the single error interrupt flag.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

Returns
None.

19.2.3.30 static void Flash_clearUncorrectableInterruptFlag (uint32_t *eccBase*) [inline], [static]

Clears the uncorrectable error interrupt flag.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

Returns

None.

19.2.3.31 static void Flash_setDataLowECCTest (uint32_t *eccBase,* uint32_t *data*) [inline], [static]

Sets the Data Low Test register for ECC testing.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.
data	is a 32-bit value that is the low double word of selected 64-bit data

Returns

None.

19.2.3.32 static void Flash_setDataHighECCTest (uint32_t *eccBase,* uint32_t *data*) [inline], [static]

Sets the Data High Test register for ECC testing.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.
data	is a 32-bit value that is the high double word of selected 64-bit data

Returns

None.

19.2.3.33 static void Flash_setECCTestAddress (uint32_t *eccBase,* uint32_t *address*) [inline], [static]

Sets the test address register for ECC testing.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.
address	is a 32-bit value containing an address. Bits 21-3 will be used as the flash word (128-bit) address.

This function left shifts the address 1 bit to convert it to a byte address

Returns

None.

19.2.3.34 static void Flash_setECCTestECCBits (uint32_t *eccBase*, uint16_t *ecc*) [inline], [static]

Sets the ECC test bits for ECC testing.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.
ecc	is a 32-bit value. The least significant 8 bits are used as the ECC Control Bits in the ECC Test.

Returns

None.

19.2.3.35 static void Flash_enableECCTestMode (uint32_t *eccBase*) [inline], [static]

Enables ECC Test mode.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

Returns

None.

19.2.3.36 static void Flash_disableECCTestMode (uint32_t *eccBase*) [inline], [static]

Disables ECC Test mode.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

Returns

None.

19.2.3.37 static void Flash_selectLowECCBlock (uint32_t *eccBase*) [inline], [static]

Selects the ECC block on bits [63:0] of bank data.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

Returns

None.

19.2.3.38 static void Flash_selectHighECCBlock (uint32_t *eccBase*) [inline], [static]

Selects the ECC block on bits [127:64] of bank data.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

Returns

None.

19.2.3.39 static void Flash_performECCCalculation (uint32_t *eccBase*) [inline], [static]

Performs the ECC calculation on the test block.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

Returns

None.

19.2.3.40 static uint32_t Flash_getTestDataOutHigh (uint32_t *eccBase*) [inline], [static]

Gets the ECC Test data out high 63:32 bits.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

Returns

Returns the ECC TEst data out High.

19.2.3.41 static uint32_t Flash_getTestDataOutLow (uint32_t *eccBase*) [inline], [static]

Gets the ECC Test data out low 31:0 bits.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

Returns

Returns the ECC Test data out Low.

19.2.3.42 static uint32_t Flash_getECCTestStatus (uint32_t *eccBase*) [inline], [static]

Gets the ECC Test status.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

This function returns the ECC test status. The values can be used with

- **FLASH_NO_ERROR**
- **FLASH_SINGLE_ERROR**
- **FLASH_UNC_ERROR**

Returns

Returns the ECC test status.

19.2.3.43 static uint32_t Flash_getECCTestErrorPosition (uint32_t *eccBase*) [inline], [static]

Gets the ECC Test single bit error position.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

Returns

Returns the ECC Test single bit error position. If the error type is check bits than the position can range from 0 to 7. If the error type is data bits than the position can range from 0 to 63.

19.2.3.44 static **Flash_SingleBitErrorIndicator** Flash_getECCTestSingleBitErrorType (uint32_t *eccBase*) [inline], [static]

Gets the single bit error type.

Parameters

eccBase	is the base address of the flash wrapper ECC registers.

Returns

Returns the single bit error type as a Flash_SingleBitErrorIndicator. FLASH_DATA_BITS and FLASH_CHECK_BITS indicate where the single bit error occurred.

19.2.3.45 static void Flash_claimPumpSemaphore (uint32_t *pumpSemBase*, **Flash_PumpOwnership** *wrapper*) [inline], [static]

Claim the flash pump semaphore.

Parameters

pumpSemBase	is the base address of the flash pump semaphore.
wrapper	is the Flash_PumpOwnership wrapper claiming the pump semaphore.

Returns

None.

References FLASH_PUMP_KEY.

19.2.3.46 static void Flash_releasePumpSemaphore (uint32_t *pumpSemBase*) [inline], [static]

Release the flash pump semaphore.

Parameters

pumpSemBase	is the base address of the flash pump semaphore.

Returns

None.

References FLASH_PUMP_KEY.

19.2.3.47 void Flash_initModule (uint32_t *ctrlBase,* uint32_t *eccBase,* uint16_t *waitstates*)

Initializes the flash control registers.

Parameters

ctrlBase	is the base address of the flash wrapper control registers.
eccBase	is the base address of the flash wrapper ECC registers.
waitstates	is the wait-state value.

This function initializes the flash control registers. At reset bank and pump are in sleep. A flash access will power up the bank and pump automatically. After a flash access, bank and pump go to low power mode (configurable in FBFALLBACK/FPAC1 registers) if there is no further access to flash. This function will power up Flash bank and pump and set the fallback mode of flash and pump as active.

This function also sets the number of wait-states for a flash access (see Flash_setWaitstates() for more details), and enables cache, the prefetch mechanism, and ECC.

Returns

None.

References FLASH_BANK, FLASH_BANK_PWR_ACTIVE, Flash_disableCache(), Flash_disablePrefetch(), Flash_enableCache(), Flash_enableECC(), Flash_enablePrefetch(), FLASH_PUMP_PWR_ACTIVE, Flash_setBankPowerMode(), Flash_setBankPowerUpDelay(), Flash_setPumpPowerMode(), and Flash_setWaitstates().

19.2.3.48 void Flash_powerDown (uint32_t *ctrlBase*)

Powers down the flash.

Parameters

ctrlBase	is the base address of the flash wrapper control registers.

This function powers down the flash bank(s) and the flash pump.

Note: For this device, you must claim the flash pump semaphore before calling this function and powering down the pump. Afterwards, you may want to relinquish the flash pump.

Returns

None.

References FLASH_BANK, FLASH_BANK_PWR_SLEEP, FLASH_PUMP_PWR_SLEEP, Flash_setBankPowerMode(), Flash_setBankPowerUpDelay(), and Flash_setPumpPowerMode().

20 GPIO Module

20.1 GPIO Introduction

The GPIO module provides an API to configure, read from, and write to the GPIO pins. Functions fall into the two categories, control and data. Control functions configure properties like direction, pin muxing, and qualification. Data functions allow you to read the value on a pin or write a value to it.

Most functions will configure a single pin at a time. The pin to be configured will be specified using its GPIO number. Refer to the device's datasheet to learn what numbers are valid for that part number. Also note that even if a GPIO number is valid for a part number, it may not be valid for all possible features. For instance, GPIO_setAnalogMode() is only usable for a fraction of the GPIO numbers.

For information and functions to configure a pin for low-power mode wake-up, see the SysCtl module.

20.2 API Functions

Enumerations

- enum GPIO_Direction { GPIO_DIR_MODE_IN, GPIO_DIR_MODE_OUT }
- enum GPIO_IntType { GPIO_INT_TYPE_FALLING_EDGE, GPIO_INT_TYPE_RISING_EDGE, GPIO_INT_TYPE_BOTH_EDGES }
- enum GPIO_QualificationMode { GPIO_QUAL_SYNC, GPIO_QUAL_3SAMPLE, GPIO_QUAL_6SAMPLE, GPIO_QUAL_ASYNC }
- enum GPIO_AnalogMode { GPIO_ANALOG_DISABLED, GPIO_ANALOG_ENABLED }
- enum GPIO_CoreSelect { GPIO_CORE_CPU1, GPIO_CORE_CPU1_CLA1, GPIO_CORE_CPU2, GPIO_CORE_CPU2_CLA1 }
- enum GPIO_Port { GPIO_PORT_A, GPIO_PORT_B, GPIO_PORT_C, GPIO_PORT_D, GPIO_PORT_E, GPIO_PORT_F }
- enum GPIO_ExternalIntNum { GPIO_INT_XINT1, GPIO_INT_XINT2, GPIO_INT_XINT3, GPIO_INT_XINT4, GPIO_INT_XINT5 }

Functions

- static void GPIO_setInterruptType (GPIO_ExternalIntNum extIntNum, GPIO_IntType intType)
- static GPIO_IntType GPIO_getInterruptType (GPIO_ExternalIntNum extIntNum)
- static void GPIO_enableInterrupt (GPIO_ExternalIntNum extIntNum)
- static void GPIO_disableInterrupt (GPIO_ExternalIntNum extIntNum)
- static uint32_t GPIO_readPin (uint32_t pin)
- static void GPIO_writePin (uint32_t pin, uint32_t outVal)

- static void GPIO_togglePin (uint32_t pin)
- static uint32_t GPIO_readPortData (GPIO_Port port)
- static void GPIO_writePortData (GPIO_Port port, uint32_t outVal)
- static void GPIO_setPortPins (GPIO_Port port, uint32_t pinMask)
- static void GPIO_clearPortPins (GPIO_Port port, uint32_t pinMask)
- static void GPIO_togglePortPins (GPIO_Port port, uint32_t pinMask)
- static void GPIO_lockPortConfig (GPIO_Port port, uint32_t pinMask)
- static void GPIO_unlockPortConfig (GPIO_Port port, uint32_t pinMask)
- static void GPIO_commitPortConfig (GPIO_Port port, uint32_t pinMask)
- void GPIO_setDirectionMode (uint32_t pin, GPIO_Direction pinIO)
- GPIO_Direction GPIO_getDirectionMode (uint32_t pin)
- void GPIO_setInterruptPin (uint32_t pin, GPIO_ExternalIntNum extIntNum)
- void GPIO_setPadConfig (uint32_t pin, uint32_t pinType)
- uint32_t GPIO_getPadConfig (uint32_t pin)
- void GPIO_setQualificationMode (uint32_t pin, GPIO_QualificationMode qualification)
- GPIO_QualificationMode GPIO_getQualificationMode (uint32_t pin)
- void GPIO_setQualificationPeriod (uint32_t pin, uint32_t divider)
- void GPIO_setMasterCore (uint32_t pin, GPIO_CoreSelect core)
- void GPIO_setAnalogMode (uint32_t pin, GPIO_AnalogMode mode)
- void GPIO_setPinConfig (uint32_t pinConfig)

20.2.1 Detailed Description

The first step to configuring GPIO is to figure out the peripheral muxing. The function to configure the mux registers is GPIO_setPinConfig(). The values to be passed to this function to specify the functionality the pin should have are found in pin_map.h.

Next, use GPIO_setPadConfig() to configure any properties like internal pullups, open-drain, or an inverted input signal. GPIO_setQualificationMode() and GPIO_setQualificationPeriod() can be used to configure any needed input qualification.

Then, for pins configured as GPIOs, use GPIO_setDirectionMode() to select a direction. Take care to write the desired initial value for that pin using GPIO_writePin() before configuring a pin as an output to avoid any glitches.

Several functions are provided for the configuration of external interrupts. These functions use the device's XINT module. The Input X-BAR is also leveraged to configure the pin on which an event will cause an interrupt. These functions are GPIO_setInterruptType(), GPIO_getInterruptType(), GPIO_enableInterrupt(), GPIO_disableInterrupt(), and GPIO_setInterruptPin().

Most functions operate on one pin at a time. However, there are a few functions that can operate on an entire port at once for the sake of efficiency. These are the data functions GPIO_readPortData(), GPIO_writePortData(), GPIO_setPortPins(), GPIO_clearPortPins(), and GPIO_togglePortPins(). Other data functions that affect a single pin at a time are GPIO_readPin(), GPIO_writePin(), and GPIO_togglePin().

The code for this module is contained in `driverlib/gpio.c`, with `driverlib/gpio.h` containing the API declarations for use by applications.

20.2.2 Enumeration Type Documentation

20.2.2.1 enum **GPIO_Direction**

Values that can be passed to GPIO_setDirectionMode() as the *pinIO* parameter and returned from GPIO_getDirectionMode().

Enumerator

GPIO_DIR_MODE_IN Pin is a GPIO input.

GPIO_DIR_MODE_OUT Pin is a GPIO output.

20.2.2.2 enum **GPIO_IntType**

Values that can be passed to GPIO_setInterruptType() as the *intType* parameter and returned from GPIO_getInterruptType().

Enumerator

GPIO_INT_TYPE_FALLING_EDGE Interrupt on falling edge.

GPIO_INT_TYPE_RISING_EDGE Interrupt on rising edge.

GPIO_INT_TYPE_BOTH_EDGES Interrupt on both edges.

20.2.2.3 enum **GPIO_QualificationMode**

Values that can be passed to GPIO_setQualificationMode() as the *qualification* parameter and returned by GPIO_getQualificationMode().

Enumerator

GPIO_QUAL_SYNC Synchronization to SYSCLKOUT.

GPIO_QUAL_3SAMPLE Qualified with 3 samples.

GPIO_QUAL_6SAMPLE Qualified with 6 samples.

GPIO_QUAL_ASYNC No synchronization.

20.2.2.4 enum **GPIO_AnalogMode**

Values that can be passed to GPIO_setAnalogMode() as the *mode* parameter.

Enumerator

GPIO_ANALOG_DISABLED Pin is in digital mode.

GPIO_ANALOG_ENABLED Pin is in analog mode.

20.2.2.5 enum **GPIO_CoreSelect**

Values that can be passed to GPIO_setMasterCore() as the *core* parameter.

Enumerator

GPIO_CORE_CPU1 CPU1 selected as master core.

GPIO_CORE_CPU1_CLA1 CPU1's CLA1 selected as master core.

GPIO_CORE_CPU2 CPU2 selected as master core.

GPIO_CORE_CPU2_CLA1 CPU2's CLA1 selected as master core.

20.2.2.6 enum **GPIO_Port**

Values that can be passed to GPIO_readPortData(), GPIO_setPortPins(), GPIO_clearPortPins(), and GPIO_togglePortPins() as the *port* parameter.

Enumerator

GPIO_PORT_A GPIO port A.

GPIO_PORT_B GPIO port B.

GPIO_PORT_C GPIO port C.

GPIO_PORT_D GPIO port D.

GPIO_PORT_E GPIO port E.

GPIO_PORT_F GPIO port F.

20.2.2.7 enum **GPIO_ExternalIntNum**

Values that can be passed to GPIO_setInterruptPin(), GPIO_setInterruptType(), GPIO_getInterruptType(), GPIO_enableInterrupt(), GPIO_disableInterrupt(), as the *extIntNum* parameter.

Enumerator

GPIO_INT_XINT1 External Interrupt 1.

GPIO_INT_XINT2 External Interrupt 2.

GPIO_INT_XINT3 External Interrupt 3.

GPIO_INT_XINT4 External Interrupt 4.

GPIO_INT_XINT5 External Interrupt 5.

20.2.3 Function Documentation

20.2.3.1 static void GPIO_setInterruptType (**GPIO_ExternalIntNum** *extIntNum,* **GPIO_IntType** *intType*) `[inline]`, `[static]`

Sets the interrupt type for the specified pin.

Parameters

extIntNum	specifies the external interrupt.
intType	specifies the type of interrupt trigger mechanism.

This function sets up the various interrupt trigger mechanisms for the specified pin on the selected GPIO port.

The following defines can be used to specify the external interrupt for the *extIntNum* parameter:

- **GPIO_INT_XINT1**
- **GPIO_INT_XINT2**
- **GPIO_INT_XINT3**
- **GPIO_INT_XINT4**
- **GPIO_INT_XINT5**

One of the following flags can be used to define the *intType* parameter:

- **GPIO_INT_TYPE_FALLING_EDGE** sets detection to edge and trigger to falling
- **GPIO_INT_TYPE_RISING_EDGE** sets detection to edge and trigger to rising
- **GPIO_INT_TYPE_BOTH_EDGES** sets detection to both edges

Returns
None.

20.2.3.2 static **GPIO_IntType** GPIO_getInterruptType (**GPIO_ExternalIntNum** *extIntNum*) [inline], [static]

Gets the interrupt type for a pin.

Parameters

extIntNum	specifies the external interrupt.

This function gets the interrupt type for a interrupt. The interrupt can be configured as a falling-edge, rising-edge, or both-edges detected interrupt.

The following defines can be used to specify the external interrupt for the *extIntNum* parameter:

- **GPIO_INT_XINT1**
- **GPIO_INT_XINT2**
- **GPIO_INT_XINT3**
- **GPIO_INT_XINT4**
- **GPIO_INT_XINT5**

Returns
Returns one of the flags described for GPIO_setInterruptType().

20.2.3.3 static void GPIO_enableInterrupt (**GPIO_ExternalIntNum** *extIntNum*) [inline], [static]

Enables the specified external interrupt.

Parameters

extIntNum	specifies the external interrupt.

This function enables the indicated external interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt. Disabled sources have no effect on the processor.

The following defines can be used to specify the external interrupt for the *extIntNum* parameter:

- **GPIO_INT_XINT1**
- **GPIO_INT_XINT2**
- **GPIO_INT_XINT3**
- **GPIO_INT_XINT4**
- **GPIO_INT_XINT5**

Returns
None.

20.2.3.4 static void GPIO_disableInterrupt (**GPIO_ExternalIntNum** *extIntNum*) [inline], [static]

Disables the specified external interrupt.

Parameters

extIntNum	specifies the external interrupt.

This function disables the indicated external interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt. Disabled sources have no effect on the processor.

The following defines can be used to specify the external interrupt for the *extIntNum* parameter:

- **GPIO_INT_XINT1**
- **GPIO_INT_XINT2**
- **GPIO_INT_XINT3**
- **GPIO_INT_XINT4**
- **GPIO_INT_XINT5**

Returns
None.

20.2.3.5 static uint32_t GPIO_readPin (uint32_t *pin*) [inline], [static]

Reads the value present on the specified pin.

Parameters

pin	is the identifying GPIO number of the pin.

The value at the specified pin are read, as specified by *pin*. The value is returned for both input and output pins.

The pin is specified by its numerical value. For example, GPIO34 is specified by passing 34 as *pin*.

Returns
Returns the value in the data register for the specified pin.

20.2.3.6 static void GPIO_writePin (uint32_t *pin,* uint32_t *outVal*) [inline], [static]

Writes a value to the specified pin.

Parameters

pin	is the identifying GPIO number of the pin.
outVal	is the value to write to the pin.

Writes the corresponding bit values to the output pin specified by *pin*. Writing to a pin configured as an input pin has no effect.

The pin is specified by its numerical value. For example, GPIO34 is specified by passing 34 as *pin*.

Returns

None.

20.2.3.7 static void GPIO_togglePin (uint32_t *pin*) `[inline]`, `[static]`

Toggles the specified pin.

Parameters

pin	is the identifying GPIO number of the pin.

Writes the corresponding bit values to the output pin specified by *pin*. Writing to a pin configured as an input pin has no effect.

The pin is specified by its numerical value. For example, GPIO34 is specified by passing 34 as *pin*.

Returns

None.

20.2.3.8 static uint32_t GPIO_readPortData (**GPIO_Port** *port*) `[inline]`, `[static]`

Reads the data on the specified port.

Parameters

port	is the GPIO port being accessed in the form of **GPIO_PORT_X** where X is the port letter.

Returns

Returns the value available on pin for the specified port. Each bit of the the return value represents a pin on the port, where bit 0 represents GPIO port pin 0, bit 1 represents GPIO port pin 1, and so on.

20.2.3.9 static void GPIO_writePortData (**GPIO_Port** *port*, uint32_t *outVal*) `[inline]`, `[static]`

Writes a value to the specified port.

Parameters

port	is the GPIO port being accessed.
outVal	is the value to write to the port.

This function writes the value *outVal* to the port specified by the *port* parameter which takes a value in the form of **GPIO_PORT_X** where X is the port letter. For example, use **GPIO_PORT_A** to affect port A (GPIOs 0-31).

The *outVal* is a bit-packed value, where each bit represents a bit on a GPIO port. Bit 0 represents GPIO port pin 0, bit 1 represents GPIO port pin 1, and so on.

Returns
None.

20.2.3.10 static void GPIO_setPortPins (**GPIO_Port** *port,* uint32_t *pinMask*) `[inline]`, `[static]`

Sets all of the specified pins on the specified port.

Parameters

port	is the GPIO port being accessed.
pinMask	is a mask of which of the 32 pins on the port are affected.

This function sets all of the pins specified by the *pinMask* parameter on the port specified by the *port* parameter which takes a value in the form of **GPIO_PORT_X** where X is the port letter. For example, use **GPIO_PORT_A** to affect port A (GPIOs 0-31).

The *pinMask* is a bit-packed value, where each bit that is set identifies the pin to be set. Bit 0 represents GPIO port pin 0, bit 1 represents GPIO port pin 1, and so on.

Returns
None.

20.2.3.11 static void GPIO_clearPortPins (**GPIO_Port** *port,* uint32_t *pinMask*) `[inline]`, `[static]`

Clears all of the specified pins on the specified port.

Parameters

port	is the GPIO port being accessed.
pinMask	is a mask of which of the 32 pins on the port are affected.

This function clears all of the pins specified by the *pinMask* parameter on the port specified by the *port* parameter which takes a value in the form of **GPIO_PORT_X** where X is the port letter. For example, use **GPIO_PORT_A** to affect port A (GPIOs 0-31).

The *pinMask* is a bit-packed value, where each bit that is **set** identifies the pin to be cleared. Bit 0 represents GPIO port pin 0, bit 1 represents GPIO port pin 1, and so on.

Returns
None.

20.2.3.12 static void GPIO_togglePortPins (**GPIO_Port** *port*, uint32_t *pinMask*) [inline], [static]

Toggles all of the specified pins on the specified port.

Parameters

port	is the GPIO port being accessed.
pinMask	is a mask of which of the 32 pins on the port are affected.

This function toggles all of the pins specified by the *pinMask* parameter on the port specified by the *port* parameter which takes a value in the form of **GPIO_PORT_X** where X is the port letter. For example, use **GPIO_PORT_A** to affect port A (GPIOs 0-31).

The *pinMask* is a bit-packed value, where each bit that is set identifies the pin to be toggled. Bit 0 represents GPIO port pin 0, bit 1 represents GPIO port pin 1, and so on.

Returns

None.

20.2.3.13 static void GPIO_lockPortConfig (**GPIO_Port** *port,* uint32_t *pinMask*) [inline], [static]

Locks the configuration of the specified pins on the specified port.

Parameters

port	is the GPIO port being accessed.
pinMask	is a mask of which of the 32 pins on the port are affected.

This function locks the configuration registers of the pins specified by the *pinMask* parameter on the port specified by the *port* parameter which takes a value in the form of **GPIO_PORT_X** where X is the port letter. For example, use **GPIO_PORT_A** to affect port A (GPIOs 0-31).

The *pinMask* is a bit-packed value, where each bit that is set identifies the pin to be locked. Bit 0 represents GPIO port pin 0, bit 1 represents GPIO port pin 1, 0xFFFFFFFF represents all pins on that port, and so on.

Note that this function is for locking the configuration of a pin such as the pin muxing, direction, open drain mode, and other settings. It does not affect the ability to change the value of the pin.

Returns

None.

20.2.3.14 static void GPIO_unlockPortConfig (**GPIO_Port** *port,* uint32_t *pinMask*) [inline], [static]

Unlocks the configuration of the specified pins on the specified port.

Parameters

port	is the GPIO port being accessed.
pinMask	is a mask of which of the 32 pins on the port are affected.

This function unlocks the configuration registers of the pins specified by the *pinMask* parameter on the port specified by the *port* parameter which takes a value in the form of **GPIO_PORT_X** where X is the port letter. For example, use **GPIO_PORT_A** to affect port A (GPIOs 0-31).

The *pinMask* is a bit-packed value, where each bit that is set identifies the pin to be unlocked. Bit 0 represents GPIO port pin 0, bit 1 represents GPIO port pin 1, 0xFFFFFFFF represents all pins on that port, and so on.

Returns
None.

20.2.3.15 static void GPIO_commitPortConfig (**GPIO_Port** *port,* uint32_t *pinMask*) [inline], [static]

Commits the lock configuration of the specified pins on the specified port.

Parameters

port	is the GPIO port being accessed.
pinMask	is a mask of which of the 32 pins on the port are affected.

This function commits the lock configuration registers of the pins specified by the *pinMask* parameter on the port specified by the *port* parameter which takes a value in the form of **GPIO_PORT_X** where X is the port letter. For example, use **GPIO_PORT_A** to affect port A (GPIOs 0-31).

The *pinMask* is a bit-packed value, where each bit that is set identifies the pin to be locked. Bit 0 represents GPIO port pin 0, bit 1 represents GPIO port pin 1, 0xFFFFFFFF represents all pins on that port, and so on.

Note that once this function is called, GPIO_lockPortConfig() and GPIO_unlockPortConfig() will no longer have any effect on the specified pins.

Returns
None.

20.2.3.16 void GPIO_setDirectionMode (uint32_t *pin,* **GPIO_Direction** *pinIO*)

Sets the direction and mode of the specified pin.

Parameters

pin	is the identifying GPIO number of the pin.
pinIO	is the pin direction mode.

This function configures the specified pin on the selected GPIO port as either input or output.

The parameter *pinIO* is an enumerated data type that can be one of the following values:

- **GPIO_DIR_MODE_IN**
- **GPIO_DIR_MODE_OUT**

where **GPIO_DIR_MODE_IN** specifies that the pin is programmed as an input and **GPIO_DIR_MODE_OUT** specifies that the pin is programmed as an output.

The pin is specified by its numerical value. For example, GPIO34 is specified by passing 34 as *pin*.

Returns
None.

References GPIO_DIR_MODE_OUT.

20.2.3.17 **GPIO_Direction** GPIO_getDirectionMode (uint32_t *pin*)

Gets the direction mode of a pin.

Parameters

pin	is the identifying GPIO number of the pin.

This function gets the direction mode for a specified pin. The pin can be configured as either an input or output The type of direction is returned as an enumerated data type.

Returns

Returns one of the enumerated data types described for GPIO_setDirectionMode().

20.2.3.18 void GPIO_setInterruptPin (uint32_t *pin*, **GPIO_ExternalIntNum** *extIntNum*)

Sets the pin for the specified external interrupt.

Parameters

pin	is the identifying GPIO number of the pin.
extIntNum	specifies the external interrupt.

This function sets which pin triggers the selected external interrupt.

The following defines can be used to specify the external interrupt for the *extIntNum* parameter:

- **GPIO_INT_XINT1**
- **GPIO_INT_XINT2**
- **GPIO_INT_XINT3**
- **GPIO_INT_XINT4**
- **GPIO_INT_XINT5**

The pin is specified by its numerical value. For example, GPIO34 is specified by passing 34 as *pin*.

See Also

XBAR_setInputPin()

Returns

None.

References GPIO_INT_XINT1, GPIO_INT_XINT2, GPIO_INT_XINT3, GPIO_INT_XINT4, GPIO_INT_XINT5, XBAR_INPUT1, XBAR_INPUT13, XBAR_INPUT14, XBAR_INPUT4, XBAR_INPUT5, XBAR_INPUT6, and XBAR_setInputPin().

20.2.3.19 void GPIO_setPadConfig (uint32_t *pin*, uint32_t *pinType*)

Sets the pad configuration for the specified pin.

Parameters

pin	is the identifying GPIO number of the pin.

pinType	specifies the pin type.

This function sets the pin type for the specified pin. The parameter *pinType* can be the following values:

- **GPIO_PIN_TYPE_STD** specifies a push-pull output or a floating input
- **GPIO_PIN_TYPE_PULLUP** specifies the pull-up is enabled for an input
- **GPIO_PIN_TYPE_OD** specifies an open-drain output pin
- **GPIO_PIN_TYPE_INVERT** specifies inverted polarity on an input

GPIO_PIN_TYPE_INVERT may be OR-ed with **GPIO_PIN_TYPE_STD** or **GPIO_PIN_TYPE_PULLUP**.

The pin is specified by its numerical value. For example, GPIO34 is specified by passing 34 as *pin*.

Returns
None.

20.2.3.20 uint32_t GPIO_getPadConfig (uint32_t *pin*)

Gets the pad configuration for a pin.

Parameters

pin	is the identifying GPIO number of the pin.

This function returns the pin type for the specified pin. The value returned corresponds to the values used in GPIO_setPadConfig().

Returns
Returns a bit field of the values **GPIO_PIN_TYPE_STD**, **GPIO_PIN_TYPE_PULLUP**, **GPIO_PIN_TYPE_OD**, and **GPIO_PIN_TYPE_INVERT**.

20.2.3.21 void GPIO_setQualificationMode (uint32_t *pin*, **GPIO_QualificationMode** *qualification*)

Sets the qualification mode for the specified pin.

Parameters

pin	is the identifying GPIO number of the pin.
qualification	specifies the qualification mode of the pin.

This function sets the qualification mode for the specified pin. The parameter *qualification* can be one of the following values:

- **GPIO_QUAL_SYNC**
- **GPIO_QUAL_3SAMPLE**
- **GPIO_QUAL_6SAMPLE**
- **GPIO_QUAL_ASYNC**

To set the qualification sampling period, use GPIO_setQualificationPeriod().

Returns
None.

20.2.3.22 **GPIO_QualificationMode** GPIO_getQualificationMode (uint32_t *pin*)

Gets the qualification type for the specified pin.

Parameters

pin	is the identifying GPIO number of the pin.

Returns
Returns the qualification mode in the form of one of the values **GPIO_QUAL_SYNC**, **GPIO_QUAL_3SAMPLE**, **GPIO_QUAL_6SAMPLE**, or **GPIO_QUAL_ASYNC**.

20.2.3.23 void GPIO_setQualificationPeriod (uint32_t *pin,* uint32_t *divider*)

Sets the qualification period for a set of pins

Parameters

pin	is the identifying GPIO number of the pin.
divider	specifies the output drive strength.

This function sets the qualification period for a set of **8 pins**, specified by the *pin* parameter. For instance, passing in 3 as the value of *pin* will set the qualification period for GPIO0 through GPIO7, and a value of 98 will set the qualification period for GPIO96 through GPIO103. This is because the register field that configures the divider is shared.

To think of this in terms of an equation, configuring *pin* as **n** will configure GPIO (n & ∼(7)) through GPIO ((n & ∼(7)) + 7).

divider is the value by which the frequency of SYSCLKOUT is divided. It can be 1 or an even value between 2 and 510 inclusive.

Returns
None.

20.2.3.24 void GPIO_setMasterCore (uint32_t *pin,* **GPIO_CoreSelect** *core*)

Selects the master core of a specified pin.

Parameters

pin	is the identifying GPIO number of the pin.
core	is the core that is master of the specified pin.

This function configures which core owns the specified pin's data registers (DATA, SET, CLEAR, and TOGGLE). The *core* parameter is an enumerated data type that specifies the core, such as **GPIO_CORE_CPU1_CLA1** to make CPU1's CLA1 master of the pin.

The pin is specified by its numerical value. For example, GPIO34 is specified by passing 34 as *pin*.

Returns
None.

20.2.3.25 void GPIO_setAnalogMode (uint32_t *pin*, **GPIO_AnalogMode** *mode*)

Sets the analog mode of the specified pin.

Parameters

pin	is the identifying GPIO number of the pin.
mode	is the selected analog mode.

This function configures the specified pin for either analog or digital mode. Not all GPIO pins have the ability to be switched to analog mode, so refer to the technical reference manual for details. This setting should be thought of as another level of muxing.

The parameter *mode* is an enumerated data type that can be one of the following values:

- **GPIO_ANALOG_DISABLED** - Pin is in digital mode
- **GPIO_ANALOG_ENABLED** - Pin is in analog mode

The pin is specified by its numerical value. For example, GPIO34 is specified by passing 34 as *pin*.

Returns
None.

References GPIO_ANALOG_ENABLED.

20.2.3.26 void GPIO_setPinConfig (uint32_t *pinConfig*)

Configures the alternate function of a GPIO pin.

Parameters

pinConfig	is the pin configuration value, specified as only one of the **GPIO_::_**???? values.

This function configures the pin mux that selects the peripheral function associated with a particular GPIO pin. Only one peripheral function at a time can be associated with a GPIO pin, and each peripheral function should only be associated with a single GPIO pin at a time (despite the fact that many of them can be associated with more than one GPIO pin).

The available mappings are supplied in `pin_map.h`.

Returns
None.

21 I2C Module

21.1 I2C Introduction

The inter-integrated circuit (I2C) API provides a set of functions to configure the device's I2C module. The driver supports operation in both master and slave mode and provides functions to initialize the module, to send and receive data, to obtain status information, and to manage interrupts.

21.2 API Functions

Enumerations

- enum I2C_InterruptSource {
  I2C_INTSRC_NONE, I2C_INTSRC_ARB_LOST, I2C_INTSRC_NO_ACK,
  I2C_INTSRC_REG_ACCESS_RDY,
  I2C_INTSRC_RX_DATA_RDY, I2C_INTSRC_TX_DATA_RDY,
  I2C_INTSRC_STOP_CONDITION, I2C_INTSRC_ADDR_SLAVE }
- enum I2C_TxFIFOLevel {
  I2C_FIFO_TXEMPTY, I2C_FIFO_TX0, I2C_FIFO_TX1, I2C_FIFO_TX2,
  I2C_FIFO_TX3, I2C_FIFO_TX4, I2C_FIFO_TX5, I2C_FIFO_TX6,
  I2C_FIFO_TX7, I2C_FIFO_TX8, I2C_FIFO_TX9, I2C_FIFO_TX10,
  I2C_FIFO_TX11, I2C_FIFO_TX12, I2C_FIFO_TX13, I2C_FIFO_TX14,
  I2C_FIFO_TX15, I2C_FIFO_TX16, I2C_FIFO_TXFULL }
- enum I2C_RxFIFOLevel {
  I2C_FIFO_RXEMPTY, I2C_FIFO_RX0, I2C_FIFO_RX1, I2C_FIFO_RX2,
  I2C_FIFO_RX3, I2C_FIFO_RX4, I2C_FIFO_RX5, I2C_FIFO_RX6,
  I2C_FIFO_RX7, I2C_FIFO_RX8, I2C_FIFO_RX9, I2C_FIFO_RX10,
  I2C_FIFO_RX11, I2C_FIFO_RX12, I2C_FIFO_RX13, I2C_FIFO_RX14,
  I2C_FIFO_RX15, I2C_FIFO_RX16, I2C_FIFO_RXFULL }
- enum I2C_BitCount {
  I2C_BITCOUNT_1, I2C_BITCOUNT_2, I2C_BITCOUNT_3, I2C_BITCOUNT_4,
  I2C_BITCOUNT_5, I2C_BITCOUNT_6, I2C_BITCOUNT_7, I2C_BITCOUNT_8 }
- enum I2C_AddressMode { I2C_ADDR_MODE_7BITS, I2C_ADDR_MODE_10BITS }
- enum I2C_EmulationMode { I2C_EMULATION_STOP_SCL_LOW,
  I2C_EMULATION_FREE_RUN }
- enum I2C_DutyCycle { I2C_DUTYCYCLE_33, I2C_DUTYCYCLE_50 }

Functions

- static void I2C_enableModule (uint32_t base)
- static void I2C_disableModule (uint32_t base)
- static void I2C_enableFIFO (uint32_t base)

- static void I2C_disableFIFO (uint32_t base)
- static void I2C_setFIFOInterruptLevel (uint32_t base, I2C_TxFIFOLevel txLevel, I2C_RxFIFOLevel rxLevel)
- static void I2C_getFIFOInterruptLevel (uint32_t base, I2C_TxFIFOLevel ∗txLevel, I2C_RxFIFOLevel ∗rxLevel)
- static I2C_TxFIFOLevel I2C_getTxFIFOStatus (uint32_t base)
- static I2C_RxFIFOLevel I2C_getRxFIFOStatus (uint32_t base)
- static void I2C_setSlaveAddress (uint32_t base, uint16_t slaveAddr)
- static void I2C_setOwnSlaveAddress (uint32_t base, uint16_t slaveAddr)
- static bool I2C_isBusBusy (uint32_t base)
- static uint16_t I2C_getStatus (uint32_t base)
- static void I2C_clearStatus (uint32_t base, uint16_t stsFlags)
- static void I2C_setConfig (uint32_t base, uint16_t config)
- static void I2C_setBitCount (uint32_t base, I2C_BitCount size)
- static void I2C_sendStartCondition (uint32_t base)
- static void I2C_sendStopCondition (uint32_t base)
- static void I2C_sendNACK (uint32_t base)
- static uint16_t I2C_getData (uint32_t base)
- static void I2C_putData (uint32_t base, uint16_t data)
- static bool I2C_getStopConditionStatus (uint32_t base)
- static void I2C_setDataCount (uint32_t base, uint16_t count)
- static void I2C_setAddressMode (uint32_t base, I2C_AddressMode mode)
- static void I2C_setEmulationMode (uint32_t base, I2C_EmulationMode mode)
- static void I2C_enableLoopback (uint32_t base)
- static void I2C_disableLoopback (uint32_t base)
- static I2C_InterruptSource I2C_getInterruptSource (uint32_t base)
- void I2C_initMaster (uint32_t base, uint32_t sysclkHz, uint32_t bitRate, I2C_DutyCycle dutyCycle)
- void I2C_enableInterrupt (uint32_t base, uint32_t intFlags)
- void I2C_disableInterrupt (uint32_t base, uint32_t intFlags)
- uint32_t I2C_getInterruptStatus (uint32_t base)
- void I2C_clearInterruptStatus (uint32_t base, uint32_t intFlags)

21.2.1 Detailed Description

Before initializing the I2C module, the user first must put the module into the reset state by calling I2C_disableModule(). When using the API in master mode, the user must then call I2C_initMaster() which will configure the rate and duty cycle of the master clock. For slave mode, I2C_setOwnSlaveAddress() will need to be called to set the module's address.

For both modes, this is also the time to do any FIFO or interrupt configuration. FIFOs are configured using I2C_enableFIFO() and I2C_disableFIFO() and I2C_setFIFOInterruptLevel() if interrupts are desired. The functions I2C_enableInterrupt(), I2C_disableInterrupt(), I2C_clearInterruptStatus(), and I2C_getInterruptStatus() are for management of interrupts. Note that the I2C module uses separate interrupt lines for its basic and FIFO interrupts although the functions to configure them are the same.

When configuration is complete, I2C_enableModule() should be called to enable the operation of the module.

To do a transfer, for both master and slave modes, I2C_setConfig() should be called to configure the behavior of the module. A master will need to set I2C_setSlaveAddress() to set the address of the slave to which it will communicate. I2C_putData() will place data in the transmit buffer. A start condition can be sent by a master using I2C_sendStartCondition().

When receiving data, the status of data received can be checked using I2C_getStatus() or if in FIFO mode, I2C_getRxFIFOStatus(). I2C_getData() will read the data from the receive buffer and return it.

The code for this module is contained in `driverlib/i2c.c`, with `driverlib/i2c.h` containing the API declarations for use by applications.

21.2.2 Enumeration Type Documentation

21.2.2.1 enum **I2C_InterruptSource**

I2C interrupts to be returned by I2C_getInterruptSource().

Enumerator

I2C_INTSRC_NONE No interrupt pending.
I2C_INTSRC_ARB_LOST Arbitration-lost interrupt.
I2C_INTSRC_NO_ACK NACK interrupt.
I2C_INTSRC_REG_ACCESS_RDY Register-access-ready interrupt.
I2C_INTSRC_RX_DATA_RDY Receive-data-ready interrupt.
I2C_INTSRC_TX_DATA_RDY Transmit-data-ready interrupt.
I2C_INTSRC_STOP_CONDITION Stop condition detected.
I2C_INTSRC_ADDR_SLAVE Addressed as slave interrupt.

21.2.2.2 enum **I2C_TxFIFOLevel**

Values that can be passed to I2C_setFIFOInterruptLevel() as the *txLevel* parameter, returned by I2C_getFIFOInterruptLevel() in the *txLevel* parameter, and returned by I2C_getTxFIFOStatus().

Enumerator

I2C_FIFO_TXEMPTY Transmit FIFO empty.
I2C_FIFO_TX0 Transmit FIFO empty.
I2C_FIFO_TX1 Transmit FIFO 1/16 full.
I2C_FIFO_TX2 Transmit FIFO 2/16 full.
I2C_FIFO_TX3 Transmit FIFO 3/16 full.
I2C_FIFO_TX4 Transmit FIFO 4/16 full.
I2C_FIFO_TX5 Transmit FIFO 5/16 full.
I2C_FIFO_TX6 Transmit FIFO 6/16 full.
I2C_FIFO_TX7 Transmit FIFO 7/16 full.
I2C_FIFO_TX8 Transmit FIFO 8/16 full.
I2C_FIFO_TX9 Transmit FIFO 9/16 full.
I2C_FIFO_TX10 Transmit FIFO 10/16 full.
I2C_FIFO_TX11 Transmit FIFO 11/16 full.
I2C_FIFO_TX12 Transmit FIFO 12/16 full.
I2C_FIFO_TX13 Transmit FIFO 13/16 full.
I2C_FIFO_TX14 Transmit FIFO 14/16 full.
I2C_FIFO_TX15 Transmit FIFO 15/16 full.

I2C_FIFO_TX16 Transmit FIFO full.

I2C_FIFO_TXFULL Transmit FIFO full.

21.2.2.3 enum **I2C_RxFIFOLevel**

Values that can be passed to I2C_setFIFOInterruptLevel() as the *rxLevel* parameter, returned by I2C_getFIFOInterruptLevel() in the *rxLevel* parameter, and returned by I2C_getRxFIFOStatus().

Enumerator

I2C_FIFO_RXEMPTY Receive FIFO empty.

I2C_FIFO_RX0 Receive FIFO empty.

I2C_FIFO_RX1 Receive FIFO 1/16 full.

I2C_FIFO_RX2 Receive FIFO 2/16 full.

I2C_FIFO_RX3 Receive FIFO 3/16 full.

I2C_FIFO_RX4 Receive FIFO 4/16 full.

I2C_FIFO_RX5 Receive FIFO 5/16 full.

I2C_FIFO_RX6 Receive FIFO 6/16 full.

I2C_FIFO_RX7 Receive FIFO 7/16 full.

I2C_FIFO_RX8 Receive FIFO 8/16 full.

I2C_FIFO_RX9 Receive FIFO 9/16 full.

I2C_FIFO_RX10 Receive FIFO 10/16 full.

I2C_FIFO_RX11 Receive FIFO 11/16 full.

I2C_FIFO_RX12 Receive FIFO 12/16 full.

I2C_FIFO_RX13 Receive FIFO 13/16 full.

I2C_FIFO_RX14 Receive FIFO 14/16 full.

I2C_FIFO_RX15 Receive FIFO 15/16 full.

I2C_FIFO_RX16 Receive FIFO full.

I2C_FIFO_RXFULL Receive FIFO full.

21.2.2.4 enum **I2C_BitCount**

Values that can be passed to I2C_setBitCount() as the *size* parameter.

Enumerator

I2C_BITCOUNT_1 1 bit per data byte

I2C_BITCOUNT_2 2 bits per data byte

I2C_BITCOUNT_3 3 bits per data byte

I2C_BITCOUNT_4 4 bits per data byte

I2C_BITCOUNT_5 5 bits per data byte

I2C_BITCOUNT_6 6 bits per data byte

I2C_BITCOUNT_7 7 bits per data byte

I2C_BITCOUNT_8 8 bits per data byte

21.2.2.5 enum **I2C_AddressMode**

Values that can be passed to I2C_setAddressMode() as the *mode* parameter.

Enumerator

I2C_ADDR_MODE_7BITS 7-bit address

I2C_ADDR_MODE_10BITS 10-bit address

21.2.2.6 enum **I2C_EmulationMode**

Values that can be passed to I2C_setEmulationMode() as the *mode* parameter.

Enumerator

I2C_EMULATION_STOP_SCL_LOW If SCL is low, keep it low. If high, stop when it goes low again.

I2C_EMULATION_FREE_RUN Continue I2C operation regardless.

21.2.2.7 enum **I2C_DutyCycle**

Values that can be passed to I2C_initMaster() as the *dutyCycle* parameter.

Enumerator

I2C_DUTYCYCLE_33 Clock duty cycle is 33%.

I2C_DUTYCYCLE_50 Clock duty cycle is 55%.

21.2.3 Function Documentation

21.2.3.1 static void I2C_enableModule (uint32_t *base*) [inline], [static]

Enables the I2C module.

Parameters

base	is the base address of the I2C instance used.

This function enables operation of the I2C module.

Returns

None.

21.2.3.2 static void I2C_disableModule (uint32_t *base*) [inline], [static]

Disables the I2C module.

Parameters

base	is the base address of the I2C instance used.

This function disables operation of the I2C module.

Returns

None.

21.2.3.3 static void I2C_enableFIFO (uint32_t *base*) [inline], [static]

Enables the transmit and receive FIFOs.

Parameters

base	is the base address of the I2C instance used.

This functions enables the transmit and receive FIFOs in the I2C.

Returns

None.

21.2.3.4 static void I2C_disableFIFO (uint32_t *base*) [inline], [static]

Disables the transmit and receive FIFOs.

Parameters

base	is the base address of the I2C instance used.

This functions disables the transmit and receive FIFOs in the I2C.

Returns

None.

21.2.3.5 static void I2C_setFIFOInterruptLevel (uint32_t *base*, **I2C_TxFIFOLevel** *txLevel*, **I2C_RxFIFOLevel** *rxLevel*) [inline], [static]

Sets the FIFO level at which interrupts are generated.

Parameters

base	is the base address of the I2C instance used.
txLevel	is the transmit FIFO interrupt level, specified as **I2C_FIFO_TX0**, **I2C_FIFO_TX1**, **I2C_FIFO_TX2**, . . . or **I2C_FIFO_TX16**.
rxLevel	is the receive FIFO interrupt level, specified as **I2C_FIFO_RX0**, **I2C_FIFO_RX1**, **I2C_FIFO_RX2**, . . . or **I2C_FIFO_RX16**.

This function sets the FIFO level at which transmit and receive interrupts are generated. The transmit FIFO interrupt flag will be set when the FIFO reaches a value less than or equal to *txLevel*. The receive FIFO flag will be set when the FIFO reaches a value greater than or equal to *rxLevel*.

Returns

None.

21.2.3.6 static void I2C_getFIFOInterruptLevel (uint32_t *base*, **I2C_TxFIFOLevel** ∗ *txLevel*, **I2C_RxFIFOLevel** ∗ *rxLevel*) `[inline]`, `[static]`

Gets the FIFO level at which interrupts are generated.

Parameters

base	is the base address of the I2C instance used.
txLevel	is a pointer to storage for the transmit FIFO level, returned as one of **I2C_FIFO_TX0**, **I2C_FIFO_TX1**, **I2C_FIFO_TX2**, . . . or **I2C_FIFO_TX16**.
rxLevel	is a pointer to storage for the receive FIFO level, returned as one of **I2C_FIFO_RX0**, **I2C_FIFO_RX1**, **I2C_FIFO_RX2**, . . . or **I2C_FIFO_RX16**.

This function gets the FIFO level at which transmit and receive interrupts are generated. The transmit FIFO interrupt flag will be set when the FIFO reaches a value less than or equal to *txLevel*. The receive FIFO flag will be set when the FIFO reaches a value greater than or equal to *rxLevel*.

Returns

None.

21.2.3.7 static **I2C_TxFIFOLevel** I2C_getTxFIFOStatus (uint32_t *base*) `[inline]`, `[static]`

Get the transmit FIFO status

Parameters

base	is the base address of the I2C instance used.

This function gets the current number of words in the transmit FIFO.

Returns

Returns the current number of words in the transmit FIFO specified as one of the following: **I2C_FIFO_TX0**, **I2C_FIFO_TX1**, **I2C_FIFO_TX2**, **I2C_FIFO_TX3**, ..., or **I2C_FIFO_TX16**

21.2.3.8 static **I2C_RxFIFOLevel** I2C_getRxFIFOStatus (uint32_t *base*) `[inline]`, `[static]`

Get the receive FIFO status

Parameters

base	is the base address of the I2C instance used.

This function gets the current number of words in the receive FIFO.

Returns

Returns the current number of words in the receive FIFO specified as one of the following: **I2C_FIFO_RX0**, **I2C_FIFO_RX1**, **I2C_FIFO_RX2**, **I2C_FIFO_RX3**, ..., or **I2C_FIFO_RX16**

21.2.3.9 static void I2C_setSlaveAddress (uint32_t *base*, uint16_t *slaveAddr*) `[inline]`, `[static]`

Sets the address that the I2C Master places on the bus.

Parameters

base	is the base address of the I2C instance used.
slaveAddr	7-bit or 10-bit slave address

This function configures the address that the I2C Master places on the bus when initiating a transaction.

Returns

None.

21.2.3.10 static void I2C_setOwnSlaveAddress (uint32_t *base,* uint16_t *slaveAddr*) [inline], [static]

Sets the slave address for this I2C module.

Parameters

base	is the base address of the I2C Slave module.
slaveAddr	is the 7-bit or 10-bit slave address

This function writes the specified slave address.

The parameter *slaveAddr* is the value that is compared against the slave address sent by an I2C master.

Returns

None.

21.2.3.11 static bool I2C_isBusBusy (uint32_t *base*) [inline], [static]

Indicates whether or not the I2C bus is busy.

Parameters

base	is the base address of the I2C instance used.

This function returns an indication of whether or not the I2C bus is busy. This function can be used in a multi-master environment to determine if the bus is free for another data transfer.

Returns

Returns **true** if the I2C bus is busy; otherwise, returns **false**.

21.2.3.12 static uint16_t I2C_getStatus (uint32_t *base*) [inline], [static]

Gets the current I2C module status.

Parameters

base	is the base address of the I2C instance used.

This function returns the status for the I2C module.

Returns

The current module status, enumerated as a bit field of

- **I2C_STS_ARB_LOST** - Arbitration-lost
- **I2C_STS_NO_ACK** - No-acknowledgment (NACK)
- **I2C_STS_REG_ACCESS_RDY** - Register-access-ready (ARDY)
- **I2C_STS_RX_DATA_RDY** - Receive-data-ready
- **I2C_STS_TX_DATA_RDY** - Transmit-data-ready
- **I2C_STS_STOP_CONDITION** - Stop condition detected
- **I2C_STS_ADDR_ZERO** - Address of all zeros detected
- **I2C_STS_ADDR_SLAVE** - Addressed as slave
- **I2C_STS_TX_EMPTY** - Transmit shift register empty
- **I2C_STS_RX_FULL** - Receive shift register full
- **I2C_STS_BUS_BUSY** - Bus busy, wait for STOP or reset
- **I2C_STS_NACK_SENT** - NACK was sent
- **I2C_STS_SLAVE_DIR-** Addressed as slave transmitter

21.2.3.13 static void I2C_clearStatus (uint32_t *base,* uint16_t *stsFlags*) `[inline]`, `[static]`

Clears I2C status flags.

Parameters

base	is the base address of the I2C instance used.
stsFlags	is a bit mask of the status flags to be cleared.

This function clears the specified I2C status flags. The *stsFlags* parameter is the logical OR of the following values:

- **I2C_STS_ARB_LOST**
- **I2C_STS_NO_ACK**,
- **I2C_STS_REG_ACCESS_RDY**
- **I2C_STS_RX_DATA_RDY**
- **I2C_STS_STOP_CONDITION**
- **I2C_STS_NACK_SENT**
- **I2C_STS_SLAVE_DIR**

Note

Note that some of the status flags returned by I2C_getStatus() cannot be cleared by this function. Some may only be cleared by hardware or a reset of the I2C module.

Returns

None.

21.2.3.14 static void I2C_setConfig (uint32_t *base,* uint16_t *config*) `[inline]`, `[static]`

Controls the state of the I2C module.

Parameters

base	is the base address of the I2C instance used.
config	is the command to be issued to the I2C module.

This function is used to control the state of the master and slave send and receive operations. The *config* is a logical OR of the following options.

One of the following four options:

- **I2C_MASTER_SEND_MODE** - Master-transmitter mode
- **I2C_MASTER_RECEIVE_MODE** - Master-receiver mode
- **I2C_SLAVE_SEND_MODE** - Slave-transmitter mode
- **I2C_SLAVE_RECEIVE_MODE** - Slave-receiver mode

Any of the following:

- **I2C_REPEAT_MODE** - Sends data until stop bit is set, ignores data count
- **I2C_START_BYTE_MODE** - Use start byte mode
- **I2C_FREE_DATA_FORMAT** - Use free data format, transfers have no address

Returns

None.

21.2.3.15 static void I2C_setBitCount (uint32_t *base*, **I2C_BitCount** *size*) `[inline]`, `[static]`

Sets the data byte bit count the I2C module.

Parameters

base	is the base address of the I2C instance used.
size	is the number of bits per data byte.

The *size* parameter is a value I2C_BITCOUNT_x where x is the number of bits per data byte. The default and maximum size is 8 bits.

Returns

None.

21.2.3.16 static void I2C_sendStartCondition (uint32_t *base*) `[inline]`, `[static]`

Issues an I2C START condition.

Parameters

base	is the base address of the I2C instance used.

This function causes the I2C module to generate a start condition. This function is only valid when the I2C module specified by the **base** parameter is a master.

Returns

None.

21.2.3.17 static void I2C_sendStopCondition (uint32_t *base*) [inline], [static]

Issues an I2C STOP condition.

Parameters

base	is the base address of the I2C instance used.

This function causes the I2C module to generate a stop condition. This function is only valid when the I2C module specified by the **base** parameter is a master.

To check on the status of the STOP condition, I2C_getStopConditionStatus() can be used.

Returns
None.

21.2.3.18 static void I2C_sendNACK (uint32_t *base*) [inline], [static]

Issues a no-acknowledge (NACK) bit.

Parameters

base	is the base address of the I2C instance used.

This function causes the I2C module to generate a NACK bit. This is only applicable when the I2C module is acting as a receiver.

Returns
None.

21.2.3.19 static uint16_t I2C_getData (uint32_t *base*) [inline], [static]

Receives a byte that has been sent to the I2C.

Parameters

base	is the base address of the I2C instance used.

This function reads a byte of data from the I2C Data Receive Register.

Returns
Returns the byte received from by the I2C cast as an uint16_t.

21.2.3.20 static void I2C_putData (uint32_t *base*, uint16_t *data*) [inline], [static]

Transmits a byte from the I2C.

Parameters

base	is the base address of the I2C instance used.
data	is the data to be transmitted from the I2C Master.

This function places the supplied data into I2C Data Transmit Register.

Returns
None.

21.2.3.21 static bool I2C_getStopConditionStatus (uint32_t *base*) [inline], [static]

Get stop condition status.

Parameters

base	is the base address of the I2C instance used.

This function reads and returns the stop condition bit status.

Returns

Returns **true** if the STP bit has been set by the device to generate a stop condition when the internal data counter of the I2C module has reached 0. Returns **false** when the STP bit is zero. This bit is automatically cleared after the stop condition has been generated.

21.2.3.22 static void I2C_setDataCount (uint32_t *base,* uint16_t *count*) [inline], [static]

Set number of bytes to be to transfer or receive when repeat mode is off.

Parameters

base	is the base address of the I2C instance used.
count	is the value to be put in the I2C data count register.

This function sets the number of bytes to transfer or receive when repeat mode is off.

Returns

None.

21.2.3.23 static void I2C_setAddressMode (uint32_t *base,* **I2C_AddressMode** *mode*) [inline], [static]

Sets the addressing mode to either 7-bit or 10-bit.

Parameters

base	is the base address of the I2C instance used.
mode	is the address mode, 7-bit or 10-bit.

This function configures the I2C module for either a 7-bit address (default) or a 10-bit address. The *mode* parameter configures the address length to 10 bits when its value is **I2C_ADDR_MODE_10BITS** and 7 bits when **I2C_ADDR_MODE_7BITS**.

Returns

None.

21.2.3.24 static void I2C_setEmulationMode (uint32_t *base,* **I2C_EmulationMode** *mode*) [inline], [static]

Sets I2C emulation mode.

Parameters

base	is the base address of the I2C instance used.
mode	is the emulation mode.

This function sets the behavior of the I2C operation when an emulation suspend occurs. The *mode* parameter can be one of the following:

- **I2C_EMULATION_STOP_SCL_LOW** - If SCL is low when the breakpoint occurs, the I2C module stops immediately. If SCL is high, the I2C module waits until SCL becomes low and then stops.
- **I2C_EMULATION_FREE_RUN** - I2C operation continues regardless of a the suspend.

Returns

None.

21.2.3.25 static void I2C_enableLoopback (uint32_t *base*) [inline], [static]

Enables I2C loopback mode.

Parameters

base	is the base address of the I2C instance used.

This function enables loopback mode. This mode is only valid during master mode and is helpful during device testing as it causes data transmitted out of the data transmit register to be received in data receive register.

Returns

None.

21.2.3.26 static void I2C_disableLoopback (uint32_t *base*) [inline], [static]

Disables I2C loopback mode.

Parameters

base	is the base address of the I2C instance used.

This function disables loopback mode. Loopback mode is disabled by default after reset.

Returns

None.

21.2.3.27 static **I2C_InterruptSource** I2C_getInterruptSource (uint32_t *base*) [inline], [static]

Returns the current I2C interrupt source.

Parameters

base	is the base address of the I2C instance used.

This function returns the event that generated an I2C basic (non-FIFO) interrupt. The possible sources are the following:

- **I2C_INTSRC_NONE**
- **I2C_INTSRC_ARB_LOST**
- **I2C_INTSRC_NO_ACK**
- **I2C_INTSRC_REG_ACCESS_RDY**
- **I2C_INTSRC_RX_DATA_RDY**
- **I2C_INTSRC_TX_DATA_RDY**
- **I2C_INTSRC_STOP_CONDITION**
- **I2C_INTSRC_ADDR_SLAVE**

Calling this function will result in hardware automatically clearing the current interrupt code and if ready, loading the next pending enabled interrupt. It will also clear the corresponding interrupt flag if the source is **I2C_INTSRC_ARB_LOST**, **I2C_INTSRC_NO_ACK**, or **I2C_INTSRC_STOP_CONDITION**.

Note

Note that this function differs from I2C_getInterruptStatus() in that it returns a single interrupt source. I2C_getInterruptSource() will return the status of all interrupt flags possible, including the flags that aren't necessarily enabled to generate interrupts.

Returns

None.

21.2.3.28 void I2C_initMaster (uint32_t *base,* uint32_t *sysclkHz,* uint32_t *bitRate,* **I2C_DutyCycle** *dutyCycle*)

Initializes the I2C Master.

Parameters

base	is the base address of the I2C instance used.
sysclkHz	is the rate of the clock supplied to the I2C module (SYSCLK) in Hz.
bitRate	is the rate of the master clock signal, SCL.
dutyCycle	is duty cycle of the SCL signal.

This function initializes operation of the I2C Master by configuring the bus speed for the master. Note that the I2C module **must** be put into reset before calling this function. You can do this with the function I2C_disableModule().

A programmable prescaler in the I2C module divides down the input clock (rate specified by *sysclkHz*) to produce the module clock (calculated to be around 10 MHz in this function). That clock is then divided down further to configure the SCL signal to run at the rate specified by *bitRate*. The *dutyCycle* parameter determines the percentage of time high and time low on the clock signal. The valid values are **I2C_DUTYCYCLE_33** for 33% and **I2C_DUTYCYCLE_50** for 50%.

The peripheral clock is the system clock. This value is returned by SysCtl_getClock(), or it can be explicitly hard coded if it is constant and known (to save the code/execution overhead of a call to SysCtl_getClock()).

Returns

None.

References I2C_DUTYCYCLE_50.

21.2.3.29 void I2C_enableInterrupt (uint32_t *base*, uint32_t *intFlags*)

Enables I2C interrupt sources.

Parameters

base	is the base address of the I2C instance used.
intFlags	is the bit mask of the interrupt sources to be enabled.

This function enables the indicated I2C Master interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt. Disabled sources have no effect on the processor.

The *intFlags* parameter is the logical OR of any of the following:

- **I2C_INT_ARB_LOST** - Arbitration-lost interrupt
- **I2C_INT_NO_ACK** - No-acknowledgment (NACK) interrupt
- **I2C_INT_REG_ACCESS_RDY** - Register-access-ready interrupt
- **I2C_INT_RX_DATA_RDY** - Receive-data-ready interrupt
- **I2C_INT_TX_DATA_RDY** - Transmit-data-ready interrupt
- **I2C_INT_STOP_CONDITION** - Stop condition detected
- **I2C_INT_ADDR_SLAVE** - Addressed as slave interrupt
- **I2C_INT_RXFF** - RX FIFO level interrupt
- **I2C_INT_TXFF** - TX FIFO level interrupt

Note

I2C_INT_RXFF and **I2C_INT_TXFF** are associated with the I2C FIFO interrupt vector. All others are associated with the I2C basic interrupt.

Returns

None.

21.2.3.30 void I2C_disableInterrupt (uint32_t *base*, uint32_t *intFlags*)

Disables I2C interrupt sources.

Parameters

base	is the base address of the I2C instance used.
intFlags	is the bit mask of the interrupt sources to be disabled.

This function disables the indicated I2C Slave interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt. Disabled sources have no effect on the processor.

The *intFlags* parameter has the same definition as the *intFlags* parameter to I2C_enableInterrupt().

Returns

None.

21.2.3.31 uint32_t I2C_getInterruptStatus (uint32_t *base*)

Gets the current I2C interrupt status.

Parameters

base	is the base address of the I2C instance used.

This function returns the interrupt status for the I2C module.

Returns

The current interrupt status, enumerated as a bit field of

- **I2C_INT_ARB_LOST**
- **I2C_INT_NO_ACK**
- **I2C_INT_REG_ACCESS_RDY**
- **I2C_INT_RX_DATA_RDY**
- **I2C_INT_TX_DATA_RDY**
- **I2C_INT_STOP_CONDITION**
- **I2C_INT_ADDR_SLAVE**
- **I2C_INT_RXFF**
- **I2C_INT_TXFF**

Note

This function will only return the status flags associated with interrupts. However, a flag may be set even if its corresponding interrupt is disabled.

21.2.3.32 void I2C_clearInterruptStatus (uint32_t *base,* uint32_t *intFlags*)

Clears I2C interrupt sources.

Parameters

base	is the base address of the I2C instance used.
intFlags	is a bit mask of the interrupt sources to be cleared.

The specified I2C interrupt sources are cleared, so that they no longer assert. This function must be called in the interrupt handler to keep the interrupt from being triggered again immediately upon exit.

The *intFlags* parameter has the same definition as the *intFlags* parameter to I2C_enableInterrupt().

Note

I2C_INT_RXFF and **I2C_INT_TXFF** are associated with the I2C FIFO interrupt vector. All others are associated with the I2C basic interrupt.
Also note that some of the status flags returned by I2C_getInterruptStatus() cannot be cleared by this function. Some may only be cleared by hardware or a reset of the I2C module.

Returns

None.

22 Interrupt Module

22.1 Interrupt Introduction

The Interrupt API provides a set of functions for dealing with the Peripheral Interrupt Expansion (PIE) Controller as well as CPU-level interrupt configuration. Functions are provided to initialize interrupt-related registers, enable and disable interrupts, and register interrupt handlers.

Interrupt API functions rely on an interrupt number defined to specify which interrupt is being configured. These interrupt numbers are found in inc/hw_ints.h and are in the format **INT_X**. For example, **INT_EPWM2_TZ** would be used to specify the trip zone interrupt for EPWM2 wherever a function has an interruptNumber parameter.

22.2 API Functions

Functions

- static bool Interrupt_enableMaster (void)
- static bool Interrupt_disableMaster (void)
- static void Interrupt_register (uint32_t interruptNumber, void(∗handler)(void))
- static void Interrupt_unregister (uint32_t interruptNumber)
- static void Interrupt_enableInCPU (uint16_t cpuInterrupt)
- static void Interrupt_disableInCPU (uint16_t cpuInterrupt)
- static void Interrupt_clearACKGroup (uint16_t group)
- void Interrupt_initModule (void)
- void Interrupt_initVectorTable (void)
- void Interrupt_enable (uint32_t interruptNumber)
- void Interrupt_disable (uint32_t interruptNumber)

22.2.1 Detailed Description

The Interrupt_ API provides two functions to initialize the module, Interrupt_initModule() and Interrupt_initVectorTable(). The former puts the PIE registers and the interrupt-related registers in the CPU into a known state. It clears all flags, disables interrupts at all levels, and enables vector fetching from the PIE. The latter initializes the PIE Vector Table to a set of default handlers–Interrupt_nmiHandler() for non-maskable interrupts, Interrupt_illegalOperationHandler() for an ITRAP interrupt, and Interrupt_defaultHandler() for all others. These defaults are intended to help with debugging. They should be modified or replaced more appropriate ISRs by the user.

Each interrupt source can be individually enabled and disabled via Interrupt_enable() and Interrupt_disable(). These affect the interrupt both on the PIE and on the CPU's IER register. The processor interrupt can be enabled and disabled via Interrupt_enableMaster() and Interrupt_disableMaster(); this does not affect the individual interrupt enable states. Masking of the processor interrupt can be utilized as a simple critical section (only NMI will interrupt the processor while the processor interrupt is disabled), though this will have adverse effects on the interrupt response time.

When an interrupt occurs, in order for further interrupts on its PIE group to be received, Interrupt_clearACKGroup() must be called. This is typically done at the end of the ISR.

The code for this module is contained in `driverlib/interrupt.c`, with `driverlib/interrupt.h` containing the API declarations for use by applications.

22.2.2 Function Documentation

22.2.2.1 static bool Interrupt_enableMaster (void) `[inline]`, `[static]`

Allows the CPU to process interrupts.

This function clears the global interrupt mask bit (INTM) in the CPU, allowing the processor to respond to interrupts.

Returns

Returns **true** if interrupts were disabled when the function was called or **false** if they were initially enabled.

Referenced by Interrupt_disable(), and Interrupt_enable().

22.2.2.2 static bool Interrupt_disableMaster (void) `[inline]`, `[static]`

Stops the CPU from processing interrupts.

This function sets the global interrupt mask bit (INTM) in the CPU, preventing the processor from receiving maskable interrupts.

Returns

Returns **true** if interrupts were already disabled when the function was called or **false** if they were initially enabled.

Referenced by Interrupt_disable(), Interrupt_enable(), and Interrupt_initModule().

22.2.2.3 static void Interrupt_register (uint32_t *interruptNumber,* void(∗)(void) *handler*) `[inline]`, `[static]`

Registers a function to be called when an interrupt occurs.

Parameters

interruptNumber	specifies the interrupt in question.
handler	is a pointer to the function to be called.

This function is used to specify the handler function to be called when the given interrupt is asserted to the processor. When the interrupt occurs, if it is enabled (via Interrupt_enable()), the handler function will be called in interrupt context. Since the handler function can preempt other code, care must be taken to protect memory or peripherals that are accessed by the handler and other non-handler code.

The available *interruptNumber* values are supplied in `inc/hw_ints.h`.

Note

This function assumes that the PIE has been enabled. See Interrupt_initModule().

Returns

None.

22.2.2.4 static void Interrupt_unregister (uint32_t *interruptNumber*) [inline], [static]

Unregisters the function to be called when an interrupt occurs.

Parameters

interruptNumber	specifies the interrupt in question.

This function is used to indicate that a default handler Interrupt_defaultHandler() should be called when the given interrupt is asserted to the processor. Call Interrupt_disable() to disable the interrupt before calling this function.

The available *interruptNumber* values are supplied in `inc/hw_ints.h`.

See Also

Interrupt_register() for important information about registering interrupt handlers.

Returns

None.

22.2.2.5 static void Interrupt_enableInCPU (uint16_t *cpuInterrupt*) [inline], [static]

Enables CPU interrupt channels

Parameters

cpuInterrupt	specifies the CPU interrupts to be enabled.

This function enables the specified interrupts in the CPU. The *cpuInterrupt* parameter is a logical OR of the values **INTERRUPT_CPU_INTx** where x is the interrupt number between 1 and 14, **INTERRUPT_CPU_DLOGINT**, and **INTERRUPT_CPU_RTOSINT**.

Note

Note that interrupts 1-12 correspond to the PIE groups with those same numbers.

Returns

None.

22.2.2.6 static void Interrupt_disableInCPU (uint16_t *cpuInterrupt*) [inline], [static]

Disables CPU interrupt channels

Parameters

cpuInterrupt	specifies the CPU interrupts to be disabled.

This function disables the specified interrupts in the CPU. The *cpuInterrupt* parameter is a logical OR of the values **INTERRUPT_CPU_INTx** where x is the interrupt number between 1 and 14, **INTERRUPT_CPU_DLOGINT**, and **INTERRUPT_CPU_RTOSINT**.

Note

Note that interrupts 1-12 correspond to the PIE groups with those same numbers.

Returns

None.

22.2.2.7 static void Interrupt_clearACKGroup (uint16_t *group*) [inline], [static]

Acknowledges PIE Interrupt Group

Parameters

group	specifies the interrupt group to be acknowledged.

The specified interrupt group is acknowledged and clears any interrupt flag within that respective group.

The *group* parameter must be a logical OR of the following: **INTERRUPT_ACK_GROUP1**, **INTERRUPT_ACK_GROUP2**, **INTERRUPT_ACK_GROUP3** **INTERRUPT_ACK_GROUP4**, **INTERRUPT_ACK_GROUP5**, **INTERRUPT_ACK_GROUP6** **INTERRUPT_ACK_GROUP7**, **INTERRUPT_ACK_GROUP8**, **INTERRUPT_ACK_GROUP9** **INTERRUPT_ACK_GROUP10**, **INTERRUPT_ACK_GROUP11**, **INTERRUPT_ACK_GROUP12**.

Returns

None.

22.2.2.8 void Interrupt_initModule (void)

Initializes the PIE control registers by setting them to a known state.

This function initializes the PIE control registers. After globally disabling interrupts and enabling the PIE, it clears all of the PIE interrupt enable bits and interrupt flags.

Returns

None.

References Interrupt_disableMaster().

22.2.2.9 void Interrupt_initVectorTable (void)

Initializes the PIE vector table by setting all vectors to a default handler function.

Returns

None.

22.2.2.10 void Interrupt_enable (uint32_t *interruptNumber*)

Enables an interrupt.

Parameters

interruptNumber	specifies the interrupt to be enabled.

The specified interrupt is enabled in the interrupt controller. Other enables for the interrupt (such as at the peripheral level) are unaffected by this function.

The available *interruptNumber* values are supplied in `inc/hw_ints.h`.

Returns

None.

References Interrupt_disableMaster(), and Interrupt_enableMaster().

22.2.2.11 void Interrupt_disable (uint32_t *interruptNumber*)

Disables an interrupt.

Parameters

interruptNumber	specifies the interrupt to be disabled.

The specified interrupt is disabled in the interrupt controller. Other enables for the interrupt (such as at the peripheral level) are unaffected by this function.

The available *interruptNumber* values are supplied in `inc/hw_ints.h`.

Returns

None.

References Interrupt_disableMaster(), and Interrupt_enableMaster().

23 McBSP Module

23.1 McBSP Introduction

The Multichannel Buffered Serial Port (McBSP) API provides a set of functions to configure device's McBSP module. The driver provides functions to initialize the module, configure module Transmitter, Receiver and Sample Rate Generator, obtain status/error information and to manage interrupts. APIs are also available to configure McBSP in SPI mode. */

23.2 API Functions

Data Structures

- struct McBSP_ClockParams
- struct McBSP_TxFsyncParams
- struct McBSP_RxFsyncParams
- struct McBSP_TxDataParams
- struct McBSP_RxDataParams
- struct McBSP_RxMultichannelParams
- struct McBSP_TxMultichannelParams
- struct McBSP_SPIMasterModeParams
- struct McBSP_SPISlaveModeParams

Macros

- #define MCBSP_RX_NO_ERROR
- #define MCBSP_RX_BUFFER_ERROR
- #define MCBSP_RX_FRAME_SYNC_ERROR
- #define MCBSP_RX_BUFFER_FRAME_SYNC_ERROR
- #define MCBSP_TX_NO_ERROR
- #define MCBSP_TX_BUFFER_ERROR
- #define MCBSP_TX_FRAME_SYNC_ERROR
- #define MCBSP_TX_BUFFER_FRAME_SYNC_ERROR
- #define MCBSP_ERROR_EXCEEDED_CHANNELS
- #define MCBSP_ERROR_2_PARTITION_A
- #define MCBSP_ERROR_2_PARTITION_B
- #define MCBSP_ERROR_INVALID_MODE

Enumerations

- enum McBSP_RxSignExtensionMode { MCBSP_RIGHT_JUSTIFY_FILL_ZERO, MCBSP_RIGHT_JUSTIFY_FILL_SIGN, MCBSP_LEFT_JUSTIFY_FILL_ZER0 }

- enum McBSP_ClockStopMode { MCBSP_CLOCK_MCBSP_MODE, MCBSP_CLOCK_SPI_MODE_NO_DELAY, MCBSP_CLOCK_SPI_MODE_DELAY }
- enum McBSP_RxInterruptSource { MCBSP_RX_ISR_SOURCE_SERIAL_WORD, MCBSP_RX_ISR_SOURCE_END_OF_BLOCK, MCBSP_RX_ISR_SOURCE_FRAME_SYNC, MCBSP_RX_ISR_SOURCE_SYNC_ERROR }
- enum McBSP_EmulationMode { MCBSP_EMULATION_IMMEDIATE_STOP, MCBSP_EMULATION_SOFT_STOP, MCBSP_EMULATION_FREE_RUN }
- enum McBSP_TxInterruptSource { MCBSP_TX_ISR_SOURCE_TX_READY, MCBSP_TX_ISR_SOURCE_END_OF_BLOCK, MCBSP_TX_ISR_SOURCE_FRAME_SYNC, MCBSP_TX_ISR_SOURCE_SYNC_ERROR }
- enum McBSP_DataPhaseFrame { MCBSP_PHASE_ONE_FRAME, MCBSP_PHASE_TWO_FRAME }
- enum McBSP_DataBitsPerWord { MCBSP_BITS_PER_WORD_8, MCBSP_BITS_PER_WORD_12, MCBSP_BITS_PER_WORD_16, MCBSP_BITS_PER_WORD_20, MCBSP_BITS_PER_WORD_24, MCBSP_BITS_PER_WORD_32 }
- enum McBSP_CompandingMode { MCBSP_COMPANDING_NONE, MCBSP_COMPANDING_NONE_LSB_FIRST, MCBSP_COMPANDING_U_LAW_SET, MCBSP_COMPANDING_A_LAW_SET }
- enum McBSP_DataDelayBits { MCBSP_DATA_DELAY_BIT_0, MCBSP_DATA_DELAY_BIT_1, MCBSP_DATA_DELAY_BIT_2 }
- enum McBSP_SRGRxClockSource { MCBSP_SRG_RX_CLOCK_SOURCE_LSPCLK, MCBSP_SRG_RX_CLOCK_SOURCE_MCLKX_PIN }
- enum McBSP_SRGTxClockSource { MCBSP_SRG_TX_CLOCK_SOURCE_LSPCLK, MCBSP_SRG_TX_CLOCK_SOURCE_MCLKR_PIN }
- enum McBSP_TxInternalFrameSyncSource { MCBSP_TX_INTERNAL_FRAME_SYNC_DATA, MCBSP_TX_INTERNAL_FRAME_SYNC_SRG }
- enum McBSP_MultichannelPartition { MCBSP_MULTICHANNEL_TWO_PARTITION, MCBSP_MULTICHANNEL_EIGHT_PARTITION }
- enum McBSP_PartitionBlock { MCBSP_PARTITION_BLOCK_0, MCBSP_PARTITION_BLOCK_1, MCBSP_PARTITION_BLOCK_2, MCBSP_PARTITION_BLOCK_3, MCBSP_PARTITION_BLOCK_4, MCBSP_PARTITION_BLOCK_5, MCBSP_PARTITION_BLOCK_6, MCBSP_PARTITION_BLOCK_7 }
- enum McBSP_RxChannelMode { MCBSP_ALL_RX_CHANNELS_ENABLED, MCBSP_RX_CHANNEL_SELECTION_ENABLED }
- enum McBSP_TxChannelMode { MCBSP_ALL_TX_CHANNELS_ENABLED, MCBSP_TX_CHANNEL_SELECTION_ENABLED, MCBSP_ENABLE_MASKED_TX_CHANNEL_SELECTION, MCBSP_SYMMERTIC_RX_TX_SELECTION }
- enum McBSP_TxFrameSyncSource { MCBSP_TX_EXTERNAL_FRAME_SYNC_SOURCE, MCBSP_TX_INTERNAL_FRAME_SYNC_SOURCE }
- enum McBSP_RxFrameSyncSource { MCBSP_RX_EXTERNAL_FRAME_SYNC_SOURCE, MCBSP_RX_INTERNAL_FRAME_SYNC_SOURCE }
- enum McBSP_TxClockSource { MCBSP_EXTERNAL_TX_CLOCK_SOURCE, MCBSP_INTERNAL_TX_CLOCK_SOURCE }
- enum McBSP_RxClockSource { MCBSP_EXTERNAL_RX_CLOCK_SOURCE, MCBSP_INTERNAL_RX_CLOCK_SOURCE }
- enum McBSP_TxFrameSyncPolarity { MCBSP_TX_FRAME_SYNC_POLARITY_HIGH, MCBSP_TX_FRAME_SYNC_POLARITY_LOW }
- enum McBSP_RxFrameSyncPolarity { MCBSP_RX_FRAME_SYNC_POLARITY_HIGH, MCBSP_RX_FRAME_SYNC_POLARITY_LOW }
- enum McBSP_TxClockPolarity { MCBSP_TX_POLARITY_RISING_EDGE, MCBSP_TX_POLARITY_FALLING_EDGE }

- enum McBSP_RxClockPolarity { MCBSP_RX_POLARITY_FALLING_EDGE, MCBSP_RX_POLARITY_RISING_EDGE }
- enum McBSP_CompandingType { MCBSP_COMPANDING_U_LAW, MCBSP_COMPANDING_A_LAW }

Functions

- static void McBSP_disableLoopback (uint32_t base)
- static void McBSP_enableLoopback (uint32_t base)
- static void McBSP_setRxSignExtension (uint32_t base, const McBSP_RxSignExtensionMode mode)
- static void McBSP_setClockStopMode (uint32_t base, const McBSP_ClockStopMode mode)
- static void McBSP_disableDxPinDelay (uint32_t base)
- static void McBSP_enableDxPinDelay (uint32_t base)
- static void McBSP_setRxInterruptSource (uint32_t base, const McBSP_RxInterruptSource interruptSource)
- static void McBSP_clearRxFrameSyncError (uint32_t base)
- static uint16_t McBSP_getRxErrorStatus (uint32_t base)
- static bool McBSP_isRxReady (uint32_t base)
- static void McBSP_resetReceiver (uint32_t base)
- static void McBSP_enableReceiver (uint32_t base)
- static void McBSP_setEmulationMode (uint32_t base, const McBSP_EmulationMode emulationMode)
- static void McBSP_resetFrameSyncLogic (uint32_t base)
- static void McBSP_enableFrameSyncLogic (uint32_t base)
- static void McBSP_resetSampleRateGenerator (uint32_t base)
- static void McBSP_enableSampleRateGenerator (uint32_t base)
- static void McBSP_setTxInterruptSource (uint32_t base, const McBSP_TxInterruptSource interruptSource)
- static uint16_t McBSP_getTxErrorStatus (uint32_t base)
- static void McBSP_clearTxFrameSyncError (uint32_t base)
- static bool McBSP_isTxReady (uint32_t base)
- static void McBSP_resetTransmitter (uint32_t base)
- static void McBSP_enableTransmitter (uint32_t base)
- static void McBSP_disableTwoPhaseRx (uint32_t base)
- static void McBSP_enableTwoPhaseRx (uint32_t base)
- static void McBSP_setRxCompandingMode (uint32_t base, const McBSP_CompandingMode compandingMode)
- static void McBSP_disableRxFrameSyncErrorDetection (uint32_t base)
- static void McBSP_enableRxFrameSyncErrorDetection (uint32_t base)
- static void McBSP_setRxDataDelayBits (uint32_t base, const McBSP_DataDelayBits delayBits)
- static void McBSP_disableTwoPhaseTx (uint32_t base)
- static void McBSP_enableTwoPhaseTx (uint32_t base)
- static void McBSP_setTxCompandingMode (uint32_t base, const McBSP_CompandingMode compandingMode)
- static void McBSP_disableTxFrameSyncErrorDetection (uint32_t base)
- static void McBSP_enableTxFrameSyncErrorDetection (uint32_t base)
- static void McBSP_setTxDataDelayBits (uint32_t base, const McBSP_DataDelayBits delayBits)
- static void McBSP_setFrameSyncPulsePeriod (uint32_t base, uint16_t frameClockDivider)
- static void McBSP_setFrameSyncPulseWidthDivider (uint32_t base, uint16_t pulseWidthDivider)
- static void McBSP_setSRGDataClockDivider (uint32_t base, uint16_t dataClockDivider)
- static void McBSP_disableSRGSyncFSR (uint32_t base)

- static void McBSP_enableSRGSyncFSR (uint32_t base)
- static void McBSP_setRxSRGClockSource (uint32_t base, const McBSP_SRGRxClockSource srgClockSource)
- static void McBSP_setTxSRGClockSource (uint32_t base, const McBSP_SRGTxClockSource srgClockSource)
- static void McBSP_setTxInternalFrameSyncSource (uint32_t base, const McBSP_TxInternalFrameSyncSource syncMode)
- static void McBSP_setRxMultichannelPartition (uint32_t base, const McBSP_MultichannelPartition partition)
- static void McBSP_setRxTwoPartitionBlock (uint32_t base, const McBSP_PartitionBlock block)
- static uint16_t McBSP_getRxActiveBlock (uint32_t base)
- static void McBSP_setRxChannelMode (uint32_t base, const McBSP_RxChannelMode channelMode)
- static void McBSP_setTxMultichannelPartition (uint32_t base, const McBSP_MultichannelPartition partition)
- static void McBSP_setTxTwoPartitionBlock (uint32_t base, const McBSP_PartitionBlock block)
- static uint16_t McBSP_getTxActiveBlock (uint32_t base)
- static void McBSP_setTxChannelMode (uint32_t base, const McBSP_TxChannelMode channelMode)
- static void McBSP_setTxFrameSyncSource (uint32_t base, const McBSP_TxFrameSyncSource syncSource)
- static void McBSP_setRxFrameSyncSource (uint32_t base, const McBSP_RxFrameSyncSource syncSource)
- static void McBSP_setTxClockSource (uint32_t base, const McBSP_TxClockSource clockSource)
- static void McBSP_setRxClockSource (uint32_t base, const McBSP_RxClockSource clockSource)
- static void McBSP_setTxFrameSyncPolarity (uint32_t base, const McBSP_TxFrameSyncPolarity syncPolarity)
- static void McBSP_setRxFrameSyncPolarity (uint32_t base, const McBSP_RxFrameSyncPolarity syncPolarity)
- static void McBSP_setTxClockPolarity (uint32_t base, const McBSP_TxClockPolarity clockPolarity)
- static void McBSP_setRxClockPolarity (uint32_t base, const McBSP_RxClockPolarity clockPolarity)
- static uint16_t McBSP_read16bitData (uint32_t base)
- static uint32_t McBSP_read32bitData (uint32_t base)
- static void McBSP_write16bitData (uint32_t base, uint16_t data)
- static void McBSP_write32bitData (uint32_t base, uint32_t data)
- static uint16_t McBSP_getLeftJustifyData (uint16_t data, const McBSP_CompandingType compandingType)
- static void McBSP_enableRxInterrupt (uint32_t base)
- static void McBSP_disableRxInterrupt (uint32_t base)
- static void McBSP_enableTxInterrupt (uint32_t base)
- static void McBSP_disableTxInterrupt (uint32_t base)
- void McBSP_transmit16BitDataNonBlocking (uint32_t base, uint16_t data)
- void McBSP_transmit16BitDataBlocking (uint32_t base, uint16_t data)
- void McBSP_transmit32BitDataNonBlocking (uint32_t base, uint32_t data)
- void McBSP_transmit32BitDataBlocking (uint32_t base, uint32_t data)
- void McBSP_receive16BitDataNonBlocking (uint32_t base, uint16_t ∗receiveData)
- void McBSP_receive16BitDataBlocking (uint32_t base, uint16_t ∗receiveData)
- void McBSP_receive32BitDataNonBlocking (uint32_t base, uint32_t ∗receiveData)
- void McBSP_receive32BitDataBlocking (uint32_t base, uint32_t ∗receiveData)

- void McBSP_setRxDataSize (uint32_t base, const McBSP_DataPhaseFrame dataFrame, const McBSP_DataBitsPerWord bitsPerWord, uint16_t wordsPerFrame)
- void McBSP_setTxDataSize (uint32_t base, const McBSP_DataPhaseFrame dataFrame, const McBSP_DataBitsPerWord bitsPerWord, uint16_t wordsPerFrame)
- void McBSP_disableRxChannel (uint32_t base, const McBSP_MultichannelPartition partition, uint16_t channel)
- void McBSP_enableRxChannel (uint32_t base, const McBSP_MultichannelPartition partition, uint16_t channel)
- void McBSP_disableTxChannel (uint32_t base, const McBSP_MultichannelPartition partition, uint16_t channel)
- void McBSP_enableTxChannel (uint32_t base, const McBSP_MultichannelPartition partition, uint16_t channel)
- void McBSP_configureTxClock (uint32_t base, const McBSP_ClockParams ∗ptrClockParams)
- void McBSP_configureRxClock (uint32_t base, const McBSP_ClockParams ∗ptrClockParams)
- void McBSP_configureTxFrameSync (uint32_t base, const McBSP_TxFsyncParams ∗ptrFsyncParams)
- void McBSP_configureRxFrameSync (uint32_t base, const McBSP_RxFsyncParams ∗ptrFsyncParams)
- void McBSP_configureTxDataFormat (uint32_t base, const McBSP_TxDataParams ∗ptrDataParams)
- void McBSP_configureRxDataFormat (uint32_t base, const McBSP_RxDataParams ∗ptrDataParams)
- uint16_t McBSP_configureTxMultichannel (uint32_t base, const McBSP_TxMultichannelParams ∗ptrMchnParams)
- uint16_t McBSP_configureRxMultichannel (uint32_t base, const McBSP_RxMultichannelParams ∗ptrMchnParams)
- void McBSP_configureSPIMasterMode (uint32_t base, const McBSP_SPIMasterModeParams ∗ptrSPIMasterMode)
- void McBSP_configureSPISlaveMode (uint32_t base, const McBSP_SPISlaveModeParams ∗ptrSPISlaveMode)

23.2.1 Detailed Description

Before initializing the McBSP module, the user should first put the module transmitter, receiver, sample rate generator frame sync logic into the reset state.

Next McBSP module should be initialised as per application requirement to set properties like Tx/Rx/sample rate generator/frame sync logic clock source, data delay, tx/rx data format, enable/disable loopback, clock stop mode. McBSP can be configured either in normal McBSP mode or in SPI mode.

After initializing the modules, delay equivalent to 2 SRG cycles must be given before enabling the modules. Nest the sample rate generator must be enabled and after that delay equivalent to 2 CLKG cycles must be given. Next Tx/Rx/frame-sync module must be enabled to complete the configuration.

To transmit data, there are a few options. McBSP_transmit16BitDataNonBlocking, McBSP_transmit32BitDataNonBlocking() will simply write the specified 16/32-bit data to transmit buffer and return. It is left up to the user to check beforehand that the module is ready for a new piece of data to be written to the buffer. The other option is to use one of the two functions McBSP_transmit16BitDataBlocking() McBSP_transmit32BitDataBlocking() that will wait in a while-loop for the module to be ready.

When receiving data, again, there are a few options. McBSP_receive16BitDataNonBlocking() McBSP_receive32BitDataNonBlocking() will immediately return the contents of the receive buffer.The user should check that there is in fact data ready by checking the Rx-ready flag. McBSP_receive16BitDataBlocking() and McBSP_receive32BitDataBlocking(), however, will wait in a while-loop for data to become available.

The code for this module is contained in `driverlib/mcbsp.c`, with `driverlib/mcbsp.h` containing the API declarations for use by applications.

23.2.2 Enumeration Type Documentation

23.2.2.1 enum **McBSP_RxSignExtensionMode**

Values that can be passed to McBSP_setRxSignExtension() as the *mode* parameters.

Enumerator

MCBSP_RIGHT_JUSTIFY_FILL_ZERO Right justify and zero fill MSB.

MCBSP_RIGHT_JUSTIFY_FILL_SIGN Right justified sign extended into MSBs.

MCBSP_LEFT_JUSTIFY_FILL_ZER0 Left justifies LBS filled with zero.

23.2.2.2 enum **McBSP_ClockStopMode**

Values that can be passed to McBSP_setClockStopMode() as the *mode* parameter.

Enumerator

MCBSP_CLOCK_MCBSP_MODE Disables clock stop mode.

MCBSP_CLOCK_SPI_MODE_NO_DELAY Enables clock stop mode.

MCBSP_CLOCK_SPI_MODE_DELAY Enables clock stop mode with half cycle delay.

23.2.2.3 enum **McBSP_RxInterruptSource**

Values that can be passed to McBSP_setRxInterruptSource() as the *interruptSource* parameter.

Enumerator

MCBSP_RX_ISR_SOURCE_SERIAL_WORD Interrupt when Rx is ready.

MCBSP_RX_ISR_SOURCE_END_OF_BLOCK Interrupt at block end.

MCBSP_RX_ISR_SOURCE_FRAME_SYNC Interrupt when frame sync occurs.

MCBSP_RX_ISR_SOURCE_SYNC_ERROR Interrupt on frame sync error.

23.2.2.4 enum **McBSP_EmulationMode**

Values that can be passed to McBSP_setEmulationMode() as the *emulationMode* parameter.

Enumerator

MCBSP_EMULATION_IMMEDIATE_STOP McBSP TX and RX stop when a breakpoint is reached.

MCBSP_EMULATION_SOFT_STOP McBSP TX stops after current word transmitted.
MCBSP_EMULATION_FREE_RUN McBSP TX and RX run ignoring the breakpoint.

23.2.2.5 enum **McBSP_TxInterruptSource**

Values that can be passed to McBSP_setTxInterruptSource() as the *interruptSource* parameter.

Enumerator

MCBSP_TX_ISR_SOURCE_TX_READY Interrupt when Tx Ready.
MCBSP_TX_ISR_SOURCE_END_OF_BLOCK Interrupt at block end.
MCBSP_TX_ISR_SOURCE_FRAME_SYNC Interrupt when frame sync occurs.
MCBSP_TX_ISR_SOURCE_SYNC_ERROR Interrupt on frame sync error.

23.2.2.6 enum **McBSP_DataPhaseFrame**

Values that can be passed to to McBSP_setTxDataSize() and McBSP_setRxDataSize() as the *dataFrame* parameter.

Enumerator

MCBSP_PHASE_ONE_FRAME Single Phase.
MCBSP_PHASE_TWO_FRAME Dual Phase.

23.2.2.7 enum **McBSP_DataBitsPerWord**

Values that can be passed as of McBSP_setTxDataSize() and McBSP_setRxDataSize() as the *bitsPerWord* parameter.

Enumerator

MCBSP_BITS_PER_WORD_8 8 bit word.
MCBSP_BITS_PER_WORD_12 12 bit word.
MCBSP_BITS_PER_WORD_16 16 bit word.
MCBSP_BITS_PER_WORD_20 20 bit word.
MCBSP_BITS_PER_WORD_24 24 bit word.
MCBSP_BITS_PER_WORD_32 32 bit word.

23.2.2.8 enum **McBSP_CompandingMode**

Values that can be passed to McBSP_setTxCompandingMode() and McBSP_setRxCompandingMode() as the *compandingMode* parameter.

Enumerator

MCBSP_COMPANDING_NONE Disables companding.
MCBSP_COMPANDING_NONE_LSB_FIRST Disables companding and Enables 8 bit LSB first data reception.
MCBSP_COMPANDING_U_LAW_SET U-law companding.
MCBSP_COMPANDING_A_LAW_SET A-law companding.

23.2.2.9 enum **McBSP_DataDelayBits**

Values that can be passed to McBSP_setTxDataDelayBits() and McBSP_setRxDataDelayBits() as the *delayBits* parameter.

Enumerator

MCBSP_DATA_DELAY_BIT_0 O bit delay.

MCBSP_DATA_DELAY_BIT_1 1 bit delay.

MCBSP_DATA_DELAY_BIT_2 2 bit delay.

23.2.2.10 enum **McBSP_SRGRxClockSource**

Values that can be passed for SRG for McBSP_setRxSRGClockSource() as the *clockSource* parameter.

Enumerator

MCBSP_SRG_RX_CLOCK_SOURCE_LSPCLK LSPCLK is SRG clock source.

MCBSP_SRG_RX_CLOCK_SOURCE_MCLKX_PIN MCLKx is SRG clock source.

23.2.2.11 enum **McBSP_SRGTxClockSource**

Values that can be passed for SRG to McBSP_setTxSRGClockSource() as the *clockSource* parameter.

Enumerator

MCBSP_SRG_TX_CLOCK_SOURCE_LSPCLK LSPCLK is SRG clock source.

MCBSP_SRG_TX_CLOCK_SOURCE_MCLKR_PIN MCLKris SRG clock source.

23.2.2.12 enum **McBSP_TxInternalFrameSyncSource**

Values that can be passed to McBSP_setTxInternalFrameSyncSource() as the *syncMode* parameter.

Enumerator

MCBSP_TX_INTERNAL_FRAME_SYNC_DATA sync source. Data is frame

MCBSP_TX_INTERNAL_FRAME_SYNC_SRG sync source. SRG is frame

23.2.2.13 enum **McBSP_MultichannelPartition**

Values that can be passed to McBSP_setRxMultichannelPartition() and McBSP_setTxMultichannelPartition() as the *MultichannelPartition* parameter.

Enumerator

MCBSP_MULTICHANNEL_TWO_PARTITION Two partition.

MCBSP_MULTICHANNEL_EIGHT_PARTITION Eight partition.

23.2.2.14 enum **McBSP_PartitionBlock**

Values that can be passed to McBSP_setRxTwoPartitionBlock() and McBSP_setTxTwoPartitionBlock() as the *block* parameter.

Enumerator

MCBSP_PARTITION_BLOCK_0 Partition block 0.
MCBSP_PARTITION_BLOCK_1 Partition block 1.
MCBSP_PARTITION_BLOCK_2 Partition block 2.
MCBSP_PARTITION_BLOCK_3 Partition block 3.
MCBSP_PARTITION_BLOCK_4 Partition block 4.
MCBSP_PARTITION_BLOCK_5 Partition block 5.
MCBSP_PARTITION_BLOCK_6 Partition block 6.
MCBSP_PARTITION_BLOCK_7 Partition block 7.

23.2.2.15 enum **McBSP_RxChannelMode**

Values that can be passed to McBSP_setRxChannelMode() as the *channelMode* parameter.

Enumerator

MCBSP_ALL_RX_CHANNELS_ENABLED All Channels are enabled.
MCBSP_RX_CHANNEL_SELECTION_ENABLED Selected channels enabled.

23.2.2.16 enum **McBSP_TxChannelMode**

Values that can be passed to McBSP_setTxChannelMode() as the *channelMode* parameter.

Enumerator

MCBSP_ALL_TX_CHANNELS_ENABLED All Channels Enabled.
MCBSP_TX_CHANNEL_SELECTION_ENABLED Selection Enabled.
MCBSP_ENABLE_MASKED_TX_CHANNEL_SELECTION Masked Tx Channel.
MCBSP_SYMMERTIC_RX_TX_SELECTION Symmetric Selection.

23.2.2.17 enum **McBSP_TxFrameSyncSource**

Values that can be passed to McBSP_setTxFrameSyncSource() as the *syncSource* parameter.

Enumerator

MCBSP_TX_EXTERNAL_FRAME_SYNC_SOURCE FSR pin supplies frame sync signal.
MCBSP_TX_INTERNAL_FRAME_SYNC_SOURCE SRG supplies frame sync signal.

23.2.2.18 enum **McBSP_RxFrameSyncSource**

Values that can be passed to McBSP_setRxFrameSyncSource() as the *syncSource* parameter.

Enumerator

MCBSP_RX_EXTERNAL_FRAME_SYNC_SOURCE FSR pin supplies frame sync signal.

MCBSP_RX_INTERNAL_FRAME_SYNC_SOURCE SRG supplies frame sync signal.

23.2.2.19 enum **McBSP_TxClockSource**

Values that can be passed to McBSP_setTxClockSource() as the Transmitter *clockSource* parameter.

Enumerator

MCBSP_EXTERNAL_TX_CLOCK_SOURCE Clock source is external.

MCBSP_INTERNAL_TX_CLOCK_SOURCE Clock source is internal.

23.2.2.20 enum **McBSP_RxClockSource**

Values that can be passed toMcBSP_setRxClockSource() as the Receiver *clockSource* parameter.

Enumerator

MCBSP_EXTERNAL_RX_CLOCK_SOURCE Clock source is external.

MCBSP_INTERNAL_RX_CLOCK_SOURCE Clock source is internal.

23.2.2.21 enum **McBSP_TxFrameSyncPolarity**

Values that can be passed to McBSP_setTxFrameSyncPolarity() as the Transmitter *syncPolarity* parameter.

Enumerator

MCBSP_TX_FRAME_SYNC_POLARITY_HIGH Pulse active high.

MCBSP_TX_FRAME_SYNC_POLARITY_LOW Pulse active low.

23.2.2.22 enum **McBSP_RxFrameSyncPolarity**

Values that can be passed to McBSP_setRxFrameSyncPolarity() as the Receiver *syncPolarity* parameter.

Enumerator

MCBSP_RX_FRAME_SYNC_POLARITY_HIGH Pulse active high.

MCBSP_RX_FRAME_SYNC_POLARITY_LOW Pulse active low.

23.2.2.23 enum **McBSP_TxClockPolarity**

Values that can be passed for Transmitter of McBSP_setTxClockPolarity() as the Transmiiter *clockPolarity* parameter.

Enumerator

MCBSP_TX_POLARITY_RISING_EDGE TX data on rising edge.

MCBSP_TX_POLARITY_FALLING_EDGE TX data on falling edge.

23.2.2.24 enum **McBSP_RxClockPolarity**

Values that can be passed for Receiver of McBSP_setRxClockPolarity() as the Receiver *clockPolarity* parameter.

Enumerator

MCBSP_RX_POLARITY_FALLING_EDGE RX data sampled falling edge.

MCBSP_RX_POLARITY_RISING_EDGE RX data sampled rising edge.

23.2.2.25 enum **McBSP_CompandingType**

Values that can be passed to McBSP_getLeftJustifyData() as the *compandingType* parameter.

Enumerator

MCBSP_COMPANDING_U_LAW U-law companding.

MCBSP_COMPANDING_A_LAW A-law companding.

23.2.3 Function Documentation

23.2.3.1 static void McBSP_disableLoopback (uint32_t *base*) [inline], [static]

Disables digital loop back mode.

Parameters

base	is the base address of the McBSP module.

This function disables digital loop back mode.

Returns

None.

Referenced by McBSP_configureRxDataFormat(), McBSP_configureSPIMasterMode(), McBSP_configureSPISlaveMode(), and McBSP_configureTxDataFormat().

23.2.3.2 static void McBSP_enableLoopback (uint32_t *base*) [inline], [static]

Enables digital loop back mode.

Parameters

base	is the base address of the McBSP module.

This function enables digital loop back mode.

Returns

None.

Referenced by McBSP_configureRxDataFormat(), McBSP_configureSPIMasterMode(), McBSP_configureSPISlaveMode(), and McBSP_configureTxDataFormat().

23.2.3.3 static void McBSP_setRxSignExtension (uint32_t *base*, const **McBSP_RxSignExtensionMode** *mode*) [inline], [static]

Configures receiver sign extension mode.

Parameters

base	is the base address of the McBSP module.
mode	is the sign extension mode.

This function sets the sign extension mode. Valid values for mode are:

- **MCBSP_RIGHT_JUSTIFY_FILL_ZERO** - right justified MSB filled with zero.
- **MCBSP_RIGHT_JUSTIFY_FILL_SIGN** - right justified sign extended in MSBs.
- **MCBSP_LEFT_JUSTIFY_FILL_ZER0** - left justifies LBS filled with zero.

Returns

None.

Referenced by McBSP_configureRxDataFormat().

23.2.3.4 static void McBSP_setClockStopMode (uint32_t *base*, const **McBSP_ClockStopMode** *mode*) [inline], [static]

Configures clock stop mode.

Parameters

base	is the base address of the McBSP module.
mode	is the clock stop mode.

This function sets the cock stop mode. Valid values for mode are

- **MCBSP_CLOCK_MCBSP_MODE** disables clock stop mode.
- **MCBSP_CLOCK_SPI_MODE_NO_DELAY** enables clock stop mode
- **MCBSP_CLOCK_SPI_MODE_DELAY** enables clock stop mode with delay.

If an invalid value is provided, the function will exit with out altering the register bits involved.

Returns

None.

Referenced by McBSP_configureRxDataFormat(), McBSP_configureSPIMasterMode(), McBSP_configureSPISlaveMode(), and McBSP_configureTxDataFormat().

23.2.3.5 static void McBSP_disableDxPinDelay (uint32_t *base*) [inline], [static]

Disables delay at DX pin.

Parameters

base	is the base address of the McBSP module.

This function disables delay on pin DX when turning the module on.

Returns

None.

Referenced by McBSP_configureTxDataFormat().

23.2.3.6 static void McBSP_enableDxPinDelay (uint32_t *base*) [inline], [static]

Enables delay at DX pin.

Parameters

base	is the base address of the McBSP module.

This function enables a delay on pin DX when turning the module on. Look at McBSP timing diagrams for details.

Returns

None.

Referenced by McBSP_configureTxDataFormat().

23.2.3.7 static void McBSP_setRxInterruptSource (uint32_t *base*, const **McBSP_RxInterruptSource** *interruptSource*) [inline], [static]

Configures receiver interrupt sources.

Parameters

base	is the base address of the McBSP module.
interruptSource	is the ISR source.

This function sets the receiver interrupt sources. Valid values for interruptSource are:

- **MCBSP_RX_ISR_SOURCE_SERIAL_WORD** - interrupt at each serial word.
- **MCBSP_RX_ISR_SOURCE_END_OF_BLOCK** - interrupt at the end of block.
- **MCBSP_RX_ISR_SOURCE_FRAME_SYNC** - interrupt when frame sync occurs.
- **MCBSP_RX_ISR_SOURCE_SYNC_ERROR** - interrupt on frame sync error.

Returns

None.

Referenced by McBSP_configureRxDataFormat().

23.2.3.8 static void McBSP_clearRxFrameSyncError (uint32_t *base*) [inline], [static]

Clear the receiver frame sync error.

Parameters

base	is the base address of the McBSP module.

This function clears the receive frame sync error.

Returns

None.

23.2.3.9 static uint16_t McBSP_getRxErrorStatus (uint32_t *base*) [inline], [static]

Return receiver error.

Parameters

base	is the base address of the McBSP module.

This function returns McBSP receiver errors.

Returns

Returns the following error codes.

- **MCBSP_RX_NO_ERROR** - if there is no error.
- **MCBSP_RX_BUFFER_ERROR** - if buffergets full.
- **MCBSP_RX_FRAME_SYNC_ERROR** -if unexpected frame sync occurs.
- **MCBSP_RX_BUFFER_FRAME_SYNC_ERROR** - if buffer overrun and frame sync error occurs.

23.2.3.10 static bool McBSP_isRxReady (uint32_t *base*) [inline], [static]

Check if data is received by the receiver.

Parameters

base	is the base address of the McBSP port.

This function returns the status of the receiver buffer , indicating if new data is available.

Returns

true if new data is available or if the current data was never read. **false** if there is no new data in the receive buffer.

Referenced by McBSP_receive16BitDataBlocking(), and McBSP_receive32BitDataBlocking().

23.2.3.11 static void McBSP_resetReceiver (uint32_t *base*) [inline], [static]

Reset McBSP receiver.

Parameters

base	is the base address of the McBSP module.

This function resets McBSP receiver.

Returns

None.

23.2.3.12 static void McBSP_enableReceiver (uint32_t *base*) [inline], [static]

Enable McBSP receiver.

Parameters

base	is the base address of the McBSP module.

This function enables McBSP receiver.

Returns

None.

23.2.3.13 static void McBSP_setEmulationMode (uint32_t *base*, const **McBSP_EmulationMode** *emulationMode*) [inline], [static]

Configures emulation mode.

Parameters

base	is the base address of the McBSP module.
emulationMode	is the McBSP emulation character.

This function sets the McBSP characters when a breakpoint is encountered in emulation mode. Valid values for emulationMode are:

- **MCBSP_EMULATION_IMMEDIATE_STOP** - transmitter and receiver both stop when a breakpoint is reached.
- **MCBSP_EMULATION_SOFT_STOP** - transmitter stops after current word is transmitted. Receiver is not affected.
- **MCBSP_EMULATION_FREE_RUN** - McBSP runs ignoring the breakpoint.

Returns

None.

23.2.3.14 static void McBSP_resetFrameSyncLogic (uint32_t *base*) [inline], [static]

Reset frame sync logic.

Parameters

base	is the base address of the McBSP module.

Resets frame sync logic.

Returns

None.

23.2.3.15 static void McBSP_enableFrameSyncLogic (uint32_t *base*) [inline], [static]

Enable frame sync logic.

Parameters

base	is the base address of the McBSP module.

Enables frame sync logic.

Returns

None.

23.2.3.16 static void McBSP_resetSampleRateGenerator (uint32_t *base*) [inline], [static]

Reset sample rate generator.

Parameters

base	is the base address of the McBSP module.

Resets sample rate generator by clearing GRST bit.

Returns

23.2.3.17 static void McBSP_enableSampleRateGenerator (uint32_t *base*) [inline], [static]

Enable sample rate generator.

Parameters

base	is the base address of the McBSP module.

Enables sample rate generator by setting GRST bit.

Returns

None.

23.2.3.18 static void McBSP_setTxInterruptSource (uint32_t *base,* const **McBSP_TxInterruptSource** *interruptSource*) [inline], [static]

Configures transmitter interrupt sources.

Parameters

base	is the base address of the McBSP module.
interruptSource	is the ISR source.

This function sets the transmitter interrupt sources. Valid values for interruptSource are:

- **MCBSP_TX_ISR_SOURCE_TX_READY** - interrupt when transmitter is ready to accept data.
- **MCBSP_TX_ISR_SOURCE_END_OF_BLOCK** - interrupt at the end of block.
- **MCBSP_TX_ISR_SOURCE_FRAME_SYNC** - interrupt when frame sync occurs.
- **MCBSP_TX_ISR_SOURCE_SYNC_ERROR** - interrupt on frame sync error.

Returns

None.

Referenced by McBSP_configureTxDataFormat().

23.2.3.19 static uint16_t McBSP_getTxErrorStatus (uint32_t *base*) [inline], [static]

Return Transmitter error.

Parameters

base	is the base address of the McBSP module.

This function returns McBSP transmitter errors.

Returns

Returns the following error codes.

- **MCBSP_TX_NO_ERROR** - if buffer overrun occurs.
- **MCBSP_TX_BUFFER_ERROR** -if unexpected frame sync occurs.
- **MCBSP_TX_FRAME_SYNC_ERROR** - if there is no error.
- **MCBSP_TX_BUFFER_FRAME_SYNC_ERROR** - if buffer overrun and frame sync error occurs.

23.2.3.20 static void McBSP_clearTxFrameSyncError (uint32_t *base*) [inline], [static]

Clear the Transmitter frame sync error.

Parameters

base	is the base address of the McBSP module.

This function clears the transmitter frame sync error.

Returns

None.

23.2.3.21 static bool McBSP_isTxReady (uint32_t *base*) [inline], [static]

Check if Transmitter is ready.

Parameters

base	is the base address of the McBSP port.

This function returns the status of the transmitter ready buffer, indicating if data can be written to the transmitter.

Returns

true if transmitter is ready to accept new data. **false** if transmitter is not ready to accept new data.

Referenced by McBSP_transmit16BitDataBlocking(), and McBSP_transmit32BitDataBlocking().

23.2.3.22 static void McBSP_resetTransmitter (uint32_t *base*) [inline], [static]

Reset McBSP transmitter.

Parameters

base	is the base address of the McBSP module.

This functions resets McBSP transmitter.

Returns

None.

23.2.3.23 static void McBSP_enableTransmitter (uint32_t *base*) [inline], [static]

Enable McBSP transmitter.

Parameters

base	is the base address of the McBSP module.

This function enables McBSP transmitter.

Returns

None.

23.2.3.24 static void McBSP_disableTwoPhaseRx (uint32_t *base*) [inline], [static]

Disable 2 Phase operation for data reception.

Parameters

base	is the base address of the McBSP module.

This function disables 2 phase reception.

Returns

None.

Referenced by McBSP_configureRxDataFormat(), and McBSP_configureRxMultichannel().

23.2.3.25 static void McBSP_enableTwoPhaseRx (uint32_t *base*) [inline], [static]

Enable 2 Phase operation for data Reception.

Parameters

base	is the base address of the McBSP module.

This function enables 2 phase reception.

Returns

None.

Referenced by McBSP_configureRxDataFormat().

23.2.3.26 static void McBSP_setRxCompandingMode (uint32_t *base*, const **McBSP_CompandingMode** *compandingMode*) [inline], [static]

Configure receive data companding.

Parameters

base	is the base address of the McBSP module.
companding-Mode	is the companding mode to be used.

This function configures the receive companding logic. The following are valid compandingMode values:

- **MCBSP_COMPANDING_NONE** disables companding.
- **MCBSP_COMPANDING_NONE_LSB_FIRST** disables companding and enables 8 bit LSB first data reception.
- **MCBSP_COMPANDING_U_LAW_SET** enables U-law companding.
- **MCBSP_COMPANDING_A_LAW_SET** enables A-law companding.

Returns

None.

Referenced by McBSP_configureRxDataFormat().

23.2.3.27 static void McBSP_disableRxFrameSyncErrorDetection (uint32_t *base*) [inline], [static]

Disables receiver unexpected frame sync error detection.

Parameters

base	is the base address of the McBSP module.

This function disables unexpected frame sync error detection in the receiver.

Returns

None.

23.2.3.28 static void McBSP_enableRxFrameSyncErrorDetection (uint32_t *base*) [inline], [static]

Enable receiver unexpected frame sync error detection.

Parameters

base	is the base address of the McBSP module.

This function enables unexpected frame sync error detection in the receiver.

Returns

None.

Referenced by McBSP_configureRxFrameSync().

23.2.3.29 static void McBSP_setRxDataDelayBits (uint32_t *base*, const **McBSP_DataDelayBits** *delayBits*) [inline], [static]

Sets the receive bit data delay.

Parameters

base	is the base address of the McBSP module.
delayBits	is the number of bits to delay.

This functions sets the bit delay after the frame sync pulse as specified by delayBits. Valid delay bits are **MCBSP_DATA_DELAY_BIT_0**, **MCBSP_DATA_DELAY_BIT_1** or **MCBSP_DATA_DELAY_BIT_2** corresponding to 0, 1 or 2 bit delay respectively.

Returns

None.

Referenced by McBSP_configureRxDataFormat(), McBSP_configureSPIMasterMode(), and McBSP_configureSPISlaveMode().

23.2.3.30 static void McBSP_disableTwoPhaseTx (uint32_t *base*) [inline], [static]

Disable 2 Phase operation for data Transmission.

Parameters

base	is the base address of the McBSP module.

This function disables 2 phase transmission.

Returns

None.

Referenced by McBSP_configureSPIMasterMode(), McBSP_configureSPISlaveMode(), McBSP_configureTxDataFormat(), and McBSP_configureTxMultichannel().

23.2.3.31 static void McBSP_enableTwoPhaseTx (uint32_t *base*) [inline], [static]

Enable 2 Phase operation for data Transmission.

Parameters

base	is the base address of the McBSP module.

This function enables 2 phase transmission.

Returns
None.

Referenced by McBSP_configureTxDataFormat().

23.2.3.32 static void McBSP_setTxCompandingMode (uint32_t *base*, const **McBSP_CompandingMode** *compandingMode*) [inline], [static]

Configure transmit data companding.

Parameters

base	is the base address of the McBSP module.
companding-Mode	is the companding mode to be used.

This function configures the transmit companding logic. The following are valid compandingMode values:

- **MCBSP_COMPANDING_NONE** disables companding.
- **MCBSP_COMPANDING_NONE_LSB_FIRST** disables companding and enables 8 bit LSB first data reception.
- **MCBSP_COMPANDING_U_LAW_SET** enables U-law companding.
- **MCBSP_COMPANDING_A_LAW_SET** enables A-law companding.

Returns
None.

Referenced by McBSP_configureTxDataFormat().

23.2.3.33 static void McBSP_disableTxFrameSyncErrorDetection (uint32_t *base*) [inline], [static]

Disables transmitter unexpected frame sync error detection.

Parameters

base	is the base address of the McBSP module.

This function disables unexpected frame sync error detection in the transmitter.

Returns
None.

Referenced by McBSP_configureRxFrameSync(), and McBSP_configureTxFrameSync().

23.2.3.34 static void McBSP_enableTxFrameSyncErrorDetection (uint32_t *base*) [inline], [static]

Enable transmitter unexpected frame sync error detection.

Parameters

base	is the base address of the McBSP module.

This function enables unexpected frame sync error detection in the transmitter.

Returns

None.

Referenced by McBSP_configureTxFrameSync().

23.2.3.35 static void McBSP_setTxDataDelayBits (uint32_t *base*, const **McBSP_DataDelayBits** *delayBits*) [inline], [static]

Sets the transmit bit delay.

Parameters

base	is the base address of the McBSP module.
delayBits	is the number of bits to delay.

This function sets the bit delay after the frame sync pulse as specified by delayBits. Valid delay bits are **MCBSP_DATA_DELAY_BIT_0**, **MCBSP_DATA_DELAY_BIT_1** or **MCBSP_DATA_DELAY_BIT_2** corresponding to 0, 1 or 2 bit delay respectively.

Returns

None.

Referenced by McBSP_configureSPIMasterMode(), McBSP_configureSPISlaveMode(), and McBSP_configureTxDataFormat().

23.2.3.36 static void McBSP_setFrameSyncPulsePeriod (uint32_t *base*, uint16_t *frameClockDivider*) [inline], [static]

Sets the period for frame synchronisation pulse.

Parameters

base	is the base address of the McBSP module.
frameClockDivider	is the divider count for the sync clock.

This function sets the sample rate generator clock divider for the McBSP frame sync clock(FSG). FSG = CLKG / (frameClockDivider + 1). frameClockDivider determines the period count.

Returns

None.

Referenced by McBSP_configureRxFrameSync(), and McBSP_configureTxFrameSync().

23.2.3.37 static void McBSP_setFrameSyncPulseWidthDivider (uint32_t *base*, uint16_t *pulseWidthDivider*) [inline], [static]

Sets the frame sync pulse width divider value.

Parameters

base	is the base address of the McBSP module.
pulseWidthDivider	is the divider count for sync clock pulse.

This function sets the pulse width divider bits for the McBSP frame sync clock(FSG). (pulseWidthDivider + 1) is the pulse width in CLKG cycles. pulseWidthDivider determines the pulse width (the on count).

Returns

None.

Referenced by McBSP_configureRxFrameSync(), and McBSP_configureTxFrameSync().

23.2.3.38 static void McBSP_setSRGDataClockDivider (uint32_t *base,* uint16_t *dataClockDivider*) [inline], [static]

Sets the data clock divider values.

Parameters

base	is the base address of the McBSP module.
dataClockDivider	is the divider count for the data rate.

This function sets the sample rate generator clock divider for the McBSP data clock(CLKG). CLKG = CLKSRG / (clockDivider + 1). Valid ranges for clockDivider are 0 to 0xFF.

Returns

None.

Referenced by McBSP_configureRxClock(), McBSP_configureSPIMasterMode(), McBSP_configureSPISlaveMode(), and McBSP_configureTxClock().

23.2.3.39 static void McBSP_disableSRGSyncFSR (uint32_t *base*) [inline], [static]

Disables external clock sync with sample generator.

Parameters

base	is the base address of the McBSP module.

This function disables CLKG and FSG sync with the external pulse on pin FSR.

Returns
None.

Referenced by McBSP_configureTxClock().

23.2.3.40 static void McBSP_enableSRGSyncFSR (uint32_t *base*) [inline], [static]

Enables external clock to synch with sample generator.

Parameters

base	is the base address of the McBSP module.

This function enables CLKG and FSG to sync with the external pulse on pin FSR.

Returns

None.

Referenced by McBSP_configureTxClock().

23.2.3.41 static void McBSP_setRxSRGClockSource (uint32_t *base*, const **McBSP_SRGRxClockSource** *srgClockSource*) [inline], [static]

Configures receiver input clock source for sample generator.

Parameters

base	is the base address of the McBSP module.
srgClockSource	is clock source for the sample generator.

This functions sets the clock source for the sample rate generator. Valid values for *clockSource* are

- **MCBSP_SRG_RX_CLOCK_SOURCE_LSPCLK** for LSPCLK.
- **MCBSP_SRG_RX_CLOCK_SOURCE_MCLKX_PIN** for external clock at MCLKX pin. MCLKR pin will be an output driven by sample rate generator.

Returns

None.

Referenced by McBSP_configureRxClock(), and McBSP_configureSPISlaveMode().

23.2.3.42 static void McBSP_setTxSRGClockSource (uint32_t *base*, const **McBSP_SRGTxClockSource** *srgClockSource*) [inline], [static]

Configures transmitter input clock source for sample generator.

Parameters

base	is the base address of the McBSP module.
srgClockSource	is clock source for the sample generator.

This functions sets the clock source for the sample rate generator. Valid values for *clockSource* are

- **MCBSP_SRG_TX_CLOCK_SOURCE_LSPCLK** for LSPCLK.
- **MCBSP_SRG_TX_CLOCK_SOURCE_MCLKR_PIN** for external clock at MCLKR pin. MCLKX pin will be an output driven by sample rate generator.

Returns

None.

Referenced by McBSP_configureSPIMasterMode(), and McBSP_configureTxClock().

23.2.3.43 static void McBSP_setTxInternalFrameSyncSource (uint32_t *base,* const **McBSP_TxInternalFrameSyncSource** *syncMode*) [inline], [static]

Sets the mode for transmitter internal frame sync signal.

Parameters

base	is the base address of the McBSP module.
syncMode	is the frame sync mode.

This function sets the frame sync signal generation mode. The signal can be generated based on clock divider as set in McBSP_setFrameSyncPulsePeriod() function or when data is transferred from DXR registers to XSR registers. Valid input for syncMode are:

- **MCBSP_TX_INTERNAL_FRAME_SYNC_DATA** - frame sync signal is generated when data is transferred from DXR registers to XSR registers.
- **MCBSP_TX_INTERNAL_FRAME_SYNC_SRG** - frame sync signal is generated based on the clock counter value as defined in McBSP_setFrameSyncPulsePeriod() function.

Returns

None.

Referenced by McBSP_configureSPIMasterMode(), and McBSP_configureTxFrameSync().

23.2.3.44 static void McBSP_setRxMultichannelPartition (uint32_t *base,* const **McBSP_MultichannelPartition** *partition*) [inline], [static]

Set Multichannel receiver partitions.

Parameters

base	is the base address of the McBSP module.
partition	is the number of partitions.

This function sets the partitions for Multichannel receiver. Valid values for partition are **MCBSP_MULTICHANNEL_TWO_PARTITION** or **MCBSP_MULTICHANNEL_EIGHT_PARTITION** for 2 and 8 partitions respectively.

Returns

None.

Referenced by McBSP_configureRxMultichannel().

23.2.3.45 static void McBSP_setRxTwoPartitionBlock (uint32_t *base,* const **McBSP_PartitionBlock** *block*) [inline], [static]

Sets block to receiver in two partition configuration.

Parameters

base	is the base address of the McBSP module.
block	is the block to assign to the partition.

This function assigns the block the user provides to the appropriate receiver partition. If user sets the value of block to 0, 2, 4 or 6 the API will assign the blocks to partition A. If values 1, 3, 5, or 7 are set to block, then the API assigns the block to partition B.

Note
This function should be used with the two partition configuration only and not with eight partition configuration.

Returns
None.

Referenced by McBSP_configureRxMultichannel().

23.2.3.46 static uint16_t McBSP_getRxActiveBlock (uint32_t *base*) [inline], [static]

Returns the current active receiver block number.

Parameters

base	is the base address of the McBSP module.

This function returns the current active receiver block involved in McBSP reception.

Returns
Active block in McBSP reception. Returned values range from 0 to 7 representing the respective active block number .

23.2.3.47 static void McBSP_setRxChannelMode (uint32_t *base*, const **McBSP_RxChannelMode** *channelMode*) [inline], [static]

Configure channel selection mode for receiver.

Parameters

base	is the base address of the McBSP module.
channelMode	is the channel selection mode.

This function configures the channel selection mode. The following are valid values for channelMode:

- **MCBSP_ALL_RX_CHANNELS_ENABLED** - enables all channels.
- **MCBSP_RX_CHANNEL_SELECTION_ENABLED** - lets the user enable desired channels by using McBSP_enableRxChannel().

Returns
None.

Referenced by McBSP_configureRxMultichannel().

23.2.3.48 static void McBSP_setTxMultichannelPartition (uint32_t *base*, const **McBSP_MultichannelPartition** *partition*) [inline], [static]

Set Multichannel transmitter partitions.

Parameters

base	is the base address of the McBSP module.
partition	is the number of partitions.

This function sets the partitions for Multichannel transmitter. Valid values for partition are **MCBSP_MULTICHANNEL_TWO_PARTITION** or **MCBSP_MULTICHANNEL_EIGHT_PARTITION** for 2 and 8 partitions respectively.

Returns

None.

Referenced by McBSP_configureTxMultichannel().

23.2.3.49 static void McBSP_setTxTwoPartitionBlock (uint32_t *base*, const **McBSP_PartitionBlock** *block*) [inline], [static]

Sets block to transmitter in two partition configuration.

Parameters

base	is the base address of the McBSP module.
block	is the block to assign to the partition.

This function assigns the block the user provides to the appropriate transmitter partition. If user sets the value of block to 0, 2, 4 or 6 the API will assign the blocks to partition A. If values 1, 3, 5, or 7 are set to block, then the API assigns the block to partition B.

Note

This function should be used with the two partition configuration only and not with eight partition configuration.

Returns

None.

Referenced by McBSP_configureTxMultichannel().

23.2.3.50 static uint16_t McBSP_getTxActiveBlock (uint32_t *base*) [inline], [static]

Returns the current active transmitter block number.

Parameters

base	is the base address of the McBSP module.

This function returns the current active transmitter block involved in McBSP transmission.

Returns

Active block in McBSP transmission. Returned values range from 0 to 7 representing the respective active block number.

23.2.3.51 static void McBSP_setTxChannelMode (uint32_t *base*, const **McBSP_TxChannelMode** *channelMode*) [inline], [static]

Configure channel selection mode for transmitter.

Parameters

base	is the base address of the McBSP module.
channelMode	is the channel selection mode.

This function configures the channel selection mode. The following are valid values for channelMode:

- **MCBSP_ALL_TX_CHANNELS_ENABLED** - enables and unmasks all channels
- **MCBSP_TX_CHANNEL_SELECTION_ENABLED** - lets the user enable and unmask desired channels by using McBSP_enableTxChannel()
- **MCBSP_ENABLE_MASKED_TX_CHANNEL_SELECTION** - All channels enables but until enabled by McBSP_enableTxChannel()
- **MCBSP_SYMMERTIC_RX_TX_SELECTION** - Symmetric transmission and reception.

Returns

None.

Referenced by McBSP_configureTxMultichannel().

23.2.3.52 static void McBSP_setTxFrameSyncSource (uint32_t *base*, const **McBSP_TxFrameSyncSource** *syncSource*) [inline], [static]

Select the transmitter frame sync signal source.

Parameters

base	is the base address of the McBSP module.
syncSource	is the transmitter frame sync source.

This function sets external or internal sync signal source based on the syncSource selection. Valid input for syncSource are:

- **MCBSP_TX_EXTERNAL_FRAME_SYNC_SOURCE** - frame sync signal is supplied externally by pin FSX.
- **MCBSP_TX_INTERNAL_FRAME_SYNC_SOURCE** - frame sync signal is supplied internally.

Returns

None.

Referenced by McBSP_configureSPIMasterMode(), McBSP_configureSPISlaveMode(), and McBSP_configureTxFrameSync().

23.2.3.53 static void McBSP_setRxFrameSyncSource (uint32_t *base*, const **McBSP_RxFrameSyncSource** *syncSource*) [inline], [static]

Select receiver frame sync signal source.

Parameters

base	is the base address of the McBSP module.
syncSource	is the receiver frame sync source.

This function sets external or internal sync signal source based on the syncSource selection. Valid input for syncSource are:

- **MCBSP_RX_EXTERNAL_FRAME_SYNC_SOURCE** - frame sync signal is supplied externally by pin FSR.
- **MCBSP_RX_INTERNAL_FRAME_SYNC_SOURCE** - frame sync signal is supplied by SRG.

Returns
None.

Referenced by McBSP_configureRxFrameSync().

23.2.3.54 static void McBSP_setTxClockSource (uint32_t *base*, const **McBSP_TxClockSource** *clockSource*) [inline], [static]

Configures the Transmit clock source.

Parameters

base	is the base address of the McBSP module.
clockSource	is clock source for the transmission pin.

This function configures the clock source for the transmitter. Valid input for rxClockSource are:

- **MCBSP_INTERNAL_TX_CLOCK_SOURCE** - internal clock source. SRG is the source.
- **MCBSP_EXTERNAL_TX_CLOCK_SOURCE** - external clock source.

Returns
None.

Referenced by McBSP_configureSPIMasterMode(), McBSP_configureSPISlaveMode(), and McBSP_configureTxClock().

23.2.3.55 static void McBSP_setRxClockSource (uint32_t *base*, const **McBSP_RxClockSource** *clockSource*) [inline], [static]

Configures the Receive clock source.

Parameters

base	is the base address of the McBSP module.
clockSource	is clock source for the reception pin.

This function configures the clock source for the receiver. Valid input for base are:

- **MCBSP_INTERNAL_RX_CLOCK_SOURCE** - internal clock source. Sample Rate Generator will be used.
- **MCBSP_EXTERNAL_RX_CLOCK_SOURCE** - external clock will drive the data.

Returns
None.

Referenced by McBSP_configureRxClock().

23.2.3.56 static void McBSP_setTxFrameSyncPolarity (uint32_t *base*, const **McBSP_TxFrameSyncPolarity** *syncPolarity*) [inline], [static]

Sets transmitter frame sync polarity.

Parameters

base	is the base address of the McBSP module.
syncPolarity	is the polarity of frame sync pulse.

This function sets the polarity (rising or falling edge)of the frame sync on FSX pin. Use **MCBSP_TX_FRAME_SYNC_POLARITY_LOW** for active low frame sync pulse and **MCBSP_TX_FRAME_SYNC_POLARITY_HIGH** for active high sync pulse.

Returns
None.

Referenced by McBSP_configureSPIMasterMode(), McBSP_configureSPISlaveMode(), and McBSP_configureTxFrameSync().

23.2.3.57 static void McBSP_setRxFrameSyncPolarity (uint32_t *base*, const **McBSP_RxFrameSyncPolarity** *syncPolarity*) [inline], [static]

Sets receiver frame sync polarity.

Parameters

base	is the base address of the McBSP module.
syncPolarity	is the polarity of frame sync pulse.

This function sets the polarity (rising or falling edge)of the frame sync on FSR pin. Use **MCBSP_RX_FRAME_SYNC_POLARITY_LOW** for active low frame sync pulse and **MCBSP_RX_FRAME_SYNC_POLARITY_HIGH** for active high sync pulse.

Returns
None.

Referenced by McBSP_configureRxFrameSync().

23.2.3.58 static void McBSP_setTxClockPolarity (uint32_t *base*, const **McBSP_TxClockPolarity** *clockPolarity*) [inline], [static]

Sets transmitter clock polarity when using external clock source.

Parameters

base	is the base address of the McBSP module.
clockPolarity	is the polarity of external clock.

This function sets the polarity (rising or falling edge) of the transmitter clock on MCLKX pin. Valid values for clockPolarity are:

- **MCBSP_TX_POLARITY_RISING_EDGE** for rising edge.
- **MCBSP_TX_POLARITY_FALLING_EDGE** for falling edge.

Returns

None.

Referenced by McBSP_configureRxClock(), McBSP_configureSPIMasterMode(), McBSP_configureSPISlaveMode(), and McBSP_configureTxClock().

23.2.3.59 static void McBSP_setRxClockPolarity (uint32_t *base*, const **McBSP_RxClockPolarity** *clockPolarity*) [inline], [static]

Sets receiver clock polarity when using external clock source.

Parameters

base	is the base address of the McBSP module.
clockPolarity	is the polarity of external clock.

This function sets the polarity (rising or falling edge) of the receiver clock on MCLKR pin. If external clock is used, the polarity will affect CLKG signal. Valid values for clockPolarity are:

- **MCBSP_RX_POLARITY_RISING_EDGE** for rising edge.
- **MCBSP_RX_POLARITY_FALLING_EDGE** for falling edge.

Returns

None.

Referenced by McBSP_configureRxClock(), and McBSP_configureTxClock().

23.2.3.60 static uint16_t McBSP_read16bitData (uint32_t *base*) [inline], [static]

Read 8, 12 or 16 bit data word from McBSP data receive registers.

Parameters

base	is the base address of the McBSP port.

This function returns the data value in data receive register.

Returns

received data.

Referenced by McBSP_receive16BitDataBlocking(), and McBSP_receive16BitDataNonBlocking().

23.2.3.61 static uint32_t McBSP_read32bitData (uint32_t *base*) [inline], [static]

Read 20, 24 or 32 bit data word from McBSP data receive registers.

Parameters

base	is the base address of the McBSP port.

This function returns the data values in data receive registers.

Returns

received data.

Referenced by McBSP_receive32BitDataBlocking(), and McBSP_receive32BitDataNonBlocking().

23.2.3.62 static void McBSP_write16bitData (uint32_t *base,* uint16_t *data*) [inline], [static]

Write 8, 12 or 16 bit data word to McBSP data transmit registers.

Parameters

base	is the base address of the McBSP port.
data	is the data to be written.

This function writes 8, 12 or 16 bit data to data transmit register.

Returns

None.

Referenced by McBSP_transmit16BitDataBlocking(), and McBSP_transmit16BitDataNonBlocking().

23.2.3.63 static void McBSP_write32bitData (uint32_t *base,* uint32_t *data*) [inline], [static]

Write 20, 24 or 32 bit data word to McBSP data transmit registers.

Parameters

base	is the base address of the McBSP port.
data	is the data to be written.

This function writes 20, 24 or 32 bit data to data transmit registers.

Returns

None.

Referenced by McBSP_transmit32BitDataBlocking(), and McBSP_transmit32BitDataNonBlocking().

23.2.3.64 static uint16_t McBSP_getLeftJustifyData (uint16_t *data,* const **McBSP_CompandingType** *compandingType*) [inline], [static]

Return left justified for data for U Law or A Law companding.

Parameters

data	is the 14 bit word.
companding-Type	specifies the type comapnding desired.

This functions returns U law or A law adjusted word.

Returns
U law or A law left justified word.

23.2.3.65 static void McBSP_enableRxInterrupt (uint32_t *base*) [inline], [static]

Enable Recieve Interrupt.

Parameters

base	is the base address of the McBSP module.

This function enables Recieve Interrupt on RRDY.

Returns
None.

23.2.3.66 static void McBSP_disableRxInterrupt (uint32_t *base*) [inline], [static]

Disable Recieve Interrupt.

Parameters

base	is the base address of the McBSP module.

This function disables Recieve Interrupt on RRDY.

Returns
None.

23.2.3.67 static void McBSP_enableTxInterrupt (uint32_t *base*) [inline], [static]

Enable Transmit Interrupt.

Parameters

base	is the base address of the McBSP module.

This function enables Transmit Interrupt on XRDY.

Returns
None.

23.2.3.68 static void McBSP_disableTxInterrupt (uint32_t *base*) [inline], [static]

Disable Transmit Interrupt.

Parameters

base	is the base address of the McBSP module.

This function disables Transmit Interrupt on XRDY.

Returns

None.

23.2.3.69 void McBSP_transmit16BitDataNonBlocking (uint32_t *base,* uint16_t *data*)

Write 8, 12 or 16 bit data word to McBSP data transmit registers

Parameters

base	is the base address of the McBSP port.
data	is the data to be written.

This function sends 16 bit or less data to the transmitter buffer.

Returns

None.
None.

References McBSP_write16bitData().

23.2.3.70 void McBSP_transmit16BitDataBlocking (uint32_t *base,* uint16_t *data*)

Write 8, 12 or 16 bit data word to McBSP data transmit registers

Parameters

base	is the base address of the McBSP port.
data	is the data to be written.

This function sends 16 bit or less data to the transmitter buffer. If transmit buffer is not ready the function will wait until transmit buffer is empty. If the transmitter buffer is empty the data will be written to the data registers.

Returns

None.

References McBSP_isTxReady(), and McBSP_write16bitData().

23.2.3.71 void McBSP_transmit32BitDataNonBlocking (uint32_t *base,* uint32_t *data*)

Write 20 , 24 or 32 bit data word to McBSP data transmit registers

Parameters

base	is the base address of the McBSP port.
data	is the data to be written.

This function sends 20 , 24 or 32 bit data to the transmitter buffer. If the transmitter buffer is empty the data will be written to the data registers.

Returns
None.

References McBSP_write32bitData().

23.2.3.72 void McBSP_transmit32BitDataBlocking (uint32_t *base,* uint32_t *data*)

Write 20 , 24 or 32 bit data word to McBSP data transmit registers

Parameters

base	is the base address of the McBSP port.
data	is the data to be written.

This function sends 20 , 24 or 32 bit data to the transmitter buffer. If transmit buffer is not ready the function will wait until transmit buffer is empty. If the transmitter buffer is empty the data will be written to the data registers.

Returns
None.

References McBSP_isTxReady(), and McBSP_write32bitData().

23.2.3.73 void McBSP_receive16BitDataNonBlocking (uint32_t *base,* uint16_t ∗ *receiveData*)

Read 8, 12 or 16 bit data word from McBSP data receive registers

Parameters

base	is the base address of the McBSP port.
receiveData	is the pointer to the receive data.

This function reads 8, 12 or 16 bit data from the receiver buffer. If the receiver buffer has new data, the data will be read.

Returns
None.

References McBSP_read16bitData().

23.2.3.74 void McBSP_receive16BitDataBlocking (uint32_t *base,* uint16_t ∗ *receiveData*)

Read 8, 12 or 16 bit data word from McBSP data receive registers

Parameters

base	is the base address of the McBSP port.
receiveData	is the pointer to the receive data.

This function reads 8, 12 or 16 bit data from the receiver buffer. If receiver buffer is not ready the function will wait until receiver buffer has new data. If the receiver buffer has new data, the data will be read.

Returns

None.

References McBSP_isRxReady(), and McBSP_read16bitData().

23.2.3.75 void McBSP_receive32BitDataNonBlocking (uint32_t *base,* uint32_t ∗ *receiveData*)

Read 20, 24 or 32 bit data word from McBSP data receive registers

Parameters

base	is the base address of the McBSP port.
receiveData	is the pointer to the receive data.

This function reads 20, 24 or 32 bit data from the receiver buffer. If the receiver buffer has new data, the data will be read.

Returns

None.

References McBSP_read32bitData().

23.2.3.76 void McBSP_receive32BitDataBlocking (uint32_t *base,* uint32_t ∗ *receiveData*)

Read 20, 24 or 32 bit data word from McBSP data receive registers

Parameters

base	is the base address of the McBSP port.
receiveData	is the pointer to the receive data.

This function reads 20, 24 or 32 bit data from the receiver buffer. If receiver buffer is not ready the function will wait until receiver buffer has new data. If the receiver buffer has new data, the data will be read.

Returns
None.

References McBSP_isRxReady(), and McBSP_read32bitData().

23.2.3.77 void McBSP_setRxDataSize (uint32_t *base*, const **McBSP_DataPhaseFrame** *dataFrame*, const **McBSP_DataBitsPerWord** *bitsPerWord*, uint16_t *wordsPerFrame*)

Sets number of words per frame and bits per word for data Reception.

Parameters

base	is the base address of the McBSP module.
dataFrame	is the data frame phase.
bitsPerWord	is the number of bits per word.
wordsPerFrame	is the number of words per frame per phase.

This function sets the number of bits per word and the number of words per frame for the given phase. Valid inputs for phase are **MCBSP_PHASE_ONE_FRAME** or **MCBSP_PHASE_TWO_FRAME** representing the first or second frame phase respectively. Valid value for bitsPerWord are:

- **MCBSP_BITS_PER_WORD_8** 8 bit word.
- **MCBSP_BITS_PER_WORD_12** 12 bit word.
- **MCBSP_BITS_PER_WORD_16** 16 bit word.
- **MCBSP_BITS_PER_WORD_20** 20 bit word.
- **MCBSP_BITS_PER_WORD_24** 24 bit word.
- **MCBSP_BITS_PER_WORD_32** 32 bit word. The maximum value for wordsPerFrame is 127 (128 - 1)representing 128 words.

Returns

None.

References MCBSP_PHASE_ONE_FRAME.

Referenced by McBSP_configureRxDataFormat(), McBSP_configureSPIMasterMode(), and McBSP_configureSPISlaveMode().

23.2.3.78 void McBSP_setTxDataSize (uint32_t *base,* const **McBSP_DataPhaseFrame** *dataFrame,* const **McBSP_DataBitsPerWord** *bitsPerWord,* uint16_t *wordsPerFrame*)

Sets number of words per frame and bits per word for data Transmission.

Parameters

base	is the base address of the McBSP module.
dataFrame	is the data frame phase.
bitsPerWord	is the number of bits per word.
wordsPerFrame	is the number of words per frame per phase.

This function sets the number of bits per word and the number of words per frame for the given phase. Valid inputs for phase are **MCBSP_PHASE_ONE_FRAME** or **MCBSP_PHASE_TWO_FRAME** representing single or dual phase respectively. Valid values for bitsPerWord are:

- **MCBSP_BITS_PER_WORD_8** 8 bit word.
- **MCBSP_BITS_PER_WORD_12** 12 bit word.
- **MCBSP_BITS_PER_WORD_16** 16 bit word.
- **MCBSP_BITS_PER_WORD_20** 20 bit word.
- **MCBSP_BITS_PER_WORD_24** 24 bit word.

- **MCBSP_BITS_PER_WORD_32** 32 bit word. The maximum value for wordsPerFrame is 127 (128 - 1)representing 128 words.

Returns

None.

References MCBSP_PHASE_ONE_FRAME.

Referenced by McBSP_configureSPIMasterMode(), McBSP_configureSPISlaveMode(), and McBSP_configureTxDataFormat().

23.2.3.79 void McBSP_disableRxChannel (uint32_t *base*, const **McBSP_MultichannelPartition** *partition*, uint16_t *channel*)

Disables a channel in an eight partition receiver

Parameters

base	is the base address of the McBSP module.
partition	is the partition of the channel.
channel	is the receiver channel number to be enabled.

This function disables the given receiver channel number for the partition provided. Valid values for partition are **MCBSP_MULTICHANNEL_TWO_PARTITION** or **MCBSP_MULTICHANNEL_EIGHT_PARTITION** for 2 or 8 partitions respectively. Valid values for channel range from 0 to 127.

Returns

None.

References MCBSP_MULTICHANNEL_EIGHT_PARTITION.

23.2.3.80 void McBSP_enableRxChannel (uint32_t *base*, const **McBSP_MultichannelPartition** *partition*, uint16_t *channel*)

Enables a channel for eight partition receiver

Parameters

base	is the base address of the McBSP module.
partition	is the partition of the channel.
channel	is the receiver channel number to be enabled.

This function enables the given receiver channel number for the partition provided. Valid values for partition are **MCBSP_MULTICHANNEL_TWO_PARTITION** or **MCBSP_MULTICHANNEL_EIGHT_PARTITION** for 2 or 8 partitions respectively. Valid values for channel range from 0 to 127.

Returns

None.

References MCBSP_MULTICHANNEL_EIGHT_PARTITION.

Referenced by McBSP_configureRxMultichannel().

23.2.3.81 void McBSP_disableTxChannel (uint32_t *base*, const **McBSP_MultichannelPartition** *partition*, uint16_t *channel*)

Disables a channel in an eight partition transmitter

Parameters

base	is the base address of the McBSP module.
partition	is the partition of the channel.
channel	is the transmitter channel number to be enabled.

This function disables the given transmitter channel number for the partition provided. Valid values for partition are **MCBSP_MULTICHANNEL_TWO_PARTITION** or **MCBSP_MULTICHANNEL_EIGHT_PARTITION** for 2 or 8 partitions respectively. Valid values for channel range from 0 to 127.

Returns
None.

References MCBSP_MULTICHANNEL_EIGHT_PARTITION.

23.2.3.82 void McBSP_enableTxChannel (uint32_t *base,* const **McBSP_MultichannelPartition** *partition,* uint16_t *channel*)

Enables a channel for eight partition transmitter

Parameters

base	is the base address of the McBSP module.
partition	is the partition of the channel.
channel	is the transmitter channel number to be enabled.

This function enables the given transmitter channel number for the partition provided. Valid values for partition are **MCBSP_MULTICHANNEL_TWO_PARTITION** or **MCBSP_MULTICHANNEL_EIGHT_PARTITION** for 2 or 8 partitions respectively. Valid values for channel range from 0 to 127.

Returns
None.

References MCBSP_MULTICHANNEL_EIGHT_PARTITION.

Referenced by McBSP_configureTxMultichannel().

23.2.3.83 void McBSP_configureTxClock (uint32_t *base,* const **McBSP_ClockParams** ∗ *ptrClockParams*)

Configures transmitter clock

Parameters

base	is the base address of the McBSP module.
ptrClockParams	is a pointer to a structure containing *clock* parameters McBSP_ClockParams. This function sets up the transmitter clock. The following are valid values and ranges for the parameters of the McBSP_TxFsyncParams. ■ **clockSRGSyncFSR** - true to sync with signal on FSR pin, false to ignore signal on FSR pin. the pulse on FSR pin. ■ **clockSRGDivider** - Maximum valid value is 255. ■ **clockSource** - MCBSP_EXTERNAL_TX_CLOCK_SOURCE or MCBSP_INTERNAL_TX_CLOCK_SOURCE ■ **clockTxSRGSource** - MCBSP_SRG_TX_CLOCK_SOURCE_LSPCLK or MCBSP_SRG_TX_CLOCK_SOURCE_MCLKR_PIN ■ **clockMCLKXPolarity** - Output polarity on MCLKX pin. • MCBSP_TX_POLARITY_RISING_EDGE • MCBSP_TX_POLARITY_FALLING_EDGE ■ **clockMCLKRPolarity** - Input polarity on MCLKR pin (if SRG is sourced from MCLKR pin). • MCBSP_RX_POLARITY_FALLING_EDGE • MCBSP_RX_POLARITY_RISING_EDGE

Note

Make sure the clock divider is such that, the McBSP clock is not running faster than 1/2 the speed of the source clock.

Returns

None.

References McBSP_ClockParams::clockMCLKRPolarity, McBSP_ClockParams::clockMCLKXPolarity, McBSP_ClockParams::clockSourceTx, McBSP_ClockParams::clockSRGDivider, McBSP_ClockParams::clockSRGSyncFlag, McBSP_ClockParams::clockTxSRGSource, McBSP_disableSRGSyncFSR(), McBSP_enableSRGSyncFSR(), MCBSP_INTERNAL_TX_CLOCK_SOURCE, McBSP_setRxClockPolarity(), McBSP_setSRGDataClockDivider(), McBSP_setTxClockPolarity(), McBSP_setTxClockSource(), McBSP_setTxSRGClockSource(), and MCBSP_SRG_TX_CLOCK_SOURCE_MCLKR_PIN.

23.2.3.84 void McBSP_configureRxClock (uint32_t *base*, const **McBSP_ClockParams** ∗ *ptrClockParams*)

Configures receiver clock

Parameters

base	is the base address of the McBSP module.
ptrClockParams	is a pointer to a structure containing *clock* parameters McBSP_ClockParams. This function sets up the receiver clock. The following are valid values and ranges for the parameters of the McBSP_TxFsyncParams. ■ **clockSRGSyncFlag** - true to sync with signal on FSR pin, false to ignore the pulse on FSR pin. ■ **clockSRGDivider** - Maximum valid value is 255. ■ **clockSource** - MCBSP_EXTERNAL_RX_CLOCK_SOURCE or MCBSP_INTERNAL_RX_CLOCK_SOURCE ■ **clockRxSRGSource** - MCBSP_SRG_RX_CLOCK_SOURCE_LSPCLK or MCBSP_SRG_RX_CLOCK_SOURCE_MCLKX_PIN ■ **clockMCLKRPolarity-** output polarity on MCLKR pin. • MCBSP_RX_POLARITY_FALLING_EDGE or • MCBSP_RX_POLARITY_RISING_EDGE ■ **clockMCLKXPolarity-** Input polarity on MCLKX pin (if SRG is sourced from MCLKX pin). • MCBSP_TX_POLARITY_RISING_EDGE or • MCBSP_TX_POLARITY_FALLING_EDGE

Note

Make sure the clock divider is such that, the McBSP clock is not running faster than 1/2 the speed of the source clock.

Returns

None.

References McBSP_ClockParams::clockMCLKRPolarity, McBSP_ClockParams::clockMCLKXPolarity, McBSP_ClockParams::clockRxSRGSource, McBSP_ClockParams::clockSourceRx, McBSP_ClockParams::clockSRGDivider, MCBSP_INTERNAL_RX_CLOCK_SOURCE, McBSP_setRxClockPolarity(), McBSP_setRxClockSource(), McBSP_setRxSRGClockSource(), McBSP_setSRGDataClockDivider(), McBSP_setTxClockPolarity(), and MCBSP_SRG_RX_CLOCK_SOURCE_MCLKX_PIN.

23.2.3.85 void McBSP_configureTxFrameSync (uint32_t *base,* const **McBSP_TxFsyncParams** ∗ *ptrFsyncParams*)

Configures transmitter frame sync.

Parameters

base	is the base address of the McBSP module.
ptrFsyncParams	is a pointer to a structure containing *frame* sync parameters McBSPTxFsyncParams. This function sets up the transmitter frame sync. The following are valid values and ranges for the parameters of the McBSPTxFsyncParams. ■ **syncSRGSyncFSRFlag** - true to sync with signal on FSR pin, false to ignore the pulse on FSR pin.This value has to be similar to the value of McBSP_ClockParams.clockSRGSyncFlag. ■ **syncErrorDetect** - true to enable frame sync error detect. false to disable. ■ **syncClockDivider** - Maximum valid value is 4095. ■ **syncPulseDivider** - Maximum valid value is 255. ■ **syncSourceTx** - MCBSP_TX_INTERNAL_FRAME_SYNC_SOURCE or MCBSP_TX_EXTERNAL_FRAME_SYNC_SOURCE ■ **syncIntSource** - MCBSP_TX_INTERNAL_FRAME_SYNC_DATA or MCBSP_TX_INTERNAL_FRAME_SYNC_SRG ■ **syncFSXPolarity** - MCBSP_TX_FRAME_SYNC_POLARITY_LOW or MCBSP_TX_FRAME_SYNC_POLARITY_HIGH.

Returns

None.

References McBSP_disableTxFrameSyncErrorDetection(), McBSP_enableTxFrameSyncErrorDetection(), McBSP_setFrameSyncPulsePeriod(), McBSP_setFrameSyncPulseWidthDivider(), McBSP_setTxFrameSyncPolarity(), McBSP_setTxFrameSyncSource(), McBSP_setTxInternalFrameSyncSource(), MCBSP_TX_INTERNAL_FRAME_SYNC_SOURCE, MCBSP_TX_INTERNAL_FRAME_SYNC_SRG, McBSP_TxFsyncParams::syncClockDivider, McBSP_TxFsyncParams::syncErrorDetect, McBSP_TxFsyncParams::syncFSXPolarity, McBSP_TxFsyncParams::syncIntSource, McBSP_TxFsyncParams::syncPulseDivider, McBSP_TxFsyncParams::syncSourceTx, and McBSP_TxFsyncParams::syncSRGSyncFSRFlag.

23.2.3.86 void McBSP_configureRxFrameSync (uint32_t *base,* const **McBSP_RxFsyncParams** ∗ *ptrFsyncParams*)

Configures receiver frame sync.

Parameters

base	is the base address of the McBSP module.
ptrFsyncParams	is a pointer to a structure containing *frame* sync parameters McBSP_RxFsyncParams. This function sets up the receiver frame sync. The following are valid values and ranges for the parameters of the McBSPTxFsyncParams. ■ **syncSRGSyncFSRFlag** - true to sync with signal on FSR pin, false to ignore the pulse on FSR pin. This value has to be similar to the value of McBSP_ClockParams.clockSRGSyncFlag. ■ **syncErrorDetect** - true to enable frame sync error detect. false to disable. ■ **syncClockDivider** - Maximum valid value is 4095. ■ **syncPulseDivider** - Maximum valid value is 255. ■ **syncSourceRx** - MCBSP_RX_INTERNAL_FRAME_SYNC_SOURCE or MCBSP_RX_EXTERNAL_FRAME_SYNC_SOURCE ■ **syncFSRPolarity** - MCBSP_RX_FRAME_SYNC_POLARITY_LOW or MCBSP_RX_FRAME_SYNC_POLARITY_HIGH

Returns

None.

References McBSP_disableTxFrameSyncErrorDetection(), McBSP_enableRxFrameSyncErrorDetection(), MCBSP_RX_INTERNAL_FRAME_SYNC_SOURCE, McBSP_setFrameSyncPulsePeriod(), McBSP_setFrameSyncPulseWidthDivider(), McBSP_setRxFrameSyncPolarity(), McBSP_setRxFrameSyncSource(), McBSP_RxFsyncParams::syncClockDivider, McBSP_RxFsyncParams::syncErrorDetect, McBSP_RxFsyncParams::syncFSRPolarity, McBSP_RxFsyncParams::syncPulseDivider, McBSP_RxFsyncParams::syncSourceRx, and McBSP_RxFsyncParams::syncSRGSyncFSRFlag.

23.2.3.87 void McBSP_configureTxDataFormat (uint32_t *base*, const **McBSP_TxDataParams** ∗ *ptrDataParams*)

Configures transmitter data format.

Parameters

base	is the base address of the McBSP module.
ptrDataParams	is a pointer to a structure containing *data* format parameters McBSPTxDataParams. This function sets up the transmitter data format and properties. The following are valid values and ranges for the parameters of the McBSPTxDataParams. ■ **loopbackModeFlag** - true for digital loop-back mode. false for no loop-back mode. ■ **twoPhaseModeFlag** - true for two phase mode. false for single phase mode. ■ **pinDelayEnableFlag** - true to enable DX pin delay. false to disable DX pin delay. ■ **phase1FrameLength** - maximum value of 127. ■ **phase2FrameLength** - maximum value of 127. ■ **clockStopMode** - MCBSP_CLOCK_SPI_MODE_NO_DELAY or MCBSP_CLOCK_SPI_MODE_DELAY ■ **phase1WordLength** - MCBSP_BITS_PER_WORD_x , x = 8, 12, 16, 20, 24, 32 ■ **phase2WordLength** - MCBSP_BITS_PER_WORD_x , x = 8, 12, 16, 20, 24, 32 ■ **compandingMode** - MCBSP_COMPANDING_NONE, MCBSP_COMPANDING_NONE_LSB_FIRST MCBSP_COMPANDING_U_LAW_SET or MCBSP_COMPANDING_A_LAW_SET. ■ **dataDelayBits** - MCBSP_DATA_DELAY_BIT_0, MCBSP_DATA_DELAY_BIT_1 or MCBSP_DATA_DELAY_BIT_2 ■ **interruptMode** - MCBSP_TX_ISR_SOURCE_TX_READY, MCBSP_TX_ISR_SOURCE_END_OF_BLOCK, MCBSP_TX_ISR_SOURCE_FRAME_S or MCBSP_TX_ISR_SOURCE_SYNC_ERROR **Note** - When using companding, phase1WordLength and phase2WordLength must be 8 bits wide.

Returns

None.

References McBSP_TxDataParams::compandingMode, McBSP_TxDataParams::dataDelayBits, McBSP_TxDataParams::interruptMode, McBSP_TxDataParams::loopbackModeFlag, MCBSP_CLOCK_MCBSP_MODE, McBSP_disableDxPinDelay(), McBSP_disableLoopback(), McBSP_disableTwoPhaseTx(), McBSP_enableDxPinDelay(), McBSP_enableLoopback(), McBSP_enableTwoPhaseTx(), MCBSP_PHASE_ONE_FRAME, MCBSP_PHASE_TWO_FRAME, McBSP_setClockStopMode(), McBSP_setTxCompandingMode(), McBSP_setTxDataDelayBits(), McBSP_setTxDataSize(), McBSP_setTxInterruptSource(), McBSP_TxDataParams::phase1FrameLength, McBSP_TxDataParams::phase1WordLength, McBSP_TxDataParams::phase2FrameLength, McBSP_TxDataParams::phase2WordLength, McBSP_TxDataParams::pinDelayEnableFlag, and McBSP_TxDataParams::twoPhaseModeFlag.

23.2.3.88 void McBSP_configureRxDataFormat (uint32_t *base*, const **McBSP_RxDataParams** ∗ *ptrDataParams*)

Configures receiver data format.

Parameters

base	is the base address of the McBSP module.
ptrDataParams	is a pointer to a structure containing data format parameters McBSP_RxDataParams. This function sets up the transmitter data format and properties. The following are valid values and ranges for the parameters of the McBSP_RxDataParams. ■ **loopbackModeFlag** - true for digital loop-back mode. false for non loop-back mode. ■ **twoPhaseModeFlag** - true for two phase mode. false for single phase mode. ■ **phase1FrameLength** - maximum value of 127. ■ **phase2FrameLength** - maximum value of 127. ■ **phase1WordLength** - MCBSP_BITS_PER_WORD_x , x = 8, 12, 16, 20, 24, 32 ■ **phase2WordLength** - MCBSP_BITS_PER_WORD_x , x = 8, 12, 16, 20, 24, 32 ■ **compandingMode** - MCBSP_COMPANDING_NONE, MCBSP_COMPANDING_NONE_LSB_FIRST MCBSP_COMPANDING_U_LAW_SET or MCBSP_COMPANDING_A_LAW_SET. ■ **dataDelayBits** - MCBSP_DATA_DELAY_BIT_0, MCBSP_DATA_DELAY_BIT_1 or MCBSP_DATA_DELAY_BIT_2 ■ **signExtMode** - MCBSP_RIGHT_JUSTIFY_FILL_ZERO, MCBSP_RIGHT_JUSTIFY_FILL_SIGN or MCBSP_LEFT_JUSTIFY_FILL_ZER0 ■ **interruptMode** - MCBSP_RX_ISR_SOURCE_SERIAL_WORD, MCBSP_RX_ISR_SOURCE_END_OF_BLOCK, MCBSP_RX_ISR_SOURCE_FRAME_S or MCBSP_RX_ISR_SOURCE_SYNC_ERROR **Note** - When using companding, phase1WordLength and phase2WordLength must be 8 bits wide.

Returns

None.

References McBSP_RxDataParams::compandingMode, McBSP_RxDataParams::dataDelayBits, McBSP_RxDataParams::interruptMode, McBSP_RxDataParams::loopbackModeFlag, MCBSP_CLOCK_MCBSP_MODE, McBSP_disableLoopback(), McBSP_disableTwoPhaseRx(), McBSP_enableLoopback(), McBSP_enableTwoPhaseRx(), MCBSP_PHASE_ONE_FRAME, MCBSP_PHASE_TWO_FRAME, McBSP_setClockStopMode(), McBSP_setRxCompandingMode(), McBSP_setRxDataDelayBits(), McBSP_setRxDataSize(), McBSP_setRxInterruptSource(), McBSP_setRxSignExtension(), McBSP_RxDataParams::phase1FrameLength, McBSP_RxDataParams::phase1WordLength, McBSP_RxDataParams::phase2FrameLength, McBSP_RxDataParams::phase2WordLength, McBSP_RxDataParams::signExtMode, and McBSP_RxDataParams::twoPhaseModeFlag.

23.2.3.89 uint16_t McBSP_configureTxMultichannel (uint32_t *base*, const **McBSP_TxMultichannelParams** ∗ *ptrMchnParams*)

Configures transmitter multichannel.

Parameters

base	is the base address of the McBSP module.
ptrMchnParams	is a pointer to a structure containing multichannel parameters McBSP_TxMultichannelParams.

This function sets up the transmitter multichannel mode. The following are valid values and ranges for the parameters of the McBSP_TxMultichannelParams.

- **channelCount** - Maximum value of 128 for partition 8 Maximum value of 32 for partition 2
- **ptrChannelsList** - Pointer to an array of size channelCount that has unique channels.
- **multichannelMode** - MCBSP_ALL_TX_CHANNELS_ENABLED, MCBSP_TX_CHANNEL_SELECTION_ENABLED, MCBSP_ENABLE_MASKED_TX_CHANNEL_SELECTION or MCBSP_SYMMERTIC_RX_TX_SELECTION
- **partition** - MCBSP_MULTICHANNEL_TWO_PARTITION or MCBSP_MULTICHANNEL_EIGHT_PARTITION

  Note

  - In 2 partition mode only channels that belong to a single even or odd block number should be listed. It is valid to have an even and odd channels. For example you can have channels [48 -63] and channels [96 - 111] enables as one belongs to an even block and the other to an odd block or two partitions. But not channels [48 - 63] and channels [112 - 127] since they both are even blocks or similar partitions.

  Returns

  returns the following error codes.
  - **MCBSP_ERROR_EXCEEDED_CHANNELS** - number of channels exceeds 128
  - **MCBSP_ERROR_2_PARTITION_A** - invalid channel combination for partition A
  - **MCBSP_ERROR_2_PARTITION_B** - invalid channel combination for partition B
  - **MCBSP_ERROR_INVALID_MODE** - invalid transmitter channel mode.

  Returns the following error codes.

- **MCBSP_ERROR_EXCEEDED_CHANNELS** - Exceeded number of channels.
- **MCBSP_ERROR_2_PARTITION_A** - Error in 2 partition A setup.
- **MCBSP_ERROR_2_PARTITION_B** - Error in 2 partition B setup.
- **MCBSP_ERROR_INVALID_MODE** - Invalid mode.

References McBSP_TxMultichannelParams::channelCountTx, MCBSP_ALL_TX_CHANNELS_ENABLED, McBSP_disableTwoPhaseTx(), McBSP_enableTxChannel(), MCBSP_ERROR_2_PARTITION_A, MCBSP_ERROR_2_PARTITION_B, MCBSP_ERROR_EXCEEDED_CHANNELS, MCBSP_MULTICHANNEL_EIGHT_PARTITION, MCBSP_MULTICHANNEL_TWO_PARTITION, McBSP_setTxChannelMode(), McBSP_setTxMultichannelPartition(), McBSP_setTxTwoPartitionBlock(), McBSP_TxMultichannelParams::multichannelModeTx, McBSP_TxMultichannelParams::partitionTx, and McBSP_TxMultichannelParams::ptrChannelsListTx.

23.2.3.90 uint16_t McBSP_configureRxMultichannel (uint32_t *base*, const **McBSP_RxMultichannelParams** ∗ *ptrMchnParams*)

Configures receiver multichannel.

Parameters

base	is the base address of the McBSP module.
ptrMchnParams	is a pointer to a structure containing multichannel parameters McBSP_RxMultiChannelParams.

This function sets up the receiver multichannel mode. The following are valid values and ranges for the parameters of the McBSPMultichannelParams.

- **channelCount** - Maximum value of 128 for partition 8 Maximum value of 32 for partition 2
- **ptrChannelsList** - Pointer to an array of size channelCount that has unique channels.
- **multichannelMode** - MCBSP_ALL_RX_CHANNELS_ENABLED, MCBSP_RX_CHANNEL_SELECTION_ENABLED,
- **partition** - MCBSP_MULTICHANNEL_TWO_PARTITION or MCBSP_MULTICHANNEL_EIGHT_PARTITION

  Note

  - In 2 partition mode only channels that belong to a single even or odd block number should be listed. It is valid to have an even and odd channels. For example you can have channels [48 - 63] and channels [96 - 111] enables as one belongs to an even block and the other to an odd block or two partitions. But not channels [48 - 63]and channels [112 - 127] since they both are even blocks or similar partitions.

  Returns

  returns the following error codes.

  - **MCBSP_ERROR_EXCEEDED_CHANNELS** - number of channels exceeds 128
  - **MCBSP_ERROR_2_PARTITION_A** - invalid channel combination for partition A
  - **MCBSP_ERROR_2_PARTITION_B** - invalid channel combination for partition B
  - **MCBSP_ERROR_INVALID_MODE** - invalid transmitter channel mode.

  Returns the following error codes.

- **MCBSP_ERROR_EXCEEDED_CHANNELS** - Exceeded number of channels.
- **MCBSP_ERROR_2_PARTITION_A** - Error in 2 partition A setup.
- **MCBSP_ERROR_2_PARTITION_B** - Error in 2 partition B setup.
- **MCBSP_ERROR_INVALID_MODE** - Invalid mode.

References McBSP_RxMultichannelParams::channelCountRx, McBSP_disableTwoPhaseRx(), McBSP_enableRxChannel(), MCBSP_ERROR_2_PARTITION_A, MCBSP_ERROR_2_PARTITION_B, MCBSP_ERROR_EXCEEDED_CHANNELS, MCBSP_MULTICHANNEL_EIGHT_PARTITION, MCBSP_MULTICHANNEL_TWO_PARTITION, MCBSP_RX_CHANNEL_SELECTION_ENABLED, McBSP_setRxChannelMode(), McBSP_setRxMultichannelPartition(), McBSP_setRxTwoPartitionBlock(), McBSP_RxMultichannelParams::multichannelModeRx, McBSP_RxMultichannelParams::partitionRx, and McBSP_RxMultichannelParams::ptrChannelsListRx.

23.2.3.91 void McBSP_configureSPIMasterMode (uint32_t *base*, const **McBSP_SPIMasterModeParams** ∗ *ptrSPIMasterMode*)

Configures McBSP in SPI master mode

Parameters

base	is the base address of the McBSP module.
ptrSPIMaster-Mode	is a pointer to a structure containing SPI parameters McBSP_SPIMasterModeParams. This function sets up the McBSP module in SPI master mode.The following are valid values and ranges for the parameters of the McBSP_SPIMasterModeParams. ■ **loopbackModeFlag** - true for digital loop-back false for no loop-back ■ **clockStopMode** - MCBSP_CLOCK_SPI_MODE_NO_DELAY or MCBSP_CLOCK_SPI_MODE_DELAY ■ **wordLength** - MCBSP_BITS_PER_WORD_x , x = 8, 12, 16, 20, 24, 32 ■ **spiMode** It represents the clock polarity can take values: • MCBSP_TX_POLARITY_RISING_EDGE or MCBSP_TX_POLARITY_FALLING_EDG ■ **clockSRGDivider** - Maximum valid value is 255.

Note

Make sure the clock divider is such that, the McBSP clock is not running faster than 1/2 the speed of the source clock.

Returns

None.

References McBSP_SPIMasterModeParams::clockSRGDivider, McBSP_SPIMasterModeParams::clockStopMode, McBSP_SPIMasterModeParams::loopbackModeFlag, MCBSP_CLOCK_SPI_MODE_DELAY, MCBSP_CLOCK_SPI_MODE_NO_DELAY, MCBSP_DATA_DELAY_BIT_1, McBSP_disableLoopback(), McBSP_disableTwoPhaseTx(), McBSP_enableLoopback(), MCBSP_INTERNAL_TX_CLOCK_SOURCE, MCBSP_PHASE_ONE_FRAME, McBSP_setClockStopMode(), McBSP_setRxDataDelayBits(), McBSP_setRxDataSize(), McBSP_setSRGDataClockDivider(), McBSP_setTxClockPolarity(), McBSP_setTxClockSource(), McBSP_setTxDataDelayBits(), McBSP_setTxDataSize(), McBSP_setTxFrameSyncPolarity(), McBSP_setTxFrameSyncSource(), McBSP_setTxInternalFrameSyncSource(), McBSP_setTxSRGClockSource(), MCBSP_SRG_TX_CLOCK_SOURCE_LSPCLK, MCBSP_TX_FRAME_SYNC_POLARITY_LOW, MCBSP_TX_INTERNAL_FRAME_SYNC_DATA, MCBSP_TX_INTERNAL_FRAME_SYNC_SOURCE, McBSP_SPIMasterModeParams::spiMode, and McBSP_SPIMasterModeParams::wordLength.

23.2.3.92 void McBSP_configureSPISlaveMode (uint32_t *base*, const **McBSP_SPISlaveModeParams** ∗ *ptrSPISlaveMode*)

Configures McBSP in SPI slave mode

Parameters

base	is the base address of the McBSP module.
ptrSPISlave-Mode	is a pointer to a structure containing SPI parameters McBSP_SPISlaveModeParams. This function sets up the McBSP module in SPI slave mode.The following are valid values and ranges for the parameters of the McBSP_SPISlaveModeParams. ■ **loopbackModeFlag** - true for digital loop-back false for no loop-back ■ **clockStopMode** - MCBSP_CLOCK_SPI_MODE_NO_DELAY or MCBSP_CLOCK_SPI_MODE_DELAY ■ **wordLength** - MCBSP_BITS_PER_WORD_x , x = 8, 12, 16, 20, 24, 32 ■ **spiMode** It represents the clock polarity and can take values: • MCBSP_RX_POLARITY_FALLING_EDGE or MCBSP_RX_POLARITY_RISING_ED

Returns

None.

References McBSP_SPISlaveModeParams::clockStopMode, McBSP_SPISlaveModeParams::loopbackModeFlag, MCBSP_CLOCK_SPI_MODE_DELAY, MCBSP_CLOCK_SPI_MODE_NO_DELAY, MCBSP_DATA_DELAY_BIT_0, McBSP_disableLoopback(), McBSP_disableTwoPhaseTx(), McBSP_enableLoopback(), MCBSP_EXTERNAL_TX_CLOCK_SOURCE, MCBSP_PHASE_ONE_FRAME, McBSP_setClockStopMode(), McBSP_setRxDataDelayBits(), McBSP_setRxDataSize(), McBSP_setRxSRGClockSource(), McBSP_setSRGDataClockDivider(), McBSP_setTxClockPolarity(), McBSP_setTxClockSource(), McBSP_setTxDataDelayBits(), McBSP_setTxDataSize(), McBSP_setTxFrameSyncPolarity(), McBSP_setTxFrameSyncSource(), MCBSP_SRG_RX_CLOCK_SOURCE_LSPCLK, MCBSP_TX_EXTERNAL_FRAME_SYNC_SOURCE, MCBSP_TX_FRAME_SYNC_POLARITY_LOW, McBSP_SPISlaveModeParams::spiMode, and McBSP_SPISlaveModeParams::wordLength.

24 MemCfg Module

24.1 MemCfg Introduction

The MemCfg module provides an API to configure the device's Memory Control Module. The functions that are provided fall into three main categories: RAM section configuration, access violation status and interrupts, and memory error status an interrupts. The RAM section configuration functions can initialize RAM, configure access protection settings, and configure section ownership. The access violation and memory error categories contain functions that can return violation and error status and address information as well as configure interrupts that can be generated as a result of these issues.

24.2 API Functions

Enumerations

- enum MemCfg_CLAMemoryType { MEMCFG_CLA_MEM_DATA, MEMCFG_CLA_MEM_PROGRAM }
- enum MemCfg_LSRAMMasterSel { MEMCFG_LSRAMMASTER_CPU_ONLY, MEMCFG_LSRAMMASTER_CPU_CLA1 }
- enum MemCfg_GSRAMMasterSel { MEMCFG_GSRAMMASTER_CPU1, MEMCFG_GSRAMMASTER_CPU2 }
- enum MemCfg_TestMode { MEMCFG_TEST_FUNCTIONAL, MEMCFG_TEST_WRITE_DATA, MEMCFG_TEST_WRITE_ECC, MEMCFG_TEST_WRITE_PARITY }

Functions

- static void MemCfg_setCLAMemType (uint32_t ramSections, MemCfg_CLAMemoryType claMemType)
- static void MemCfg_enableViolationInterrupt (uint32_t intFlags)
- static void MemCfg_disableViolationInterrupt (uint32_t intFlags)
- static uint32_t MemCfg_getViolationInterruptStatus (void)
- static void MemCfg_forceViolationInterrupt (uint32_t intFlags)
- static void MemCfg_clearViolationInterruptStatus (uint32_t intFlags)
- static void MemCfg_setCorrErrorThreshold (uint32_t threshold)
- static uint32_t MemCfg_getCorrErrorCount (void)
- static void MemCfg_enableCorrErrorInterrupt (uint32_t intFlags)
- static void MemCfg_disableCorrErrorInterrupt (uint32_t intFlags)
- static uint32_t MemCfg_getCorrErrorInterruptStatus (void)
- static void MemCfg_forceCorrErrorInterrupt (uint32_t intFlags)
- static void MemCfg_clearCorrErrorInterruptStatus (uint32_t intFlags)
- static uint32_t MemCfg_getCorrErrorStatus (void)
- static uint32_t MemCfg_getUncorrErrorStatus (void)

- static void MemCfg_forceCorrErrorStatus (uint32_t stsFlags)
- static void MemCfg_forceUncorrErrorStatus (uint32_t stsFlags)
- static void MemCfg_clearCorrErrorStatus (uint32_t stsFlags)
- static void MemCfg_clearUncorrErrorStatus (uint32_t stsFlags)
- static void MemCfg_enableROMWaitState (void)
- static void MemCfg_disableROMWaitState (void)
- static void MemCfg_enableROMPrefetch (void)
- static void MemCfg_disableROMPrefetch (void)
- void MemCfg_lockConfig (uint32_t memSections)
- void MemCfg_unlockConfig (uint32_t memSections)
- void MemCfg_commitConfig (uint32_t memSections)
- void MemCfg_setProtection (uint32_t memSection, uint32_t protectMode)
- void MemCfg_setLSRAMMasterSel (uint32_t ramSection, MemCfg_LSRAMMasterSel masterSel)
- void MemCfg_setGSRAMMasterSel (uint32_t ramSections, MemCfg_GSRAMMasterSel masterSel)
- void MemCfg_setTestMode (uint32_t memSection, MemCfg_TestMode testMode)
- void MemCfg_initSections (uint32_t ramSections)
- bool MemCfg_getInitStatus (uint32_t ramSections)
- uint32_t MemCfg_getViolationAddress (uint32_t intFlag)
- uint32_t MemCfg_getCorrErrorAddress (uint32_t stsFlag)
- uint32_t MemCfg_getUncorrErrorAddress (uint32_t stsFlag)

24.2.1 Detailed Description

Many of the functions provided by this API to configure RAM sections' settings will take a RAM section identifier or an OR of several identifiers as a parameter. These are defines with names in the format **MEMCFG_SECT_X**. Take care to read the function description to learn which functions can operate on multiple sections of the same type at a time and which ones can only configure one section at a time. A quick way to check this is to see if the parameter says ramSection or the plural ramSections. Some functions may also be able to take a **MEMCFG_SECT_ALL** value to indicate that all RAM sections should be operated on at the same time. Again, read the function's detailed description to be sure.

The code for this module is contained in `driverlib/memcfg.c`, with `driverlib/memcfg.h` containing the API declarations for use by applications.

24.2.2 Enumeration Type Documentation

24.2.2.1 enum **MemCfg_CLAMemoryType**

Values that can be passed to MemCfg_setCLAMemType() as the *claMemType* parameter.

Enumerator

MEMCFG_CLA_MEM_DATA Section is CLA data memory.

MEMCFG_CLA_MEM_PROGRAM Section is CLA program memory.

24.2.2.2 enum **MemCfg_LSRAMMasterSel**

Values that can be passed to MemCfg_setLSRAMMasterSel() as the *masterSel* parameter.

Enumerator

MEMCFG_LSRAMMASTER_CPU_ONLY CPU is the master of the section.

MEMCFG_LSRAMMASTER_CPU_CLA1 CPU and CLA1 share this section.

24.2.2.3 enum **MemCfg_GSRAMMasterSel**

Values that can be passed to MemCfg_setGSRAMMasterSel() as the *masterSel* parameter.

Enumerator

MEMCFG_GSRAMMASTER_CPU1 CPU1 is master of the section.

MEMCFG_GSRAMMASTER_CPU2 CPU2 is master of the section.

24.2.2.4 enum **MemCfg_TestMode**

Values that can be passed to MemCfg_setTestMode() as the *testMode* parameter.

Enumerator

MEMCFG_TEST_FUNCTIONAL Functional mode.

MEMCFG_TEST_WRITE_DATA Writes allowed to data only.

MEMCFG_TEST_WRITE_ECC Writes allowed to ECC only (for DxRAM)

MEMCFG_TEST_WRITE_PARITY Writes allowed to parity only (for LSxRAM, GSxRAM, and MSGxRAM)

24.2.3 Function Documentation

24.2.3.1 static void MemCfg_setCLAMemType (uint32_t *ramSections,* **MemCfg_CLAMemoryType** *claMemType*) `[inline]`, `[static]`

Sets the CLA memory type of the specified RAM section.

Parameters

ramSections	is the logical OR of the sections to be configured.
claMemType	indicates data memory or program memory.

This function sets the CLA memory type configuration of the RAM section. If the *claMemType* parameter is **MEMCFG_CLA_MEM_DATA**, the RAM section will be configured as CLA data memory. If **MEMCFG_CLA_MEM_PROGRAM**, the RAM section will be configured as CLA program memory.

The *ramSections* parameter is an OR of the following indicators: **MEMCFG_SECT_LS0** through **MEMCFG_SECT_LSx**.

Note

This API only applies to LSx RAM and has no effect if the CLA isn't master of the memory section.

See Also

MemCfg_setLSRAMMasterSel()

Returns

None.

References MEMCFG_CLA_MEM_PROGRAM.

24.2.3.2 static void MemCfg_enableViolationInterrupt (uint32_t *intFlags*) [inline], [static]

Enables individual RAM access violation interrupt sources.

Parameters

intFlags	is a bit mask of the interrupt sources to be enabled. Can be a logical OR any of the following values: ■ **MEMCFG_NMVIOL_CPUREAD** - Non-master CPU read access ■ **MEMCFG_NMVIOL_CPUWRITE** - Non-master CPU write access ■ **MEMCFG_NMVIOL_CPUFETCH** - Non-master CPU fetch access ■ **MEMCFG_NMVIOL_DMAWRITE** - Non-master DMA write access ■ **MEMCFG_NMVIOL_CLA1READ** - Non-master CLA1 read access ■ **MEMCFG_NMVIOL_CLA1WRITE** - Non-master CLA1 write access ■ **MEMCFG_NMVIOL_CLA1FETCH** - Non-master CLA1 fetch access ■ **MEMCFG_MVIOL_CPUFETCH** - Master CPU fetch access ■ **MEMCFG_MVIOL_CPUWRITE** - Master CPU write access ■ **MEMCFG_MVIOL_DMAWRITE** - Master DMA write access

This function enables the indicated RAM access violation interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

Returns
None.

24.2.3.3 static void MemCfg_disableViolationInterrupt (uint32_t *intFlags*) [inline], [static]

Disables individual RAM access violation interrupt sources.

Parameters

intFlags	is a bit mask of the interrupt sources to be disabled. Can be a logical OR any of the following values: ■ **MEMCFG_NMVIOL_CPUREAD** ■ **MEMCFG_NMVIOL_CPUWRITE** ■ **MEMCFG_NMVIOL_CPUFETCH** ■ **MEMCFG_NMVIOL_DMAWRITE** ■ **MEMCFG_NMVIOL_CLA1READ** ■ **MEMCFG_NMVIOL_CLA1WRITE** ■ **MEMCFG_NMVIOL_CLA1FETCH** ■ **MEMCFG_MVIOL_CPUFETCH** ■ **MEMCFG_MVIOL_CPUWRITE** ■ **MEMCFG_MVIOL_DMAWRITE**

This function disables the indicated RAM access violation interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

Note
Note that only non-master violations may generate interrupts.

Returns
None.

24.2.3.4 static uint32_t MemCfg_getViolationInterruptStatus (void) [inline], [static]

Gets the current RAM access violation status.

This function returns the RAM access violation status. This function will return flags for both master and non-master access violations although only the non-master flags have the ability to cause the generation of an interrupt.

Returns
Returns the current violation status, enumerated as a bit field of the values:
- **MEMCFG_NMVIOL_CPUREAD** - Non-master CPU read access
- **MEMCFG_NMVIOL_CPUWRITE** - Non-master CPU write access

- **MEMCFG_NMVIOL_CPUFETCH** - Non-master CPU fetch access
- **MEMCFG_NMVIOL_DMAWRITE** - Non-master DMA write access
- **MEMCFG_NMVIOL_CLA1READ** - Non-master CLA1 read access
- **MEMCFG_NMVIOL_CLA1WRITE** - Non-master CLA1 write access
- **MEMCFG_NMVIOL_CLA1FETCH** - Non-master CLA1 fetch access
- **MEMCFG_MVIOL_CPUFETCH** - Master CPU fetch access
- **MEMCFG_MVIOL_CPUWRITE** - Master CPU write access
- **MEMCFG_MVIOL_DMAWRITE** - Master DMA write access

24.2.3.5 static void MemCfg_forceViolationInterrupt (uint32_t *intFlags*) `[inline]`, `[static]`

Sets the RAM access violation status.

Parameters

intFlags	is a bit mask of the access violation flags to be set. Can be a logical OR any of the following values: ■ **MEMCFG_NMVIOL_CPUREAD** ■ **MEMCFG_NMVIOL_CPUWRITE** ■ **MEMCFG_NMVIOL_CPUFETCH** ■ **MEMCFG_NMVIOL_DMAWRITE** ■ **MEMCFG_NMVIOL_CLA1READ** ■ **MEMCFG_NMVIOL_CLA1WRITE** ■ **MEMCFG_NMVIOL_CLA1FETCH** ■ **MEMCFG_MVIOL_CPUFETCH** ■ **MEMCFG_MVIOL_CPUWRITE** ■ **MEMCFG_MVIOL_DMAWRITE**

This function sets the RAM access violation status. This function will set flags for both master and non-master access violations, and an interrupt will be generated if it is enabled.

Returns

None.

24.2.3.6 static void MemCfg_clearViolationInterruptStatus (uint32_t *intFlags*) `[inline]`, `[static]`

Clears RAM access violation flags.

Parameters

intFlags	is a bit mask of the access violation flags to be cleared. Can be a logical OR any of the following values: ■ **MEMCFG_NMVIOL_CPUREAD** ■ **MEMCFG_NMVIOL_CPUWRITE** ■ **MEMCFG_NMVIOL_CPUFETCH** ■ **MEMCFG_NMVIOL_DMAWRITE** ■ **MEMCFG_NMVIOL_CLA1READ** ■ **MEMCFG_NMVIOL_CLA1WRITE** ■ **MEMCFG_NMVIOL_CLA1FETCH** ■ **MEMCFG_MVIOL_CPUFETCH** ■ **MEMCFG_MVIOL_CPUWRITE** ■ **MEMCFG_MVIOL_DMAWRITE**

Returns
None.

24.2.3.7 static void MemCfg_setCorrErrorThreshold (uint32_t *threshold*) `[inline]`, `[static]`

Sets the correctable error threshold value.

Parameters

threshold	is the correctable error threshold.

This value sets the error-count threshold at which a correctable error interrupt is generated. That is when the error count register reaches the value specified by the *threshold* parameter, an interrupt is generated if it is enabled.

Returns
None.

24.2.3.8 static uint32_t MemCfg_getCorrErrorCount (void) `[inline]`, `[static]`

Gets the correctable error count.

Returns
Returns the number of correctable error have occurred.

24.2.3.9 static void MemCfg_enableCorrErrorInterrupt (uint32_t *intFlags*) `[inline]`, `[static]`

Enables individual RAM correctable error interrupt sources.

Parameters

intFlags	is a bit mask of the interrupt sources to be enabled. Can take the value **MEMCFG_CERR_CPUREAD** only. Other values are reserved.

This function enables the indicated RAM correctable error interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

Note

Note that only correctable errors may generate interrupts.

Returns

None.

24.2.3.10 static void MemCfg_disableCorrErrorInterrupt (uint32_t *intFlags*) [inline], [static]

Disables individual RAM correctable error interrupt sources.

Parameters

intFlags	is a bit mask of the interrupt sources to be disabled. Can take the value **MEMCFG_CERR_CPUREAD** only. Other values are reserved.

This function disables the indicated RAM correctable error interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

Note

Note that only correctable errors may generate interrupts.

Returns

None.

24.2.3.11 static uint32_t MemCfg_getCorrErrorInterruptStatus (void) [inline], [static]

Gets the current RAM correctable error interrupt status.

Returns

Returns the current error interrupt status. Will return a value of **MEMCFG_CERR_CPUREAD** if an interrupt has been generated. If not, the function will return 0.

24.2.3.12 static void MemCfg_forceCorrErrorInterrupt (uint32_t *intFlags*) [inline], [static]

Sets the RAM correctable error interrupt status.

Parameters

intFlags	is a bit mask of the interrupt sources to be set. Can take the value **MEMCFG_CERR_CPUREAD** only. Other values are reserved.

This function sets the correctable error interrupt flag.

Note

Note that only correctable errors may generate interrupts.

Returns

None.

24.2.3.13 static void MemCfg_clearCorrErrorInterruptStatus (uint32_t *intFlags*) [inline], [static]

Clears the RAM correctable error interrupt status.

Parameters

intFlags	is a bit mask of the interrupt sources to be cleared. Can take the value **MEMCFG_CERR_CPUREAD** only. Other values are reserved.

This function clears the correctable error interrupt flag.

Note

Note that only correctable errors may generate interrupts.

Returns

None.

24.2.3.14 static uint32_t MemCfg_getCorrErrorStatus (void) [inline], [static]

Gets the current correctable RAM error status.

Returns

Returns the current error status, enumerated as a bit field of **MEMCFG_CERR_CPUREAD**, **MEMCFG_CERR_DMAREAD**, or **MEMCFG_CERR_CLA1READ**

24.2.3.15 static uint32_t MemCfg_getUncorrErrorStatus (void) [inline], [static]

Gets the current uncorrectable RAM error status.

Returns

Returns the current error status, enumerated as a bit field of **MEMCFG_UCERR_CPUREAD**, **MEMCFG_UCERR_DMAREAD**, **MEMCFG_UCERR_CLA1READ**, or **MEMCFG_UCERR_ECATMEMREAD**.

24.2.3.16 static void MemCfg_forceCorrErrorStatus (uint32_t *stsFlags*) [inline], [static]

Sets the specified correctable RAM error status flag.

Parameters

stsFlags	is a bit mask of the error sources. This parameter can be any of the following values: **MEMCFG_CERR_CPUREAD**, **MEMCFG_CERR_DMAREAD**, or **MEMCFG_CERR_CLA1READ**.

This function sets the specified correctable RAM error status flag.

Returns
None.

24.2.3.17 static void MemCfg_forceUncorrErrorStatus (uint32_t *stsFlags*) [inline], [static]

Sets the specified uncorrectable RAM error status flag.

Parameters

stsFlags	is a bit mask of the error sources. This parameter can be any of the following values: **MEMCFG_UCERR_CPUREAD**, **MEMCFG_UCERR_DMAREAD**, **MEMCFG_UCERR_CLA1READ**, or **MEMCFG_UCERR_ECATMEMREAD**.

This function sets the specified uncorrectable RAM error status flag.

Returns
None.

24.2.3.18 static void MemCfg_clearCorrErrorStatus (uint32_t *stsFlags*) [inline], [static]

Clears correctable RAM error flags.

Parameters

stsFlags	is a bit mask of the status flags to be cleared. This parameter can be any of the **MEMCFG_CERR_CPUREAD**, **MEMCFG_CERR_DMAREAD**, or **MEMCFG_CERR_CLA1READ** values.

This function clears the specified correctable RAM error flags.

Returns
None.

24.2.3.19 static void MemCfg_clearUncorrErrorStatus (uint32_t *stsFlags*) [inline], [static]

Clears uncorrectable RAM error flags.

Parameters

stsFlags	is a bit mask of the status flags to be cleared. This parameter can be any of the **MEMCFG_UCERR_CPUREAD**, **MEMCFG_UCERR_DMAREAD**, **MEMCFG_UCERR_CLA1READ**, or **MEMCFG_UCERR_ECATMEMREAD** values.

This function clears the specified uncorrectable RAM error flags.

Returns
None.

24.2.3.20 static void MemCfg_enableROMWaitState (void) [inline], [static]

Enables ROM wait state.

This function enables the ROM wait state. This mean CPU accesses to ROM are 1-wait.

Returns
None.

24.2.3.21 static void MemCfg_disableROMWaitState (void) [inline], [static]

Disables ROM wait state.

This function enables the ROM wait state. This mean CPU accesses to ROM are 0-wait.

Returns
None.

24.2.3.22 static void MemCfg_enableROMPrefetch (void) [inline], [static]

Enables ROM prefetch.

This function enables the ROM prefetch for both secure ROM and boot ROM.

Returns
None.

24.2.3.23 static void MemCfg_disableROMPrefetch (void) [inline], [static]

Disables ROM prefetch.

This function enables the ROM prefetch for both secure ROM and boot ROM.

Returns
None.

24.2.3.24 void MemCfg_lockConfig (uint32_t *memSections*)

Locks the writes to the configuration of specified memory sections.

Parameters

memSections	is the logical OR of the sections to be configured.

This function locks writes to the access protection and master select configuration of a memory section.That means calling MemCfg_setProtection() or MemCfg_setLSRAMMasterSel() for a locked memory section will have no effect until MemCfg_unlockConfig() is called.

The *memSections* parameter is an OR of one of the following sets of indicators:

- **MEMCFG_SECT_D0** and **MEMCFG_SECT_D1** or **MEMCFG_SECT_DX_ALL**
- **MEMCFG_SECT_LS0** through **MEMCFG_SECT_LSx** or **MEMCFG_SECT_LSX_ALL**
- **MEMCFG_SECT_GS0** through **MEMCFG_SECT_GSx** or **MEMCFG_SECT_GSX_ALL**
- **OR** use **MEMCFG_SECT_ALL** to configure all possible sections.

Returns
None.

24.2.3.25 void MemCfg_unlockConfig (uint32_t *memSections*)

Unlocks the writes to the configuration of a memory section.

Parameters

memSections	is the logical OR of the sections to be configured.

This function unlocks writes to the access protection and master select configuration of a memory section that has been locked using MemCfg_lockConfig().

The *memSections* parameter is an OR of one of the following sets of indicators:

- **MEMCFG_SECT_D0** and **MEMCFG_SECT_D1** or **MEMCFG_SECT_DX_ALL**
- **MEMCFG_SECT_LS0** through **MEMCFG_SECT_LSx** or **MEMCFG_SECT_LSX_ALL**
- **MEMCFG_SECT_GS0** through **MEMCFG_SECT_GSx** or **MEMCFG_SECT_GSX_ALL**
- **OR** use **MEMCFG_SECT_ALL** to configure all possible sections.

Returns
None.

24.2.3.26 void MemCfg_commitConfig (uint32_t *memSections*)

Permanently locks writes to the configuration of a memory section.

Parameters

memSections	is the logical OR of the sections to be configured.

This function permanently locks writes to the access protection and master select configuration of a memory section. That means calling MemCfg_setProtection() or MemCfg_setLSRAMMasterSel() for a locked memory section will have no effect. To lock the configuration in a nonpermanent way, use MemCfg_lockConfig().

The *memSections* parameter is an OR of one of the following sets of indicators:

- **MEMCFG_SECT_D0** and **MEMCFG_SECT_D1** or **MEMCFG_SECT_DX_ALL**
- **MEMCFG_SECT_LS0** through **MEMCFG_SECT_LSx** or **MEMCFG_SECT_LSX_ALL**
- **MEMCFG_SECT_GS0** through **MEMCFG_SECT_GSx** or **MEMCFG_SECT_GSX_ALL**
- **OR** use **MEMCFG_SECT_ALL** to configure all possible sections.

Returns
None.

24.2.3.27 void MemCfg_setProtection (uint32_t *memSection,* uint32_t *protectMode*)

Sets the access protection mode of a single memory section.

Parameters

memSection	is the memory section to be configured.
protectMode	is the logical OR of the settings to be applied.

This function sets the access protection mode of a specified memory section. The mode is passed into the *protectMode* parameter as the logical OR of the following values:

- **MEMCFG_PROT_ALLOWCPUFETCH** or **MEMCFG_PROT_BLOCKCPUFETCH** - CPU fetch
- **MEMCFG_PROT_ALLOWCPUWRITE** or **MEMCFG_PROT_BLOCKCPUWRITE** - CPU write
- **MEMCFG_PROT_ALLOWDMAWRITE** or **MEMCFG_PROT_BLOCKDMAWRITE** - DMA write

The *memSection* parameter is one of the following indicators:

- **MEMCFG_SECT_D0** or **MEMCFG_SECT_D1**
- **MEMCFG_SECT_LS0** through **MEMCFG_SECT_LSx**
- **MEMCFG_SECT_GS0** through **MEMCFG_SECT_GSx**

This function will have no effect if the associated registers have been locked by MemCfg_lockConfig() or MemCfg_commitConfig() or if the memory is configured as CLA program memory.

Returns
None.

24.2.3.28 void MemCfg_setLSRAMMasterSel (uint32_t *ramSection,* **MemCfg_LSRAMMasterSel** *masterSel*)

Sets the master of the specified LSxRAM section.

Parameters

ramSection	is the LSxRAM section to be configured.
masterSel	is the sharing selection.

This function sets the master select configuration of the LSxRAM section.If the *masterSel* parameter is **MEMCFG_LSRAMMASTER_CPU_ONLY**, the LSxRAM section passed into the *ramSection* parameter will be dedicated to the CPU. If **MEMCFG_LSRAMMASTER_CPU_CLA1**, the memory section will be shared between the CPU and the CLA.

The *ramSection* parameter should be a value from **MEMCFG_SECT_LS0** through **MEMCFG_SECT_LSx**.

This function will have no effect if the associated registers have been locked by MemCfg_lockConfig() or MemCfg_commitConfig().

Note

This API only applies to LSxRAM.

Returns

None.

24.2.3.29 void MemCfg_setGSRAMMasterSel (uint32_t *ramSections,* **MemCfg_GSRAMMasterSel** *masterSel*)

Sets the master of the specified GSxRAM section.

Parameters

ramSections	is the logical OR of the sections to be configured.
masterSel	is the sharing selection.

This function sets the master select configuration of the GSxRAM section.If the *masterSel* parameter is **MEMCFG_GSRAMMASTER_CPU1**, the GSRAM sections passed into the *ramSections* parameter will be dedicated to CPU1. If **MEMCFG_GSRAMMASTER_CPU2**, the memory section will be dedicated to CPU2.

The *ramSections* parameter should be a logical OR of values from **MEMCFG_SECT_GS0** through **MEMCFG_SECT_GSx**.

This function will have no effect if the associated registers have been locked by MemCfg_lockConfig() or MemCfg_commitConfig().

Note

This API only applies to GSxRAM.

Returns

None.

References MEMCFG_GSRAMMASTER_CPU1.

24.2.3.30 void MemCfg_setTestMode (uint32_t *memSection,* **MemCfg_TestMode** *testMode*)

Sets the test mode of the specified memory section.

Parameters

memSection	is the memory section to be configured.
testMode	is the test mode selected.

This function sets the test mode configuration of the RAM section. The *testMode* parameter can take one of the following values:

- **MEMCFG_TEST_FUNCTIONAL**
- **MEMCFG_TEST_WRITE_DATA**
- **MEMCFG_TEST_WRITE_ECC** (DxRAM) or MEMCFG_TEST_WRITE_PARITY (LSx, GSx, or MSGxRAM)

The *memSection* parameter is one of the following indicators:

- **MEMCFG_SECT_M0** or **MEMCFG_SECT_M1**
- **MEMCFG_SECT_D0** or **MEMCFG_SECT_D1**
- **MEMCFG_SECT_LS0** through **MEMCFG_SECT_LSx**
- **MEMCFG_SECT_GS0** through **MEMCFG_SECT_GSx**
- **MEMCFG_SECT_MSGCPUTOCPU**, **MEMCFG_SECT_MSGCPUTOCLA1**, or **MEMCFG_SECT_MSGCLA1TOCPU**

Returns

None.

24.2.3.31 void MemCfg_initSections (uint32_t *ramSections*)

Starts the initialization the specified RAM sections.

Parameters

ramSections	is the logical OR of the sections to be initialized.

This function starts the initialization of the specified RAM sections. Use MemCfg_getInitStatus() to check if the initialization is done.

The *ramSections* parameter is an OR of one of the following sets of indicators:

- **MEMCFG_SECT_D0** and **MEMCFG_SECT_D1** or **MEMCFG_SECT_DX_ALL**
- **MEMCFG_SECT_LS0** through **MEMCFG_SECT_LSx** or **MEMCFG_SECT_LSX_ALL**
- **MEMCFG_SECT_GS0** through **MEMCFG_SECT_GSx** or **MEMCFG_SECT_GSX_ALL**
- **MEMCFG_SECT_MSGCPUTOCPU**, **MEMCFG_SECT_MSGCPUTOCLA1**, and **MEMCFG_SECT_MSGCLA1TOCPU** or **MEMCFG_SECT_MSGX_ALL**
- **OR** use **MEMCFG_SECT_ALL** to configure all possible sections.

Returns

None.

24.2.3.32 bool MemCfg_getInitStatus (uint32_t *ramSections*)

Get the status of initialized RAM sections.

Parameters

ramSections	is the logical OR of the sections to be checked.

This function gets the initialization status of the RAM sections specified by the *ramSections* parameter.

The *ramSections* parameter is an OR of one of the following sets of indicators:

- **MEMCFG_SECT_M0**, **MEMCFG_SECT_M1**, **MEMCFG_SECT_D0**, and **MEMCFG_SECT_D1** or **MEMCFG_SECT_DX_ALL**
- **MEMCFG_SECT_LS0** through **MEMCFG_SECT_LSx** or **MEMCFG_SECT_LSX_ALL**
- **MEMCFG_SECT_GS0** through **MEMCFG_SECT_GSx** or **MEMCFG_SECT_GSX_ALL**
- **MEMCFG_SECT_MSGCPUTOCPU**, **MEMCFG_SECT_MSGCPUTOCLA1**, and **MEMCFG_SECT_MSGCLA1TOCPU** or **MEMCFG_SECT_MSGX_ALL**
- **OR** use **MEMCFG_SECT_ALL** to get status of all possible sections.

Note

Use MemCfg_initSections() to start the initialization.

Returns

Returns **true** if all the sections specified by *ramSections* have been initialized and **false** if not.

24.2.3.33 uint32_t MemCfg_getViolationAddress (uint32_t *intFlag*)

Get the violation address associated with a intFlag.

Parameters

intFlag	is the type of access violation as indicated by ONE of these values: ■ **MEMCFG_NMVIOL_CPUREAD** ■ **MEMCFG_NMVIOL_CPUWRITE** ■ **MEMCFG_NMVIOL_CPUFETCH** ■ **MEMCFG_NMVIOL_DMAWRITE** ■ **MEMCFG_NMVIOL_CLA1READ** ■ **MEMCFG_NMVIOL_CLA1WRITE** ■ **MEMCFG_NMVIOL_CLA1FETCH** ■ **MEMCFG_MVIOL_CPUFETCH** ■ **MEMCFG_MVIOL_CPUWRITE** ■ **MEMCFG_MVIOL_DMAWRITE**

Returns

Returns the violation address associated with the *intFlag*.

24.2.3.34 uint32_t MemCfg_getCorrErrorAddress (uint32_t *stsFlag*)

Get the correctable error address associated with a stsFlag.

Parameters

stsFlag	is the type of error to which the returned address will correspond. Can currently take the value **MEMCFG_CERR_CPUREAD** only. Other values are reserved.

Returns

Returns the error address associated with the stsFlag.

24.2.3.35 uint32_t MemCfg_getUncorrErrorAddress (uint32_t *stsFlag*)

Get the uncorrectable error address associated with a stsFlag.

Parameters

stsFlag	is the type of error to which the returned address will correspond. It may be passed one of these values: **MEMCFG_UCERR_CPUREAD**, **MEMCFG_UCERR_DMAREAD**, **MEMCFG_UCERR_CLA1READ**, or **MEMCFG_UCERR_ECATMEMREAD** values.

Returns

Returns the error address associated with the stsFlag.

25 SCI Module

25.1 SCI Introduction

The SCI driver provides functions which can configure the data word length, baud rate, parity, and stop bits of the SCI communication. It can also be used to perform an autobaud lock, enable or disable loopback mode, enable the FIFO enhancement, configure interrupts, and send and receive data. If FIFO enhancement is enabled, the application must use the provided FIFO read and write functions to guarantee proper execution.

25.2 API Functions

Macros

- #define SCI_INT_RXERR
- #define SCI_INT_RXRDY_BRKDT
- #define SCI_INT_TXRDY
- #define SCI_INT_TXFF
- #define SCI_INT_RXFF
- #define SCI_INT_FE
- #define SCI_INT_OE
- #define SCI_INT_PE
- #define SCI_CONFIG_WLEN_MASK
- #define SCI_CONFIG_WLEN_8
- #define SCI_CONFIG_WLEN_7
- #define SCI_CONFIG_WLEN_6
- #define SCI_CONFIG_WLEN_5
- #define SCI_CONFIG_WLEN_4
- #define SCI_CONFIG_WLEN_3
- #define SCI_CONFIG_WLEN_2
- #define SCI_CONFIG_WLEN_1
- #define SCI_CONFIG_STOP_MASK
- #define SCI_CONFIG_STOP_ONE
- #define SCI_CONFIG_STOP_TWO
- #define SCI_CONFIG_PAR_MASK
- #define SCI_RXSTATUS_WAKE
- #define SCI_RXSTATUS_PARITY
- #define SCI_RXSTATUS_OVERRUN
- #define SCI_RXSTATUS_FRAMING
- #define SCI_RXSTATUS_BREAK
- #define SCI_RXSTATUS_READY
- #define SCI_RXSTATUS_ERROR

Enumerations

- enum SCI_ParityType { SCI_CONFIG_PAR_NONE, SCI_CONFIG_PAR_EVEN, SCI_CONFIG_PAR_ODD }
- enum SCI_TxFIFOLevel {
  SCI_FIFO_TX0, SCI_FIFO_TX1, SCI_FIFO_TX2, SCI_FIFO_TX3,
  SCI_FIFO_TX4, SCI_FIFO_TX5, SCI_FIFO_TX6, SCI_FIFO_TX7,
  SCI_FIFO_TX8, SCI_FIFO_TX9, SCI_FIFO_TX10, SCI_FIFO_TX11,
  SCI_FIFO_TX12, SCI_FIFO_TX13, SCI_FIFO_TX14, SCI_FIFO_TX15,
  SCI_FIFO_TX16 }
- enum SCI_RxFIFOLevel {
  SCI_FIFO_RX0, SCI_FIFO_RX1, SCI_FIFO_RX2, SCI_FIFO_RX3,
  SCI_FIFO_RX4, SCI_FIFO_RX5, SCI_FIFO_RX6, SCI_FIFO_RX7,
  SCI_FIFO_RX8, SCI_FIFO_RX9, SCI_FIFO_RX10, SCI_FIFO_RX11,
  SCI_FIFO_RX12, SCI_FIFO_RX13, SCI_FIFO_RX14, SCI_FIFO_RX15,
  SCI_FIFO_RX16 }

Functions

- static void SCI_setParityMode (uint32_t base, SCI_ParityType parity)
- static SCI_ParityType SCI_getParityMode (uint32_t base)
- static void SCI_lockAutobaud (uint32_t base)
- static void SCI_setFIFOInterruptLevel (uint32_t base, SCI_TxFIFOLevel txLevel, SCI_RxFIFOLevel rxLevel)
- static void SCI_getFIFOInterruptLevel (uint32_t base, SCI_TxFIFOLevel ∗txLevel, SCI_RxFIFOLevel ∗rxLevel)
- static void SCI_getConfig (uint32_t base, uint32_t lspclkHz, uint32_t ∗baud, uint32_t ∗config)
- static void SCI_enableModule (uint32_t base)
- static void SCI_disableModule (uint32_t base)
- static void SCI_enableFIFO (uint32_t base)
- static void SCI_disableFIFO (uint32_t base)
- static bool SCI_isFIFOEnabled (uint32_t base)
- static void SCI_resetRxFIFO (uint32_t base)
- static void SCI_resetTxFIFO (uint32_t base)
- static void SCI_resetChannels (uint32_t base)
- static bool SCI_isDataAvailableNonFIFO (uint32_t base)
- static bool SCI_isSpaceAvailableNonFIFO (uint32_t base)
- static SCI_TxFIFOLevel SCI_getTxFIFOStatus (uint32_t base)
- static SCI_RxFIFOLevel SCI_getRxFIFOStatus (uint32_t base)
- static bool SCI_isTransmitterBusy (uint32_t base)
- static void SCI_writeCharBlockingFIFO (uint32_t base, uint16_t data)
- static void SCI_writeCharBlockingNonFIFO (uint32_t base, uint16_t data)
- static void SCI_writeCharNonBlocking (uint32_t base, uint16_t data)
- static uint16_t SCI_readCharBlockingFIFO (uint32_t base)
- static uint16_t SCI_readCharBlockingNonFIFO (uint32_t base)
- static uint16_t SCI_readCharNonBlocking (uint32_t base)
- static uint16_t SCI_getRxStatus (uint32_t base)
- static void SCI_performSoftwareReset (uint32_t base)
- static void SCI_enableLoopback (uint32_t base)
- static void SCI_disableLoopback (uint32_t base)
- static bool SCI_getOverflowStatus (uint32_t base)
- static void SCI_clearOverflowStatus (uint32_t base)
- void SCI_setConfig (uint32_t base, uint32_t lspclkHz, uint32_t baud, uint32_t config)
- void SCI_writeCharArray (uint32_t base, const uint16_t ∗const array, uint16_t length)
- void SCI_readCharArray (uint32_t base, uint16_t ∗const array, uint16_t length)

- void SCI_enableInterrupt (uint32_t base, uint32_t intFlags)
- void SCI_disableInterrupt (uint32_t base, uint32_t intFlags)
- uint32_t SCI_getInterruptStatus (uint32_t base)
- void SCI_clearInterruptStatus (uint32_t base, uint32_t intFlags)

25.2.1 Detailed Description

The code for this module is contained in `driverlib/sci.c`, with `driverlib/sci.h` containing the API declarations for use by applications.

25.2.2 Enumeration Type Documentation

25.2.2.1 enum **SCI_ParityType**

Values that can be used with SCI_setParityMode() and SCI_getParityMode() to describe the parity of the SCI communication.

Enumerator

SCI_CONFIG_PAR_NONE No parity.
SCI_CONFIG_PAR_EVEN Even parity.
SCI_CONFIG_PAR_ODD Odd parity.

25.2.2.2 enum **SCI_TxFIFOLevel**

Values that can be passed to SCI_setFIFOInterruptLevel() as the txLevel parameter and returned by SCI_getFIFOInteruptLevel() and SCI_getTxFIFOStatus().

Enumerator

SCI_FIFO_TX0 Transmit interrupt empty.
SCI_FIFO_TX1 Transmit interrupt 1/16 full.
SCI_FIFO_TX2 Transmit interrupt 2/16 full.
SCI_FIFO_TX3 Transmit interrupt 3/16 full.
SCI_FIFO_TX4 Transmit interrupt 4/16 full.
SCI_FIFO_TX5 Transmit interrupt 5/16 full.
SCI_FIFO_TX6 Transmit interrupt 6/16 full.
SCI_FIFO_TX7 Transmit interrupt 7/16 full.
SCI_FIFO_TX8 Transmit interrupt 8/16 full.
SCI_FIFO_TX9 Transmit interrupt 9/16 full.
SCI_FIFO_TX10 Transmit interrupt 10/16 full.
SCI_FIFO_TX11 Transmit interrupt 11/16 full.
SCI_FIFO_TX12 Transmit interrupt 12/16 full.
SCI_FIFO_TX13 Transmit interrupt 13/16 full.
SCI_FIFO_TX14 Transmit interrupt 14/16 full.
SCI_FIFO_TX15 Transmit interrupt 15/16 full.
SCI_FIFO_TX16 Transmit interrupt full.

25.2.2.3 enum **SCI_RxFIFOLevel**

Values that can be passed to SCI_setFIFOInterruptLevel() as the rxLevel parameter and returned by SCI_getFIFOInterruptLevel() and SCI_getRxFIFOStatus().

Enumerator

SCI_FIFO_RX0 Receive interrupt empty.
SCI_FIFO_RX1 Receive interrupt 1/16 full.
SCI_FIFO_RX2 Receive interrupt 2/16 full.
SCI_FIFO_RX3 Receive interrupt 3/16 full.
SCI_FIFO_RX4 Receive interrupt 4/16 full.
SCI_FIFO_RX5 Receive interrupt 5/16 full.
SCI_FIFO_RX6 Receive interrupt 6/16 full.
SCI_FIFO_RX7 Receive interrupt 7/16 full.
SCI_FIFO_RX8 Receive interrupt 8/16 full.
SCI_FIFO_RX9 Receive interrupt 9/16 full.
SCI_FIFO_RX10 Receive interrupt 10/16 full.
SCI_FIFO_RX11 Receive interrupt 11/16 full.
SCI_FIFO_RX12 Receive interrupt 12/16 full.
SCI_FIFO_RX13 Receive interrupt 13/16 full.
SCI_FIFO_RX14 Receive interrupt 14/16 full.
SCI_FIFO_RX15 Receive interrupt 15/16 full.
SCI_FIFO_RX16 Receive interrupt full.

25.2.3 Function Documentation

25.2.3.1 static void SCI_setParityMode (uint32_t *base*, **SCI_ParityType** *parity*) `[inline]`, `[static]`

Sets the type of parity.

Parameters

base	is the base address of the SCI port.
parity	specifies the type of parity to use.

Sets the type of parity to use for transmitting and expect when receiving. The *parity* parameter must be one of the following: **SCI_CONFIG_PAR_NONE**, **SCI_CONFIG_PAR_EVEN**, **SCI_CONFIG_PAR_ODD**.

Returns

None.

References SCI_CONFIG_PAR_MASK.

25.2.3.2 static **SCI_ParityType** SCI_getParityMode (uint32_t *base*) `[inline]`, `[static]`

Gets the type of parity currently being used.

Parameters

base	is the base address of the SCI port.

This function gets the type of parity used for transmitting data and expected when receiving data.

Returns

Returns the current parity settings, specified as one of the following: **SCI_CONFIG_PAR_NONE**, **SCI_CONFIG_PAR_EVEN**, **SCI_CONFIG_PAR_ODD**.

References SCI_CONFIG_PAR_MASK.

25.2.3.3 static void SCI_lockAutobaud (uint32_t *base*) [inline], [static]

Locks Autobaud.

Parameters

base	is the base address of the SCI port.

This function performs an autobaud lock for the SCI.

Returns

None.

25.2.3.4 static void SCI_setFIFOInterruptLevel (uint32_t *base*, **SCI_TxFIFOLevel** *txLevel*, **SCI_RxFIFOLevel** *rxLevel*) [inline], [static]

Sets the FIFO interrupt level at which interrupts are generated.

Parameters

base	is the base address of the SCI port.
txLevel	is the transmit FIFO interrupt level, specified as one of the following: **SCI_FIFO_TX0**, **SCI_FIFO_TX1**, **SCI_FIFO_TX2**, . . . or **SCI_FIFO_TX15**.
rxLevel	is the receive FIFO interrupt level, specified as one of the following **SCI_FIFO_RX0**, **SCI_FIFO_RX1**, **SCI_FIFO_RX2**, ... or **SCI_FIFO_RX15**.

This function sets the FIFO level at which transmit and receive interrupts are generated.

Returns

None.

25.2.3.5 static void SCI_getFIFOInterruptLevel (uint32_t *base*, **SCI_TxFIFOLevel** ∗ *txLevel*, **SCI_RxFIFOLevel** ∗ *rxLevel*) [inline], [static]

Gets the FIFO interrupt level at which interrupts are generated.

Parameters

base	is the base address of the SCI port.
txLevel	is a pointer to storage for the transmit FIFO interrupt level, returned as one of the following: **SCI_FIFO_TX0**, **SCI_FIFO_TX1**, **SCI_FIFO_TX2**, ... or **SCI_FIFO_TX15**.
rxLevel	is a pointer to storage for the receive FIFO interrupt level, returned as one of the following: **SCI_FIFO_RX0**, **SCI_FIFO_RX1**, **SCI_FIFO_RX2**, ... or **SCI_FIFO_RX15**.

This function gets the FIFO level at which transmit and receive interrupts are generated.

Returns

None.

25.2.3.6 static void SCI_getConfig (uint32_t *base,* uint32_t *lspclkHz,* uint32_t ∗ *baud,* uint32_t ∗ *config*) `[inline]`, `[static]`

Gets the current configuration of a SCI.

Parameters

base	is the base address of the SCI port.
lspclkHz	is the rate of the clock supplied to the SCI module. This is the LSPCLK.
baud	is a pointer to storage for the baud rate.
config	is a pointer to storage for the data format.

The baud rate and data format for the SCI is determined, given an explicitly provided peripheral clock (hence the ExpClk suffix). The returned baud rate is the actual baud rate; it may not be the exact baud rate requested or an “official” baud rate. The data format returned in *config* is enumerated the same as the *config* parameter of SCI_setConfig().

The peripheral clock is the low speed peripheral clock. This will be the value returned by SysCtl_getLowSeedClock(), or it can be explicitly hard coded if it is constant and known (to save the code/execution overhead of a call to SysCtl_getLowSpeedClock()).

Returns

None.

References SCI_CONFIG_PAR_MASK, SCI_CONFIG_STOP_MASK, and SCI_CONFIG_WLEN_MASK.

25.2.3.7 static void SCI_enableModule (uint32_t *base*) `[inline]`, `[static]`

Enables transmitting and receiving.

Parameters

base	is the base address of the SCI port.

Enables SCI by taking SCI out of the software reset. Sets the TXENA, and RXENA bits which enables transmit and receive.

Returns

None.

Referenced by SCI_setConfig().

25.2.3.8 static void SCI_disableModule (uint32_t *base*) [inline], [static]

Disables transmitting and receiving.

Parameters

base	is the base address of the SCI port.

Clears the SCIEN, TXE, and RXE bits. The user should ensure that all the data has been sent before disable the module during transmission.

Returns

None.

Referenced by SCI_setConfig().

25.2.3.9 static void SCI_enableFIFO (uint32_t *base*) [inline], [static]

Enables the transmit and receive FIFOs.

Parameters

base	is the base address of the SCI port.

This functions enables the transmit and receive FIFOs in the SCI.

Returns

None.

25.2.3.10 static void SCI_disableFIFO (uint32_t *base*) [inline], [static]

Disables the transmit and receive FIFOs.

Parameters

base	is the base address of the SCI port.

This functions disables the transmit and receive FIFOs in the SCI.

Returns

None.

25.2.3.11 static bool SCI_isFIFOEnabled (uint32_t *base*) [inline], [static]

Determines if the FIFO enhancement is enabled.

Parameters

base	is the base address of the SCI port.

This function returns a flag indicating whether or not the FIFO enhancement is enabled.

Returns

Returns **true** if the FIFO enhancement is enabled or **false** if the FIFO enhancement is disabled.

Referenced by SCI_isTransmitterBusy(), SCI_readCharArray(), and SCI_writeCharArray().

25.2.3.12 static void SCI_resetRxFIFO (uint32_t *base*) [inline], [static]

Resets the receive FIFO.

Parameters

base	is the base address of the SCI port.

This functions resets the receive FIFO of the SCI.

Returns

None.

25.2.3.13 static void SCI_resetTxFIFO (uint32_t *base*) [inline], [static]

Resets the transmit FIFO.

Parameters

base	is the base address of the SCI port.

This functions resets the transmit FIFO of the SCI.

Returns

None.

25.2.3.14 static void SCI_resetChannels (uint32_t *base*) [inline], [static]

Resets the SCI Transmit and Receive Channels

Parameters

base	is the base address of the SCI port.

This functions resets transmit and receive channels in the SCI.

Returns

None.

25.2.3.15 static bool SCI_isDataAvailableNonFIFO (uint32_t *base*) [inline], [static]

Determines if there are any characters in the receive buffer when the FIFO enhancement is not enabled.

Parameters

base	is the base address of the SCI port.

This function returns a flag indicating whether or not there is data available in the receive buffer.

Returns

Returns **true** if there is data in the receive buffer or **false** if there is no data in the receive buffer.

Referenced by SCI_readCharArray(), and SCI_readCharBlockingNonFIFO().

25.2.3.16 static bool SCI_isSpaceAvailableNonFIFO (uint32_t *base*) [inline], [static]

Determines if there is any space in the transmit buffer when the FIFO enhancement is not enabled.

Parameters

base	is the base address of the SCI port.

This function returns a flag indicating whether or not there is space available in the transmit buffer when not using the FIFO enhancement.

Returns

Returns **true** if there is space available in the transmit buffer or **false** if there is no space available in the transmit buffer.

Referenced by SCI_writeCharArray(), and SCI_writeCharBlockingNonFIFO().

25.2.3.17 static **SCI_TxFIFOLevel** SCI_getTxFIFOStatus (uint32_t *base*) `[inline]`, `[static]`

Get the transmit FIFO status

Parameters

base	is the base address of the SCI port.

This functions gets the current number of words in the transmit FIFO.

Returns

Returns the current number of words in the transmit FIFO specified as one of the following: **SCI_FIFO_TX0**, **SCI_FIFO_TX1**, **SCI_FIFO_TX2**, **SCI_FIFO_TX3** **SCI_FIFO_TX4**, ..., or **SCI_FIFO_TX16**

Referenced by SCI_writeCharArray(), and SCI_writeCharBlockingFIFO().

25.2.3.18 static **SCI_RxFIFOLevel** SCI_getRxFIFOStatus (uint32_t *base*) `[inline]`, `[static]`

Get the receive FIFO status

Parameters

base	is the base address of the SCI port.

This functions gets the current number of words in the receive FIFO.

Returns

Returns the current number of words in the receive FIFO specified as one of the following: **SCI_FIFO_RX0**, **SCI_FIFO_RX1**, **SCI_FIFO_RX2**, **SCI_FIFO_RX3** **SCI_FIFO_RX4**, ..., or **SCI_FIFO_RX16**

Referenced by SCI_readCharArray(), and SCI_readCharBlockingFIFO().

25.2.3.19 static bool SCI_isTransmitterBusy (uint32_t *base*) `[inline]`, `[static]`

Determines whether the SCI transmitter is busy or not.

Parameters

base	is the base address of the SCI port.

Allows the caller to determine whether all transmitted bytes have cleared the transmitter hardware when the FIFO is not enabled. When the FIFO is enabled, this function allows the caller to determine whether there is any data in the FIFO.

Without the FIFO enabled, if **false** is returned, the transmit buffer and shift registers are empty and the transmitter is not busy. With the FIFO enabled, if **false** is returned, the FIFO is empty. This does not necessarily mean that the transmitter is not busy. The empty FIFO does not reflect the status of the transmitter shift register. The FIFO may be empty while the transmitter is still transmitting data.

Returns

Returns **true** if the SCI is transmitting or **false** if transmissions are complete.

References SCI_isFIFOEnabled().

25.2.3.20 static void SCI_writeCharBlockingFIFO (uint32_t *base,* uint16_t *data*) [inline], [static]

Waits to send a character from the specified port when the FIFO enhancement is enabled.

Parameters

base	is the base address of the SCI port.
data	is the character to be transmitted.

Sends the character *data* to the transmit buffer for the specified port. If there is no space available in the transmit FIFO, this function waits until there is space available before returning. *data* is a uint16_t but only 8 bits are written to the SCI port. SCI only transmits 8 bit characters.

Returns

None.

References SCI_FIFO_TX15, and SCI_getTxFIFOStatus().

25.2.3.21 static void SCI_writeCharBlockingNonFIFO (uint32_t *base,* uint16_t *data*) [inline], [static]

Waits to send a character from the specified port.

Parameters

base	is the base address of the SCI port.
data	is the character to be transmitted.

Sends the character *data* to the transmit buffer for the specified port. If there is no space available in the transmit buffer, or the transmit FIFO if it is enabled, this function waits until there is space available before returning. *data* is a uint16_t but only 8 bits are written to the SCI port. SCI only transmits 8 bit characters.

Returns

None.

References SCI_isSpaceAvailableNonFIFO().

25.2.3.22 static void SCI_writeCharNonBlocking (uint32_t *base,* uint16_t *data*) `[inline]`, `[static]`

Sends a character to the specified port.

Parameters

base	is the base address of the SCI port.
data	is the character to be transmitted.

Writes the character *data* to the transmit buffer for the specified port. This function does not block and only writes to the transmit buffer. The user should use SCI_isSpaceAvailableNonFIFO() or SCI_getTxFIFOStatus() to determine if the transmit buffer or FIFO have space available. *data* is a uint16_t but only 8 bits are written to the SCI port. SCI only transmits 8 bit characters.

This function replaces the original SCICharNonBlockingPut() API and performs the same actions. A macro is provided in `sci.h` to map the original API to this API.

Returns

None.

25.2.3.23 static uint16_t SCI_readCharBlockingFIFO (uint32_t *base*) `[inline]`, `[static]`

Waits for a character from the specified port when the FIFO enhancement is enabled.

Parameters

base	is the base address of the SCI port.

Gets a character from the receive FIFO for the specified port. If there are no characters available, this function waits until a character is received before returning.

Returns

Returns the character read from the specified port as *uint16_t*.

References SCI_FIFO_RX0, and SCI_getRxFIFOStatus().

25.2.3.24 static uint16_t SCI_readCharBlockingNonFIFO (uint32_t *base*) `[inline]`, `[static]`

Waits for a character from the specified port when the FIFO enhancement is not enabled.

Parameters

base	is the base address of the SCI port.

Gets a character from the receive buffer for the specified port. If there is no characters available, this function waits until a character is received before returning.

Returns

Returns the character read from the specified port as *uint16_t*.

References SCI_isDataAvailableNonFIFO().

25.2.3.25 static uint16_t SCI_readCharNonBlocking (uint32_t *base*) [inline], [static]

Receives a character from the specified port.

Parameters

base	is the base address of the SCI port.

Gets a character from the receive buffer for the specified port. This function does not block and only reads the receive buffer. The user should use SCI_isDataAvailableNonFIFO() or SCI_getRxFIFOStatus() to determine if the receive buffer or FIFO have data available.

This function replaces the original SCICharNonBlockingGet() API and performs the same actions. A macro is provided in `sci.h` to map the original API to this API.

Returns

Returns *uin16_t* which is read from the receive buffer.

25.2.3.26 static uint16_t SCI_getRxStatus (uint32_t *base*) [inline], [static]

Gets current receiver status flags.

Parameters

base	is the base address of the SCI port.

This function returns the current receiver status flags. The returned error flags are equivalent to the error bits returned via the previous reading or receiving of a character with the exception that the overrun error is set immediately the overrun occurs rather than when a character is next read.

Returns

Returns a bitwise OR combination of the receiver status flags, **SCI_RXSTATUS_WAKE**, **SCI_RXSTATUS_PARITY**, **SCI_RXSTATUS_OVERRUN**, **SCI_RXSTATUS_FRAMING**, **SCI_RXSTATUS_BREAK**, **SCI_RXSTATUS_READY**, and **SCI_RXSTATUS_ERROR**.

25.2.3.27 static void SCI_performSoftwareReset (uint32_t *base*) [inline], [static]

Performs a software reset of the SCI and Clears all reported receiver status flags.

Parameters

base	is the base address of the SCI port.

This function performs a software reset of the SCI port. It affects the operating flags of the SCI, but it neither affects the configuration bits nor restores the reset values.

Returns
None.

Referenced by SCI_clearInterruptStatus().

25.2.3.28 static void SCI_enableLoopback (uint32_t *base*) [inline], [static]

Enables Loop Back Test Mode

Parameters

base	is the base address of the SCI port.

Enables the loop back test mode where the Tx pin is internally connected to the Rx pin.

Returns
None.

25.2.3.29 static void SCI_disableLoopback (uint32_t *base*) [inline], [static]

Disables Loop Back Test Mode

Parameters

base	is the base address of the SCI port.

Disables the loop back test mode where the Tx pin is no longer internally connected to the Rx pin.

Returns
None.

25.2.3.30 static bool SCI_getOverflowStatus (uint32_t *base*) [inline], [static]

Get the receive FIFO Overflow flag status

Parameters

base	is the base address of the SCI port.

This functions gets the receive FIFO overflow flag status.

Returns
Returns **true** if overflow has occurred, else returned **false** if an overflow hasn't occurred.

25.2.3.31 static void SCI_clearOverflowStatus (uint32_t *base*) [inline], [static]

Clear the receive FIFO Overflow flag status

Parameters

base	is the base address of the SCI port.

This functions clears the receive FIFO overflow flag status.

Returns

None.

25.2.3.32 void SCI_setConfig (uint32_t *base,* uint32_t *lspclkHz,* uint32_t *baud,* uint32_t *config*)

Sets the configuration of a SCI.

Parameters

base	is the base address of the SCI port.
lspclkHz	is the rate of the clock supplied to the SCI module. This is the LSPCLK.
baud	is the desired baud rate.
config	is the data format for the port (number of data bits, number of stop bits, and parity).

This function configures the SCI for operation in the specified data format. The baud rate is provided in the *baud* parameter and the data format in the *config* parameter.

The *config* parameter is the bitwise OR of three values: the number of data bits, the number of stop bits, and the parity. **SCI_CONFIG_WLEN_8**, **SCI_CONFIG_WLEN_7**, **SCI_CONFIG_WLEN_6**, **SCI_CONFIG_WLEN_5**, **SCI_CONFIG_WLEN_4**, **SCI_CONFIG_WLEN_3**, **SCI_CONFIG_WLEN_2**, and **SCI_CONFIG_WLEN_1**. Select from eight to one data bits per byte (respectively). **SCI_CONFIG_STOP_ONE** and **SCI_CONFIG_STOP_TWO** select one or two stop bits (respectively). **SCI_CONFIG_PAR_NONE**, **SCI_CONFIG_PAR_EVEN**, **SCI_CONFIG_PAR_ODD**, select the parity mode (no parity bit, even parity bit, odd parity bit respectively).

The peripheral clock is the low speed peripheral clock. This will be the value returned by SysCtl_getLowSpeedClock(), or it can be explicitly hard coded if it is constant and known (to save the code/execution overhead of a call to SysCtl_getLowSpeedClock()).

Returns

None.

References SCI_CONFIG_PAR_MASK, SCI_CONFIG_STOP_MASK, SCI_CONFIG_WLEN_MASK, SCI_disableModule(), and SCI_enableModule().

25.2.3.33 void SCI_writeCharArray (uint32_t *base,* const uint16_t ∗const *array,* uint16_t *length*)

Waits to send an array of characters from the specified port.

Parameters

base	is the base address of the SCI port.
array	is the address of the array of characters to be transmitted. It is pointer to the array of characters to be transmitted.
length	is the length of the array, or number of characters in the array to be transmitted.

Sends the number of characters specified by *length*, starting at the address *array*, out of the transmit buffer for the specified port. If there is no space available in the transmit buffer, or the transmit FIFO if it is enabled, this function waits until there is space available and *length* number of characters are transmitted before returning. *array* is a pointer to uint16_ts but only the least significant 8 bits are written to the SCI port. SCI only transmits 8 bit characters.

Returns

None.

References SCI_FIFO_TX15, SCI_getTxFIFOStatus(), SCI_isFIFOEnabled(), and SCI_isSpaceAvailableNonFIFO().

25.2.3.34 void SCI_readCharArray (uint32_t *base,* uint16_t ∗const *array,* uint16_t *length*)

Waits to receive an array of characters from the specified port.

Parameters

base	is the base address of the SCI port.
array	is the address of the array of characters to be received. It is a pointer to the array of characters to be received.
length	is the length of the array, or number of characters in the array to be received.

Receives an array of characters from the receive buffer for the specified port, and stores them as an array of characters starting at address *array*. This function waits until the *length* number of characters are received before returning.

Returns

None.

References SCI_FIFO_RX0, SCI_getRxFIFOStatus(), SCI_isDataAvailableNonFIFO(), and SCI_isFIFOEnabled().

25.2.3.35 void SCI_enableInterrupt (uint32_t *base,* uint32_t *intFlags*)

Enables individual SCI interrupt sources.

Parameters

base	is the base address of the SCI port.
intFlags	is the bit mask of the interrupt sources to be enabled.

Enables the indicated SCI interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

The *intFlags* parameter is the bitwise OR of any of the following:

- **SCI_INT_RXERR** - RXERR Interrupt
- **SCI_INT_RXRDY_BRKDT** - RXRDY/BRKDT Interrupt

- **SCI_INT_TXRDY** - TXRDY Interrupt
- **SCI_INT_TXFF** - TX FIFO Level Interrupt
- **SCI_INT_RXFF** - RX FIFO Level Interrupt
- **SCI_INT_FE** - Frame Error
- **SCI_INT_OE** - Overrun Error
- **SCI_INT_PE** - Parity Error

Returns

None.

References SCI_INT_RXERR, SCI_INT_RXFF, SCI_INT_RXRDY_BRKDT, SCI_INT_TXFF, and SCI_INT_TXRDY.

25.2.3.36 void SCI_disableInterrupt (uint32_t *base,* uint32_t *intFlags*)

Disables individual SCI interrupt sources.

Parameters

base	is the base address of the SCI port.
intFlags	is the bit mask of the interrupt sources to be disabled.

Disables the indicated SCI interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

The *intFlags* parameter has the same definition as the *intFlags* parameter to SCI_enableInterrupt().

Returns

None.

References SCI_INT_RXERR, SCI_INT_RXFF, SCI_INT_RXRDY_BRKDT, SCI_INT_TXFF, and SCI_INT_TXRDY.

25.2.3.37 uint32_t SCI_getInterruptStatus (uint32_t *base*)

Gets the current interrupt status.

Parameters

base	is the base address of the SCI port.

Returns

Returns the current interrupt status, enumerated as a bit field of values described in SCI_enableInterrupt().

References SCI_INT_FE, SCI_INT_OE, SCI_INT_PE, SCI_INT_RXERR, SCI_INT_RXFF, SCI_INT_RXRDY_BRKDT, SCI_INT_TXFF, and SCI_INT_TXRDY.

25.2.3.38 void SCI_clearInterruptStatus (uint32_t *base,* uint32_t *intFlags*)

Clears SCI interrupt sources.

Parameters

base	is the base address of the SCI port.
intFlags	is a bit mask of the interrupt sources to be cleared.

The specified SCI interrupt sources are cleared, so that they no longer assert. This function must be called in the interrupt handler to keep the interrupt from being recognized again immediately upon exit.

The *intFlags* parameter has the same definition as the *intFlags* parameter to SCI_enableInterrupt().

Returns

None.

References SCI_INT_FE, SCI_INT_OE, SCI_INT_PE, SCI_INT_RXERR, SCI_INT_RXFF, SCI_INT_RXRDY_BRKDT, SCI_INT_TXFF, and SCI_performSoftwareReset().

26 SDFM Module

26.1 SDFM Introduction

The Sigma-Delta Filter Module (SDFM) API provides a set of functions for configuring and using the SDFM module. The functions provided allow the user to setup and configure the Input data type to SDFM filters, the Primary (data) and Secondary (comparator) filters, Data FIFO, the PWM - SDFM sync signals, comparator threshold values and interrupt sources. Functions are also provided to read the filter data and the status of the SDFM module components.

Note that the Secondary (comparator) Filter configuration APIs have the "Comp" key word embedded to represent access to the Comparator sub-module. For example the function SDFM_setComparatorFilterType() sets the comparator filter type while SDFM_setFilterType() sets the primary filter type.

APIs providing higher level abstraction are also available in the sdfm.c source file. These APIs can be used to configure the Comparator, Data Filter and the Data filter FIFO.

26.2 API Functions

Macros

- #define SDFM_GET_LOW_THRESHOLD(C)
- #define SDFM_GET_HIGH_THRESHOLD(C)
- #define SDFM_SET_OSR(X)
- #define SDFM_SHIFT_VALUE(X)
- #define SDFM_THRESHOLD(H, L)
- #define SDFM_SET_FIFO_LEVEL(X)
- #define SDFM_SET_ZERO_CROSS_THRESH_VALUE(X)
- #define SDFM_FILTER_DISABLE
- #define SDFM_MODULATOR_FAILURE_INTERRUPT
- #define SDFM_LOW_LEVEL_THRESHOLD_INTERRUPT
- #define SDFM_HIGH_LEVEL_THRESHOLD_INTERRUPT
- #define SDFM_DATA_FILTER_ACKNOWLEDGE_INTERRUPT
- #define SDFM_MASTER_INTERRUPT_FLAG
- #define SDFM_FILTER_1_HIGH_THRESHOLD_FLAG
- #define SDFM_FILTER_1_LOW_THRESHOLD_FLAG
- #define SDFM_FILTER_2_HIGH_THRESHOLD_FLAG
- #define SDFM_FILTER_2_LOW_THRESHOLD_FLAG
- #define SDFM_FILTER_3_HIGH_THRESHOLD_FLAG
- #define SDFM_FILTER_3_LOW_THRESHOLD_FLAG
- #define SDFM_FILTER_4_HIGH_THRESHOLD_FLAG
- #define SDFM_FILTER_4_LOW_THRESHOLD_FLAG
- #define SDFM_FILTER_1_MOD_FAILED_FLAG
- #define SDFM_FILTER_2_MOD_FAILED_FLAG
- #define SDFM_FILTER_3_MOD_FAILED_FLAG
- #define SDFM_FILTER_4_MOD_FAILED_FLAG

- #define SDFM_FILTER_1_NEW_DATA_FLAG
- #define SDFM_FILTER_2_NEW_DATA_FLAG
- #define SDFM_FILTER_3_NEW_DATA_FLAG
- #define SDFM_FILTER_4_NEW_DATA_FLAG

Enumerations

- enum SDFM_OutputThresholdStatus { SDFM_OUTPUT_WITHIN_THRESHOLD, SDFM_OUTPUT_ABOVE_THRESHOLD, SDFM_OUTPUT_BELOW_THRESHOLD }
- enum SDFM_FilterNumber { SDFM_FILTER_1, SDFM_FILTER_2, SDFM_FILTER_3, SDFM_FILTER_4 }
- enum SDFM_FilterType { SDFM_FILTER_SINC_FAST, SDFM_FILTER_SINC_1, SDFM_FILTER_SINC_2, SDFM_FILTER_SINC_3 }
- enum SDFM_ModulatorClockMode { SDFM_MODULATOR_CLK_EQUAL_DATA_RATE, SDFM_MODULATOR_CLK_HALF_DATA_RATE, SDFM_MODULATOR_CLK_OFF, SDFM_MODULATOR_CLK_DOUBLE_DATA_RATE }
- enum SDFM_OutputDataFormat { SDFM_DATA_FORMAT_16_BIT, SDFM_DATA_FORMAT_32_BIT }

Functions

- static void SDFM_enableExternalReset (uint32_t base, SDFM_FilterNumber filterNumber)
- static void SDFM_disableExternalReset (uint32_t base, SDFM_FilterNumber filterNumber)
- static void SDFM_enableFilter (uint32_t base, SDFM_FilterNumber filterNumber)
- static void SDFM_disableFilter (uint32_t base, SDFM_FilterNumber filterNumber)
- static void SDFM_setFilterType (uint32_t base, SDFM_FilterNumber filterNumber, SDFM_FilterType filterType)
- static void SDFM_setFilterOverSamplingRatio (uint32_t base, SDFM_FilterNumber filterNumber, uint16_t overSamplingRatio)
- static void SDFM_setupModulatorClock (uint32_t base, SDFM_FilterNumber filterNumber, SDFM_ModulatorClockMode clockMode)
- static void SDFM_setOutputDataFormat (uint32_t base, SDFM_FilterNumber filterNumber, SDFM_OutputDataFormat dataFormat)
- static void SDFM_setDataShiftValue (uint32_t base, SDFM_FilterNumber filterNumber, uint16_t shiftValue)
- static void SDFM_setCompFilterHighThreshold (uint32_t base, SDFM_FilterNumber filterNumber, uint16_t highThreshold)
- static void SDFM_setCompFilterLowThreshold (uint32_t base, SDFM_FilterNumber filterNumber, uint16_t lowThreshold)
- static void SDFM_enableInterrupt (uint32_t base, SDFM_FilterNumber filterNumber, uint16_t intFlags)
- static void SDFM_disableInterrupt (uint32_t base, SDFM_FilterNumber filterNumber, uint16_t intFlags)
- static void SDFM_setComparatorFilterType (uint32_t base, SDFM_FilterNumber filterNumber, SDFM_FilterType filterType)
- static void SDFM_setCompFilterOverSamplingRatio (uint32_t base, SDFM_FilterNumber filterNumber, uint16_t overSamplingRatio)
- static uint32_t SDFM_getFilterData (uint32_t base, SDFM_FilterNumber filterNumber)
- static SDFM_OutputThresholdStatus SDFM_getThresholdStatus (uint32_t base, SDFM_FilterNumber filterNumber)
- static bool SDFM_getModulatorStatus (uint32_t base, SDFM_FilterNumber filterNumber)
- static bool SDFM_getNewFilterDataStatus (uint32_t base, SDFM_FilterNumber filterNumber)

- static bool SDFM_getIsrStatus (uint32_t base)
- static void SDFM_clearInterruptFlag (uint32_t base, uint32_t flag)
- static void SDFM_enableMasterInterrupt (uint32_t base)
- static void SDFM_disableMasterInterrupt (uint32_t base)
- static void SDFM_enableMasterFilter (uint32_t base)
- static void SDFM_disableMasterFilter (uint32_t base)
- void SDFM_configComparator (uint32_t base, uint16_t config1, uint32_t config2)
- void SDFM_configDataFilter (uint32_t base, uint16_t config1, uint16_t config2)

26.2.1 Detailed Description

The code for this module is contained in `driverlib/sdfm.c`, with `driverlib/sdfm.h` containing the API declarations for use by applications.

26.2.2 Macro Definition Documentation

26.2.2.1 #define SDFM_GET_LOW_THRESHOLD(*C*)

Macro to get the low threshold

Referenced by SDFM_configComparator().

26.2.2.2 #define SDFM_GET_HIGH_THRESHOLD(*C*)

Macro to get the high threshold

Referenced by SDFM_configComparator().

26.2.2.3 #define SDFM_SET_OSR(*X*)

Macro to convert comparator over sampling ratio to acceptable bit location

26.2.2.4 #define SDFM_SHIFT_VALUE(*X*)

Macro to convert the data shift bit values to acceptable bit location

26.2.2.5 #define SDFM_THRESHOLD(*H*, *L*)

Macro to combine high threshold and low threshold values

26.2.2.6 #define SDFM_SET_FIFO_LEVEL(*X*)

Macro to set the FIFO level to acceptable bit location

26.2.2.7 #define SDFM_SET_ZERO_CROSS_THRESH_VALUE(*X*)

Macro to set and enable the zero cross threshold value.

26.2.2.8 #define SDFM_FILTER_DISABLE

Macros to enable or disable filter.

26.2.2.9 #define SDFM_MODULATOR_FAILURE_INTERRUPT

Interrupt is generated if Modulator fails.

Referenced by SDFM_disableInterrupt(), and SDFM_enableInterrupt().

26.2.2.10 #define SDFM_LOW_LEVEL_THRESHOLD_INTERRUPT

Interrupt on Comparator low-level threshold.

Referenced by SDFM_disableInterrupt(), and SDFM_enableInterrupt().

26.2.2.11 #define SDFM_HIGH_LEVEL_THRESHOLD_INTERRUPT

Interrupt on Comparator high-level threshold.

Referenced by SDFM_disableInterrupt(), and SDFM_enableInterrupt().

26.2.2.12 #define SDFM_DATA_FILTER_ACKNOWLEDGE_INTERRUPT

Interrupt on Acknowledge flag

Referenced by SDFM_disableInterrupt(), and SDFM_enableInterrupt().

26.2.2.13 #define SDFM_MASTER_INTERRUPT_FLAG

Master interrupt flag

26.2.2.14 #define SDFM_FILTER_1_HIGH_THRESHOLD_FLAG

Filter 1 high -level threshold flag

26.2.2.15 #define SDFM_FILTER_1_LOW_THRESHOLD_FLAG

Filter 1 low -level threshold flag

26.2.2.16 #define SDFM_FILTER_2_HIGH_THRESHOLD_FLAG

Filter 2 high -level threshold flag

26.2.2.17 #define SDFM_FILTER_2_LOW_THRESHOLD_FLAG

Filter 2 low -level threshold flag

26.2.2.18 #define SDFM_FILTER_3_HIGH_THRESHOLD_FLAG

Filter 3 high -level threshold flag

26.2.2.19 #define SDFM_FILTER_3_LOW_THRESHOLD_FLAG

Filter 3 low -level threshold flag

26.2.2.20 #define SDFM_FILTER_4_HIGH_THRESHOLD_FLAG

Filter 4 high -level threshold flag

26.2.2.21 #define SDFM_FILTER_4_LOW_THRESHOLD_FLAG

Filter 4 low -level threshold flag

26.2.2.22 #define SDFM_FILTER_1_MOD_FAILED_FLAG

Filter 1 modulator failed flag

26.2.2.23 #define SDFM_FILTER_2_MOD_FAILED_FLAG

Filter 2 modulator failed flag

26.2.2.24 #define SDFM_FILTER_3_MOD_FAILED_FLAG

Filter 3 modulator failed flag

26.2.2.25 #define SDFM_FILTER_4_MOD_FAILED_FLAG

Filter 4 modulator failed flag

26.2.2.26 #define SDFM_FILTER_1_NEW_DATA_FLAG

Filter 1 new data flag

26.2.2.27 #define SDFM_FILTER_2_NEW_DATA_FLAG

Filter 2 new data flag

26.2.2.28 #define SDFM_FILTER_3_NEW_DATA_FLAG

Filter 3 new data flag

26.2.2.29 #define SDFM_FILTER_4_NEW_DATA_FLAG

Filter 4 new data flag

26.2.3 Enumeration Type Documentation

26.2.3.1 enum **SDFM_OutputThresholdStatus**

Values that can be returned from SDFM_getThresholdStatus()

Enumerator

SDFM_OUTPUT_WITHIN_THRESHOLD SDFM output is within threshold.
SDFM_OUTPUT_ABOVE_THRESHOLD SDFM output is above threshold.
SDFM_OUTPUT_BELOW_THRESHOLD SDFM output is below threshold.

26.2.3.2 enum **SDFM_FilterNumber**

Values that can be passed to all functions as the *filterNumber* parameter.

Enumerator

SDFM_FILTER_1 Digital filter 1.
SDFM_FILTER_2 Digital filter 2.
SDFM_FILTER_3 Digital filter 3.
SDFM_FILTER_4 Digital filter 4.

26.2.3.3 enum **SDFM_FilterType**

Values that can be passed to SDFM_setFilterType(), SDFM_setComparatorFilterType() as the *filterType* parameter.

Enumerator

SDFM_FILTER_SINC_FAST Digital filter with SincFast structure.

SDFM_FILTER_SINC_1 Digital filter with Sinc1 structure.
SDFM_FILTER_SINC_2 Digital filter with Sinc3 structure.
SDFM_FILTER_SINC_3 Digital filter with Sinc4 structure.

26.2.3.4 enum **SDFM_ModulatorClockMode**

Values that can be passed to SDFM_setupModulatorClock(), as the *clockMode* parameter.

Enumerator

SDFM_MODULATOR_CLK_EQUAL_DATA_RATE Modulator clock is identical to the data rate.
SDFM_MODULATOR_CLK_HALF_DATA_RATE Modulator clock is half the data rate.
SDFM_MODULATOR_CLK_OFF Modulator clock is off. Data is Manchester coded.
SDFM_MODULATOR_CLK_DOUBLE_DATA_RATE Modulator clock is double the data rate.

26.2.3.5 enum **SDFM_OutputDataFormat**

Values that can be passed to SDFM_setOutputDataFormat(), as the *dataFormat* parameter.

Enumerator

SDFM_DATA_FORMAT_16_BIT Filter output is in 16 bits 2's complement format.
SDFM_DATA_FORMAT_32_BIT Filter output is in 32 bits 2's complement format.

26.2.4 Function Documentation

26.2.4.1 static void SDFM_enableExternalReset (uint32_t *base*, **SDFM_FilterNumber** *filterNumber*) [inline], [static]

Enable external reset

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.

This function enables data filter to be reset by an external source (PWM compare output).

Returns

None.

26.2.4.2 static void SDFM_disableExternalReset (uint32_t *base*, **SDFM_FilterNumber** *filterNumber*) [inline], [static]

Disable external reset

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.

This function disables data filter from being reset by an external source (PWM compare output).

Returns
None.

26.2.4.3 static void SDFM_enableFilter (uint32_t *base*, **SDFM_FilterNumber** *filterNumber*) [inline], [static]

Enable filter

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.

This function enables the filter specified by the *filterNumber* variable.

Returns
None.

Referenced by SDFM_configDataFilter().

26.2.4.4 static void SDFM_disableFilter (uint32_t *base*, **SDFM_FilterNumber** *filterNumber*) [inline], [static]

Disable filter

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.

This function disables the filter specified by the *filterNumber* variable.

Returns
None.

Referenced by SDFM_configDataFilter().

26.2.4.5 static void SDFM_setFilterType (uint32_t *base*, **SDFM_FilterNumber** *filterNumber*, **SDFM_FilterType** *filterType*) [inline], [static]

Set filter type.

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.
filterType	is the filter type or structure.

This function sets the filter type or structure to be used as specified by filterType for the selected filter number as specified by filterNumber.

Returns

None.

Referenced by SDFM_configDataFilter().

26.2.4.6 static void SDFM_setFilterOverSamplingRatio (uint32_t *base*, **SDFM_FilterNumber** *filterNumber*, uint16_t *overSamplingRatio*) [inline], [static]

Set data filter over sampling ratio.

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.
overSamplingRatio	is the data filter over sampling ratio.

This function sets the filter oversampling ratio for the filter specified by the filterNumber variable.Valid values for the variable overSamplingRatio are 0 to 255 inclusive. The actual oversampling ratio will be this value plus one.

Returns

None.

Referenced by SDFM_configDataFilter().

26.2.4.7 static void SDFM_setupModulatorClock (uint32_t *base*, **SDFM_FilterNumber** *filterNumber*, **SDFM_ModulatorClockMode** *clockMode*) [inline], [static]

Set modulator clock mode.

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.
clockMode	is the modulator clock mode.

This function sets the modulator clock mode specified by clockMode for the filter specified by filterNumber.

Returns

None.

26.2.4.8 static void SDFM_setOutputDataFormat (uint32_t *base*, **SDFM_FilterNumber** *filterNumber*, **SDFM_OutputDataFormat** *dataFormat*) [inline], [static]

Set the output data format

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.
dataFormat	is the output data format.

This function sets the output data format for the filter specified by filterNumber.

Returns

None.

Referenced by SDFM_configDataFilter().

26.2.4.9 static void SDFM_setDataShiftValue (uint32_t *base*, **SDFM_FilterNumber** *filterNumber*, uint16_t *shiftValue*) [inline], [static]

Set data shift value.

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.
shiftValue	is the data shift value.

This function sets the shift value for the 16 bit 2's complement data format. The valid maximum value for shiftValue is 31.

Note: Use this function with 16 bit 2's complement data format only.

Returns

None.

Referenced by SDFM_configDataFilter().

26.2.4.10 static void SDFM_setCompFilterHighThreshold (uint32_t *base*, **SDFM_FilterNumber** *filterNumber*, uint16_t *highThreshold*) [inline], [static]

Set Filter output high-level threshold.

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.
highThreshold	is the high-level threshold.

This function sets the unsigned high-level threshold value for the Comparator filter output. If the output value of the filter exceeds highThreshold and interrupt generation is enabled, an interrupt will be issued.

Returns

None.

Referenced by SDFM_configComparator().

26.2.4.11 static void SDFM_setCompFilterLowThreshold (uint32_t *base*, **SDFM_FilterNumber** *filterNumber*, uint16_t *lowThreshold*) `[inline]`, `[static]`

Set Filter output low-level threshold.

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.
lowThreshold	is the low-level threshold.

This function sets the unsigned low-level threshold value for the Comparator filter output. If the output value of the filter gets below lowThreshold and interrupt generation is enabled, an interrupt will be issued.

Returns

None.

Referenced by SDFM_configComparator().

26.2.4.12 static void SDFM_enableInterrupt (uint32_t *base*, **SDFM_FilterNumber** *filterNumber*, uint16_t *intFlags*) [inline], [static]

Enable SDFM interrupts.

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.
intFlags	is the interrupt source.

This function enables the low threshold , high threshold or modulator failure interrupt as determined by intFlags for the filter specified by filterNumber. Valid values for intFlags are:
SDFM_MODULATOR_FAILURE_INTERRUPT ,
SDFM_LOW_LEVEL_THRESHOLD_INTERRUPT,
SDFM_HIGH_LEVEL_THRESHOLD_INTERRUPT,
SDFM_DATA_FILTER_ACKNOWLEDGE_INTERRUPT

Returns

None.

References SDFM_DATA_FILTER_ACKNOWLEDGE_INTERRUPT, SDFM_HIGH_LEVEL_THRESHOLD_INTERRUPT, SDFM_LOW_LEVEL_THRESHOLD_INTERRUPT, and SDFM_MODULATOR_FAILURE_INTERRUPT.

26.2.4.13 static void SDFM_disableInterrupt (uint32_t *base*, **SDFM_FilterNumber** *filterNumber*, uint16_t *intFlags*) [inline], [static]

Disable SDFM interrupts.

Parameters

base	is the base address of the SDFM module

filterNumber	is the filter number.
intFlags	is the interrupt source.

This function disables the low threshold , high threshold or modulator failure interrupt as determined by intFlags for the filter specified by filterNumber. Valid values for intFlags are:
SDFM_MODULATOR_FAILURE_INTERRUPT ,
SDFM_LOW_LEVEL_THRESHOLD_INTERRUPT,
SDFM_HIGH_LEVEL_THRESHOLD_INTERRUPT,
SDFM_DATA_FILTER_ACKNOWLEDGE_INTERRUPT

Returns

None.

References SDFM_DATA_FILTER_ACKNOWLEDGE_INTERRUPT, SDFM_HIGH_LEVEL_THRESHOLD_INTERRUPT, SDFM_LOW_LEVEL_THRESHOLD_INTERRUPT, and SDFM_MODULATOR_FAILURE_INTERRUPT.

26.2.4.14 static void SDFM_setComparatorFilterType (uint32_t *base*, **SDFM_FilterNumber** *filterNumber*, **SDFM_FilterType** *filterType*) [inline], [static]

Set the comparator filter type.

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.
filterType	is the comparator filter type or structure.

This function sets the Comparator filter type or structure to be used as specified by filterType for the selected filter number as specified by filterNumber.

Returns

None.

Referenced by SDFM_configComparator().

26.2.4.15 static void SDFM_setCompFilterOverSamplingRatio (uint32_t *base*, **SDFM_FilterNumber** *filterNumber*, uint16_t *overSamplingRatio*) [inline], [static]

Set Comparator filter over sampling ratio.

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.

overSamplingRatio	is the comparator filter over sampling ration.

This function sets the comparator filter oversampling ratio for the filter specified by the filterNumber.Valid values for the variable overSamplingRatio are 0 to 31 inclusive. The actual oversampling ratio will be this value plus one.

Returns
None.

Referenced by SDFM_configComparator().

26.2.4.16 static uint32_t SDFM_getFilterData (uint32_t *base,* **SDFM_FilterNumber** *filterNumber*) [inline], [static]

Get the filter data output.

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.

This function returns the latest data filter output. Depending on the filter data output format selected, the valid value will be the lower 16 bits or the whole 32 bits of the returned value.

Returns
Returns the latest data filter output.

26.2.4.17 static **SDFM_OutputThresholdStatus** SDFM_getThresholdStatus (uint32_t *base,* **SDFM_FilterNumber** *filterNumber*) [inline], [static]

Get the Comparator threshold status.

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.

This function returns the Comparator output threshold status for the given filterNumber.

Returns
Returns the following status flags.
- **SDFM_OUTPUT_WITHIN_THRESHOLD** if the output is within the specified threshold.
- **SDFM_OUTPUT_ABOVE_THRESHOLD** if the output is above the high threshold
- **SDFM_OUTPUT_BELOW_THRESHOLD** if the output is below the low threshold.

26.2.4.18 static bool SDFM_getModulatorStatus (uint32_t *base,* **SDFM_FilterNumber** *filterNumber*) [inline], [static]

Get the Modulator status.

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.

This function returns the Modulator status.

Returns

Returns true if the Modulator is operating normally Returns false if the Modulator has failed

26.2.4.19 static bool SDFM_getNewFilterDataStatus (uint32_t *base,* **SDFM_FilterNumber** *filterNumber*) [inline], [static]

Check if new Filter data is available.

Parameters

base	is the base address of the SDFM module
filterNumber	is the filter number.

This function returns new filter data status.

Returns

Returns **true** if new filter data is available Returns **false** if no new filter data is available

26.2.4.20 static bool SDFM_getIsrStatus (uint32_t *base*) [inline], [static]

Get pending interrupt.

Parameters

base	is the base address of the SDFM module

This function returns any pending interrupt status.

Returns

Returns **true** if there is a pending interrupt. Returns **false** if no interrupt is pending.

26.2.4.21 static void SDFM_clearInterruptFlag (uint32_t *base,* uint32_t *flag*) [inline], [static]

Clear pending flags.

Parameters

base	is the base address of the SDFM module
flag	is the SDFM status

This function clears the specified pending interrupt flag. Valid values are SDFM_MASTER_INTERRUPT_FLAG, SDFM_FILTER_1_NEW_DATA_FLAG, SDFM_FILTER_2_NEW_DATA_FLAG, SDFM_FILTER_3_NEW_DATA_FLAG, SDFM_FILTER_4_NEW_DATA_FLAG, SDFM_FILTER_1_MOD_FAILED_FLAG, SDFM_FILTER_2_MOD_FAILED_FLAG, SDFM_FILTER_3_MOD_FAILED_FLAG, SDFM_FILTER_4_MOD_FAILED_FLAG, SDFM_FILTER_1_HIGH_THRESHOLD_FLAG,

SDFM_FILTER_1_LOW_THRESHOLD_FLAG, SDFM_FILTER_2_HIGH_THRESHOLD_FLAG, SDFM_FILTER_2_LOW_THRESHOLD_FLAG, SDFM_FILTER_3_HIGH_THRESHOLD_FLAG, SDFM_FILTER_3_LOW_THRESHOLD_FLAG, SDFM_FILTER_4_HIGH_THRESHOLD_FLAG, SDFM_FILTER_4_LOW_THRESHOLD_FLAG or any combination of the above flags.

Returns
None

26.2.4.22 static void SDFM_enableMasterInterrupt (uint32_t *base*) `[inline]`, `[static]`

Enable master interrupt.

Parameters

base	is the base address of the SDFM module

This function enables the master SDFM interrupt.

Returns
None

26.2.4.23 static void SDFM_disableMasterInterrupt (uint32_t *base*) `[inline]`, `[static]`

Disable master interrupt.

Parameters

base	is the base address of the SDFM module

This function disables the master SDFM interrupt.

Returns
None

26.2.4.24 static void SDFM_enableMasterFilter (uint32_t *base*) `[inline]`, `[static]`

Enable master filter.

Parameters

base	is the base address of the SDFM module

This function enables master filter.

Returns
None

26.2.4.25 static void SDFM_disableMasterFilter (uint32_t *base*) `[inline]`, `[static]`

Disable master filter.

Parameters

base	is the base address of the SDFM module

This function disables master filter.

Returns

None

26.2.4.26 void SDFM_configComparator (uint32_t *base,* uint16_t *config1,* uint32_t *config2*)

Configures SDFM comparator for filter config & threshold values

Parameters

base	is the base address of the SDFM module
config1	is the filter number, filter type and over sampling ratio.
config2	is high-level and low-level threshold values.

This function configures the comparator filter for filter config and threshold values based on provided inputs.

The config1 parameter is the logical OR of the filter number, filter type and oversampling ratio. The bit definitions for config1 are as follow:

- config1.[3:0] filter number
- config1.[7:4] filter type
- config1.[15:8] Over sampling Ratio Valid values for filter number and filter type are defined in SDFM_FilterNumber and SDFM_FilterType enumerations respectively. SDFM_SET_OSR(X) macro can be used to set the value of the oversampling ratio , which ranges [1, 32] inclusive, in the appropriate bit location. For example the value (SDFM_FILTER_1 | SDFM_FILTER_SINC_2 | SDFM_SET_OSR(16)) will select Filter 1, SINC 2 type with an oversampling ratio of 16.

The config2 parameter is the logical OR of the filter high and low threshold values. The bit definitions for config2 are as follow:

- config2.[15:0] low threshold
- config2.[31:16] high threshold The upper 16 bits define the high threshold and the lower 16 bits define the low threshold. SDFM_THRESHOLD(H, L) can be used to combine the high and low thresholds.

Returns

None.

References SDFM_GET_HIGH_THRESHOLD, SDFM_GET_LOW_THRESHOLD, SDFM_setComparatorFilterType(), SDFM_setCompFilterHighThreshold(), SDFM_setCompFilterLowThreshold(), and SDFM_setCompFilterOverSamplingRatio().

26.2.4.27 void SDFM_configDataFilter (uint32_t *base,* uint16_t *config1,* uint16_t *config2*)

Configure SDFM data filter

Parameters

base	is the base address of the SDFM module
config1	is the filter number, filter type and over sampling ratio configuration.
config2	is filter switch, data representation and data shift values configuration.

This function configures the data filter based on configurations config1 and config2.

The config1 parameter is the logical OR of the filter number, filter type and oversampling ratio. The bit definitions for config1 are as follow:

- config1.[3:0] Filter number
- config1.[7:4] Filter type
- config1.[15:8] Over sampling Ratio Valid values for filter number and filter type are defined in SDFM_FilterNumber and SDFM_FilterType enumerations respectively. SDFM_SET_OSR(X) macro can be used to set the value of the oversampling ratio , which ranges [1, 256] inclusive , in the appropriate bit location for config1. For example the value (SDFM_FILTER_2 | SDFM_FILTER_SINC_3 | SDFM_SET_OSR(64)) will select Filter 2 , SINC 3 type with an oversampling ratio of 64.

The config2 parameter is the logical OR of data representation, filter switch, and data shift values The bit definitions for config2 are as follow:

- config2.[0] Data representation
- config2.[1] Filter switch
- config2.[15:2] Shift values Valid values for data representation are given in SDFM_OutputDataFormat enumeration. SDFM_FILTER_DISABLE or SDFM_FILTER_ENABLE will define the filter switch values.SDFM_SHIFT_VALUE(X) macro can be used to set the value of the data shift value, which ranges [0, 31] inclusive, in the appropriate bit location for config2. The shift value is valid only in SDFM_DATA_FORMAT_16_BIT data representation format.

Returns

None.

References SDFM_DATA_FORMAT_16_BIT, SDFM_disableFilter(), SDFM_enableFilter(), SDFM_setDataShiftValue(), SDFM_setFilterOverSamplingRatio(), SDFM_setFilterType(), and SDFM_setOutputDataFormat().

27 SPI Module

27.1 SPI Introduction

The serial peripheral interface (SPI) API provides a set of functions to configure the device's SPI module. Functions are provided to initialize the module, to send and receive data, to obtain status information, and to manage interrupts. Both master and slave modes are supported.

27.2 API Functions

Enumerations

- enum SPI_TransferProtocol { SPI_PROT_POL0PHA0, SPI_PROT_POL0PHA1, SPI_PROT_POL1PHA0, SPI_PROT_POL1PHA1 }
- enum SPI_Mode { SPI_MODE_SLAVE, SPI_MODE_MASTER, SPI_MODE_SLAVE_OD, SPI_MODE_MASTER_OD }
- enum SPI_TxFIFOLevel { SPI_FIFO_TXEMPTY, SPI_FIFO_TX0, SPI_FIFO_TX1, SPI_FIFO_TX2, SPI_FIFO_TX3, SPI_FIFO_TX4, SPI_FIFO_TX5, SPI_FIFO_TX6, SPI_FIFO_TX7, SPI_FIFO_TX8, SPI_FIFO_TX9, SPI_FIFO_TX10, SPI_FIFO_TX11, SPI_FIFO_TX12, SPI_FIFO_TX13, SPI_FIFO_TX14, SPI_FIFO_TX15, SPI_FIFO_TX16, SPI_FIFO_TXFULL }
- enum SPI_RxFIFOLevel { SPI_FIFO_RXEMPTY, SPI_FIFO_RX0, SPI_FIFO_RX1, SPI_FIFO_RX2, SPI_FIFO_RX3, SPI_FIFO_RX4, SPI_FIFO_RX5, SPI_FIFO_RX6, SPI_FIFO_RX7, SPI_FIFO_RX8, SPI_FIFO_RX9, SPI_FIFO_RX10, SPI_FIFO_RX11, SPI_FIFO_RX12, SPI_FIFO_RX13, SPI_FIFO_RX14, SPI_FIFO_RX15, SPI_FIFO_RX16, SPI_FIFO_RXFULL, SPI_FIFO_RXDEFAULT }
- enum SPI_EmulationMode { SPI_EMULATION_STOP_MIDWAY, SPI_EMULATION_FREE_RUN, SPI_EMULATION_STOP_AFTER_TRANSMIT }
- enum SPI_STEPolarity { SPI_STE_ACTIVE_LOW, SPI_STE_ACTIVE_HIGH }

Functions

- static void SPI_enableModule (uint32_t base)
- static void SPI_disableModule (uint32_t base)
- static void SPI_enableFIFO (uint32_t base)
- static void SPI_disableFIFO (uint32_t base)
- static void SPI_resetTxFIFO (uint32_t base)
- static void SPI_resetRxFIFO (uint32_t base)
- static void SPI_setFIFOInterruptLevel (uint32_t base, SPI_TxFIFOLevel txLevel, SPI_RxFIFOLevel rxLevel)
- static void SPI_getFIFOInterruptLevel (uint32_t base, SPI_TxFIFOLevel ∗txLevel, SPI_RxFIFOLevel ∗rxLevel)

- static SPI_TxFIFOLevel SPI_getTxFIFOStatus (uint32_t base)
- static SPI_RxFIFOLevel SPI_getRxFIFOStatus (uint32_t base)
- static bool SPI_isBusy (uint32_t base)
- static void SPI_writeDataNonBlocking (uint32_t base, uint16_t data)
- static uint16_t SPI_readDataNonBlocking (uint32_t base)
- static void SPI_writeDataBlockingFIFO (uint32_t base, uint16_t data)
- static uint16_t SPI_readDataBlockingFIFO (uint32_t base)
- static void SPI_writeDataBlockingNonFIFO (uint32_t base, uint16_t data)
- static uint16_t SPI_readDataBlockingNonFIFO (uint32_t base)
- static void SPI_enableTriWire (uint32_t base)
- static void SPI_disableTriWire (uint32_t base)
- static void SPI_enableLoopback (uint32_t base)
- static void SPI_disableLoopback (uint32_t base)
- static void SPI_setSTESignalPolarity (uint32_t base, SPI_STEPolarity polarity)
- static void SPI_enableHighSpeedMode (uint32_t base)
- static void SPI_disableHighSpeedMode (uint32_t base)
- static void SPI_setEmulationMode (uint32_t base, SPI_EmulationMode mode)
- static void SPI_setTxFifoTransmitDelay (uint32_t base, uint16_t delay)
- static uint16_t SPI_readRxEmulationBuffer (uint32_t base)
- static void SPI_enableTalk (uint32_t base)
- static void SPI_disableTalk (uint32_t base)
- void SPI_setConfig (uint32_t base, uint32_t lspclkHz, SPI_TransferProtocol protocol, SPI_Mode mode, uint32_t bitRate, uint16_t dataWidth)
- void SPI_setBaudRate (uint32_t base, uint32_t lspclkHz, uint32_t bitRate)
- void SPI_enableInterrupt (uint32_t base, uint32_t intFlags)
- void SPI_disableInterrupt (uint32_t base, uint32_t intFlags)
- uint32_t SPI_getInterruptStatus (uint32_t base)
- void SPI_clearInterruptStatus (uint32_t base, uint32_t intFlags)

27.2.1 Detailed Description

This module is used for SPI configurations. Before initializing the SPI module, the user first must put the module into the reset state by calling SPI_disableModule(). The next call should be to SPI_setConfig() to set properties like master or slave mode, bit rate of the SPI clock signal, data width, and the number of bits per frame.

The next step is to do any any FIFO or interrupt configuration. FIFOs are configured using SPI_enableFIFO() and SPI_disableFIFO() and SPI_setFIFOInterruptLevel() if interrupts are desired. The functions SPI_enableInterrupt(), SPI_disableInterrupt(), SPI_clearInterruptStatus(), and SPI_getInterruptStatus() are for management of interrupts. Note that the SPI module uses separate interrupt lines for its receive and transmit interrupts when in FIFO mode, but only the "receive" interrupt line when not in FIFO mode.

When configuration is complete, SPI_enableModule() should be called to enable the operation of the module.

To transmit data, there are a few options. SPI_writeDataNonBlocking() will simply write the specified data to the transmit buffer and return. It is left up to the user to check beforehand that the module is ready for a new piece of data to be written to the buffer. This means checking the buffer-full flag is not set or, if in FIFO mode, checking how full the FIFO is using SPI_getTxFIFOStatus() when in FIFO mode. The other option is to use one of the two functions SPI_writeDataBlockingNonFIFO() and SPI_writeDataBlockingFIFO() that will wait in a while-loop for the module to be ready.

When receiving data, again, there are a few options. SPI_readDataNonBlocking() will immediately return the contents of the receive buffer. The user should check that there is in fact data ready by checking the buffer-full flag or, if in FIFO mode, checking how full the FIFO is using SPI_getRxFIFOStatus(). SPI_readDataBlockingNonFIFO() and SPI_readDataBlockingFIFO(), however, will wait in a while-loop for data to become available.

The code for this module is contained in `driverlib/spi.c`, with `driverlib/spi.h` containing the API declarations for use by applications.

27.2.2 Enumeration Type Documentation

27.2.2.1 enum **SPI_TransferProtocol**

Values that can be passed to SPI_setConfig() as the *protocol* parameter.

Enumerator

SPI_PROT_POL0PHA0 Mode 0. Polarity 0, phase 0. Rising edge without delay.
SPI_PROT_POL0PHA1 Mode 1. Polarity 0, phase 1. Rising edge with delay.
SPI_PROT_POL1PHA0 Mode 2. Polarity 1, phase 0. Falling edge without delay.
SPI_PROT_POL1PHA1 Mode 3. Polarity 1, phase 1. Falling edge with delay.

27.2.2.2 enum **SPI_Mode**

Values that can be passed to SPI_setConfig() as the *mode* parameter.

Enumerator

SPI_MODE_SLAVE SPI slave.
SPI_MODE_MASTER SPI master.
SPI_MODE_SLAVE_OD SPI slave w/ output (TALK) disabled.
SPI_MODE_MASTER_OD SPI master w/ output (TALK) disabled.

27.2.2.3 enum **SPI_TxFIFOLevel**

Values that can be passed to SPI_setFIFOInterruptLevel() as the *txLevel* parameter, returned by SPI_getFIFOInterruptLevel() in the *txLevel* parameter, and returned by SPI_getTxFIFOStatus().

Enumerator

SPI_FIFO_TXEMPTY Transmit FIFO empty.
SPI_FIFO_TX0 Transmit FIFO empty.
SPI_FIFO_TX1 Transmit FIFO 1/16 full.
SPI_FIFO_TX2 Transmit FIFO 2/16 full.
SPI_FIFO_TX3 Transmit FIFO 3/16 full.
SPI_FIFO_TX4 Transmit FIFO 4/16 full.
SPI_FIFO_TX5 Transmit FIFO 5/16 full.
SPI_FIFO_TX6 Transmit FIFO 6/16 full.
SPI_FIFO_TX7 Transmit FIFO 7/16 full.
SPI_FIFO_TX8 Transmit FIFO 8/16 full.

SPI_FIFO_TX9 Transmit FIFO 9/16 full.
SPI_FIFO_TX10 Transmit FIFO 10/16 full.
SPI_FIFO_TX11 Transmit FIFO 11/16 full.
SPI_FIFO_TX12 Transmit FIFO 12/16 full.
SPI_FIFO_TX13 Transmit FIFO 13/16 full.
SPI_FIFO_TX14 Transmit FIFO 14/16 full.
SPI_FIFO_TX15 Transmit FIFO 15/16 full.
SPI_FIFO_TX16 Transmit FIFO full.
SPI_FIFO_TXFULL Transmit FIFO full.

27.2.2.4 enum **SPI_RxFIFOLevel**

Values that can be passed to SPI_setFIFOInterruptLevel() as the *rxLevel* parameter, returned by SPI_getFIFOInterruptLevel() in the *rxLevel* parameter, and returned by SPI_getRxFIFOStatus().

Enumerator

SPI_FIFO_RXEMPTY Receive FIFO empty.
SPI_FIFO_RX0 Receive FIFO empty.
SPI_FIFO_RX1 Receive FIFO 1/16 full.
SPI_FIFO_RX2 Receive FIFO 2/16 full.
SPI_FIFO_RX3 Receive FIFO 3/16 full.
SPI_FIFO_RX4 Receive FIFO 4/16 full.
SPI_FIFO_RX5 Receive FIFO 5/16 full.
SPI_FIFO_RX6 Receive FIFO 6/16 full.
SPI_FIFO_RX7 Receive FIFO 7/16 full.
SPI_FIFO_RX8 Receive FIFO 8/16 full.
SPI_FIFO_RX9 Receive FIFO 9/16 full.
SPI_FIFO_RX10 Receive FIFO 10/16 full.
SPI_FIFO_RX11 Receive FIFO 11/16 full.
SPI_FIFO_RX12 Receive FIFO 12/16 full.
SPI_FIFO_RX13 Receive FIFO 13/16 full.
SPI_FIFO_RX14 Receive FIFO 14/16 full.
SPI_FIFO_RX15 Receive FIFO 15/16 full.
SPI_FIFO_RX16 Receive FIFO full.
SPI_FIFO_RXFULL Receive FIFO full.
SPI_FIFO_RXDEFAULT To prevent interrupt at reset.

27.2.2.5 enum **SPI_EmulationMode**

Values that can be passed to SPI_setEmulationMode() as the *mode* parameter.

Enumerator

SPI_EMULATION_STOP_MIDWAY Transmission stops after midway in the bit stream.
SPI_EMULATION_FREE_RUN Continue SPI operation regardless.
SPI_EMULATION_STOP_AFTER_TRANSMIT Transmission will stop after a started transmission completes.

27.2.2.6 enum **SPI_STEPolarity**

Values that can be passed to SPI_setSTESignalPolarity() as the *polarity* parameter.

Enumerator

SPI_STE_ACTIVE_LOW SPISTE is active low (normal)

SPI_STE_ACTIVE_HIGH SPISTE is active high (inverted)

27.2.3 Function Documentation

27.2.3.1 static void SPI_enableModule (uint32_t *base*) [inline], [static]

Enables the serial peripheral interface.

Parameters

base	specifies the SPI module base address.

This function enables operation of the serial peripheral interface. The serial peripheral interface must be configured before it is enabled.

Returns

None.

27.2.3.2 static void SPI_disableModule (uint32_t *base*) [inline], [static]

Disables the serial peripheral interface.

Parameters

base	specifies the SPI module base address.

This function disables operation of the serial peripheral interface. Call this function before doing any configuration.

Returns

None.

27.2.3.3 static void SPI_enableFIFO (uint32_t *base*) [inline], [static]

Enables the transmit and receive FIFOs.

Parameters

base	is the base address of the SPI port.

This functions enables the transmit and receive FIFOs in the SPI.

Returns

None.

27.2.3.4 static void SPI_disableFIFO (uint32_t *base*) [inline], [static]

Disables the transmit and receive FIFOs.

Parameters

base	is the base address of the SPI port.

This functions disables the transmit and receive FIFOs in the SPI.

Returns

None.

27.2.3.5 static void SPI_resetTxFIFO (uint32_t *base*) [inline], [static]

Resets the transmit FIFO.

Parameters

base	is the base address of the SPI port.

This function resets the transmit FIFO, setting the FIFO pointer back to zero.

Returns

None.

27.2.3.6 static void SPI_resetRxFIFO (uint32_t *base*) [inline], [static]

Resets the receive FIFO.

Parameters

base	is the base address of the SPI port.

This function resets the receive FIFO, setting the FIFO pointer back to zero.

Returns

None.

27.2.3.7 static void SPI_setFIFOInterruptLevel (uint32_t *base,* **SPI_TxFIFOLevel** *txLevel,* **SPI_RxFIFOLevel** *rxLevel*) [inline], [static]

Sets the FIFO level at which interrupts are generated.

Parameters

base	is the base address of the SPI port.
txLevel	is the transmit FIFO interrupt level, specified as **SPI_FIFO_TX0**, **SPI_FIFO_TX1**, **SPI_FIFO_TX2**, . . . or **SPI_FIFO_TX16**.
rxLevel	is the receive FIFO interrupt level, specified as **SPI_FIFO_RX0**, **SPI_FIFO_RX1**, **SPI_FIFO_RX2**, . . . or **SPI_FIFO_RX16**.

This function sets the FIFO level at which transmit and receive interrupts are generated.

Returns

None.

27.2.3.8 static void SPI_getFIFOInterruptLevel (uint32_t *base*, **SPI_TxFIFOLevel** ∗ *txLevel*, **SPI_RxFIFOLevel** ∗ *rxLevel*) `[inline]`, `[static]`

Gets the FIFO level at which interrupts are generated.

Parameters

base	is the base address of the SPI port.
txLevel	is a pointer to storage for the transmit FIFO level, returned as one of **SPI_FIFO_TX0**, **SPI_FIFO_TX1**, **SPI_FIFO_TX2**, . . . or **SPI_FIFO_TX16**.
rxLevel	is a pointer to storage for the receive FIFO level, returned as one of **SPI_FIFO_RX0**, **SPI_FIFO_RX1**, **SPI_FIFO_RX2**, . . . or **SPI_FIFO_RX16**.

This function gets the FIFO level at which transmit and receive interrupts are generated.

Returns

None.

27.2.3.9 static **SPI_TxFIFOLevel** SPI_getTxFIFOStatus (uint32_t *base*) [inline], [static]

Get the transmit FIFO status

Parameters

base	is the base address of the SPI port.

This function gets the current number of words in the transmit FIFO.

Returns

Returns the current number of words in the transmit FIFO specified as one of the following: **SPI_FIFO_TX0**, **SPI_FIFO_TX1**, **SPI_FIFO_TX2**, **SPI_FIFO_TX3**, ..., or **SPI_FIFO_TX16**

Referenced by SPI_writeDataBlockingFIFO().

27.2.3.10 static **SPI_RxFIFOLevel** SPI_getRxFIFOStatus (uint32_t *base*) [inline], [static]

Get the receive FIFO status

Parameters

base	is the base address of the SPI port.

This function gets the current number of words in the receive FIFO.

Returns

Returns the current number of words in the receive FIFO specified as one of the following: **SPI_FIFO_RX0**, **SPI_FIFO_RX1**, **SPI_FIFO_RX2**, **SPI_FIFO_RX3**, ..., or **SPI_FIFO_RX16**

Referenced by SPI_readDataBlockingFIFO().

27.2.3.11 static bool SPI_isBusy (uint32_t *base*) [inline], [static]

Determines whether the SPI transmitter is busy or not.

Parameters

base	is the base address of the SPI port.

This function allows the caller to determine whether all transmitted bytes have cleared the transmitter hardware. If **false** is returned, then the transmit FIFO is empty and all bits of the last transmitted word have left the hardware shift register. This function is only valid when operating in FIFO mode.

Returns

Returns **true** if the SPI is transmitting or **false** if all transmissions are complete.

27.2.3.12 static void SPI_writeDataNonBlocking (uint32_t *base,* uint16_t *data*) `[inline]`, `[static]`

Puts a data element into the SPI transmit buffer.

Parameters

base	specifies the SPI module base address.
data	is the left-justified data to be transmitted over SPI.

This function places the supplied data into the transmit buffer of the specified SPI module.

Note

The data being sent must be left-justified in *data*. The lower 16 - N bits will be discarded where N is the data width selected in SPI_setConfig(). For example, if configured for a 6-bit data width, the lower 10 bits of data will be discarded.

Returns

None.

27.2.3.13 static uint16_t SPI_readDataNonBlocking (uint32_t *base*) `[inline]`, `[static]`

Gets a data element from the SPI receive buffer.

Parameters

base	specifies the SPI module base address.

This function gets received data from the receive buffer of the specified SPI module and returns it.

Note

Only the lower N bits of the value written to *data* contain valid data, where N is the data width as configured by SPI_setConfig(). For example, if the interface is configured for 8-bit data width, only the lower 8 bits of the value written to *data* contain valid data.

Returns

Returns the word of data read from the SPI receive buffer.

27.2.3.14 static void SPI_writeDataBlockingFIFO (uint32_t *base*, uint16_t *data*) [inline], [static]

Waits for space in the FIFO and then puts data into the transmit buffer.

Parameters

base	specifies the SPI module base address.
data	is the left-justified data to be transmitted over SPI.

This function places the supplied data into the transmit buffer of the specified SPI module once space is available in the transmit FIFO. This function should only be used when the FIFO is enabled.

Note

The data being sent must be left-justified in *data*. The lower 16 - N bits will be discarded where N is the data width selected in SPI_setConfig(). For example, if configured for a 6-bit data width, the lower 10 bits of data will be discarded.

Returns

None.

References SPI_FIFO_TXFULL, and SPI_getTxFIFOStatus().

27.2.3.15 static uint16_t SPI_readDataBlockingFIFO (uint32_t *base*) [inline], [static]

Waits for data in the FIFO and then reads it from the receive buffer.

Parameters

base	specifies the SPI module base address.

This function waits until there is data in the receive FIFO and then reads received data from the receive buffer. This function should only be used when FIFO mode is enabled.

Note

Only the lower N bits of the value written to *data* contain valid data, where N is the data width as configured by SPI_setConfig(). For example, if the interface is configured for 8-bit data width, only the lower 8 bits of the value written to *data* contain valid data.

Returns

Returns the word of data read from the SPI receive buffer.

References SPI_FIFO_RXEMPTY, and SPI_getRxFIFOStatus().

27.2.3.16 static void SPI_writeDataBlockingNonFIFO (uint32_t *base,* uint16_t *data*) [inline], [static]

Waits for the transmit buffer to empty and then writes data to it.

Parameters

base	specifies the SPI module base address.
data	is the left-justified data to be transmitted over SPI.

This function places the supplied data into the transmit buffer of the specified SPI module once it is empty. This function should not be used when FIFO mode is enabled.

Note

The data being sent must be left-justified in *data*. The lower 16 - N bits will be discarded where N is the data width selected in SPI_setConfig(). For example, if configured for a 6-bit data width, the lower 10 bits of data will be discarded.

Returns

None.

27.2.3.17 static uint16_t SPI_readDataBlockingNonFIFO (uint32_t *base*) [inline], [static]

Waits for data to be received and then reads it from the buffer.

Parameters

base	specifies the SPI module base address.

This function waits for data to be received and then reads it from the receive buffer of the specified SPI module. This function should not be used when FIFO mode is enabled.

Note

Only the lower N bits of the value written to *data* contain valid data, where N is the data width as configured by SPI_setConfig(). For example, if the interface is configured for 8-bit data width, only the lower 8 bits of the value written to *data* contain valid data.

Returns

Returns the word of data read from the SPI receive buffer.

27.2.3.18 static void SPI_enableTriWire (uint32_t *base*) [inline], [static]

Enables SPI 3-wire mode.

Parameters

base	is the base address of the SPI port.

This function enables 3-wire mode. When in master mode, this allows SPISIMO to become SPIMOMI and SPISOMI to become free for non-SPI use. When in slave mode, SPISOMI because the SPISISO pin and SPISIMO is free for non-SPI use.

Returns

None.

27.2.3.19 static void SPI_disableTriWire (uint32_t *base*) [inline], [static]

Disables SPI 3-wire mode.

Parameters

base	is the base address of the SPI port.

This function disables 3-wire mode. SPI will operate in normal 4-wire mode.

Returns

None.

27.2.3.20 static void SPI_enableLoopback (uint32_t *base*) [inline], [static]

Enables SPI loopback mode.

Parameters

base	is the base address of the SPI port.

This function enables loopback mode. This mode is only valid during master mode and is helpful during device testing as it internally connects SIMO and SOMI.

Returns

None.

27.2.3.21 static void SPI_disableLoopback (uint32_t *base*) [inline], [static]

Disables SPI loopback mode.

Parameters

base	is the base address of the SPI port.

This function disables loopback mode. Loopback mode is disabled by default after reset.

Returns

None.

27.2.3.22 static void SPI_setSTESignalPolarity (uint32_t *base*, **SPI_STEPolarity** *polarity*) [inline], [static]

Set the slave select (SPISTE) signal polarity.

Parameters

base	is the base address of the SPI port.
polarity	is the SPISTE signal polarity.

This function sets the polarity of the slave select (SPISTE) signal. The two modes to choose from for the *polarity* parameter are **SPI_STE_ACTIVE_LOW** for active-low polarity (typical) and **SPI_STE_ACTIVE_HIGH** for active-high polarity (considered inverted).

Note

This has no effect on the STE signal when in master mode. It is only applicable to slave mode.

Returns
None.

27.2.3.23 static void SPI_enableHighSpeedMode (uint32_t *base*) [inline], [static]

Enables SPI high speed mode.

Parameters

base	is the base address of the SPI port.

This function enables high speed mode.

Returns
None.

27.2.3.24 static void SPI_disableHighSpeedMode (uint32_t *base*) [inline], [static]

Disables SPI high speed mode.

Parameters

base	is the base address of the SPI port.

This function disables high speed mode. High speed mode is disabled by default after reset.

Returns
None.

27.2.3.25 static void SPI_setEmulationMode (uint32_t *base,* **SPI_EmulationMode** *mode*) [inline], [static]

Sets SPI emulation mode.

Parameters

base	is the base address of the SPI port.
mode	is the emulation mode.

This function sets the behavior of the SPI operation when an emulation suspend occurs. The *mode* parameter can be one of the following:

- **SPI_EMULATION_STOP_MIDWAY** - Transmission stops midway through the bit stream. The rest of the bits will be transmitting after the suspend is deasserted.
- **SPI_EMULATION_STOP_AFTER_TRANSMIT** - If the suspend occurs before the first SPICLK pulse, the transmission will not start. If it occurs later, the transmission will be completed.
- **SPI_EMULATION_FREE_RUN** - SPI operation continues regardless of a the suspend.

Returns
None.

27.2.3.26 static void SPI_setTxFifoTransmitDelay (uint32_t *base,* uint16_t *delay*) [inline], [static]

Configures the FIFO Transmit Delay

Parameters

base	is the base address of the SPI port.
delay	Tx FIFO delay to be configured in cycles (0..0xFF)

This function sets the delay between every transfer from FIFO transmit buffer to transmit shift register. The delay is defined in number SPI serial clock cycles.

Returns
None

27.2.3.27 static uint16_t SPI_readRxEmulationBuffer (uint32_t *base*) [inline], [static]

Returns the Emulation Buffer Received Data

Parameters

base	is the base address of the SPI port.

This function returns the Emulation Buffer Received Data

Returns
Rx emulation buffer data

27.2.3.28 static void SPI_enableTalk (uint32_t *base*) [inline], [static]

Enable Trasnmit

Parameters

base	is the base address of the SPI port.

This function sets the TALK bit enabling the data trasnmission. This bit is enabled by SPI_setConfig if the parameter mode is selected as SPI_MODE_SLAVE or SPI_MODE_MASTER.

Returns
None

27.2.3.29 static void SPI_disableTalk (uint32_t *base*) [inline], [static]

Disable Trasnmit

Parameters

base	is the base address of the SPI port.

This function clears the TALK bit disabling the data trasnmission. The outpiut pin will be put in high-impedance state. This bit is enabled by SPI_setConfig if the parameter mode is selected as SPI_MODE_SLAVE or SPI_MODE_MASTER.

Returns
None

27.2.3.30 void SPI_setConfig (uint32_t *base,* uint32_t *lspclkHz,* **SPI_TransferProtocol** *protocol,* **SPI_Mode** *mode,* uint32_t *bitRate,* uint16_t *dataWidth*)

Configures the serial peripheral interface.

Parameters

base	specifies the SPI module base address.
lspclkHz	is the rate of the clock supplied to the SPI module (LSPCLK) in Hz.
protocol	specifies the data transfer protocol.
mode	specifies the mode of operation.
bitRate	specifies the clock rate in Hz.
dataWidth	specifies number of bits transferred per frame.

This function configures the serial peripheral interface. It sets the SPI protocol, mode of operation, bit rate, and data width.

The *protocol* parameter defines the data frame format. The *protocol* parameter can be one of the following values: **SPI_PROT_POL0PHA0**, **SPI_PROT_POL0PHA1**, **SPI_PROT_POL1PHA0**, or **SPI_PROT_POL1PHA1**. These frame formats encode the following polarity and phase configurations:

```
Polarity Phase       Mode
  0       0    SPI_PROT_POL0PHA0
  0       1    SPI_PROT_POL0PHA1
  1       0    SPI_PROT_POL1PHA0
  1       1    SPI_PROT_POL1PHA1
```

The *mode* parameter defines the operating mode of the SPI module. The SPI module can operate as a master or slave; the SPI can also be be configured to disable output on its serial output line. The *mode* parameter can be one of the following values: **SPI_MODE_MASTER**, **SPI_MODE_SLAVE**, **SPI_MODE_MASTER_OD** or **SPI_MODE_SLAVE_OD** ("OD" indicates "output disabled").

The *bitRate* parameter defines the bit rate for the SPI. This bit rate must satisfy the following clock ratio criteria:

- *bitRate* can be no greater than lspclkHz divided by 4.
- *lspclkHz* / *bitRate* cannot be greater than 128.

The *dataWidth* parameter defines the width of the data transfers and can be a value between 1 and 16, inclusive.

The peripheral clock is the low speed peripheral clock. This value is returned by SysCtl_getLowSpeedClock(), or it can be explicitly hard coded if it is constant and known (to save the code/execution overhead of a call to SysCtl_getLowSpeedClock()).

Note

SPI operation should be disabled via SPI_disableModule() before any changes to its configuration.

Returns

None.

27.2.3.31 void SPI_setBaudRate (uint32_t *base,* uint32_t *lspclkHz,* uint32_t *bitRate*)

Configures the baud rate of the serial peripheral interface.

Parameters

base	specifies the SPI module base address.
lspclkHz	is the rate of the clock supplied to the SPI module (LSPCLK) in Hz.
bitRate	specifies the clock rate in Hz.

This function configures the SPI baud rate. The *bitRate* parameter defines the bit rate for the SPI. This bit rate must satisfy the following clock ratio criteria:

- *bitRate* can be no greater than *lspclkHz* divided by 4.
- *lspclkHz* / *bitRate* cannot be greater than 128.

The peripheral clock is the low speed peripheral clock. This value is returned by SysCtl_getLowSpeedClock(), or it can be explicitly hard coded if it is constant and known (to save the code/execution overhead of a call to SysCtl_getLowSpeedClock()).

Note

SPI_setConfig() also sets the baud rate. Use SPI_setBaudRate() if you wish to configure it separately from protocol and mode.

Returns

None.

27.2.3.32 void SPI_enableInterrupt (uint32_t *base*, uint32_t *intFlags*)

Enables individual SPI interrupt sources.

Parameters

base	specifies the SPI module base address.
intFlags	is a bit mask of the interrupt sources to be enabled.

This function enables the indicated SPI interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor. The *intFlags* parameter can be any of the following values:

- **SPI_INT_RX_OVERRUN** - Receive overrun interrupt
- **SPI_INT_RX_DATA_TX_EMPTY** - Data received, transmit empty
- **SPI_INT_RXFF** (also enables **SPI_INT_RXFF_OVERFLOW**) - RX FIFO level interrupt (and RX FIFO overflow)
- **SPI_INT_TXFF** - TX FIFO level interrupt

Note

SPI_INT_RX_OVERRUN, **SPI_INT_RX_DATA_TX_EMPTY**, **SPI_INT_RXFF_OVERFLOW**, and **SPI_INT_RXFF** are associated with **SPIRXINT**; **SPI_INT_TXFF** is associated with **SPITXINT**.

Returns

None.

27.2.3.33 void SPI_disableInterrupt (uint32_t *base,* uint32_t *intFlags*)

Disables individual SPI interrupt sources.

Parameters

base	specifies the SPI module base address.
intFlags	is a bit mask of the interrupt sources to be disabled.

This function disables the indicated SPI interrupt sources. The *intFlags* parameter can be any of the following values:

- **SPI_INT_RX_OVERRUN**
- **SPI_INT_RX_DATA_TX_EMPTY**
- **SPI_INT_RXFF** (also disables **SPI_INT_RXFF_OVERFLOW**)
- **SPI_INT_TXFF**

Note

SPI_INT_RX_OVERRUN, **SPI_INT_RX_DATA_TX_EMPTY**, **SPI_INT_RXFF_OVERFLOW**, and **SPI_INT_RXFF** are associated with **SPIRXINT**; **SPI_INT_TXFF** is associated with **SPITXINT**.

Returns

None.

27.2.3.34 uint32_t SPI_getInterruptStatus (uint32_t *base*)

Gets the current interrupt status.

Parameters

base	specifies the SPI module base address.

This function returns the interrupt status for the SPI module.

Returns

The current interrupt status, enumerated as a bit field of the following values:

- **SPI_INT_RX_OVERRUN** - Receive overrun interrupt
- **SPI_INT_RX_DATA_TX_EMPTY** - Data received, transmit empty
- **SPI_INT_RXFF** - RX FIFO level interrupt
- **SPI_INT_RXFF_OVERFLOW** - RX FIFO overflow
- **SPI_INT_TXFF** - TX FIFO level interrupt

27.2.3.35 void SPI_clearInterruptStatus (uint32_t *base,* uint32_t *intFlags*)

Clears SPI interrupt sources.

Parameters

base	specifies the SPI module base address.
intFlags	is a bit mask of the interrupt sources to be cleared.

This function clears the specified SPI interrupt sources so that they no longer assert. This function must be called in the interrupt handler to keep the interrupts from being triggered again immediately upon exit. The *intFlags* parameter can consist of a bit field of the following values:

- **SPI_INT_RX_OVERRUN**
- **SPI_INT_RX_DATA_TX_EMPTY**
- **SPI_INT_RXFF**
- **SPI_INT_RXFF_OVERFLOW**
- **SPI_INT_TXFF**

Note

SPI_INT_RX_DATA_TX_EMPTY is cleared by a read of the receive receive buffer, so it usually doesn't need to be cleared using this function.
Also note that **SPI_INT_RX_OVERRUN**, **SPI_INT_RX_DATA_TX_EMPTY**, **SPI_INT_RXFF_OVERFLOW**, and **SPI_INT_RXFF** are associated with **SPIRXINT**; **SPI_INT_TXFF** is associated with **SPITXINT**.

Returns

None.

28 SysCtl Module

28.1 SysCtl Introduction

System Control (SysCtl) determines the overall operation of the device. The API provides functions to configure the clocking of the device, the set of peripherals that are enabled, the windowed watchdog, the NMI watchdog, and low-power modes. It also provides functions to handle and obtain information about resets and missing clock detection failures.

28.2 API Functions

Macros

- #define SYSCTL_SYSDIV(x)
- #define SYSCTL_IMULT(x)

Enumerations

- enum SysCtl_PeripheralPCLOCKCR {
SYSCTL_PERIPH_CLK_CLA1, SYSCTL_PERIPH_CLK_DMA,
SYSCTL_PERIPH_CLK_TIMER0, SYSCTL_PERIPH_CLK_TIMER1,
SYSCTL_PERIPH_CLK_TIMER2, SYSCTL_PERIPH_CLK_HRPWM,
SYSCTL_PERIPH_CLK_TBCLKSYNC, SYSCTL_PERIPH_CLK_GTBCLKSYNC,
SYSCTL_PERIPH_CLK_EMIF1, SYSCTL_PERIPH_CLK_EMIF2,
SYSCTL_PERIPH_CLK_EPWM1, SYSCTL_PERIPH_CLK_EPWM2,
SYSCTL_PERIPH_CLK_EPWM3, SYSCTL_PERIPH_CLK_EPWM4,
SYSCTL_PERIPH_CLK_EPWM5, SYSCTL_PERIPH_CLK_EPWM6,
SYSCTL_PERIPH_CLK_EPWM7, SYSCTL_PERIPH_CLK_EPWM8,
SYSCTL_PERIPH_CLK_EPWM9, SYSCTL_PERIPH_CLK_EPWM10,
SYSCTL_PERIPH_CLK_EPWM11, SYSCTL_PERIPH_CLK_EPWM12,
SYSCTL_PERIPH_CLK_ECAP1, SYSCTL_PERIPH_CLK_ECAP2,
SYSCTL_PERIPH_CLK_ECAP3, SYSCTL_PERIPH_CLK_ECAP4,
SYSCTL_PERIPH_CLK_ECAP5, SYSCTL_PERIPH_CLK_ECAP6,
SYSCTL_PERIPH_CLK_EQEP1, SYSCTL_PERIPH_CLK_EQEP2,
SYSCTL_PERIPH_CLK_EQEP3, SYSCTL_PERIPH_CLK_SD1,
SYSCTL_PERIPH_CLK_SD2, SYSCTL_PERIPH_CLK_SCIA,
SYSCTL_PERIPH_CLK_SCIB, SYSCTL_PERIPH_CLK_SCIC,
SYSCTL_PERIPH_CLK_SCID, SYSCTL_PERIPH_CLK_SPIA,
SYSCTL_PERIPH_CLK_SPIB, SYSCTL_PERIPH_CLK_SPIC,
SYSCTL_PERIPH_CLK_I2CA, SYSCTL_PERIPH_CLK_I2CB,
SYSCTL_PERIPH_CLK_CANA, SYSCTL_PERIPH_CLK_CANB,
SYSCTL_PERIPH_CLK_MCBSPA, SYSCTL_PERIPH_CLK_MCBSPB,

SYSCTL_PERIPH_CLK_USBA, SYSCTL_PERIPH_CLK_UPPA, SYSCTL_PERIPH_CLK_ADCA, SYSCTL_PERIPH_CLK_ADCB, SYSCTL_PERIPH_CLK_ADCC, SYSCTL_PERIPH_CLK_ADCD, SYSCTL_PERIPH_CLK_CMPSS1, SYSCTL_PERIPH_CLK_CMPSS2, SYSCTL_PERIPH_CLK_CMPSS3, SYSCTL_PERIPH_CLK_CMPSS4, SYSCTL_PERIPH_CLK_CMPSS5, SYSCTL_PERIPH_CLK_CMPSS6, SYSCTL_PERIPH_CLK_CMPSS7, SYSCTL_PERIPH_CLK_CMPSS8, SYSCTL_PERIPH_CLK_DACA, SYSCTL_PERIPH_CLK_DACB, SYSCTL_PERIPH_CLK_DACC }

- enum SysCtl_PeripheralSOFTPRES { SYSCTL_PERIPH_RES_CPU1_CLA1, SYSCTL_PERIPH_RES_CPU2_CLA1, SYSCTL_PERIPH_RES_EMIF1, SYSCTL_PERIPH_RES_EMIF2, SYSCTL_PERIPH_RES_EPWM1, SYSCTL_PERIPH_RES_EPWM2, SYSCTL_PERIPH_RES_EPWM3, SYSCTL_PERIPH_RES_EPWM4, SYSCTL_PERIPH_RES_EPWM5, SYSCTL_PERIPH_RES_EPWM6, SYSCTL_PERIPH_RES_EPWM7, SYSCTL_PERIPH_RES_EPWM8, SYSCTL_PERIPH_RES_EPWM9, SYSCTL_PERIPH_RES_EPWM10, SYSCTL_PERIPH_RES_EPWM11, SYSCTL_PERIPH_RES_EPWM12, SYSCTL_PERIPH_RES_ECAP1, SYSCTL_PERIPH_RES_ECAP2, SYSCTL_PERIPH_RES_ECAP3, SYSCTL_PERIPH_RES_ECAP4, SYSCTL_PERIPH_RES_ECAP5, SYSCTL_PERIPH_RES_ECAP6, SYSCTL_PERIPH_RES_EQEP1, SYSCTL_PERIPH_RES_EQEP2, SYSCTL_PERIPH_RES_EQEP3, SYSCTL_PERIPH_RES_SD1, SYSCTL_PERIPH_RES_SD2, SYSCTL_PERIPH_RES_SCIA, SYSCTL_PERIPH_RES_SCIB, SYSCTL_PERIPH_RES_SCIC, SYSCTL_PERIPH_RES_SCID, SYSCTL_PERIPH_RES_SPIA, SYSCTL_PERIPH_RES_SPIB, SYSCTL_PERIPH_RES_SPIC, SYSCTL_PERIPH_RES_I2CA, SYSCTL_PERIPH_RES_I2CB, SYSCTL_PERIPH_RES_MCBSPA, SYSCTL_PERIPH_RES_MCBSPB, SYSCTL_PERIPH_RES_USBA, SYSCTL_PERIPH_RES_ADCA, SYSCTL_PERIPH_RES_ADCB, SYSCTL_PERIPH_RES_ADCC, SYSCTL_PERIPH_RES_ADCD, SYSCTL_PERIPH_RES_CMPSS1, SYSCTL_PERIPH_RES_CMPSS2, SYSCTL_PERIPH_RES_CMPSS3, SYSCTL_PERIPH_RES_CMPSS4, SYSCTL_PERIPH_RES_CMPSS5, SYSCTL_PERIPH_RES_CMPSS6, SYSCTL_PERIPH_RES_CMPSS7, SYSCTL_PERIPH_RES_CMPSS8, SYSCTL_PERIPH_RES_DACA, SYSCTL_PERIPH_RES_DACB, SYSCTL_PERIPH_RES_DACC }
- enum SysCtl_CPUSelPeripheral { SYSCTL_CPUSEL0_EPWM, SYSCTL_CPUSEL1_ECAP, SYSCTL_CPUSEL2_EQEP, SYSCTL_CPUSEL4_SD, SYSCTL_CPUSEL5_SCI, SYSCTL_CPUSEL6_SPI, SYSCTL_CPUSEL7_I2C, SYSCTL_CPUSEL8_CAN, SYSCTL_CPUSEL9_MCBSP, SYSCTL_CPUSEL11_ADC, SYSCTL_CPUSEL12_CMPSS, SYSCTL_CPUSEL14_DAC }
- enum SysCtl_CPUSel { SYSCTL_CPUSEL_CPU1, SYSCTL_CPUSEL_CPU2 }
- enum SysCtl_WDPrescaler { SYSCTL_WD_PRESCALE_1, SYSCTL_WD_PRESCALE_2, SYSCTL_WD_PRESCALE_4, SYSCTL_WD_PRESCALE_8, SYSCTL_WD_PRESCALE_16, SYSCTL_WD_PRESCALE_32, SYSCTL_WD_PRESCALE_64 }
- enum SysCtl_WDMode { SYSCTL_WD_MODE_RESET, SYSCTL_WD_MODE_INTERRUPT }

- enum SysCtl_LSPCLKPrescaler {
  SYSCTL_LSPCLK_PRESCALE_1, SYSCTL_LSPCLK_PRESCALE_2,
  SYSCTL_LSPCLK_PRESCALE_4, SYSCTL_LSPCLK_PRESCALE_6,
  SYSCTL_LSPCLK_PRESCALE_8, SYSCTL_LSPCLK_PRESCALE_10,
  SYSCTL_LSPCLK_PRESCALE_12, SYSCTL_LSPCLK_PRESCALE_14 }
- enum SysCtl_EPWMCLKDivider { SYSCTL_EPWMCLK_DIV_1,
  SYSCTL_EPWMCLK_DIV_2 }
- enum SysCtl_EMIF1CLKDivider { SYSCTL_EMIF1CLK_DIV_1, SYSCTL_EMIF1CLK_DIV_2
  }
- enum SysCtl_EMIF2CLKDivider { SYSCTL_EMIF2CLK_DIV_1, SYSCTL_EMIF2CLK_DIV_2
  }
- enum SysCtl_ClockOut {
  SYSCTL_CLOCKOUT_PLLSYS, SYSCTL_CLOCKOUT_PLLRAW,
  SYSCTL_CLOCKOUT_SYSCLK, SYSCTL_CLOCKOUT_INTOSC1,
  SYSCTL_CLOCKOUT_INTOSC2, SYSCTL_CLOCKOUT_XTALOSC }
- enum SysCtl_SyncInput {
  SYSCTL_SYNC_IN_EPWM4, SYSCTL_SYNC_IN_EPWM7, SYSCTL_SYNC_IN_EPWM10,
  SYSCTL_SYNC_IN_ECAP1,
  SYSCTL_SYNC_IN_ECAP4 }
- enum SysCtl_SyncInputSource {
  SYSCTL_SYNC_IN_SRC_EPWM1SYNCOUT,
  SYSCTL_SYNC_IN_SRC_EPWM4SYNCOUT,
  SYSCTL_SYNC_IN_SRC_EPWM7SYNCOUT,
  SYSCTL_SYNC_IN_SRC_EPWM10SYNCOUT,
  SYSCTL_SYNC_IN_SRC_ECAP1SYNCOUT, SYSCTL_SYNC_IN_SRC_EXTSYNCIN1,
  SYSCTL_SYNC_IN_SRC_EXTSYNCIN2 }
- enum SysCtl_SyncOutputSource { SYSCTL_SYNC_OUT_SRC_EPWM1SYNCOUT,
  SYSCTL_SYNC_OUT_SRC_EPWM4SYNCOUT,
  SYSCTL_SYNC_OUT_SRC_EPWM7SYNCOUT,
  SYSCTL_SYNC_OUT_SRC_EPWM10SYNCOUT }
- enum SysCtl_DeviceParametric {
  SYSCTL_DEVICE_QUAL, SYSCTL_DEVICE_PINCOUNT, SYSCTL_DEVICE_INSTASPIN,
  SYSCTL_DEVICE_FLASH,
  SYSCTL_DEVICE_PARTID, SYSCTL_DEVICE_FAMILY, SYSCTL_DEVICE_PARTNO,
  SYSCTL_DEVICE_CLASSID }

Functions

- static void SysCtl_resetPeripheral (SysCtl_PeripheralSOFTPRES peripheral)
- static void SysCtl_enablePeripheral (SysCtl_PeripheralPCLOCKCR peripheral)
- static void SysCtl_disablePeripheral (SysCtl_PeripheralPCLOCKCR peripheral)
- static void SysCtl_resetDevice (void)
- static uint32_t SysCtl_getResetCause (void)
- static void SysCtl_clearResetCause (uint32_t rstCauses)
- static void SysCtl_setLowSpeedClock (SysCtl_LSPCLKPrescaler prescaler)
- static void SysCtl_setEPWMClockDivider (SysCtl_EPWMCLKDivider divider)
- static void SysCtl_setEMIF1ClockDivider (SysCtl_EMIF1CLKDivider divider)
- static void SysCtl_setEMIF2ClockDivider (SysCtl_EMIF2CLKDivider divider)
- static void SysCtl_selectClockOutSource (SysCtl_ClockOut source)
- static uint16_t SysCtl_getExternalOscCounterValue (void)
- static void SysCtl_turnOnOsc (uint32_t oscSource)
- static void SysCtl_turnOffOsc (uint32_t oscSource)
- static void SysCtl_enterIdleMode (void)
- static void SysCtl_enterStandbyMode (void)

- static void SysCtl_enterHaltMode (void)
- static void SysCtl_enterHibernateMode (void)
- static void SysCtl_enableLPMWakeupPin (uint32_t pin)
- static void SysCtl_disableLPMWakeupPin (uint32_t pin)
- static void SysCtl_setStandbyQualificationPeriod (uint16_t cycles)
- static void SysCtl_enableWatchdogStandbyWakeup (void)
- static void SysCtl_disableWatchdogStandbyWakeup (void)
- static void SysCtl_enableWatchdogInHalt (void)
- static void SysCtl_disableWatchdogInHalt (void)
- static void SysCtl_setWatchdogMode (SysCtl_WDMode mode)
- static bool SysCtl_isWatchdogInterruptActive (void)
- static void SysCtl_disableWatchdog (void)
- static void SysCtl_enableWatchdog (void)
- static void SysCtl_serviceWatchdog (void)
- static void SysCtl_setWatchdogPrescaler (SysCtl_WDPrescaler prescaler)
- static uint16_t SysCtl_getWatchdogCounterValue (void)
- static bool SysCtl_getWatchdogResetStatus (void)
- static void SysCtl_clearWatchdogResetStatus (void)
- static void SysCtl_setWatchdogWindowValue (uint16_t value)
- static void SysCtl_enableNMIGlobalInterrupt (void)
- static bool SysCtl_getNMIStatus (void)
- static uint16_t SysCtl_getNMIFlagStatus (void)
- static bool SysCtl_isNMIFlagSet (uint32_t nmiFlags)
- static void SysCtl_clearNMIStatus (uint32_t nmiFlags)
- static void SysCtl_clearAllNMIFlags (void)
- static void SysCtl_forceNMIFlags (uint32_t nmiFlags)
- static uint16_t SysCtl_getNMIWatchdogCounter (void)
- static void SysCtl_setNMIWatchdogPeriod (uint16_t wdPeriod)
- static uint16_t SysCtl_getNMIWatchdogPeriod (void)
- static uint32_t SysCtl_getNMIShadowFlagStatus (void)
- static bool SysCtl_isNMIShadowFlagSet (uint32_t nmiFlags)
- static void SysCtl_enableMCD (void)
- static void SysCtl_disableMCD (void)
- static bool SysCtl_isMCDClockFailureDetected (void)
- static void SysCtl_resetMCD (void)
- static void SysCtl_connectMCDClockSource (void)
- static void SysCtl_disconnectMCDClockSource (void)
- static void SysCtl_setSyncInputConfig (SysCtl_SyncInput syncInput, SysCtl_SyncInputSource syncSrc)
- static void SysCtl_setSyncOutputConfig (SysCtl_SyncOutputSource syncSrc)
- static void SysCtl_enableExtADCSOCSource (uint32_t adcsocSrc)
- static void SysCtl_disableExtADCSOCSource (uint32_t adcsocSrc)
- static void SysCtl_lockExtADCSOCSelect (void)
- static void SysCtl_selectSecMaster (uint16_t periFrame1Config, uint16_t periFrame2Config)
- static void SysCtl_lockSyncSelect (void)
- static void SysCtl_selectCPUForPeripheral (SysCtl_CPUSelPeripheral peripheral, uint16_t peripheralInst, SysCtl_CPUSel cpuInst)
- static uint32_t SysCtl_getDeviceRevision (void)
- void SysCtl_delay (uint32_t count)
- uint32_t SysCtl_getClock (uint32_t clockInHz)
- uint32_t SysCtl_getAuxClock (uint32_t clockInHz)
- bool SysCtl_setClock (uint32_t config)
- void SysCtl_selectOscSource (uint32_t oscSource)
- uint32_t SysCtl_getLowSpeedClock (uint32_t clockInHz)
- uint16_t SysCtl_getDeviceParametric (SysCtl_DeviceParametric parametric)
- void SysCtl_setAuxClock (uint32_t config)

28.2.1 Detailed Description

Many of the functions provided by the SysCtl API are related to device clocking. The most important of these functions is SysCtl_setClock() which will configure which oscillator is to be used, configure the PLL, and configure the system clock divider. SysCtl_getClock() is a complementary function to this one that will, given the frequency of the oscillator source used, read back the configuration of the PLL and clock divider and calculate the system clock frequency. A similar pair of functions is provided for the low-speed peripheral clock, SysCtl_setLowSpeedClock() and SysCtl_getLowSpeedClock().

The ability to enable (turn on the module clock), disable (gate off the module clock), and perform a software reset on most of the peripherals on a device is provided by SysCtl_enablePeripheral(), SysCtl_disablePeripheral(), and SysCtl_resetPeripheral() respectively.

The device's windowed watchdog is enabled and disabled by SysCtl_enableWatchdog() and SysCtl_disableWatchdog() respectively. The watchdog can be serviced by SysCtl_serviceWatchdog(). Several functions are also provided to configure the watchdog's clock and windowed functionality.

This section will give further details of these functions and each of the others used for the configuration of SysCtl.

The code for this module is contained in `driverlib/sysctl.c`, with `driverlib/sysctl.h` containing the API declarations for use by applications.

28.2.2 Macro Definition Documentation

28.2.2.1 #define SYSCTL_SYSDIV(*x*)

Macro to format system clock divider value. x must be 1 or even values up to 126.

28.2.2.2 #define SYSCTL_IMULT(*x*)

Macro to format integer multiplier value. x is a number from 1 to 127.

28.2.3 Enumeration Type Documentation

28.2.3.1 enum **SysCtl_PeripheralPCLOCKCR**

The following are values that can be passed to SysCtl_enablePeripheral() and SysCtl_disablePeripheral() as the *peripheral* parameter.

Enumerator

SYSCTL_PERIPH_CLK_CLA1 CLA1 clock.
SYSCTL_PERIPH_CLK_DMA DMA clock.
SYSCTL_PERIPH_CLK_TIMER0 CPUTIMER0 clock.
SYSCTL_PERIPH_CLK_TIMER1 CPUTIMER1 clock.
SYSCTL_PERIPH_CLK_TIMER2 CPUTIMER2 clock.
SYSCTL_PERIPH_CLK_HRPWM HRPWM clock.

SYSCTL_PERIPH_CLK_TBCLKSYNC ePWM time base clock sync
SYSCTL_PERIPH_CLK_GTBCLKSYNC ePWM global time base sync
SYSCTL_PERIPH_CLK_EMIF1 EMIF1 clock.
SYSCTL_PERIPH_CLK_EMIF2 EMIF2 clock.
SYSCTL_PERIPH_CLK_EPWM1 ePWM1 clock
SYSCTL_PERIPH_CLK_EPWM2 ePWM2 clock
SYSCTL_PERIPH_CLK_EPWM3 ePWM3 clock
SYSCTL_PERIPH_CLK_EPWM4 ePWM4 clock
SYSCTL_PERIPH_CLK_EPWM5 ePWM5 clock
SYSCTL_PERIPH_CLK_EPWM6 ePWM6 clock
SYSCTL_PERIPH_CLK_EPWM7 ePWM7 clock
SYSCTL_PERIPH_CLK_EPWM8 ePWM8 clock
SYSCTL_PERIPH_CLK_EPWM9 ePWM9 clock
SYSCTL_PERIPH_CLK_EPWM10 ePWM10 clock
SYSCTL_PERIPH_CLK_EPWM11 ePWM11 clock
SYSCTL_PERIPH_CLK_EPWM12 ePWM12 clock
SYSCTL_PERIPH_CLK_ECAP1 eCAP1 clock
SYSCTL_PERIPH_CLK_ECAP2 eCAP2 clock
SYSCTL_PERIPH_CLK_ECAP3 eCAP3 clock
SYSCTL_PERIPH_CLK_ECAP4 eCAP4 clock
SYSCTL_PERIPH_CLK_ECAP5 eCAP5 clock
SYSCTL_PERIPH_CLK_ECAP6 eCAP6 clock
SYSCTL_PERIPH_CLK_EQEP1 eQEP1 clock
SYSCTL_PERIPH_CLK_EQEP2 eQEP2 clock
SYSCTL_PERIPH_CLK_EQEP3 eQEP3 clock
SYSCTL_PERIPH_CLK_SD1 SDFM1 clock.
SYSCTL_PERIPH_CLK_SD2 SDFM2 clock.
SYSCTL_PERIPH_CLK_SCIA SCIA clock.
SYSCTL_PERIPH_CLK_SCIB SCIB clock.
SYSCTL_PERIPH_CLK_SCIC SCIC clock.
SYSCTL_PERIPH_CLK_SCID SCID clock.
SYSCTL_PERIPH_CLK_SPIA SPIA clock.
SYSCTL_PERIPH_CLK_SPIB SPIB clock.
SYSCTL_PERIPH_CLK_SPIC SPIC clock.
SYSCTL_PERIPH_CLK_I2CA I2CA clock.
SYSCTL_PERIPH_CLK_I2CB I2CB clock.
SYSCTL_PERIPH_CLK_CANA CANA clock.
SYSCTL_PERIPH_CLK_CANB CANB clock.
SYSCTL_PERIPH_CLK_MCBSPA McBSPA clock.
SYSCTL_PERIPH_CLK_MCBSPB McBSPB clock.
SYSCTL_PERIPH_CLK_USBA USBA clock.
SYSCTL_PERIPH_CLK_UPPA uPPA clock
SYSCTL_PERIPH_CLK_ADCA ADCA clock.
SYSCTL_PERIPH_CLK_ADCB ADCB clock.
SYSCTL_PERIPH_CLK_ADCC ADCC clock.
SYSCTL_PERIPH_CLK_ADCD ADCD clock.

SYSCTL_PERIPH_CLK_CMPSS1 CMPSS1 clock.
SYSCTL_PERIPH_CLK_CMPSS2 CMPSS2 clock.
SYSCTL_PERIPH_CLK_CMPSS3 CMPSS3 clock.
SYSCTL_PERIPH_CLK_CMPSS4 CMPSS4 clock.
SYSCTL_PERIPH_CLK_CMPSS5 CMPSS5 clock.
SYSCTL_PERIPH_CLK_CMPSS6 CMPSS6 clock.
SYSCTL_PERIPH_CLK_CMPSS7 CMPSS7 clock.
SYSCTL_PERIPH_CLK_CMPSS8 CMPSS8 clock.
SYSCTL_PERIPH_CLK_DACA DACA clock.
SYSCTL_PERIPH_CLK_DACB DACB clock.
SYSCTL_PERIPH_CLK_DACC DACC clock.

28.2.3.2 enum **SysCtl_PeripheralSOFTPRES**

The following are values that can be passed to SysCtl_resetPeripheral() as the *peripheral* parameter.

Enumerator

SYSCTL_PERIPH_RES_CPU1_CLA1 Reset CPU1 CLA1.
SYSCTL_PERIPH_RES_CPU2_CLA1 Reset CPU2 CLA1.
SYSCTL_PERIPH_RES_EMIF1 Reset EMIF1.
SYSCTL_PERIPH_RES_EMIF2 Reset EMIF2.
SYSCTL_PERIPH_RES_EPWM1 Reset ePWM1.
SYSCTL_PERIPH_RES_EPWM2 Reset ePWM2.
SYSCTL_PERIPH_RES_EPWM3 Reset ePWM3.
SYSCTL_PERIPH_RES_EPWM4 Reset ePWM4.
SYSCTL_PERIPH_RES_EPWM5 Reset ePWM5.
SYSCTL_PERIPH_RES_EPWM6 Reset ePWM6.
SYSCTL_PERIPH_RES_EPWM7 Reset ePWM7.
SYSCTL_PERIPH_RES_EPWM8 Reset ePWM8.
SYSCTL_PERIPH_RES_EPWM9 Reset ePWM9.
SYSCTL_PERIPH_RES_EPWM10 Reset ePWM10.
SYSCTL_PERIPH_RES_EPWM11 Reset ePWM11.
SYSCTL_PERIPH_RES_EPWM12 Reset ePWM12.
SYSCTL_PERIPH_RES_ECAP1 Reset eCAP1.
SYSCTL_PERIPH_RES_ECAP2 Reset eCAP2.
SYSCTL_PERIPH_RES_ECAP3 Reset eCAP3.
SYSCTL_PERIPH_RES_ECAP4 Reset eCAP4.
SYSCTL_PERIPH_RES_ECAP5 Reset eCAP5.
SYSCTL_PERIPH_RES_ECAP6 Reset eCAP6.
SYSCTL_PERIPH_RES_EQEP1 Reset eQEP1.
SYSCTL_PERIPH_RES_EQEP2 Reset eQEP2.
SYSCTL_PERIPH_RES_EQEP3 Reset eQEP3.
SYSCTL_PERIPH_RES_SD1 Reset SDFM1.
SYSCTL_PERIPH_RES_SD2 Reset SDFM2.
SYSCTL_PERIPH_RES_SCIA Reset SCIA.

SYSCTL_PERIPH_RES_SCIB Reset SCIB.
SYSCTL_PERIPH_RES_SCIC Reset SCIC.
SYSCTL_PERIPH_RES_SCID Reset SCID.
SYSCTL_PERIPH_RES_SPIA Reset SPIA.
SYSCTL_PERIPH_RES_SPIB Reset SPIB.
SYSCTL_PERIPH_RES_SPIC Reset SPIC.
SYSCTL_PERIPH_RES_I2CA Reset I2CA.
SYSCTL_PERIPH_RES_I2CB Reset I2CB.
SYSCTL_PERIPH_RES_MCBSPA Reset McBSPA.
SYSCTL_PERIPH_RES_MCBSPB Reset McBSPB.
SYSCTL_PERIPH_RES_USBA Reset USBA.
SYSCTL_PERIPH_RES_ADCA Reset ADCA.
SYSCTL_PERIPH_RES_ADCB Reset ADCB.
SYSCTL_PERIPH_RES_ADCC Reset ADCC.
SYSCTL_PERIPH_RES_ADCD Reset ADCD.
SYSCTL_PERIPH_RES_CMPSS1 Reset CMPSS1.
SYSCTL_PERIPH_RES_CMPSS2 Reset CMPSS2.
SYSCTL_PERIPH_RES_CMPSS3 Reset CMPSS3.
SYSCTL_PERIPH_RES_CMPSS4 Reset CMPSS4.
SYSCTL_PERIPH_RES_CMPSS5 Reset CMPSS5.
SYSCTL_PERIPH_RES_CMPSS6 Reset CMPSS6.
SYSCTL_PERIPH_RES_CMPSS7 Reset CMPSS7.
SYSCTL_PERIPH_RES_CMPSS8 Reset CMPSS8.
SYSCTL_PERIPH_RES_DACA Reset DACA.
SYSCTL_PERIPH_RES_DACB Reset DACB.
SYSCTL_PERIPH_RES_DACC Reset DACC.

28.2.3.3 enum **SysCtl_CPUSelPeripheral**

The following are values that can be passed to SysCtl_selectCPUForPeripheral() & SysCtl_lockCPUSelectRegs() as the *peripheral* parameter.

Enumerator

SYSCTL_CPUSEL0_EPWM Configure CPU Select for EPWM.
SYSCTL_CPUSEL1_ECAP Configure CPU Select for ECAP.
SYSCTL_CPUSEL2_EQEP Configure CPU Select for EQEP.
SYSCTL_CPUSEL4_SD Configure CPU Select for SD.
SYSCTL_CPUSEL5_SCI Configure CPU Select for SCI.
SYSCTL_CPUSEL6_SPI Configure CPU Select for SPI.
SYSCTL_CPUSEL7_I2C Configure CPU Select for I2C.
SYSCTL_CPUSEL8_CAN Configure CPU Select for CAN.
SYSCTL_CPUSEL9_MCBSP Configure CPU Select for MCBSP.
SYSCTL_CPUSEL11_ADC Configure CPU Select for ADC.
SYSCTL_CPUSEL12_CMPSS Configure CPU Select for CMPSS.
SYSCTL_CPUSEL14_DAC Configure CPU Select for DAC.

28.2.3.4 enum **SysCtl_CPUSel**

The following are values that can be passed to SysCtl_selectCPUForPeripheral() as *cpuInst* parameter.

Enumerator

SYSCTL_CPUSEL_CPU1 Connect the peripheral (indicated by SysCtl_CPUSelPeripheral) to CPU1.

SYSCTL_CPUSEL_CPU2 Connect the peripheral (indicated by SysCtl_CPUSelPeripheral) to CPU2.

28.2.3.5 enum **SysCtl_WDPrescaler**

The following are values that can be passed to SysCtl_setWatchdogPrescaler() as the *prescaler* parameter.

Enumerator

SYSCTL_WD_PRESCALE_1 WDCLK = PREDIVCLK / 1.

SYSCTL_WD_PRESCALE_2 WDCLK = PREDIVCLK / 2.

SYSCTL_WD_PRESCALE_4 WDCLK = PREDIVCLK / 4.

SYSCTL_WD_PRESCALE_8 WDCLK = PREDIVCLK / 8.

SYSCTL_WD_PRESCALE_16 WDCLK = PREDIVCLK / 16.

SYSCTL_WD_PRESCALE_32 WDCLK = PREDIVCLK / 32.

SYSCTL_WD_PRESCALE_64 WDCLK = PREDIVCLK / 64.

28.2.3.6 enum **SysCtl_WDMode**

The following are values that can be passed to SysCtl_setWatchdogMode() as the *prescaler* parameter.

Enumerator

SYSCTL_WD_MODE_RESET Watchdog can generate a reset signal.

SYSCTL_WD_MODE_INTERRUPT Watchdog can generate an interrupt signal; reset signal is disabled.

28.2.3.7 enum **SysCtl_LSPCLKPrescaler**

The following are values that can be passed to SysCtl_setLowSpeedClock() as the *prescaler* parameter.

Enumerator

SYSCTL_LSPCLK_PRESCALE_1 LSPCLK = SYSCLK / 1.

SYSCTL_LSPCLK_PRESCALE_2 LSPCLK = SYSCLK / 2.

SYSCTL_LSPCLK_PRESCALE_4 LSPCLK = SYSCLK / 4 (default)

SYSCTL_LSPCLK_PRESCALE_6 LSPCLK = SYSCLK / 6.

SYSCTL_LSPCLK_PRESCALE_8 LSPCLK = SYSCLK / 8.

SYSCTL_LSPCLK_PRESCALE_10 LSPCLK = SYSCLK / 10.

SYSCTL_LSPCLK_PRESCALE_12 LSPCLK = SYSCLK / 12.
SYSCTL_LSPCLK_PRESCALE_14 LSPCLK = SYSCLK / 14.

28.2.3.8 enum **SysCtl_EPWMCLKDivider**

The following are values that can be passed to SysCtl_setEPWMClockDivider() as the *divider* parameter.

Enumerator
SYSCTL_EPWMCLK_DIV_1 EPWMCLK = PLLSYSCLK / 1.
SYSCTL_EPWMCLK_DIV_2 EPWMCLK = PLLSYSCLK / 2.

28.2.3.9 enum **SysCtl_EMIF1CLKDivider**

The following are values that can be passed to SysCtl_setEMIF1ClockDivider() as the *divider* parameter.

Enumerator
SYSCTL_EMIF1CLK_DIV_1 EMIF1CLK = PLLSYSCLK / 1.
SYSCTL_EMIF1CLK_DIV_2 EMIF1CLK = PLLSYSCLK / 2.

28.2.3.10 enum **SysCtl_EMIF2CLKDivider**

The following are values that can be passed to SysCtl_setEMIF2ClockDivider() as the *divider* parameter.

Enumerator
SYSCTL_EMIF2CLK_DIV_1 EMIF2CLK = PLLSYSCLK / 1.
SYSCTL_EMIF2CLK_DIV_2 EMIF2CLK = PLLSYSCLK / 2.

28.2.3.11 enum **SysCtl_ClockOut**

The following are values that can be passed to SysCtl_selectClockOutSource() as the *source* parameter.

Enumerator
SYSCTL_CLOCKOUT_PLLSYS PLL System Clock post SYSCLKDIV.
SYSCTL_CLOCKOUT_PLLRAW PLL Raw Clock.
SYSCTL_CLOCKOUT_SYSCLK CPU System Clock.
SYSCTL_CLOCKOUT_INTOSC1 Internal Oscillator 1.
SYSCTL_CLOCKOUT_INTOSC2 Internal Oscillator 2.
SYSCTL_CLOCKOUT_XTALOSC External Oscillator.

28.2.3.12 enum **SysCtl_SyncInput**

The following values define the *syncInput* parameter for SysCtl_setSyncInputConfig().

Enumerator

SYSCTL_SYNC_IN_EPWM4 Sync input to ePWM 4.
SYSCTL_SYNC_IN_EPWM7 Sync input to ePWM 7.
SYSCTL_SYNC_IN_EPWM10 Sync input to ePWM 10.
SYSCTL_SYNC_IN_ECAP1 Sync input to eCAP 1.
SYSCTL_SYNC_IN_ECAP4 Sync input to eCAP 4.

28.2.3.13 enum **SysCtl_SyncInputSource**

The following values define the *syncSrc* parameter for SysCtl_setSyncInputConfig(). Note that some of these are only valid for certain values of *syncInput*. See device technical reference manual for info on time-base counter synchronization for details.

Enumerator

SYSCTL_SYNC_IN_SRC_EPWM1SYNCOUT EPWM1SYNCOUT.
SYSCTL_SYNC_IN_SRC_EPWM4SYNCOUT EPWM4SYNCOUT.
SYSCTL_SYNC_IN_SRC_EPWM7SYNCOUT EPWM7SYNCOUT.
SYSCTL_SYNC_IN_SRC_EPWM10SYNCOUT EPWM10SYNCOUT.
SYSCTL_SYNC_IN_SRC_ECAP1SYNCOUT ECAP1SYNCOUT.
SYSCTL_SYNC_IN_SRC_EXTSYNCIN1 EXTSYNCIN1–Valid for all values of syncInput.
SYSCTL_SYNC_IN_SRC_EXTSYNCIN2 EXTSYNCIN2–Valid for all values of syncInput.

28.2.3.14 enum **SysCtl_SyncOutputSource**

The following values define the *syncSrc* parameter for SysCtl_setSyncOutputConfig().

Enumerator

SYSCTL_SYNC_OUT_SRC_EPWM1SYNCOUT EPWM1SYNCOUT –> EXTSYNCOUT.
SYSCTL_SYNC_OUT_SRC_EPWM4SYNCOUT EPWM4SYNCOUT –> EXTSYNCOUT.
SYSCTL_SYNC_OUT_SRC_EPWM7SYNCOUT EPWM7SYNCOUT –> EXTSYNCOUT.
SYSCTL_SYNC_OUT_SRC_EPWM10SYNCOUT EPWM10SYNCOUT –> EXTSYNCOUT.

28.2.3.15 enum **SysCtl_DeviceParametric**

The following values define the *parametric* parameter for SysCtl_getDeviceParametric().

Enumerator

SYSCTL_DEVICE_QUAL Device Qualification Status.
SYSCTL_DEVICE_PINCOUNT Device Pin Count.
SYSCTL_DEVICE_INSTASPIN Device InstaSPIN Feature Set.
SYSCTL_DEVICE_FLASH Device Flash size (KB)
SYSCTL_DEVICE_PARTID Device Part ID Format Revision.

SYSCTL_DEVICE_FAMILY Device Family.
SYSCTL_DEVICE_PARTNO Device Part Number.
SYSCTL_DEVICE_CLASSID Device Class ID.

28.2.4 Function Documentation

28.2.4.1 static void SysCtl_resetPeripheral (**SysCtl_PeripheralSOFTPRES** *peripheral*) [inline], [static]

Resets a peripheral

Parameters

peripheral	is the peripheral to reset.

This function uses the SOFTPRESx registers to reset a specified peripheral. Module registers will be returned to their reset states.

Note

This includes registers containing trim values.The peripheral software reset needed by CPU2 can be communicated to CPU1 via IPC for all shared peripherals.

Returns

None.

28.2.4.2 static void SysCtl_enablePeripheral (**SysCtl_PeripheralPCLOCKCR** *peripheral*) [inline], [static]

Enables a peripheral.

Parameters

peripheral	is the peripheral to enable.

Peripherals are enabled with this function. At power-up, all peripherals are disabled; they must be enabled in order to operate or respond to register reads/writes.

Returns

None.

28.2.4.3 static void SysCtl_disablePeripheral (**SysCtl_PeripheralPCLOCKCR** *peripheral*) [inline], [static]

Disables a peripheral.

Parameters

peripheral	is the peripheral to disable.

Peripherals are disabled with this function. Once disabled, they will not operate or respond to register reads/writes.

Returns
None.

28.2.4.4 static void SysCtl_resetDevice (void) [inline], [static]

Resets the device.

This function performs a watchdog reset of the device.

Returns
This function does not return.

28.2.4.5 static uint32_t SysCtl_getResetCause (void) [inline], [static]

Gets the reason for a reset.

This function will return the reason(s) for a reset. Since the reset reasons are sticky until either cleared by software or an external reset, multiple reset reasons may be returned if multiple resets have occurred. The reset reason will be a logical OR of

- **SYSCTL_CAUSE_POR** - Power-on reset
- **SYSCTL_CAUSE_XRS** - External reset pin
- **SYSCTL_CAUSE_WDRS** - Watchdog reset
- **SYSCTL_CAUSE_NMIWDRS** - NMI watchdog reset
- **SYSCTL_CAUSE_SCCRESET** - SCCRESETn reset from DCSM

Note
If you re-purpose the reserved boot ROM RAM, the POR and XRS reset statuses won't be accurate.

Returns
Returns the reason(s) for a reset.

28.2.4.6 static void SysCtl_clearResetCause (uint32_t *rstCauses*) [inline], [static]

Clears reset reasons.

Parameters

rstCauses	are the reset causes to be cleared; must be a logical OR of **SYSCTL_CAUSE_POR**, **SYSCTL_CAUSE_XRS**, **SYSCTL_CAUSE_WDRS**, **SYSCTL_CAUSE_NMIWDRS**, and/or **SYSCTL_CAUSE_SCCRESET**.

This function clears the specified sticky reset reasons. Once cleared, another reset for the same reason can be detected, and a reset for a different reason can be distinguished (instead of having two reset causes set). If the reset reason is used by an application, all reset causes should be cleared after they are retrieved with SysCtl_getResetCause().

Note

Some reset causes are cleared by the boot ROM.

Returns

None.

28.2.4.7 static void SysCtl_setLowSpeedClock (**SysCtl_LSPCLKPrescaler** *prescaler*) [inline], [static]

Sets the low speed peripheral clock rate prescaler.

Parameters

prescaler	is the LSPCLK rate relative to SYSCLK

This function configures the clock rate of the low speed peripherals. The *prescaler* parameter is the value by which the SYSCLK rate is divided to get the LSPCLK rate. For example, a *prescaler* of **SYSCTL_LSPCLK_PRESCALE_4** will result in a LSPCLK rate that is a quarter of the SYSCLK rate.

Returns

None.

28.2.4.8 static void SysCtl_setEPWMClockDivider (**SysCtl_EPWMCLKDivider** *divider*) [inline], [static]

Sets the ePWM clock divider.

Parameters

divider	is the value by which PLLSYSCLK is divided

This function configures the clock rate of the EPWMCLK. The *divider* parameter is the value by which the SYSCLK rate is divided to get the EPWMCLK rate. For example, **SYSCTL_EPWMCLK_DIV_2** will select an EPWMCLK rate that is half the PLLSYSCLK rate.

Returns

None.

28.2.4.9 static void SysCtl_setEMIF1ClockDivider (**SysCtl_EMIF1CLKDivider** *divider*) [inline], [static]

Sets the EMIF1 clock divider.

Parameters

divider	is the value by which PLLSYSCLK (or CPU1.SYSCLK on a dual core device) is divided

This function configures the clock rate of the EMIF1CLK. The *divider* parameter is the value by which the SYSCLK rate is divided to get the EMIF1CLK rate. For example, **SYSCTL_EMIF1CLK_DIV_2** will select an EMIF1CLK rate that is half the PLLSYSCLK (or CPU1.SYSCLK on a dual core device) rate.

Returns
None.

References SYSCTL_EMIF1CLK_DIV_2.

28.2.4.10 static void SysCtl_setEMIF2ClockDivider (**SysCtl_EMIF2CLKDivider** *divider*) [inline], [static]

Sets the EMIF2 clock divider.

Parameters

divider	is the value by which PLLSYSCLK (or CPU1.SYSCLK on a dual core device) is divided

This function configures the clock rate of the EMIF2CLK. The *divider* parameter is the value by which the SYSCLK rate is divided to get the EMIF2CLK rate. For example, **SYSCTL_EMIF2CLK_DIV_2** will select an EMIF2CLK rate that is half the PLLSYSCLK (or CPU1.SYSCLK on a dual core device) rate.

Returns
None.

References SYSCTL_EMIF2CLK_DIV_2.

28.2.4.11 static void SysCtl_selectClockOutSource (**SysCtl_ClockOut** *source*) [inline], [static]

Selects a clock source to mux to an external GPIO pin (XCLKOUT).

Parameters

source	is the internal clock source to be configured.

This function configures the specified clock source to be muxed to an external clock out (XCLKOUT) GPIO pin. The *source* parameter may take a value of one of the following values:

- **SYSCTL_CLOCKOUT_PLLSYS**
- **SYSCTL_CLOCKOUT_PLLRAW**
- **SYSCTL_CLOCKOUT_SYSCLK**
- **SYSCTL_CLOCKOUT_INTOSC1**
- **SYSCTL_CLOCKOUT_INTOSC2**
- **SYSCTL_CLOCKOUT_XTALOSC**

Returns
None.

28.2.4.12 static uint16_t SysCtl_getExternalOscCounterValue (void) [inline], [static]

Gets the external oscillator counter value.

This function returns the X1 clock counter value. When the return value reaches 0x3FF, it freezes. Before switching from INTOSC2 to an external oscillator (XTAL), an application should call this function to make sure the counter is saturated.

Returns
Returns the value of the 10-bit X1 clock counter.

28.2.4.13 static void SysCtl_turnOnOsc (uint32_t *oscSource*) [inline], [static]

Turns on the specified oscillator sources.

Parameters

oscSource	is the oscillator source to be configured.

This function turns on the oscillator specified by the *oscSource* parameter which may take a value of **SYSCTL_OSCSRC_OSC2** or **SYSCTL_OSCSRC_XTAL**.

Note
SYSCTL_OSCSRC_OSC1 is not a valid value for *oscSource*.

Returns
None.

28.2.4.14 static void SysCtl_turnOffOsc (uint32_t *oscSource*) [inline], [static]

Turns off the specified oscillator sources.

Parameters

oscSource	is the oscillator source to be configured.

This function turns off the oscillator specified by the *oscSource* parameter which may take a value of **SYSCTL_OSCSRC_OSC2** or **SYSCTL_OSCSRC_XTAL**.

Note
SYSCTL_OSCSRC_OSC1 is not a valid value for *oscSource*.

Returns
None.

28.2.4.15 static void SysCtl_enterIdleMode (void) [inline], [static]

Enters IDLE mode.

This function puts the device into IDLE mode. The CPU clock is gated while all peripheral clocks are left running. Any enabled interrupt will wake the CPU up from IDLE mode.

Returns
None.

28.2.4.16 static void SysCtl_enterStandbyMode (void) [inline], [static]

Enters STANDBY mode.

This function puts the device into STANDBY mode. This will gate both the CPU clock and any peripheral clocks derived from SYSCLK. The watchdog is left active, and an NMI or an optional watchdog interrupt will wake the CPU subsystem from STANDBY mode.

GPIOs may be configured to wake the CPU subsystem. See SysCtl_enableLPMWakeupPin().

The CPU will receive an interrupt (WAKEINT) on wakeup.

Returns
None.

28.2.4.17 static void SysCtl_enterHaltMode (void) [inline], [static]

Enters HALT mode.

This function puts the device into HALT mode. This will gate almost all systems and clocks and allows for the power-down of oscillators and analog blocks. The watchdog may be left clocked to produce a reset. See SysCtl_enableWatchdogInHalt() to enable this. GPIOs should be configured to wake the CPU subsystem. See SysCtl_enableLPMWakeupPin().

Enter HALT mode (dual CPU). Puts CPU2 in IDLE mode first.

The CPU will receive an interrupt (WAKEINT) on wakeup.

Returns
None.

28.2.4.18 static void SysCtl_enterHibernateMode (void) [inline], [static]

Enters Hibernate mode.

This function puts the device into Hibernate mode. Hibernate (HIB) is a global low-power mode that gates the supply voltages to most of the system. This mode affects both CPU subsystems. HIB is essentially a controlled power-down with remote wakeup capability, and can be used to save power during long periods of inactivity.

To wake the device from HIB mode:

1. Assert the dedicated GPIOHIBWAKE pin (GPIO41) low to enable the power-up of the device clock sources.
2. Assert GPIOHIBWAKE pin high again. This triggers the power-up of the rest of the device.

To enter Hibernate mode in dual CPU put CPU2 in STANDBY mode first.

Returns
None.

28.2.4.19 static void SysCtl_enableLPMWakeupPin (uint32_t *pin*) [inline], [static]

Enables a pin to wake up the device from STANDBY or HALT.

Parameters

pin	is the identifying number of the pin.

This function connects a pin to the LPM circuit, allowing an event on the pin to wake up the device when when it is in STANDBY or HALT mode.

The pin is specified by its numerical value. For example, GPIO34 is specified by passing 34 as *pin*. Only GPIOs 0 through 63 are capable of being connected to the LPM circuit.

Returns
None.

28.2.4.20 static void SysCtl_disableLPMWakeupPin (uint32_t *pin*) [inline], [static]

Disables a pin to wake up the device from STANDBY or HALT.

Parameters

pin	is the identifying number of the pin.

This function disconnects a pin to the LPM circuit, disallowing an event on the pin to wake up the device when when it is in STANDBY or HALT mode.

The pin is specified by its numerical value. For example, GPIO34 is specified by passing 34 as *pin*. Only GPIOs 0 through 63 are valid.

Returns
None.

28.2.4.21 static void SysCtl_setStandbyQualificationPeriod (uint16_t *cycles*) [inline], [static]

Sets the number of cycles to qualify an input on waking from STANDBY mode.

Parameters

cycles	is the number of OSCCLK cycles.

This function sets the number of OSCCLK clock cycles used to qualify the selected inputs when waking from STANDBY mode. The *cycles* parameter should be passed a cycle count between 2 and 65 cycles inclusive.

Returns
None.

28.2.4.22 static void SysCtl_enableWatchdogStandbyWakeup (void) [inline], [static]

Enable the device to wake from STANDBY mode upon a watchdog interrupt.

Note
In order to use this option, you must configure the watchdog to generate an interrupt using SysCtl_setWatchdogMode().

Returns
None.

28.2.4.23 static void SysCtl_disableWatchdogStandbyWakeup (void) [inline], [static]

Disable the device from waking from STANDBY mode upon a watchdog interrupt.

Returns
None.

28.2.4.24 static void SysCtl_enableWatchdogInHalt (void) [inline], [static]

Enable the watchdog to run while in HALT mode.

This function configures the watchdog to continue to run while in HALT mode. Additionally, INTOSC1 and INTOSC2 are not powered down when the system enters HALT mode. By default the watchdog is gated when the system enters HALT.

Returns
None.

28.2.4.25 static void SysCtl_disableWatchdogInHalt (void) [inline], [static]

Disable the watchdog from running while in HALT mode.

This function gates the watchdog when the system enters HALT mode. INTOSC1 and INTOSC2 will be powered down. This is the default behavior of the device.

Returns
None.

28.2.4.26 static void SysCtl_setWatchdogMode (**SysCtl_WDMode** *mode*) [inline], [static]

Configures whether the watchdog generates a reset or an interrupt signal.

Parameters

mode	is a flag to select the watchdog mode.

This function configures the action taken when the watchdog counter reaches its maximum value. When the *mode* parameter is **SYSCTL_WD_MODE_INTERRUPT**, the watchdog is enabled to generate a watchdog interrupt signal and disables the generation of a reset signal. This will allow the watchdog module to wake up the device from IDLE or STANDBY if desired (see SysCtl_enableWatchdogStandbyWakeup()).

When the *mode* parameter is **SYSCTL_WD_MODE_RESET**, the watchdog will be put into reset mode and generation of a watchdog interrupt signal will be disabled. This is how the watchdog is configured by default.

Note
Check the status of the watchdog interrupt using SysCtl_isWatchdogInterruptActive() before calling this function. If the interrupt is still active, switching from interrupt mode to reset mode will immediately reset the device.

Returns
None.

References SYSCTL_WD_MODE_INTERRUPT.

28.2.4.27 static bool SysCtl_isWatchdogInterruptActive (void) [inline], [static]

Gets the status of the watchdog interrupt signal.

This function returns the status of the watchdog interrupt signal. If the interrupt is active, this function will return **true**. If **false**, the interrupt is NOT active.

Note
Make sure to call this function to ensure that the interrupt is not active before making any changes to the configuration of the watchdog to prevent any unexpected behavior. For instance, switching from interrupt mode to reset mode while the interrupt is active will immediately reset the device.

Returns
true if the interrupt is active and **false** if it is not.

28.2.4.28 static void SysCtl_disableWatchdog (void) [inline], [static]

Disables the watchdog.

This function disables the watchdog timer. Note that the watchdog timer is enabled on reset.

Returns
None.

28.2.4.29 static void SysCtl_enableWatchdog (void) [inline], [static]

Enables the watchdog.

This function enables the watchdog timer. Note that the watchdog timer is enabled on reset.

Returns
None.

28.2.4.30 static void SysCtl_serviceWatchdog (void) [inline], [static]

Services the watchdog.

This function resets the watchdog.

Returns
None.

Referenced by SysCtl_setClock().

28.2.4.31 static void SysCtl_setWatchdogPrescaler (**SysCtl_WDPrescaler** *prescaler*) [inline], [static]

Sets up watchdog clock (WDCLK) prescaler.

Parameters

prescaler	is the value that configures the watchdog clock relative to the value from the pre-divider.

This function sets up the watchdog clock (WDCLK) prescaler. The *prescaler* parameter divides INTOSC1 down to WDCLK.

Returns
None.

28.2.4.32 static uint16_t SysCtl_getWatchdogCounterValue (void) [inline], [static]

Gets the watchdog counter value.

Returns

Returns the current value of the 8-bit watchdog counter. If this count value overflows, a watchdog output pulse is generated.

28.2.4.33 static bool SysCtl_getWatchdogResetStatus (void) `[inline]`, `[static]`

Gets the watchdog reset status.

This function returns the watchdog reset status. If this function returns **true**, that indicates that a watchdog reset generated the last reset condition. Otherwise, it was an external device or power-up reset condition.

Returns

Returns **true** if the watchdog generated the last reset condition.

28.2.4.34 static void SysCtl_clearWatchdogResetStatus (void) `[inline]`, `[static]`

Clears the watchdog reset status.

This function clears the watchdog reset status. To check if it was set first, see SysCtl_getWatchdogResetStatus().

Returns

None.

28.2.4.35 static void SysCtl_setWatchdogWindowValue (uint16_t *value*) `[inline]`, `[static]`

Set the minimum threshold value for windowed watchdog

Parameters

value	is the value to set the window threshold

This function sets the minimum threshold value used to define the lower limit of the windowed watchdog functionality.

Returns

None.

28.2.4.36 static void SysCtl_enableNMIGlobalInterrupt (void) `[inline]`, `[static]`

Enable the NMI Global interrupt bit

Note: This bit should be set after the device security related initialization is complete.

Returns

None.

28.2.4.37 static bool SysCtl_getNMIStatus (void) `[inline]`, `[static]`

Read NMI interrupts.

Read the current state of NMI interrupt.

Returns

true if NMI interrupt is triggered, **false** if not.

28.2.4.38 static uint16_t SysCtl_getNMIFlagStatus (void) `[inline]`, `[static]`

Read NMI Flags.

Read the current state of individual NMI interrupts

Returns

Value of NMIFLG register. These defines are provided to decode the value:

- **SYSCTL_NMI_NMIINT** - Non-maskable interrupt
- **SYSCTL_NMI_CLOCKFAIL** - Clock Failure
- **SYSCTL_NMI_RAMUNCERR** - Uncorrectable RAM error
- **SYSCTL_NMI_FLUNCERR** - Uncorrectable Flash error
- **SYSCTL_NMI_PIEVECTERR** - PIE Vector Fetch Error
- **SYSCTL_NMI_CPU2WDRSN** - CPU2 WDRSn Reset
- **SYSCTL_NMI_CPU2NMIWDRSN** - CPU2 NMIWDRSn Reset

Referenced by SysCtl_clearAllNMIFlags().

28.2.4.39 static bool SysCtl_isNMIFlagSet (uint32_t *nmiFlags*) `[inline]`, `[static]`

Check if the individual NMI interrupts are set.

Parameters

nmiFlags	Bit mask of the NMI interrupts that user wants to clear. The bit format of this parameter is same as of the NMIFLG register. These defines are provided: ■ **SYSCTL_NMI_NMIINT** - Non-maskable interrupt ■ **SYSCTL_NMI_CLOCKFAIL** - Clock Failure ■ **SYSCTL_NMI_RAMUNCERR** - Uncorrectable RAM error ■ **SYSCTL_NMI_FLUNCERR** - Uncorrectable Flash error ■ **SYSCTL_NMI_PIEVECTERR** - PIE vector Fetch error ■ **SYSCTL_NMI_CPU2WDRSN** - CPU2 WDRSn Reset ■ **SYSCTL_NMI_CPU2NMIWDRSN** - CPU2 NMIWDRSn Reset

Check if interrupt flags corresponding to the passed in bit mask are asserted.

Returns

true if any of the NMI asked for in the parameter bit mask is set. **false** if none of the NMI requested in the parameter bit mask are set.

28.2.4.40 static void SysCtl_clearNMIStatus (uint32_t *nmiFlags*) [inline], [static]

Function to clear individual NMI interrupts.

Parameters

nmiFlags	Bit mask of the NMI interrupts that user wants to clear. The bit format of this parameter is same as of the NMIFLG register. These defines are provided: ■ **SYSCTL_NMI_CLOCKFAIL** ■ **SYSCTL_NMI_RAMUNCERR** ■ **SYSCTL_NMI_FLUNCERR** ■ **SYSCTL_NMI_PIEVECTERR** ■ **SYSCTL_NMI_CPU2WDRSN** ■ **SYSCTL_NMI_CPU2NMIWDRSN**

Clear NMI interrupt flags that correspond with the passed in bit mask.

Note: The NMI Interrupt flag is always cleared by default and therefore doesn't have to be included in the bit mask.

Returns

None.

28.2.4.41 static void SysCtl_clearAllNMIFlags (void) [inline], [static]

Clear all the NMI Flags that are currently set.

Returns

None.

References SysCtl_getNMIFlagStatus().

28.2.4.42 static void SysCtl_forceNMIFlags (uint32_t *nmiFlags*) [inline], [static]

Function to force individual NMI interrupt fail flags

Parameters

nmiFlags	Bit mask of the NMI interrupts that user wants to clear. The bit format of this parameter is same as of the NMIFLG register. These defines are provided: ■ **SYSCTL_NMI_CLOCKFAIL** ■ **SYSCTL_NMI_RAMUNCERR** ■ **SYSCTL_NMI_FLUNCERR** ■ **SYSCTL_NMI_PIEVECTERR** ■ **SYSCTL_NMI_CPU2WDRSN** ■ **SYSCTL_NMI_CPU2NMIWDRSN**

Returns
None.

28.2.4.43 static uint16_t SysCtl_getNMIWatchdogCounter (void) [inline], [static]

Gets the NMI watchdog counter value.

Note: The counter is clocked at the SYSCLKOUT rate.

Returns
Returns the NMI watchdog counter register's current value.

28.2.4.44 static void SysCtl_setNMIWatchdogPeriod (uint16_t *wdPeriod*) [inline], [static]

Sets the NMI watchdog period value.

Parameters

wdPeriod	is the 16-bit value at which a reset is generated.

This function writes to the NMI watchdog period register that holds the value to which the NMI watchdog counter is compared. When the two registers match, a reset is generated. By default, the period is 0xFFFF.

Note
If a value smaller than the current counter value is passed into the *wdPeriod* parameter, a NMIRSn will be forced.

Returns
None.

28.2.4.45 static uint16_t SysCtl_getNMIWatchdogPeriod (void) [inline], [static]

Gets the NMI watchdog period value.

Returns
Returns the NMI watchdog period register's current value.

28.2.4.46 static uint32_t SysCtl_getNMIShadowFlagStatus (void) [inline], [static]

Read NMI Shadow Flags.

Read the current state of individual NMI interrupts

Returns

Value of NMISHDFLG register. These defines are provided to decode the value:

- **SYSCTL_NMI_NMIINT** - Non-maskable interrupt
- **SYSCTL_NMI_CLOCKFAIL** - Clock Failure
- **SYSCTL_NMI_RAMUNCERR** - Uncorrectable RAM error
- **SYSCTL_NMI_FLUNCERR** - Uncorrectable Flash error
- **SYSCTL_NMI_PIEVECTERR** - PIE Vector Fetch Error
- **SYSCTL_NMI_CPU2WDRSN** - CPU2 WDRSn Reset
- **SYSCTL_NMI_CPU2NMIWDRSN** - CPU2 NMIWDRSn Reset

28.2.4.47 static bool SysCtl_isNMIShadowFlagSet (uint32_t *nmiFlags*) [inline], [static]

Check if the individual NMI shadow flags are set.

Parameters

nmiFlags	Bit mask of the NMI interrupts that user wants to clear. The bit format of this parameter is same as of the NMIFLG register. These defines are provided: ■ **SYSCTL_NMI_NMIINT** ■ **SYSCTL_NMI_CLOCKFAIL** ■ **SYSCTL_NMI_RAMUNCERR** ■ **SYSCTL_NMI_FLUNCERR** ■ **SYSCTL_NMI_PIEVECTERR** ■ **SYSCTL_NMI_CPU2WDRSN** ■ **SYSCTL_NMI_CPU2NMIWDRSN**

Check if interrupt flags corresponding to the passed in bit mask are asserted.

Returns

true if any of the NMI asked for in the parameter bit mask is set. **false** if none of the NMI requested in the parameter bit mask are set.

28.2.4.48 static void SysCtl_enableMCD (void) [inline], [static]

Enable the missing clock detection (MCD) Logic

Returns

None.

28.2.4.49 static void SysCtl_disableMCD (void) [inline], [static]

Disable the missing clock detection (MCD) Logic

Returns
None.

28.2.4.50 static bool SysCtl_isMCDClockFailureDetected (void) [inline], [static]

Get the missing clock detection Failure Status

Note
A failure means the oscillator clock is missing

Returns
Returns **true** if a failure is detected or **false** if a failure isn't detected

Referenced by SysCtl_getClock(), and SysCtl_setClock().

28.2.4.51 static void SysCtl_resetMCD (void) [inline], [static]

Reset the missing clock detection logic after clock failure

Returns
None.

28.2.4.52 static void SysCtl_connectMCDClockSource (void) [inline], [static]

Re-connect missing clock detection clock source to stop simulating clock failure

Returns
None.

28.2.4.53 static void SysCtl_disconnectMCDClockSource (void) [inline], [static]

Disconnect missing clock detection clock source to simulate clock failure. This is for testing the MCD functionality.

Returns
None.

28.2.4.54 static void SysCtl_setSyncInputConfig (**SysCtl_SyncInput** *syncInput,* **SysCtl_SyncInputSource** *syncSrc*) [inline], [static]

Configures the sync input source for the ePWM and eCAP signals.

Parameters

syncInput	is the sync input being configured
syncSrc	is sync input source selection.

This function configures the sync input source for the ePWM and eCAP modules. The *syncInput* parameter is the sync input being configured. It should be passed a value of **SYSCTL_SYNC_IN_XXXX**, where XXXX is the ePWM or eCAP instance the sync signal is entering.

The *syncSrc* parameter is the sync signal selected as the source of the sync input. It should be passed a value of **SYSCTL_SYNC_IN_SRC_XXXX**, XXXX is a sync signal coming from an ePWM, eCAP or external sync output. where For example, a *syncInput* value of **SYSCTL_SYNC_IN_ECAP1** and a *syncSrc* value of **SYSCTL_SYNC_IN_SRC_EPWM1SYNCOUT** will make the EPWM1SYNCOUT signal drive eCAP1's SYNCIN signal.

Note that some *syncSrc* values are only valid for certain values of *syncInput*. See device technical reference manual for details on time-base counter synchronization.

Returns
None.

28.2.4.55 static void SysCtl_setSyncOutputConfig (**SysCtl_SyncOutputSource** *syncSrc*) [inline], [static]

Configures the sync output source.

Parameters

syncSrc	is sync output source selection.

This function configures the sync output source from the ePWM modules. The *syncSrc* parameter is a value **SYSCTL_SYNC_OUT_SRC_XXXX**, where XXXX is a sync signal coming from an ePWM such as SYSCTL_SYNC_OUT_SRC_EPWM1SYNCOUT

Returns
None.

28.2.4.56 static void SysCtl_enableExtADCSOCSource (uint32_t *adcsocSrc*) [inline], [static]

Enables ePWM SOC signals to drive an external (off-chip) ADCSOC signal.

Parameters

adcsocSrc	is a bit field of the selected signals to be enabled

This function configures which ePWM SOC signals are enabled as a source for either ADCSOCAO or ADCSOCBO. The *adcsocSrc* parameter takes a logical OR of **SYSCTL_ADCSOC_SRC_PWMxSOCA/B** values that correspond to different signals.

Returns
None.

28.2.4.57 static void SysCtl_disableExtADCSOCSource (uint32_t *adcsocSrc*) [inline], [static]

Disables ePWM SOC signals from driving an external ADCSOC signal.

Parameters

adcsocSrc	is a bit field of the selected signals to be disabled

This function configures which ePWM SOC signals are disabled as a source for either ADCSOCAO or ADCSOCBO. The *adcsocSrc* parameter takes a logical OR of **SYSCTL_ADCSOC_SRC_PWMxSOCA/B** values that correspond to different signals.

Returns

None.

28.2.4.58 static void SysCtl_lockExtADCSOCSelect (void) [inline], [static]

Locks the SOC Select of the Trig X-BAR.

This function locks the external ADC SOC select of the Trig X-BAR.

Returns

None.

28.2.4.59 static void SysCtl_selectSecMaster (uint16_t *periFrame1Config,* uint16_t *periFrame2Config*) [inline], [static]

Configures whether the dual ported bridge is connected with DMA or CLA as the secondary master.

Parameters

per-iFrame1Config	indicates whether CLA or DMA is configured as secondary master on peripheral frame 1.
per-iFrame2Config	indicates whether CLA or DMA is configured as secondary master on peripheral frame 2.

One of the following values can be passed as parameter. **SYSCTL_SEC_MASTER_CLA SYSCTL_SEC_MASTER_DMA**

Returns

None.

28.2.4.60 static void SysCtl_lockSyncSelect (void) [inline], [static]

Locks the Sync Select of the Trig X-BAR.

This function locks Sync Input and Output Select of the Trig X-BAR.

Returns

None.

28.2.4.61 static void SysCtl_selectCPUForPeripheral (**SysCtl_CPUSelPeripheral** *peripheral,* uint16_t *peripheralInst,* **SysCtl_CPUSel** *cpuInst*) `[inline]`, `[static]`

Configures whether a peripheral is connected to CPU1 or CPU2.

Parameters

peripheral	is the peripheral for which CPU needs to be configured.
peripheralInst	is the instance for which CPU needs to be configured.
cpuInst	is the CPU to which the peripheral instance need to be connected.

The *peripheral* parameter can have one enumerated value from SysCtl_CPUSelPeripheral

The *peripheralInst* parameter is the instance number for example 1 for EPWM1, 2 for EPWM2 so on.For instances which are named with alphabets (instead of numbers) the following convention needs to be followed. 1 for A (SPI_A), 2 for B (SPI_B), 3 for C (SPI_C) so on...

The *cpuInst* parameter can have one the following values:

- **SYSCTL_CPUSEL_CPU1** - to connect to CPU1
- **SYSCTL_CPUSEL_CPU2** - to connect to CPU2

Note

This API is applicable only for the CPU1 subsystem.

Returns

None.

References SYSCTL_CPUSEL14_DAC.

28.2.4.62 static uint32_t SysCtl_getDeviceRevision (void) [inline], [static]

Get the Device Silicon Revision ID

This function returns the silicon revision ID for the device.

Note

This API is applicable only for the CPU1 subsystem.

Returns

Returns the silicon revision ID value.

28.2.4.63 void SysCtl_delay (uint32_t *count*)

Delays for a fixed number of cycles.

Parameters

count	is the number of delay loop iterations to perform.

This function generates a constant length delay using assembly code. The loop takes 5 cycles per iteration plus 9 cycles of overhead.

Note

If count is equal to zero, the loop will underflow and run for a very long time.

Returns

None.

Referenced by CAN_initModule(), SysCtl_setAuxClock(), and SysCtl_setClock().

28.2.4.64 uint32_t SysCtl_getClock (uint32_t *clockInHz*)

Calculates the system clock frequency (SYSCLK).

Parameters

clockInHz	is the frequency of the oscillator clock source (OSCCLK).

This function determines the frequency of the system clock based on the frequency of the oscillator clock source (from *clockInHz*) and the PLL and clock divider configuration registers.

Returns

Returns the system clock frequency. If a missing clock is detected, the function will return the INTOSC1 frequency. This needs to be corrected and cleared (see SysCtl_resetMCD()) before trying to call this function again.

References SysCtl_isMCDClockFailureDetected().

Referenced by SysCtl_getLowSpeedClock().

28.2.4.65 uint32_t SysCtl_getAuxClock (uint32_t *clockInHz*)

Calculates the system auxiliary clock frequency (AUXPLLCLK).

Parameters

clockInHz	is the frequency of the oscillator clock source (AUXOSCCLK).

This function determines the frequency of the auxiliary clock based on the frequency of the oscillator clock source (from *clockInHz*) and the AUXPLL and clock divider configuration registers.

Returns

Returns the auxiliary clock frequency.

28.2.4.66 bool SysCtl_setClock (uint32_t *config*)

Configures the clocking of the device.

Parameters

config	is the required configuration of the device clocking.

This function configures the clocking of the device. The input crystal frequency, oscillator to be used, use of the PLL, and the system clock divider are all configured with this function.

The *config* parameter is the OR of several different values, many of which are grouped into sets where only one can be chosen.

- The system clock divider is chosen with the macro **SYSCTL_SYSDIV(x)** where x is either 1 or an even value up to 126.
- The use of the PLL is chosen with either **SYSCTL_PLL_ENABLE** or **SYSCTL_PLL_DISABLE**.
- The integer multiplier is chosen **SYSCTL_IMULT(x)** where x is a value from 1 to 127.
- The fractional multiplier is chosen with either **SYSCTL_FMULT_0**, **SYSCTL_FMULT_1_4**, **SYSCTL_FMULT_1_2**, or **SYSCTL_FMULT_3_4**.
- The oscillator source chosen with **SYSCTL_OSCSRC_OSC2**, **SYSCTL_OSCSRC_XTAL**, or **SYSCTL_OSCSRC_OSC1**.

This function uses the watchdog as a monitor for the PLL. The user watchdog settings will be modified and restored upon completion. Make sure that the WDOVERRIDE bit isn't set before calling this function. Re-lock attempt is carried out if either SLIP condition occurs or SYSCLK to input clock ratio is off by 10%.

This function uses the following resources to support PLL initialization:

- Watchdog
- CPU Timer 1
- CPU Timer 2

Note

See your device errata for more details about locking the PLL.

Returns

Returns **false** if a missing clock error is detected. This needs to be cleared (see SysCtl_resetMCD()) before trying to call this function again. Otherwise, returns **true**.

References SysCtl_delay(), SysCtl_isMCDClockFailureDetected(), SysCtl_selectOscSource(), and SysCtl_serviceWatchdog().

28.2.4.67 void SysCtl_selectOscSource (uint32_t *oscSource*)

Selects the oscillator to be used for the clocking of the device.

Parameters

oscSource	is the oscillator source to be configured.

This function configures the oscillator to be used in the clocking of the device. The *oscSource* parameter may take a value of **SYSCTL_OSCSRC_OSC2**, **SYSCTL_OSCSRC_XTAL**, or **SYSCTL_OSCSRC_OSC1**.

See Also

SysCtl_turnOnOsc()

Returns

None.

Referenced by SysCtl_setClock().

28.2.4.68 uint32_t SysCtl_getLowSpeedClock (uint32_t *clockInHz*)

Calculates the low-speed peripheral clock frequency (LSPCLK).

Parameters

clockInHz	is the frequency of the oscillator clock source (OSCCLK).

This function determines the frequency of the low-speed peripheral clock based on the frequency of the oscillator clock source (from *clockInHz*) and the PLL and clock divider configuration registers.

Returns

Returns the low-speed peripheral clock frequency.

References SysCtl_getClock().

28.2.4.69 uint16_t SysCtl_getDeviceParametric (**SysCtl_DeviceParametric** *parametric*)

Get the device part parametric value

Parameters

parametric	is the requested device parametric value

This function gets the device part parametric value.

The *parametric* parameter can have one the following enumerated values:

- **SYSCTL_DEVICE_QUAL** - Device Qualification Status
- **SYSCTL_DEVICE_PINCOUNT** - Device Pin Count
- **SYSCTL_DEVICE_INSTASPIN** - Device InstaSPIN Feature Set
- **SYSCTL_DEVICE_FLASH** - Device Flash size (KB)
- **SYSCTL_DEVICE_PARTID** - Device PARTID Format Revision
- **SYSCTL_DEVICE_FAMILY** - Device Family
- **SYSCTL_DEVICE_PARTNO** - Device Part Number
- **SYSCTL_DEVICE_CLASSID** - Device Class ID

Note

This API is applicable only for the CPU1 subsystem.

Returns

Returns the specified parametric value.

References SYSCTL_DEVICE_CLASSID, SYSCTL_DEVICE_FAMILY, SYSCTL_DEVICE_FLASH, SYSCTL_DEVICE_INSTASPIN, SYSCTL_DEVICE_PARTID, SYSCTL_DEVICE_PARTNO, SYSCTL_DEVICE_PINCOUNT, and SYSCTL_DEVICE_QUAL.

28.2.4.70 void SysCtl_setAuxClock (uint32_t *config*)

Configures the auxiliary PLL for clocking USB.

Parameters

config	is the required configuration of the device clocking.

This function configures the clock source for auxiliary PLL, the integer multiplier, fractional multiplier and divider.

The *config* parameter is the OR of several different values, many of which are grouped into sets where only one can be chosen.

- The system clock divider is chosen with one of the following macros: **SYSCTL_AUXPLL_DIV_1**, **SYSCTL_AUXPLL_DIV_2**, **SYSCTL_AUXPLL_DIV_4**, **SYSCTL_AUXPLL_DIV_8**

- The use of the PLL is chosen with either **SYSCTL_AUXPLL_ENABLE** or **SYSCTL_AUXPLL_DISABLE**.
- The integer multiplier is chosen with **SYSCTL_AUXPLL_IMULT(x)** where x is a value from 1 to 127.
- The oscillator source chosen with one of **SYSCTL_AUXPLL_OSCSRC_OSC2**, **SYSCTL_AUXPLL_OSCSRC_XTAL**, **SYSCTL_AUXPLL_OSCSRC_AUXCLKIN**,

Note

This function uses CPU Timer 2 to monitor a successful lock of the AUXPLL. For this function to properly detect the PLL startup SYSCLK $>=$ 2$*$AUXPLLCLK after the AUXPLL is selected as the clocking source. User configuration of CPU Timer 2 will be backed up and restored. See your device errata for more details about locking the PLL.

Returns

None.

References SysCtl_delay().

29 UPP Module

29.1 UPP Introduction

The universal parallel port (UPP) API provides a set of functions to configure device's UPP module. The driver provides functions to initialize the module, obtain status information and to manage interrupts. Both transmitter and receiver modes are supported.

29.2 API Functions

Data Structures

- struct UPP_DMADescriptor
- struct UPP_DMAChannelStatus

Macros

- #define UPP_INT_CHI_DMA_PROG_ERR
- #define UPP_INT_CHI_UNDER_OVER_RUN
- #define UPP_INT_CHI_END_OF_WINDOW
- #define UPP_INT_CHI_END_OF_LINE
- #define UPP_INT_CHQ_DMA_PROG_ERR
- #define UPP_INT_CHQ_UNDER_OVER_RUN
- #define UPP_INT_CHQ_END_OF_WINDOW
- #define UPP_INT_CHQ_END_OF_LINE

Enumerations

- enum UPP_EmulationMode { UPP_EMULATIONMODE_HARDSTOP, UPP_EMULATIONMODE_RUNFREE, UPP_EMULATIONMODE_SOFTSTOP }
- enum UPP_OperationMode { UPP_RECEIVE_MODE, UPP_TRANSMIT_MODE }
- enum UPP_DataRate { UPP_DATA_RATE_SDR, UPP_DATA_RATE_DDR }
- enum UPP_TxSDRInterleaveMode { UPP_TX_SDR_INTERLEAVE_DISABLE, UPP_TX_SDR_INTERLEAVE_ENABLE }
- enum UPP_DDRDemuxMode { UPP_DDR_DEMUX_DISABLE, UPP_DDR_DEMUX_ENABLE }
- enum UPP_SignalPolarity { UPP_SIGNAL_POLARITY_HIGH, UPP_SIGNAL_POLARITY_LOW }
- enum UPP_SignalMode { UPP_SIGNAL_DISABLE, UPP_SIGNAL_ENABLE }
- enum UPP_ClockPolarity { UPP_CLK_NOT_INVERTED, UPP_CLK_INVERTED }
- enum UPP_TxIdleDataMode { UPP_TX_IDLE_DATA_IDLE, UPP_TX_IDLE_DATA_TRISTATED }
- enum UPP_DMAChannel { UPP_DMA_CHANNEL_I, UPP_DMA_CHANNEL_Q }

- enum UPP_ThresholdSize { UPP_THR_SIZE_64BYTE, UPP_THR_SIZE_128BYTE, UPP_THR_SIZE_256BYTE }
- enum UPP_InputDelay { UPP_INPUT_DLY_4, UPP_INPUT_DLY_6, UPP_INPUT_DLY_9, UPP_INPUT_DLY_14 }

Functions

- static bool UPP_isDMAActive (uint32_t base)
- static void UPP_performSoftReset (uint32_t base)
- static void UPP_enableModule (uint32_t base)
- static void UPP_disableModule (uint32_t base)
- static void UPP_enableEmulationMode (uint32_t base)
- static void UPP_disableEmulationMode (uint32_t base)
- static void UPP_setEmulationMode (uint32_t base, UPP_EmulationMode emuMode)
- static void UPP_setOperationMode (uint32_t base, UPP_OperationMode opMode)
- static void UPP_setDataRate (uint32_t base, UPP_DataRate dataRate)
- static void UPP_setTxSDRInterleaveMode (uint32_t base, UPP_TxSDRInterleaveMode mode)
- static void UPP_setDDRDemuxMode (uint32_t base, UPP_DDRDemuxMode mode)
- static void UPP_setControlSignalPolarity (uint32_t base, UPP_SignalPolarity waitPola, UPP_SignalPolarity enablePola, UPP_SignalPolarity startPola)
- static void UPP_setTxControlSignalMode (uint32_t base, UPP_SignalMode waitMode)
- static void UPP_setRxControlSignalMode (uint32_t base, UPP_SignalMode enableMode, UPP_SignalMode startMode)
- static void UPP_setTxClockDivider (uint32_t base, uint16_t divider)
- static void UPP_setClockPolarity (uint32_t base, UPP_ClockPolarity clkPolarity)
- static void UPP_configTxIdleDataMode (uint32_t base, UPP_TxIdleDataMode config)
- static void UPP_setTxIdleValue (uint32_t base, uint16_t idleVal)
- static void UPP_setTxThreshold (uint32_t base, UPP_ThresholdSize size)
- static void UPP_enableInterrupt (uint32_t base, uint16_t intFlags)
- static void UPP_disableInterrupt (uint32_t base, uint16_t intFlags)
- static uint16_t UPP_getInterruptStatus (uint32_t base)
- static uint16_t UPP_getRawInterruptStatus (uint32_t base)
- static void UPP_clearInterruptStatus (uint32_t base, uint16_t intFlags)
- static void UPP_enableGlobalInterrupt (uint32_t base)
- static void UPP_disableGlobalInterrupt (uint32_t base)
- static bool UPP_isInterruptGenerated (uint32_t base)
- static void UPP_clearGlobalInterruptStatus (uint32_t base)
- static void UPP_enableInputDelay (uint32_t base)
- static void UPP_disableInputDelay (uint32_t base)
- static void UPP_setInputDelay (uint32_t base, UPP_InputDelay delay)
- void UPP_setDMAReadThreshold (uint32_t base, UPP_DMAChannel channel, UPP_ThresholdSize size)
- void UPP_setDMADescriptor (uint32_t base, UPP_DMAChannel channel, const UPP_DMADescriptor ∗const desc)
- void UPP_getDMAChannelStatus (uint32_t base, UPP_DMAChannel channel, UPP_DMAChannelStatus ∗const status)
- bool UPP_isDescriptorPending (uint32_t base, UPP_DMAChannel channel)
- bool UPP_isDescriptorActive (uint32_t base, UPP_DMAChannel channel)
- uint16_t UPP_getDMAFIFOWatermark (uint32_t base, UPP_DMAChannel channel)
- void UPP_readRxMsgRAM (uint32_t rxBase, uint16_t array[ ], uint16_t length, uint16_t offset)
- void UPP_writeTxMsgRAM (uint32_t txBase, const uint16_t array[ ], uint16_t length, uint16_t offset)

29.2.1 Detailed Description

The UPP API includes functions to enable/disable uPP module, perform software reset, configure uPP as Transmitter or Receiver, set data rate to SDR or DDR, set interleaving demultiplexing configurations, set control signal polarities, enable/disable optional control signals, set Tx clock value polarity, configure idle Tx dataline values, enable/disable, clear get status for uPP interrupts.

The code for this module is contained in `driverlib/upp.c`, with `driverlib/upp.h` containing the API declarations for use by applications.

29.2.2 Enumeration Type Documentation

29.2.2.1 enum **UPP_EmulationMode**

Values that can be passed to UPP_setEmulationMode() as *emuMode* parameter.

Enumerator

UPP_EMULATIONMODE_HARDSTOP uPP stops immediately
UPP_EMULATIONMODE_RUNFREE uPP unaffected by suspend
UPP_EMULATIONMODE_SOFTSTOP uPP stops at DMA transaction finish

29.2.2.2 enum **UPP_OperationMode**

Values that can be passed to UPP_setOperationMode() as *opMode* parameter.

Enumerator

UPP_RECEIVE_MODE uPP to be configured as Receiver
UPP_TRANSMIT_MODE uPP to be configured as Transmitter

29.2.2.3 enum **UPP_DataRate**

Values that can be passed to UPP_setDataRate() as *dataRate* parameter.

Enumerator

UPP_DATA_RATE_SDR uPP to operate in Single Data Rate Mode
UPP_DATA_RATE_DDR uPP to operate in Double Data Rate Mode

29.2.2.4 enum **UPP_TxSDRInterleaveMode**

Values that can be passed to UPP_setTxSDRInterleaveMode() as *mode* parameter.

Enumerator

UPP_TX_SDR_INTERLEAVE_DISABLE Interleaving disabled in Tx SDR.
UPP_TX_SDR_INTERLEAVE_ENABLE Interleaving enabled in Tx SDR.

29.2.2.5 enum **UPP_DDRDemuxMode**

Values that can be passed to UPP_setDDRDemuxMode() as *mode* parameter.

Enumerator

UPP_DDR_DEMUX_DISABLE Demultiplexing disabled in DDR mode.

UPP_DDR_DEMUX_ENABLE Demultiplexing enabled in DDR mode.

29.2.2.6 enum **UPP_SignalPolarity**

Values that can be passed to UPP_setControlSignalPolarity() as *waitPola*, *enablePola* & *startPola* parameters.

Enumerator

UPP_SIGNAL_POLARITY_HIGH Signal polarity is active high.

UPP_SIGNAL_POLARITY_LOW Signal polarity is active low.

29.2.2.7 enum **UPP_SignalMode**

Values that can be passed to UPP_setTxControlSignalMode() & UPP_setRxControlSignalMode() as *waitMode* & *startMode*, *enableMode* parameters respectively.

Enumerator

UPP_SIGNAL_DISABLE Control Signal is disabled for uPP.

UPP_SIGNAL_ENABLE Control Signal is enabled for uPP.

29.2.2.8 enum **UPP_ClockPolarity**

Values that can be passed to UPP_setClockPolarity() as *clkPolarity* parameter.

Enumerator

UPP_CLK_NOT_INVERTED uPP Clock is not inverted

UPP_CLK_INVERTED uPP clock is inverted

29.2.2.9 enum **UPP_TxIdleDataMode**

Values that can be passed to UPP_configTxIdleDataMode() as *config* parameter. It specifies whether the data lines will drive idle value or get tri-stated when uPP goes to idle state.

Enumerator

UPP_TX_IDLE_DATA_IDLE Data lines will drive idle val.

UPP_TX_IDLE_DATA_TRISTATED Data lines will be tristated.

29.2.2.10 enum **UPP_DMAChannel**

Values that can be passed to UPP_setDMAReadThreshold(), UPP_getDMAChannelStatus(), UPP_setDMADescriptor(), UPP_isDescriptorPending(), UPP_isDescriptorActive() & UPP_getDMAFIFOWatermark() as *channel* parameter.

Enumerator

UPP_DMA_CHANNEL_I uPP internal DMA channel I

UPP_DMA_CHANNEL_Q uPP internal DMA channel Q

29.2.2.11 enum **UPP_ThresholdSize**

Values that can be passed to UPP_setTxThreshold() and UPP_setDMAReadThreshold() as *size* parameter.

Enumerator

UPP_THR_SIZE_64BYTE Tx threshold size is 64 bytes.

UPP_THR_SIZE_128BYTE Tx threshold size is 128 bytes.

UPP_THR_SIZE_256BYTE Tx threshold size is 256 bytes.

29.2.2.12 enum **UPP_InputDelay**

Values that can be passed to UPP_setInputDelay() as *delay* parameter. All the following values lead to 2 cycle delay on clock pin.

Enumerator

UPP_INPUT_DLY_4 4 cycle delay for data & control pins

UPP_INPUT_DLY_6 6 cycle delay for data & control pins

UPP_INPUT_DLY_9 9 cycle delay for data & control pins

UPP_INPUT_DLY_14 14 cycle delay for data & control pins

29.2.3 Function Documentation

29.2.3.1 static bool UPP_isDMAActive (uint32_t *base*) [inline], [static]

Returns uPP internal DMA state machine status.

Parameters

base	is the configuration address of the uPP instance used.

This function returns whether the uPP internal DMA state machine status is idle or burst transaction is active.

Returns

Returns the DMA machine status. It can return following values:

- **true** - DMA burst transaction is active
- **false** - DMA is idle

29.2.3.2 static void UPP_performSoftReset (uint32_t *base*) [inline], [static]

Resets the uPP module.

Parameters

base	is the configuration address of the uPP instance used.

This function initiates software reset in uPP.

Returns
None.

29.2.3.3 static void UPP_enableModule (uint32_t *base*) [inline], [static]

Enables the uPP module.

Parameters

base	is the configuration address of the uPP instance used.

This function enables the uPP module.

Returns
None.

29.2.3.4 static void UPP_disableModule (uint32_t *base*) [inline], [static]

Disables the uPP module.

Parameters

base	is the configuration address of the uPP instance used.

This function disables the uPP module.

Returns
None.

29.2.3.5 static void UPP_enableEmulationMode (uint32_t *base*) [inline], [static]

Enables real time emulation mode for uPP module.

Parameters

base	is the configuration address of the uPP instance used.

This function enables real time emulation mode in uPP module.

Returns
None.

29.2.3.6 static void UPP_disableEmulationMode (uint32_t *base*) [inline], [static]

Disables real time emulation mode for uPP module.

Parameters

base	is the configuration address of the uPP instance used.

This function disables real time emulation mode for uPP module.

Returns
None.

29.2.3.7 static void UPP_setEmulationMode (uint32_t *base*, **UPP_EmulationMode** *emuMode*) [inline], [static]

Sets the emulation mode for the uPP module.

Parameters

base	is the configuration address of the uPP instance used.
emuMode	is the mode of operation upon an emulation suspend.

This function sets the uPP module's emulation mode. This mode determines how the uPP module is affected by an emulation suspend. Valid values for *emuMode* parameter are the following:

- **UPP_EMULATIONMODE_HARDSTOP** - The uPP module stops immediately.
- **UPP_EMULATIONMODE_RUNFREE** - The uPP module is unaffected by an emulation suspend.
- **UPP_EMULATIONMODE_SOFTSTOP** - The uPP module stops after completing current DMA burst transaction.

Returns
None.

29.2.3.8 static void UPP_setOperationMode (uint32_t *base*, **UPP_OperationMode** *opMode*) [inline], [static]

Sets uPP mode of operation.

Parameters

base	is the configuration address of the uPP instance used.
opMode	is mode of operation for uPP module.

This function sets the uPP mode of opeartion. The *opMode* parameter determines whether uPP module should be configured as transmitter or receiver. It should be passed any of the following values:

- **UPP_RECEIVE_MODE** - uPP is to be operated in Rx mode.
- **UPP_TRANSMIT_MODE** - uPP is to be operated in Tx mode.

Returns
None.

29.2.3.9 static void UPP_setDataRate (uint32_t *base*, **UPP_DataRate** *dataRate*) `[inline]`, `[static]`

Sets uPP data rate mode.

Parameters

base	is the configuration address of the uPP instance used.
dataRate	is the required uPP data rate mode.

This function sets the data rate mode for uPP module as single data rate or double data rate mode. It should be passed any of the following values:

- **UPP_DATA_RATE_SDR** - uPP is to be operated in single data rate mode.
- **UPP_DATA_RATE_DDR** - uPP is to be operated in double data rate mode.

Returns
None.

29.2.3.10 static void UPP_setTxSDRInterleaveMode (uint32_t *base*, **UPP_TxSDRInterleaveMode** *mode*) [inline], [static]

Sets Tx SDR interleave mode for uPP module.

Parameters

base	is the configuration address of the uPP instance used.
mode	is the required SDR interleave mode.

This function sets the required interleave mode for SDR Tx uPP. It is valid only for Tx SDR mode & not for Rx SDR mode. The *mode* parameter determines whether interleaving should be enabled or disabled for SDR Tx uPP mode. It should be passed any of the following values:

- **UPP_TX_SDR_INTERLEAVE_DISABLE** - specifies interleaving is disabled
- **UPP_TX_SDR_INTERLEAVE_ENABLE** - specifies interleaving is enabled

Returns
None.

29.2.3.11 static void UPP_setDDRDemuxMode (uint32_t *base*, **UPP_DDRDemuxMode** *mode*) [inline], [static]

Sets DDR de-multiplexing mode for uPP module.

Parameters

base	is the configuration address of the uPP instance used.
mode	is the required DDR de-multiplexing mode.

This function sets the demultiplexing mode for uPP DDR mode. The *mode* parameter determines whether demuliplexing to enabled or disabled in DDR mode. It should take following values:

- **UPP_DDR_DEMUX_DISABLE** - specifies demultiplexing is disabled
- **UPP_DDR_DEMUX_ENABLE** - specifies demultiplexing is enabled

Returns
None.

29.2.3.12 static void UPP_setControlSignalPolarity (uint32_t *base*, **UPP_SignalPolarity** *waitPola*, **UPP_SignalPolarity** *enablePola*, **UPP_SignalPolarity** *startPola*) [inline], [static]

Sets control signal polarity for uPP module.

Parameters

base	is the configuration address of the uPP instance used.
waitPola	is the required wait signal polarity.
enablePola	is the required enable signal polarity.
startPola	is the required start signal polarity.

This function sets the control signal polarity for uPP module. The *waitPola*, *enablePola*, *startPola* parameters determines the control signal polarities. Valid values for these parameters are the following:

- **UPP_SIGNAL_POLARITY_HIGH** - Signal polarity to be set as active high.
- **UPP_SIGNAL_POLARITY_LOW** - Signal polarity to be set as active low.

Returns
None.

29.2.3.13 static void UPP_setTxControlSignalMode (uint32_t *base*, **UPP_SignalMode** *waitMode*) [inline], [static]

Sets the mode for optional control signals for uPP module in Tx mode.

Parameters

base	is the configuration address of the uPP instance used.
waitMode	is the required mode for wait signal.

This function sets the mode for optional control signals in Tx mode for uPP module. The *waitMode* parameter determine whether the wait signal is to be enabled or disabled while uPP is in transmit mode. It can take following values:

- **UPP_SIGNAL_DISABLE** - Wait signal will be disabled.
- **UPP_SIGNAL_ENABLE** - Wait signal will be enabled.

Returns
None.

29.2.3.14 static void UPP_setRxControlSignalMode (uint32_t *base*, **UPP_SignalMode** *enableMode*, **UPP_SignalMode** *startMode*) [inline], [static]

Sets the mode for optional control signals for uPP module in Rx mode.

Parameters

base	is the configuration address of the uPP instance used.
enableMode	is the required mode for enable signal.
startMode	is the required mode for start signal.

This function sets the mode for optional control signal mode in Rx mode for uPP module.The *enableMode* & *startMode* parameter determine whether the enable & start signals are to be enabled or disabled while uPP is in receive mode. These can take following values:

- **UPP_SIGNAL_DISABLE** - Signal will be disabled.

- **UPP_SIGNAL_ENABLE** - Signal will be enabled.

Returns
None.

29.2.3.15 static void UPP_setTxClockDivider (uint32_t *base*, uint16_t *divider*) [inline], [static]

Sets the clock divider when uPP is in Tx mode.

Parameters

base	is the configuration address of the uPP instance used.
divider	is the value by which PLLSYSCLK (or CPU1.SYSCLK on a dual core device) is divided.

This function configures the clock rate of uPP when it is operating in Tx mode. The *divider* parameter is the value by which SYSCLK rate is divided to get the desired uPP Tx clock rate.

Returns
None.

29.2.3.16 static void UPP_setClockPolarity (uint32_t *base*, **UPP_ClockPolarity** *clkPolarity*) [inline], [static]

Sets the uPP clock polarity.

Parameters

base	is the configuration address of the uPP instance used.
clkPolarity	is the required clock polarity.

This function sets the uPP clock polarity. The *clkPolarity* parameter in Tx mode determines whether output Tx clock is to be inverted or not, while in Rx mode it determines whether the Rx input clock is to be treated as inverted or not.

Returns
None.

29.2.3.17 static void UPP_configTxIdleDataMode (uint32_t *base*, **UPP_TxIdleDataMode** *config*) [inline], [static]

Configures data line behaviour when uPP goes to idle state in Tx mode.

Parameters

base	is the configuration address of the uPP instance used.
config	is the required idle mode data line behaviour.

This function configures the Tx mode data line behaviour in uPP. The *config* determines whether tri-state is enabled or disabled for uPP idlle time. It can take following values:

- **UPP_TX_IDLE_DATA_IDLE** - uPP will drive idle values to data lines when it goes to idle mode while operating in Tx mode.
- **UPP_TX_IDLE_DATA_TRISTATED** - uPP will tri-state data lines when it goes to idle mode while operating in Tx mode.

Returns
None.

29.2.3.18 static void UPP_setTxIdleValue (uint32_t *base*, uint16_t *idleVal*) [inline], [static]

Sets idle value to be driven by data line when uPP goes to idle state when operating in Tx mode.

Parameters

base	is the configuration address of the uPP instance used.
idleVal	is the required idle value to be driven in Tx idle state.

This function sets idle value to be driven in idle state while uPP is operating in Tx mode. The parameter *idleVal* is the value to be driven *when* Tx uPP is in idle state.

Returns
None.

29.2.3.19 static void UPP_setTxThreshold (uint32_t *base*, **UPP_ThresholdSize** *size*) [inline], [static]

Sets the I/O transmit threshold.

Parameters

base	is the configuration address of the uPP instance used.
size	is the required Tx threshold size in bytes.

This function sets the i/o transmit threshold. The *size* parameter determines the required size for the threshold to reach in transmit buffer before the tranmission begins. It can take following values:

- **UPP_THR_SIZE_64BYTE** - Sets the Tx threshold to 64 bytes.
- **UPP_THR_SIZE_128BYTE** - Sets the Tx threshold to 128 bytes.
- **UPP_THR_SIZE_256BYTE** - Sets the Tx threshold to 256 bytes.

Returns
None.

29.2.3.20 static void UPP_enableInterrupt (uint32_t *base*, uint16_t *intFlags*) [inline], [static]

Enables individual uPP module interrupts.

Parameters

base	is the configuration address of the uPP instance used.
intFlags	is a bit mask of the interrupt sources to be enabled.

This function enables uPP module interrupt sources. The *intFlags* parameter can be any of the following values OR'd together:

- **UPP_INT_CHI_DMA_PROG_ERR** - DMA Channel I Programming Error
- **UPP_INT_CHI_UNDER_OVER_RUN** - DMA Channel I Underrun/Overrun
- **UPP_INT_CHI_END_OF_WINDOW** - DMA Channel I End of Window Event
- **UPP_INT_CHI_END_OF_LINE** - DMA Channel I End of Line Event
- **UPP_INT_CHQ_DMA_PROG_ERR** - DMA Channel Q Programming Error
- **UPP_INT_CHQ_UNDER_OVER_RUN** - DMA Channel Q Underrun/Overrun
- **UPP_INT_CHQ_END_OF_WINDOW** - DMA Channel Q End of Window Event
- **UPP_INT_CHQ_END_OF_LINE** - DMA Channel Q End of Line Event

Returns

None.

29.2.3.21 static void UPP_disableInterrupt (uint32_t *base*, uint16_t *intFlags*) `[inline]`, `[static]`

Disables individual uPP module interrupts.

Parameters

base	is the configuration address of the uPP instance used.
intFlags	is a bit mask of the interrupt sources to be disabled.

This function disables uPP module interrupt sources. The *intFlags* parameter can be any of the following values OR'd together:

- **UPP_INT_CHI_DMA_PROG_ERR** - DMA Channel I Programming Error
- **UPP_INT_CHI_UNDER_OVER_RUN** - DMA Channel I Underrun/Overrun
- **UPP_INT_CHI_END_OF_WINDOW** - DMA Channel I End of Window Event
- **UPP_INT_CHI_END_OF_LINE** - DMA Channel I End of Line Event
- **UPP_INT_CHQ_DMA_PROG_ERR** - DMA Channel Q Programming Error
- **UPP_INT_CHQ_UNDER_OVER_RUN** - DMA Channel Q Underrun/Overrun
- **UPP_INT_CHQ_END_OF_WINDOW** - DMA Channel Q End of Window Event
- **UPP_INT_CHQ_END_OF_LINE** - DMA Channel Q End of Line Event

Returns

None.

29.2.3.22 static uint16_t UPP_getInterruptStatus (uint32_t *base*) `[inline]`, `[static]`

Gets the current uPP interrupt status for enabled interrupts.

Parameters

base	is the configuration address of the uPP instance used.

This function returns the interrupt status of enabled interrupts for the uPP module.

Returns

Returns current interrupt status for enabled interrupts, enumerated as a bit field of any of the following values:

- **UPP_INT_CHI_DMA_PROG_ERR** - DMA Channel I Programming Error
- **UPP_INT_CHI_UNDER_OVER_RUN** - DMA Channel I Underrun/Overrun
- **UPP_INT_CHI_END_OF_WINDOW** - DMA Channel I End of Window Event
- **UPP_INT_CHI_END_OF_LINE** - DMA Channel I End of Line Event
- **UPP_INT_CHQ_DMA_PROG_ERR** - DMA Channel Q Programming Error
- **UPP_INT_CHQ_UNDER_OVER_RUN** - DMA Channel Q Underrun/Overrun
- **UPP_INT_CHQ_END_OF_WINDOW** - DMA Channel Q End of Window Event
- **UPP_INT_CHQ_END_OF_LINE** - DMA Channel Q End of Line Event

29.2.3.23 static uint16_t UPP_getRawInterruptStatus (uint32_t *base*) [inline], [static]

Gets the current uPP interrupt status for all the interrupts.

Parameters

base	is the configuration address of the uPP instance used.

This function returns the interrupt status of all the interrupts for the uPP module.

Returns

Returns current interrupt status for all the interrupts, enumerated as a bit field of any of the following values:

- **UPP_INT_CHI_DMA_PROG_ERR** - DMA Channel I Programming Error
- **UPP_INT_CHI_UNDER_OVER_RUN** - DMA Channel I Underrun/Overrun
- **UPP_INT_CHI_END_OF_WINDOW** - DMA Channel I End of Window Event
- **UPP_INT_CHI_END_OF_LINE** - DMA Channel I End of Line Event
- **UPP_INT_CHQ_DMA_PROG_ERR** - DMA Channel Q Programming Error
- **UPP_INT_CHQ_UNDER_OVER_RUN** - DMA Channel Q Underrun/Overrun
- **UPP_INT_CHQ_END_OF_WINDOW** - DMA Channel Q End of Window Event
- **UPP_INT_CHQ_END_OF_LINE** - DMA Channel Q End of Line Event

29.2.3.24 static void UPP_clearInterruptStatus (uint32_t *base*, uint16_t *intFlags*) [inline], [static]

Clears individual uPP module interrupts.

Parameters

base	is the configuration address of the uPP instance used.
intFlags	is a bit mask of the interrupt sources to be cleared.

This function clears uPP module interrupt flags. The *intFlags* parameter can be any of the following values OR'd together:

- **UPP_INT_CHI_DMA_PROG_ERR** - DMA Channel I Programming Error
- **UPP_INT_CHI_UNDER_OVER_RUN** - DMA Channel I Underrun/Overrun
- **UPP_INT_CHI_END_OF_WINDOW** - DMA Channel I End of Window Event
- **UPP_INT_CHI_END_OF_LINE** - DMA Channel I End of Line Event
- **UPP_INT_CHQ_DMA_PROG_ERR** - DMA Channel Q Programming Error
- **UPP_INT_CHQ_UNDER_OVER_RUN** - DMA Channel Q Underrun/Overrun
- **UPP_INT_CHQ_END_OF_WINDOW** - DMA Channel Q End of Window Event
- **UPP_INT_CHQ_END_OF_LINE** - DMA Channel Q End of Line Event

Returns

None.

29.2.3.25 static void UPP_enableGlobalInterrupt (uint32_t *base*) [inline], [static]

Enables uPP global interrupt.

Parameters

base	is the configuration address of the uPP instance used.

This function enables the global interrupt for uPP module which allows uPP to generate interrupts.

Returns

None.

29.2.3.26 static void UPP_disableGlobalInterrupt (uint32_t *base*) [inline], [static]

Disables uPP global interrupt.

Parameters

base	is the configuration address of the uPP instance used.

This function disables global interrupt for uPP module which restricts uPP to generate any interrupts.

Returns

None.

29.2.3.27 static bool UPP_isInterruptGenerated (uint32_t *base*) [inline], [static]

Get uPP global interrupt status.

Parameters

base	is the configuration address of the uPP instance used.

This function returns whether any of the uPP interrupt is generated.

Returns

Returns global interrupt status. It can return following values:

- **true** - Interrupt has been generated.
- **false** - No interrupt has been generated.

29.2.3.28 static void UPP_clearGlobalInterruptStatus (uint32_t *base*) [inline], [static]

Clears uPP global interrupt status.

Parameters

base	is the configuration address of the uPP instance used.

This function clears global interrupt status for uPP module.

Returns

None.

29.2.3.29 static void UPP_enableInputDelay (uint32_t *base*) [inline], [static]

Enables extra delay on uPP input pins.

Parameters

base	is the configuration address of the uPP instance used.

This function enables configurable extra delay on uPP input pins.

Returns

None.

29.2.3.30 static void UPP_disableInputDelay (uint32_t *base*) [inline], [static]

Disables extra delay on uPP input pins.

Parameters

base	is the configuration address of the uPP instance used.

This function disables extra delay on uPP input pins.

Returns

None.

29.2.3.31 static void UPP_setInputDelay (uint32_t *base*, **UPP_InputDelay** *delay*) [inline], [static]

Configures delay for uPP input pins.

Parameters

base	is the configuration address of the uPP instance used.
delay	is the delay to be introduced in input & clock pins.

This function sets input delay for uPP input pins. The *delay* parameter specifies the delay to be introduced to input & clock pins. It can take following values. All the following values lead to 2 cycle delay on clock pin.

- **UPP_INPUT_DLY_4** - 4 cycle delay for data & control pins
- **UPP_INPUT_DLY_6** - 6 cycle delay for data & control pins
- **UPP_INPUT_DLY_9** - 9 cycle delay for data & control pins
- **UPP_INPUT_DLY_14** - 14 cycle delay for data & control pins

Returns
None.

29.2.3.32 void UPP_setDMAReadThreshold (uint32_t *base*, **UPP_DMAChannel** *channel*, **UPP_ThresholdSize** *size*)

Sets the read threshold for uPP internal DMA channels.

Parameters

base	is the configuration address of the uPP instance used.
channel	is the required uPP internal DMA channel to be configured.
size	is the required read threshold size in bytes.

This function sets the read threshold for DMA channel I or Q. The *size* parameter specifies the read threshold in bytes. It can following values:

- **UPP_THR_SIZE_64BYTE** - Sets the DMA read threshold to 64 bytes.
- **UPP_THR_SIZE_128BYTE** - Sets the DMA read threshold to 128 bytes.
- **UPP_THR_SIZE_256BYTE** - Sets the DMA read threshold to 256 bytes.

Returns
None.

References UPP_DMA_CHANNEL_I.

29.2.3.33 void UPP_setDMADescriptor (uint32_t *base*, **UPP_DMAChannel** *channel*, const **UPP_DMADescriptor** ∗const *desc*)

Sets uPP Internal DMA Channel Descriptors.

Parameters

base	is the configuration address of the uPP instance used.
channel	is the required uPP internal DMA channel to be configured.
desc	is the required DMA descriptor setting.

This function configures DMA descriptors for either channel I or Q which includes starting address of DMA transfer, line count, byte count & line offset address for DMA transfer. In Tx mode, starting address is the address of data buffer to be transmitted while in Rx mode it is the address of buffer where recieved data is to be copied. The *channel* parameter can take any of the following values:

- **UPP_DMA_CHANNEL_I** - uPP DMA channel I
- **UPP_DMA_CHANNEL_Q** - uPP DMA channel Q

Returns
None.

References UPP_DMADescriptor::addr, UPP_DMADescriptor::byteCount, UPP_DMADescriptor::lineCount, UPP_DMADescriptor::lineOffset, and UPP_DMA_CHANNEL_I.

29.2.3.34 void UPP_getDMAChannelStatus (uint32_t *base*, **UPP_DMAChannel** *channel*, **UPP_DMAChannelStatus** ∗const *status*)

Returns current status of uPP internal DMA channel transfer.

Parameters

base	is the configuration address of the uPP instance used.
channel	is the required uPP internal DMA channel.
status	is current status for DMA channel returned by the api.

This function returns the current status for either channel I or Q active transfer which includes current DMA transfer address, current line & byte number of the transfer. The *channel* parameter can take any of the following values:

- **UPP_DMA_CHANNEL_I** - uPP DMA channel I
- **UPP_DMA_CHANNEL_Q** - uPP DMA channel Q

Returns
None.

References UPP_DMAChannelStatus::curAddr, UPP_DMAChannelStatus::curByteCount, UPP_DMAChannelStatus::curLineCount, and UPP_DMA_CHANNEL_I.

29.2.3.35 bool UPP_isDescriptorPending (uint32_t *base*, **UPP_DMAChannel** *channel*)

Returns Pend status of uPP internal DMA channel descriptor.

Parameters

base	is the configuration address of the uPP instance used.
channel	is the required uPP internal DMA channel.

This function returns the Pend status for DMA channel I or Q descriptor which specifies whether previous descriptor is copied from shadow register to original register & new descriptor can be programmed or the previous descriptor is still pending & new descriptor cannot be programmed. The *channel* parameter can take following values:

- **UPP_DMA_CHANNEL_I** - uPP DMA channel I
- **UPP_DMA_CHANNEL_Q** - uPP DMA channel Q

Returns

Returns pend status of DMA channel I descriptor. It can return following values:

- **true** - specifies that writing of new DMA descriptor is not allowed.
- **false** - specifies that writing of new DMA descriptor is allowed.

References UPP_DMA_CHANNEL_I.

29.2.3.36 bool UPP_isDescriptorActive (uint32_t *base,* **UPP_DMAChannel** *channel*)

Returns active status of uPP Internal DMA Channel descriptor.

Parameters

base	is the configuration address of the uPP instance used.
channel	is the required uPP internal DMA channel to be configured.

This function returns the active status of uPP internal DMA channel I or Q descriptor which specifies whether the descriptor is being currently active(transferring data) or idle. The *channel* parameter can take following values:

- **UPP_DMA_CHANNEL_I** - uPP DMA channel I
- **UPP_DMA_CHANNEL_Q** - uPP DMA channel Q

Returns

Returns active status of uPP internal DMA channel descriptor. It can return following values:

- **true** - specifies that desciptor is currently active.
- **false** - specifies that desciptor is currently idle.

References UPP_DMA_CHANNEL_I.

29.2.3.37 uint16_t UPP_getDMAFIFOWatermark (uint32_t *base,* **UPP_DMAChannel** *channel*)

Returns watermark for FIFO block count for uPP internal DMA Channel.

Parameters

base	is the configuration address of the uPP instance used.
channel	is the required uPP internal DMA channel.

This function returns watermark for FIFO block count for uPP internal DMA Channel I or Q based on *channel* parameter. The *channel* paramter can take following values:

- **UPP_DMA_CHANNEL_I** - uPP DMA channel I
- **UPP_DMA_CHANNEL_Q** - uPP DMA channel Q

Returns

Returns active status of DMA channel I descriptor. It can return following values:

- **true** - specifies that desciptor is currently active.
- **false** - specifies that desciptor is currently idle.

References UPP_DMA_CHANNEL_I.

29.2.3.38 void UPP_readRxMsgRAM (uint32_t *rxBase,* uint16_t *array[ ],* uint16_t *length,* uint16_t *offset*)

Reads the received data from uPP Rx MSG RAM.

Parameters

rxBase	is the uPP Rx MSG RAM base address.
array	is the address of the array of words to be transmitted.
length	is the number of words in the array to be transmitted.
offset	is offset in Rx Data RAM from where data read will start.

This function reads the received data from uPP Rx MSG RAM. The sum of parameters *length* & *offset* should be less than the size of the Rx MSG RAM.

Returns

None.

29.2.3.39 void UPP_writeTxMsgRAM (uint32_t *txBase,* const uint16_t *array[ ],* uint16_t *length,* uint16_t *offset*)

Writes the data to be transmitted in uPP Tx MSG RAM.

Parameters

txBase	is the uPP Tx MSG RAM base address.
array	is the address of the array of words to be transmitted.
length	is the number of words in the array to be transmitted.
offset	is offset in Tx Data RAM from where data write will start.

This function writes the data to be transmitted to uPP Rx MSG RAM. The sum of parameters *length* & *offset* should be less than the size of the Tx MSG RAM.

Returns

None.

30 Version Module

30.1 Version Introduction

The version driver provides a function which can be used to check the version number of the driverlib.lib that is in use.

30.2 API Functions

Macros

- #define VERSION_NUMBER

Functions

- uint32_t Version_getLibVersion (void)

30.2.1 Detailed Description

The code for this module is contained in `driverlib/version.c`, with `driverlib/version.h` containing the API declarations for use by applications.

30.2.2 Macro Definition Documentation

30.2.2.1 #define VERSION_NUMBER

Version number to be returned by Version_getLibVersion()

Referenced by Version_getLibVersion().

30.2.3 Function Documentation

30.2.3.1 uint32_t Version_getLibVersion (void)

Returns the driverlib version number

This function can be used to check the version number of the driverlib.lib that is in use. The version number will take the format x.xx.xx.xx, so for example, if the function returns 2100200, the driverlib version being used is 2.10.02.00.

Returns

Returns an integer value indicating the driverlib version.

References VERSION_NUMBER.

31 X-BAR Module

31.1 X-BAR Introduction

The crossbar or X-BAR API is a set of functions to configure the three X-BARs on the device–the Input X-BAR, the Output X-BAR, and the ePWM X-BAR. The X-BARs route both signals from pins and internal signals from IP blocks to a degree beyond what is possible with GPIO muxing alone. Functions are provided by the API to configure the various muxes, enable and disable signals, and lock in the configurations selected.

31.2 API Functions

Enumerations

- enum XBAR_OutputNum {
  XBAR_OUTPUT1, XBAR_OUTPUT2, XBAR_OUTPUT3, XBAR_OUTPUT4,
  XBAR_OUTPUT5, XBAR_OUTPUT6, XBAR_OUTPUT7, XBAR_OUTPUT8 }
- enum XBAR_TripNum {
  XBAR_TRIP4, XBAR_TRIP5, XBAR_TRIP7, XBAR_TRIP8,
  XBAR_TRIP9, XBAR_TRIP10, XBAR_TRIP11, XBAR_TRIP12 }
- enum XBAR_InputNum {
  XBAR_INPUT1, XBAR_INPUT2, XBAR_INPUT3, XBAR_INPUT4,
  XBAR_INPUT5, XBAR_INPUT6, XBAR_INPUT7, XBAR_INPUT8,
  XBAR_INPUT9, XBAR_INPUT10, XBAR_INPUT11, XBAR_INPUT12,
  XBAR_INPUT13, XBAR_INPUT14 }

Functions

- static void XBAR_enableOutputMux (XBAR_OutputNum output, uint32_t muxes)
- static void XBAR_disableOutputMux (XBAR_OutputNum output, uint32_t muxes)
- static void XBAR_setOutputLatchMode (XBAR_OutputNum output, bool enable)
- static bool XBAR_getOutputLatchStatus (XBAR_OutputNum output)
- static void XBAR_clearOutputLatch (XBAR_OutputNum output)
- static void XBAR_forceOutputLatch (XBAR_OutputNum output)
- static void XBAR_invertOutputSignal (XBAR_OutputNum output, bool invert)
- static void XBAR_enableEPWMMux (XBAR_TripNum trip, uint32_t muxes)
- static void XBAR_disableEPWMMux (XBAR_TripNum trip, uint32_t muxes)
- static void XBAR_invertEPWMSignal (XBAR_TripNum trip, bool invert)
- static void XBAR_setInputPin (XBAR_InputNum input, uint16_t pin)
- static void XBAR_lockInput (XBAR_InputNum input)
- static void XBAR_lockOutput (void)
- static void XBAR_lockEPWM (void)
- void XBAR_setOutputMuxConfig (XBAR_OutputNum output, XBAR_OutputMuxConfig muxConfig)

- void XBAR_setEPWMMuxConfig (XBAR_TripNum trip, XBAR_EPWMMuxConfig muxConfig)
- bool XBAR_getInputFlagStatus (XBAR_InputFlag inputFlag)
- void XBAR_clearInputFlag (XBAR_InputFlag inputFlag)

31.2.1 Detailed Description

The functions used to configure the ePWM and the Output X-BAR are identifiable as their names will either contain the word EPWM or Output. Both of these X-BARs have multiple output signals that have 32 associated muxes. The select signal of these muxes is configured using the XBAR_setEPWMMuxConfig() and XBAR_setOutputMuxConfig() functions. Each of these mux signals can be enabled and disabled before they are logically OR'd together to arrive at the output signal using XBAR_enableOutputMux() and XBAR_disableOutputMux() and XBAR_enableEPWMMux() and XBAR_disableEPWMMux().

The functions XBAR_getInputFlagStatus() and XBAR_clearInputFlag(), despite their names, are not related to the Input X-BAR. They provide a way to get and clear the status of the signals that are inputs to the ePWM and Output X-BARs. Since these two X-BARs share nearly all of their inputs, they share this set of flags.

The Input X-BAR takes a signal of a GPIO and routes it to an IP block destination. This pin can be selected for each input using the XBAR_setInputPin() function. Note that the descriptions for the values of the XBAR_InputNum enumerated type provide a list of the possible destinations for each input.

The code for this module is contained in `driverlib/xbar.c`, with `driverlib/xbar.h` containing the API declarations for use by applications.

31.2.2 Enumeration Type Documentation

31.2.2.1 enum **XBAR_OutputNum**

The following values define the *output* parameter for XBAR_setOutputMuxConfig(), XBAR_enableOutputMux(), and XBAR_disableOutputMux().

Enumerator

XBAR_OUTPUT1 OUTPUT1 of the Output X-BAR.
XBAR_OUTPUT2 OUTPUT2 of the Output X-BAR.
XBAR_OUTPUT3 OUTPUT3 of the Output X-BAR.
XBAR_OUTPUT4 OUTPUT4 of the Output X-BAR.
XBAR_OUTPUT5 OUTPUT5 of the Output X-BAR.
XBAR_OUTPUT6 OUTPUT6 of the Output X-BAR.
XBAR_OUTPUT7 OUTPUT7 of the Output X-BAR.
XBAR_OUTPUT8 OUTPUT8 of the Output X-BAR.

31.2.2.2 enum **XBAR_TripNum**

The following values define the *trip* parameter for XBAR_setEPWMMuxConfig(), XBAR_enableEPWMMux(), and XBAR_disableEPWMMux().

Enumerator

XBAR_TRIP4 TRIP4 of the ePWM X-BAR.
XBAR_TRIP5 TRIP5 of the ePWM X-BAR.
XBAR_TRIP7 TRIP7 of the ePWM X-BAR.
XBAR_TRIP8 TRIP8 of the ePWM X-BAR.
XBAR_TRIP9 TRIP9 of the ePWM X-BAR.
XBAR_TRIP10 TRIP10 of the ePWM X-BAR.
XBAR_TRIP11 TRIP11 of the ePWM X-BAR.
XBAR_TRIP12 TRIP12 of the ePWM X-BAR.

31.2.2.3 enum **XBAR_InputNum**

The following values define the *input* parameter for XBAR_setInputPin().

Enumerator

XBAR_INPUT1 ePWM[TZ1], ePWM[TRIP1], X-BARs
XBAR_INPUT2 ePWM[TZ2], ePWM[TRIP2], X-BARs
XBAR_INPUT3 ePWM[TZ3], ePWM[TRIP3], X-BARs
XBAR_INPUT4 ADC wrappers, X-BARs, XINT1.
XBAR_INPUT5 EXTSYNCIN1, X-BARs, XINT2.
XBAR_INPUT6 EXTSYNCIN2, ePWM[TRIP6], X-BARs, XINT3.
XBAR_INPUT7 eCAP1, X-BARs
XBAR_INPUT8 eCAP2, X-BARs
XBAR_INPUT9 eCAP3, X-BARs
XBAR_INPUT10 eCAP4, X-BARs
XBAR_INPUT11 eCAP5, X-BARs
XBAR_INPUT12 eCAP6, X-BARs
XBAR_INPUT13 XINT4, X-BARs.
XBAR_INPUT14 XINT5, X-BARs.

31.2.3 Function Documentation

31.2.3.1 static void XBAR_enableOutputMux (**XBAR_OutputNum** *output,* uint32_t *muxes*) [inline], [static]

Enables the Output X-BAR mux values to be passed to the output signal.

Parameters

output	is the X-BAR output being configured.
muxes	is a bit field of the muxes to be enabled.

This function enables the mux values to be passed to the X-BAR output signal. The *output* parameter is a value **XBAR_OUTPUTy** where y is the output number between 1 and 8 inclusive.

The *muxes* parameter is a bit field of the muxes being enabled where bit 0 represents mux 0, bit 1 represents mux 1 and so on. Defines are provided in the form of **XBAR_MUXnn** that can be OR'd together to enable several muxes on an output at the same time. For example, passing this function (**XBAR_MUX04** | **XBAR_MUX10**) would enable muxes 4 and 10.

Returns

None.

31.2.3.2 static void XBAR_disableOutputMux (**XBAR_OutputNum** *output,* uint32_t *muxes*) [inline], [static]

Disables the Output X-BAR mux values from being passed to the output.

Parameters

output	is the X-BAR output being configured.
muxes	is a bit field of the muxes to be disabled.

This function disables the mux values from being passed to the X-BAR output signal. The *output* parameter is a value **XBAR_OUTPUTy** where y is the output number between 1 and 8 inclusive.

The *muxes* parameter is a bit field of the muxes being disabled where bit 0 represents mux 0, bit 1 represents mux 1 and so on. Defines are provided in the form of **XBAR_MUXnn** that can be OR'd together to disable several muxes on an output at the same time. For example, passing this function (**XBAR_MUX04** | **XBAR_MUX10**) would disable muxes 4 and 10.

Returns

None.

31.2.3.3 static void XBAR_setOutputLatchMode (**XBAR_OutputNum** *output,* bool *enable*) [inline], [static]

Enables or disables the output latch to drive the selected output.

Parameters

output	is the X-BAR output being configured.
enable	is a flag that determines whether or not the latch is selected to drive the X-BAR output.

This function sets the Output X-BAR output signal latch mode. If the *enable* parameter is **true**, the output specified by *output* will be driven by the output latch.

Returns

None.

31.2.3.4 static bool XBAR_getOutputLatchStatus (**XBAR_OutputNum** *output*) [inline], [static]

Returns the status of the output latch

Parameters

output	is the X-BAR output being checked.

Returns

Returns **true** if the output corresponding to *output* was triggered. If not, it will return **false**.

31.2.3.5 static void XBAR_clearOutputLatch (**XBAR_OutputNum** *output*) [inline], [static]

Clears the output latch for the specified output.

Parameters

output	is the X-BAR output being configured.

This function clears the Output X-BAR output latch. The output to be configured is specified by the *output* parameter.

Returns

None.

31.2.3.6 static void XBAR_forceOutputLatch (**XBAR_OutputNum** *output*) [inline], [static]

Forces the output latch for the specified output.

Parameters

output	is the X-BAR output being configured.

This function forces the Output X-BAR output latch. The output to be configured is specified by the *output* parameter.

Returns

None.

31.2.3.7 static void XBAR_invertOutputSignal (**XBAR_OutputNum** *output,* bool *invert*) [inline], [static]

Configures the polarity of an Output X-BAR output.

Parameters

output	is the X-BAR output being configured.
invert	is a flag that determines whether the output is active-high or active-low.

This function inverts the Output X-BAR signal if the *invert* parameter is **true**. If *invert* is **false**, the signal will be passed as is. The *output* parameter is a value **XBAR_OUTPUTy** where y is the output number between 1 and 8 inclusive.

Returns

None.

31.2.3.8 static void XBAR_enableEPWMMux (**XBAR_TripNum** *trip,* uint32_t *muxes*) [inline], [static]

Enables the ePWM X-BAR mux values to be passed to an ePWM module.

Parameters

trip	is the X-BAR output being configured.
muxes	is a bit field of the muxes to be enabled.

This function enables the mux values to be passed to the X-BAR trip signal. The *trip* parameter is a value **XBAR_TRIPy** where y is the number of the trip signal on the ePWM.

The *muxes* parameter is a bit field of the muxes being enabled where bit 0 represents mux 0, bit 1 represents mux 1 and so on. Defines are provided in the form of **XBAR_MUXnn** that can be logically OR'd together to enable several muxes on an output at the same time.

Returns

None.

31.2.3.9 static void XBAR_disableEPWMMux (**XBAR_TripNum** *trip,* uint32_t *muxes*) [inline], [static]

Disables the ePWM X-BAR mux values to be passed to an ePWM module.

Parameters

trip	is the X-BAR output being configured.
muxes	is a bit field of the muxes to be disabled.

This function disables the mux values to be passed to the X-BAR trip signal. The *trip* parameter is a value **XBAR_TRIPy** where y is the number of the trip signal on the ePWM.

The *muxes* parameter is a bit field of the muxes being disabled where bit 0 represents mux 0, bit 1 represents mux 1 and so on. Defines are provided in the form of **XBAR_MUXnn** that can be logically OR'd together to disable several muxes on an output at the same time.

Returns

None.

31.2.3.10 static void XBAR_invertEPWMSignal (**XBAR_TripNum** *trip,* bool *invert*) [inline], [static]

Configures the polarity of an ePWM X-BAR output.

Parameters

trip	is the X-BAR output being configured.
invert	is a flag that determines whether the output is active-high or active-low.

This function inverts the ePWM X-BAR trip signal if the *invert* parameter is **true**. If *invert* is **false**, the signal will be passed as is. The *trip* parameter is a value **XBAR_TRIPy** where y is the number of the trip signal on the ePWM X-BAR that is being configured.

Returns

None.

31.2.3.11 static void XBAR_setInputPin (**XBAR_InputNum** *input*, uint16_t *pin*) [inline], [static]

Sets the GPIO pin for an Input X-BAR input.

Parameters

input	is the X-BAR input being configured.
pin	is the identifying number of the pin.

This function configures which GPIO is assigned to an Input X-BAR input. The *input* parameter is a value in the form of a define **XBAR_INPUTy** where y is a the input number for the Input X-BAR.

The pin is specified by its numerical value. For example, GPIO34 is specified by passing 34 as *pin*.

For the other non - GPIO values: 0xFFFD: '1' will be driven to the destination 0xFFFE: '1' will be driven to the destination 0xFFFF: '0' will be driven to the destination NOTE: Pin value greater than the available number of GPIO pins on a device (except 0xFFFF) will cause the destination to be driven '1'.

Returns

None.

Referenced by GPIO_setInterruptPin().

31.2.3.12 static void XBAR_lockInput (**XBAR_InputNum** *input*) [inline], [static]

Locks an input to the Input X-BAR.

Parameters

input	is an input to the Input X-BAR.

This function locks the specific input on the Input X-BAR.

Returns

None.

31.2.3.13 static void XBAR_lockOutput (void) [inline], [static]

Locks the Output X-BAR.

This function locks the Output X-BAR.

Returns

None.

31.2.3.14 static void XBAR_lockEPWM (void) [inline], [static]

Locks the ePWM X-BAR.

This function locks the ePWM X-BAR.

Returns

None.

31.2.3.15 void XBAR_setOutputMuxConfig (**XBAR_OutputNum** *output,* XBAR_OutputMuxConfig *muxConfig*)

Configures the Output X-BAR mux that determines the signals passed to an output.

Parameters

output	is the X-BAR output being configured.
muxConfig	is mux configuration that specifies the signal.

This function configures an Output X-BAR mux. This determines which signal(s) should be passed through the X-BAR to a GPIO. The *output* parameter is a value **XBAR_OUTPUTy** where y is a the output number between 1 and 8 inclusive.

The *muxConfig* parameter is the mux configuration value that specifies which signal will be passed from the mux. The values have the format of **XBAR_OUT_MUXnn_xx** where the 'xx' is the signal and nn is the mux number (00 through 11). The possible values are found in `xbar.h`

This function may be called for each mux of an output and their values will be logically OR'd before being passed to the output signal. This means that this function may be called, for example, with the argument **XBAR_OUT_MUX00_ECAP1_OUT** and then with the argument **XBAR_OUT_MUX01_INPUTXBAR1**, resulting in the values of MUX00 and MUX01 being logically OR'd if both are enabled. Calling the function twice for the same mux on the output will result in the configuration in the second call overwriting the first.

Returns
None.

31.2.3.16 void XBAR_setEPWMMuxConfig (**XBAR_TripNum** *trip,* XBAR_EPWMMuxConfig *muxConfig*)

Configures the ePWM X-BAR mux that determines the signals passed to an ePWM module.

Parameters

trip	is the X-BAR output being configured.
muxConfig	is mux configuration that specifies the signal.

This function configures an ePWM X-BAR mux. This determines which signal(s) should be passed through the X-BAR to an ePWM module. The *trip* parameter is a value **XBAR_TRIPy** where y is a the number of the trip signal on the ePWM.

The *muxConfig* parameter is the mux configuration value that specifies which signal will be passed from the mux. The values have the format of **XBAR_EPWM_MUXnn_xx** where the 'xx' is the signal and nn is the mux number (0 through 31). The possible values are found in `xbar.h`

This function may be called for each mux of an output and their values will be logically OR'd before being passed to the trip signal. This means that this function may be called, for example, with the argument **XBAR_EPWM_MUX00_ECAP1_OUT** and then with the argument **XBAR_EPWM_MUX01_INPUTXBAR1**, resulting in the values of MUX00 and MUX03 being logically OR'd if both are enabled. Calling the function twice for the same mux on the output will result in the configuration in the second call overwriting the first.

Returns
None.

31.2.3.17 bool XBAR_getInputFlagStatus (XBAR_InputFlag *inputFlag*)

Returns the status of the input latch.

Parameters

inputFlag	is the X-BAR input latch being checked. Values are in the format of /b XBAR_INPUT_FLG_XXXX where "XXXX" is name of the signal.

Returns

Returns **true** if the X-BAR input corresponding to the *inputFlag* has been triggered. If not, it will return **false**.

31.2.3.18 void XBAR_clearInputFlag (XBAR_InputFlag *inputFlag*)

Clears the input latch for the specified input latch.

Parameters

inputFlag	is the X-BAR input latch being cleared.

This function clears the Input X-BAR input latch. The input latch to be cleared is specified by the *inputFlag* parameter.

Returns

None.

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