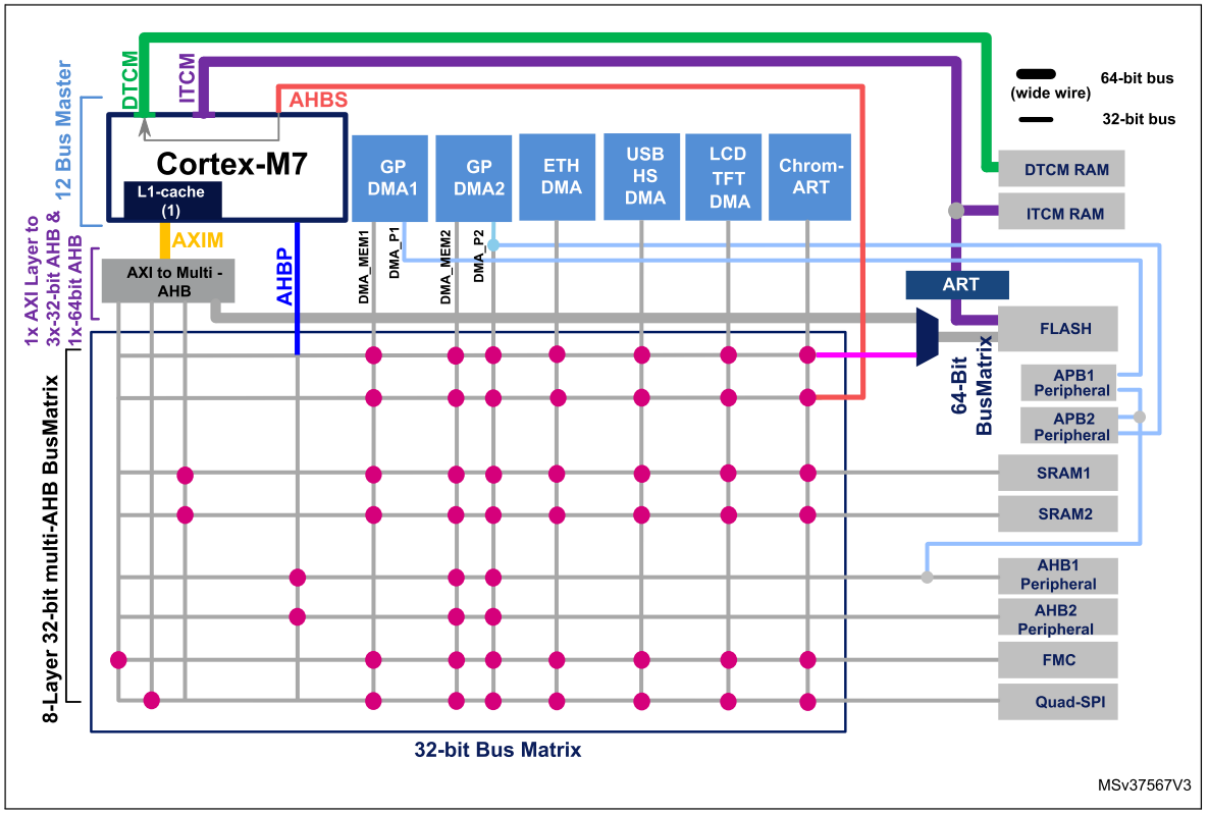
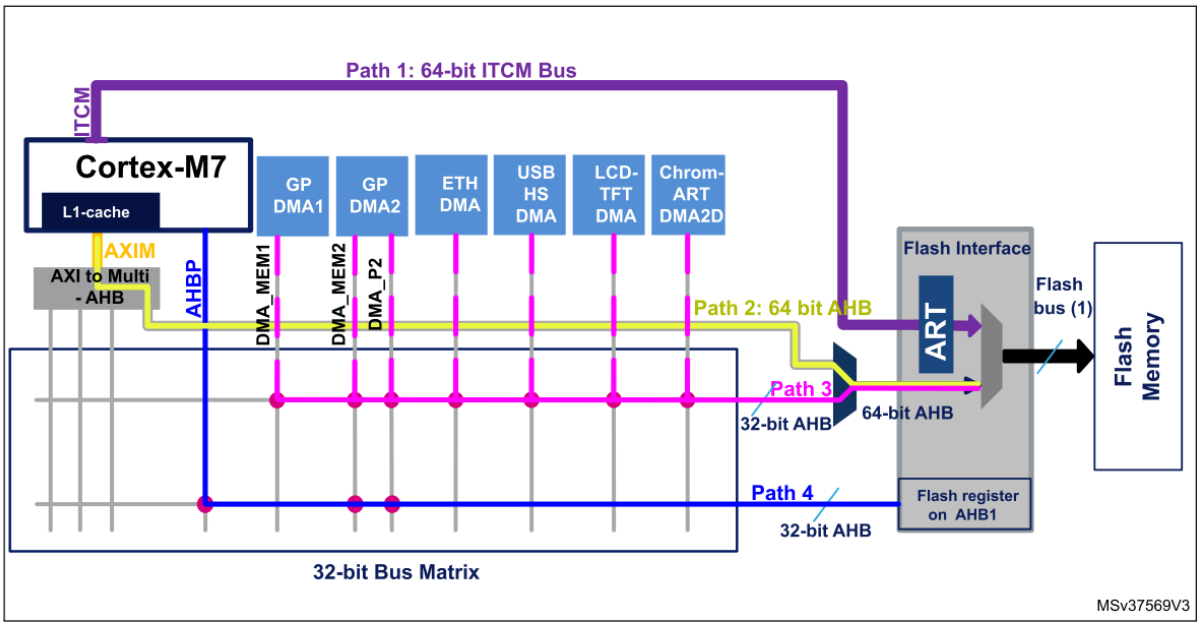
Speicher vom STM32F746G Discovery

Figure 1. STM32F7 Series system architecture



1. I/D cache size:
   - For STM32F74xxx and STM32F75xxx devices: 4 Kbytes.

Figure 2. Flash memory interfaces (pathes: 1, 2, 3, 4)



1. The Flash memory wide size:
   - For STM32F74xxx and STM32F75xxx devices: 256 bits.

Figure 3. Flash memory interfaces (pathes: 5, 6, 7, 8)

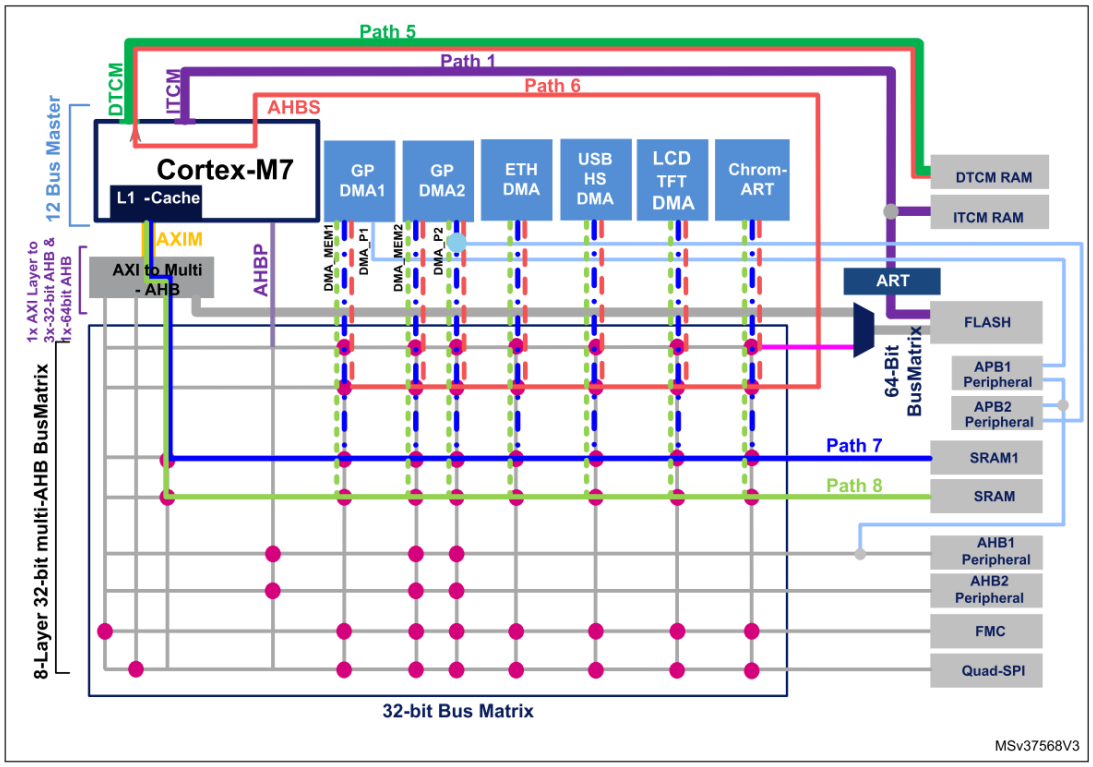
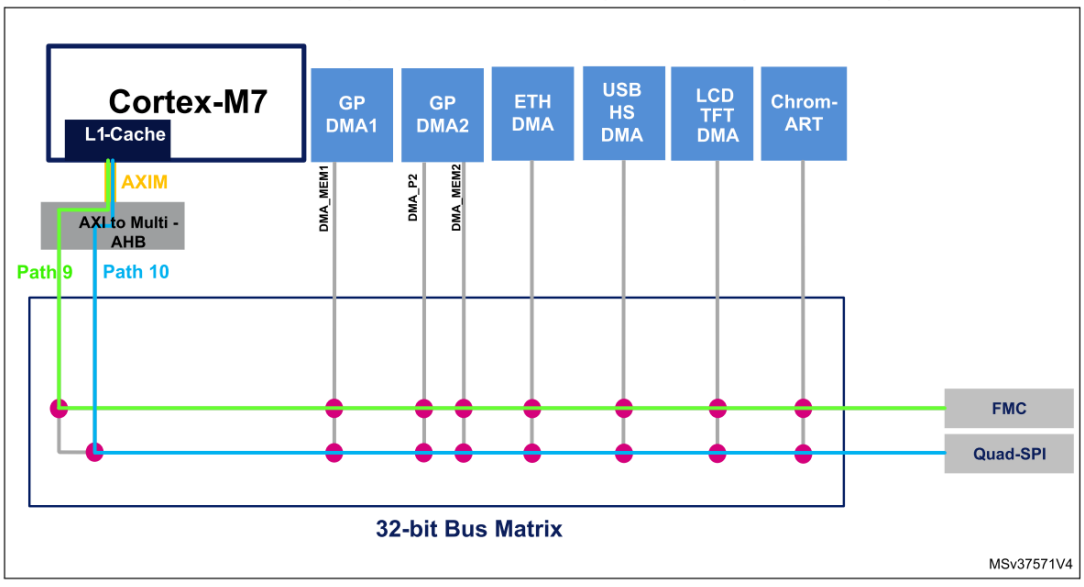


Table 3. internal memory summary of the STM32F74xxx/STM32F75xxx devices

Memory type	Memory region	Address start	Address end	Size	Access interfaces
FLASH	FLASH-ITCM	0x0020 0000	0x002F FFFF	1 Mbyte	ITCM (64-bit)
	FLASH-AXIM	0x0800 0000	0x080F FFFF		AHB (64-bit) AHB (32-bit)
RAM	DTCM-RAM	0x2000 0000	0x2000 FFFF	64 Kbytes	DTCM (64-bit)
	ITCM-RAM	0x0000 0000	0x0000 3FFF	16 Kbytes	ITCM (64-bit)
	SRAM1	0x2001 0000	0x2004 BFFF	240 Kbytes	AHB (32-bit)
	SRAM2	0x2004 C000	0x2004 FFFF	16 KBytes	AHB (32-bit)

Figure 4. External memory interfaces (pathes: 9, 10)



Interner Speicher

Flash: 1 Mbytes = 1024Kbytes
RAM: 340 KBytes

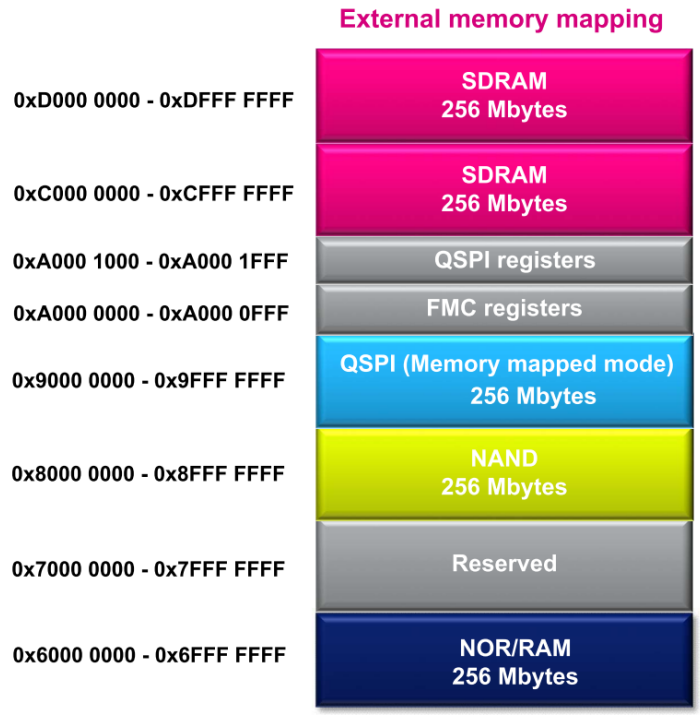
Externer Speicher

Quad-SPI Nor Flash memory

128-Mbit Quad-SPI Nor Flash memory (N25Q128A13EF840E from MICRON) is connected to the Quad-SPI interface of the STM32F746NGH6.

SDRAM memory

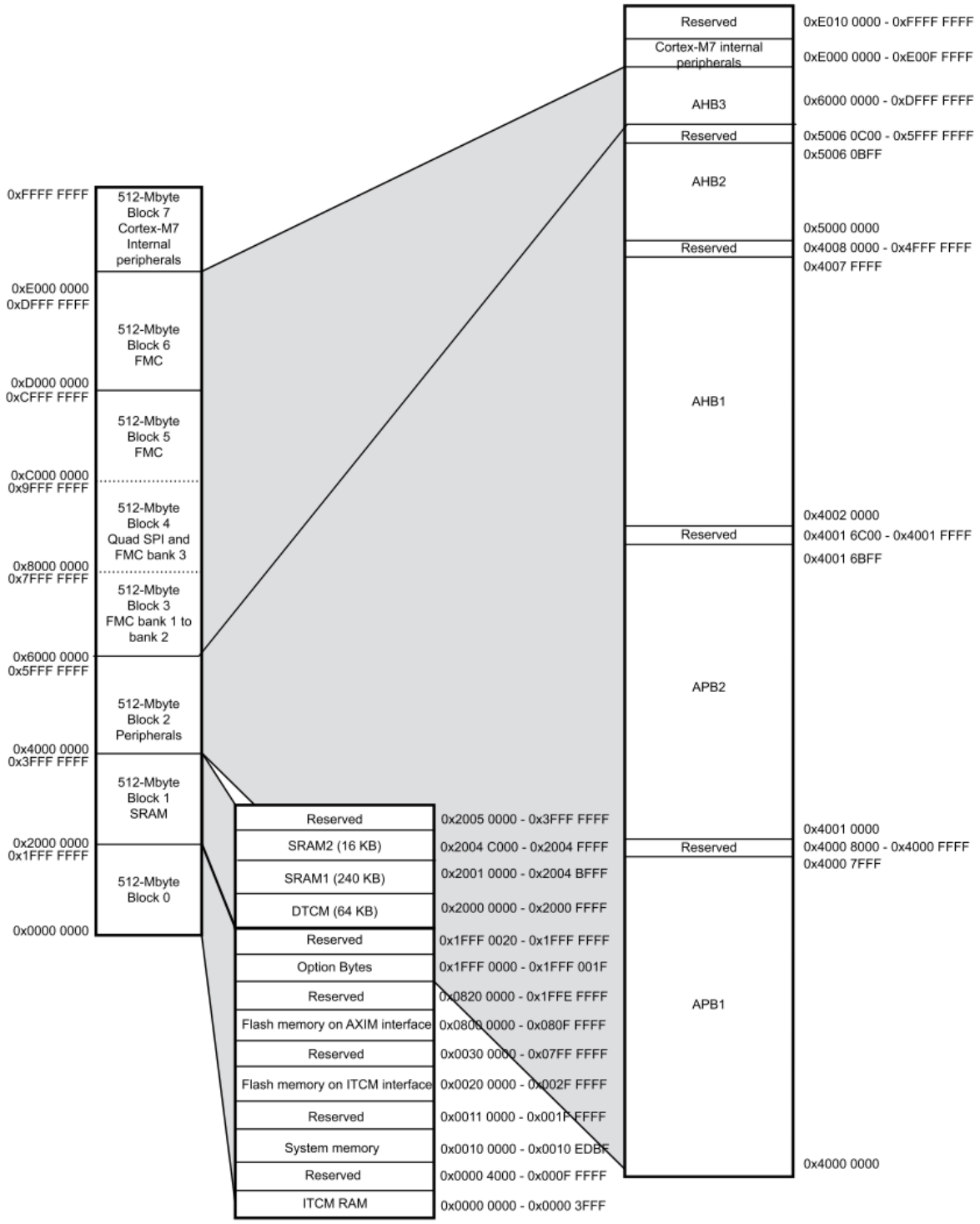
128-Mbit SDRAM (MT48LC4M32B2B5-6A from MICRON) is connected to the FMC interface of the STM32F746NGH6. Only the lowest 16-bit data are used (64-Mbit accessible). DQ16 to DQ31 are unused and connected to a 10K ohm pull-down resistor.



128-Mbit = 16-Mbytes = 0xF42400

Table 2. Cortex®-M7 default memory attributes after reset

Address range	Region name	Type	Attributes	Execute Never?
0x00000000-0x1FFFFFFF	Code	Normal	Cacheable, Write-Through, Allocate on read miss	No
0x20000000-0x3FFFFFFF	SRAM	Normal	Cacheable, Write-Back, Allocate on read and write miss	No
0x40000000-0x5FFFFFFF	Peripheral	Device	Non-shareable	Yes
0x60000000-0x7FFFFFFF	RAM	Normal	Cacheable, Write-Back, Allocate on read and write miss	No
0x80000000-0x9FFFFFFF	RAM	Normal	Cacheable, Write-Through, Allocate on read miss	No
0xA0000000-0xBFFFFFFF	External Device	Device	Shareable	Yes
0xC0000000-0xDFFFFFFF	External Device	Device	Non-shareable	Yes
0xE0000000-0xE000FFFF	Private peripheral bus	Strongly ordered	-	Yes
0xE0010000-0xFFFFFFFF	Vendor system	Device	Non-shareable	Yes


0xFFFF FFFF
512-Mbyte Block 7 Cortex-M7 Internal peripherals
0xE000 0000
0xDFFF FFFF
512-Mbyte Block 6 FMC
0xD000 0000
0xCFFF FFFF
512-Mbyte Block 5 FMC
0xC000 0000
0x9FFF FFFF
512-Mbyte Block 4 Quad SPI and FMC bank 3
0x8000 0000
0x7FFF FFFF
512-Mbyte Block 3 FMC bank 1 to bank 2
0x6000 0000
0x5FFF FFFF
512-Mbyte Block 2 Peripherals
0x4000 0000
0x3FFF FFFF
512-Mbyte Block 1 SRAM
0x2000 0000
0x1FFF FFFF
512-Mbyte Block 0
0x0000 0000
Reserved
0x2005 0000 - 0x3FFF FFFF
SRAM2 (16 KB)
0x2004 C000 - 0x2004 FFFF
SRAM1 (240 KB)
0x2001 0000 - 0x2004 BFFF
DTCM (64 KB)
0x2000 0000 - 0x2000 FFFF
Reserved
0x1FFF 0020 - 0x1FFF FFFF
Option Bytes
0x1FFF 0000 - 0x1FFF 001F
Reserved
0x0820 0000 - 0x1FFE FFFF
Flash memory on AXIM interface
0x0800 0000 - 0x080F FFFF
Reserved
0x0030 0000 - 0x07FF FFFF
Flash memory on ITCM interface
0x0020 0000 - 0x002F FFFF
Reserved
0x0011 0000 - 0x001F FFFF
System memory
0x0010 0000 - 0x0010 EDBF
Reserved
0x0000 4000 - 0x000F FFFF
ITCM RAM
0x0000 0000 - 0x0000 3FFF
Reserved
0xE010 0000 - 0xFFFF FFFF
Cortex-M7 internal peripherals
0xE000 0000 - 0xE00F FFFF
AHB3
0x6000 0000 - 0xDFFF FFFF
Reserved
0x5006 0C00 - 0x5FFF FFFF
0x5006 0BFF
AHB2
0x5000 0000
Reserved
0x4008 0000 - 0x4FFF FFFF
0x4007 FFFF
AHB1
0x4002 0000
Reserved
0x4001 6C00 - 0x4001 FFFF
0x4001 6BFF
APB2
0x4001 0000
Reserved
0x4000 8000 - 0x4000 FFFF
0x4000 7FFF
APB1
0x4000 0000

Linker Script (*.ld)

```
/* Specify the memory areas */
MEMORY
{
FLASH (rx)      : ORIGIN = 0x08000000, LENGTH = 1024K
Memory1 (xrw)   : ORIGIN = 0x20000000, LENGTH = 0xA0        = 160 Bytes
Memory2 (xrw)   : ORIGIN = 0x200000A0, LENGTH = 0xA0        = 160 Bytes
Memory3 (xrw)   : ORIGIN = 0x20000140, LENGTH = 0x1dc4      = 7.620 Bytes = 7 Kbytes
Memory4 (xrw)   : ORIGIN = 0x20001F04, LENGTH = 0x1dc4      = 7.620 Bytes = 7 Kbytes
RAM1 (xrw)      : ORIGIN = 0x20003CC8, LENGTH = 0x6024      = 24.612 Bytes = 24 Kbytes
RAM2 (xrw)      : ORIGIN = 0x20009CEC, LENGTH = 0x7800      = 30.720 Bytes = 30 Kbytes
RAM (xrw)       : ORIGIN = 0x200114EC, LENGTH = 0x3EB14     = 256.788 Bytes = 250 Kbytes
QSPI (rx)       : ORIGIN = 0x90000000, LENGTH = 16M
}

...

  .ARM.attributes 0 : { *(.ARM.attributes) }
  .RxDecripSection (NOLOAD) : { *(.RxDecripSection) } >Memory1
  .TxDescripSection (NOLOAD) : { *(.TxDescripSection) } >Memory2
  .RxBUF (NOLOAD) : { *(.RxBUF) } >Memory3
  .TxBUF (NOLOAD) : { *(.TxBUF) } >Memory4
  .RamData1 (NOLOAD) : { *(.RamData1) } >RAM1
  .RamData2 (NOLOAD): { *(.RamData2) } >RAM2
  .ExtQSPIFlashSection : { *(.ExtQSPIFlashSection) } >QSPI
```

Map File (*.map)

Memory Configuration

Name	Origin	Length	Attributes
FLASH	0x08000000	0x00100000	xr
Memory1	0x20000000	0x000000a0	xrw
Memory2	0x200000a0	0x000000a0	xrw
Memory3	0x20000140	0x00001dc4	xrw
Memory4	0x20001f04	0x00001dc4	xrw
RAM1	0x20003cc8	0x00006024	xrw
RAM2	0x20009cec	0x00007800	xrw
RAM	0x200114ec	0x0003eb14	xrw
QSPI	0x90000000	0x01000000	xr
default	0x00000000	0xffffffff	

The QSPI external flash loader is not integrated with supported toolchains, it's only supported with STM32 ST-Link Utility V3.9

To load the demonstration, use STM32 ST-Link Utility to program both internal Flash and external QSPI memory.

To edit and debug the demonstration you need first to program the external QSPI memory using STLink utility and then use your preferred toolchain to update and debug the internal flash content.

In order to program the demonstration you must do the following:

1- Open STM32 ST-Link Utility V3.9, click on "External Loader" from the bar menu then check "N25Q128A_STM32F746G-DISCO" box
2- Connect the STM32746G-DISCOVERY board to PC with USB cable through CN14
3- Use "STM32CubeDemo_STM32746G-DISCO_V1.1.2.hex" file provided under "Binary" with STM32 ST-Link Utility to program both internal Flash and external QSPI memory
4- copy the audio and video files provided under "Utilities/Media/" in the USB key
5- Plug a USB micro A-Male to A-Female cable on CN12 connector
-> The internal Flash and the external QSPI are now programmed and the demonstration is shown on the board.

In order to Edit and debug the program, you must do the following

- if not done, perform step 1, 2, 3, 4 and 5 described above,
- Open your preferred toolchain,
- Use the IDE to update and load the internal flash content,
- Run the demonstration.

Note If the user code size exceeds the DTCM-RAM size or starts from internal cacheable memories (SRAM1 and SRAM2), it is recommended to configure the latters as Write Through. This is ensured by configuring the memory attributes at MPU level in order to ensure cache coherence on SRAM1 and SRAM2. Please, refer to Template project for a typical MPU configuration.

Note If external memory is shared between several processors, it is recommended to configure it as Write Back (bufferable), shareable and cacheable. The memory base address and size must be properly updated. The user needs to manage the cache coherence at application level.
For more details about the MPU configuration and use, please refer to AN4838 "Managing memory protection unit (MPU) in STM32 MCUs"