# 1. Description

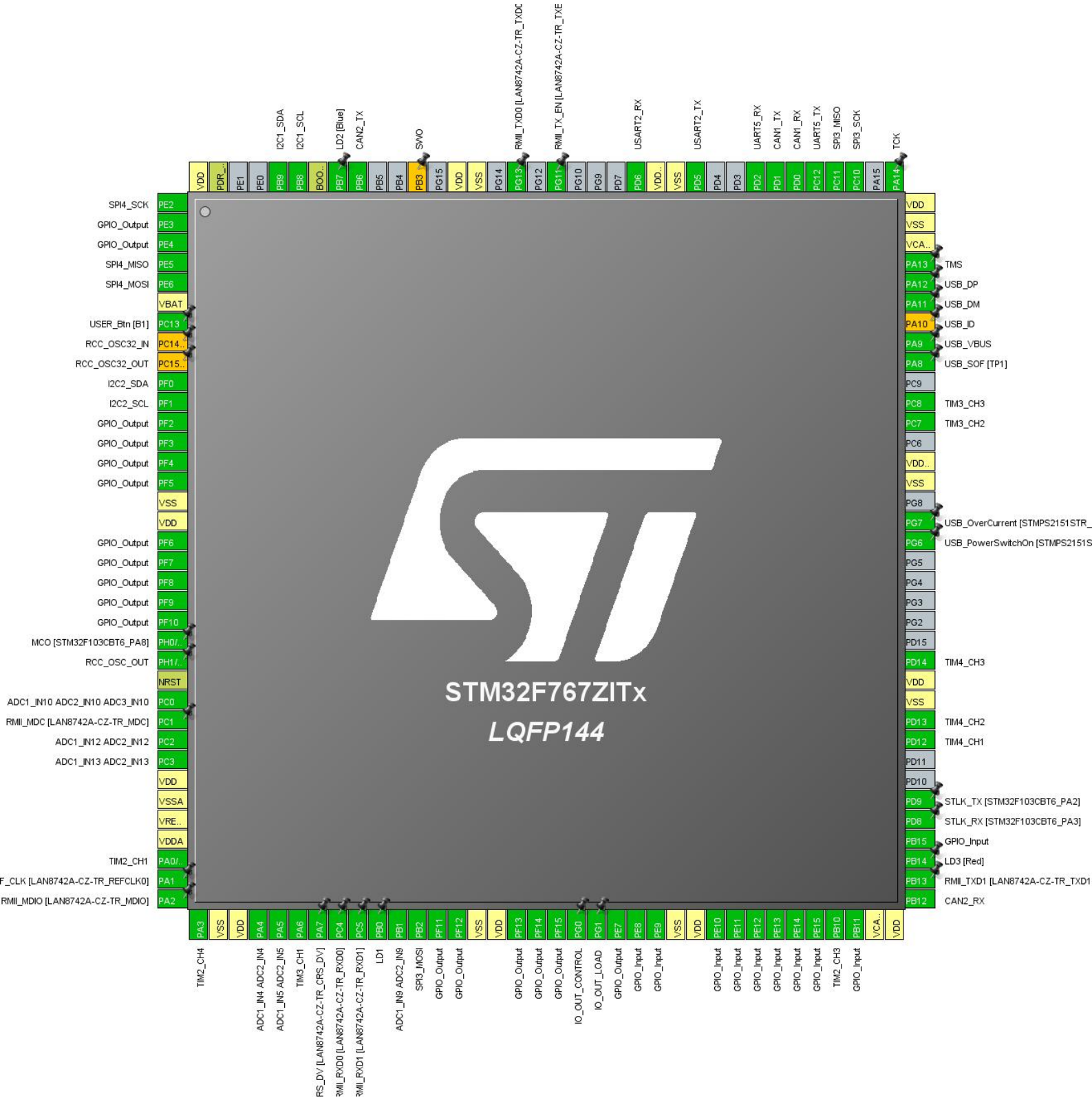
## 1.1. Project

| | |
|---|---|
| Project Name | HorizonXIX_Firmware |
| Board Name | NUCLEO-F767ZI |
| Generated with: | STM32CubeMX 5.1.0 |
| Date | 07/24/2019 |

## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F7 |
| MCU Line | STM32F7x7 |
| MCU name | STM32F767ZITx |
| MCU Package | LQFP144 |
| MCU Pin number | 144 |

## 2. Pinout Configuration



# 3. Pins Configuration

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 1 | PE2 | I/O | SPI4_SCK | |
| 2 | PE3 * | I/O | GPIO_Output | |
| 3 | PE4 * | I/O | GPIO_Output | |
| 4 | PE5 | I/O | SPI4_MISO | |
| 5 | PE6 | I/O | SPI4_MOSI | |
| 6 | VBAT | Power | | |
| 7 | PC13 | I/O | GPIO_EXTI13 | USER_Btn [B1] |
| 8 | PC14/OSC32_IN ** | I/O | RCC_OSC32_IN | |
| 9 | PC15/OSC32_OUT ** | I/O | RCC_OSC32_OUT | |
| 10 | PF0 | I/O | I2C2_SDA | |
| 11 | PF1 | I/O | I2C2_SCL | |
| 12 | PF2 * | I/O | GPIO_Output | |
| 13 | PF3 * | I/O | GPIO_Output | |
| 14 | PF4 * | I/O | GPIO_Output | |
| 15 | PF5 * | I/O | GPIO_Output | |
| 16 | VSS | Power | | |
| 17 | VDD | Power | | |
| 18 | PF6 * | I/O | GPIO_Output | |
| 19 | PF7 * | I/O | GPIO_Output | |
| 20 | PF8 * | I/O | GPIO_Output | |
| 21 | PF9 * | I/O | GPIO_Output | |
| 22 | PF10 * | I/O | GPIO_Output | |
| 23 | PH0/OSC_IN | I/O | RCC_OSC_IN | MCO [STM32F103CBT6_PA8] |
| 24 | PH1/OSC_OUT | I/O | RCC_OSC_OUT | |
| 25 | NRST | Reset | | |
| 26 | PC0 | I/O | ADC1_IN10, ADC2_IN10, ADC3_IN10 | |
| 27 | PC1 | I/O | ETH_MDC | RMII_MDC [LAN8742A-CZ-TR_MDC] |
| 28 | PC2 | I/O | ADC1_IN12, ADC2_IN12 | |
| 29 | PC3 | I/O | ADC1_IN13, ADC2_IN13 | |
| 30 | VDD | Power | | |
| 31 | VSSA | Power | | |
| 32 | VREF+ | Power | | |
| 33 | VDDA | Power | | |

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 34 | PA0/WKUP | I/O | TIM2_CH1 | |
| 35 | PA1 | I/O | ETH_REF_CLK | RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0] |
| 36 | PA2 | I/O | ETH_MDIO | RMII_MDIO [LAN8742A-CZ-TR_MDIO] |
| 37 | PA3 | I/O | TIM2_CH4 | |
| 38 | VSS | Power | | |
| 39 | VDD | Power | | |
| 40 | PA4 | I/O | ADC1_IN4, ADC2_IN4 | |
| 41 | PA5 | I/O | ADC1_IN5, ADC2_IN5 | |
| 42 | PA6 | I/O | TIM3_CH1 | |
| 43 | PA7 | I/O | ETH_CRS_DV | RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV] |
| 44 | PC4 | I/O | ETH_RXD0 | RMII_RXD0 [LAN8742A-CZ-TR_RXD0] |
| 45 | PC5 | I/O | ETH_RXD1 | RMII_RXD1 [LAN8742A-CZ-TR_RXD1] |
| 46 | PB0 * | I/O | GPIO_Output | LD1 |
| 47 | PB1 | I/O | ADC1_IN9, ADC2_IN9 | |
| 48 | PB2 | I/O | SPI3_MOSI | |
| 49 | PF11 * | I/O | GPIO_Output | |
| 50 | PF12 * | I/O | GPIO_Output | |
| 51 | VSS | Power | | |
| 52 | VDD | Power | | |
| 53 | PF13 * | I/O | GPIO_Output | |
| 54 | PF14 * | I/O | GPIO_Output | |
| 55 | PF15 * | I/O | GPIO_Output | |
| 56 | PG0 * | I/O | GPIO_Output | IO_OUT_CONTROL |
| 57 | PG1 * | I/O | GPIO_Output | IO_OUT_LOAD |
| 58 | PE7 * | I/O | GPIO_Output | |
| 59 | PE8 * | I/O | GPIO_Input | |
| 60 | PE9 * | I/O | GPIO_Input | |
| 61 | VSS | Power | | |
| 62 | VDD | Power | | |
| 63 | PE10 * | I/O | GPIO_Input | |
| 64 | PE11 * | I/O | GPIO_Input | |
| 65 | PE12 * | I/O | GPIO_Input | |
| 66 | PE13 * | I/O | GPIO_Input | |
| 67 | PE14 * | I/O | GPIO_Input | |

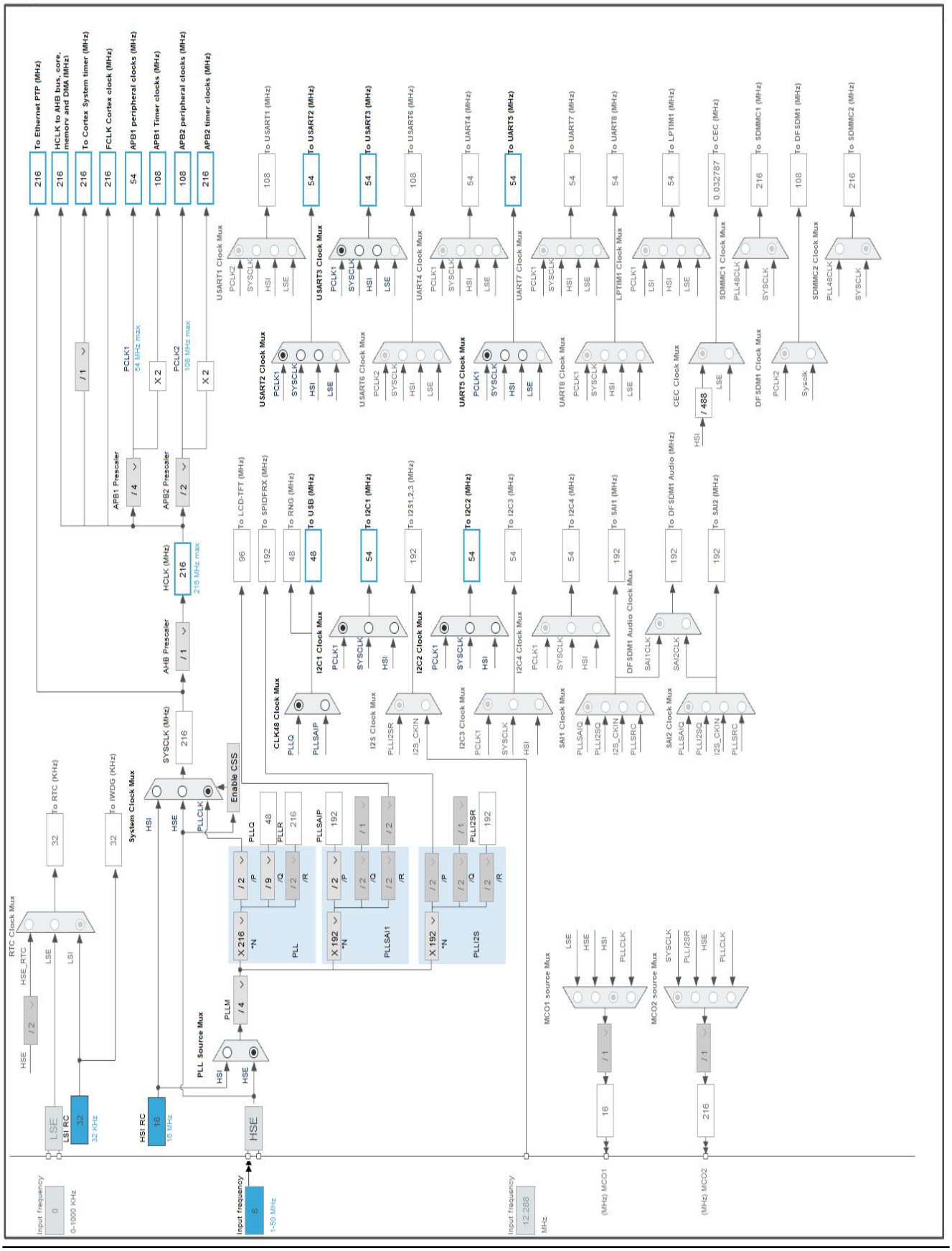
| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 68 | PE15 * | I/O | GPIO_Input | |
| 69 | PB10 | I/O | TIM2_CH3 | |
| 70 | PB11 * | I/O | GPIO_Input | |
| 71 | VCAP_1 | Power | | |
| 72 | VDD | Power | | |
| 73 | PB12 | I/O | CAN2_RX | |
| 74 | PB13 | I/O | ETH_TXD1 | RMII_TXD1 [LAN8742A-CZ-TR_TXD1] |
| 75 | PB14 * | I/O | GPIO_Output | LD3 [Red] |
| 76 | PB15 * | I/O | GPIO_Input | |
| 77 | PD8 | I/O | USART3_TX | STLK_RX [STM32F103CBT6_PA3] |
| 78 | PD9 | I/O | USART3_RX | STLK_TX [STM32F103CBT6_PA2] |
| 81 | PD12 | I/O | TIM4_CH1 | |
| 82 | PD13 | I/O | TIM4_CH2 | |
| 83 | VSS | Power | | |
| 84 | VDD | Power | | |
| 85 | PD14 | I/O | TIM4_CH3 | |
| 91 | PG6 * | I/O | GPIO_Output | USB_PowerSwitchOn [STMPS2151STR_EN] |
| 92 | PG7 * | I/O | GPIO_Input | USB_OverCurrent [STMPS2151STR_FAULT] |
| 94 | VSS | Power | | |
| 95 | VDDUSB | Power | | |
| 97 | PC7 | I/O | TIM3_CH2 | |
| 98 | PC8 | I/O | TIM3_CH3 | |
| 100 | PA8 | I/O | USB_OTG_FS_SOF | USB_SOF [TP1] |
| 101 | PA9 | I/O | USB_OTG_FS_VBUS | USB_VBUS |
| 102 | PA10 ** | I/O | USB_OTG_FS_ID | USB_ID |
| 103 | PA11 | I/O | USB_OTG_FS_DM | USB_DM |
| 104 | PA12 | I/O | USB_OTG_FS_DP | USB_DP |
| 105 | PA13 | I/O | SYS_JTMS-SWDIO | TMS |
| 106 | VCAP_2 | Power | | |
| 107 | VSS | Power | | |
| 108 | VDD | Power | | |
| 109 | PA14 | I/O | SYS_JTCK-SWCLK | TCK |
| 111 | PC10 | I/O | SPI3_SCK | |
| 112 | PC11 | I/O | SPI3_MISO | |
| 113 | PC12 | I/O | UART5_TX | |

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 114 | PD0 | I/O | CAN1_RX | |
| 115 | PD1 | I/O | CAN1_TX | |
| 116 | PD2 | I/O | UART5_RX | |
| 119 | PD5 | I/O | USART2_TX | |
| 120 | VSS | Power | | |
| 121 | VDDSDMMC | Power | | |
| 122 | PD6 | I/O | USART2_RX | |
| 126 | PG11 | I/O | ETH_TX_EN | RMII_TX_EN [LAN8742A-CZ-TR_TXEN] |
| 128 | PG13 | I/O | ETH_TXD0 | RMII_TXD0 [LAN8742A-CZ-TR_TXD0] |
| 130 | VSS | Power | | |
| 131 | VDD | Power | | |
| 133 | PB3 ** | I/O | SYS_JTDO-SWO | SWO |
| 136 | PB6 | I/O | CAN2_TX | |
| 137 | PB7 * | I/O | GPIO_Output | LD2 [Blue] |
| 138 | BOOT0 | Boot | | |
| 139 | PB8 | I/O | I2C1_SCL | |
| 140 | PB9 | I/O | I2C1_SDA | |
| 143 | PDR_ON | Reset | | |
| 144 | VDD | Power | | |

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

# 4. Clock Tree Configuration



# 5. Software Project

## 5.1. Project Settings

| Name | Value |
|---|---|
| Project Name | HorizonXIX_Firmware |
| Project Folder | D:\Dateien\Master\erc\Software_Atolic\FRoST_HorizonXIX_Firmware_Git |
| Toolchain / IDE | TrueSTUDIO |
| Firmware Package Name and Version | STM32Cube FW_F7 V1.15.0 |

## 5.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube Firmware Library Package | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files | Yes |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |

# 6. Power Consumption Calculator report

6.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32F7 |
| Line | STM32F7x7 |
| MCU | STM32F767ZITx |
| Datasheet | 029041_Rev4 |

6.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.6 |

# 7. IPs and Middleware Configuration

## 7.1. ADC1

**mode: IN4**

**mode: IN5**

**mode: IN9**

**mode: IN10**

**mode: IN12**

**mode: IN13**

**mode: Temperature Sensor Channel**

**mode: Vrefint Channel**

### 7.1.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | **PCLK2 divided by 8 *** |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | **Channel Temperature Sensor *** |
| Sampling Time | **28 Cycles *** |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## 7.2. ADC2

**mode: IN4**

**mode: IN5**

**mode: IN9**

**mode: IN10**

**mode: IN12**

**mode: IN13**

### 7.2.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | **PCLK2 divided by 8 *** |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel 4 |
| Sampling Time | **28 Cycles *** |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## 7.3. ADC3

**mode: IN10**

### 7.3.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | **PCLK2 divided by 8 *** |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel 10 |
| Sampling Time | 3 Cycles |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## *7.4. CAN1*

### mode: Mode

### 7.4.1. Parameter Settings:

**Bit Timings Parameters:**

| | |
|---|---|
| Prescaler (for Time Quantum) | **6 *** |
| Time Quantum | **111.11111111111111 *** |
| Time Quanta in Bit Segment 1 | **12 Times *** |
| Time Quanta in Bit Segment 2 | **5 Times *** |
| ReSynchronization Jump Width | 1 Time |

**Basic Parameters:**

| | |
|---|---|
| Time Triggered Communication Mode | Disable |
| Automatic Bus-Off Management | Disable |
| Automatic Wake-Up Mode | Disable |
| No-Automatic Retransmission | Disable |
| Receive Fifo Locked Mode | Disable |

| | |
|---|---|
| Transmit Fifo Priority | Disable |

**Advanced Parameters:**

| | |
|---|---|
| Operating Mode | Normal |

## 7.5. CAN2

**mode: Mode**

### 7.5.1. Parameter Settings:

**Bit Timings Parameters:**

| | |
|---|---|
| Prescaler (for Time Quantum) | **6 *** |
| Time Quantum | **111.11111111111111 *** |
| Time Quanta in Bit Segment 1 | **12 Times *** |
| Time Quanta in Bit Segment 2 | **5 Times *** |
| ReSynchronization Jump Width | 1 Time |

**Basic Parameters:**

| | |
|---|---|
| Time Triggered Communication Mode | Disable |
| Automatic Bus-Off Management | Disable |
| Automatic Wake-Up Mode | Disable |
| No-Automatic Retransmission | Disable |
| Receive Fifo Locked Mode | Disable |
| Transmit Fifo Priority | Disable |

**Advanced Parameters:**

| | |
|---|---|
| Operating Mode | Normal |

## 7.6. CORTEX_M7

### 7.6.1. Parameter Settings:

**Cortex Interface Settings:**

| | |
|---|---|
| Flash Interface | AXI Interface |
| ART ACCLERATOR | Disabled |
| Instruction Prefetch | Disabled |
| CPU ICache | Disabled |
| CPU DCache | Disabled |

**Cortex Memory Protection Unit Control Settings:**

| | |
|---|---|
| MPU Control Mode | MPU NOT USED |

## 7.7. ETH

### Mode: RMII

### 7.7.1. Parameter Settings:

**Advanced : Ethernet Media Configuration:**

| | |
|---|---|
| Auto Negotiation | Enabled |

**General : Ethernet Configuration:**

| | |
|---|---|
| Ethernet MAC Address | 00:80:E1:00:00:00 |
| PHY Address | **0 *** |

**Ethernet Basic Configuration:**

| | |
|---|---|
| Rx Mode | Interrupt Mode |
| TX IP Header Checksum Computation | By hardware |

### 7.7.2. Advanced Parameters:

**External PHY Configuration:**

| | |
|---|---|
| PHY | LAN8742A_PHY_ADDRESS |
| PHY Address Value | 0 |
| PHY Reset delay these values are based on a 1 ms Systick interrupt | **0x000000FF *** |
| PHY Configuration delay | **0x00000FFF *** |
| PHY Read TimeOut | **0x0000FFFF *** |
| PHY Write TimeOut | **0x0000FFFF *** |

**Common : External PHY Configuration:**

| | |
|---|---|
| Transceiver Basic Control Register | **0x00 *** |
| Transceiver Basic Status Register | **0x01 *** |
| PHY Reset | **0x8000 *** |
| Select loop-back mode | **0x4000 *** |
| Set the full-duplex mode at 100 Mb/s | **0x2100 *** |
| Set the half-duplex mode at 100 Mb/s | **0x2000 *** |
| Set the full-duplex mode at 10 Mb/s | **0x0100 *** |
| Set the half-duplex mode at 10 Mb/s | **0x0000 *** |
| Enable auto-negotiation function | **0x1000 *** |
| Restart auto-negotiation function | **0x0200 *** |
| Select the power down mode | **0x0800 *** |

| | |
|---|---|
| Isolate PHY from MII | **0x0400 *** |
| Auto-Negotiation process completed | **0x0020 *** |
| Valid link established | **0x0004 *** |
| Jabber condition detected | **0x0002 *** |

**Extended : External PHY Configuration:**

| | |
|---|---|
| PHY special control/status register Offset | **0x1F *** |
| PHY Speed mask | **0x0004 *** |
| PHY Duplex mask | **0x0010 *** |
| PHY Interrupt Source Flag register Offset | **0x001D *** |
| PHY Link down inturrupt | **0x000B *** |

## *7.8. GFXSIMULATOR*

### 7.8.1. Simulator Graphic:

## *7.9. I2C1*

### I2C: I2C

### 7.9.1. Parameter Settings:

**Timing configuration:**

| | |
|---|---|
| I2C Speed Mode | **Fast Mode *** |
| I2C Speed Frequency (KHz) | 400 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | **0x6000030D *** |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

## *7.10. I2C2*

### I2C: I2C

### 7.10.1. Parameter Settings:

**Timing configuration:**

| | |
|---|---|
| I2C Speed Mode | Standard Mode |
| I2C Speed Frequency (KHz) | 100 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | **0x20404768 *** |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

## *7.11. RCC*

**High Speed Clock (HSE): BYPASS Clock Source**

### 7.11.1. Parameter Settings:

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |
| Flash Latency(WS) | 7 WS (8 CPU cycle) |

**RCC Parameters:**

| | |
|---|---|
| HSI Calibration Value | 16 |
| TIM Prescaler Selection | Disabled |
| HSE Startup Timout Value (ms) | 100 |
| LSE Startup Timout Value (ms) | 5000 |

**Power Parameters:**

| | |
|---|---|
| Power Over Drive | Enabled |
| Power Regulatror Voltage Scale | Power Regulator Voltage Scale 1 |

## *7.12. SPI3*

**Mode: Full-Duplex Master**

### 7.12.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |
| Data Size | **8 Bits *** |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | **16 *** |
| Baud Rate | **3.375 MBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |
| NSS Signal Type | Software |

## *7.13. SPI4*

### Mode: Full-Duplex Master

### 7.13.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |
| Data Size | 4 Bits |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | 2 |
| Baud Rate | **54.0 MBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |
| NSS Signal Type | Software |

## *7.14. SYS*

### Debug: Serial Wire

**Timebase Source: TIM14**

## 7.15. TIM2

**Channel1: PWM Generation CH1**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

### 7.15.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 4:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

## 7.16. TIM3

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

### 7.16.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

## *7.17. TIM4*

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

### 7.17.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

## *7.18. TIM6*

### mode: Activated

### 7.18.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **5400-1 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **1 *** |
| auto-reload preload | **Enable *** |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

## *7.19. UART5*

### Mode: Asynchronous

### 7.19.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

## *7.20. USART2*

### Mode: Asynchronous

### 7.20.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

## 7.21. USART3

### Mode: Asynchronous

### 7.21.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

## 7.22. USB_OTG_FS

### Mode: Device_Only

### mode: Activate_SOF

### mode: Activate_VBUS

### 7.22.1. Parameter Settings:

| | |
|---|---|
| Speed | Device Full Speed 12MBit/s |
| Low power | Disabled |
| Link Power Management | Disabled |
| VBUS sensing | Enabled |
| Signal start of frame | Enabled |

## 7.23. FREERTOS

### Interface: CMSIS_V1

### 7.23.1. Config parameters:

**API:**

| | |
|---|---|
| FreeRTOS API | CMSIS v1 |

**Versions:**

| | |
|---|---|
| FreeRTOS version | 10.0.1 |
| CMSIS-RTOS version | 1.02 |

**Kernel settings:**

| | |
|---|---|
| USE_PREEMPTION | Enabled |
| CPU_CLOCK_HZ | SystemCoreClock |
| TICK_RATE_HZ | 1000 |
| MAX_PRIORITIES | 7 |
| MINIMAL_STACK_SIZE | 128 |
| MAX_TASK_NAME_LEN | **30 *** |
| USE_16_BIT_TICKS | Disabled |
| IDLE_SHOULD_YIELD | Enabled |
| USE_MUTEXES | Enabled |
| USE_RECURSIVE_MUTEXES | Disabled |
| USE_COUNTING_SEMAPHORES | Disabled |
| QUEUE_REGISTRY_SIZE | **16 *** |
| USE_APPLICATION_TASK_TAG | Disabled |
| ENABLE_BACKWARD_COMPATIBILITY | Enabled |
| USE_PORT_OPTIMISED_TASK_SELECTION | Enabled |
| USE_TICKLESS_IDLE | Disabled |
| USE_TASK_NOTIFICATIONS | Enabled |
| RECORD_STACK_HIGH_ADDRESS | Disabled |

**Memory management settings:**

| | |
|---|---|
| Memory Allocation | Dynamic |
| TOTAL_HEAP_SIZE | **61440 *** |
| Memory Management scheme | heap_4 |

**Hook function related definitions:**

| | |
|---|---|
| USE_IDLE_HOOK | **Enabled *** |
| USE_TICK_HOOK | Disabled |
| USE_MALLOC_FAILED_HOOK | Disabled |
| USE_DAEMON_TASK_STARTUP_HOOK | Disabled |
| CHECK_FOR_STACK_OVERFLOW | Disabled |

**Run time and task stats gathering related definitions:**

| | |
|---|---|
| GENERATE_RUN_TIME_STATS | **Enabled *** |
| USE_TRACE_FACILITY | **Enabled *** |
| USE_STATS_FORMATTING_FUNCTIONS | Disabled |

**Co-routine related definitions:**

| | |
|---|---|
| USE_CO_ROUTINES | Disabled |
| MAX_CO_ROUTINE_PRIORITIES | 2 |

**Software timer definitions:**

| | |
|---|---|
| USE_TIMERS | **Enabled *** |
| TIMER_TASK_PRIORITY | 2 |
| TIMER_QUEUE_LENGTH | 10 |
| TIMER_TASK_STACK_DEPTH | 256 |

**Interrupt nesting behaviour configuration:**

| | |
|---|---|
| LIBRARY_LOWEST_INTERRUPT_PRIORITY | 15 |
| LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY | 5 |

## 7.23.2. Include parameters:

**Include definitions:**

| | |
|---|---|
| vTaskPrioritySet | Enabled |
| uxTaskPriorityGet | Enabled |
| vTaskDelete | Enabled |
| vTaskCleanUpResources | Disabled |
| vTaskSuspend | Enabled |
| vTaskDelayUntil | Disabled |
| vTaskDelay | Enabled |
| xTaskGetSchedulerState | Enabled |
| xTaskResumeFromISR | Enabled |
| xQueueGetMutexHolder | Disabled |
| xSemaphoreGetMutexHolder | Disabled |
| pcTaskGetTaskName | Disabled |
| uxTaskGetStackHighWaterMark | Disabled |
| xTaskGetCurrentTaskHandle | Disabled |
| eTaskGetState | Disabled |
| xEventGroupSetBitFromISR | Disabled |
| xTimerPendFunctionCall | Disabled |
| xTaskAbortDelay | Disabled |
| xTaskGetHandle | Disabled |

## 7.24. LWIP

**mode: Enabled**

Advanced parameters are not listed except if modified by user.

### 7.24.1. General Settings:

| | |
|---|---|
| **LwIP Version:** | |
| LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **) | 2.0.3 |
| **IPv4 - DHCP Options:** | |
| LWIP_DHCP (DHCP Module) | **Disabled *** |
| **IP Address Settings:** | |
| IP_ADDRESS (IP Address) | **192.168.000.022 *** |
| NETMASK_ADDRESS (Netmask Address) | **255.255.255.000 *** |
| GATEWAY_ADDRESS (Gateway Address) | **192.168.000.001 *** |
| **RTOS Dependency:** | |
| WITH_RTOS (Use FREERTOS ** CubeMX specific **) | Enabled |
| **Protocols Options:** | |
| LWIP_ICMP (ICMP Module Activation) | Enabled |
| LWIP_IGMP (IGMP Module) | Disabled |
| LWIP_DNS (DNS Module) | Disabled |
| LWIP_UDP (UDP Module) | Enabled |
| MEMP_NUM_UDP_PCB (Number of UDP Connections) | **6 *** |
| LWIP_TCP (TCP Module) | Enabled |
| MEMP_NUM_TCP_PCB (Number of TCP Connections) | 5 |

### 7.24.2. Key Options:

| | |
|---|---|
| **Infrastructure - OS Awarness Option:** | |
| NO_SYS (OS Awarness) | OS Used |
| **Infrastructure - Timers Options:** | |
| LWIP_TIMERS (Use Support For sys_timeout) | Enabled |
| **Infrastructure - Core Locking and MPU Options:** | |
| SYS_LIGHTWEIGHT_PROT (Memory Functions Protection) | Enabled |
| **Infrastructure - Heap and Memory Pools Options:** | |
| MEM_SIZE (Heap Memory Size) | 1600 |
| **Infrastructure - Internal Memory Pool Sizes:** | |
| MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs) | 16 |
| MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks) | 4 |
| MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections) | 8 |

| | |
|---|---|
| MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued) | 16 |
| MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List) | 1 |

#### Pbuf Options:

| | |
|---|---|
| PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool) | 16 |
| PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool) | 592 |

#### IPv4 - ARP Options:

| | |
|---|---|
| LWIP_ARP (ARP Functionality) | Enabled |

#### Callback - TCP Options:

| | |
|---|---|
| TCP_TTL (Number of Time-To-Live Used by TCP Packets) | 255 |
| TCP_WND (TCP Receive Window Maximum Size) | 2144 |
| TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets) | Enabled |
| TCP_MSS (Maximum Segment Size) | 536 |
| TCP_SND_BUF (TCP Sender Buffer Space) | 1072 |
| TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender) | 9 |

#### Network Interfaces Options:

| | |
|---|---|
| LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes) | Disabled |
| LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes) | Disabled |

#### NETIF - Loopback Interface Options:

| | |
|---|---|
| LWIP_NETIF_LOOPBACK (NETIF Loopback) | Disabled |

#### Infrastructure - Threading Options:

| | |
|---|---|
| TCPIP_THREAD_NAME (TCPIP Thread Name) | "tcpip_thread" |
| TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size) | 1024 |
| TCPIP_THREAD_PRIO (TCPIP Thread Priority Level) | 3 |
| TCPIP_MBOX_SIZE (TCPIP Mailbox Size) | 6 |
| DEFAULT_THREAD_NAME (Default LwIP Thread Name) | "lwIP" |
| DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size) | 1024 |
| DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level) | 3 |
| DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw) | 0 |
| DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP) | 6 |
| DEFAULT_ACCEPTMBOX_SIZE (Default Mailbox Size for Incoming Connections) | 6 |

#### Thread Safe APIs - Netconn Options:

| | |
|---|---|
| LWIP_NETCONN (NETCONN API) | Enabled |

#### Thread Safe APIs - Socket Options:

| | |
|---|---|
| LWIP_SOCKET (Socket API) | Enabled |
| LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names) | 1 |
| LWIP_SOCKET_OFFSET (Socket Offset Number) | 0 |

### 7.24.3. PPP:

#### PPP Options:

| | |
|---|---|
| PPP_SUPPORT (PPP Module) | Disabled |

### 7.24.4. IPv6:

**IPv6 Options:**

| | |
|---|---|
| LWIP_IPV6 (IPv6 Protocol) | Disabled |

### 7.24.5. HTTPD:

**HTTPD Options:**

| | |
|---|---|
| LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **) | Disabled |

### 7.24.6. SNMP:

**SNMP Options:**

| | |
|---|---|
| LWIP_SNMP (LwIP SNMP Agent) | Disabled |

### 7.24.7. SNTP:

**SNTP Options:**

| | |
|---|---|
| LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **) | Disabled |

### 7.24.8. MDNS/TFTP:

**MDNS Options:**

| | |
|---|---|
| LWIP_MDNS (Multicast DNS Support ** CubeMX specific **) | Disabled |

**TFTP Options:**

| | |
|---|---|
| LWIP_TFTP (TFTP Support ** CubeMX specific **) | Disabled |

### 7.24.9. Perf/Checks:

**Sanity Checks:**

| | |
|---|---|
| LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks) | Disabled |
| LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks) | Disabled |

**Performance Options:**

| | |
|---|---|
| LWIP_PERF (Performace Testing for LwIP) | Disabled |

## 7.24.10. Statistics:

### Debug - Statistics Options:

| | |
|---|---|
| LWIP_STATS (Statictics Collection) | Disabled |

## 7.24.11. Checksum:

### Infrastructure - Checksum Options:

| | |
|---|---|
| CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **) | Disabled |
| LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif) | Disabled |
| CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets) | Disabled |
| CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets) | Disabled |
| CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets) | Disabled |
| CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets) | Disabled |
| CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets) | Disabled |
| CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets) | Disabled |
| CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets) | Disabled |
| CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets) | Disabled |
| CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets) | Disabled |
| CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets) | Disabled |

## 7.24.12. Debug:

### LwIP Main Debugging Options:

| | |
|---|---|
| LWIP_DBG_MIN_LEVEL (Minimum Level) | All |

*** User modified value**

# 8. System Configuration

## 8.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC1 | PC0 | ADC1_IN10 | Analog mode | No pull-up and no pull-down | n/a | |
| | PC2 | ADC1_IN12 | Analog mode | No pull-up and no pull-down | n/a | |
| | PC3 | ADC1_IN13 | Analog mode | No pull-up and no pull-down | n/a | |
| | PA4 | ADC1_IN4 | Analog mode | No pull-up and no pull-down | n/a | |
| | PA5 | ADC1_IN5 | Analog mode | No pull-up and no pull-down | n/a | |
| | PB1 | ADC1_IN9 | Analog mode | No pull-up and no pull-down | n/a | |
| ADC2 | PC0 | ADC2_IN10 | Analog mode | No pull-up and no pull-down | n/a | |
| | PC2 | ADC2_IN12 | Analog mode | No pull-up and no pull-down | n/a | |
| | PC3 | ADC2_IN13 | Analog mode | No pull-up and no pull-down | n/a | |
| | PA4 | ADC2_IN4 | Analog mode | No pull-up and no pull-down | n/a | |
| | PA5 | ADC2_IN5 | Analog mode | No pull-up and no pull-down | n/a | |
| | PB1 | ADC2_IN9 | Analog mode | No pull-up and no pull-down | n/a | |
| ADC3 | PC0 | ADC3_IN10 | Analog mode | No pull-up and no pull-down | n/a | |
| CAN1 | PD0 | CAN1_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PD1 | CAN1_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| CAN2 | PB12 | CAN2_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PB6 | CAN2_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| ETH | PC1 | ETH_MDC | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_MDC [LAN8742A-CZ-TR_MDC] |
| | PA1 | ETH_REF_CLK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0] |
| | PA2 | ETH_MDIO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_MDIO [LAN8742A-CZ-TR_MDIO] |
| | PA7 | ETH_CRS_DV | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV] |
| | PC4 | ETH_RXD0 | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_RXD0 [LAN8742A-CZ-TR_RXD0] |
| | PC5 | ETH_RXD1 | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_RXD1 [LAN8742A-CZ-TR_RXD1] |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | PB13 | ETH_TXD1 | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_TXD1 [LAN8742A-CZ-TR_TXD1] |
| | PG11 | ETH_TX_EN | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_TX_EN [LAN8742A-CZ-TR_TXEN] |
| | PG13 | ETH_TXD0 | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_TXD0 [LAN8742A-CZ-TR_TXD0] |
| I2C1 | PB8 | I2C1_SCL | Alternate Function Open Drain | Pull-up | **Very High *** | |
| | PB9 | I2C1_SDA | Alternate Function Open Drain | Pull-up | **Very High *** | |
| I2C2 | PF0 | I2C2_SDA | Alternate Function Open Drain | Pull-up | **Very High *** | |
| | PF1 | I2C2_SCL | Alternate Function Open Drain | Pull-up | **Very High *** | |
| RCC | PH0/OSC_IN | RCC_OSC_IN | n/a | n/a | n/a | MCO [STM32F103CBT6_PA8] |
| | PH1/OSC_OUT | RCC_OSC_OUT | n/a | n/a | n/a | |
| SPI3 | PB2 | SPI3_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PC10 | SPI3_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PC11 | SPI3_MISO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| SPI4 | PE2 | SPI4_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PE5 | SPI4_MISO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PE6 | SPI4_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| SYS | PA13 | SYS_JTMS-SWDIO | n/a | n/a | n/a | TMS |
| | PA14 | SYS_JTCK-SWCLK | n/a | n/a | n/a | TCK |
| TIM2 | PA0/WKUP | TIM2_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA3 | TIM2_CH4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PB10 | TIM2_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| TIM3 | PA6 | TIM3_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PC7 | TIM3_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | PC8 | TIM3_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| TIM4 | PD12 | TIM4_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD13 | TIM4_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD14 | TIM4_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| UART5 | PC12 | UART5_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PD2 | UART5_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| USART2 | PD5 | USART2_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PD6 | USART2_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| USART3 | PD8 | USART3_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | STLK_RX [STM32F103CBT6_PA3] |
| | PD9 | USART3_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | STLK_TX [STM32F103CBT6_PA2] |
| USB_OTG_FS | PA8 | USB_OTG_FS_SOF | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | USB_SOF [TP1] |
| | PA9 | USB_OTG_FS_VBUS | Input mode | No pull-up and no pull-down | **n/a** | USB_VBUS |
| | PA11 | USB_OTG_FS_DM | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | USB_DM |
| | PA12 | USB_OTG_FS_DP | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | USB_DP |
| Single Mapped Signals | PC14/OSC32_IN | RCC_OSC32_IN | n/a | n/a | n/a | |
| | PC15/OSC32_OUT | RCC_OSC32_OUT | n/a | n/a | n/a | |
| | PA10 | USB_OTG_FS_ID | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | USB_ID |
| | PB3 | SYS_JTDO-SWO | n/a | n/a | **n/a** | SWO |
| GPIO | PE3 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PE4 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PC13 | GPIO_EXTI13 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | USER_Btn [B1] |
| | PF2 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PF3 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PF4 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | | | | | | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | PF5 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PF6 | GPIO_Output | Output Push Pull | **Pull-down *** | **High *** | |
| | PF7 | GPIO_Output | Output Push Pull | **Pull-down *** | **High *** | |
| | PF8 | GPIO_Output | Output Push Pull | **Pull-down *** | **High *** | |
| | PF9 | GPIO_Output | Output Push Pull | **Pull-down *** | **High *** | |
| | PF10 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PB0 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | LD1 |
| | PF11 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PF12 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PF13 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PF14 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PF15 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PG0 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | IO_OUT_CONTROL |
| | PG1 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | IO_OUT_LOAD |
| | PE7 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PE8 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PE9 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PE10 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PE11 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PE12 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PE13 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PE14 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PE15 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PB11 | GPIO_Input | Input mode | **Pull-down *** | n/a | |
| | PB14 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | LD3 [Red] |
| | PB15 | GPIO_Input | Input mode | **Pull-down *** | n/a | |
| | PG6 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | USB_PowerSwitchOn [STMPS2151STR_EN] |
| | PG7 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | USB_OverCurrent [STMPS2151STR_FAULT] |
| | PB7 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | LD2 [Blue] |

## *8.2. DMA configuration*

nothing configured in DMA service

## 8.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 1 | 0 |
| Pre-fetch fault, memory access fault | true | 1 | 0 |
| Undefined instruction or illegal state | true | 1 | 0 |
| System service call via SWI instruction | true | 1 | 0 |
| Debug monitor | true | 1 | 0 |
| Pendable request for system service | true | 15 | 0 |
| System tick timer | true | 15 | 0 |
| ADC1, ADC2 and ADC3 global interrupts | true | 5 | 0 |
| CAN1 RX0 interrupts | true | 5 | 0 |
| CAN1 RX1 interrupt | true | 5 | 0 |
| EXTI line[15:10] interrupts | true | 5 | 0 |
| TIM8 trigger and commutation interrupts and TIM14 global interrupt | true | 0 | 0 |
| TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts | true | 5 | 0 |
| Ethernet global interrupt | true | 5 | 0 |
| CAN2 RX0 interrupts | true | 5 | 0 |
| CAN2 RX1 interrupt | true | 5 | 0 |
| PVD interrupt through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| CAN1 TX interrupts | unused | | |
| CAN1 SCE interrupt | unused | | |
| TIM2 global interrupt | unused | | |
| TIM3 global interrupt | unused | | |
| TIM4 global interrupt | unused | | |
| I2C1 event interrupt | unused | | |
| I2C1 error interrupt | unused | | |
| I2C2 event interrupt | unused | | |
| I2C2 error interrupt | unused | | |
| USART2 global interrupt | unused | | |
| USART3 global interrupt | unused | | |
| SPI3 global interrupt | unused | | |
| UART5 global interrupt | unused | | |
| Ethernet wake-up interrupt through EXTI line 19 | unused | | |
| CAN2 TX interrupts | unused | | |
| CAN2 SCE interrupt | unused | | |
| | | | |

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| USB On The Go FS global interrupt | unused | | |
| FPU global interrupt | unused | | |
| SPI4 global interrupt | unused | | |

*** User modified value**

# 9. Software Pack Report