1. Description

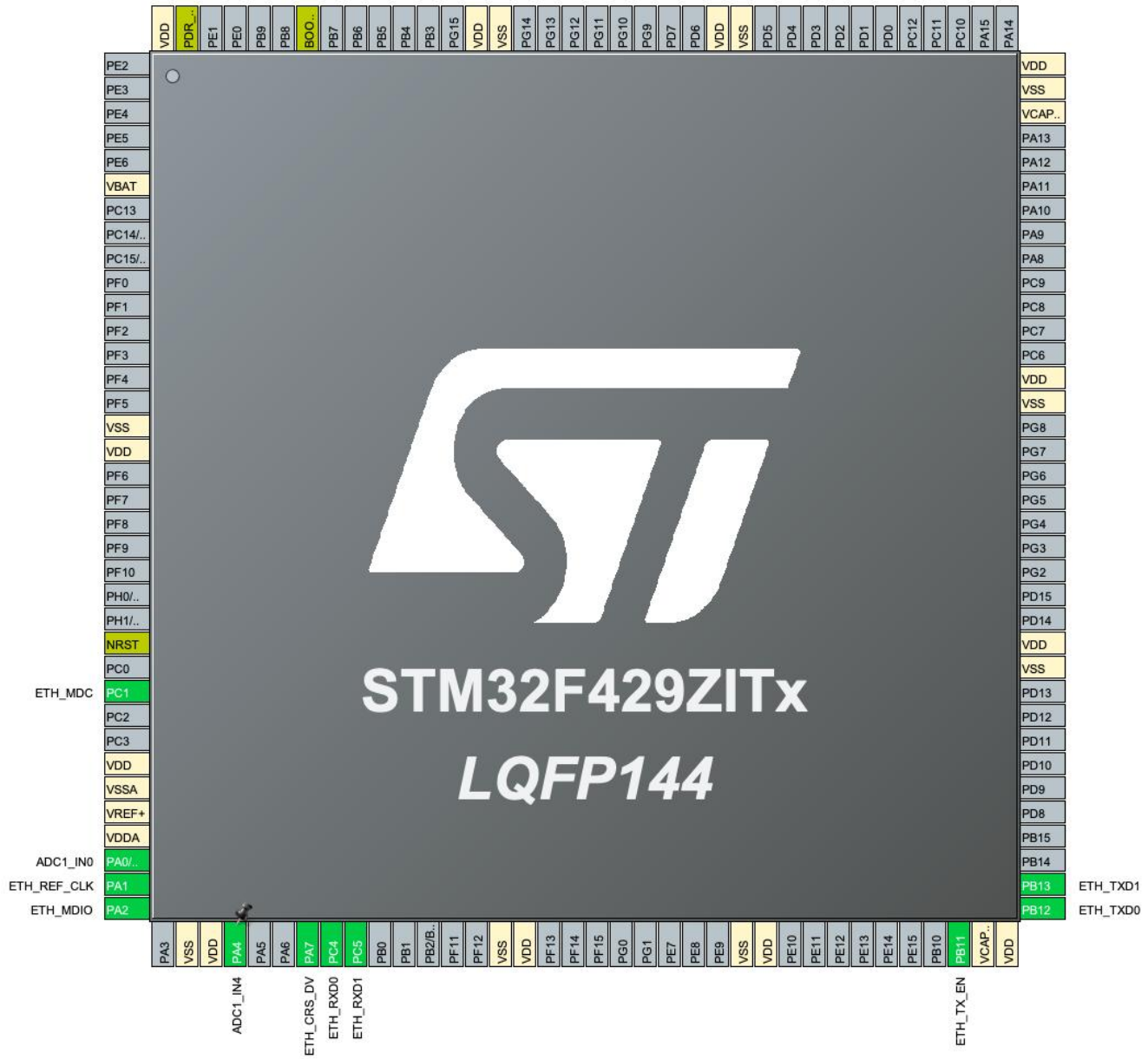
1.1. Project

Project Name	adcadcadc
Board Name	custom
Generated with:	STM32CubeMX 5.4.0
Date	12/23/2019

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration

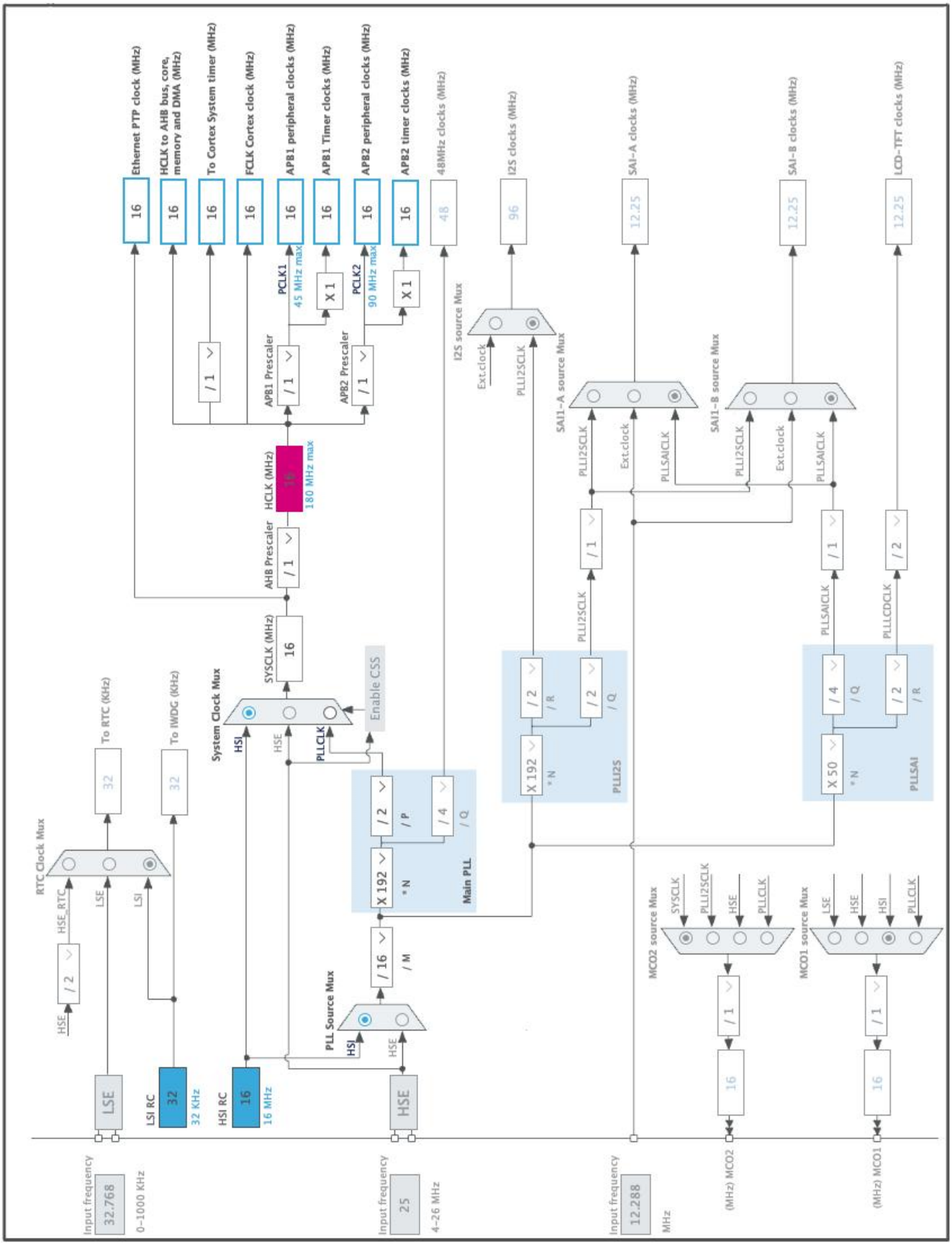


3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
25	NRST	Reset		
27	PC1	I/O	ETH_MDC	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	ADC1_IN0	
35	PA1	I/O	ETH_REF_CLK	
36	PA2	I/O	ETH_MDIO	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	ADC1_IN4	
43	PA7	I/O	ETH_CRS_DV	
44	PC4	I/O	ETH_RXD0	
45	PC5	I/O	ETH_RXD1	
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
70	PB11	I/O	ETH_TX_EN	
71	VCAP_1	Power		
72	VDD	Power		
73	PB12	I/O	ETH_TXD0	
74	PB13	I/O	ETH_TXD1	
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDD	Power		
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
120	VSS	Power		
121	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
130	VSS	Power		
131	VDD	Power		
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	adcadcadc
Project Folder	/Users/sungjinkim/stm32workspace00/adcadcadc
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.24.2

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429ZITx
Datasheet	024030_Rev9

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN0

mode: IN4

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles
Rank	**2 ***
Channel	**Channel 4 ***
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. ETH

Mode: RMII

7.2.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	1

Ethernet Basic Configuration:

Rx Mode	Polling Mode
TX IP Header Checksum Computation	By hardware

7.2.2. Advanced Parameters:

External PHY Configuration:

PHY	LAN8742A_PHY_ADDRESS
PHY Address Value	1
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset

	0x1F *
PHY Speed mask	**0x0004 ***
PHY Duplex mask	**0x0010 ***
PHY Interrupt Source Flag register Offset	**0x001D ***
PHY Link down inturrupt	**0x000B ***

7.3. GFXSIMULATOR

7.3.1. Simulator Graphic:

7.4. GPIO

7.5. SYS

Timebase Source: SysTick

7.6. TIM2

Clock Source : Internal Clock

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**8399 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**9999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0/WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM2 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report