1. Description

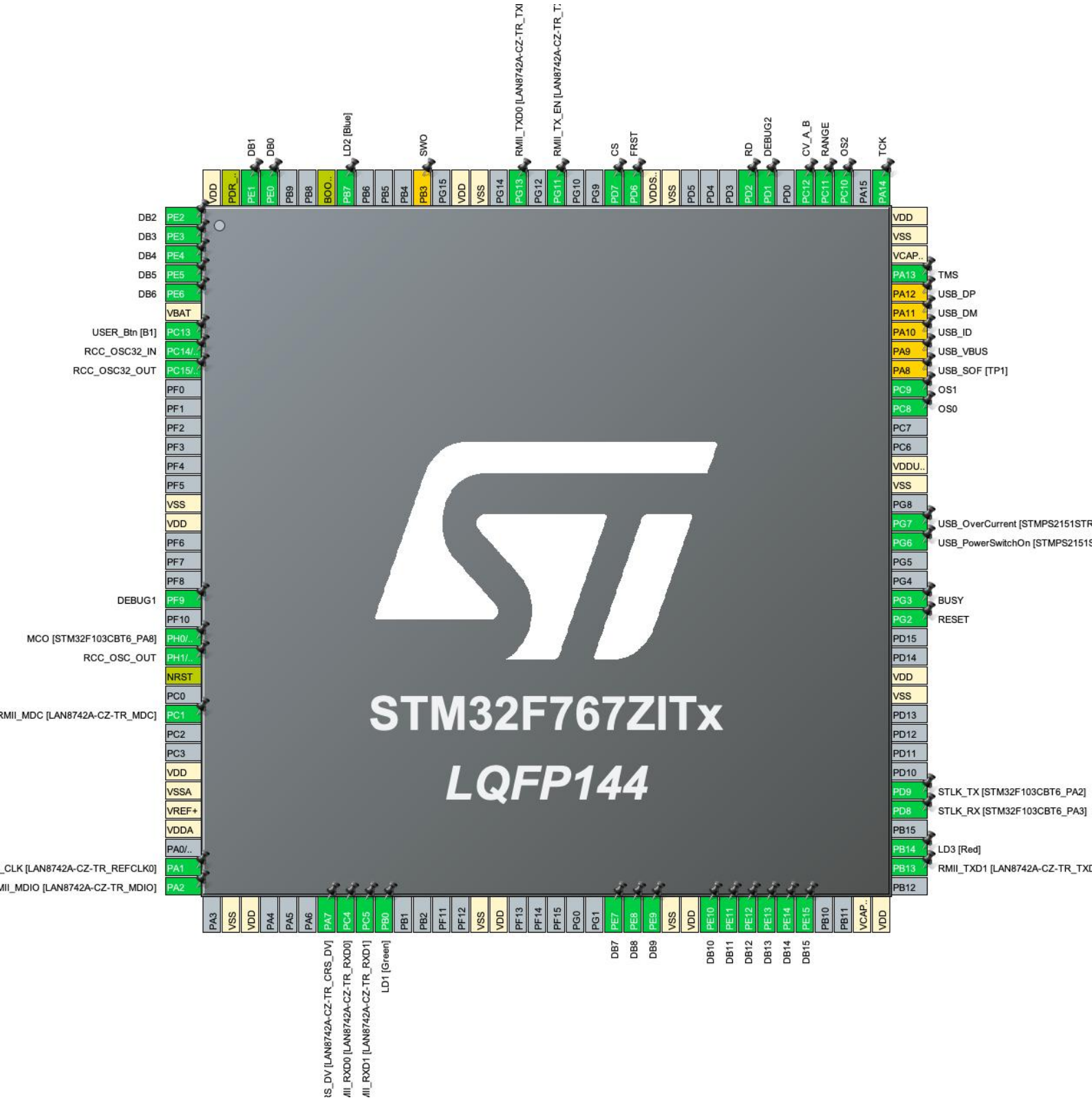
1.1. Project

Project Name	AD7606
Board Name	NUCLEO-F767ZI
Generated with:	STM32CubeMX 5.4.0
Date	12/15/2019

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Input	DB2
2	PE3 *	I/O	GPIO_Input	DB3
3	PE4 *	I/O	GPIO_Input	DB4
4	PE5 *	I/O	GPIO_Input	DB5
5	PE6 *	I/O	GPIO_Input	DB6
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	USER_Btn [B1]
8	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
16	VSS	Power		
17	VDD	Power		
21	PF9 *	I/O	GPIO_Output	DEBUG1
23	PH0/OSC_IN	I/O	RCC_OSC_IN	MCO [STM32F103CBT6_PA8]
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
27	PC1	I/O	ETH_MDC	RMII_MDC [LAN8742A-CZ-TR_MDC]
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
35	PA1	I/O	ETH_REF_CLK	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
36	PA2	I/O	ETH_MDIO	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
38	VSS	Power		
39	VDD	Power		
43	PA7	I/O	ETH_CRS_DV	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]
44	PC4	I/O	ETH_RXD0	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
45	PC5	I/O	ETH_RXD1	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
46	PB0 *	I/O	GPIO_Output	LD1 [Green]
51	VSS	Power		

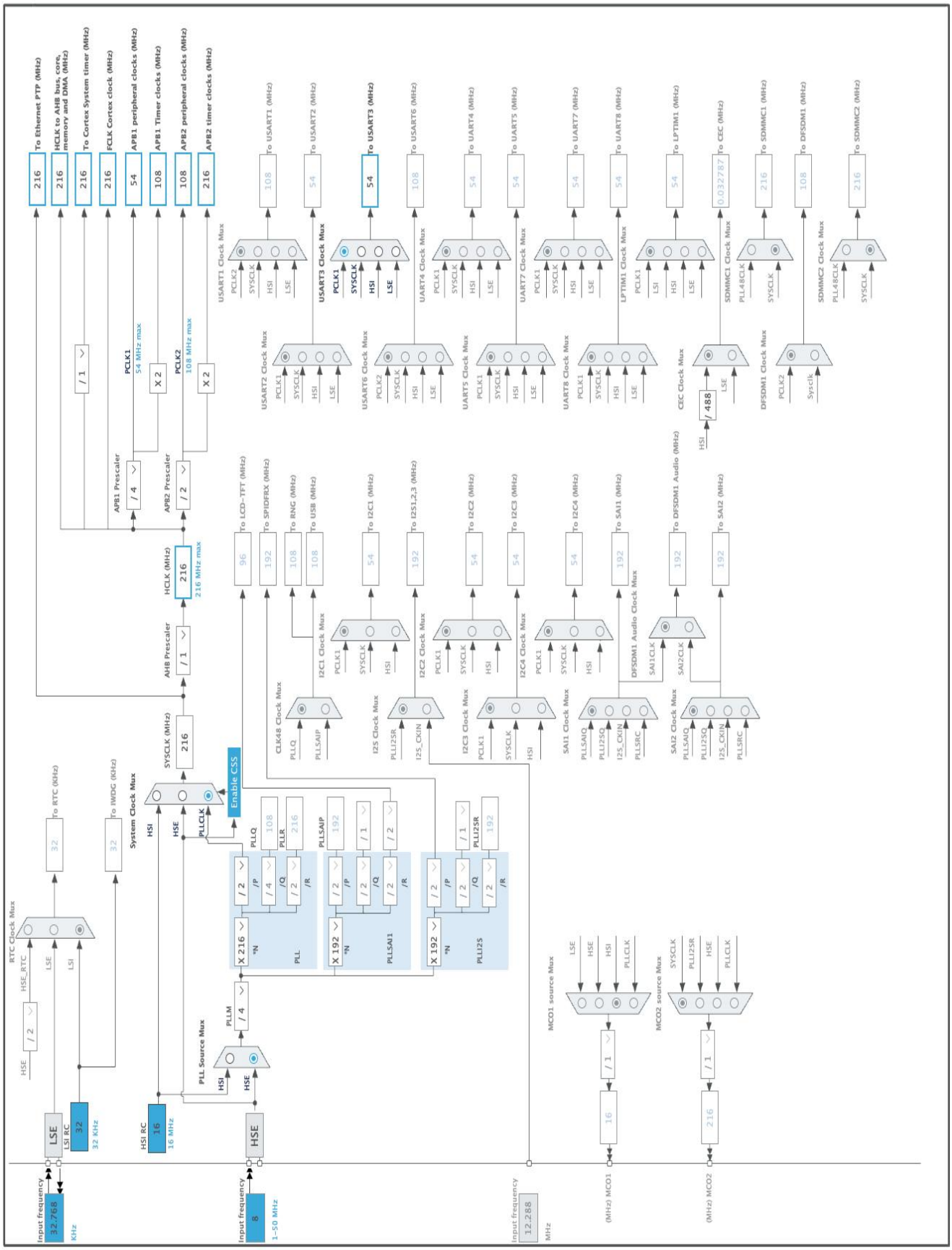
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
52	VDD	Power		
58	PE7 *	I/O	GPIO_Input	DB7
59	PE8 *	I/O	GPIO_Input	DB8
60	PE9 *	I/O	GPIO_Input	DB9
61	VSS	Power		
62	VDD	Power		
63	PE10 *	I/O	GPIO_Input	DB10
64	PE11 *	I/O	GPIO_Input	DB11
65	PE12 *	I/O	GPIO_Input	DB12
66	PE13 *	I/O	GPIO_Input	DB13
67	PE14 *	I/O	GPIO_Input	DB14
68	PE15 *	I/O	GPIO_Input	DB15
71	VCAP_1	Power		
72	VDD	Power		
74	PB13	I/O	ETH_TXD1	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
75	PB14 *	I/O	GPIO_Output	LD3 [Red]
77	PD8	I/O	USART3_TX	STLK_RX [STM32F103CBT6_PA3]
78	PD9	I/O	USART3_RX	STLK_TX [STM32F103CBT6_PA2]
83	VSS	Power		
84	VDD	Power		
87	PG2 *	I/O	GPIO_Output	RESET
88	PG3 *	I/O	GPIO_Input	BUSY
91	PG6 *	I/O	GPIO_Output	USB_PowerSwitchOn [STMPS2151STR_EN]
92	PG7 *	I/O	GPIO_Input	USB_OverCurrent [STMPS2151STR_FAULT]
94	VSS	Power		
95	VDDUSB	Power		
98	PC8 *	I/O	GPIO_Output	OS0
99	PC9 *	I/O	GPIO_Output	OS1
100	PA8 **	I/O	USB_OTG_FS_SOF	USB_SOF [TP1]
101	PA9 **	I/O	USB_OTG_FS_VBUS	USB_VBUS
102	PA10 **	I/O	USB_OTG_FS_ID	USB_ID
103	PA11 **	I/O	USB_OTG_FS_DM	USB_DM
104	PA12 **	I/O	USB_OTG_FS_DP	USB_DP
105	PA13	I/O	SYS_JTMS-SWDIO	TMS
106	VCAP_2	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	TCK
111	PC10 *	I/O	GPIO_Output	OS2
112	PC11 *	I/O	GPIO_Output	RANGE
113	PC12 *	I/O	GPIO_Output	CV_A_B
115	PD1 *	I/O	GPIO_Output	DEBUG2
116	PD2 *	I/O	GPIO_Output	RD
120	VSS	Power		
121	VDDSDMMC	Power		
122	PD6 *	I/O	GPIO_Input	FRST
123	PD7 *	I/O	GPIO_Output	CS
126	PG11	I/O	ETH_TX_EN	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
128	PG13	I/O	ETH_TXD0	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
130	VSS	Power		
131	VDD	Power		
133	PB3 **	I/O	SYS_JTDO-SWO	SWO
137	PB7 *	I/O	GPIO_Output	LD2 [Blue]
138	BOOT0	Boot		
141	PE0 *	I/O	GPIO_Input	DB0
142	PE1 *	I/O	GPIO_Input	DB1
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	AD7606
Project Folder	/Users/christiansager/klanghabitat_quantum/firmware/STM32_Workspace/AD760
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F7 V1.15.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	029041_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.6

7. IPs and Middleware Configuration

7.1. ETH

Mode: RMII

7.1.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	**0 ***

Ethernet Basic Configuration:

Rx Mode	Polling Mode
TX IP Header Checksum Computation	By hardware

7.1.2. Advanced Parameters:

External PHY Configuration:

PHY	LAN8742A_PHY_ADDRESS
PHY Address Value	0
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***

Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x1F ***
PHY Speed mask	**0x0004 ***
PHY Duplex mask	**0x0010 ***
PHY Interrupt Source Flag register Offset	**0x001D ***
PHY Link down inturrupt	**0x000B ***

7.2. GFXSIMULATOR

7.2.1. Simulator Graphic:

7.3. GPIO

7.4. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.5. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.6. TIM6

mode: Activated

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**216 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.7. TIM7

mode: Activated

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**216 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.8. USART3

Mode: Asynchronous

7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_MDC [LAN8742A-CZ-TR_MDC]
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO [STM32F103CBT6_PA8]
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	STLK_RX [STM32F103CBT6_PA3]
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	STLK_TX [STM32F103CBT6_PA2]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
Single Mapped Signals	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_SOF [TP1]
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	**n/a**	USB_VBUS
	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_ID
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DM
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DP
	PB3	SYS_JTDO-SWO	n/a	n/a	**n/a**	SWO
GPIO	PE2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB2
	PE3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB3
	PE4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB4
	PE5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB5
	PE6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB6
	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USER_Btn [B1]
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DEBUG1
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 [Green]
	PE7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB7
	PE8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB8
	PE9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB9
	PE10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB10
	PE11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB11
	PE12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB12
	PE13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB13
	PE14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB14
	PE15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB15
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red]
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RESET
	PG3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BUSY
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OverCurrent [STMPS2151STR_FAULT]
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OS0
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OS1
	PC10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OS2
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RANGE

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CV_A_B
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DEBUG2
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RD
	PD6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	FRST
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CS
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Blue]
	PE0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB0
	PE1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB1

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0
TIM7 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART3 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report