

February 2008

# MM74HC00 Quad 2-Input NAND Gate

#### **Features**

Typical propagation delay: 8nsWide power supply range: 2V–6V

■ Low quiescent current: 20µA maximum (74HC Series)

■ Low input current: 1µA maximum

■ Fanout of 10 LS-TTL loads

## **General Description**

The MM74HC00 NAND gates utilize advanced silicongate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{\rm CC}$  and ground.

## **Ordering Information**

Order Number	Package Number	Package Description
MM74HC00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC00MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC00N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

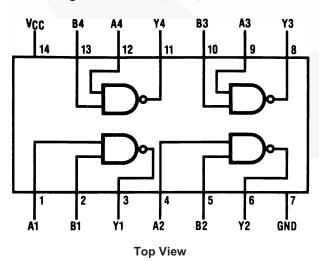
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



All packages are lead free per JEDEC: J-STD-020B standard.

## **Connection Diagram**

Pin Assignments for DIP, SOIC, SOP and TSSOP



### **Logic Diagram**

## Absolute Maximum Ratings<sup>(1)</sup>

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V <sub>CC</sub>	Supply Voltage	-0.5 to +7.0V
V <sub>IN</sub>	DC Input Voltage	–1.5 to V <sub>CC</sub> +1.5V
V <sub>OUT</sub>	DC Output Voltage	–0.5 to V <sub>CC</sub> +0.5V
I <sub>IK</sub> , I <sub>OK</sub>	Clamp Diode Current	±20mA
I <sub>OUT</sub>	DC Output Current, per pin	±25mA
I <sub>CC</sub>	DC V <sub>CC</sub> or GND Current, per pin	±50mA
T <sub>STG</sub>	Storage Temperature Range	−65°C to +150°C
P <sub>D</sub>	Power Dissipation Note 2	600mW
	S.O. Package only	500mW
TL	Lead Temperature (Soldering 10 seconds)	260°C

#### Notes:

- 1. Unless otherwise specified all voltages are referenced to ground.
- 2. Power Dissipation temperature derating plastic "N" package: -12mW/°C from 65°C to 85°C.

## **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V <sub>CC</sub>	Supply Voltage	2	6	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input or Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature Range	-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Times			
	$V_{CC} = 2.0V$		1000	ns
	$V_{CC} = 4.5V$		500	ns
	V <sub>CC</sub> = 6.0V		400	ns

## DC Electrical Characteristics<sup>(3)</sup>

				<b>T</b> <sub>A</sub> =	25°C	T <sub>A</sub> =-40°C to 85°C	T <sub>A</sub> = -55°C to 125°C	
Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	Тур.		Guaranteed	Limits	Units
V <sub>IH</sub>	Minimum HIGH Level	2.0			1.5	1.5	1.5	V
	Input Voltage	4.5			3.15	3.15	3.15	
		6.0			4.2	4.2	4.2	
V <sub>IL</sub>	Maximum LOW Level	2.0			0.5	0.5	0.5	V
	Input Voltage	4.5			1.35	1.35	1.35	
		6.0			1.8	1.8	1.8	
V <sub>OH</sub>	Minimum HIGH Level	2.0	$V_{IN} = V_{IH}$ or $V_{IL}$ ,	2.0	1.9	1.9	1.9	V
	Output Voltage	4.5	I <sub>OUT</sub>   ≤ 20μA	4.5	4.4	4.4	4.4	
		6.0		6.0	5.9	5.9	5.9	
		4.5	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $ I_{OUT}  \le 4.0 \text{mA}$	4.2	3.98	3.84	3.7	
		6.0	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $ I_{OUT}  \le 5.2 \text{mA}$	5.7	5.48	5.34	5.2	
V <sub>OL</sub>		2.0	$V_{IN} = V_{IH},$	0	0.1	0.1	0.1	V
	Output Voltage	4.5	I <sub>OUT</sub>   ≤ 20μA	0	0.1	0.1	0.1	
		6.0		0	0.1	0.1	0.1	
		4.5	$V_{IN} = V_{IH},$ $ I_{OUT}  \le 4.0 \text{mA}$	0.2	0.26	0.33	0.4	
		6.0	$V_{IN} = V_{IH},$ $ I_{OUT}  \le 5.2 \text{mA}$	0.2	0.26	0.33	0.4	
I <sub>IN</sub>	Maximum Input Current	6.0	$V_{IN} = V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Icc	Maximum Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$		2.0	20	40	μA

#### Note:

3. For a power supply of 5V  $\pm 10\%$  the worst case output voltages (V<sub>OH</sub>, and V<sub>OL</sub>) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V<sub>IH</sub> and V<sub>IL</sub> occur at V<sub>CC</sub> = 5.5V and 4.5V respectively. (The V<sub>IH</sub> value at 5.5V is 3.85V.) The worst case leakage current (I<sub>IN</sub>, I<sub>CC</sub>, and I<sub>OZ</sub>) occur for CMOS at the higher voltage and so the 6.0V values should be used.

## **AC Electrical Characteristics**

 $V_{CC}$  = 5V,  $T_A$  = 25°C,  $C_L$  = 15pF,  $t_r$  =  $t_f$  = 6ns

Symbol	Parameter	Conditions	Тур.	Guaranteed Limit	Units
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay		8	15	ns

## **AC Electrical Characteristics**

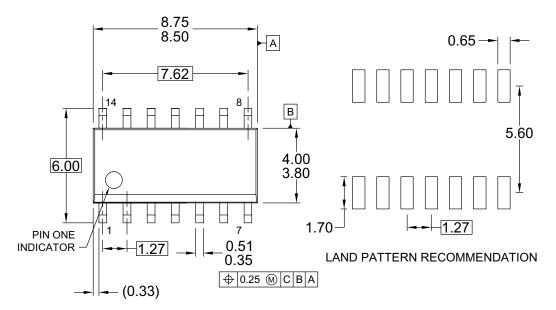
 $V_{CC}$  = 2.0V to 6.0V,  $C_L$  = 50pF,  $t_r$  =  $t_f$  = 6ns (unless otherwise specified)

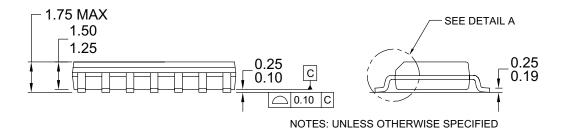
				<b>T</b> <sub>A</sub> =	25°C	T <sub>A</sub> = -40°C to 85°C	T <sub>A</sub> = -55°C to 125°C	
Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	Тур.		Guaranteed	Limits	Units
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum	2.0		45	90	113	134	ns
	Propagation Delay	4.5		9	18	23	27	1
		6.0		8	15	19	23	1
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output	2.0		30	75	95	110	ns
Rise and Fall 1	Rise and Fall Time	4.5		8	15	19	22	
		6.0		7	13	16	19	1
C <sub>PD</sub>	Power Dissipation Capacitance <sup>(4)</sup>		(per gate)	20				pF
C <sub>IN</sub>	Maximum Input Capacitance			5	10	10	10	pF

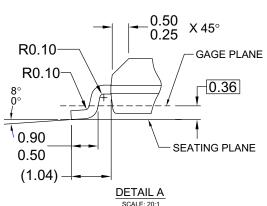
#### Note

4.  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} \ V_{CC} \ f + I_{CC}$ .

## **Physical Dimensions**







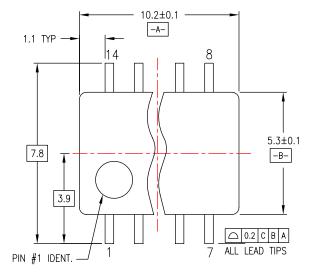
- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

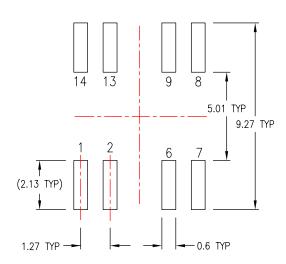
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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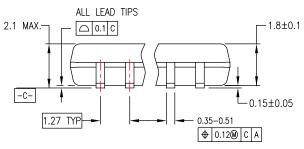
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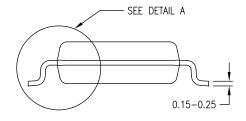
## Physical Dimensions (Continued)





#### LAND PATTERN RECOMMENDATION

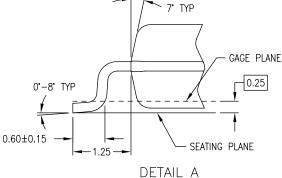




DIMENSIONS ARE IN MILLIMETERS

#### NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  B. DIMENSIONS ARE IN MILLIMETERS.
  C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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#### Physical Dimensions (Continued) 5.0±0.1 -A-0.65 0.43 TYP 6.4 4.4±0.1 -B-1.65 3.2 □ 0.2 C B A PIN #1 IDENT. 6.10 0.45 -LAND PATTERN RECOMMENDATION SEE DETAIL A ALL LEAD TIPS 0.90+0.15 1.2 MAX □ 0.1 C 0.09-0.20 -C-0.10±0.05 0.65 0.19 - 0.30⊕ |0.13\\(\) |A |B\(\) |C\(\) 12.00°TOP & BOTTOM R0.09 min GAGE PLANE 0.25 0°-8° NOTES: 0.6±0.1 A. CONFORMS TO JEDEC REGISTRATION MO-153, SEATING PLANE R0.09min VARIATION AB, REF NOTE 6 -1 00 **DETAIL A**

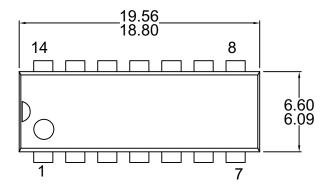
- **B. DIMENSIONS ARE IN MILLIMETERS**
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

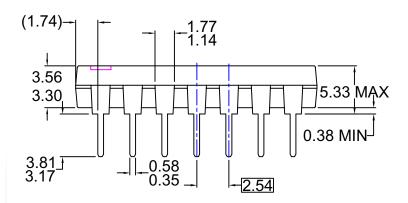
Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

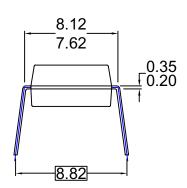
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## Physical Dimensions (Continued)







NOTES: UNLESS OTHERWISE SPECIFIED THIS PACKAGE CONFORMS TO

- A) JEDEC MS-001 VARIATION BA
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
  DIMENSIONS ARE EXCLUSIVE OF BURRS.
- C) MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DIMENSIONS AND TOLERANCES PER ASME Y14.5-1994
- E) DRAWING FILE NAME: MKT-N14AREV7

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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