

September 1983 Revised January 2005

MM74HC393 **Dual 4-Bit Binary Counter**

General Description

The MM74HC393 counter circuits contain independent ripple carry counters and utilize advanced silicon-gate CMOS technology. The MM74HC393 contains two 4-bit ripple carry binary counters, which can be cascaded to create a single divide-by-256 counter.

Each of the two 4-bit counters is incremented on the HIGHto-LOW transition (negative edge) of the clock input, and each has an independent clear input. When clear is set HIGH all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

Each of the counters outputs can drive 10 low power Schottky TTL equivalent loads. This counter is functionally as well as pin equivalent to the 74LS393. All inputs are protected from damage due to static discharge by diodes to $V_{\mbox{\footnotesize CC}}$ and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 13 ns (Ck to Q_A)
- Wide operating supply voltage range: 2-6V
- Low input current: <1 µA
- Low quiescent supply current: 80 µA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

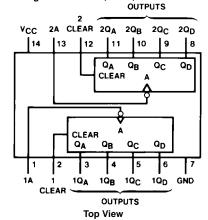
Ordering Code:

Order Number	Package	Package Description				
	Number	l ackage bescription				
MM74HC393M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow				
MM74HC393SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide				
MM74HC393MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide				
MM74HC393N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide				

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code. Pb-Free package per JEDEC J-STD-020B.

Connection Diagram





Absolute Maximum Ratings (Note 2)

(Note 1) Supply Voltage (V_{CC}) -0.5 to +7.0V DC Input Voltage (V_{IN}) -1.5 to $V_{CC} + 1.5V$ DC Output Voltage (V_{OUT}) -0.5 to V_{CC} +0.5VClamp Diode Current (I_{IK}, I_{OK}) ±20 mA DC Output Current, per pin (I_{OUT}) $\pm 25~\text{mA}$ DC V_{CC} or GND Current, per pin (I_{CC}) ±50 mA

Storage Temperature Range (T_{STG}) $-65^{\circ}C$ to $+150^{\circ}C$ Power Dissipation (P_D) (Note 3)

S.O. Package only Lead Temperature (T_L)

(Soldering 10 seconds)

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	-40	+85	°C
Input Rise or Fall Times			
$(t_r, t_f) V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	T _A = -55 to 125°C	Units
Syllibol			*CC	Тур		Guaranteed L	imits	Units
V _{IH}	Minimum HIGH Level		2.0V		1.5	1.5	1.5	V
	Input Voltage		4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V _{IL}	Maximum LOW Level		2.0V		0.5	0.5	0.5	V
	Input Voltage		4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V _{OH}	Minimum HIGH Level	$V_{IN} = V_{IH}$ or V_{IL}						
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	5.7	5.48	5.34	5.2	V
V _{OL}	Maximum LOW Level	$V_{IN} = V_{IH}$ or V_{IL}						
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	0.2	0.26	0.33	0.4	V
I _{IN}	Maximum Input	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μА
	Current							
Icc	Maximum Quiescent	$V_{IN} = V_{CC}$ or GND	6.0V		8.0	80	160	μΑ
	Supply Current	$I_{OUT} = 0 \mu A$						

600 mW

500 mW

260°C

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage curvature of the V_{IH} value at V_{IH} value rent (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

 $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

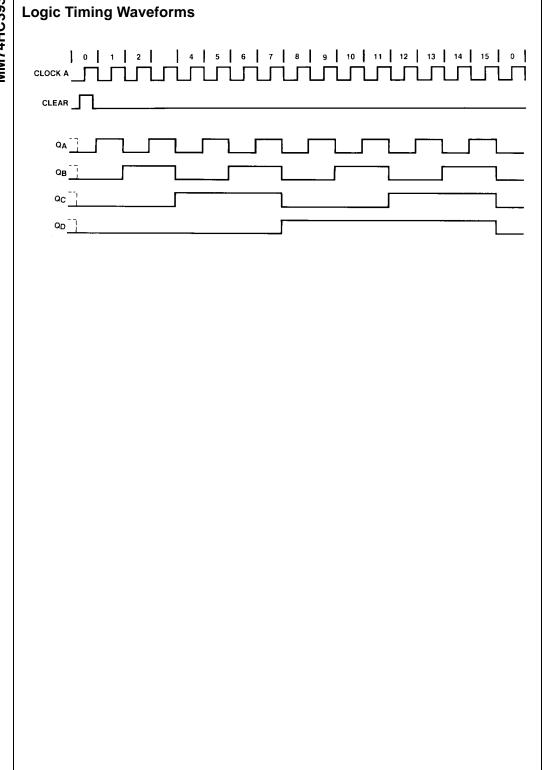
Symbol	Parameter	Conditions	Тур	Guaranteed	Units	
- Cymbol	i didilictor	Conditions	.,,,,	Limit	Jints	
f _{MAX}	Maximum Operating Frequency		50	30	MHz	
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Clock A to Q _A		13	20	ns	
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Clock A to QB		19	35	ns	
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Clock A to Q _C		23	42	ns	
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Clock A to Q _D		27	50	ns	
t _{PHL}	Maximum Propagation Delay, Clear to any Q		15	28	ns	
t _{REM}	Minimum Removal Time		-2	5	ns	
t _W	Minimum Pulse Width Clear or Clock		10	16	ns	

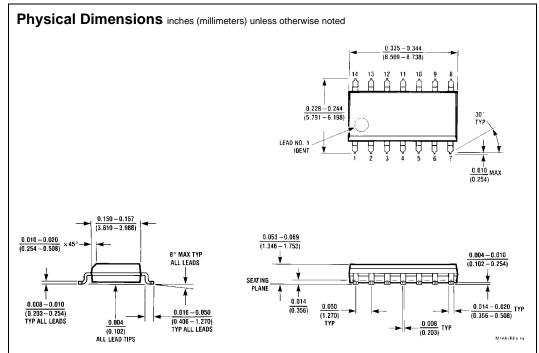
AC Electrical Characteristics

 $C_L = 50$ pF, $t_f = t_f = 6$ ns (unless otherwise specified)

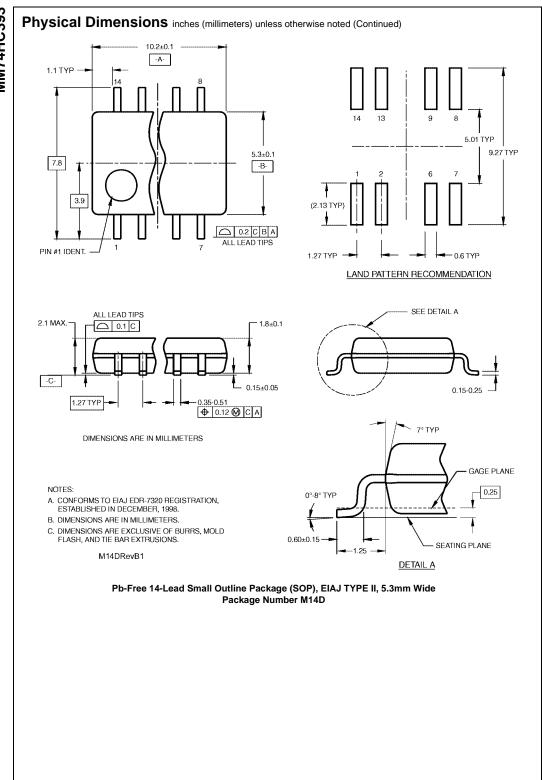
Symbol	Parameter	Conditions	V _{CC}	T _A =	= 25°C	T _A = -40 to 85°C	T _A = -55 to 125°C	Units
		Conditions	*CC	Тур		Guaranteed Limits		Ullits
f _{MAX}	Maximum Operating		2.0V		5	4	3	
	Frequency		4.5V	İ	27	21	18	MHz
			6.0V	1	31	24	20	MHz
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	45	120	150	180	ns
	Delay Clock A to Q _A		4.5V	15	24	30	35	ns
			6.0V	13	21	26	31	ns
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	68	190	240	285	ns
	Delay Clock A to Q _B		4.5V	23	38	47	57	ns
			6.0V	20	32	40	48	ns
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	90	240	300	360	ns
	Delay Clock A to Q _C		4.5V	30	48	60	72	ns
			6.0V	26	41	51	61	ns
$t_{\rm PHL},t_{\rm PLH}$	Maximum Propagation Delay		2.0V	100	290	360	430	ns
	Clock to Q _D		4.5V	35	58	72	87	ns
			6.0V	30	50	62	75	ns
t _{PHL}	Maximum Propagation		2.0V	54	165	210	250	ns
	Delay Clear to any Q		4.5V	18	33	41	49	ns
			6.0V	15	28	35	42	ns
t _{REM}	Minimum Clear		2.0V		25	25	25	ns
	Removal Time		4.5V	İ	5	5	5	ns
			6.0V	İ	5	5	5	ns
t _W	Minimum Pulse Width		2.0V	30	80	100	120	ns
	Clear or Clock		4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t _{THL} , t _{TLH}	Maximum Output		2.0V	30	75	95	110	ns
	Rise and Fall Time		4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t _r , t _f	Maximum Input				1000	1000	1000	ns
	Rise and Fall Time			1	500	500	500	ns
				İ	400	400	400	ns
C _{PD}	Power Dissipation	(per counter)		42		1		pF
	Capacitance (Note 5)			1				
C _{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \ V_{CC}^2 f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \ V_{CC} f + I_{CC}$.

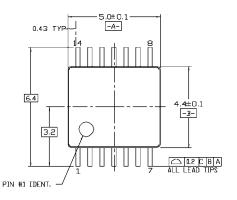


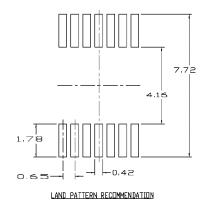


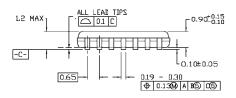
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





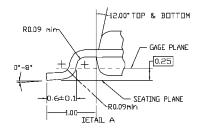




NOTES:

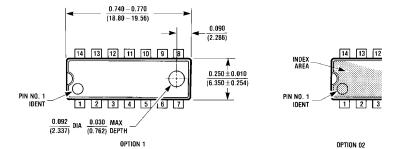
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
 D. DIMENSIONING AND TOLERANCES PER ANSI Y14-5M, BY

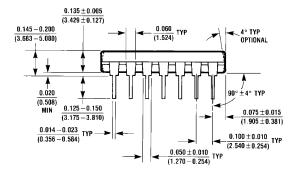
MTC14revD

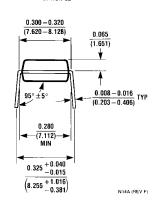


14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)







14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com