

STD840DN40

Dual NPN high voltage transistors in a single package

Datasheet — production data

Features

- Low V_{CE(sat)}
- Simplified circuit design
- Reduced component count
- Fast switching speed

Applications

- Compact fluorescent lamp (CFL) 220 V mains
- Electronic ballast for fluorescent lighting



This device is a dual NPN high voltage power transistor manufactured using multi-epitaxial planar technology. It is housed in a dual-island DIP-8 package, with separated terminals for a high degree of mounting flexibility.

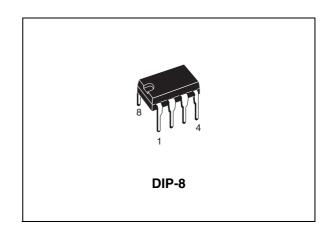


Figure 1. Internal schematic diagram

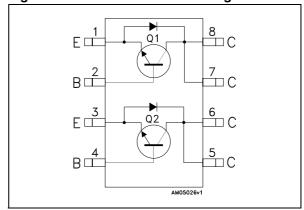


Table 1. Device summary

Order code	Marking	Package	Packaging
STD840DN40	D840DN40	DIP-8	Tube

Electrical ratings STD840DN40

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CBO}	Collector-base voltage (I _E = 0)	700	V
V _{CEO}	Collector-emitter voltage (I _B = 0)	400	V
V _{EBO}	Emitter-base voltage ($I_C = 0$, $I_B = 1.5 \text{ A}$, $t_p < 10 \text{ ms}$)	V _{(BR)EBO}	V
I _C	Collector current	4	Α
I _{CM}	Collector peak current (t _P < 5 ms)	8	Α
I _B	Base current	1.5	Α
I _{BM}	Base peak current (t _P < 5 ms)	3	Α
D.	Total dissipation at $T_{amb} = 25$ °C single transistor	3	W
P _{TOT}	Total dissipation at T _{case} = 25 °C single transistor	45	W
T _{STG}	Storage temperature	-65 to 150	°C
T_J	Max. operating junction temperature	150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R _{thJA} ⁽¹⁾	Thermal resistance junction-ambient (single transistor)	42	°C/W
R _{thJC}	Thermal resistance junction-case (single transistor)	2.7	°C/W

^{1.} Device mounted on PCB area of 25 mm².

2 Electrical characteristics

 T_{case} = 25 °C unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions		Min.	Тур.	Max.	Unit
I _{CES}	Collector cut-off current (V _{BE} = 0)	V _{CE} = 700 V V _{CE} = 700 V T _c =	125 °C			100 500	μ Α μ Α
I _{CEO}	Collector cut-off current (I _B = 0)	V _{CE} = 400 V				250	μΑ
V _{(BR)EBO}	Emitter-base breakdown voltage (I _C = 0)	I _E = 10 mA		9		18	٧
V _{CEO(sus)} ⁽¹⁾	Collector-emitter sustaining voltage (I _B = 0)	I _C = 10 mA		400			V
V _{CE(sat)} ⁽¹⁾	Collector-emitter saturation voltage		$I_B = 0.2 A$ $I_B = 0.4 A$			0.5 1	V V
V _{BE(sat)} ⁽¹⁾	Base-emitter saturation voltage		$I_B = 0.2 A$ $I_B = 0.4 A$			1.2 1.3	V V
h _{FE} ⁽¹⁾	DC current gain	•	V _{CE} = 5 V V _{CE} = 5 V	10 8		24	
V _F	Diode forward voltage	I _F = 1 A				2.5	٧
t _s	Resistive load Storage time Fall time	$I_{C} = 1 \text{ A}$ $I_{B1} = V_{CC} = 125 \text{ V}$ t_{i}			2.5 0.2		μs μs

^{1.} Pulse test: pulse duration ≤300 µs, duty cycle ≤ 2 %.

2.1 Electrical characteristics (curves)

Figure 2. DC current gain $(V_{CE} = 1 V)$

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Figure 3. DC current gain $(V_{CE} = 5 V)$

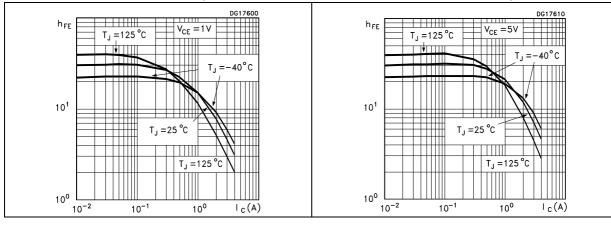


Figure 4. Collector-emitter saturation voltage Figure 5. Base-emitter saturation voltage

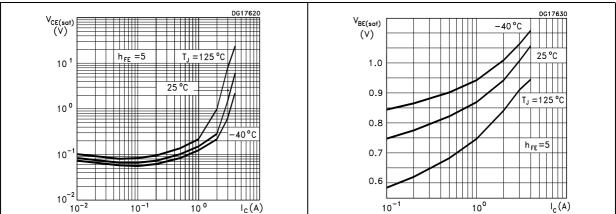
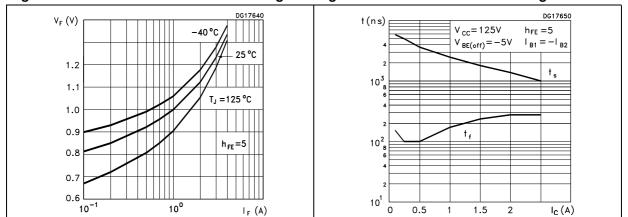


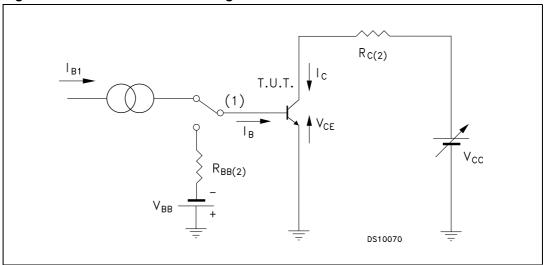
Figure 6. Freewheel diode forward voltage Figure 7. Resistive load switching time



STD840DN40 Test circuit

3 Test circuit

Figure 8. Resistive load switching test circuit



- 1. Fast electronic switch
- 2. Non-inductive resistor

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK[®] is an ST trademark.

Table 5. DIP-8 mechanical data

Dim.		mm.	
	Min.	Тур.	Max.
А			4.80
A1	0.50		
A2	3.10		3.50
A3	1.40		1.60
b	0.38		0.55
b1	0.38		0.51
b2	1.47		1.57
b3	0.89		1.09
С	0.21		0.35
c1	0.20		0.30
D	9.10		9.30
D1	0.13		
E	7.62		8.25
E1	6.25		6.45
е		2.54	
eA		7.62	
eB	7.62		10.90
eC	0		1.52
L	2.92		3.81

GC GAUGE PLANE 0.38 eЯ eВ \Box エ E1 A 1 A3 8145726_A

Figure 9. Drawing dimension DIP-8

Revision history STD840DN40

5 Revision history

Table 6. Document revision history

Date	Revision	Changes
18-Nov-2009	1	Initial release.
16-Apr-2010	2	Inserted P _{TOT} and R _{thJA} values <i>Table 2</i> and <i>Table 3 on page 2</i> .
23-Oct-2012	3	Modified P _{TOT} and R _{thJA} values in <i>Table 2</i> and <i>Table 3 on page 2</i> . Minor text changes.

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