FAIRCHILD
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MM74HC273
Octal D-Type Flip-Flops with Clear

General Description

The MM74HC273 edge triggered flip-flops utilize advanced silicon-gate CMOS technology to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 8 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the LOW-to-HIGH transition of the CLOCK input. The CLEAR input when LOW, sets all outputs to a low state.

Each output can drive 10 low power Schottky TTL equivalent loads. The MM74HC273 is functionally as well as pin compatible to the 74LS273. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

■ Typical propagation delay: 18 ns
■ Wide operating voltage range
■ Low input current: 1 µA maximum
■ Low quiescent current: 80 µA (74 Series)
■ Output drive: 10 LS-TTL loads

Ordering Code:

Order Number	Package Number	Package Description
MM74HC273WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC273MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC273N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Top View

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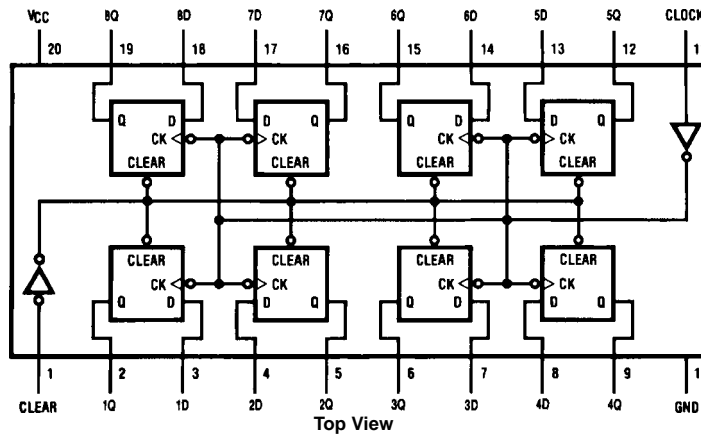
Truth Table

(Each Flip-Flop)

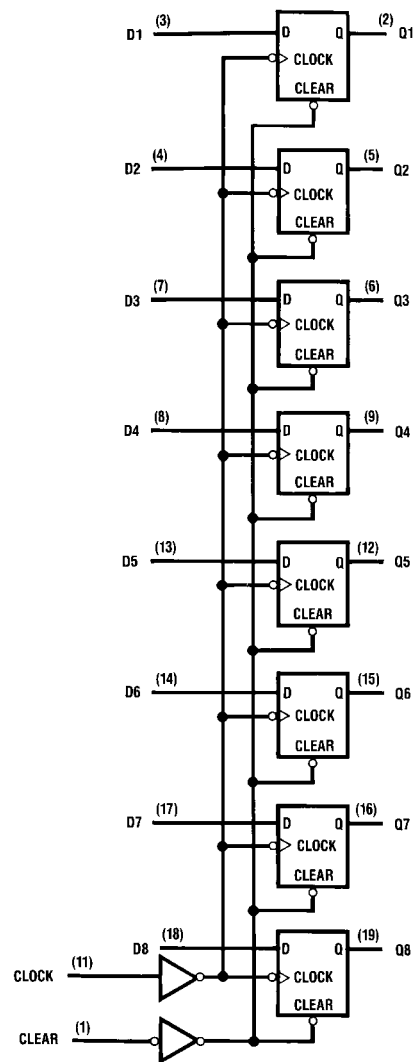| Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = HIGH Level (Steady State)
L = LOW Level (Steady State)
X = Don't Care
↑ = Transition from LOW-to-HIGH level
Q_0 = The level of Q before the indicated steady state input conditions were
established

Logic Diagram

Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	$T_A = −40$ to $85°C$	$T_A = −55$ to $125°C$	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level		2.0V		1.5	1.5	1.5	V
	Input Voltage		4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level		2.0V		0.5	0.5	0.5	V
	Input Voltage		4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level	$V_{IN} = V_{IH}$ or V_{IL}						
	Output Voltage	$|I_{OUT}| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$|I_{OUT}| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level	$V_{IN} = V_{IH}$ or V_{IL}						
	Output Voltage	$|I_{OUT}| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$|I_{OUT}| \leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\ \mu A$	6.0V		8	80	160	μA

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.
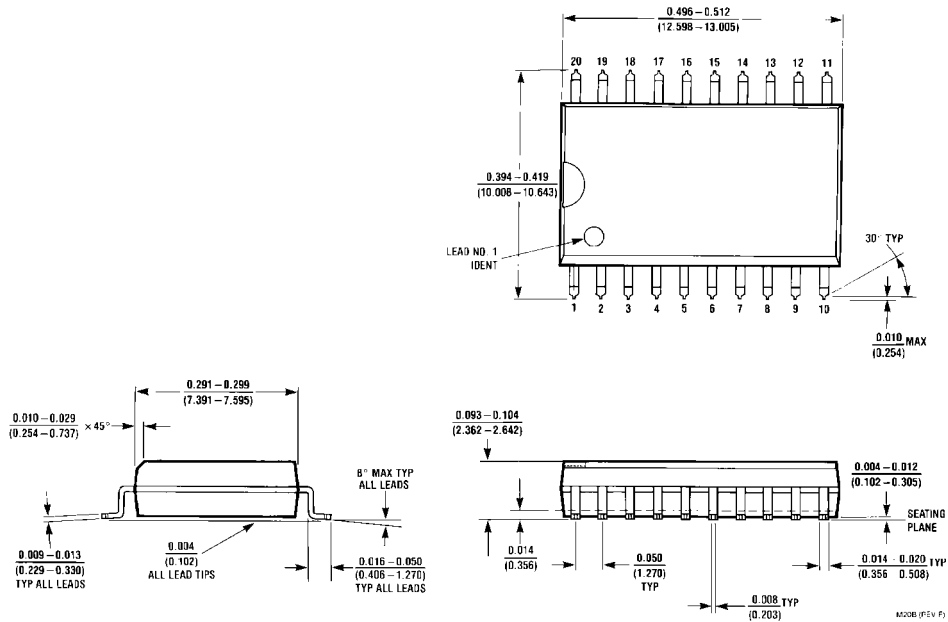
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AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		18	27	ns
t_{PHL}	Maximum Propagation Delay, Clear to Output		18	27	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_s	Minimum Setup Time Data to Clock		10	20	ns
t_H	Minimum Hold Time Clock to Data		−2	0	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	ns

AC Electrical Characteristics

C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C Typ	T_A = 25°C Guaranteed Limits	T_A = −40 to 85°C	T_A = −55 to 125°C	Units
f_{MAX}	Maximum Operating Frequency		2.0V	16	5	4	3	MHz
			4.5V	74	27	21	18	MHz
			6.0V	78	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		2.0V	38	135	170	205	ns
			4.5V	14	27	34	41	ns
			6.0V	12	23	29	35	ns
t_{PHL}	Maximum Propagation Delay, Clear to Output		2.0V	42	135	170	205	ns
			4.5V	19	27	34	41	ns
			6.0V	18	23	29	35	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V	0	25	32	37	ns
			4.5V	0	5	6	7	ns
			6.0V	0	4	5	6	ns
t_s	Minimum Setup Time Data to Clock		2.0V	26	100	125	150	ns
			4.5V	7	20	25	30	ns
			6.0V	5	17	21	25	ns
t_H	Minimum Hold Time Clock to Data		2.0V	−15	0	0	0	ns
			4.5V	−6	0	0	0	ns
			6.0V	−4	0	0	0	ns
t_W	Minimum Pulse Width Clock or Clear		2.0V	34	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	10	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	28	75	95	110	ns
			4.5V	11	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		45				pF
C_{IN}	Maximum Input Capacitance			7	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted

0.496 − 0.512
(12.598 − 13.005)

20 19 18 17 16 15 14 13 12 11

0.394 − 0.419
(10.008 − 10.643)

LEAD NO. 1
IDENT

1 2 3 4 5 6 7 8 9 10

30° TYP

0.010 MAX
(0.254)

0.291 − 0.299
(7.391 − 7.595)

0.010 − 0.029
(0.254 − 0.737) × 45°

8° MAX TYP
ALL LEADS

0.009 − 0.013
(0.229 − 0.330)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.093 − 0.104
(2.362 − 2.642)

0.004 − 0.012
(0.102 − 0.305)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.014 − 0.020 TYP
(0.356 − 0.508)

0.008 TYP
(0.203)

M20B (REV F)

20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

12.6±0.10

-A-

0.40 TYP

20   11

7.8

3.9

5.3±0.10

-B-

⌒ 0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.   1   10

LAND PATTERN RECOMMENDATION

20 19   12 11

5.01 TYP

9.27 TYP

1   2   9 10

(2.13 TYP)

1.27 TYP   0.6 TYP

ALL LEAD TIPS

⌒ 0.1 C

2.1 MAX.

-C-

1.8±0.1

0.15±0.05

1.27 TYP   0.35-0.51

⊕ 0.12 Ⓜ C A

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.15-0.25

7° TYP

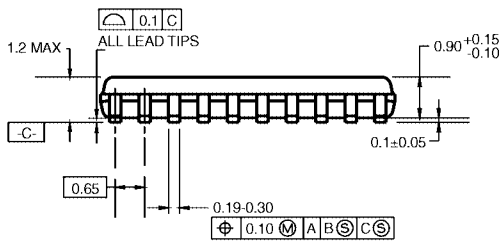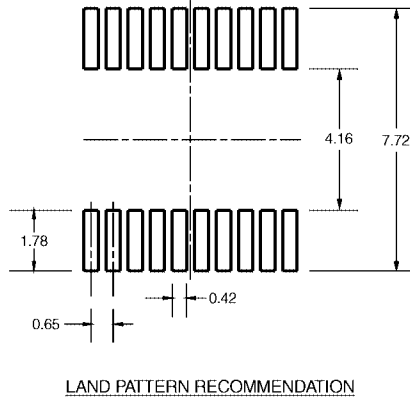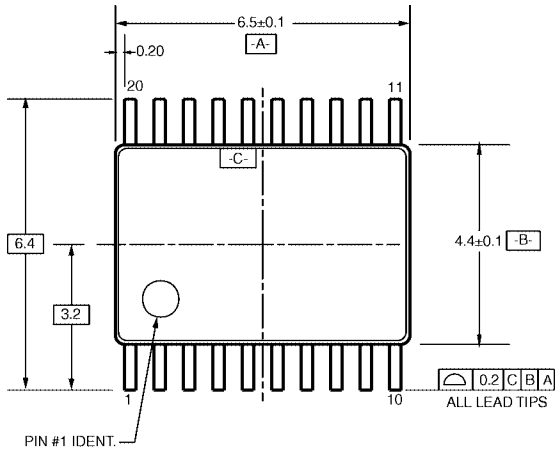GAGE PLANE

0°-8° TYP   0.25

0.60±0.15   SEATING PLANE

1.25

DETAIL A

NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
   ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
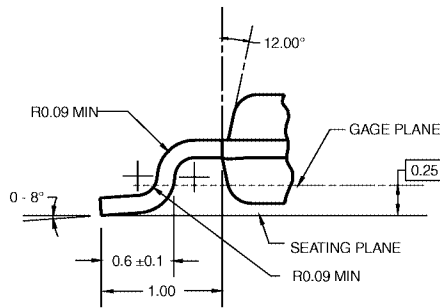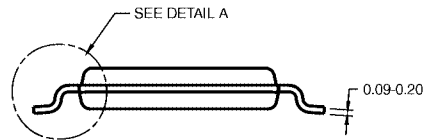C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
   FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

6.5±0.1 -A-
0.20
20
11
-C-
6.4
4.4±0.1 -B-
3.2
1
10
⌒ 0.2 C B A
ALL LEAD TIPS
PIN #1 IDENT.

LAND PATTERN RECOMMENDATION
4.16 7.72
1.78
0.65
0.42

⌒ 0.1 C
ALL LEAD TIPS
1.2 MAX
0.90 +0.15 -0.10
-C-
0.1±0.05
0.65
0.19-0.30
⊕ 0.10 Ⓜ A BⓈ CⓈ

DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

SEE DETAIL A
0.09-0.20
12.00°
R0.09 MIN
GAGE PLANE
0.25
0 - 8°
SEATING PLANE
0.6 ±0.1
R0.09 MIN
1.00
DETAIL A

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.092 × 0.030
(2.337 × 0.762)
MAX DP

PIN NO. 1 IDENT

OPTION 1

1.013−1.040
(25.73−26.42)

0.260 ±0.005
(6.604 −0.127)

0.032 ±0.005
(0.813 ±0.127)
RAD

PIN NO. 1 IDENT

OPTION 2

0.280
(7.112)
MIN

0.300−0.320
(7.620−8.128)

0.065
(1.651)

95° ± 5°

0.009−0.015
(0.229−0.381)
TYP

0.060 ±0.005
(1.524 ±0.127)

0.325 +0.040 −0.015
(8.255 +1.016 −0.381)

0.090
(2.286)

0.060 NOM
(1.524)
TYP

0.040
(1.016)
TYP

OPTION 2
4° (4X)

0.100 ± 0.010
(2.540 ± 0.254)

0.018 ± 0.003
(0.457 ± 0.076)

90°± 0.004°

0.130 0.005
(3.302 0.127)

0.145−0.200
(3.683−5.080)

0.125−0.140
(3.175−3.556)

0.020
(0.508)
MIN

N20A (REV G)

20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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