#### INTEGRATED CIRCUITS

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

# 74HC/HCT75 Quad bistable transparent latch

Product specification
File under Integrated Circuits, IC06

December 1990





#### **74HC/HCT75**

#### **FEATURES**

- Complementary Q and Q outputs
- V<sub>CC</sub> and GND on the centre pins
- · Output capability: standard
- I<sub>CC</sub> category: MSI

#### **GENERAL DESCRIPTION**

The 74HC/HCT75 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT75 have four bistable latches. The two latches are simultaneously controlled by one of two active HIGH enable inputs (LE<sub>1-2</sub> and LE<sub>3-4</sub>). When LE<sub>n-n</sub> is HIGH, the data enters the latches and appears at the nQ outputs. The nQ outputs follow the data inputs (nD) as long as LE<sub>n-n</sub> is HIGH (transparent). The data on the nD inputs one set-up time prior to the HIGH-to-LOW transition of the LE<sub>n-n</sub> will be stored in the latches. The latched outputs remain stable as long as the LE<sub>n-n</sub> is LOW.

#### **QUICK REFERENCE DATA**

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$ 

SYMBOL	PARAMETER	CONDITIONS	TYPI	UNIT	
	PARAMETER	CONDITIONS	НС	нст	UNII
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay	$C_L = 15 \text{ pF}; V_{CC} = 5 \text{ V}$			
	nD to nQ, $n\overline{Q}$		11	12	ns
	$LE_{n-n}$ to nQ, n $\overline{Q}$		11	11	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per latch	notes 1 and 2	42	42	pF

#### **Notes**

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$ 

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is  $V_I = GND$  to  $V_{CC}$ 

For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 \text{ V}$ 

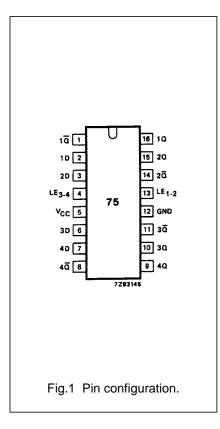
#### **ORDERING INFORMATION**

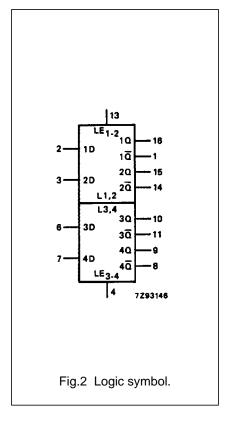
See "74HC/HCT/HCU/HCMOS Logic Package Information".

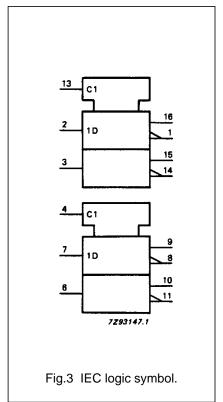
# 74HC/HCT75

#### **PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 14, 11, 8	1Q to 4Q	complementary latch outputs
2, 3, 6, 7	1D to 4D	data inputs
4	LE <sub>3-4</sub>	latch enable input, latches 3 and 4 (active HIGH)
5	V <sub>CC</sub>	positive supply voltage
12	GND	ground (0 V)
13	LE <sub>1-2</sub>	latch enable input, latches 1 and 2 (active HIGH)
16, 15, 10, 9	1Q to 4Q	latch outputs







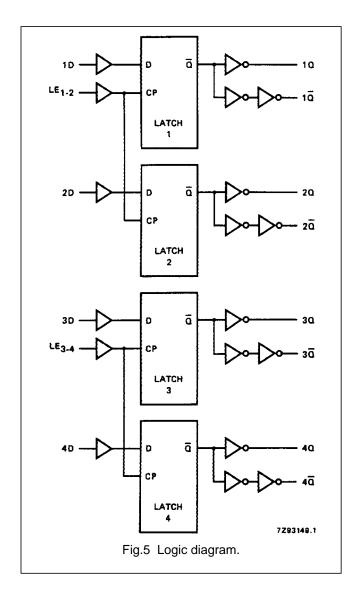
### 74HC/HCT75

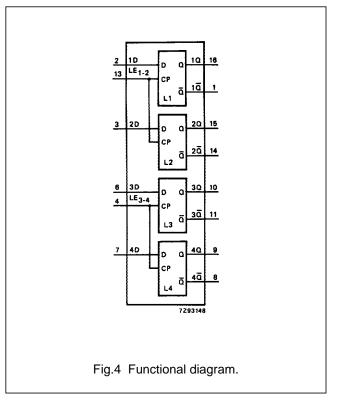
#### **FUNCTION TABLE**

OPERATING	INPUT	S	OUTPUTS			
MODES	LE <sub>n-n</sub>	nD	nQ	nQ		
data enabled	Н	L	L	Н		
uata eriabieu	Н	Н	Н	L		
data latched	L	Х	q	q		

#### **Notes**

- 1. H = HIGH voltage level
  - L = LOW voltage level
  - $\label{eq:q} q = \text{lower case letters indicate the state of the} \\ \text{referenced output one set-up time prior} \\ \text{to the HIGH-to-LOW LE}_{\text{n-n}} \text{ transition} \\$
  - X = don't care





Philips Semiconductors Product specification

# Quad bistable transparent latch

**74HC/HCT75** 

#### DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

#### **AC CHARACTERISTICS FOR 74HC**

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$ 

	PARAMETER		T <sub>amb</sub> (°C)							TEST CONDITIONS	
SYMBOL			74HC						UNIT		
			+25			-40 to+85		-40 to+125		V <sub>CC</sub>	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		(•)	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nD to nQ		33 12 10	110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nD to nQ		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE <sub>n-n</sub> to nQ		33 12 10	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig.8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $LE_{n-n} \text{ to } n \overline{Q}$		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7
t <sub>W</sub>	enable pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>su</sub>	set-up time nD to LE <sub>n-n</sub>	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.9
th	hold time nD to LE <sub>n-n</sub>	3 3 3	-8 -3 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig.9

Philips Semiconductors Product specification

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74HC/HCT75

#### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

#### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nD	0.75
LE <sub>n-n</sub>	1.00

#### **AC CHARACTERISTICS FOR 74HCT**

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$ 

SYMBOL	PARAMETER		T <sub>amb</sub> (°C)							TEST CONDITIONS	
			74HCT								
		+25			-40 to +85		-40 to +125		UNIT	V <sub>CC</sub>	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		(-,	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nD to nQ		15	28		35		42	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nD to nQ		15	28		35		42	ns	4.5	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE <sub>n-n</sub> to nQ		13	28		35		42	ns	4.5	Fig.8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE <sub>n-n</sub> to nQ		15	30		38		45	ns	4.5	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7
t <sub>W</sub>	enable pulse width HIGH	16	4		20		24		ns	4.5	Fig.8
t <sub>su</sub>	set-up time nD to LE <sub>n-n</sub>	12	4		15		18		ns	4.5	Fig.9
t <sub>h</sub>	hold time nD to LE <sub>n-n</sub>	3	-2		3		3		ns	4.5	Fig.9

#### 74HC/HCT75

#### **AC WAVEFORMS**

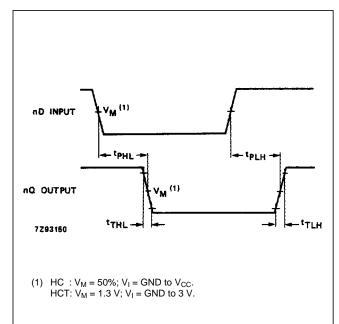
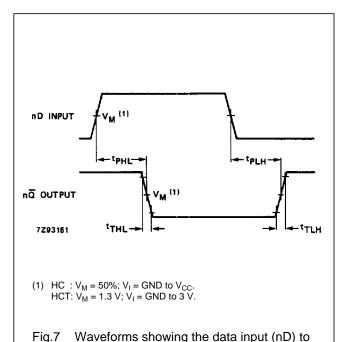
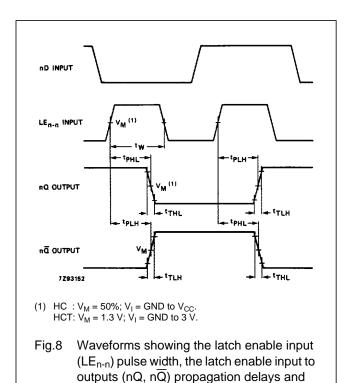


Fig.6 Waveforms showing the data input (nD) to output (nQ) propagation delays and the output transition times.

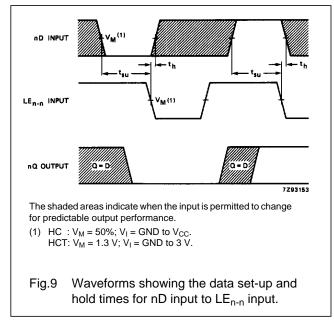


output (nQ) propagation delays and the

output transition times.



the output transition times.



#### **PACKAGE OUTLINES**

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".