## 74HC237

# 3-to-8 line decoder, demultiplexer with address latches Rev. 5 — 9 December 2011 Product da

Product data sheet

#### 1. **General description**

The 74HC237 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). The 74HC237 is specified in compliance with JEDEC standard no. 7A.

The 74HC237 is a 3-to-8 line decoder, demultiplexer with latches at the three address inputs (An). The 74HC237 essentially combines the 3-to-8 decoder function with a 3-bit storage latch. When the latch is enabled (LE = LOW), the 74HC237 acts as a 3-to-8 active LOW decoder. When the latch enable (LE) goes from LOW-to-HIGH, the last data present at the inputs before this transition, is stored in the latches. Further address changes are ignored as long as LE remains HIGH. The output enable input (E1 and E2) controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless E1 is LOW and E2 is HIGH. The 74HC237 is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

#### Features and benefits 2.

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active HIGH mutually exclusive outputs
- Low-power dissipation
- ESD protection:
  - ♦ HBM JESD22-A114F exceeds 2 000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

#### Ordering information 3.

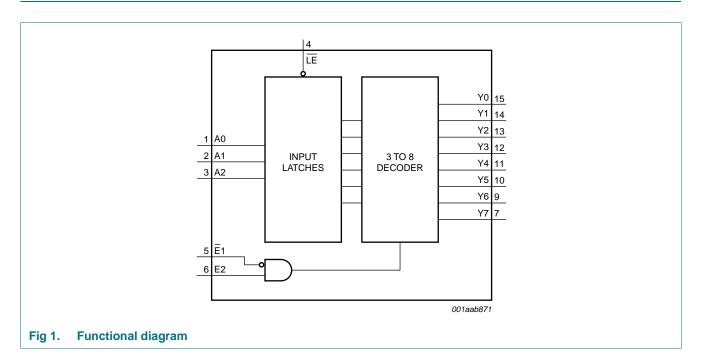
Table 1. **Ordering information** 

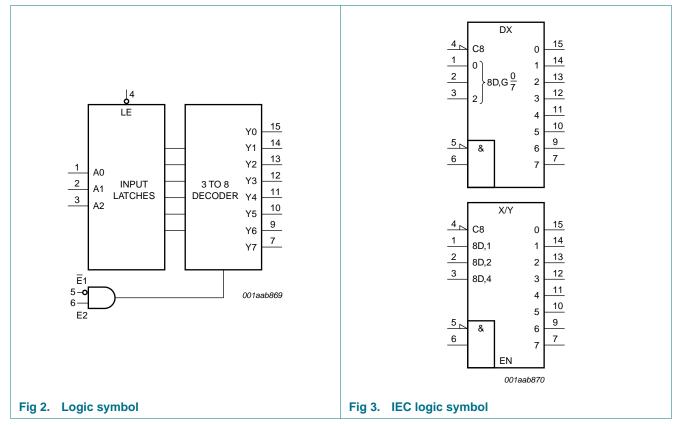
Type number	Package	Package											
	Temperature range	Name	Description	Version									
74HC237N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4									
74HC237D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1									
74HC237DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1									



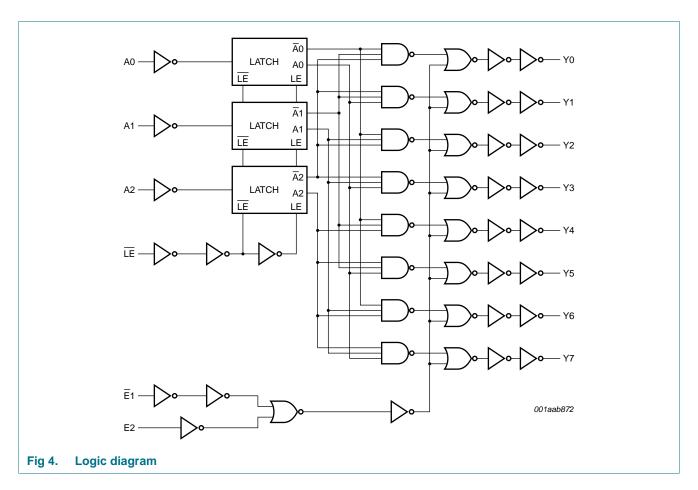
3-to-8 line decoder, demultiplexer with address latches

### 4. Functional diagram



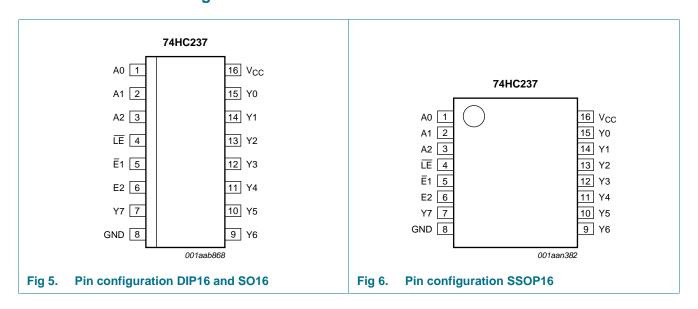


### 3-to-8 line decoder, demultiplexer with address latches



### 5. Pinning information

### 5.1 Pinning



74HC237

### 3-to-8 line decoder, demultiplexer with address latches

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0 to A2	1, 2, 3	data input
LE	4	latch enable input (active LOW)
E1	5	data enable input 1 (active LOW)
E2	6	data enable input 2 (active HIGH)
Y0 to Y7	15, 14, 13, 12, 11,	10, 9, 7 output
GND	8	ground (0 V)
V <sub>CC</sub>	16	supply voltage

### 6. Functional description

Table 3: Function table

Enabl	le		Input			Outp	ut						
LE	<u>E</u> 1	E2	A0	A1	A2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Н	L	Н	X	Χ	X	stable	)	'	'	'	'	'	'
Χ	Н	X	X	Χ	Χ	L	L	L	L	L	L	L	L
Χ	Х	L	X	Χ	Х	L	L	L	L	L	L	L	L
L	L	Н	L	L	L	Н	L	L	L	L	L	L	L
			Н	L	L	L	Н	L	L	L	L	L	L
			L	Н	L	L	L	Н	L	L	L	L	L
			Н	Н	L	L	L	L	Н	L	L	L	L
			L	L	Н	L	L	L	L	Н	L	L	L
			Н	L	Н	L	L	L	L	L	Н	L	L
			L	Н	Н	L	L	L	L	L	L	Н	L
			Н	Н	Н	L	L	L	L	L	L	L	Н

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

### 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$	-	±20	mA
I <sub>OK</sub>	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	-	±20	mA
I <sub>O</sub>	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-	±25	mA
I <sub>CC</sub>	supply current		-	+50	mA
$I_{GND}$	ground current		-	-50	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	DIP16 package	<u>[1]</u> _	750	mW
		SO16 and SSOP16 packages	[2] -	500	mW
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- [1] For DIP16 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.
- [2] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C. For SSOP16 package:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

### 8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	6.0	V
VI	input voltage		0	-	$V_{CC}$	V
Vo	output voltage		0	-	$V_{CC}$	V
T <sub>amb</sub>	ambient temperature	-40	+25	+125	°C	
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 2.0 \text{ V}$	-	-	625	ns/V
		$V_{CC} = 4.5 \text{ V}$	-	1.67	139	ns/V
		$V_{CC} = 6.0 \text{ V}$	-	-	83	ns/V

### 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -		T <sub>amb</sub> = - +12	Unit	
			Min	Тур	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level	$V_{CC} = 2.0 \text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0 \text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0 \text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -20 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20 \mu A$ ; $V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20 \mu A$ ; $V_{CC} = 6.0 \text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0 \text{ mA}$ ; $V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
$V_{OL}$	LOW-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	$I_O = 20 \mu A; V_{CC} = 2.0 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A$ ; $V_{CC} = 6.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}$ ; $V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_{O} = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V

### 3-to-8 line decoder, demultiplexer with address latches

 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions			T <sub>amb</sub> = -40 °C to +85 °C		T <sub>amb</sub> = - +12	Unit		
			Min	Min Typ Max		Min	Max	Min	Max	
I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80	-	160	μΑ
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

### 10. Dynamic characteristics

#### Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit see <u>Figure 10</u>.

Symbol	Parameter	Conditions		T <sub>an</sub>	<sub>nb</sub> = 25	°C		= –40 °C ⋅85 °C	T <sub>amb</sub> = to +1	-40 °C 25 °C	Unit
				Min	Тур	Max	Min	Max	Min	Max	
t <sub>pd</sub>	propagation	An to Yn; see Figure 7	<u>[1]</u>								
	delay	$V_{CC} = 2.0 \text{ V}$		-	52	160	-	200	-	240	ns
		$V_{CC} = 4.5 \text{ V}$		-	19	32	-	40	-	48	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$		-	16	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$		-	15	27	-	34	-	41	ns
		LE to Yn; see Figure 7	<u>[1]</u>								
		$V_{CC} = 2.0 \text{ V}$		-	61	190	-	240	-	285	ns
		$V_{CC} = 4.5 \text{ V}$		-	22	38	-	48	-	57	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$		-	19	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$		-	18	32	-	41	-	48	ns
		E1to Yn; see Figure 8	<u>[1]</u>								
		$V_{CC} = 2.0 \text{ V}$		-	47	145	-	180	-	220	ns
		$V_{CC} = 4.5 \text{ V}$		-	17	29	-	36	-	44	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$		-	14	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$		-	14	25	-	31	-	38	ns
		E2 to Yn; see Figure 7	[1]								
		$V_{CC} = 2.0 \text{ V}$		-	47	145	-	180	-	220	ns
		$V_{CC} = 4.5 \text{ V}$		-	17	29	-	36	-	44	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$		-	14	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$		-	14	25	-	31	-	38	ns
t <sub>t</sub>	transition time	Yn; see <u>Figure 7</u> and <u>Figure 8</u>	[2]								
		$V_{CC} = 2.0 \text{ V}$		-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V		-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0 \text{ V}$		-	6	13	-	16	-	19	ns

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 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit see Figure 10.

Symbol	Parameter	Conditions	T <sub>ar</sub>	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +85 °C		T <sub>amb</sub> = -40 °C to +125 °C	
			Min	Тур	Max	Min	Max	Min	Max	
$t_{W}$	pulse width	LE HIGH; see Figure 9								
		V <sub>CC</sub> = 2.0 V	50	11	-	65	-	75	-	ns
		V <sub>CC</sub> = 4.5 V	10	4	-	13	-	15	-	ns
		$V_{CC} = 6.0 \text{ V}$	9	3	-	11	-	13	-	ns
t <sub>su</sub> set-up time		An to LE; see Figure 9								
		V <sub>CC</sub> = 2.0 V	50	6	-	65	-	75	-	ns
		V <sub>CC</sub> = 4.5 V	10	2	-	13	-	15	-	ns
		V <sub>CC</sub> = 6.0 V	9	2	-	11	-	13	-	ns
t <sub>h</sub>	hold time	An to LE; see Figure 9					-			
		V <sub>CC</sub> = 2.0 V	30	3	-	40	-	45	-	ns
		V <sub>CC</sub> = 4.5 V	6	1	-	8	-	9	-	ns
		V <sub>CC</sub> = 6.0 V	5	1	-	7	-	8	-	ns
C <sub>PD</sub>	power dissipation capacitance	$C_L = 50 \text{ pF}; f = 1 \text{ MHz};$ $V_I = \text{GND to } V_{CC}$	-	60	-	-	-	-	-	pF

<sup>[1]</sup>  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;

fo = output frequency in MHz;

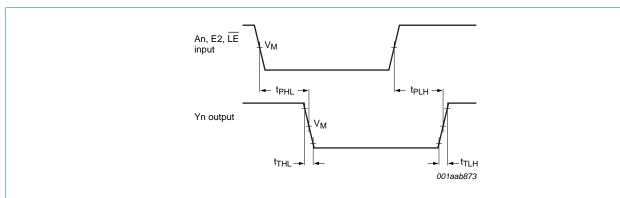
C<sub>L</sub> = output load capacitance in pF;

 $V_{CC}$  = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$ 

### 11. Waveforms



Measurement points are given in <u>Table 8</u>.

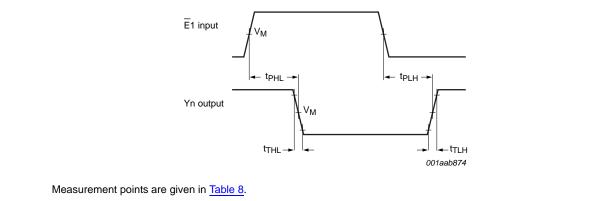
 $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical voltage output levels that occur with the output load.

Fig 7. Propagation delay input (An) and enable inputs (E2, LE) to output (Yn) and output transition time

74HC237

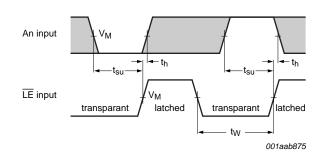
<sup>[2]</sup>  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

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V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

Fig 8. Propagation enable inputs (E1) to output (Yn) and output transition time



Measurement points are given in Table 8.

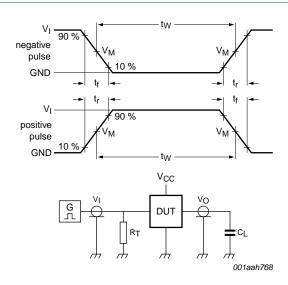
 $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical voltage output levels that occur with the output load.

Fig 9. The data input (An) to latch enable input (LE) set-up times, latch enable input (LE) to data input (An) hold times and latch enable input (LE) pulse width

Table 8. Measurement points

Туре	Input	Output
	V <sub>M</sub>	V <sub>M</sub>
74HC237	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>

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Test data is given in Table 9.

Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

 $C_L$  = Load capacitance including jig and probe capacitance.

R<sub>L</sub> = Load resistance.

S1 = Test selection switch.

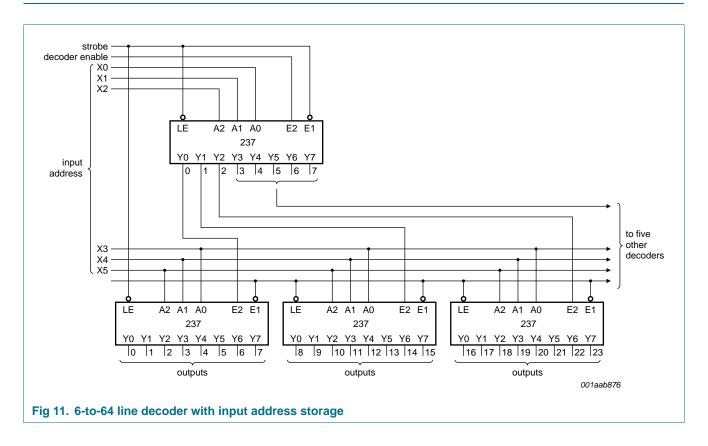
Fig 10. Test circuit for measuring switching times

Table 9. Test data

Туре	Input		Load	Test
	VI	t <sub>r</sub> , t <sub>f</sub>	CL	
74HC237	V <sub>CC</sub>	6.0 ns	15 pF, 50 pF	t <sub>PLH</sub> , t <sub>PHL</sub>

### 3-to-8 line decoder, demultiplexer with address latches

### 12. Application information



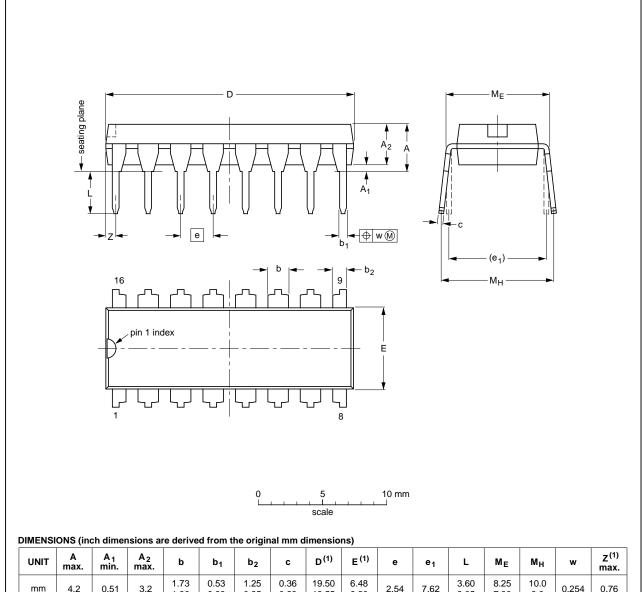
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### 3-to-8 line decoder, demultiplexer with address latches

### 13. Package outline

### DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	C	D <sup>(1)</sup>	E <sup>(1)</sup>	е	e <sub>1</sub>	L	ME	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT38-4						<del>95-01-14</del> 03-02-13

Fig 12. Package outline SOT38-4 (DIP16)

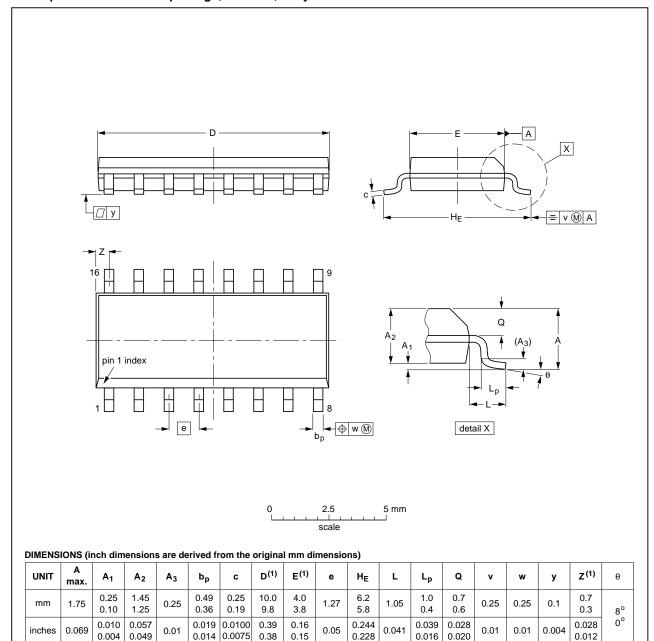
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### 3-to-8 line decoder, demultiplexer with address latches

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION ISSUE DAT	
SOT109-1	076E07	MS-012				<del>99-12-27</del> 03-02-19

Fig 13. Package outline SOT109-1 (SO16)

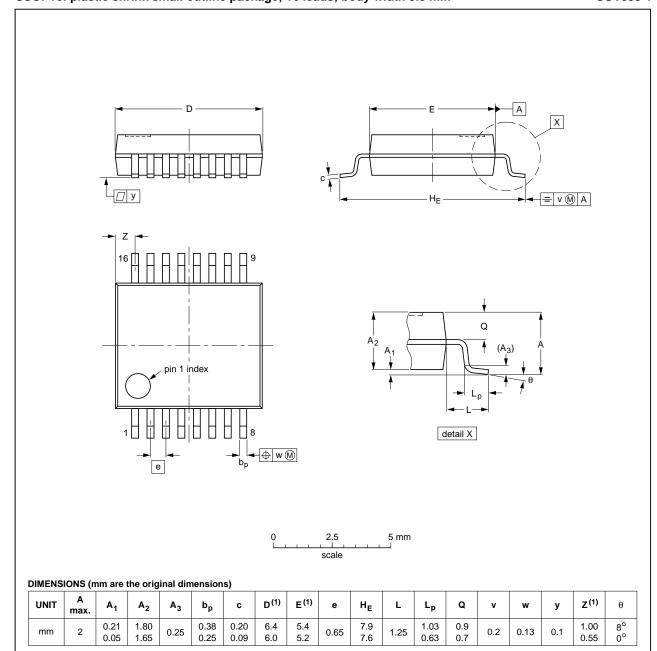
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### 3-to-8 line decoder, demultiplexer with address latches

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



#### Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE	REFERENCES			EUROPEAN	IOOUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT338-1		MO-150				<del>99-12-27</del> 03-02-19

Fig 14. Package outline SOT338-1 (SSOP16)

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### 3-to-8 line decoder, demultiplexer with address latches

### 14. Abbreviations

#### Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

### 15. Revision history

### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC237 v.5	20111209	Product data sheet	-	74HC237 v.4
Modifications:	<ul> <li>Legal page</li> </ul>	es updated.		
74HC237 v.4	20110110	Product data sheet	-	74HC237 v.3
74HC237 v.3	20041112	Product data sheet	-	74HC_HCT237_CNV v.2
74HC_HCT237_CNV v.2	19970828	Product specification	-	74HC_HCT237 v.1
74HC_HCT237 v.1	19901201	Product specification	-	-

#### 3-to-8 line decoder, demultiplexer with address latches

### 16. Legal information

#### 16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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### 3-to-8 line decoder, demultiplexer with address latches

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3-to-8 line decoder, demultiplexer with address latches

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